TECHNICAL UNIVERSITY OF CRETE
DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING

Design of low-power low-noise integrated CMOS biosignal amplifier

DIPLOMA THESIS

Nikolaos Gkouvatsos

THESIS COMMITTEE

Associate Professor Matthias Bucher, Supervisor

Professor Konstantinos Balas

Professor Konstantinos Kalaitzakis

Chania, October 2020

Περίληψη

Σε αυτήν την εργασία θα μελετήσουμε τη διαδικασία σχεδίασης ενός ενισχυτή χαμηλής ισχύος και χαμηλού θορύβου με εφαρμογή στην ενίσχυση εγκεφαλικών σημάτων. Ο βιο-ενισχυτής υλοποιήθηκε σε CMOS τεχνολογία 90 nm έτσι ώστε να είναι κατάλληλος για ενσωμάτωση σε πολυκάναλα καταγραφικά εμφυτεύματα. Το ηλεκτρόδιο καταγραφής σημάτων του βιο-ενισχυτή συνδέεται άμεσα στην είσοδο ενός ενισχυτή χαμηλού θορύβου ο οποίος περιλαμβάνει στην ανάδρασή του έναν ολοκληρωτή Miller. Ο ολοκληρωτής, επιτυγχάνοντας μεγάλη χρονική σταθερά, προσδίδει στον βιο-ενισχυτή την ικανότητα απόρριψης ανεπιθύμητων σημάτων χαμηλών συχνοτήτων καθώς θέτει την χαμηλή συχνότητα αποκοπής του στα 121.5 Hz. Η μεγάλη χρονική σταθερά του ολοκληρωτή προκύπτει από μια δομή διοδικών τρανζίστορ που παρουσιάζει υψηλή αντίσταση και επιτρέπει την χρήση πυκνωτή μειωμένης χωρητικότητας και επιφάνειας. Η σχεδίαση του ενισχυτή υπό τους περιορισμούς που προκύπτουν από την χαμηλή τάση τροφοδοσίας της τεχνολογίας 90 nm, 1.2 V, έγινε με την μεθοδολογία του δείκτη αναστροφής (IC). Το κέρδος του ενισχυτή στη μέση ζώνη είναι 46.8 dB, το εύρος ζώνης του 10.84 kHz, ο θόρυβος στην είσοδό 5.8 μV_{rms} και η κατανάλωση 8.4 μW.

Abstract

In this work we will study the designing procedure of a low-power low-noise amplifier, with application in brain signals amplification. The bio-amplifier was implemented in a 90 nm CMOS process so that it is suitable for integration into multichannel recording implants. The recording electrode of the bio-amplifier is directly connected to the input of a low-noise amplifier which includes a Miller integrator in its feedback. The integrator, achieving a long time constant, gives the bio-amplifier the ability to reject unwanted low frequency signals as it sets its low cut-off frequency at 113.7 Hz. The large time constant of the integrator results from a structure of diode-connected transistors which employs a high resistance and allows the use of capacitors of reduced capacitance and area. The design of the amplifier under the constraints resulting from the low supply voltage of 90 nm technology, 1.2 V, was done with the inversion coefficient methodology (IC) that allows design in weak, moderate and strong inversion. The midband gain of the amplifier is 47.5 dB, its bandwidth is 10.3 kHz, the noise at the input 6 μVrms and the power dissipation 8.4 μW.

Acknowledgements

First of all, I would like to express my sincere gratitude to my supervisor Prof. Matthias Bucher for the continuous support of my thesis with his valuable knowledge and for inspiring me to engage with analog circuit design.

I would also like to thank all the members of the Electronics laboratory and especially Alexia Papadopoulou. I greatly appreciate all those hours she spent answering my questions and helping me face difficulties that arose during my thesis.

Finally, I would like to express my love to my family and my friends for their invaluable support and their thoughtfulness. These people are the greatest gift of my life.

Dedicated to my beloved family,
Vasilis, Voula, Marsia and Roumiana

Contents

Chapter 1 Introduction

Chapter 2 Biosignals

2.1 Information Flow Inside the Brain 2
2.2 Action Potentials 2
2.3 Neural Circuits 3
2.4 Action Potentials Recording Methods 4
2.5 Why Action Potentials Recording? 5
2.6 Action Potentials Amplification 5

Chapter 3 MOSFET Device

3.1 MOSFET Structure 7
3.2 MOSFET Operation 8
3.3 Regions of Operation 11

Chapter 4 Circuit Design Methodology

4.1 Channel Inversion Regions 13
4.2 Inversion Coefficient Design Methodology 14

Chapter 5 Noise

5.1 Noise in MOSFET 18
5.1.1 Flicker Noise (1/f) 18
5.1.2 Thermal Noise 19
5.1.3 Shot Noise 20
5.1.4 Substrate Noise 20
5.1.5 Generation-Recombination Noise 20
5.2 Noise in Circuits 20

Chapter 6 Bioamplifier

6.1 Two-Stage OTA 22
6.1.1 Circuit Topology 23
6.1.2 Transfer Function 25

6.1.3 Input-Referred Noise 26
6.2 Pseudoresistor 26
6.3 Miller Integrator 27
6.4 Current Mirror OTA 28
6.4.1 Circuit Topology 28
6.4.2 Transfer Function 29
6.4.3 Input-Referred Noise 30
6.5 Bioamplifier 32
6.5.1 Miller Integrator as DC Cancelling Circuit 33
6.5.2 Input-Referred Noise 35
6.6 Design 35
6.6.1 Two Stage OTA 36
6.6.2 Pseudoresistor 40
6.6.3 Miller Integrator 40
6.6.4 Current Mirror OTA 42
6.6.5 Bioamplifier 46

Chapter 7 Conclusion
Chapter 8 References

Chapter 1 Introduction

In order to sense and record biosignals in high quality, biomedical implantable devices are required. Many different forms of implants have been developed for this purpose. Such devices must operate under a limited energy budget and have low power consumption to guarantee long time of autonomous operation. To achieve this requirement, CMOS integrated circuit must comprise MOSFETs that operate in subthreshold region. In this thesis, we begin by giving a brief description of biosignals' characteristics in chapter 2. In chapters 3 and 4, we study the structure of MOSFETs and a methodology that is convenient for designing in weak, moderate and strong inversion with good accuracy. In chapter 5, we discuss the types of noise present in a MOSFET while it is a crucial constraint in amplifiers dedicated to amplify low voltage signals. Finally, in chapter 6 we present, in detail, the design procedure of a bioamplifier that meets the specifications of implantable sensing devices.

Chapter 2 Biosignals

2.1 Information flow inside the brain

The fundamental building blocks of the nervous system are neurons. Neurons are electrically active cells and communicate with each other to convey information. Communication procedure between neurons consists of the following steps. Firstly, information is received at the neurons' receivers (dendrites) in chemical form, it diffuses at the cell body (soma) and is transferred through a conducting path (axon) as electric impulse. Finally, information passes onto the next neuron through a junction (synapse) where chemical (and rarely electrical) exchange of information takes place. The structure of a neuron and its' connection with another one is depicted in Figure 2.1.

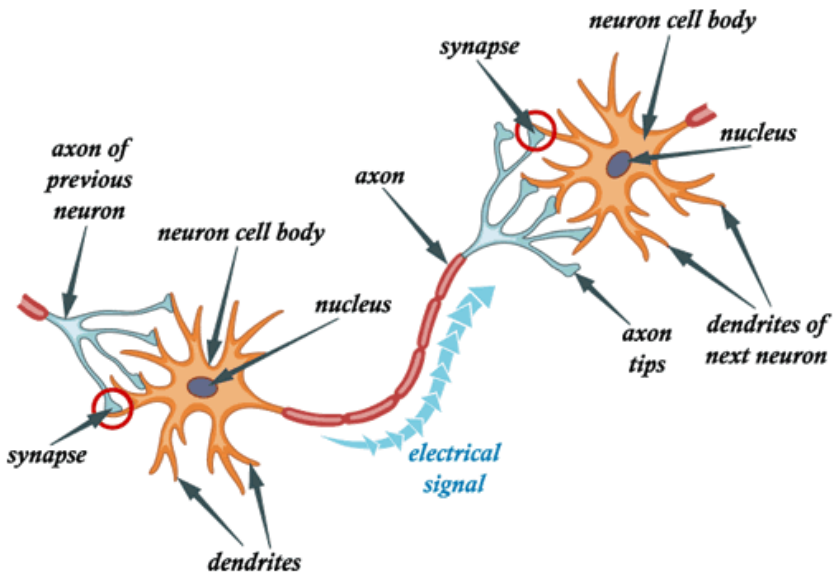

Figure 2.1 Neuron cell structure and interconnection between neurons

.

2.2 Action Potentials

Regularly, neurons generate a negative potential across their membrane in the range of -40mV to -90mV, called the resting membrane potential [1]. When the tansmembrane potential cell surpasses a value, called threshold potential [1], and

gets positive value, an action potential occurs. Action potentials, or spikes, are electrical signals (Figure 2.2) responsible for long-distance (millimeters to meters) propagation of information. They travel through neurons' axons until they reach the target tissues. An essential feature of action potentials is that they occur fully or not at all, meaning that if a more intense stimulus is to be transmitted by an action potential, modulation appears in the frequency rather than in the amplitude of the signal [1]. Therefore, information is encoded only in the timing domain of spikes [2]. The frequency content of action potentials commonly ranges between 100Hz and 7kHz [3].

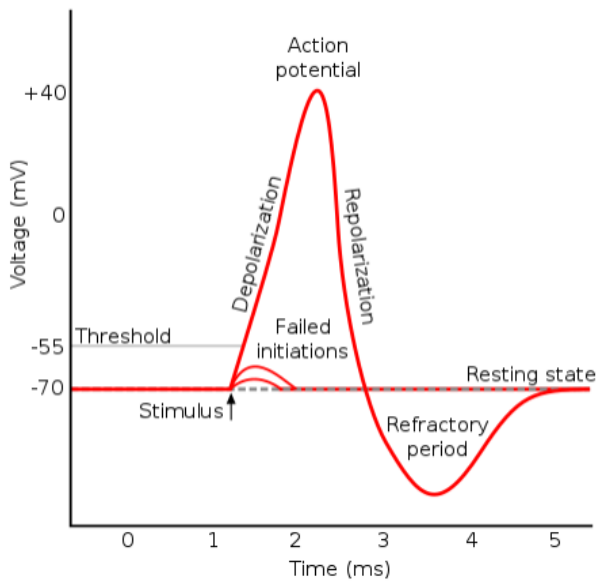

Figure 2.2 Action potential in a voltage vs time plot

2.3 Neural Circuits

Neurons are organized into groups, called neural circuits, responsible for a specific functionality. In each neural circuit, neurons are divided into the following three groups [1]:

Afferent neurons: send signals towards the brain or spinal cord.

Efferent neurons: send signals away from the brain or spinal cord.

Interneurons: have short axons and are limited to a small area.

In Figure 2.3 the knee-jerk reflex along with the described neural structure is depicted.

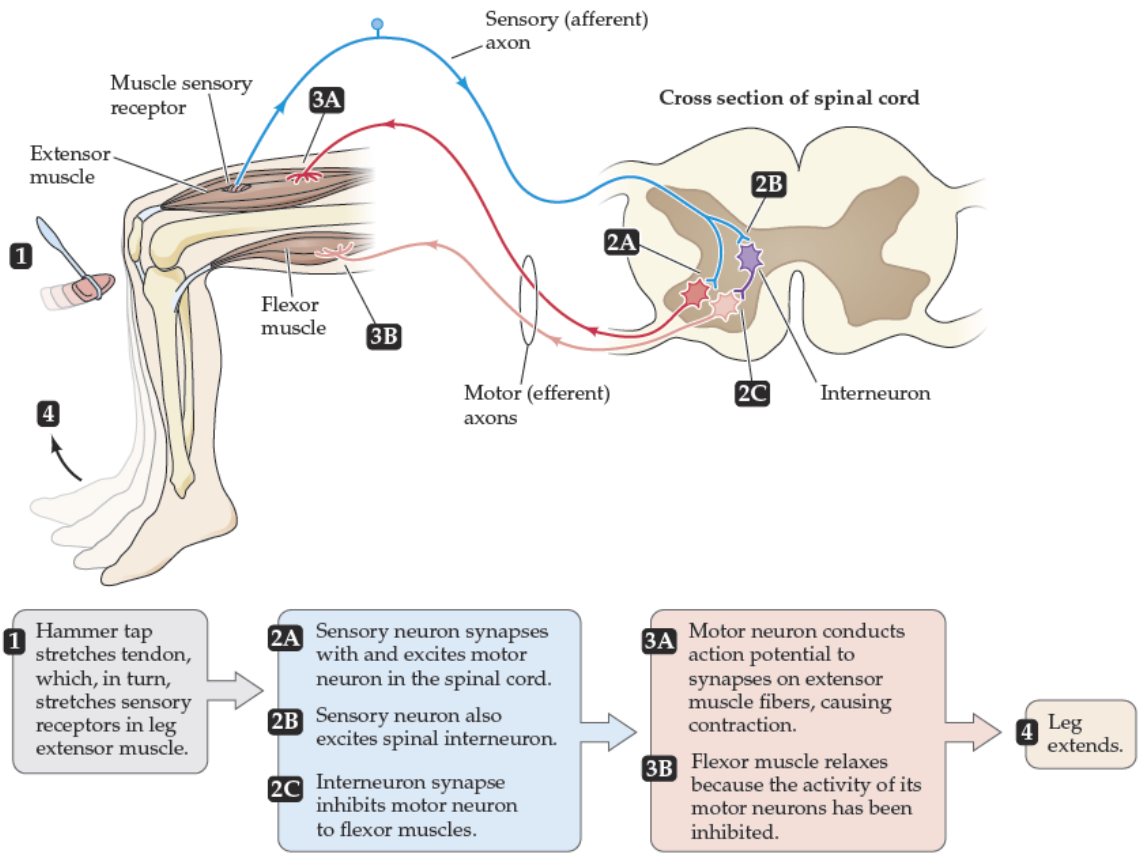

Figure 2.3 Knee-jerk reflex procedure [1]

2.4 Action Potentials Recording Methods

There are two methods to measure neural electrical signals. The first method is to use an intracellular microelectrode and measure the potential across neuron's membrane. Internal voltage changes are on the order of 100mV, relative to the extracellular fluid, and can give us meaningful and precise information about neurons' activity. Nevertheless, measuring action potentials intracellularly is typically difficult and expensive [1, 4]. The second method is to implant multi-electrode arrays at a short distance (several microns) from the cell and measure extracellular potentials [2]. External voltage signals undergo much attenuation and

their amplitude is on the order of 100 μV. In contrast with intercellular recording of action potentials, extracellular recording is easier to implement and give us a decent insight of neural activity.

2.5 Why Action Potentials Recording

Brain is the most powerful and incomprehensible organ in human body. Ideas, emotions, memories and intelligence are derived from it. In addition, brain is linked with two essential mechanisms, sensory and motor. The pathway between brain, body muscles and sensors, is formed by the spinal cord which is a tubular structure made of nervous tissue located in a narrow canal that runs through the center of spine. When a spinal cord injury (SCI) occurs, the flow of messages between the brain and the rest of the body is interrupted. This interruption leads to total or partial loss of the ability to sense environmental stimuli and/or control over the limbs. The higher up the injury occurs; the more functionality of the body is affected. In this manner, tetraplegia is caused by a damage to the brain or SCIs and is one of the most severe forms of paralysis affecting both the upper and the lower body. Obviously, people suffering from tetraplegia lack self-reliance and are dependent on the help of others to complete a simple task. Although there is no way to reverse the damage of SCIs, the power of technology can help patients become self-reliant again. In more detail, the absence of a pathway allowing information flow between brain and body can be overcome if a new communication channel is created. The latter has to be composed of two elementary structures: a) a circuit designed for measuring, processing and transmitting action potentials b) an actuator (i.e. a robotic arm) or a second circuit responsible for receiving signals and stimulating neurons following the damaged ones. To measure action potentials associated with planning, control and execution of movements, an implant must be placed at the motor cortex (shown in Figure 2.4), a region of cerebral cortex involved in the aforementioned functionality.

2.6 Action Potentials Amplification

For the purpose of processing and transmitting small amplitude signals, like action potentials, amplification is required. This thesis focuses on the design of a front-end analog CMOS amplifier that comply with the specifications arising from action potentials' attributes. The amplifier must have [2,5,6] :

- Input-referred noise below 10 uVrms. Greater values will degenerate signal quality because, as described in paragraph 2.4, extracellular voltage signals are on the order of 100 μV but may appear weaker if the distance between neuron and measuring electrode is longer.
- Enough dynamic range to amplify signals up to 2mv.
- High input impedance and negligible input current.
- Bandpass response with high cut-off frequency equal to 10kHz and low cut-off frequency equal to 100Hz to accurately capture spiking activity.
- DC offset rejection circuitry to remove dc offset across differential sensing electrodes.
- High common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) to reduce noise on the transmission lines and power noise, respectively.
- Power dissipation below a few hundred microwatts per channel to avoid harming cerebral cortex and extend autonomous operation time under a given energy budget.
- Adequately small area (typically 0.16mm^2 per channel) to avoid oversized implants and satisfy inter-electrode spacing (commonly 400 μm).

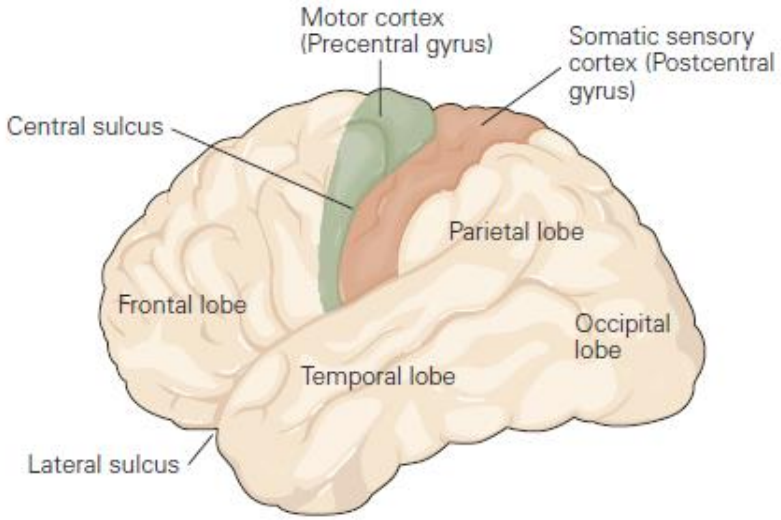

Figure 2.5 Brain structure

Chapter 3 MOSFET Device

Aiming to have a better perception of concepts discussed in this thesis, it is essential to understand MOSFET devices structure and physics. In this chapter, the above are discussed at the minimum level of detail required to achieve our goal.

3.1 MOSFET Structure

MOS transistor is a four terminal field effect device, mainly composed of semiconductor materials arranged in such a way that gives the device unique properties and functionality. Semiconductors utilized to construct MOSFETs are of two types, p-type and n-type. N-type provide electrons as majority carriers and holes as minority carriers. Conversely in p-type, electrons are the minority carriers and holes are the majority carriers. Depending on how n-type and p-type materials are arranged within the device, two types of MOSFET arise, NMOS and PMOS. The basic structure of NMOS devices is shown in Figure 3.1. For PMOS devices all dopings are inverted (see Figure 3.2).

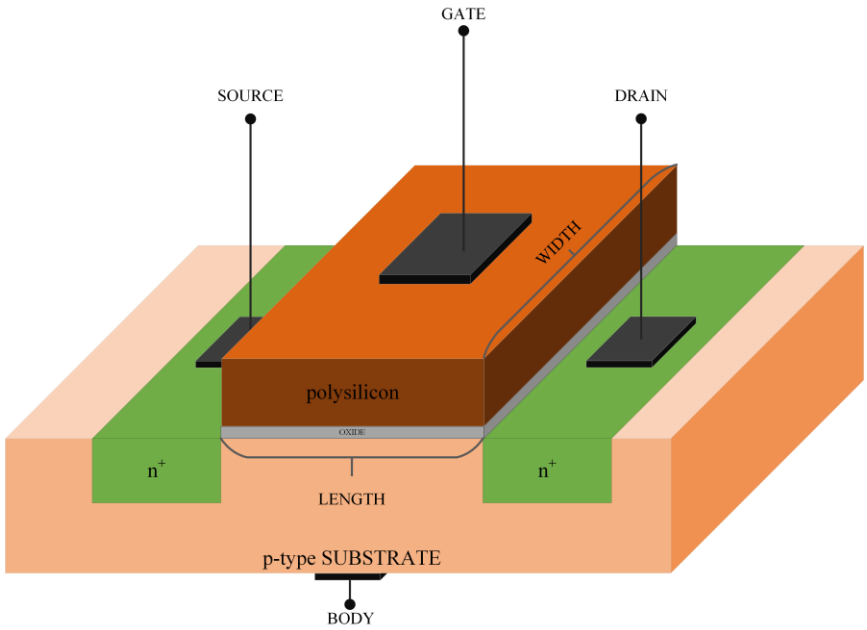

Figure 3.1 3D illustration of NMOS device

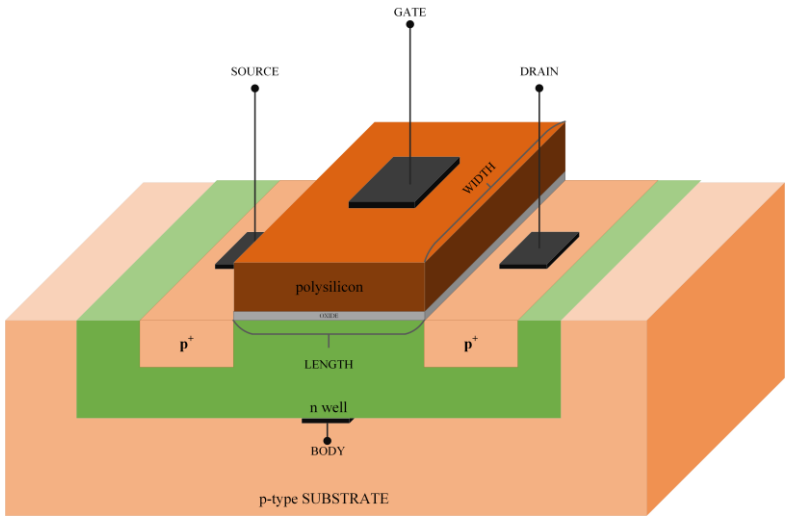

Figure 3.2 3D illustration of PMOS device

The material on which the whole NMOS device stands is a p-type silicon substrate and is called bulk or body (B). Two metal contacts, called drain (D) and source (S), are connected to the body through diffusions of heavily doped n-type material (n^+).

The presence of n^+ diffusions, under the contacts, results in low resistivity at the drain and source terminals. On top of the semiconductors, a thin insulating layer of silicon dioxide (oxide) is placed at the area enclosed by drain and source, while on this layer resides a plate made of noncrystalline silicon (polysilicon) with heavy doping, known as gate (G). Hence, gate is insulated from the body. Very important in circuit design procedure is the careful selection of gate dimensions, width (W) and length (L). These two parameters affect most of the characteristics in a MOSFET.

We observe that MOSFET structure is symmetrical with respect to a vertical axis at the middle of the device. Thus, a reasonable question is how we distinguish source and drain terminals. In NMOS transistors, drain is connected to higher voltage than source and in PMOS transistors, drain and source terminals are connected inversely.

3.2 MOSFET Operation

If we examine the structure of NMOS, shown in Figure 3.1, we notice that there is not any conductive path between drain and source. By applying a positive voltage to the gate, p-type substrate minority carriers, electrons, are attracted at the piece of

silicon under the insulating layer and a conductive channel is formed [7]. The more positive voltage applied to the gate; the more electrons attracted to the channel. Thus, channel resistance is reduced and if we apply a positive voltage between drain and source, current starts flowing.

The remainder of this chapter deals with analyzing MOSFET operation under different biasing conditions. Henceforth, we consider the bulk grounded for n-MOS devices and connected to high voltage for p-MOS devices (not shown in the next figures).

We start our analysis assuming that drain and source terminals are grounded and we vary the gate voltage from zero to positive values. The initial condition in MOSFET, when all terminals are grounded (V_G=0), is shown in Figure 3.3.Transistor is off, meaning that the channel is not formed yet.

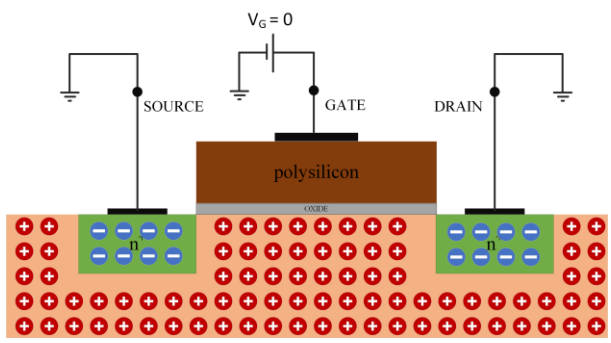

Figure 3.3 2D NMOS illustration with zero voltages at its terminals

Before continuing with the analysis, we must mention that the structure polysilicon-oxide-p-type silicon operates as a capacitor. Hence, we expect that any positive charge at the gate will appear negative at the interface between oxide and substrate[7]. We now gradually increase gate voltage. A positive voltage at the gate repels substrate holes and repelled holes leave behind negative ions. As a result, the surface under the gate is depleted of free carriers. Therefore, n-MOS is still off and the channel is not formed yet (Figure 3.4).

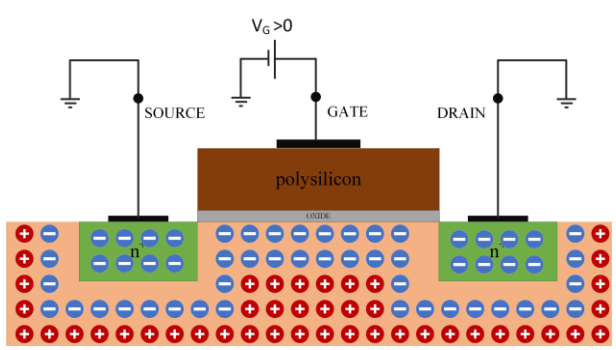

Figure 3.4 NMOS with low positive voltage at its gate

By rising gate to source voltage (V_{GS}), depletion region depth increases (Figure 3.5) until gate voltage exceeds a value, called threshold voltage (V_{TH}). For V_{GS} voltages beyond V_{TH}, electrons are attracted under the gate oxide and a conductive channel is established. Considering that free electrons are concentrated in the p-type bulk we say that the interface is inverted and the channel is called inversion layer [8] (Figure 3.6). Further increase of gate voltage above the threshold, results in a more conductive channel because it contains more electrons.

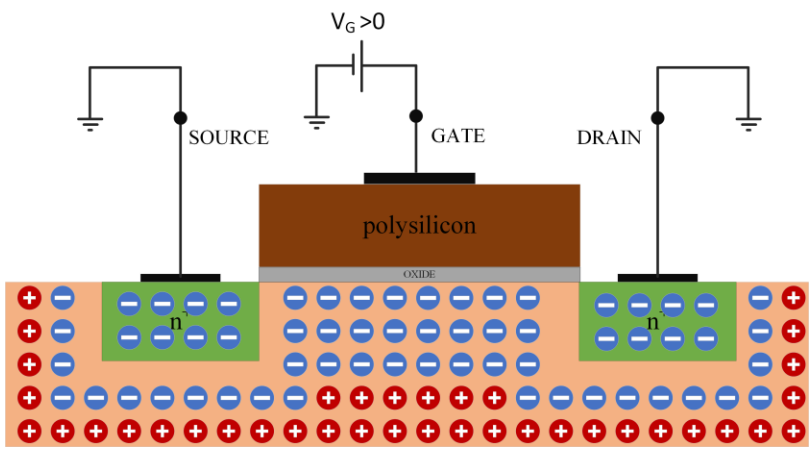

Figure 3.5 NMOS with $V_{GS}<V_{TH}$ and widen depletion region

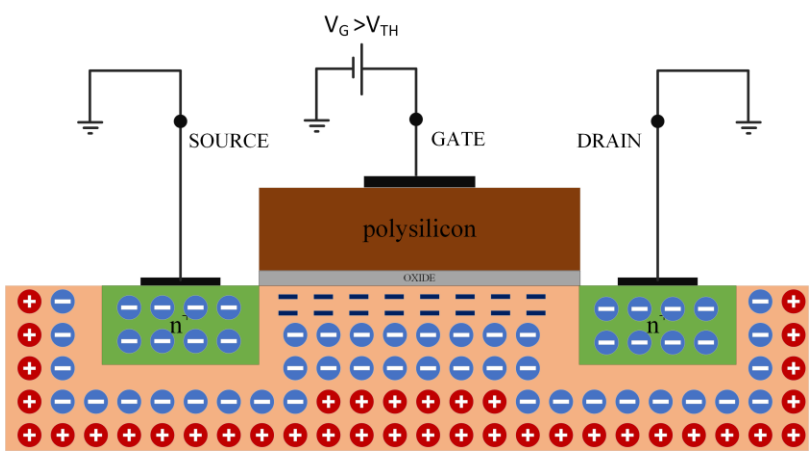

Figure 3.6 NMOS with $V_{GS}>V_{TH}$. Inversion layer establishment

As the channel is formed, if we apply a positive voltage at the drain, current (I_{DS}) will start flowing. Before studying current flow, we must focus on how charges are distributed in the channel. Charge density at a point in the channel is proportional to V_{GS}-V_{TH}-V(x), where V(x) is the channel potential at this point [8]. Hence, charges are not distributed uniformly for the reason that voltage difference is not uniform across the channel. At a point near the drain, voltage difference between gate and channel is equal to V_G-V_D, where V_D>0. In contrast, near the source, voltage difference between gate and channel is equal to V_G because source is grounded. As an outcome, channel has the shape shown in Figure 3.7.

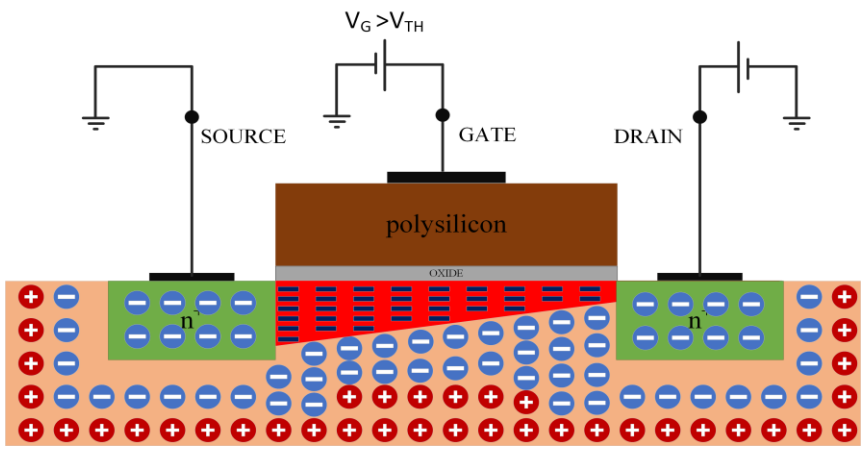

Figure 3.7 NMOS with V_{GS}>0 and V_{DS}>0

3.3 Regions of Operation

The voltage V_{GS} in excess of V_{TH} is called overdrive (or effective) voltage (V_{OV}) and is defined as the voltage required to turn on the transistor. Overdrive voltage alters channel resistivity by attracting curriers at the region of substrate under the oxide. Consequently, it directly controls the current flowing through the transistor. Additionally, current is controlled by V_{DS} voltage which is the voltage difference between drain and source. In view of the foregoing, three regions of operation arise:

- **Cutoff** (V_{OV}<0): MOSFET is off and channel is not formed.

- **Triode** ($V_{OV} > 0$ and $V_{DS} < V_{OV}$): The device conducts current roughly linear proportional to V_{DS}. In this region MOSFET behaves like a voltage dependent resistor.

- **Saturation**($V_{OV} > 0$) & $V_{DS} \geq V_{OV}$: When V_{DS} exceeds a value called saturation voltage, $V_{DS,sat}$, there is no more a linear relationship between V_{DS} and I_{DS}. Further increase in V_{DS}, does not have a significant effect on drain current, I_{DS} is saturated. This happens because the application of a drain voltage reduces gate to substrate potential near the drain and thus, fewer charges are concentrated at this region. If V_{DS} is below $V_{DS,sat}$, inversion layer has the form depicted in Figure 3.7. When V_{DS} is greater than $V_{DS,sat}$, channel is shortened (Figure 3.8) and extends from the source to a point called pinch off. In this case we say that inversion layer is pinched off and higher V_{DS} voltages result in a shorter channel. When channel is pinched off, electrons gain high speed, because of the high electric field, and pass through the depletion region between pinch off and drain. Under this condition, I_{DS} is relatively independent of V_{DS}. In saturation MOSFET, operates like a dependent current source controlled by V_{GS}.

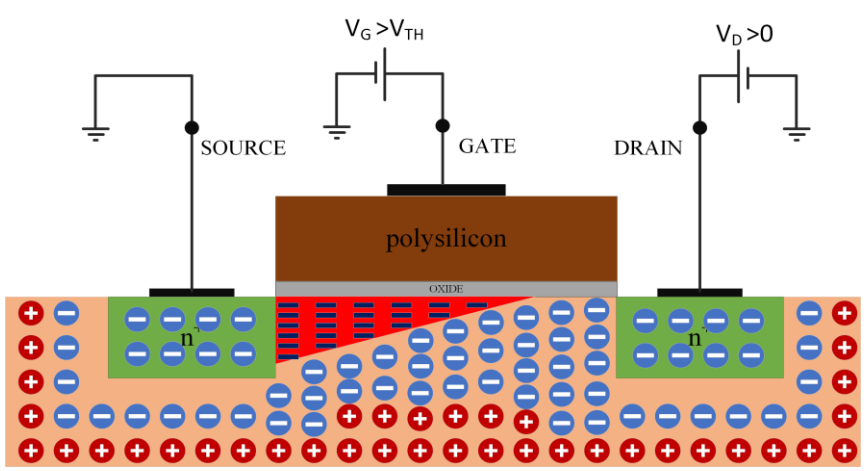

Figure 3.8 NMOS with $V_{GS}>0$ and $V_{DS}> V_{DS,sat}$, pinched off channel

Chapter 4 Circuit Design Methodology

In the previous chapter we analyzed MOSFET as a device which conducts current when a channel, between source and drain, is formed. We stated that this is achieved for V_{GS} values greater than or equal to threshold voltage, V_{TH}. In fact, even when V_{GS} is below the threshold voltage, a weakly inverted layer is formed. Let us now study the dependence between inversion layer and V_{GS}.

4.1 Channel Inversion Regions

Gate to source voltage determines the level of inversion at the channel. Depending on V_{GS} voltage, three regions of inversion arise. The first region is called weak inversion (WI) or subthreshold region. This region emerges for V_{GS} below V_{TH} by at least 72mV and the channel is weakly inverted. When MOSFET operates in weak inversion, drain diffusion current dominates and its dependence on V_{GS} is exponential. In the second region, channel is strongly inverted and is called strong inversion (SI) region. This occurs when $V_{GS} \geq V_{TH}$, and drift current dominates. In this region, current is proportional to the square of V_{GS}. The region between WI and SI is called moderate inversion (MI) and its characteristics is a superposition of WI and SI.

Transistors operate at a specific region of inversion (WI, MI, SI) and operation (cutoff, triode, saturation) proportional to their biasing. The most common region of operation for MOSFETs in analog circuits is saturation. Saturation voltage and drain current can be calculated from the following equations:

Weak Inversion Saturation Voltage:

$$V_{DS,sat} = 4 \cdot U_T$$

$$U_T = \frac{k \cdot T}{q}$$

Where,

- U_T is the thermal voltage and has value $U_T \approx 26$mV at room temperature
- $k = 1.3086 \cdot 10^{-23}$ J/K is the Boltzmann's constant

- $q = 1.602 \cdot 10^{-19}$ C is the electric charge carried by an electron

Strong Inversion Saturation Voltage:

$$V_{DS,sat} = \frac{V_G - n \cdot V_S - V_{TH}}{n}$$

Where,

- n is the slope factor, $1.1 < n < 1.6$ [9]
- V_G and V_S is the gate and source voltage respectively
- V_{TH} is the threshold voltage

Drain Current in Weak Inversion, saturation:

$$I_D = 2 \cdot \mu \cdot n \cdot C'_{OX} \cdot \frac{W}{L} \cdot e^{\frac{V_G - n \cdot V_S - V_{TH}}{n \cdot U_T}}$$

Where,

- μ is the current carriers' mobility
- C'_{OX} is the gate-oxide capacitance per unit area of the oxide

Gate-oxide capacitance per unit area is calculated by:

$$C'_{OX} = \frac{\varepsilon_{ox}}{T_{ox}}$$

Where,

- ε_{ox} is the oxide permittivity, $\varepsilon_{ox(SiO_2)} = 3.45 \cdot 10^{-11} F/m$
- T_{ox} is the oxide thicknes and depends on the fabrication process

4.2 Inversion Coefficient Design Methodology

Biomedical implantable devices, as already discussed in chapter 1, must operate under low power and low voltage to guarantee long periods of operation and low heating of the device. Low power circuits require transistors to operate in weak and moderate inversion. In this chapter we discuss about IC methodology on which the design of this work is done.

The region and level of inversion in the channel of a single MOSFET can be signified by a numeric value called inversion coefficient (IC). Using EKV MOS model equations[10], IC provides a good insight into design tradeoffs and let us design in all regions of operation. Also, trial-and-error simulations are reduced because a good initial design is attainable with this method. Regions of MOS inversion are related to IC in the following way:

IC<0.1	→	weak inversion
0.1<IC<10	→	moderate inversion
IC>10	→	strong inversion

IC design methodology is based on the selection of three parameters, inversion coefficient (IC), gate length (L) and drain current (I_D). The following expressions help us comprehend how these parameters affect MOSFET parameters.

Inversion Coefficient:

$$\mathrm{IC} = \frac{I_D}{I_{spec} \cdot \frac{W}{L}} \qquad \text{or} \qquad \mathrm{W} = \frac{I_D \cdot L}{I_{spec} \cdot IC}.$$

Where Ispec is called specific or technology current. Specific current is a fundamental parameter that can be extracted for a given technology from the circuit shown in figure Figure 4.1 [11] and then be used as a constant value in the design procedure. Subsequently, the above equation gives us the gate width for specific IC, L and I_D.

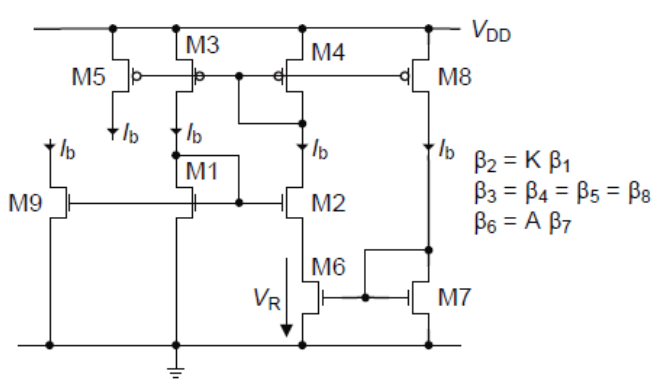

Figure 4.1 Circuit for extraction of I_{spec}

Saturation Voltage:

$$\text{Vds, sat} = 2 \cdot U_T \cdot \sqrt{IC + \frac{1}{4}} + 3 \cdot U_T$$

$$\text{WI:} \quad V_{DS,sat} \approx 4 \cdot U_T$$

$$\text{SI:} \quad V_{DS,sat} = V_p - V_S$$

Transconductance (saturation)[9]**:**

$$g_m = \frac{I_D}{U_T \cdot n} \cdot G(IC)$$

Where G(IC) is the normalized transconductance and represents the percentage of the maximum transconductance a transistor exploits for a give IC.

$$G(IC) = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + IC}}$$

From the equation of transconductance, g_m, we observe that for a constant bias current, maximum transconductance is reached in WI. One of the most powerful Figures of Merit (FoMs) in low-power analog design is the transconductance efficiency ($\frac{g_m}{I_D}$). It appears in many optimization expressions and quantifies the transconductance produced for a given bias current [12].

$$\frac{g_m}{I_D} = \frac{1}{U_T \cdot n} \cdot \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + IC}}$$

The transconductance efficiency is maximum in WI. From WI to MI monotonically decreases and in SI is minimized.

Overdrive voltage[13]**:**

$$V_{OV} = 2 \cdot n \cdot U_T \cdot ln(e^{\sqrt{IC}} - 1)$$

Unity gain transit frequency:

$$f_T = \frac{\mu \cdot U_T}{2 \cdot \pi \cdot {L_{eff}}^2} \cdot \left(\sqrt{1 + 4 \cdot IC} - 1\right)$$

Where L_{eff} is the effective channel length.

Drain current and gate source mismatch:

$$\sigma_{\frac{\Delta I_D}{I_D}} = \sqrt{{\sigma_{\frac{\Delta\beta}{\beta}}}^2 + \left(\frac{g_m}{I_D} \cdot \sigma_{\Delta V_T}\right)^2} \qquad \sigma_{\Delta V_{GS}} = \sqrt{{\sigma_{\Delta V_T}}^2 + \left(\sigma_{\Delta V_T} \frac{\sigma_{\frac{\Delta\beta}{\beta}}}{\frac{g_m}{I_D}}\right)^2}$$

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{W \cdot L}}$$

$$\sigma_{\frac{\Delta_\beta}{\beta}} = \frac{A_\beta}{\sqrt{W \cdot L}}$$

Where A_β and A_{VT} are constant for a given technology.

We mentioned that $\frac{g_m}{I_D}$ is a function of inversion coefficient. So, mismatch is also controlled by IC.

Chapter 5 Noise

Noise is usually an undesired phenomenon present in CMOS devices. By its nature, noise is random and unpredictable. If an analog CMOS circuit is designed without taking noise into consideration, it may suffer from signal quality degradation. Hence, to face its effect we must encounter noise sources and minimize their contribution to the signal. Since noise is random, it is characterized by statistical models. In this chapter we study the different types of noise in a MOSFET and their origin.

5.1 Noise in MOSFET

Environmental sources, such as capacitive or inductive coupling, generate noise in circuits. This type of noise is called artificial and is mainly reduced with improvements on physical layout [14]. Moreover, the transistor itself generates noise, called fundamental noise. To minimize the effect of transistor's intrinsic noise we must change the circuit topology, MOSFET dimensions and other design parameters[15]. Fundamental noise is composed of four types that are explained below.

5.1.1 Flicker Noise (1/f)

One of the most important noise components in MOSFET devices operating in low frequencies is the flicker noise. It is inversely proportional to frequency and dominates at low frequencies up to some tens of kilo Hertz. That is the reason we are referred to it as 1/f noise too. The origin of flicker noise are dangling bonds appearing at the interface between the oxide and the substrate. These defects create energy states which act as traps for the channel carriers. When carriers pass through the channel, some of them, are trapped and released randomly at the traps [8]. This trapping and de-trapping mechanism fluctuates channel carrier density and hence noise is generated. Typically, more advanced technologies exhibit reduced flicker noise. That is because fabrication process affects oxide-substrate interface quality which in turn affects flicker noise. Additionally, PMOS transistors exhibit lesser flicker noise in compare to NMOS because of their reduced carrier mobility and trap density[16]. Flicker noise can be modeled as the power spectral density of drain current and gate voltage by the following equations:

$$S_{\Delta VG}(f) = \frac{K_F}{C_{OX} \cdot W \cdot L} \cdot \frac{1}{f^{AF}} \qquad S_{\Delta ID}(f) = \frac{g^2{}_m \cdot K_F}{C_{OX} \cdot W \cdot L} \cdot \frac{1}{f^{AF}}$$

Where,

- K_F is the flicker noise coefficient
- C_{OX} is the gate capacitance
- W is the gate width
- L is the gate length
- f is the frequency of operation
- AF is the flicker noise exponent
- g_m is the MOSFET transconductance

We observe that for large area transistors, noise is reduced.

5.1.2 Thermal Noise

Thermal noise or Johnson-Nyquist is caused by Brownian motion [14]. In a given medium, random thermal motion of electrons take place. This phenomenon is independent of the dc current flowing in the component and therefore introduces noise source in the device . The power spectral density of thermal noise is constant across all frequencies and we are usually referred to it as white noise. For a resistive element thermal noise is given by:

$$S_{Vg} = 4 \cdot k \cdot T \cdot R$$

Where,

- k is the Boltzmann's constant
- T is the operating Temperature
- R is the resistance

For a MOSFET in saturation, thermal noise can be modeled by:

$$S_{I_{D,thermal}} = 4 \cdot k \cdot T \cdot \gamma \cdot g_{ms}$$

Where,

- g_{ms} is the source transconductance, $g_{ms} = n \cdot g_{mg}$
- γ is the thermal noise factor and is equal to $\frac{1}{\cdot 2}$ in WI and $\frac{2}{\cdot 3}$ in SI

5.1.3 Shot Noise

Shot noise, occurs due to the potential barriers present in pn junctions of MOS devices. In a pn junction, a voltage exists between the p-type and the n-type regions. Current flow starts when electrons and carriers at p and n regions have sufficient energy to overcome the potential barrier [14,17]. Carriers pass across the potential barrier randomly and they cause fluctuations in current. MOSFETs experience shot noise in channel depletion region and junctions between drain and source with the bulk. It is given by:

$$S_{I_{D,shotnoise}} = 2 \cdot q \cdot I_D$$

Where,

- q is the electric charge carried by an electron.
- I_D is the current flowing through the MOSFET

5.1.4 Substrate Noise

In a MOSFET, source and drain form capacitors with the bulk. At low frequencies, these capacitances do not influence the performance because they act as high resistances (DC open circuit). In contrast, at high frequencies capacitors act as low resistances (DC shorts) and small currents pass through the bulk, reducing the current at the channel.

5.1.5 Generation-Recombination Noise

Like flicker noise, generation-recombination noise is generated by bulk defects that capture or release carriers randomly. This mechanism affects the number of carriers in the channel participating in the current flow[14].

5.2 Noise in Circuits

Noise in CMOS circuits can be measured at the output or the input of the circuit. We refer to noise measured at the input and the output, as input-referred and output referred noise, respectively. Output-referred noise is a physical quantity

which can be measured in the laboratory using a spectrum analyzer. However, it is not a good parameter for comparison between circuits since it is affected by the gain. Input-referred noise is calculated from the division of the output-referred noise by the gain of the circuit and cannot be measured practically. Nevertheless, it can be used directly for comparison between different circuits without considering other characteristics. Also, input-referred noise specifies the minimum input signal with respect to a required signal to noise ratio (SNR).

To calculate input-referred noise in a circuit, we first must calculate output noise. Initially we replace every transistor in the circuit with its small-signal equivalent and its noise sources. After that, we calculate the noise contribution of each source to the output noise by setting the rest of the sources to zero (voltage sources become shorts and output sources become opens). Finally, the total output noise results from the superposition of all individual noise contributions. Hence, we can have an expression for the input-referred noise by dividing the output-referred noise with the gain of the circuit.

From the above analysis, input noise power spectral density $(\frac{V^2}{\sqrt{Hz}})$ is calculated. This gives as a useful picture of how noise power is distributed into frequencies, but it does not allow us to easily compare between two circuits. That is why we convert it to rms value which represents the average noise voltage. To accomplish this, we integrate power spectral density across the frequencies of interest, and we take the square root of the result.

$$NoiseVotalge_{(rms)} = \sqrt{\int_{f1}^{f2} Noise\ power\ spectral\ density\ \cdot df}$$

Chapter 6 Bioamplifier

In this chapter we will study the components that construct the Bioamplifier of this work. We will give some useful expressions about bioamplifier's components characteristics. These expressions give us an insight about system's performance and in what manner each design option affects it.

6.1 Two-Stage OTA

The block diagram of a two stage OTA is shown in Figure 6.1. This topology is composed of two cascaded amplifiers. The first stage is a differential pair with active load (Figure 6.2) and the second stage is a common source amplifier(Figure 6.3).

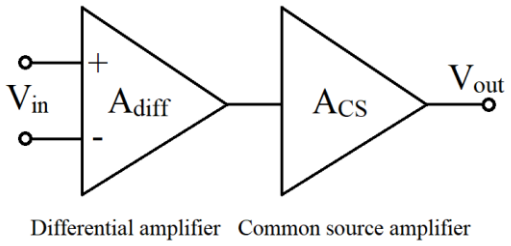

Figure 6.1 Two stage OTA block diagram

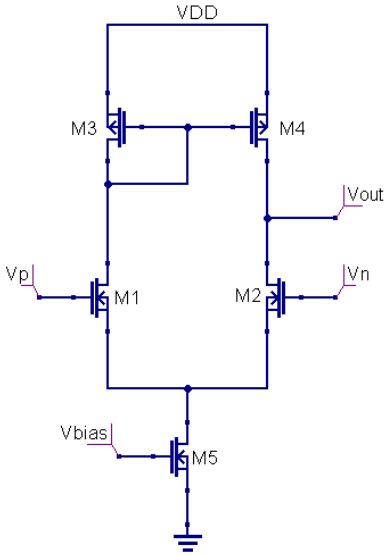

Figure 6.2 Differential amplifier topology

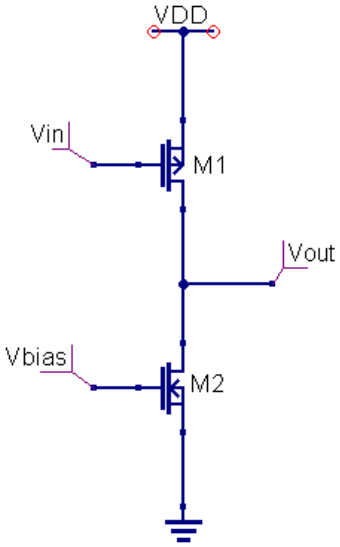

Figure 6.3 Common source amplifier topology

This topology exhibits high DC gain equal to the product of the gains of each stage.

$$A_{\text{two stage OTA}} = A_{\text{diff. pair}} \cdot A_{CS}$$

6.1.1 Circuit Topology

The topology of two stage OTA is depicted in Figure 6.4. It comprises an NMOS differential pair at its inputs ($M_{1,2}$), a PMOS current mirror active load ($M_{3,4}$), a PMOS transistor at the input of the CS stage (M_7) and two current mirrors for the biasing (M_5,M_6,M_8) of the stages.

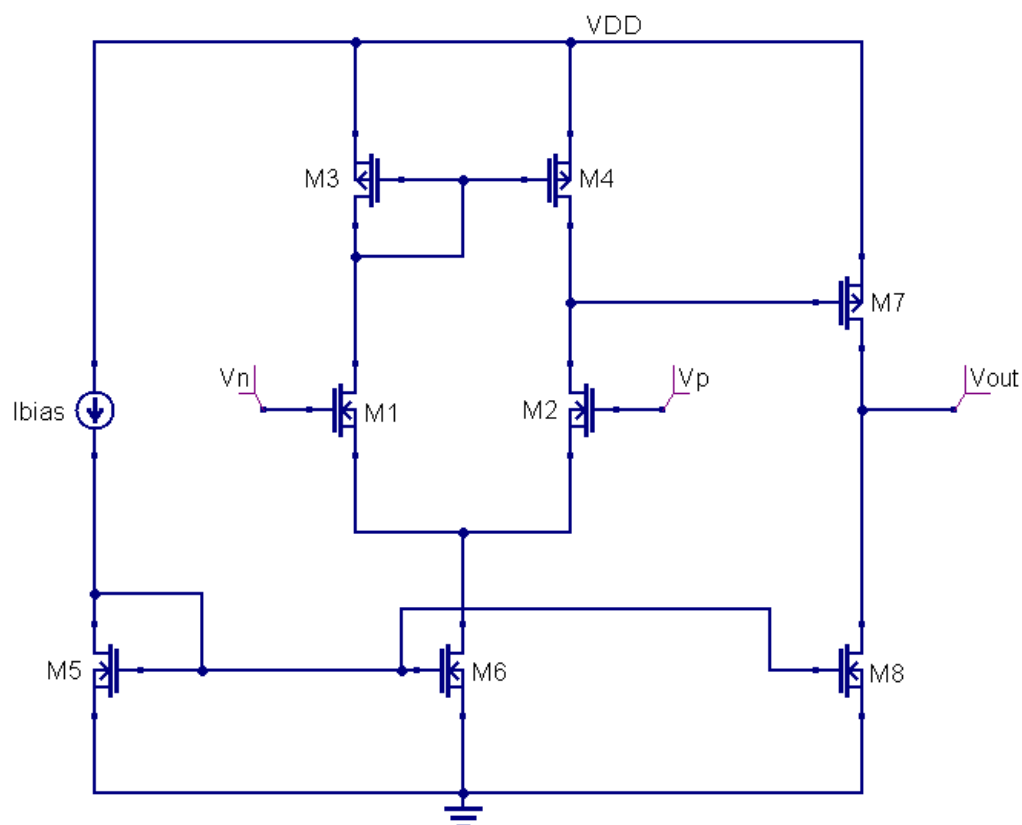

Figure 6.4 Two stage OTA topology

In the configuration shown in Figure 6.4, the amplifier operates as a second order system because it has two poles, associated with each stage, appearing in frequencies lower than the unity gain frequency. Consequently, the amplifier will

evidently be unstable. The simplest way to compensate it is to connect a capacitor within the high gain stage. This compensation technique, moves the lower frequency pole in lower frequency and the higher pole in higher frequency, utilizing the Miller effect [18]. Nevertheless, the compensating capacitor in high frequencies acts as a short and creates a feed-forward path which results in a right half plane (RHP) zero. This RHP zero has the same impact as a left half plane pole (LHP) and hence degrades phase margin and settling time [18, 19].

To shift the zero (created from the capacitor) to higher frequencies, we can connect a resistor in series with the compensating capacitor that attenuates the higher frequency signals [18]. Therefore, the amplifier operates as a first order system since it has only one pole in frequencies lower than unity gain frequency. This compensation technique is called lead-compensation. The two stage OTA with lead compensation is illustrated in Figure 6.5.

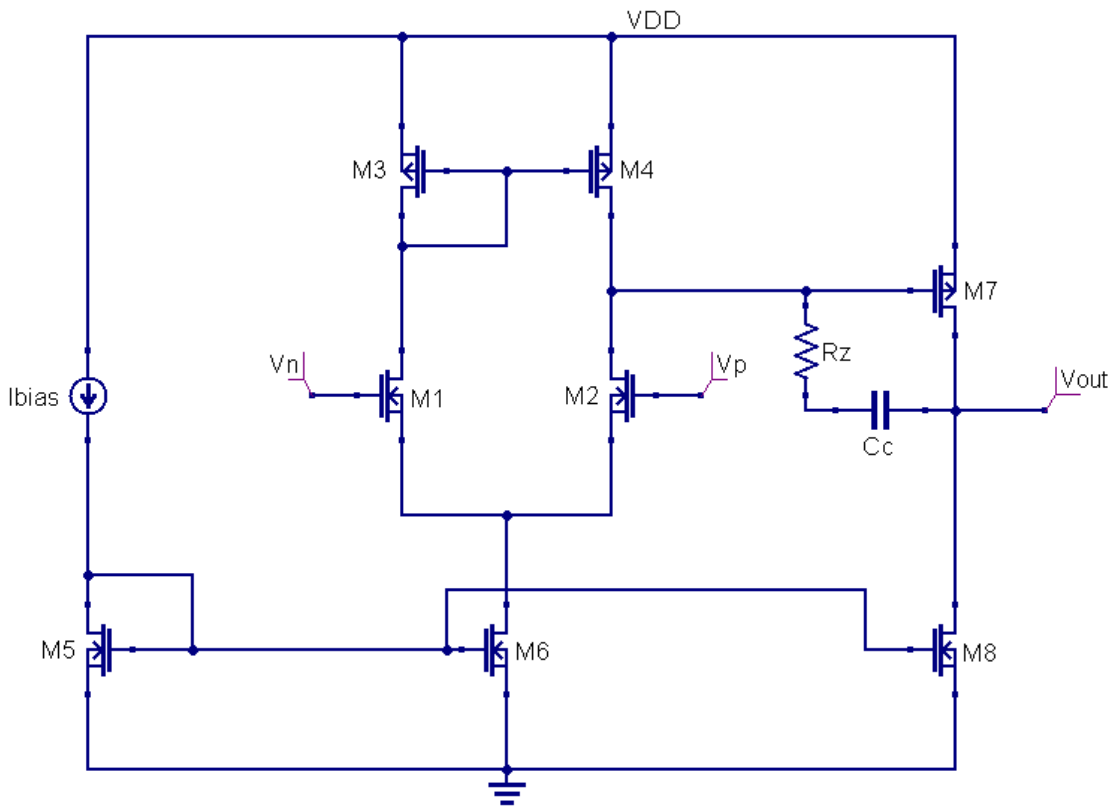

Figure 6.5 Two stage OTA with lead compensation topology

6.1.2 Transfer Function

From the small-signal equivalent circuit [19] presented in figure Figure 6.6 we can find amplifier's transfer function. The capacitance, C_L is the output load.

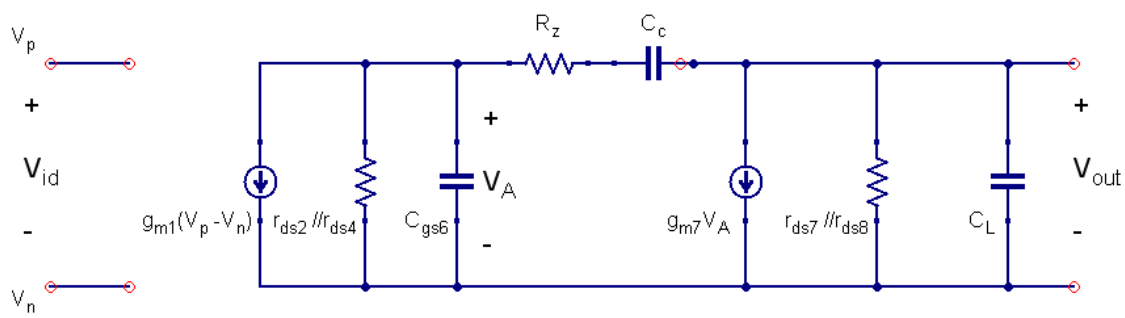

Figure 6.6 Two stage OTA small-signal equivalent

The transfer function is given by expression $\frac{V_{out}}{V_{id}}$ below, if the next conditions hold[19]:

$$g_{m6} \cdot R_B \gg \frac{C_{gs6}}{C_c}$$

$$g_{m6} \cdot R_A \gg \frac{C_L}{C_c}$$

$$R_Z \gg R_A \quad \& \quad R_Z \gg R_A$$

Where

$$R_A = r_{ds2}//r_{ds4}$$

$$R_B = r_{ds7}//r_{ds8}$$

$$\frac{V_{out}}{V_{id}} = A_o \frac{1 - sC_c(\frac{1}{g_{m6}} - R_Z)}{1 + g_{m6}R_AR_BC_cs + R_AR_B(C_{gs6}C_L + C_{gs6}C_c + C_cC_L)s^2 + R_AR_BR_ZC_{gs6}C_cC_Ls^2}$$

Where A_o is the open loop gain and is equal to:

$$A_o = g_{m1} \cdot (r_{ds2}//r_{ds4}) \cdot g_{m7} \cdot (r_{ds7}//r_{ds8})$$

It is preferred, the output resistance of the input transistor in CS (M_7) to be much lesser than the output conductance of the current source load(M_8). In this case, low-frequency open loop gain is equal to:

$$A_o = g_{m1} \cdot (r_{ds2}//r_{ds4}) \cdot g_{m7} \cdot (r_{ds8})$$

Where,

- $g_{m1} \cdot (r_{ds2}//r_{ds4})$ is the open loop gain of the diff. amplifier
- $g_{m7} \cdot (r_{ds8})$ is the open loop gain of the CS amplifier

6.1.3 Input-Referred Noise

The input-referred thermal noise spectral density of the two stage OTA is given by [19]:

$$S_n(f) = 16kT \frac{1}{g_{m1,2}} (\gamma_{1,2} + \gamma_{3,4} \frac{g_{m3,4}}{g_{m1,2}})$$

Where γ_i is the thermal noise factor of the ith MOSFET and is equal to $\frac{1}{2}$ in WI and $\frac{2}{3}$ in SI

To reduce input-referred noise, we must increase $g_{m3,4}$ and decrease $g_{m1,2}$. As shown in chapter 4.2, MOSFET transconductance can be calculated from the following expression:

$$g_m = \frac{I_D}{U_T \cdot n} \cdot G(IC)$$

If we replace transconductance to the noise expression we get:

$$S_n(f) = 16kT \frac{n \cdot U_T}{I_{D1} \cdot G(IC_{1,2})} (\gamma_{1,2} + \gamma_{3,4} \frac{G(IC_{3,4})}{G(IC_{1,2})})$$

Thus, transistors M_1 and M_2 must operate in WI, low IC, and transistors M_3 and M_4 must operate in SI, high IC.

6.2 Pseudoresistor

A high resistance can be achieved if we connect two diode-connected MOSFETs in series (shown in Figure 6.7). This topology has resistance greater than 10 GΩ when signals with low amplitude $|\Delta V| < 100mV$ are applied to it. In more detail,

if $\Delta V < 0$, transistors M_1 and M_2 act like diode-connected MOSFETs. When $\Delta V > 0$, transistors are off and parasitic source-well-drain p-n-p bipolar junction transistors are activated, resulting in two diode-connected BJTs. Since in this topology transistors act as diodes for low voltage differences, and diodes exhibit high resistivity for low voltages, the total resistance of the topology is high for small $|\Delta V|$ [6].

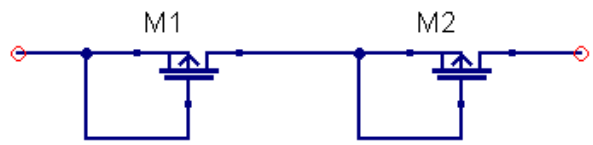

Figure 6.7 Diode-connected transistors in series acting as a high resistor

6.3 Miller Integrator

We can implement a Miller integrator using the foregoing two-stage OTA, a pseudoresistor and a capacitor. The topology of the Miller integrator is depicted in Figure 6.8.

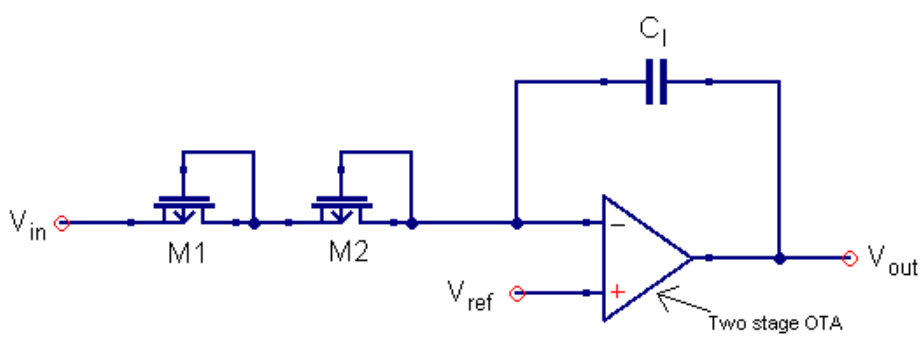

Figure 6.8 Miller integrator using a two-stage OTA, a pseudoresistor and a capacitor

Miller integrator amplifies signals in low frequencies and attenuates the high frequencies. Moreover, miller integrator exhibits a dc gain equal to the two-stage amplifier's gain and has its corner frequency at [6]:

$$\omega = \frac{1}{\tau \cdot A_o}$$

$$\tau = R_{eq} C_I$$

Where

- A_o is the dc gain of the two stage amplifier.
- τ is the time constant of the integrator.
- R_{eq} is the equivalent resistance of the pseudoresistor.
- C_I is the integrator's feedback capacitor.

We observe that large time constant is attained for high capacitance and resistance values. Nonetheless, high capacitances require large dimensions occupying increased area which must be avoided for integrated devices for use in implants. Aiming to use small area capacitor, which exhibits low capacitance, it is necessary to use very high resistance. Therefore, the pseudoresistor topology described earlier is of high importance since it offers high resistance while occupying small area. The miller integrator will be used as a dc offset cancelling amplifier in the top-level design as we will see in paragraph 6.5.1.

6.4 Current Mirror OTA

The current mirror OTA topology is one of the most popular OTA topologies and is used in many applications. It is considered as single-stage OTA since it consists of a differential pair and a few current mirrors. Additionally, it is a suitable candidate for low-voltage low-power applications as it exhibits low power consumption and high output impedance. Finally, large transconductance, slew rate and gain bandwidth are accomplished with this topology [20].

6.4.1 Circuit Topology

In figure Figure 6.9 the schematic of the amplifier is shown. PMOS transistors $M_{1,2}$ implement a differential pair while diode-connected NMOS transistors $M_{3,4}$ act as loads for the differential pair [21]. PMOS transistors $M_{5,6,12,12}$ employ a cascode mirror used for the biasing of the differential pair.

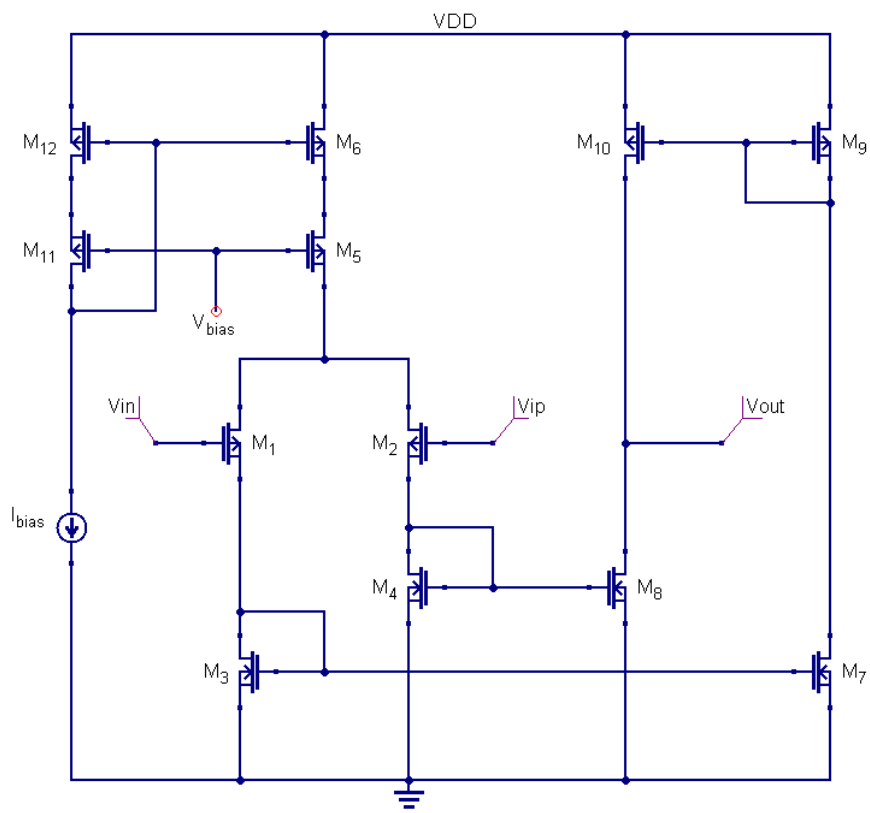

Figure 6.9 Current Mirror OTA topology

6.4.2 Transfer Function

For an amplifier, the DC gain can be calculated from the following formula:

$$A = g_m \cdot R_{out}$$

Where g_m is the amplifier's transconductance and Rout is the output resistance. For the current mirror OTA, the DC gain is given by:

$$A_o = g_m \cdot (r_{ds8} // r_{ds10}) \qquad \text{or} \qquad A_o = \frac{g_m}{g_{ds8} + g_{ds10}}$$

Where g_m is the transconductance of the input transistros $M_{1,2}$ and g_{ds8}, g_{ds10} is the output conductance of the output transistors M_8 and M_{10}, respectively.

The poles and the zeros of the OTA are:

$$\omega_{p1} = \frac{g_{ds8} + g_{ds10}}{C_L}$$

$$\omega_{p3,4} = \frac{g_{m3,4}}{C_{3,4}}$$

$$\omega_{p10} = \frac{g_{m10}}{C_{10}}$$

$$\omega_z = 2 \cdot \omega_{p10}$$

Where,

- C_L is the capacitance of the capacitive load at the output of the amplifier.
- $C_{3,4}$ are the total capacitances seen at the gates of transistors $M_{3,4}$
- C_{10} is the total capacitance seen at the gate of transistor M_{10}

The dominant pole is ω_{p1} because it is set from the load capacitance which is higher than capacitances created by MOSFETs. Substituting $g_{ds8} + g_{ds10}$ with the open loop gain equation the dominant pole is given by:

$$\omega_{p1} = \frac{g_m}{A_o C_L}$$

6.4.3 Input-Referred Noise

If we replace the small signal equivalent and the noise sources for each transistor, we can find the formula for the input-referred noise of the OTA. In our analysis, we will consider only thermal noise for aims explained in the following lines.

Flicker noise corner frequency: the frequency where the magnitudes of the thermal (white) noise and the flicker noise are equal (see Figure 6.10) [22].

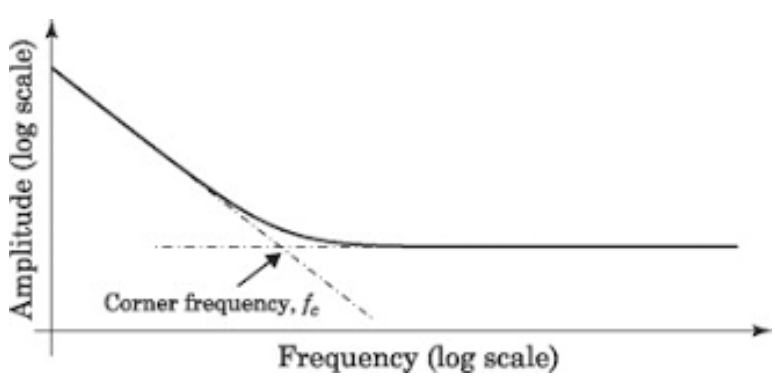

Figure 6.10 Noise vs frequency

Flicker noise: Input transistors of the amplifier are selected to be PMOS because they exhibit less flicker noise than NMOS devices. Moreover, for large geometries lesser flicker noise is produced, as shown by the expression below, and flicker noise corner frequency is shifted downwards. Thus, in our design we select large input transistors to reduce flicker noise corner frequency (about 100Hz) and the total noise of the amplifier is dominated by the thermal noise.

$$S_{\Delta VG}(f) = \frac{\mathrm{KF}}{\mathrm{Cox} \cdot \mathrm{W} \cdot \mathrm{L}} \cdot \frac{1}{\mathrm{f}}$$

Current Mirror OTA Thermal Noise: For long channel devices, the thermal noise power of the current mirror OTA results from equation [6]:

$$\mathrm{v}^2{}_{\mathrm{ni,thermal}} = 2 \cdot \mathrm{v}^2{}_{\mathrm{n1}} + 4 \cdot \mathrm{v}^2{}_{\mathrm{n3}} \cdot \left(\frac{\mathrm{g_{m3}}}{\mathrm{g_{m1}}}\right)^2 + 2 \cdot \mathrm{v}^2{}_{\mathrm{n9}} \cdot \left(\frac{\mathrm{g_{m9}}}{\mathrm{g_{m1}}}\right)^2$$

$$\mathrm{v}^2{}_{\mathrm{ni}} = \frac{4 \cdot \mathrm{k} \cdot \mathrm{T} \cdot \mathrm{n} \cdot \gamma_{\mathrm{i}}}{\mathrm{g_{mi}}} \cdot \Delta \mathrm{f}$$

$$\mathrm{g_m} = \frac{\mathrm{I_D}}{\mathrm{U_T} \cdot \mathrm{n}} \cdot \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + \mathrm{IC}}}$$

Where,

- $\mathrm{v}^2{}_{\mathrm{ni}}$ is the thermal noise power of the ith transistor .
- γ_{i} is the thermal noise factor of the ith MOSFET and is equal to $\frac{1}{2}$ in WI and $\frac{2}{3}$ in SI
- $\mathrm{g_{mi}}$ is the ith transistor transconductance

Substituting $\mathrm{g_m}$ into thermal noise expression, we get:

$$\mathrm{v}^2{}_{\mathrm{ni,thermal}} = \left[8\mathrm{k} \cdot \mathrm{T} \frac{\mathrm{n}^2 \cdot \mathrm{U_T}}{\mathrm{I_{D1}}} \frac{1}{\mathrm{G(IC_1)}} \left(\gamma_1 + 2\frac{\mathrm{G(IC_3)}}{\mathrm{G(IC_1)}}\gamma_3 + \frac{\mathrm{G(IC_9)}}{\mathrm{G(IC_1)}}\gamma_9\right)\right] \Delta \mathrm{f}$$

Like for the two-stage OTA described in paragraph 6.1, the expression of noise for the current mirror OTA show us that if it is desired to minimize the input-referred noise, we must select low ICs (WI) for the input transistors at the differential pair and high ICs(SI) for the current mirror transistors. As mentioned at the beginning of the analysis, flicker noise can be neglected for large input devices and hence the thermal noise, given above, is equal to the input-referred noise for the frequencies of the application.

6.5 Bioamplifier

The scheme of the bioamplifier implemented in this work is a grouping of the subcircuits studied in the previous paragraphs. The bioamplifier, with a capacitive load (C_L) at its output, is depicted in figure Figure 6.11. We observe that the feedback is connected to the positive input of A1 and seems like it employs positive feedback. In Fact, A1 has a negative feedback because the miller integrator inverts the signal.

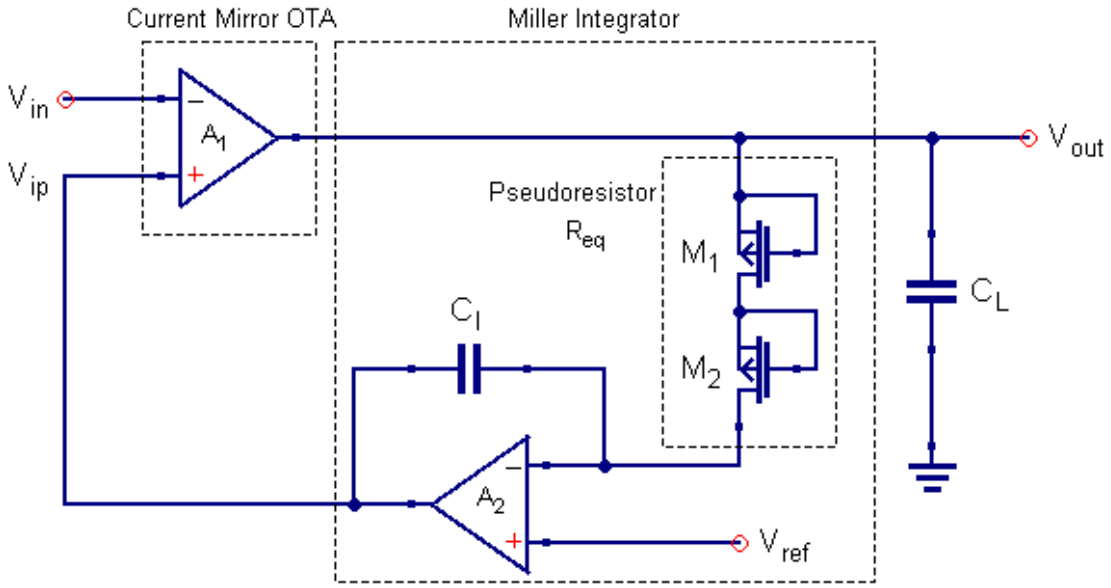

Figure 6.11 Bioamplifier Scheme

It is useful now to consider what features, of the bioamplifier, each sub-circuit affects[6].

Midband gain, A:
Bioamplifier's midband gain is equal to the low-frequency open loop gain of the current mirror OTA (A1), A_{o1}.

$$A = A_{o1}$$

$$A_o = \frac{g_m}{g_{ds8} + g_{ds10}}$$

We observe that transconductanses of $M_{1,2}$ input transistors and output conductances of $M_{8,10}$ output transistors in A1 are crucial design parameters. We must carefully select the sizing and biasing of these transistors to accomplish a good gain

Highpass cutoff frequency (-3dB), f_{hp} : The highpass cutoff frequency of the bioamplifier is a function of Miller integrator's time constant, $\tau = R_{eq} \cdot C_I$, and open loop gain of A1.

$$f_{hp} = \frac{1}{2\pi} \cdot \frac{A_{o1}}{R_{eq} \cdot C_I}$$

Lowpass cutoff frequency (-3dB): The lowpass cutoff frequency of the bioamplifier results from the dominant pole of amplifier A1.

$$f_{lp} = \frac{1}{2\pi} \cdot \frac{g_m}{A_{o1} \cdot C_L}$$

Where g_m is the transconductance of PMOS transistors (M_1,M_2) at the input of A1.

6.5.1 Miller Integrator as DC Cancelling Circuit

Dynamic offset compensation techniques can be accomplished with two techniques, auto-zeroing and chopping. In auto-zeroing, firstly the offset is measured and then it is subtracted from the input [23]. The Miller integrator is used in the bioamplifier as an offset detector. It detects the offsets by integrating the output signal of the amplifier A1 and applies a correction voltage at the positive input of A1 ,representative of the offset amount detected. Since the transfer function of the Miller integrator is that of a low pass amplifier, only the low frequency signals are fed back to the positive input of amplifier A1 and subtracted from the input signal because the integrator attaches a negative sign to them. Its low-frequency gain is defined by the

gain of A2 amplifier, A_{o2}. The corner frequency is a function of integrator's time constant, τ, and the dc gain of A2 amplifier.

Integrator gain: $A_{miller} = A_{o2}$

Integrator corner frequency: $\omega = \frac{1}{\tau \cdot A_{o2}}$

To accomplish a wide dynamic range for the bioamplifier, dc offsets must be reduced as much as possible [24]. As shown in the expression for f_{hp}, the bioamplifier's highpass cutoff frequency is controlled by the gain of the signal amplifier, A1, and integrators' time constant, τ.

Output-Referred Noise: Since the output of the Miller integrator is connected to the positive input of A1 amplifier, the estimation of output-referred noise presented at the Miller integrator is necessary because it contributes to the bioamplifier's input-referred noise. Noise sources in the Miller integrator are the two stage OTA (A2), the pseudoresistor (R_{eq}) and the electrode of reference voltage which exhibits resistance. The total noise output power for the integrator is given by:

$$v^2{}_{no} = (e^2{}_n + e^2{}_{tRef} + i^2{}_{n2}R^2{}_{ref})(f_{lp} - f_{hp}) + \left(\frac{e^2{}_{tReq}}{\tau^2} + \frac{i^2{}_{n1}}{C^2{}_I}\right)\frac{f_{lp} - f_{hp}}{f_{lp} \cdot f_{hp}}$$

Where,

- e_n is the input-referred noise spectral density of A2
- e_{tRef} is the thermal noise spectral density caused by the reference electrode
- e_{tReq} is the thermal noise spectral density caused by the pseudoresistor
- i_{n1} is the input current noise spectral density for OTA A2
- i_{n2} is the current noise spectral density compose of shot noise and thermally induced gate-current noise
- f_{lp} and f_{hp} are the lowpass and highpass cutoff frequencies respectively τ is integrators time constant
- C_I is the capacitance of the feedback capacitor in the integrator

In the expression of output noise power, we notice that noise contributions from the pseudoresistor, e_{tReq}, and the input currents of A2, i_{n1}, can be neglected because of the time constant τ and the feedback capacitance, C_I, which reduce them. Additionally, i_{n2} is much lesser than the resistance of the reference electrode and hence the noise source $i^2{}_{n2} \cdot R^2{}_{ref}$ contribution is insignificant [25]. Taking into

consideration the above mentioned, we conclude that the noise of integrator is dominated by the noise of A2. Therefore, the total noise output power of the integrator is given by:

$$v^2{}_{no} = e^2{}_n(f_{lp} - f_{hp})$$

The analysis that got done previously for the input-referred noise of A2, gives us an insight into the reduction of integrator's output noise power.

6.5.2 Input-Referred Noise

The input-referred noise of the bioamplifier results from the noise contribution of both A1 amplifier and Miller integrator. To diminish the noise, we must reduce the noise of both the current mirror OTA, A1, and the Miller integrator. Nonetheless, because of the design tradeoff between noise and power consumption, the noise impact of Miller integrator can be disregarded if we bias it with double current compared to the biasing current of A1.

6.6 Design

As already mentioned, the amplifier was designed with the guidance of the IC methodology. After finding the equations for the behavior of all subcircuits and the total circuit, we chose the IC, the dimensions, and the biasing of each transistor so that the bioamplifier is within the specifications. Next, we designed the circuit in 90 nm TSMC technology in the Virtuoso program and simulated it with the Specter simulator. The results were relatively close to the estimated by the hand calculations but to achieve better accuracy, we made small changes to the design, which is always the case in analog circuit design. In this section we will present in detail the design of the circuits described in this chapter and list their schematics and simulations.

In all subsequent schematics the supply voltage is the maximum possible so that there is no risk to damage the MOSFETs. For a 90 nm technology, maximum voltage is equal to 1.2V, $V_{DD} = 1.2$ V and Vss = 0 V. Also, at the differential pair of A1 the voltage biasing gate is equal to half the supply voltage, V_G =600mV so as to ensure that the DC output voltage of the amplifiers is equal to 600mV and will allow almost the same voltage change for negative and positive input voltage.

6.6.1 Two Stage OTA

In figure Figure 6.12, OTA A2 is illustrated. The dimensions and operating points for transistors are shown in Table 1. For the compensation of the amplifier a resistor R_z=100kΩ and a capacitor C_c=3pF are connected from the output node to the drain of M_2.

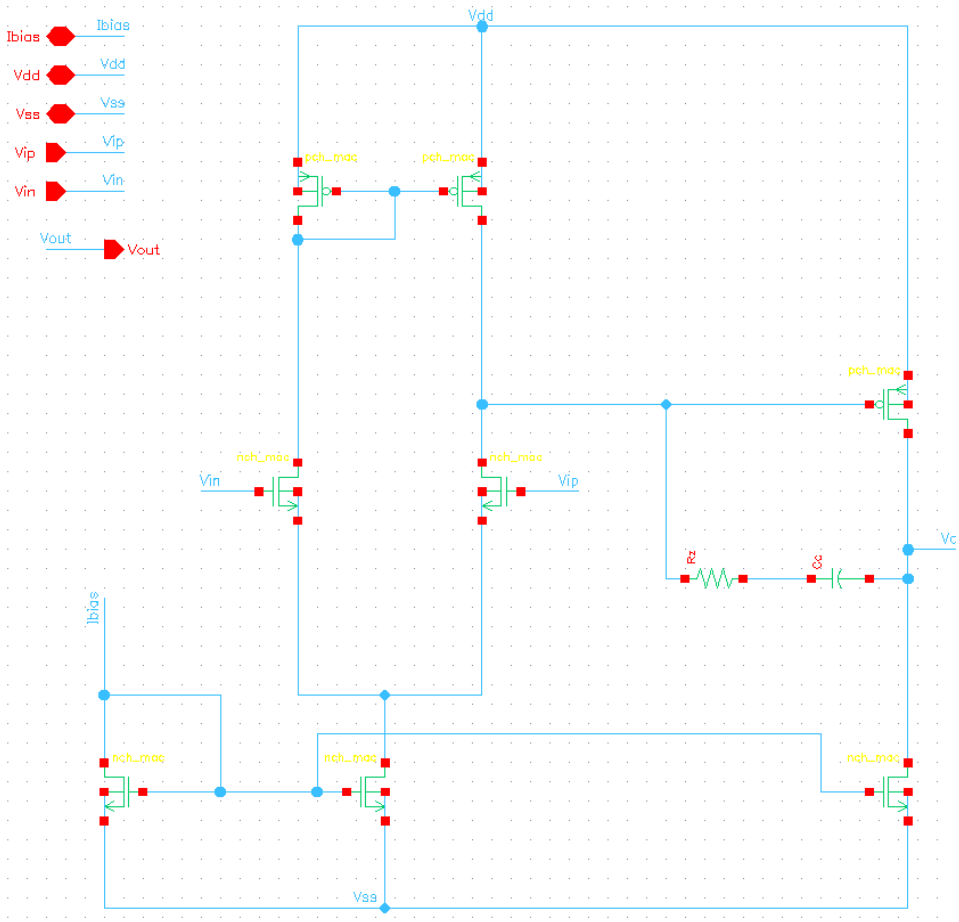

Figure 6.12 Two stage OTA with lead compensation topology in 90 nm TSMC process

Table 1

Dimensions and operating points for transistors in A2

Type	MOS	ID(µA)	IC	W(µm)	L(µm)	$V_{ds,sat}$(mV)	g_m(norm.)
NMOS	$M_{1,2}$	1	0.01	465.1	4	104	0.99
PMOS	$M_{3,4}$	1	5.5	14.5	20	201	0.34
NMOS	$M_{5,6,8}$	2	7	1.3	4	216	0.31
PMOS	M_7	2	0.1	80	1	108	0.91

We can see in Table 1 that all transistors are long and wide. This design choice was made to reduce flicker noise as much as possible. The bias current of the circuit was selected to be 2 μA and input transistors M_1,M_2 are selected to operate in deep weak inversion to maximize their transconductance. This design options were made with respect to an acceptable noise performance according to the expressions shown in paragraph 6.1.3. Additionally, M_1 and M_2 have multi-finger gates (16 fingers) for further reduction of their thermal noise contribution [14]. Transistors M_3 and M_4 operate in moderate inversion because for a selected biasing current (I_{bias}=2uA ⇒ $I_{D3,4}$=1uA), going towards weak inversion results in a better matching for the current mirror. M_7 operates in weak inversion to achieve high transconductance and low $V_{DS,sat}$.. The current mirrors M_5,M_6,M_8 are in moderate inversion to get good matching and reduce their $V_{DS,sat}$. This intention to reduce the saturation voltage of output transistors is due to the fact that high saturation voltages at the output reduce the dynamic range of the amplifier. Additionally, the high transconductances attained for the input transistors of each stage, increase amplifier's gain (see open loop gain in paragraph 6.1.2). Finally, we see that the aspect ratios ($\frac{W}{L}$)of transistor M_5,M_6,M_8 are equal. Therefore, the bias current is equal to 2uA for both the differential amplifier and the common source amplifier.

Open loop gain, phase and noise simulation: To measure the open-loop gain of the amplifier, we use the circuit shown in Figure 6.13. The time constant RC must be well below the amplifier's dominant pole and hence we select high values for R and C (C=1F,R=10MΩ). The voltage-controlled voltage source (VCVS) in the feedback path is used to buffer the output because direct connection of the resistor to the output may shift the amplifier's bias points. Under this configuration, amplifier's dc output voltage will be very close to the dc voltage of the input. The little difference between dc output voltage and dc input voltage is called dc input-offset. To simulate the open-loop gain, an AC magnitude equal to 1 is set to the input voltage source. This allows us to measure the gain directly from the AC output voltage since the transfer function is given by $V_{out(s)}/V_{in}(s)$ and $V_{in}(s)=1$. The BODE plot of the amplifier A2 and its input-referred noise are depicted in figures Figure 6.14 and Figure 6.15 respectively.

We notice that the amplifier shows a high open loop gain of 60dB. Also, has only one pole thanks to the applied compensation technique. The phase margin is :

$$PM=180^0+\varphi$$

Where φ is the phase when gain is equal to 1dB (or $0\frac{V}{V}$) and hence $PM=56{,}8^0$.

From the plot of input-referred noise we see that the flicker noise corner frequency is very low (a few hundred Hz), like we want it to be. Its rms noise for the frequency range 100Hz-10kHz is equal to V_{rms} =3 uV.

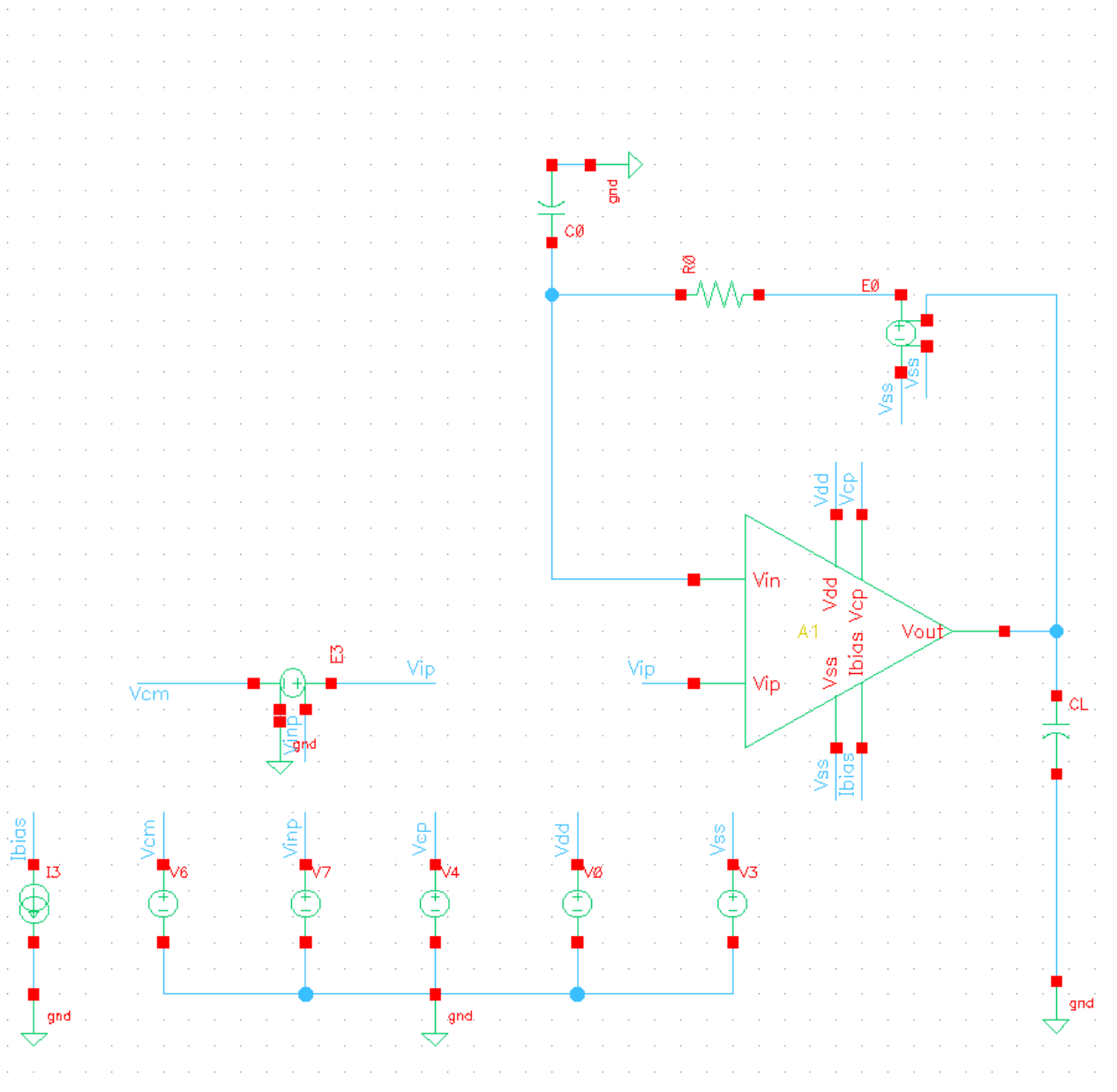

Figure 6.13 Setup for measuring A2 gain, phase and input-referred noise

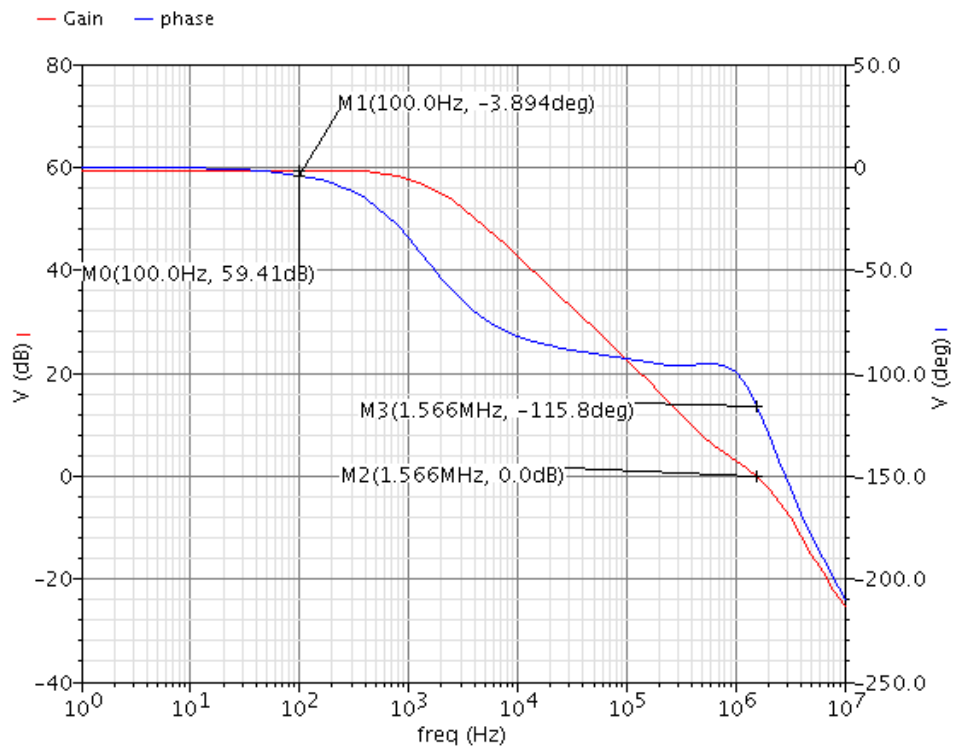

Figure 6.14 A2 BODE plot

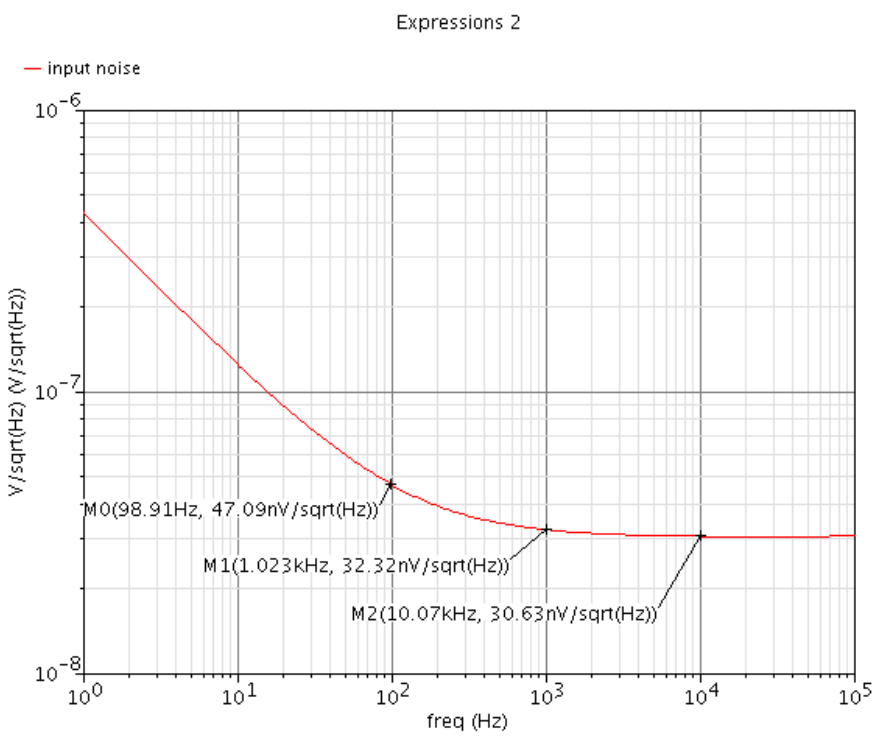

Figure 6.15 A2 input-referred noise

6.6.2 Pseudoresistor

For the PMOS devices of the pseudoresistor, minimum process dimensions were selected, W=125nm and L=100nm. The method to measure their resistance was to sweep the DC supply voltage from negative to positive values and divide it by the drain current.

$$R_{eq} = \frac{V_{DD}}{I_D}$$

Results are shown in Figure 6.16. We observe that high resistance, $R_{eq} \approx 16.5$ GΩ is achieved for low voltage drop |ΔV|.

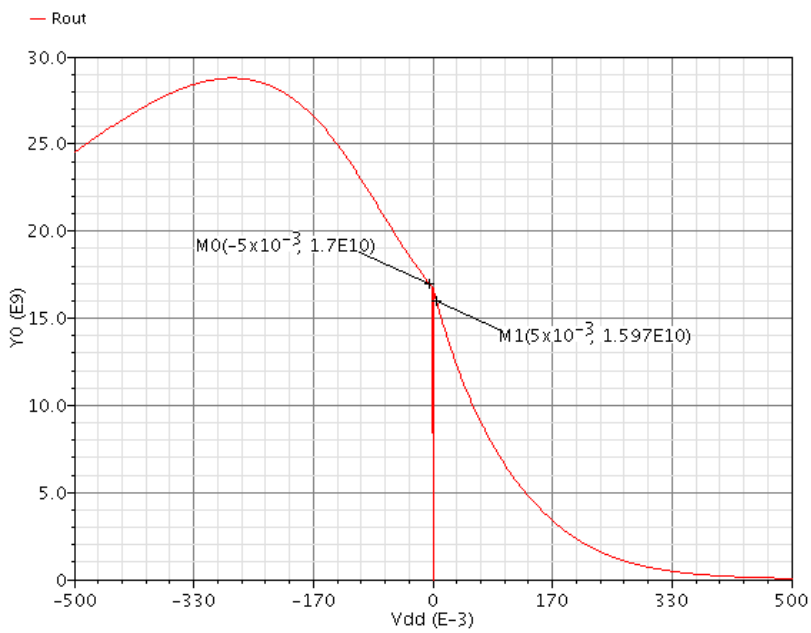

Figure 6.16 Pseudo resistor output resistance vs voltage drop across it

6.6.3 Miller Integrator

For the Miller Integrator, we set the feedback capacitor $C_I = 53$ pF to establish bioamplifier's highpass cutoff frequency to 125.8 Hz (see 6.5). The voltage V_{ref} is zero and is replicated to A1 positive input (V_{ip}) for providing common mode voltage rejection. If a DC offset appears at bioamplifier's output, the Miller integrator adapts its output proportionally to the offset seen at the output of the bioamplifier. Thus, it changes the biasing to reject the counterbalance.

Gain, phase and noise simulation: Integrator's gain, phase and noise was simulated with the configuration in Figure 6.17. The BODE plot is shown in Figure 6.18. The noise of interest for the integrator, as we said in our previous discussions, is the output-referred and is shown in Figure 6.19.

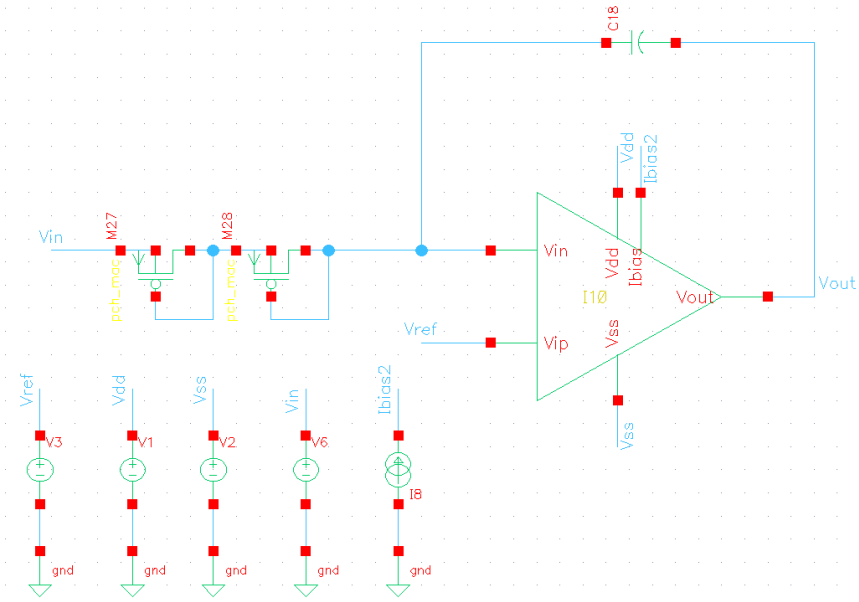

Figure 6.17 Setup for measuring Miller Integrator's gain, phase and input-referred noise

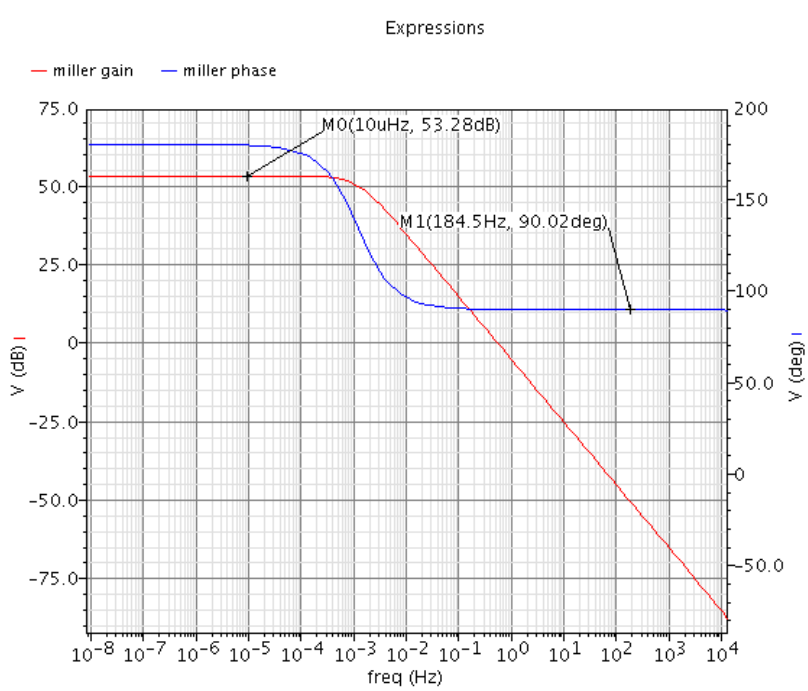

Figure 6.18 Miller integrator's BODE plot

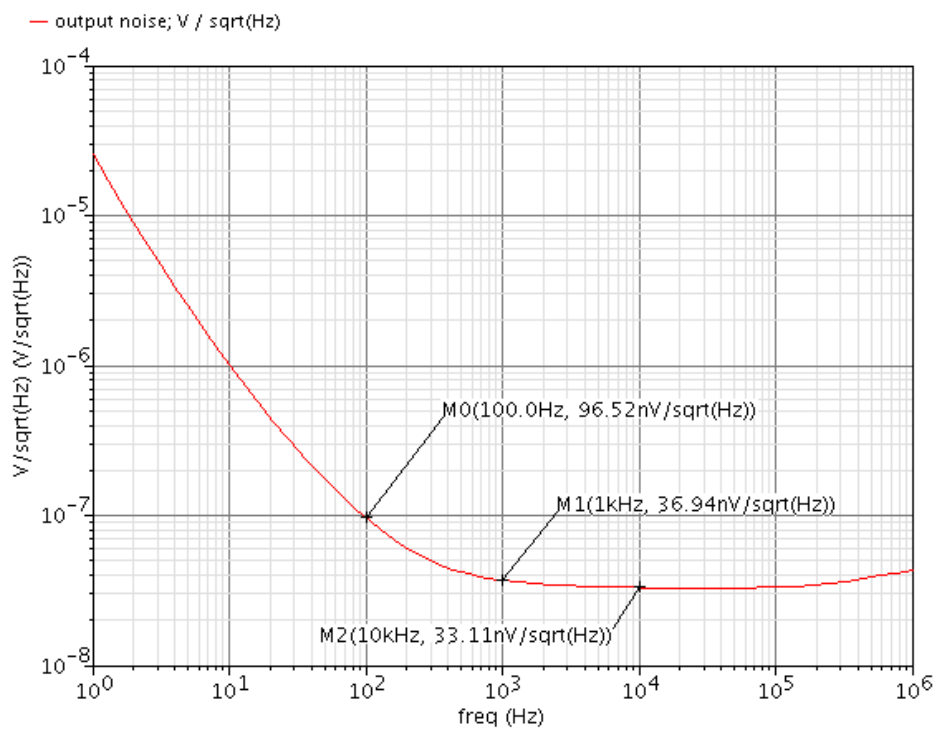

Figure 6.19 Miller integrator's output-referred noise

6.6.4 Current Mirror OTA

In Figure 6.20, OTA A1 is illustrated. The dimensions and operating points for transistors are shown in Table 2. The bias current of the circuit was selected to be 1 μA considering its impact in noise. The selection of inversion coefficients for A1 was made with the same reasoning as for A2. We chose large dimensions for flicker noise reduction and we accomplished thermal noise reduction by sizing input transistors in such a way that they have much higher transconductance than transistors in current mirrors (see noise analysis in 6.4.3).

Bioamplifier's gain is equal to the DC gain of A1 which is increased for high transconductances at the input transistors, $M_{1,2}$, and low output conductances at the output transistors, $M_{7,8,9,10}$ (see gain in 6.4.2). We achieved high transconductances for M_1 and M_2 by operating them in deep weak inversion. However, output conductance of $M_{8,10}$ is difficult to predict because it is vulnerable in second order effects [26]. In a first order approximation, output conductance can be given by [27]:

$$g_{ds} = \frac{I_D}{V_A}$$

$$V_A = V_{AL} \cdot L$$

Where,

- V_A is the Early voltage
- V_{AL} is a quality factor that describes how much V_A is produced for a given L and is a function of IC, L and V_{DS}.

For a given IC, L and V_{DS}, V_A has a specific value. From the above expressions we realize that as channel length increases, V_A increases too and g_{ds} decreases. The explanation of this phenomenon is the fact that for larger devices, channel length modulation is reduced. Also, for devices above the process minimum length, V_A increases rapidly with L because of the decreased DIBL effect for large devices. When V_{DS} is high enough, V_A increases linearly with L [27]. From the above, we conclude that for an increased gain in A1, large devices must be placed at its output. As we can see, these devices are implemented using three stacked MOSFETs for each. That is because the maximum channel length allowed in 90 nm TSMC process is 20 µm. To reduce power dissipation, current mirrors $M_{3,7}$ and $M_{4,8}$ divide the bias current by a factor of 2. To conclude the design, a low voltage cascode mirror is composed of MOSFETs $M_{5,6,11,12}$ and is used for the biasing of the amplifier. These transistors operate in moderate inversion for good matching and high output impedance in the current source. Such operation improves CMRR [18].

Gain, phase and noise simulation: To simulate open-loop gain, phase and input-referred noise of A1 we did the same setup as for A2 (Figure 6.21). The BODE plot and the input-referred noise for A1 are shown in Figure 6.22 and Figure 6.23, respectively.

Table 2

Dimensions and operating points for transistors in A1

Type	MOS	ID(µA)	IC	W(µm)	L(µm)	$V_{ds,sat}$(mV)	g_m(norm.)
PMOS	$M_{1,2}$	1	0.01	900	2	104	0.99
NMOS	$M_{3,4}$	1	8	8.3	60	226	0.29
NMOS	$M_{7,8}$	0.5	8	4.2	60	226	0.29
PMOS	$M_{9,10}$	0.5	30	4.5	60	361	0.16
PMOS	$M_{5,6,11,12}$	2	4	15.4	8	184	0.39

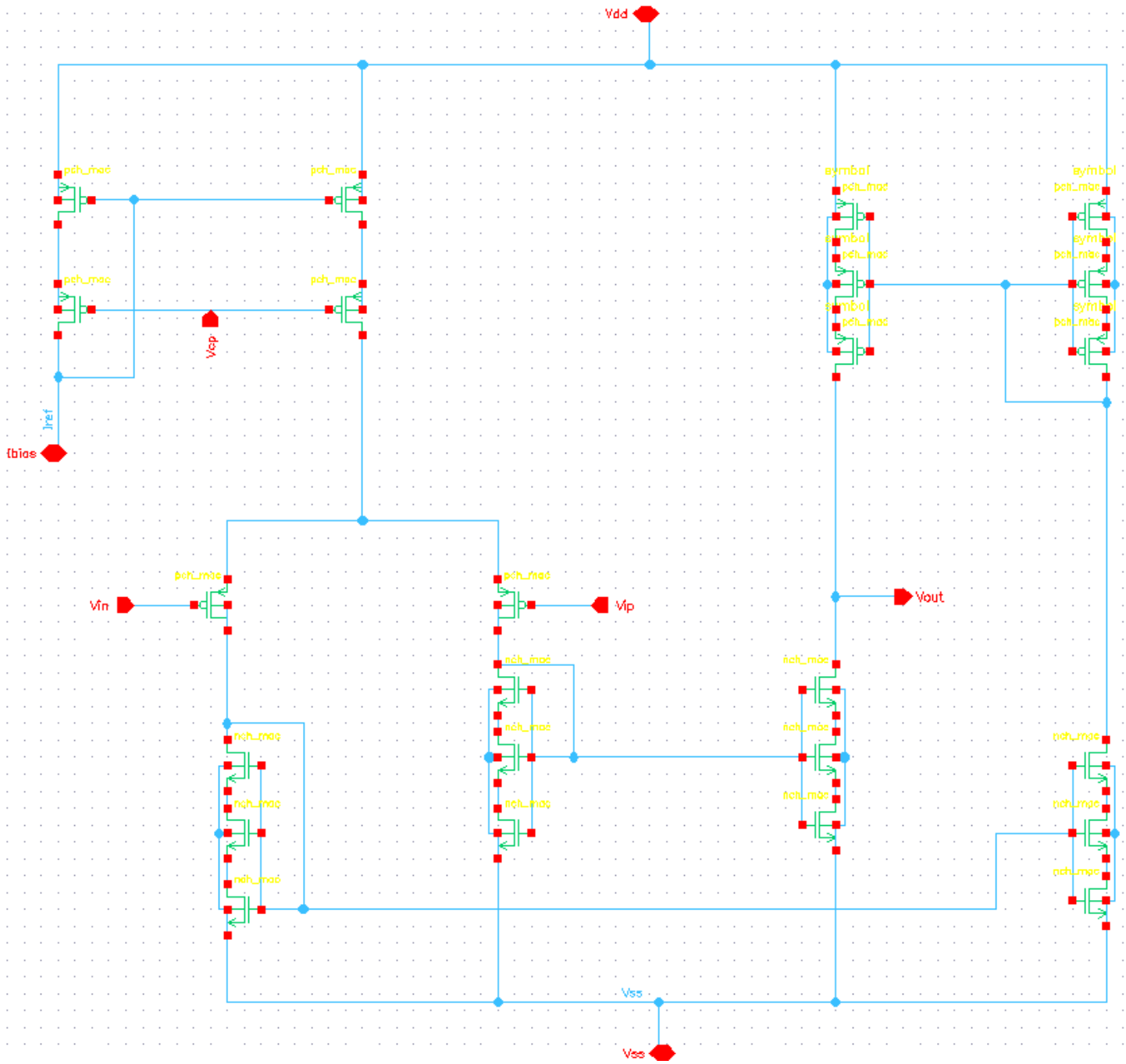

Figure 6.20 Current Mirror OTA topology in 90 nm TSMC process

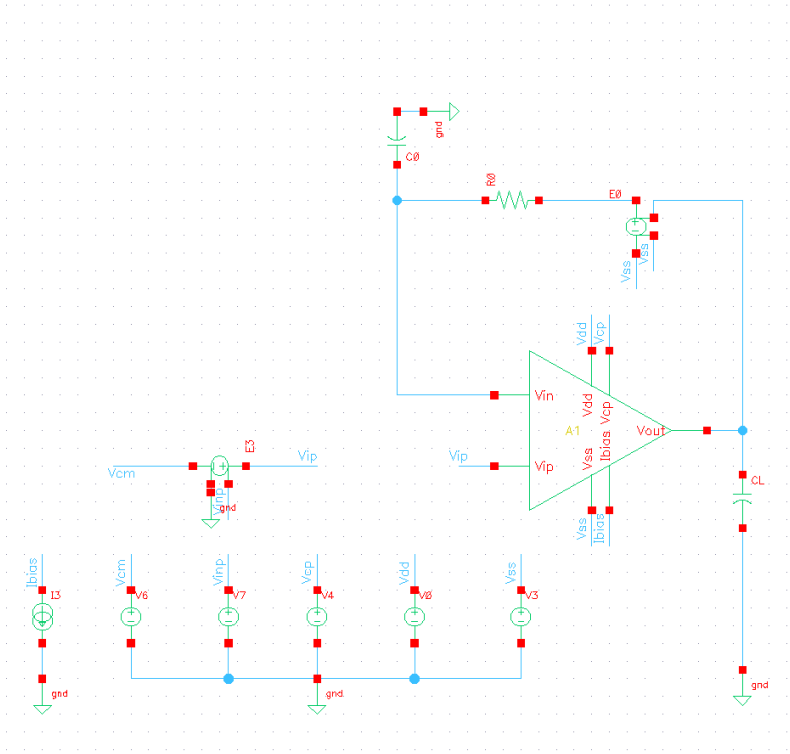

Figure 6.21 Setup for measuring A1open loop gain, phase and input-referred noise

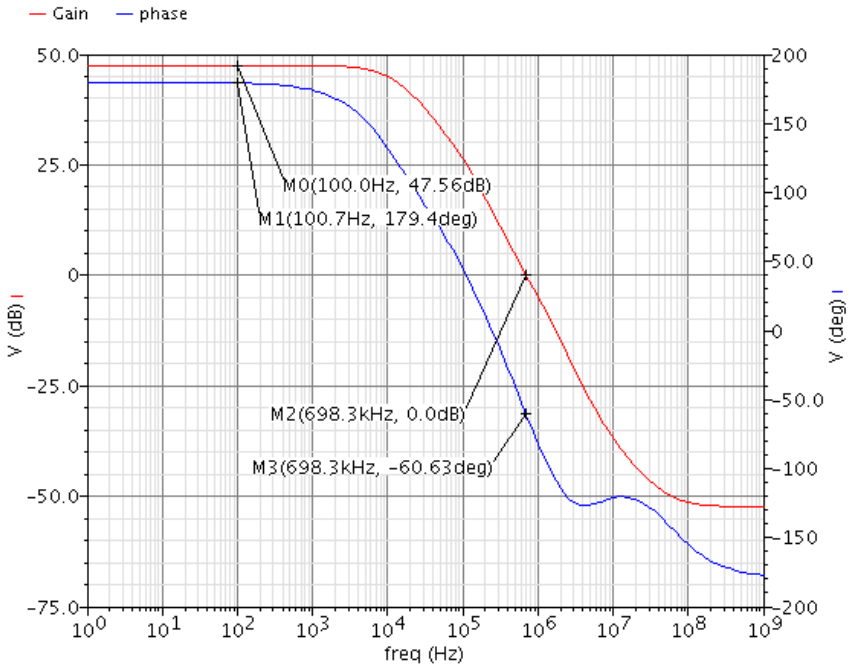

Figure 6.22 A1 BODE plot

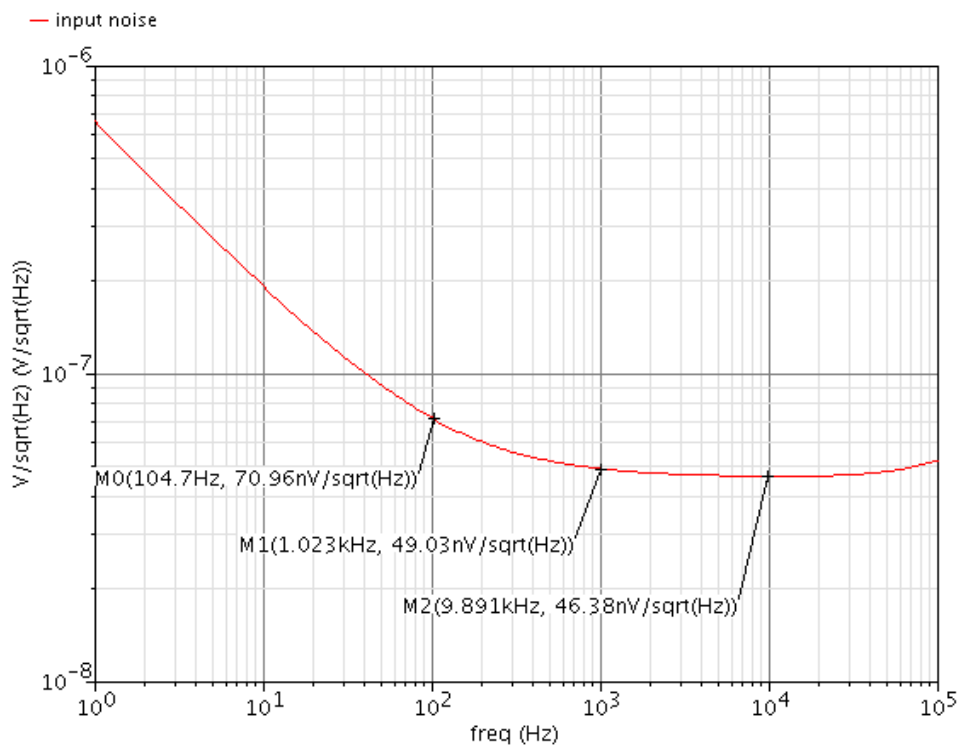

Figure 6.23 A1 input-referred noise

The amplifier produces gain 47.5 dB and rms input-reffered noise V_{rms}=4.657uV

6.6.5 Bioamplifier

By combining all of the circuits shown in the previous paragraphs, we impement the total amplifier. To simulate bioamplifier's frequency response and noise we used the circuit shown in Figure 6.24. The load capacitor is set to C_L=550 fF for a f_{lp}=10.85 kHz. All the components of the bioamplifier are summarized in Table 3. Figures 6.27-6.30 show the features after simulation of the bioamplifier.

Table 3

Bioamplifier components

C_L=550fF	C_I=53pF	V_{DD}=0.6 V	V_{SS}=-0.6 V
I_{bias1}=1 uA	I_{bias2}=2 uA	Vin_{AC_mag}=1 (phase=180^0)	$V_{ref,DC}$=0V

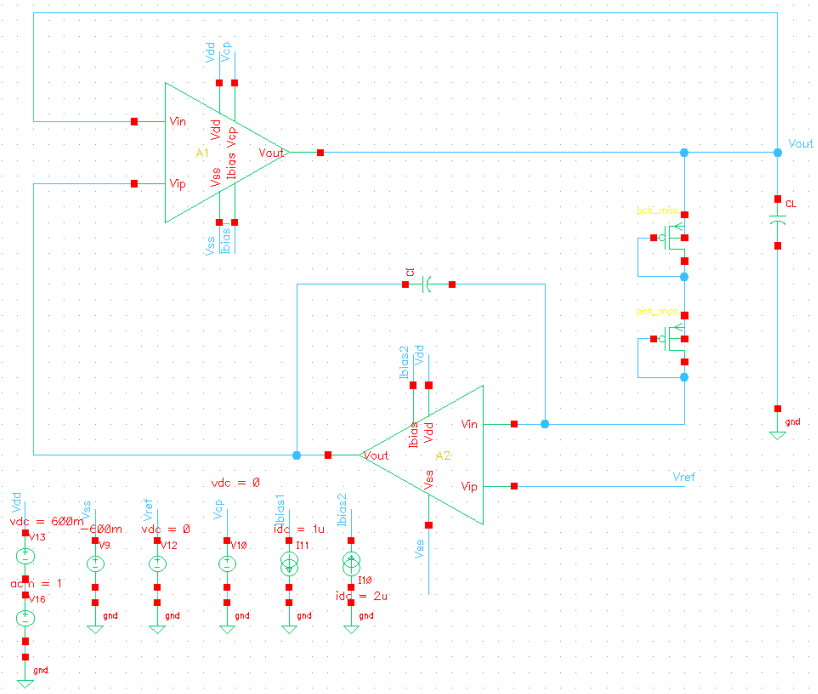

Figure 6.24 Setup for measuring Bioamplifier's open loop gain, phase and input-referred noise

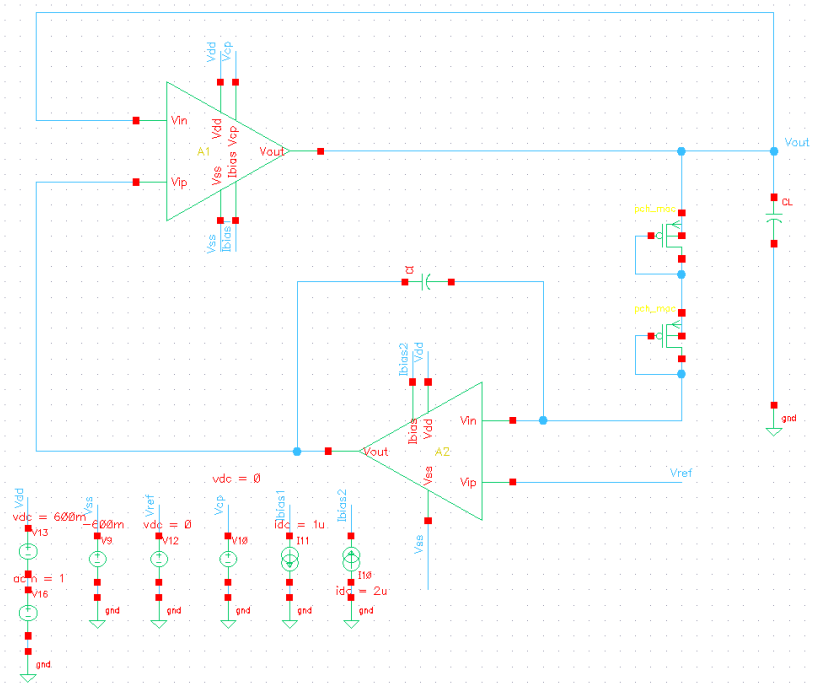

Figure 6.25 Setup for measuring Bioamplifier's PSRR

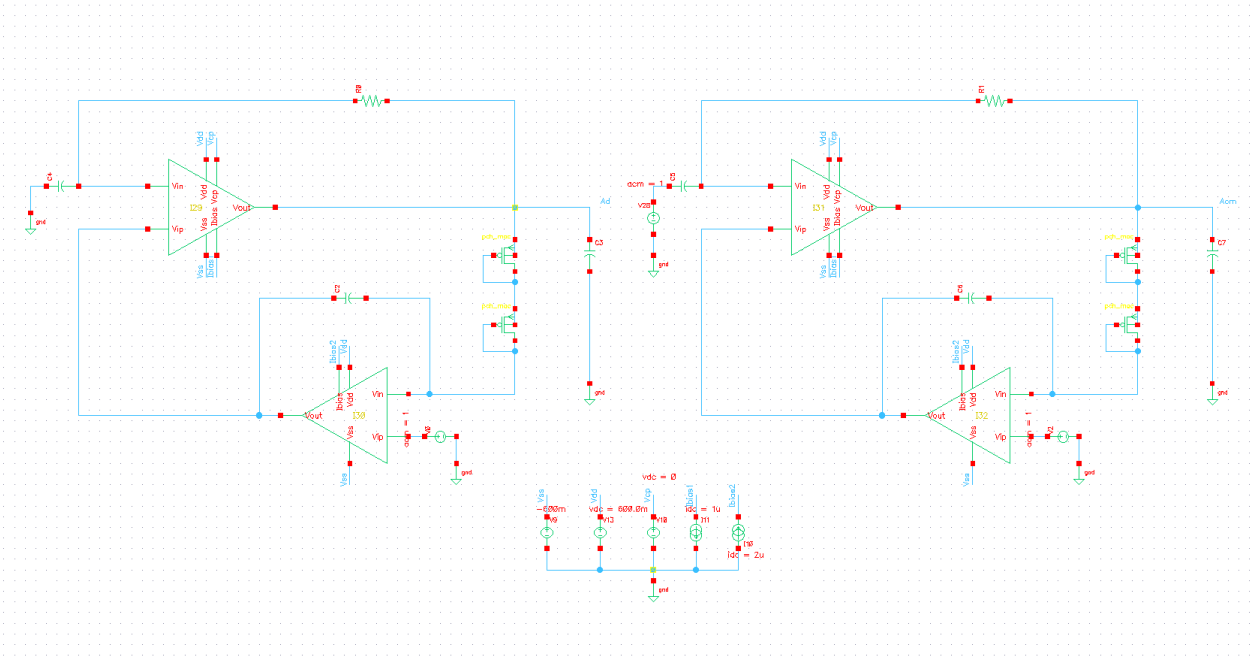

Figure 6.26 Setup for measuring Bioamplifier's CMRR

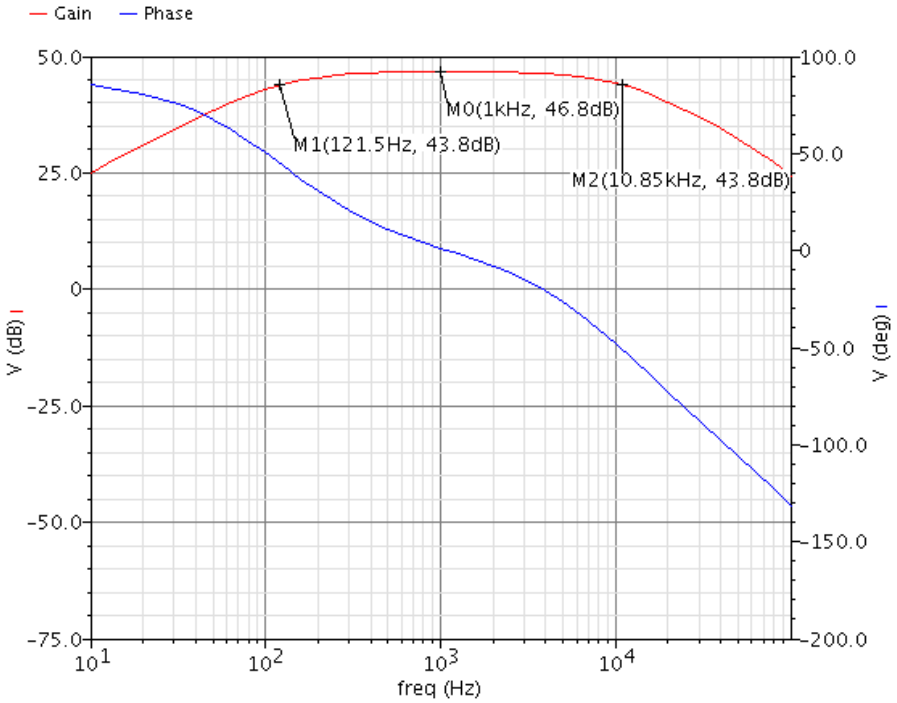

Figure 6.27 Bioamplifier BODE plot

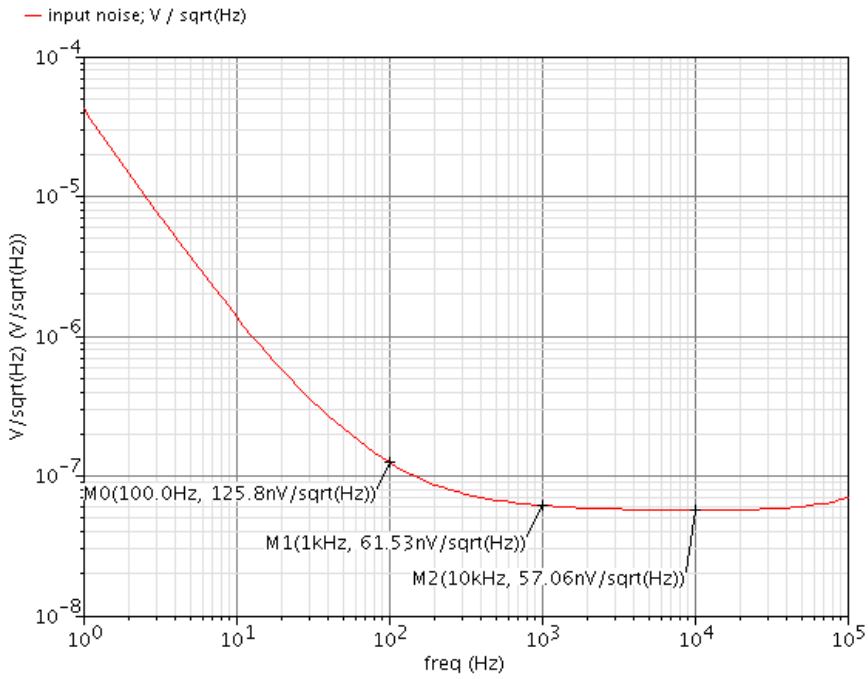

Figure 6.28 Bioamplifier input-referred noise

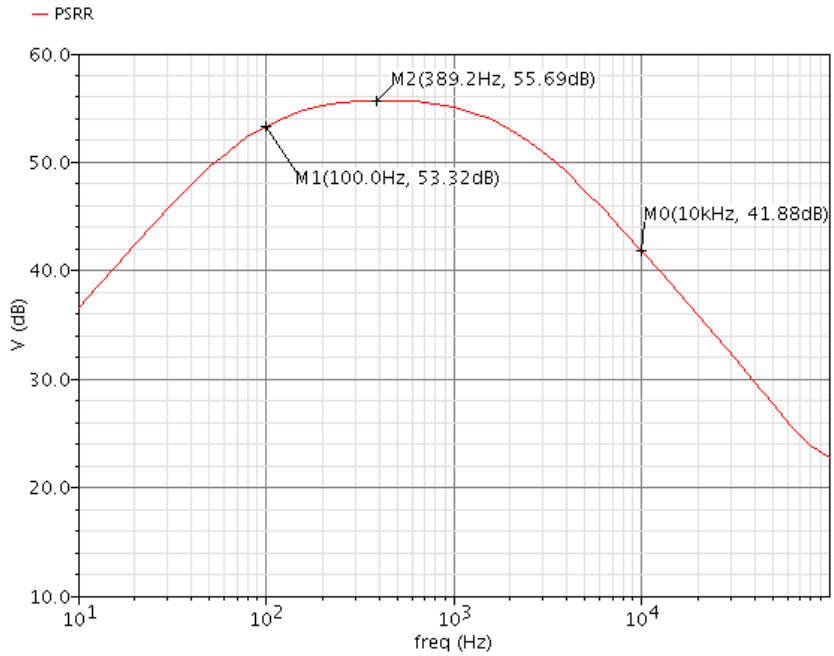

Figure 6.29 BIoamplifier PSRR

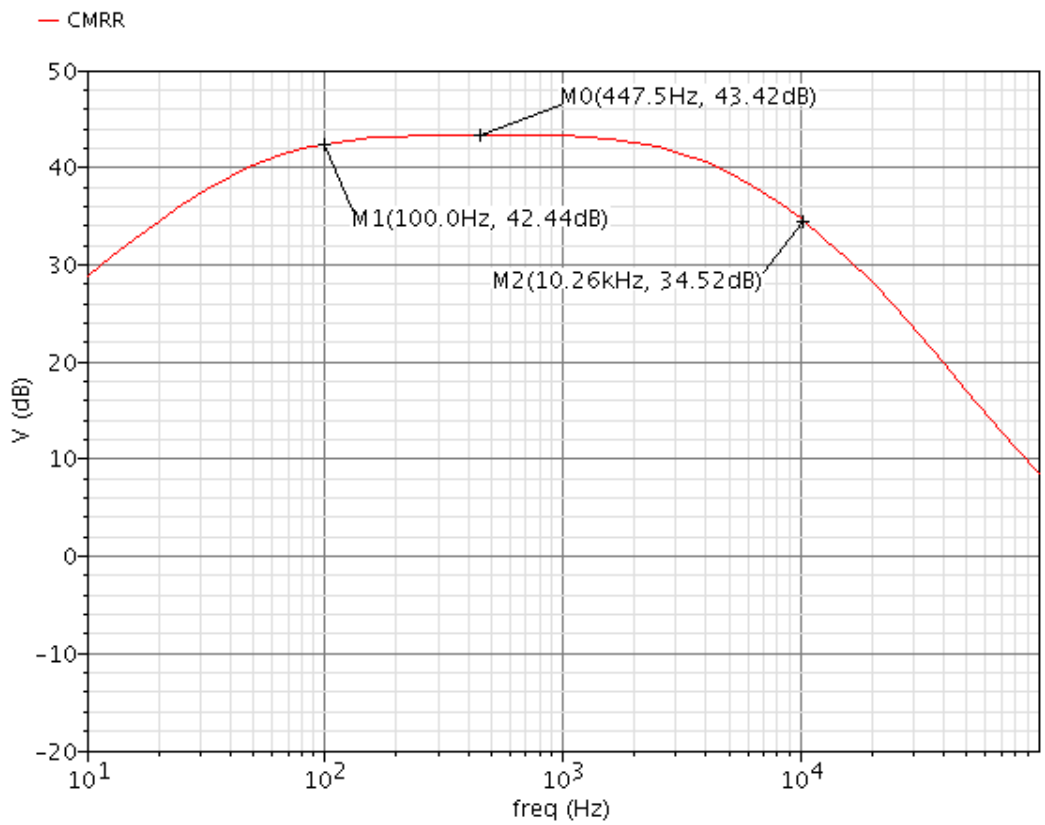

Figure 6.30 Bioamplifier CMRR

From Figure 6.31 we see that at unity-gain frequency the phase margin of the whole amplifier is 6.5^0. That's because the bioamplifier introduce a negative phase shift of -180^0, A1 has a negative phase shift of $-96{,}5^0$ and the Miller integrator has a positive phase shift of 90^0. Thus ,

$$PM=180^0+(-180^0-96.5^0+90^0)= 6.5^0$$

From the above simulation results we summarize the performance of the amplifier in Table 4.

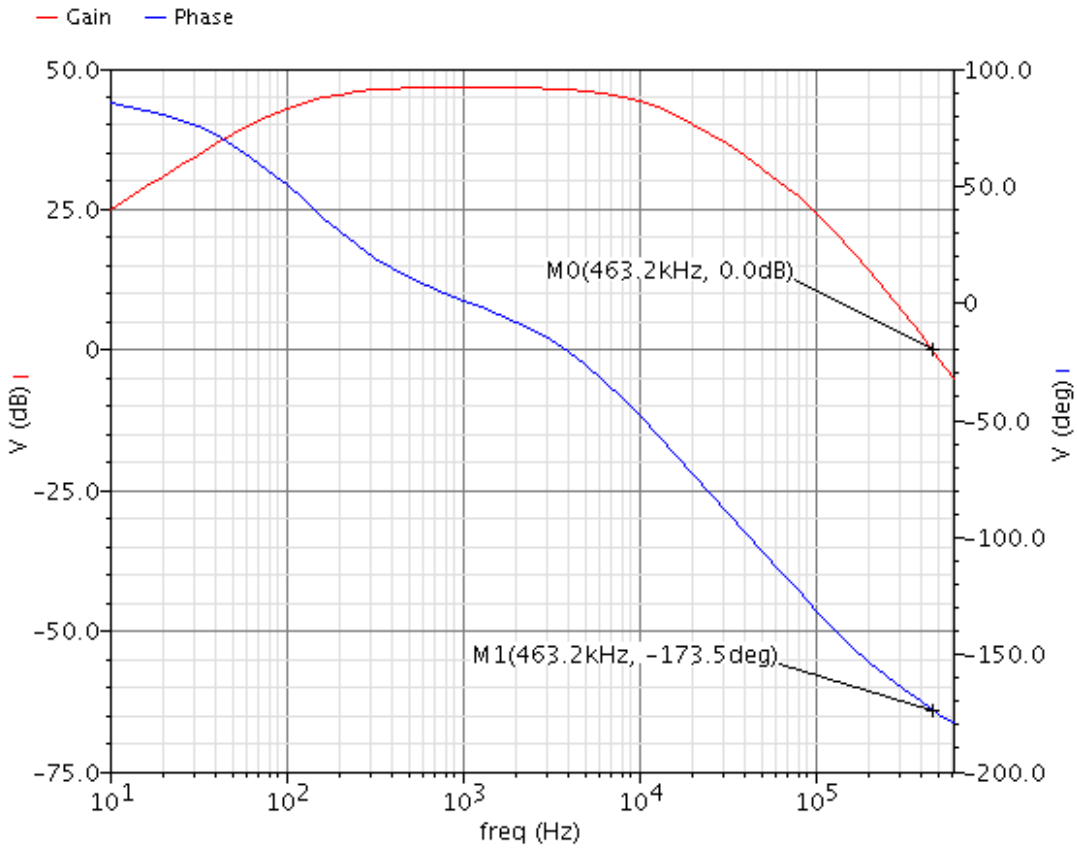

Figure 6.31 Bioamplifier phase margin

Table 4

Bioamplifier parameters

Parameter	Simulation Result
Midband gain	46.8dB
High-pass cutoff frequency	121.5 Hz
Low-pass cutoff frequency	10.85 kHz
Input-referred noise	5.8 μV_{rms}
PSRR	>41.88 dB
CMRR	>34.52 dB
Power dissipation	8.4uW

Chapter 7 Conclusion

In this work we implemented a low-power, low-noise amplifier, in a 90 nm CMOS process. The amplifier meets the specifications for implantable devices discussed in paragraph 2.6. The biosignal amplifier is designed under a 1.2V supply, with a power consumption of 8.4 μW, a mid-band gain of 47.5 dB from 113.7Hz to 10.41 kHz with input-referred noise of 6 μVrms. Its structure is beneficial for active suppression of low frequency signal parts, avoiding the use of large RC passive networks, and hence leads to a reduced overall size of the circuit. This makes it a good candidate for amplification of neural signals for the integration of multi-channel recording devices.

A similar amplifier has previously been developed in a 180 nm CMOS process [6]. The comparison between the present work and [6] is shown in Table 5. As has been discussed, the biosignal amplifier developed in the present work, which is operating under a reduced power supply of 1.2V, exhibits lower power consumption than [6], while showing similar, although slightly inferior, performance for other parameters such as gain. Overall, this outcome should be judged positive as the migration of analog circuitry to more advanced processes often is a challenging task. The bioamplifier of this work is implemented in 2 generations more advanced CMOS process compared to [6]. In digital circuits, where transistors operate as switches, supply voltage scaling and smaller device sizes are beneficial while they offer reduced power consumption and increased switching speed. However, the procedure of porting the analog part of a chip to a new process is a more demanding task, notably due to reduced voltage supply. Another problem is that advanced process nodes degrade MOSFET intrinsic small signal gain for long-channel devices, as are required for the present work. This makes it very hard to achieve high gains in analog circuits. Furthermore, the shrinking of power supply diminishes the maximum available signal swing at the output, thus reducing the maximum possible signal-to-noise ratio. Also, voltage headroom is limited and the achievement of high gain by device stacking is not feasible. Transconductance efficiency or g_m/I_D is the key FoM for power efficient circuits. In weak inversion (subthreshold) highest transconductance efficiency is achieved. Therefore, in deep submicron processes it is imperative to design in weak inversion using advanced design techniques. In conclusion, the present work has largely benefitted from using the inversion coefficient (IC) based design methodology favoring low-power, low-voltage design in weak and moderate inversion.

Table 5

Comparison between 90 nm and 0,18 μm process implementations

Parameter	This work	[6]
Process	90 nm	0,18μm
Midband gain	46.8dB	52 dB
High-pass cutoff frequency	121.5 Hz	105 Hz
Low-pass cutoff frequency	10.85 kHz	9.2 kHz
Input-referred noise	5.8 μV_{rms}	5,4 μV_{rms}
PSRR	>41.88 dB	>45 dB
CMRR	>34.52 dB	>45 dB
Supply Voltage	1.2 V	1.8 V
Power dissipation	8.4 μW	8.6 μW

Chapter 8 References

[1] Purves, Dale, et al. *Neuroscience*. Oxford University Press, 2018.

[2] Iniewski, Krzysztof. *VLSI circuits for biomedical applications*. Artech House, 2008.

[3] Yang, Tan, and Jeremy Holleman. "An ultralow-power low-noise CMOS biopotential amplifier for neural recording." *IEEE Transactions on Circuits and Systems II: Express Briefs* 62.10 (2015): 927-931.

[4] Hamilton, Franz, Tyrus Berry, and Timothy Sauer. "Tracking intracellular dynamics through extracellular measurements."*PloS one*13.10 (2018): e0205031.

[5] Srinivasan, Lakshminarayan, Lav R. Varshney, and Julius Kusuma. "Acquisition of action potentials with ultra-low sampling rates."*2010 Annual International Conference of the IEEE Engineering in Medicine and Biology*. IEEE, 2010.

[6] Gosselin, Benoit, Mohamad Sawan, and C. Andrew Chapman. "A low-power integrated bioamplifier with active low-frequency suppression." *IEEE Transactions on biomedical circuits and systems* 1.3 (2007): 184-192.

[7] Razavi, Behzad. *Fundamentals of microelectronics*. Wiley, 2008.

[8] Razavi, Behzad. *Design of analog CMOS integrated circuits*. Tata McGraw-Hill Education, 2002.

[9] Bucher, Matthias, et al. "Analysis of transconductances at all levels of inversion in deep submicron CMOS." *9th International Conference on Electronics, Circuits and Systems*. Vol. 3. IEEE, 2002.

[10] Bucher, Matthias. *Analytical MOS transistor modelling for analog circuit simulation*. Diss. Verlag nicht ermittelbar, 2000.

[11] Enz, Christian, Maria-Anna Chalkiadaki, and Anurag Mangla. "Low-power analog/RF circuit design based on the inversion coefficient." *ESSCIRC Conference 2015-41st European Solid-State Circuits Conference (ESSCIRC)*. IEEE, 2015.

[12] Enz, Christian, Francesco Chicco, and Alessandro Pezzotta. "Nanoscale MOSFET modeling: Part 1: The simplified EKV model for the design of low-power analog circuits." *IEEE Solid-State Circuits Magazine* 9.3 (2017): 26-35.

[13] Colombo, Dalton Martini, Gilson Inacio Wirth, and Christian Fayomi. "Design methodology using inversion coefficient for low-voltage low-power CMOS voltage

reference." *Proceedings of the 23rd symposium on Integrated circuits and system design*. 2010.

[14] Archanaa, M., and Karthigha Balamurugan. "Analysis of thermal noise and noise reduction in CMOS device." *2014 International Conference on Green Computing Communication and Electrical Engineering (ICGCCEE)*. IEEE, 2014.

[15] Johns, David A., and Ken Martin. *Analog integrated circuit design*. John Wiley & Sons, 2008.

[16] Jakobson, C. G., I. Bloom, and Y. Nemirovsky. "1/f noise in CMOS transistors for analog applications." *Proceedings of 19th Convention of Electrical and Electronics Engineers in Israel*. IEEE, 1996.

[17] Gray, Paul R., et al. *Analysis and design of analog integrated circuits*. John Wiley & Sons, 2009.

[18] Baker, R. Jacob. *CMOS: circuit design, layout, and simulation*. John Wiley & Sons, 2019.

[19] Mahattanakul, Jirayuth, and Jamorn Chutichatuporn. "Design procedure for two-stage CMOS opamp with flexible noise-power balancing scheme." *IEEE Transactions on Circuits and Systems I: Regular Papers* 52.8 (2005): 1508-1514.

[20] Jusoh, Wan Mohammad Ehsan Aiman Wan, and Siti Hawa Ruslan. "Design and analysis of current mirror OTA in 45 nm and 90 nm CMOS technology for bio-medical application." *Bulletin of Electrical Engineering and Informatics* 9.1 (2020): 221-228.

[21] Deo, Nikhil, Tripurari Sharan, and Tanmay Dubey. "Subthreshold biased enhanced bulk-driven double recycling current mirror OTA." *Analog Integrated Circuits and Signal Processing* (2020): 1-14.

[22] Bahreyni, Behraad. *Fabrication & design of resonant microdevices*. William Andrew, 2008.

[23] Witte, Frerik, Kofi Makinwa, and Johan Huijsing. *Dynamic offset compensated CMOS amplifiers*. Springer Science & Business Media, 2009.

[24] Nagahori, Takeshi, et al. "Offset cancelling amplifier circuit having Miller integrator as offset detector." U.S. Patent No. 5,798,664. 25 Aug. 1998.

[25] Frank, David J., et al. "Device scaling limits of Si MOSFETs and their application dependencies." *Proceedings of the IEEE* 89.3 (2001): 259-288.

[26] Schneider, M. C., C. Galup-Montero, and A. I. A. Cunha. "A single-piece charge-based model for the output conductance of MOS transistors." *1998 IEEE*

International Conference on Electronics, Circuits and Systems. Surfing the Waves of Science and Technology (Cat. No. 98EX196). Vol. 1. IEEE, 1998.

[27] Binkley, David M. "Tradeoffs and optimization in analog CMOS design." *2007 14th International Conference on Mixed Design of Integrated Circuits and Systems*. IEEE, 2007.