TCAD simulation of organic field-effect transistors based on spray-coated small molecule organic semiconductor with an insulating polymer blend

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ABSTRACT: A commercial TCAD tool (Silvaco-Atlas) is used for the simulation of Organic Field-Effect Transistor (OFET) devices based on sprayed 6,13-bis(triisopropylsilylethynyl)-pentacene (TIPS-Pentacene) organic semiconductor and Polystyrene (PS) insulating polymer blends (0.8:0.2w/w). The simulation results are validated and improved after systematic comparison with experimental data. Shallow donor-like bulk and interface traps density of states (DOS) are taken into account for better convergence with the experimental data. Also, the necessity to include negative interface charge density was revealed. Furthermore, the constant low-field mobility model as well as the band-to-band tunneling model were selected, while their parameters were properly adjusted. Simulated electrical characteristics and experimental data demonstrate a very good agreement but necessitate further improvement. The important physical quantity of root-mean-square (RMS) roughness at the TIPS-Pentacene/PS interface is also included in the simulation considering various patterns. Different levels of RMS roughness at the active interface and different patterns are considered. Also, the TIPS-Pentacene thickness non-uniformity was examined, and the simulation results suggest that it is more significant when the TIPS-Pentacene thickness is thinner near the drain electrode side. Finally, the effects of non-uniformity on the device's overall electrical behavior are systematically investigated.

KEYWORDS: OFET; TCAD simulation; shallow traps DOS; interface charges; interface roughness; thickness non-uniformity

1. INTRODUCTION

Over the last decades, Organic Thin-Film Transistors (OTFTs) have attracted a particular scientific interest because they present a series of advantages over the traditional a-Si TFTs, which include the mechanical flexibility of the plastic substrates, the relatively low-temperature processing and the simple manufacturing methodologies. Based on these OTFTs' advantages, several studies demonstrated a successful integration of OTFTs into simple[1,2] and complicated integrated circuits (ICs)[2,3], RFID tags[4], AMOLEDs[5,6] as well as into sensors[7,8] and biosensors[9,10]. Significant progress in the field of OTFTs has been noticed in the last two decades by the chemical synthesis of new organic semiconductor materials with mobility values which can clearly exceed those of a-Si (μ_{FE}>1cm^2/Vs)[11,12]. Furthermore, the easy solution processability of these organic semiconductors with a variety of Roll-to-Roll (R2R) compatible methods, makes them ideal candidates for the large-area and low-cost manufacturing of OTFTs and their applications.

So far, several scientific groups have successfully incorporated into their studies the 2D physics-based simulation tool to investigate physical quantities including the field-dependent mobility, the contact barriers, the interface charges as well as the bulk traps of the organic semiconductor and the traps at the active interface of the organic semiconductor and the insulator, which are correlated to the electrical behavior of the OTFT device. To achieve that investigation, they compared the current-voltage electrical characteristics of the simulated OTFT devices with those of the OTFTs fabricated into the laboratory environment. Specifically, Dwivedi et al. recently combined the simulation results of OTFTs that were based on pentacene organic

semiconductor with the experimental results, by taking into account the field-dependent mobility and the bulk trap density of states[13]. More analytical studies conducted an investigation of the effect of the above mentioned physical quantities in combination to the interface charges and contact barriers quantities on the experimentally measured input and output electrical characteristics of the OTFT devices that were based on p-type organic semiconductors, such as pentacene[14] and TIPS-Pentacene[15], as well as on n-type organic semiconductor, such as Polyera^{TM} N2200[14]. Another study by Mahato et al. was focused on the simulation of TIPS-Pentacene:polystyreneblend OTFTs and the comparison of the simulation results with those of the experiment, by taking into account all the aforementioned physical quantities. In the same study, simulation results were also taken under different operating temperatures and electrical bias-stress for 2 hours of TIPS-Pentacene:polystyreneblend OTFTs and were compared to the experimental ones. Finally, simulations at different operating temperatures of simple inverter circuits that were based on TIPS-Pentacene:polystyrene blend OTFTs, were realized by the same group who further compared the simulated inverters with those of the experiment and estimated the performance of the inverters at different operating temperatures[16].

According to the previously reported studies, the organic semiconductor material of the OTFT's experimental structure was deposited by a vacuum process[13,14] or a lab-scale solution-processing method, such as drop-casting[15,16] or spin-coating[14]. As the tendency towards the commercial exploitation of OTFTs and their applications is continuously increasing, due to a series of advantageous features they have demonstrated so far, it would be a challenge to simulate the OTFT devices with the organic semiconductor layer processed by a scalable method.

To the best of our knowledge, there have been noreports so far in the literature on the OTFT devices simulation that have taken into account another important physical quantity, such as the root-mean-square (RMS) roughness at the active interface of the organic semiconductor and the gate dielectric layer. As it has already been mentioned elsewhere[17], the RMS roughness at the active interface has an important effect on the OTFT's electrical performance. In particular, Feng et al., in an attempt to fabricate all Ink-Jetprinted low-voltage OTFTs on flexible substrates, ensured a smooth surface of the cPVP dielectric layer with a low RMS roughness value of about 0.3nm by optimizing their Ink-Jet printing process, thus reducing the interface traps density of states and therefore decreasing the subthreshold slope (SS) value and finally obtaining low operating voltage OTFTs.

The high RMS roughness value at the active interface hinders the charge carrier transport by introducing additional charge scattering sites and by increasing the interface traps density of states[17]. Furthermore, as indicated by several studies in review papers[18,19], the rough surface of the dielectric film has a great impact on the film morphology of the organic semiconductor grown onto the dielectric film, resulting in a severe degradation of the OTFT's charge carrier mobility. Additionally, large leakage currents through the gate electrode have also been mentioned in these reviews as a consequence of the rough interface between the organic semiconductor and the gate dielectric layer, resulting in reduced field-effect mobility values as well as in low on/off current ratios. These findings clearly indicate the effect of the RMS roughness at the active interface of the organic semiconductor and the gate dielectric layer, on the electrical parameters of the field-effect mobility (μ_{FE}), the on/off current ratio (I_{on}/I_{off}) and the subthreshold slope (SS) that characterize the OTFT's electrical performance. Therefore, it would be a challenge to simulate the OTFT devices with the additional physical quantity of the RMS roughness at the organic semiconductor/dielectric interface. This would ensure a more accurate, complete and realistic approach to the experimental data.

In the present study, we used a commercial TCAD tool (Silvaco-Atlas) to simulate the OFET devices based on the deposited TIPS-Pentacene:PS blends with the scalable spraying

method and compared TIPS-Pentacene:PS blend OFETs with the experimentally fabricated ones. To realize that simulation study, we initially considered physical quantities concerning theshallow donor-type bulk and interface traps DOS and the interface charges. The physical models we selected to simulate TIPS-Pentacene:PS blend OFETs included the constant low-field mobility model and the band-to-band tunneling model. An investigation study of the effect of the bulk and interface traps DOSas well as of the interface charges on the experimental input electrical characteristics was carried out. The comparison ofthe simulated input electrical characteristics with the experimental ones revealed a sufficiently good agreement between them, while the simulated output electrical characteristics fitted satisfactorily with those of the experiment. Further, to improve our simulation results, we included roughness at the TIPS-Pentacene/PS active interface, quantified by the root-mean-square (RMS) of the interface roughness.

2. EXPERIMENTAL SECTION

Fig. 1 depicts the 3D representation of the experimentally fabricated OFET device. A bottom-gate top-contact (BG-TC) device configuration was adopted. The devices were fabricated onto a heavily doped p-type silicon substrate which served as the common gate electrode with a 300nm thermally grown silicon dioxide (SiO_2) which served as the common gate dielectric layer. The substrates were thoroughly cleaned by a procedure reported elsewhere[20]. After the preparation of the TIPS-Pentacene organic semiconductor and PS insulating polymer solutions in anisole at a concentration of 0.5%wt and 3%wt, respectively, were blended at the 0.8:0.2 w/w composition ratio. By using a commercially available Iwata airbrush sprayer (HP-CR model) with a 0.5mm nozzle diameter and optimizing the critical spraying parameters including the substrate temperature, the nozzle to substrate distance and the nitrogen (N_2) pressure[20], the TIPS-Pentacene:PS (0.8:0.2 w/w) blends were sprayed directly onto the SiO_2(300nm)/Si substrate under ambient conditions. The sprayed TIPS-Pentacene:PS blend films were left to evaporate freely in air without further to be subjected to thermal annealing. After the solvent evaporation from the sprayed blends, the samples were transferred to a low vacuum chamber (0.1 mbar, 60min) in order to remove the remaining solvent from the blend films. According to our previously reported study[20], the sprayed TIPS-Pentacene:PS blends at the composition ratio of 0.8:0.2 w/w resulted in phase-separated TIPS-Pentacene crystals at the top interface of the TIPS-Pentacene:PS blend film with the air and a phase-separated PSlayerat the bottom interface of the TIPS-pentacene:PS blend film with the substrate, as a consequence of the efficient phase separation phenomena between the two materials within the TIPS-Pentacene:PS blend film.

As estimated by Atomic Force Microscopy (AFM) measurements, the thickness of the phase-separated PS film was found to be around 63nm[20], while the thickness of the phase-separated TIPS-Pentacene crystals was ranging from 70 to 90nm. The above mentioned range of the TIPS-Pentacene thicknessvalueswas specified by comparing adjacent regions of the sample with and without the TIPS-Pentacene film (peak-to-valley values). After the deposition of the TIPS-Pentacene:PS blend films by the spraying method, gold source drain electrodes (60 nm) were thermally evaporated (1 Å/sec) in a high vacuum chamber (1×10^{-6} mbar) through a shadow mask with channel lengths and widths varying from 30 to 80 μm and 1000μm, respectively. Finally, the OFET's current-voltage electrical characteristics were recorded by a Keithley 4200SCS semiconductor parameter analyzer under ambient conditions and dark, at room temperature.

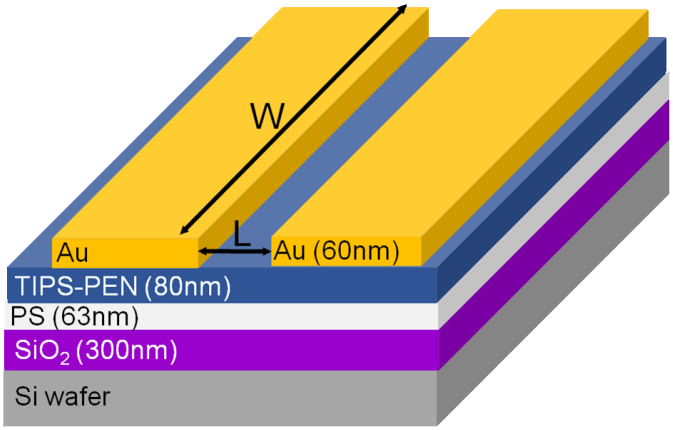

Fig.1.3 D representation of a typical (dimensions can have a small variation) bottom-gate, top-contact OFET device fabricated by spray-coating the TIPS-Pentacene:PS blends at the 0.8:0.2 w/w composition ratio. The p+ Si wafer served as the gate contact, while the SiO_2 (300nm) served as the gate dielectric.

3. RESULTS AND DISCUSSION

In DevEdit tool we simulated the two dimensional (2D) BG-TC TIPS-Pentacene:PS blend OFET device structure, as shown in Fig.2.In particular, to define the regions of the simulated TIPS-Pentacene:PS blend OFET device structure, we took into account the geometrical factors of the experimental device (Fig. 1) concerning the channel's length (L=80μm) and depth (W=1000μm) as well as the thickness of each individual layer. The thicknesses we used to simulate the device structure in DevEdit tool were 300nm, 63nm, 80nm and 60nm for SiO_2, PS, TIPS-Pentacene and Au source and drain electrodes, respectively. To fully define the regions of the simulated device, we also took into account the materials we selected to fabricate the experimental device structure (Fig.1). As far as the gate is concerned, we used a layer of copper (Cu) underneath the structure. It is important to note here that, we used default materials to simulate the TIPS-Pentacene:PSblend OFET device structure, however, it was necessary to specifically define the energy band gap of the TIPS-Pentacene organic semiconductor using the MATERIAL statement in Atlas tool since it is not included in the material library of the Silvaco software. Likewise, the permittivity of the PS insulating polymer was also specified in a MATERIAL statement.

In Table 1, the material simulation parameters including the energy band gap, the electron affinity and the dielectric constant of TIPS-Pentacene, the effective density of states in HOMO and LUMO, the permittivity of PS and SiO_2 as well as the work function of Au contacts, are summarized. We introduced the energy band gap value of TIPS-Pentacene[15], the permittivity value of PS[20] as well as the gold work function[21] according to the literature, while we used the default values for all the other material parameters. The gold work function value reported in the literature is 5.10 eV[21]while in our simulation study we adjusted the gold source and drain contacts work function in the WORKFUN statement[22] in order to add a barrier height equal to 0.15 eV (Table 1). Thus, we increased the barrier height (difference between the gold work function and the TIPS-PEN organic semiconductor HOMO level) from 0.50 eV (value reported in the literature) to 0.65 eV in our simulation study in order to achieve a better convergence between the simulated input and output electrical characteristics with those obtained from the experiment and also reproduce the non-ohmic behavior indicated in the experimental data.

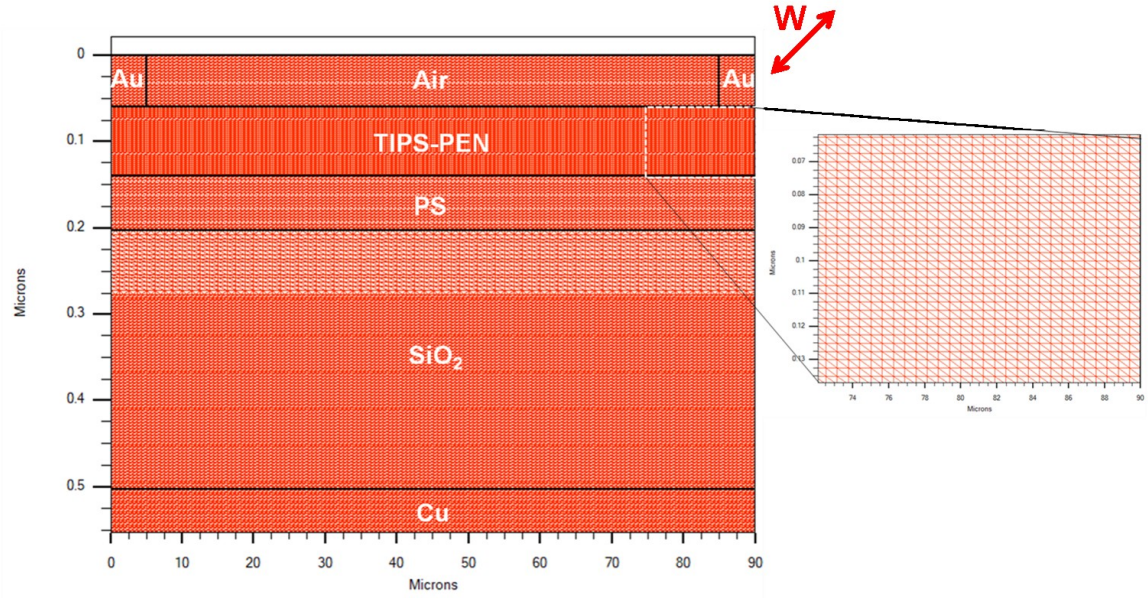

Fig. 2. The 2D-simulated device indicating the geometry of the device as well as the regions created (different materials) and the mesh used in the simulations. The depth W (1000μm) correspondsto the 3rd dimension. The inset image showing the 2D mesh within the channel (TIPS-Pentacene) region is 5 times (x5) magnified.

The 2D mesh was also specified in DevEdit tool and can be observed in Fig. 2. By tuning the meshing parameters[23] we obtained a fine 2D mesh, which is denser in the TIPS-Pentacene organic semiconductor region (Fig. 2) without affecting the simulation run, as more accuracy is required in the calculations within this region. It was also necessary to increase the accuracy of the calculations (simulation) to 160bit in order to have more reliable results. A magnified image (inset image) of the 2D mesh within the TIPS-Pentacene organic semiconductor region is also depicted in Fig. 2.

Material Simulation Parameters	Value
Energy band gap of TIPS-PEN (eV)	1.80
Electron affinity of TIPS-PEN (eV)	2.80
Dielectric constant of TIPS-PEN	4.0
Effective density of states (HOMO) (cm^{-3})	2.0×10^{21}
Effective density of states (LUMO) (cm^{-3})	2.0×10^{21}
Permittivity of Polystyrene (PS)	2.40
Permittivity of Silicon dioxide (SiO_2)	3.90
Work function of Au contacts (eV)	5.25

Table 1. Summary of the material simulation parameters which were necessary to modify or define the simulated materials.

In our simulation study, we selected a p-type TIPS-Pentacene organic semiconductor, introducing also shallow donor-type traps density of states within the bulk of the TIPS-Pentacene organic semiconductor as well as at the active interface between the TIPS-Pentacene organic semiconductor and the PS insulating polymer. Such traps could be attributed to the oxygen molecules (O_2)[24], introduced during the spray-coating process of the TIPS-Pentacene:PS blends in ambient conditions. The migration of the oxygen molecules (O_2) from the atmosphere within the TIPS-Pentacene organic semiconductor is inevitable. The exponential density of states of the shallow donor-type traps is given by the following equation 1[22]:

$$g_D(E) = \frac{HD}{kTCD} \exp\left(\frac{E_{HOMO} - E}{kTCD}\right) \quad (1)$$

where HD is the donor-type traps density of states in cm^{-3}, TCD is the donor-type traps characteristic temperature in K, k is the Boltzmann constant, and E is the energy within the forbidden energy band gap, expressed in eV.

To simulate the TIPS-Pentacene:PS blend OFET device by taking into account the shallow donor-type traps density of states within the bulk of TIPS-Pentacene and at the TIPS-Pentacene/PS active interface and then investigate their effect on the current-voltage input electrical characteristic, we properly adjusted the parameters of HD and TCD according to the Table 2.

Bulk		Interface	
Parameter	Value	Parameter	Value
HD1	9.25×10^{17} cm^{-3}	HD1	2.80×10^{13} cm^{-2}
TCD1	4.29×10^{3} K	TCD1	4.41×10^{2} K
HD2	4.75×10^{17} cm^{-3}	HD2	3.70×10^{9} cm^{-2}
TCD2	4.41×10^{2} K	TCD2	4.29×10^{2} K

Table 2. Simulation Parameter values of the exponential density of states of the shallow donor-like traps within the bulk of TIPS-Pentacene and at the TIPS-Pentacene/PS interface.

As can be seen in Fig. S1a, in the simulation which does not consider any traps, the I_{DS}-V_{GS} electrical characteristic (continuous curve) at V_{DS}=-5Vcorresponds toasubthreshold slope(SS) equal to 0.14 V/dec. It is also evident in Fig. S1a that neglecting any traps, there is significant divergence of the simulated I_{DS}-V_{GS} electrical characteristic with the experimentally measured one (dotted curve). The simulation with donor-type traps density of states within the bulk of the TIPS-Pentacene organic semiconductor (green curve) resulted in a value of the subthreshold voltage (SS=1.16 V/dec) which was found to be about 8 times larger than that arising from the simulation without any traps. The addition of the donor-type traps density of states at the TIPS-Pentacene/PS active interface in combination to the bulk traps (red curve) did not increase further the subthreshold voltage value, as shown in Fig. S1a. However, the combination of bulk and interface traps resulted in an ON current (I_{ON}) reduction from 8×10^{-6} A (in the case we consider only bulk traps) to 3.1×10^{-6} A which is closer to the experimental ON current, therefore, better convergence to the experimental characteristic (Fig. S1a). Finally, it is worth noting that the addition of the interface traps in combination with the bulk traps reduced further (by one order of magnitude) the ON current – as opposed to the case without any traps (Fig. S1a).

Further, we investigated the effect of the positive and negative fixed charges (Q_f) at the active interface of the TIPS-Pentacene organic semiconductor and the PS insulating polymer on the experimental I_{DS}-V_{GS}input electrical characteristic at V_{DS}=-5V. Introducing a negative interface charge density value of Q_f= -2.42×10^{11} cm^{-2}, results in a shift towards the positive gate voltages of the corresponding simulated I_{DS}-V_{GS} input electrical characteristic (shown for V_{DS}=-5V), while a positive one causes shift towards more negative voltage. The variation of the interface charge density value from -2.42×10^{11} to +2.42×10^{11} cm^{-2}significantly affected the threshold voltage (V_T) value which changed from -8.90 to -17.33 V, respectively (Fig. S1b). Correspondingly, the onset voltage (V_{ON}) value varied from-2.97 to -12.0 V. It is important to note here that, the values of the electrical parametersof the threshold voltage and the onset voltage exhibited a better convergence with the experimental ones (V_T = -7.36V, V_{ON} = - 4.66 V) when a negative charge density value (-2.42×10^{11} cm^{-2}) is introduced, correspondingin better I_{DS}-V_{GS}fitting (Fig.S1b). At the same time, the variation of the ON current (I_{ON}) was in the range of 2.18×$10^{-6}$to 3.64×10^{-6} A (Fig. S1b).

In the TCAD simulation we introduced physical models which comprise the constant low-field mobility[22] and the band-to-band tunnelling[22]. In the constant low-field mobility model, the carrier scattering with the lattice at room temperature (T=300K) is also taken into account.

Parameter	Value
MUP	2.50 cm^2/Vs
TMUP	1.50
MUN	2.50 cm^2/Vs
TMUN	1.50
BB.A	9.66 × 10^{12} cm^{-1} V^{-2} s^{-1}
BB.B	3.0 × 10^7 V/cm
BB.GAMMA	2.0

Table 3. Simulation parameter values of the constant low-field mobility model as well as of the band-to-band tunneling model.

Fig. 5 illustrates the overall device electricfield distribution. By considering a more detailed mesh (of higher density) inside the TIPS-PEN organic semiconductor region (Fig. 2) and properly adjusting the meshing parameters, the calculated in Atlas tool (Silvaco) electrical fields localized under the source and drain contacts are found to be lower than 9.0 × 10^5 V/cm. The electrical fields of this order of magnitude could be attributed to the Schottky contacts consideration included inthe simulations. An investigation study of the effect of the gold work function on the electrical field underneath the source and drain contacts was realized. We initially specified in the WORKFUN statement[22] the gold work function of the source and drain contacts to be equal to 5.10 eV in addition to the barrier heights of 0 eV, 0.15 eV and 0.40 eV. Therefore, the energy barrier in respect to the TIPS-PEN organic semiconductor HOMO level (4.60 eV) is increased from 0.50 to 0.90 eV. Such energy barriers are attributed to the presence of interface dipoles between the gold source and drain contacts and the TIPS-PEN organic semiconductor[15]. These interface dipoles modify the energy diagrams resulting from a metal when brought to contact with an organic semiconductor according to recently published review studies[25,26]. As can

be clearly seen in Fig. S2, by comparing the different gold work function values of the source and drain contacts in the range from 5.10 to 5.50 eV (also with the default one), an important increase of the electrical field of about one order of magnitude is observed when the source and drain contacts are considered to be Schottky contacts[22] (gold work function in the range from 5.10 to 5.50 eV). In the default work function case, the Silvaco software is considering ohmic source and drain contacts[22]. Moreover, an electrical field variation from 8.5×10^5 to 9.5×10^5 V/cm is observed when the gold work function value is changing (from 5.10 to 5.50 eV) in Fig. S2.

Similar electrical field strengths (7×10^5 V/cm) have been calculated by Hurkx et al. using the band-to-band tunneling model in their study at room temperature[27], considering also Schottky contacts. So far, two mechanisms have been reported by Liu et al. in order to describe the charge injection from metal/organic semiconductor (OSC) junction[26]. The first of them concerns the thermionic emission through an energy barrier while the second one the tunneling mechanism. The authors reported that the tunneling mechanism (inset image in Fig.S2) becomes predominant when the thickness of the space charge region (depletion layer) within an organic semiconductor is as thin as a few nanometers (< 10 nm) and therefore the charges can directly tunnel from metal to an organic semiconductor[26]. In our study we estimated the width of the zone with higher electric fields (8.5×10^5-9.5×10^5 V/cm) which is distributed underneath the source and drain electrodes to be less than 2 nm (Fig. S2). Thus, this high electric field distribution is able to activate the band-to-band tunneling mechanism and therefore permit the charges to tunnel directly from the gold metal to the TIPS-PEN organic semiconductor.

Furthermore, as the TIPS-Pentacene material is a direct energy gap organic semiconductor[28], we selected to use the standard band-to-band tunneling model with a tunneling generation rate which is given in the following equation 2[22]:

$$G_{BBT} = D\, BB.A\, E^{BB.GAMMA} \exp\left(-\frac{BB.B}{E}\right) \qquad (2)$$

where $E$is the magnitude of the electric field (in V/cm), D is a statistical factor, BB.A and BB.B are the model's parameters in $cm^{-1}V^{-2}s^{-1}$ and V/cm, respectively, and the BB.GAMMA is the dimensionless parameter of the model which is taking the value of 2.0 for direct transitions[27].
In our simulation study, for the BB.Bparameter (of the standard band-to-band tunneling model) we preserved the default value (Table 3), while we properly adjusted the BB.A parameter of this model in order to obtain the best fit of the simulated results in respect to the experimental data.

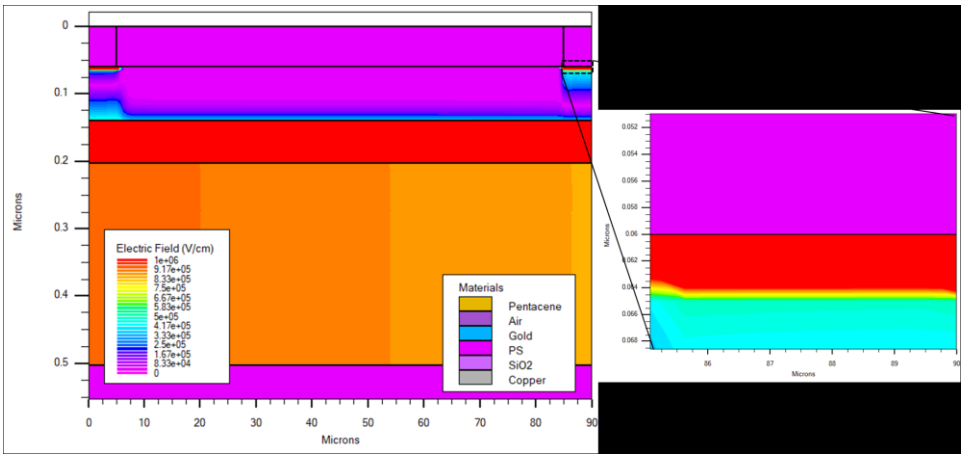

Fig. 5. The 2D simulated device illustrating the electric field variation, at V_{DS}=-5V and V_{GS}=-40V. The inset image depicting the high electric field under the drain electrode is 18 times (x18) magnified.

The effect of the standard band-to-band tunneling model on the experimental I_{DS}-V_{GS} electrical characteristics measured at V_{DS}=-5V (linear region) and V_{DS}=-50V (saturation region) is shown in Fig. 6. It is evident in the same figure that the introduction of the standard band-to-band tunneling model in our simulation strongly influences the OFF current of the simulated I_{DS}-V_{GS} electrical characteristics at V_{DS}=-5Vand V_{DS}=-50V.Specifically, the OFF current of the simulated input characteristics varied from $2.62\times10^{-13}$to 1.0×10^{-9} A and from 2.0×10^{-13} to 6.76×10^{-12} A for the saturation and linear regions, respectively, when the standard band-to-band tunneling model is included. The best fit of the simulated I_{DS}-V_{GS} electrical characteristics with the experimental data was obtained when the BB.A= 9.66×10^{12} cm^{-1} V^{-2} s^{-1}(also registeredin Table 3). As indicated in Fig. 6, the simulation with the standard band-to-band tunneling model results in a slight increase of the ON current while the subthreshold voltage (SS) has also been slightly affected. The extracted SS values from the simulated I_{DS}-V_{GS} electrical characteristics at V_{DS}=-50V and V_{DS}=-5V with the standard band-to-band tunneling model were found to be 1.96 V/dec and 2.04 V/dec, respectively.

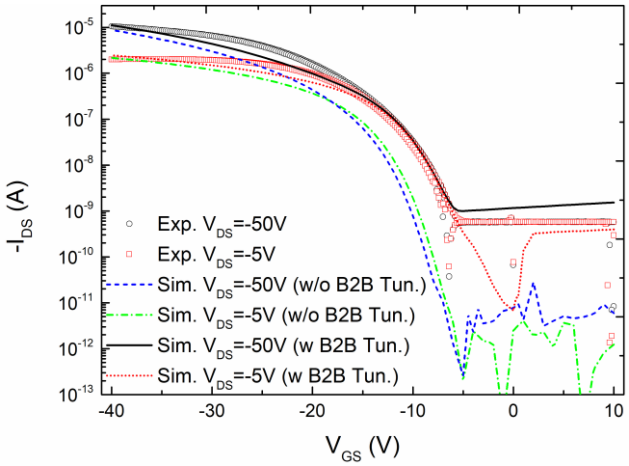

Fig.6. Effect of thestandard Band-to-Band (B2B) tunneling model on the simulated I_{DS}-V_{GS} electrical characteristics at V_{DS}=-50V and V_{DS}=-5 V (with: w and without: w/o B2B). The best fit is achieved by adjusting the simulation parameters of the standard B2B tunneling model.

Fig. 7a and Fig. 7b exhibit the simulation results from the simulation of the input (I_{DS}-V_{GS}) and output (I_{DS}-V_{DS}) electrical characteristics at V_{DS}=-50V and V_{DS}=-5V and at V_{GS}=-10V, V_{GS}=-20V, V_{GS}=-30V and V_{GS}=-40V, respectively. Experimental data of one of the best-performing TIPS-Pentacene:PS blend OFET devices are also included for comparison. In Fig. 7a, the experimental input (I_{DS}-V_{GS}) electrical characteristics are in good agreement with the simulated ones. A qualitative observation showed an excellent convergence of the simulated I_{DS}-V_{GS} electrical characteristics with the experimental ones in the subthreshold region, which was verified by the extracted subthreshold voltage (SS) values. These values were found to be 2.47V/dec and 2.22 V/dec in the saturation and linear regions, respectively, and were also sufficiently close to the experimentally measured ones (2.25 V/dec at V_{DS}=-50V, 2.30 V/dec at V_{DS}=-5V). Moreover, as can be observed in Fig. 7a, the ON current (I_{ON}) at V_{GS}=-40V in the saturation region fitted very well with the experimental one, and this also can be seen from their values which are equal to 2.84×10^{-5} A and 2.77×10^{-5} A for the experiment and the simulation, respectively. A slight deviation between the ON current at V_{GS}=-40V in the linear region with that from the experiment was also observed in the same figure. This is also confirmed by comparing the simulated ON current's value which was found to be 7.02×10^{-6} A with the experimental one which is equal to 5.46×10^{-6} A. Further improvement of the simulated I_{DS}-V_{GS} electrical characteristic at V_{DS}=-5V is

needed in order to converge better with the experimental one at the high gate voltage value of -40V.

In Fig. 7b, it is evident that the simulated output electrical characteristics at the gate voltages of -10V, -20V and -30V exhibited excellent fit with the corresponding output electrical characteristics from the experiment both in the linear (V_{DS}=-5V) as well as in the saturation (V_{DS}=-40V) regions. However, there was a noticeable discrepancy at V_{GS}=-40V. Therefore, a further improvement of the simulated output electrical characteristic at V_{GS}=-40V is mandatory to obtain an overall good consistency with the experimentally measured ones.

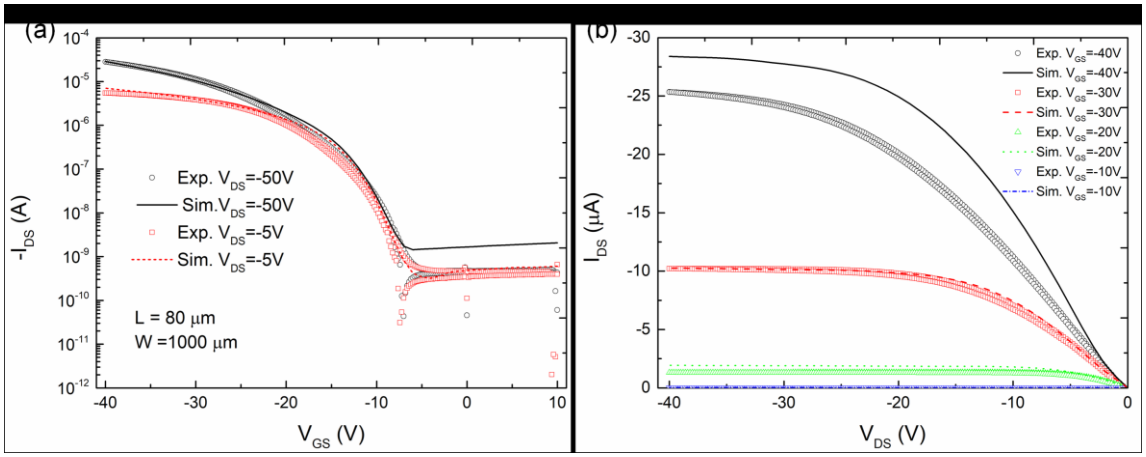

Fig. 7. Comparison of the (a):input (I_{DS}-V_{GS}) electrical characteristics (at V_{DS}=-50V and V_{DS}=-5V)and (b): output (I_{DS}-V_{DS}) electrical characteristics (at V_{DS}=-10V, V_{DS}=-20V, V_{DS}=-30V and V_{DS}=-40V) with the experimental ones.

Fig. 8 represents the simulation results from the Atlas tool in comparison to the experimental data of two similar TIPS-Pentacene:PS blend OFET devices with the same channel length (L=80μm). It is evident that though these samples have the same channel length and construction characteristics, the ON currents (I_{ON}) at V_{GS}=-40V of the two experimentally measured TIPS-Pentacene:PS blend OFET devices aresignificantly different. Therefore,we needed to simulate the TIPS-Pentacene:PS blend OFET devices with a different set of the MUP and MUN parameters of the constant low-field mobility model. The discrepancy between the two experimental ON currents is therefore attributed to the low field mobility variation, already discussed in previously reported study[20]. The effective low field mobility values were found to be 0.89 cm^2/Vs and 0.44 cm^2/Vs for these two input characteristics (of Fig.8). The best fit between the simulated I_{DS}-V_{GS} electrical characteristic and the "upper" experimental one was obtained by setting both theMUP and MUN parametersequal to 2.50 cm^2/Vs,while for the "lower" experimental one by specifying these values to be 0.80 cm^2/Vs. Furthermore, the upper experimental I_{DS}-V_{GS}electrical characteristic is slightly shifted in respect to the bottom experimental one, and therefore we utilized different interface charge density (Q_f) values of the corresponding simulated I_{DS}-V_{GS} electrical characteristics. Particularly, the best fit with the upper experimental input electrical characteristic was achieved by using an interface charge density value equal to -1.15×10^{11} cm^{-2}, while a slightly larger value of the interface charge density of -2.42×10^{11} $cm^{-2}$was found to fit well with the bottom experimental input electrical characteristic. Therefore, we conclude that there is not a simulated input electrical characteristicthat could represent all the experimentally measured TIPS-Pentacene:PS blend OFET devices, because of the inherent variability. Thus, a new set of certain simulation parameters is needed to be determined for each experimental device, or even a set of mean fitting values is needed in order to describe an average electrical behavior of the samples.

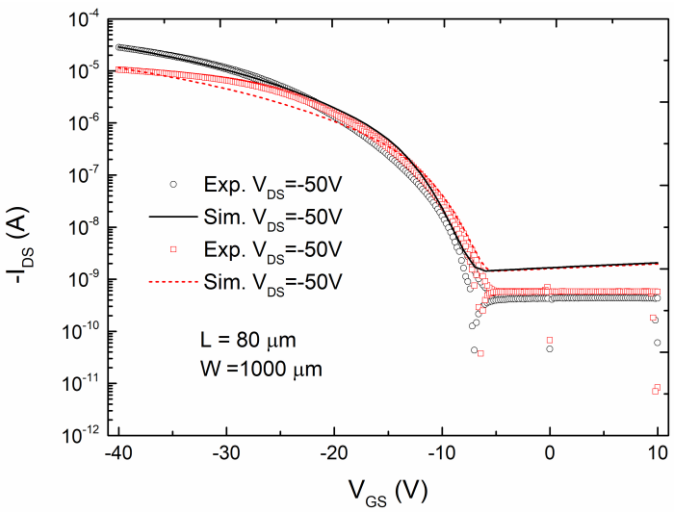

Fig. 8. Experimental I_{DS}-V_{GS} electrical characteristics at V_{DS}=-50V taken from two different TIPS-Pentacene:PS blend OFET devices with the same channel length (L=80μm, W=1000μm) and from the same sample, and their corresponding simulation curves.

Among other physical quantities which can vary from sample to sample, the roughness at the active interface of the TIPS-Pentacene organic semiconductor and the PS insulating polymer, is also very important and should be considered in the simulations in order to improve further the simulation results and can also insert the variation which is observed. To achieve that we can consider the root-mean-square (RMS) ofthe interface roughness. This implies the necessity to also consider a specific pattern in the interface morphology for the calculations of the RMS.Initially we introduced a “square wave pattern” at the TIPS-Pentacene/PS interface with specific characteristics including the RMSparameter and the number of periods with values of 1.25 nm and 9, respectively. Fig. 9illustrates thetwo dimensional (2D) simulated BG-TC TIPS-Pentacene:PS blend OFET device structure which includes as quare wave interface pattern with the abovementioned characteristics, as it is implemented in DevEdit tool. A magnified area of the image depicting the square wave pattern at the active interface is also shown (Fig. 9 inset). The new interface was achieved by modifying the region of the TIPS-Pentacene organic semiconductor (upper-yellow region) as well as the region of the PS insulating polymer (lower-purple region). The extra degrees of freedom added through this pattern can lead to more realistic simulation results. Different patterns can be used, but very complex ones can make the simulation effort very laborious. The first attempt was to compare the ideal-flat interface with a square wave pattern at the active interface with an RMS parameter value of 1.25 nm and number of periods equal to 9. These parameters can change by adjusting the amplitude and the length of the square pattern accordingly. Also, in the new meshes created, we tried not to change the mesh details of the rest regions significantly (a different “neighbor” approach is usually necessary), in order to maintain the same accuracy in the results. Thus, most of the regions maintained the same mesh details as previously (device without interface roughness).

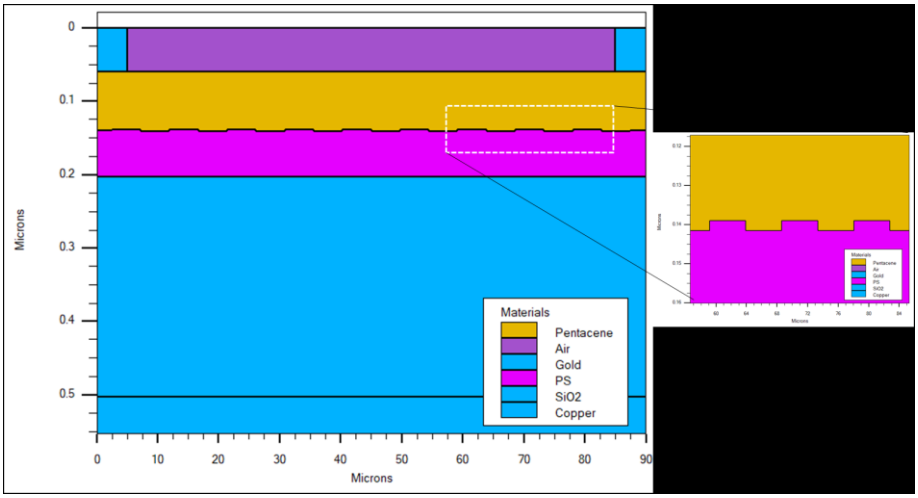

Fig. 9. The 2D-simulated device including roughness at the TIPS-Pentacene/PS interface, by adding 9 periods of a square wave pattern at the active interface with an RMS parameter value equal to 1.25 nm. The inset image depicts a part of the square wave pattern at the TIPS-Pentacene/PS interface is 3 times (x3) magnified.

The simulation results from the Atlas tool concerning the input (I_{DS}-V_{GS}) electrical characteristics at V_{DS}=-5V and V_{DS}=-50Vas well as the output (I_{DS}-V_{DS}) electrical characteristics at V_{GS}=-10V, V_{GS}=-20V, V_{GS}=-30V and V_{GS}=-40V when a square wave pattern with an RMS parameter value of 1.25nm and a number of periods of 9 is introduced at the active interface, are shown in Fig. 10a and Fig. 10b, respectively. In Fig. 1a the experimental measurements of the best-performing sample are also included. A better convergence of the ON current (I_{ON}) at V_{DS}=-40V with the experimental one, is achieved, as a consequence of a decrease of the ON currentdue to the interface roughness at the active interface, and the results are tabulated inTable 4. Moreover, a slight decrease of the subthreshold slope (SS)is observed – as compared to the ideal case (RMS=0nm). Finally, the simulated I_{DS}-V_{GS} electrical characteristic at V_{DS}=-50V depicted in Fig. 10a, exhibited a slight decrease of the subthreshold slope(SS) as well as of the ON current compared to those obtained by neglecting the interface roughness. As a result, the overallgood fitting in Fig. 10a between the simulated I_{DS}-V_{GS} electrical characteristic at V_{DS}=-50V and the experimental one is maintained sufficiently well.

In Fig. 10b, it is evident that there is a clear effect of the introduction of the RMS roughness at the TIPS-Pentacene/PS interface on the simulated I_{DS}-V_{DS}electrical characteristic. The reduction of the drain current (I_{DS}) -after introducing roughness at the active interface - results in a better converge of the experimental I_{DS}-V_{DS} electrical characteristic. This is more noticeable at V_{GS}=-40V (within the experimental range of V_{DS}), after comparison with corresponding characteristic without interface roughness (Fig. 7b). It is worth noting that the simulated I_{DS}-V_{DS} electrical characteristics at V_{GS}=-10V, V_{GS}=-20V and V_{GS}=-30V illustrated in Fig. 10b, did not show any substantial difference with those obtained by neglecting the roughness(zero RMS value) at the active interface, thus maintaining sufficiently well fit with the corresponding experimental I_{DS}-V_{DS} electrical characteristics.

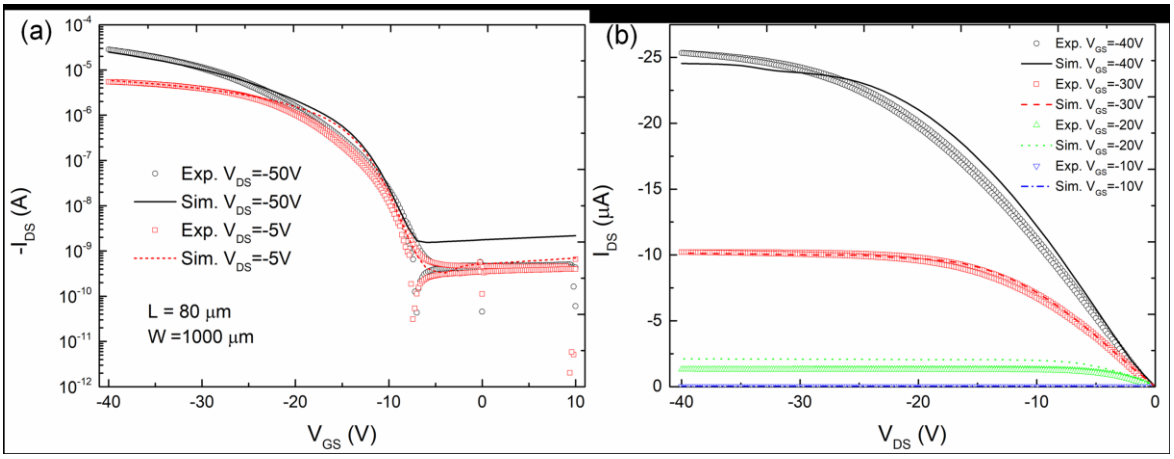

Fig. 10. Diagrams showing the simulation results with roughness (RMS=1.25nm) at the active interface and the comparison between thesimulated input (I_{DS}-V_{GS}) electrical characteristics at V_{DS}=-50V and V_{DS}=-5V and the experimental ones (a), as well as between the simulatedoutput (I_{DS}-V_{DS}) electrical characteristics at V_{DS}=-10V, V_{DS}=-20V, V_{DS}=-30V and V_{DS}=-40V with those obtained from the experiment (b).

Electrical Parameter	Experiment	Simulation with RMS=0nm	Simulation with RMS=1.25nm
Linear region (V_{DS}= -5V)			
SS (V/dec)	2.30	2.22	2.08
I_{ON} (A)	5.46×10^{-6}	7.02×10^{-6}	5.88×10^{-6}
Saturation (V_{DS}= -50V)			
SS (V/dec)	2.25	2.47	2.32
I_{ON} (A)	2.77×10^{-5}	2.84×10^{-5}	2.48×10^{-5}

Table 4. Comparison between the values of the I_{ON} and SS electrical parameters obtained by the simulation without (RMS=0 nm) and with (RMS=1.25 nm) roughness at the TIPS-Pentacene/PS interface and the ones extracted from experiment data.

The very good convergence which is achieved between the simulated output electrical characteristics and the experimental ones at the very low drain voltages (V_{DS}) in Fig. 7b and in Fig. 10b could be attributed to the Schottky contacts consideration in our simulation study with a barrier height of 0.65 eV[29]. In this region the "current crowding" effect is apparent in output electrical characteristics as a result of the non-ohmic (non-linear) behavior of the drain current (I_{DS}) at the very low drain voltages (V_{DS}). This phenomenon has also been observed in a previously reported work by Gupta et al., who performed an analytical study on the simulation of OFETs with a device configuration similar to that reported here. Specifically, the authors succeeded a very good agreement of their simulated output electrical characteristics and the experimental ones at the low drain voltages, V_{DS} (linear region) by considering the gold work function of 5.0 eV and increasing the barrier height from 0.30 to 0.38 eV in combination to the Pool-Frenkel (PF) model[15].

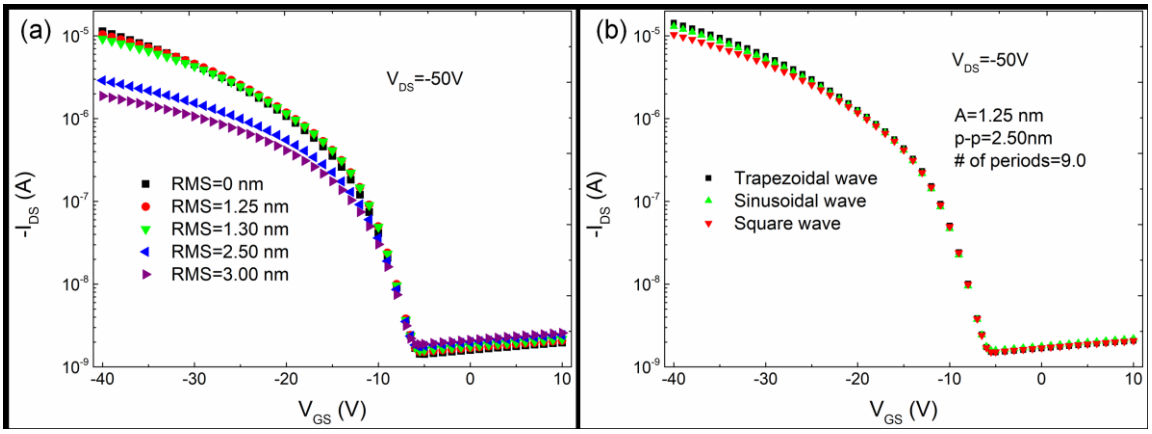

Fig. 11. Impact of the different RMS roughness values (a) as well as of the different patterns (b) at the TIPS-Pentacene/PS interface, on the simulated I_{DS}-V_{GS} electrical characteristics at V_{DS}=-50V.

Furthermore, in order to investigate the effect of the magnitude of the RMS value of the roughness - at the interface between the TIPS-Pentacene organic semiconductor and the PS insulating polymer on - the simulated I_{DS}-V_{GS} electrical characteristics at V_{DS}=-50Vwas estimated for devices with different RMS parameter values in the range from 1.25 to 3.00 nm. We examined typically expected values of the RMS parameter, after considering the thickness of the conducting channel (typically in the range from 5-10nm). The number of periods (equal to 9) is kept the same for all the devices. The simulation results from the Atlas tool are depicted in Fig. 11a, revealing a severe deterioration of the ON current (I_{ON}) value at V_{DS}=-40V from 1.12×10^{-5} A to 1.87×10^{-6} A with increasing the RMS roughness value from 0 to 3.00 nm. Also, higher values of RMS roughness induced a slight degradation of the SS(from 2.39 to 2.70 V/dec), while no significant change of the OFF current (from 1.53×10^{-9}A to1.87×10^{-9} A) was observed.

Also, by changing the number of periods from 4 to 19 -of the square wave pattern at the TIPS-Pentacene/PS interface - and by keeping constant the RMS parameter value to 1.25nm, we estimated a reduction of the ON current value at V_{GS}=-40V from 1.31×10^{-5}A (4 periods) to 7.58×10^{-6} A (19 periods). Thus, the change of the on-current is by a factor of less than 2, indicating that the number of periods in such a range is not as crucial as the RMS parameter.

Finally, we obtained data by simulating different patterns at the TIPS-Pentacene/PS interfaceby including trapezoidal and sinusoidal patterns in addition to the square one. The peak-to-peak amplitude of the pattern and the number of periods were fixed to 2.5 nm and 9, respectively, for the different patterns at the active interface. In Fig11b, we observe that there is a clear effect of the different patterns at the TIPS-Pentacene/PS interface on the ON current value of the simulated I_{DS}-V_{GS} electrical characteristics at V_{DS}=-50V. The greatest degradation in the on-current was in the case of the square form, while the least degradation was in the case of the trapezoidal one. More specifically by changing the pattern at the active interface from square to sinusoidal and trapezoidal, the ON current value increased from $1.02 \times 10^{-5}$to 1.33×10^{-5} and 1.44×10^{-5} A. Most probably the sinusoidal case could be the most representative to be used, but still the differences in the results are not important.

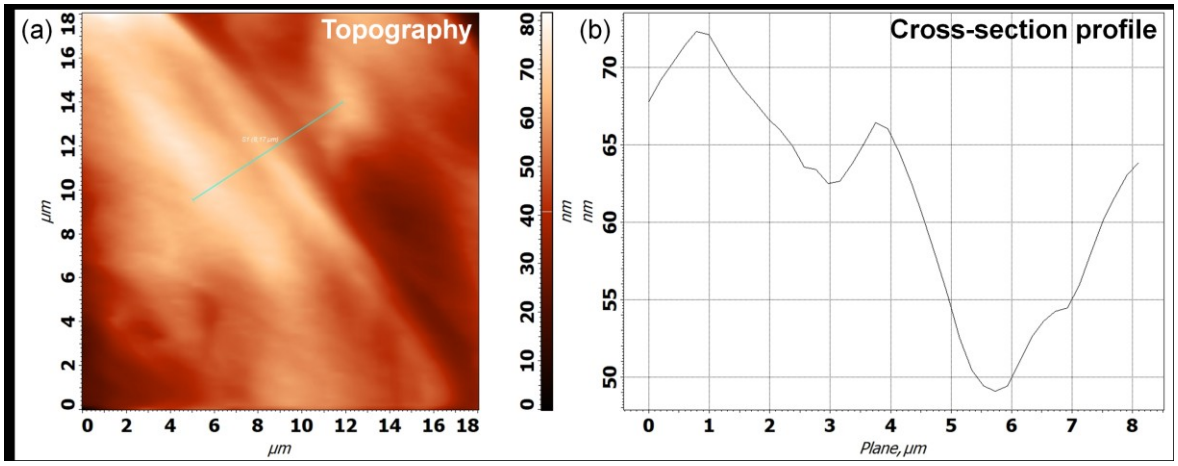

Fig.12. AFM topography image (a) and the corresponding cross-section profile image (b) of the sprayed TIPS-Pentacene:PS blend (0.8:0.2 w/w) film.

Another issue which can be investigated and improve the results (be more realistic) can be the homogeneity (in the thickness) of the channel - TIPS-Pentacene film. Consulting different AFM topography images of the TIPS-Pentacene organic semiconductor film surface, a relative thickness difference is indicated between the adjacent TIPS-Pentacene crystals and was found to be within the amplitude of up to ±20 nm (up to 40 nm peak-to-peak), proving the non-uniformity of the TIPS-Pentacene organic semiconductor film thickness. A representative AFM topography image with the corresponding cross-section profile image revealing an amplitude of ±10 nm (up to 20 nm peak-to-peak) of the relative thickness difference of the TIPS-Pentacene crystals, are depicted in Fig. 12a and Fig.12b, respectively. In our study, the non-uniformity of the TIPS-Pentacene organic semiconductor film identified by AFM topography images, could reasonably explain why the simulation results do not perfectly fit with the experimental data, as it has already been shown previously in this study.

So far in our simulation we assumed the ideal case of the uniform TIPS-Pentacene film thickness without considering any non-uniformity of it. To introduce the non-uniformity of the TIPS-Pentacene organic semiconductor film thickness we modified the regions of TIPS-Pentacene, the air dielectric and the source and drain electrodes (as described inFig.2) in DevEdit tool in order to define a TIPS-Pentacene of mean width of 80 nm with the one side to be thicker (+10nm in respect to the mean width) while the other one to be thinner (-10nm in respect to the mean width). Therefore, a step is observed in the middle of the channel length, keeping the average thickness of the channel same with the initial (ideal) consideration. The first number used in our notation of non-uniform devices (Fig.13) indicates the relative change of the thickness near the Source, while the second one near the Drain. Thus, the device marked as [-10, 10] means the thickness is 70 nm in the Source's side while it is 90 nm in the Drain's, as compared to the "untouched" having a constant thickness of 80 nm. The opposite holds for the [10, -10] device simulated.

As can be clearly seen in Fig. 13a and Fig. 13b, the comparison between the "untouched" (ideal) device and the devices with non-uniform channel thickness, revealed that the non-uniformity of the TIPS-Pentacene organic semiconductor film thicknesswhen the side near the drain electrode is thinner- sample [10, -10] - suffered the most dramatic impact on the input (Fig.13a) and output (Fig.13b) electrical characteristics, degrading theTIPS-Pentacene:PS blend OFET's drain current and electrical parameters. These electrical parameters include the threshold voltage (V_{Th}), the Subthreshold Slope (SS) as well as the on/off current ratio and the transconductance (g_m).

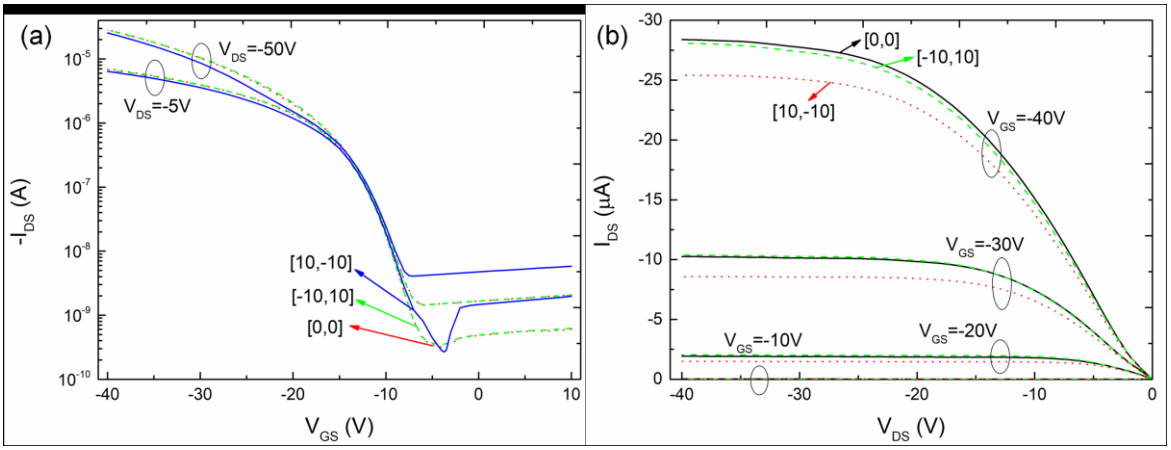

Fig. 13. Effect of the TIPS-Pentacene film thicknessnon-uniformity on the I_{DS}-V_{GS} (input) (a) and I_{DS}-V_{DS}(output) (b) electrical characteristics. All devices have an average channel thickness of 80 nm, while [10,-10] corresponds to thinner by 10 nm channel near the Drain electrode side and [-10,10] corresponds to thinner by 10 nm channel near the Source electrode side.

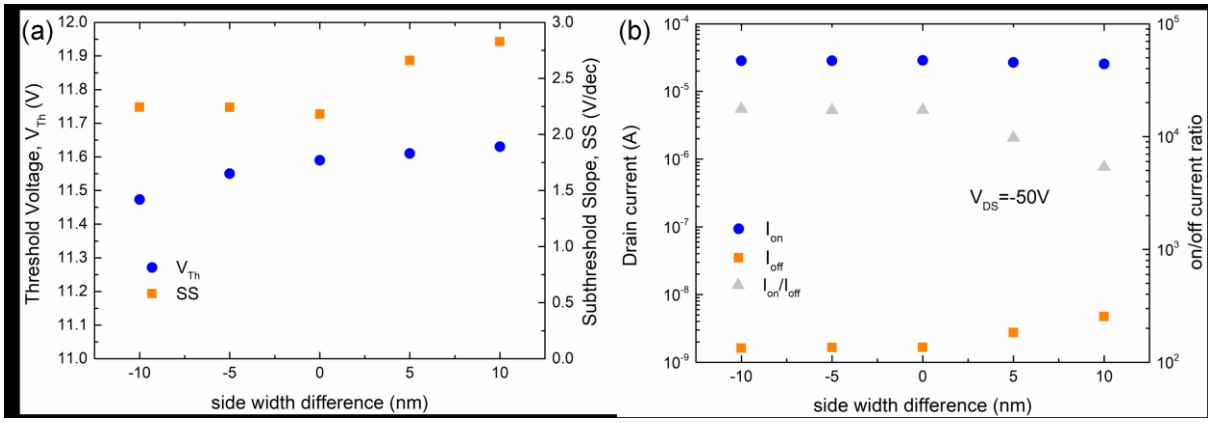

Fig. 14. Effect of the TIPS-Pentacene film thickness non-uniformityin electrical characteristics of devices with average 80 nm channel thickness and local differences of thickness up to ±10 nm. Graph of the extracted parameter variation of the threshold voltage (V_{Th}) and the subthreshold slope (SS) (a), as well as of the I_{ON}, the I_{OFF} and the ON/OFF current ratio (b) for the same range change of the side width difference.

Fig. 14a illustrates the threshold voltage (V_{Th}) and Subthreshold Slope (SS) electrical parameters variation with the side width difference. Particularly, V_{Th} is monotonously increasing with increasing the side width difference near the source electrode from -10 nm (+10 nm near the drain electrode) to +10 nm (-10 nm near the drain electrode), while the best SS value (the lowest SS value) is observed in the "untouched" (ideal) device (side width difference equal to 0 nm). In the range of -10 nm to +10 nm the SS value is changing from 2.18 V/dec to 2.83 V/dec (Fig.14a). According to the Fig.14b, the ON current (I_{ON}) is not significantly affected by the side width difference -only a slight decrease of its value to be observed when the side near the drain electrode is thinner (thicker near the source electrode). On the other side, the OFF current (I_{OFF}) exhibited animportant variation with increasing the side width difference, as can be observed in Fig.14b,and therefore the ON/OFF current ratio (I_{ON}/I_{OFF}) also showed a substantial change in its value in the range from -10 nm to + 10 nm (Fig.14b). Finally, in all cases the non-uniformity is introduced, the electrical parameter of transconductance (g_m) is dramatically affected, decreasing its value about 5 times as compared to the "untouched" (ideal) device ($g_m = 1.27 \times 10^{-5}$S).

Trying to investigate the contribution of the interface roughness and local channel thickness variation, we conducted several simulations, presented in Fig. S3, either with interface traps (a to c) or without interface traps (d to f). In Fig. S3e we see the simulated output (I_{DS}-V_{DS}) electrical characteristics of the device with local channel thickness smaller by 10 nm in respect to the mean channel thickness of 80 nm near the drain electrode and zero traps at the TIPS-PEN/PS interface. In the same figure the simulated output (I_{DS}-V_{DS}) electrical characteristics of the device with a uniform TIPS-PEN organic semiconductor film thickness and traps at the active interface (TIPS-PEN/PS) are also shown. It is evident in Fig. S3e that the drain current (I_{DS}) of the simulated output electrical characteristics is significantly larger in the case we consider a non-uniform TIPS-PEN organic semiconductor film thickness bur neglect the interface traps. This is a quite reasonable result for the given device architecture (BG-TC) we examine here,since the TIPS-PEN thickness non-uniformity is introduced at the top interface of TIPS-PEN, while the interface traps are introduced at the bottom interface (active interface) of TIPS-PEN with the PS insulating polymer within the conductive channel thickness. We conclude that the major contribution to the simulated output electrical characteristics is achieved after combining the TIPS-PEN thickness non-uniformity and the non-zero traps at the active interface (Fig. S3b) in the presence of the interface traps.

Similar results were obtained by simulating with an interface roughness (RMS=1.25 nm) and without interface traps (Fig. S3d) compared with a device which includedboth interface roughness and local channel thickness non-uniformities (local channel thickness is smaller by 10 nm in one side and larger by 10 nm in the other side) and without interface traps (Fig. S3f). However, the drain current (I_{DS}) of the simulated output electrical characteristics obtained from these cases is not as large as in the case we consider a non-uniform TIPS-PEN thickness without interface traps (Fig. S3e) due to the presence of the roughness at the active interface.

It is concluded that the interface traps cannot be neglected, since they have the major impact on the simulated output electrical characteristics, also, they have larger impact when they are combined with the interface roughness (Fig. S3a), or with the local channel thickness non-uniformities (Fig. S3b), or both (Fig. S3c).

Convergence of the simulated output electrical characteristics with the experimental ones can be achieved considering the interface traps combined with the interface roughness (Fig. S3a), but in order to explain the variability in the electrical behavior of "similar" samples, local channel thickness non-uniformities should be taken also into account.

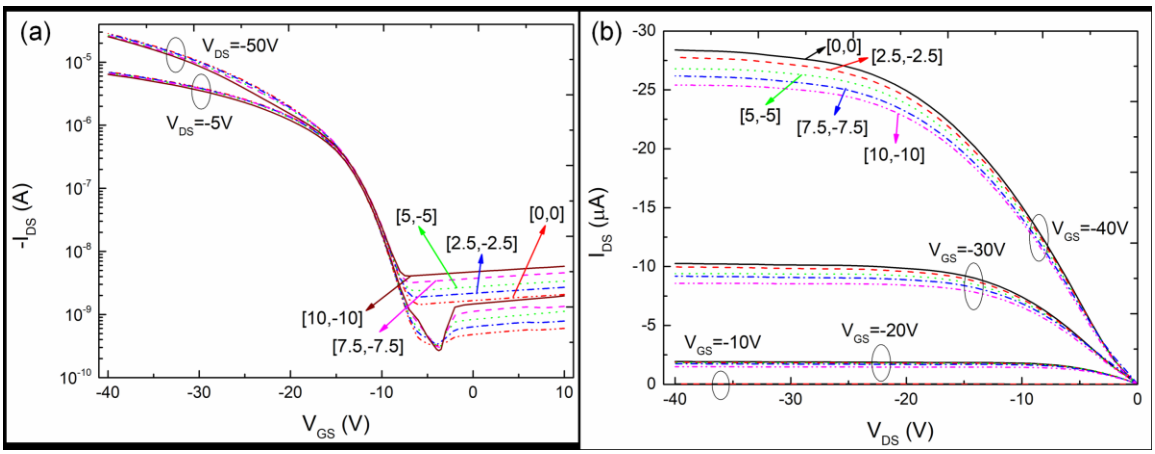

Fig. 15. Effect of the TIPS-Pentacene film thickness on the I_{DS}-V_{GS} (input) (a) and I_{DS}-V_{DS} (output) (b) electrical characteristics of devices with average 80 nm channel thickness – thinner near the Drain side and local differences of thickness up to ±10 nm.

Since non-uniformity near the Drain (thinner channel) is more crucial in the electrical behavior of the device, next "experiment" was to investigate how different thickness variations near the critical side (Drain side) of the device affect the characteristics of the device and the implications to the corresponding extracted electrical parameters, especially when the thickness is decreased down to 10 nm. In this case we change the local thickness of the channel, by increasing it up to 10 nm in the first half of the channel near the source side and decreasing itdown to 10 nmfrom the middle of the channel until the drain side, thus maintaining the mean value of the channel thickness (80 nm) in all cases we compared.

Fig. 15a and Fig. 15b are showing the effect of the different step heights on the input (Fig. 15a) and output (Fig. 15b)electrical characteristics, indicating an obvious degradation of the drain current and the ON/OFF current ratio (I_{ON}/I_{OFF}) electrical parameter with increasing the step height from 0 to 10 nm.

Extraction of the corresponding electrical parameters reveals that the threshold voltage (V_{Th}) electrical parameter is monotonously decreasing as it is shown in Fig.16a, without exhibiting any significant change in its value when the step height is varying from 0 to 10 nm. Likewise, the TIPS-Pentacene:PS blend OFETs' subthreshold slope (SS) electrical parameter did not show its value which is ranging from 2.18 to 2.12 V/dec to differ importantly in the range of 0 to 10 nm (Fig. 16a). In the same figure, the "untouched" (ideal) device exhibited the highest SS value. Fig. 16b depicts the ON current (I_{ON}) electrical parameter variation with the step height, indicating that it is little affected by increasing the step height from 0 to 10 nm and more specifically a slight decrease in its value is observed in this range. Contrary to the ON currentbehavior in the range of 0 to 10 nm, the OFF current (I_{OFF}) electrical parameter presented a significant difference in its value in the same range, and particularly a degradation of that electrical parameter can be clearly seen in Fig. 16b when the width near the drain side is becoming thinner (80 to 70 nm). As a result, the ON/OFF current ratio (I_{ON}/I_{OFF}) also demonstratedan important degradation of its value with increasing the step height from 0 to 10 nm (Fig. 16b).

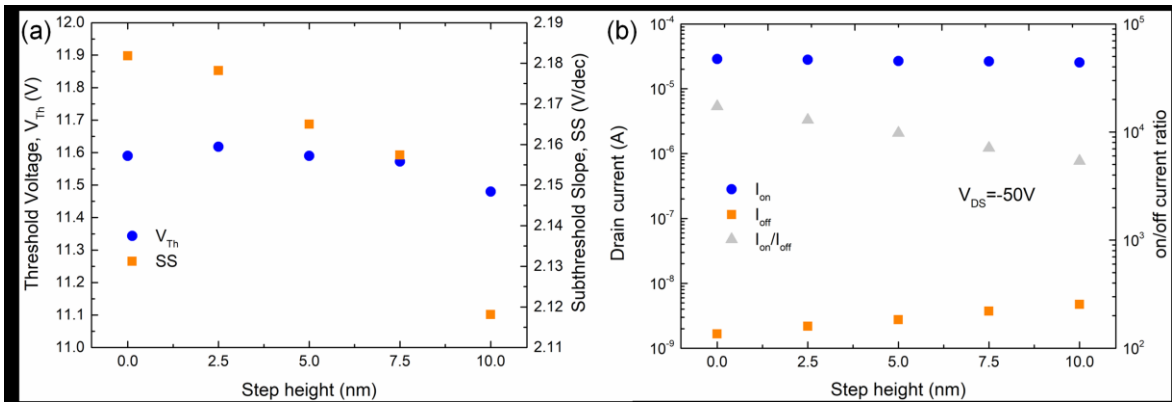

Fig. 16. Variation of the threshold voltage (V_{Th}) and the subthreshold slope (SS) (a) as well as of the on-current I_{ON}, off-current I_{OFF} and their ratio(b) for inhomogeneity extending in the half channel and varying in the step height near the Drain increasing from 0 (ideal case) to 10 nm.

Next possible simulation of inhomogeneity in channel comprised a thinner channel near the drain (by 10 nm) and varying length (extend) from 0 nm (ideal device) to 40 nm (which corresponds to the half channel length). Surprisingly, only the SS was really affected, since all the devices – except the untouched – had very similar electrical behavior, making this comparison less important.The above-mentioned results allowed us to conclude that only the insertion of the non-

uniformity has caused deviation from the behavior of the ideal case but the differences among samples of different step width are not important, something we did not expect a priori.

Similarly, by creating within the channel a step (of 20 nm length and a height of 10 nm)- introducing an area with smaller channel width- and moving its center from the Source's side (center initially at 20 nm) up to the Drain's side (final center at 60 nm), we concluded again that the only observable change was in the SS (2.20 to 2.15 V/dec), which is not significant. It is worth to note here that, among the different step positions, the lowest drain current value is obtained in the case that the step is in the middle of the channel (step center position at 40 nm). The step looks like to divide the channel in two areas and this becomes more important when the narrow side is in the middle of the channel.

To further extend our simulation study and verify our scientific findings in other device geometries and materials, we incorporated the bottom-gate bottom-contact (BG-BC) OFET device geometry that has been broadly used so far in OFET device simulation studies[14,15]. In order to define the regions and create the 2D BG-BC OFET device structure in DevEdit tool we used the geometrical characteristics concerning the channel length (L = 50 μm) and width (W = 1000 μm) as well as the thicknesses (t) of the individual layers according to a recently published work[14]. Moreover, we consulted the same study in order to specify the materials we used in our simulations and these materials included the pentacene organic semiconductor, the Au source and drain electrodes, the SiO_2 gate dielectric and the Cu gate electrode. Fig. 17a illustrates the 2D BG-BC OFET device structure as specified in DevEdit tool. The material thicknesses (t) are also shown in Fig. 17a. The simulated I_{DS}-V_{DS} (output) electrical characteristics obtained from the Atlas (Silvaco) tool and referred to the BG-BC OFET device (Fig. 17a) are depicted in Fig. 17b.

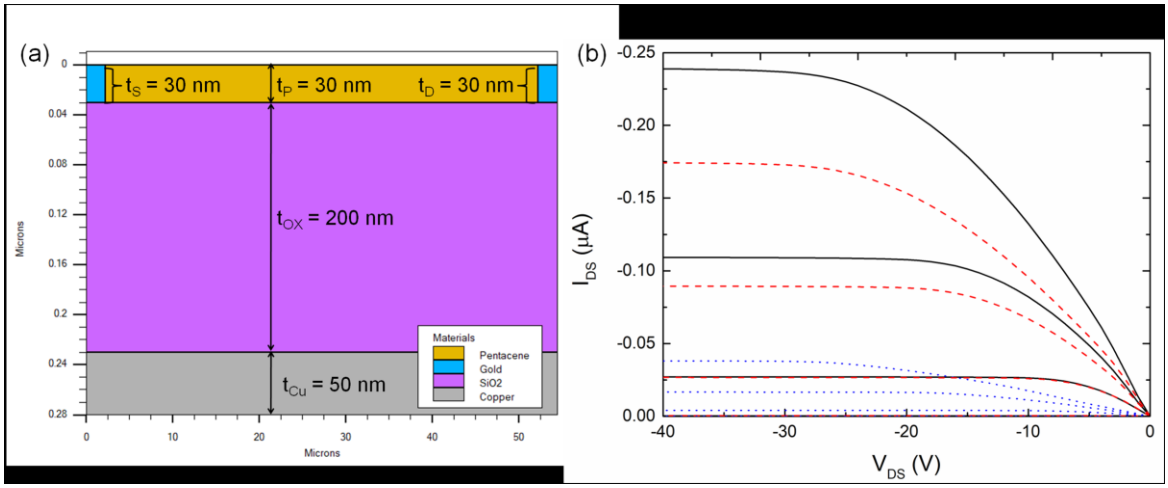

Fig. 17. The 2D BG-BC OFET device structure created in DevEdit tool (a) as well as the corresponding I_{DS}-V_{DS} (output) electrical characteristics obtained from the Atlas simulator (black solid lines) (b). The simulated I_{DS}-V_{DS} electrical characteristics obtained from a non-uniform pentacene organic semiconductor film thickness (red dashed lines) as well as the simulated I_{DS}-V_{DS} electrical characteristics obtained in the case a roughness is considered at the pentacene/SiO_2 active interface (blue dotted lines) (b). The gate voltage (V_{GS}) is varied from -10 to -40 V with a step (ΔV_{GS}) of -10 V.

Consequently, in order to investigate the effect of the pentacene organic semiconductor film thickness non-uniformity on the simulated I_{DS}-V_{DS} (output) electrical characteristics, we reduced by 20 nm the local channel thickness from the middle of the channel to the source electrode side (Fig.S4b). We replaced the empty region resulted from the local channel thickness reduction (by 20 nm) near the source electrode with air-dielectric. As expected, the simulated results revealedareduction of the drain current (I_{DS}) of the simulated I_{DS}-V_{DS} electrical

characteristics (red dashed lines in Fig. 17b) compared to that of the simulated I_{DS}-V_{DS} electrical characteristics obtained from a uniform pentacene film thickness (black solid lines in Fig. 17b). This result is attributed to a smaller contact area between the Au source electrode and the pentacene organic semiconductor.

Finally, we introduced interface roughness by inserting a square wave pattern at the pentacene/SiO_2 active interface (Fig. S4a) with specific characteristics including an RMS value equal to 1.25 nm (peak-to-peak value is 2.50 nm) and number of periods equal to 9. The simulated results indicated that the introduction of the interface roughness greatly influenced the simulated I_{DS}-V_{DS} electrical characteristics (blue dotted lines in Fig. 17b). In particular, it resulted in a large drain current (I_{DS}) reduction compared to that obtained without interface roughness (black solid lines in Fig.17b),and significantly lower than that in the case we consider an "exaggerated" reduction of the local channel thickness near the source electrode (red dashed lines in Fig. 17b). Thus, as expected, these two alterations of the devices can be very important also in other devices' geometries and materials.

CONCLUSIONS

We herein reported on the simulation resultsfrom the OFET devices based on the spray-deposited TIPS-Pentacene:PS blends (0.8:0.2w/w). The simulation results were obtained with a commercial TCAD tool (Silvaco-Atlas) and validated against the experimental ones. Physical quantities including the shallow donor-type bulk and interface traps DOS and negative interface chargeswere considered in our study, along with proper values in their models, as they emerged from the necessity to achieve better convergence of the simulations to the experimental data. Also, the physical models we selected in our study included the constant low-field mobility model as well as the band-to-band tunneling model. The parameters of both models needed to be carefully adjusted in order to obtain the best fit with the experimental data. By comparing the simulated I_{DS}-V_{GS} electrical characteristics with the experimental ones a very good convergence was revealed, while the comparison between the simulated I_{DS}-V_{DS} electrical characteristics and those obtained from the experiment demonstrated a significant divergence. To further improve the simulated I-V electrical characteristics, we also included in our simulations different approaches simulating the interface roughness at the active interface. Critical parameter to describe this was the RMS of the interface roughness. The best simulation results were obtained with an RMS roughness of 1.25nm and the overall results were clearly improved when they were compared to the experimental data. Further simulation results revealed a severe degradation of the device's electrical performance with increasing the RMS roughness at the TIPS-Pentacene/PS interface from 0 to 3nm, while applying different patterns to the active interface - such as trapezoidal, sinusoidal and square - is of less importance.

Finally, in order to explain the weakness to describe better some of the data representing specific similar samples, we examined the result of the TIPS-Pentacene thickness non-uniformity we observed in all samples. According to the simulation outcomes, the inhomogeneity in the thickness of the active channel is more important (performance degradation) when the semiconductor is thinner near the drain side. We followed different approaches to introduce practically the non-uniformity and revealed the impact on the device's overall electrical behavior and the corresponding variability it can cause.

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SupportingInformation

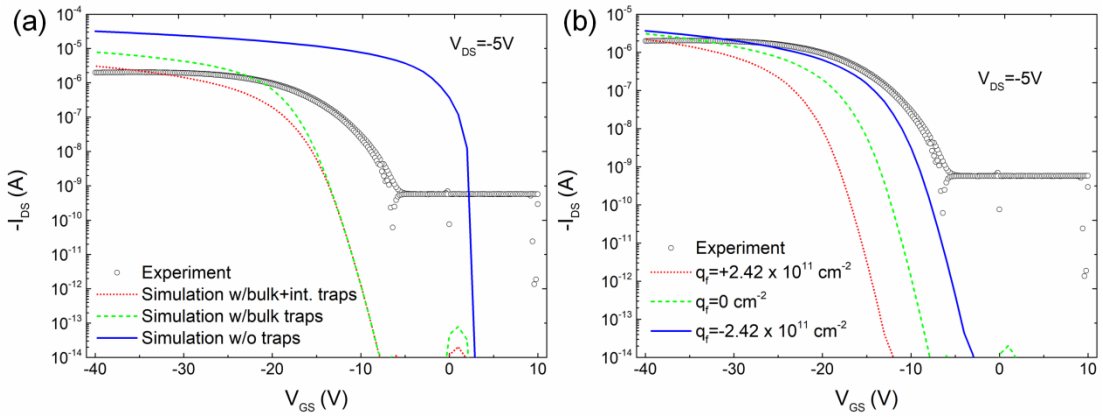

Fig. S1. Comparison of the simulated I_{DS}-V_{GS} electrical characteristic at V_{DS}= -5V without traps (blue continuous curve), with bulk traps (green dashed curve),with both traps -bulk as well as with interface traps- (red dotted curve), and the experimental one (a). Effect of the interface charge density to the simulated I_{DS}-V_{GS} electrical characteristic at V_{DS}= -5V, with zero (green dashed curve), positive (red dotted curve) and negative (blue continuous curve) charge density values, as compared to the experimental characteristic (b).

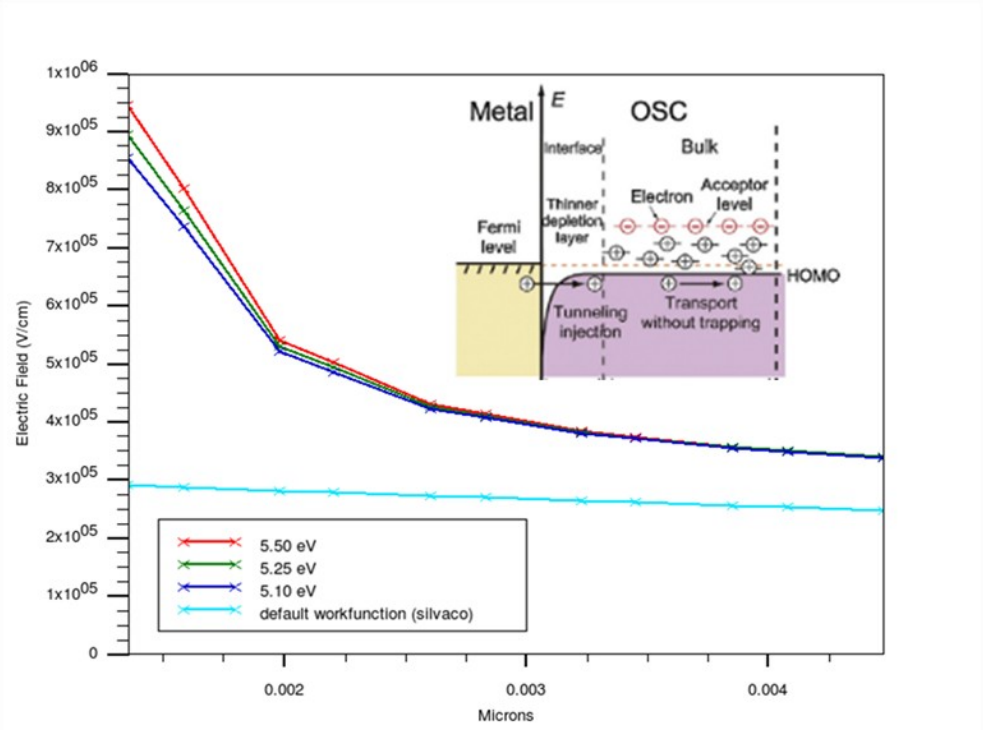

Fig. S2. Diagram showing the electrical field variation underneath the source and drain contacts by changing the gold source and drain contacts work function value. The inset image shows the direct tunneling mechanism from metal to an organic semiconductor (OSC).

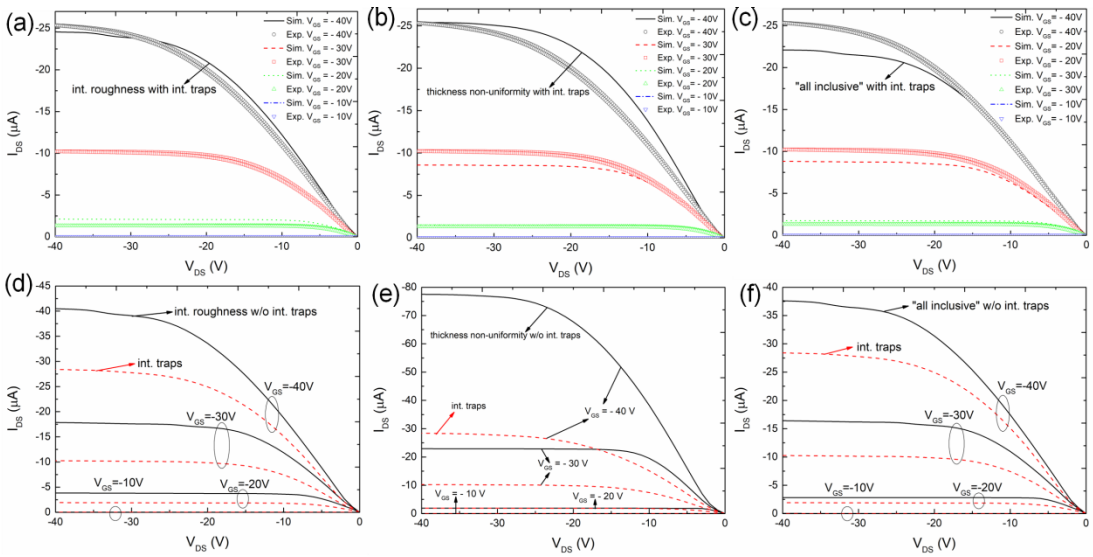

Fig. S3. Diagrams showing the effect of the interface traps on the simulated output electrical characteristics (I_{DS}-V_{DS}) combined with interface roughness (RMS=1.25 nm)(a), TIPS-PEN thickness non-uniformity (local channel thickness is smaller by 10 nm in respect to the mean channel thickness of 80nm near the drain electrode)(b) and both interface roughness (RMS=1.25 nm) and local channel thickness non-uniformities (local channel thickness is smaller by 10 nm in one side and larger by 10 nm in the other side) ("all inclusive") (c). In these diagrams the experimental characteristics are included for comparison. In diagrams (d)to (f) the same characteristics are depicted without the influence of the interface traps and compared to those of the device with a uniform TIPS-PEN film thickness and interface traps, to stress out the importance of the interface traps in the electrical behavior of the device.

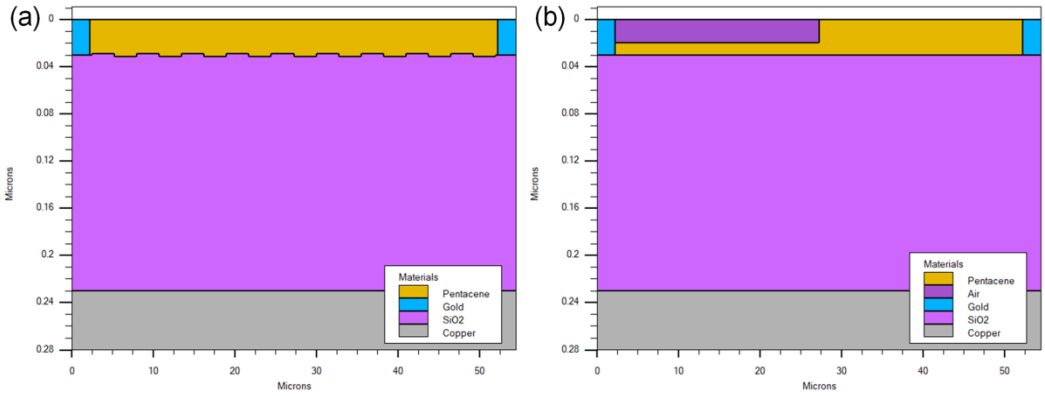

Fig. S4. The BG-BC OFET device structure including interface roughness by inserting a square wave pattern at the pentacene/SiO_2 active interface with an RMS parameter value and a number of periods equal to 1.25 nm and 9.0, respectively (a) as well as a reduction by 20 nm of the local channel thickness from the middle of the channel up to the source electrode side (b).