ΠΟΛΥΤΕΧΝΕΙΟ ΚΡΗΤΗΣ

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On-wafer Electrical Characterization of Silicon Carbide (SiC) JFETs

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ABSTRACT

Power electronics technologies are very important in electrical energy conversion systems, where the power semiconductor devices play a crucial role. Power electronics technologies have developed with silicon (Si) material which is approaching its theoretical limits. As a result, nowadays new wide bandgap (WBG) semiconductor materials exhibit great interest and seem to be suitable for the next generation power electronics applications.

Silicon Carbide (SiC) is a very promising WBG material with a set of superior properties, including wide bandgap, high thermal conductivity, high critical electric field and high electron mobility. This makes it an excellent material for electronic device applications that can operate under high temperature and high power conditions. Our work was focused on the electrical characterization of Junction Field-Effect Transistors (JFETs) and diodes fabricated with this material at the premises of Microelectronics Research Group at IESL-FORTH. Many samples were characterized which led to the extraction of useful results and conclusions about both the electrical characterization procedure, and the design and fabrication process that has been followed. Detailed information about the latter ones is provided in chapter 3. Hereby, the results from two samples are reported as the measurements and the extraction procedure in their case, were systematic and can, thus, give a comprehensive description of the subject.

In chapters 4 and 5 the electrical characterization procedure, including the different measurements that need to be carried out and the corresponding experimental setups are described, along with the results of the characterization of the two different samples. Moreover, in the last chapter the agreement of the measured characteristics with the theoretically anticipated ones according to the JFET theory, is investigated. There is comparison between some measured results and the corresponding simulated. The theory for the JFET operation, is presented in chapter 2. It is worthwhile to mention that for the simulations the MATLAB software was used.

In the Appendices, the reader can find a comprehensive report for the capacitance voltage-measurements in FETs (Appendix 1) and a compact handbook including equations for the calculation of critical JFET parameters (Appendix 2). Moreover, in Appendix 3, the MATLAB scripts used for the simulations are presented.

ΠΡΟΛΟΓΟΣ

Η παρούσα διπλωματική εργασία εκπονήθηκε στον τομέα Ηλεκτρονικής και Αρχιτεκτονικής Υπολογιστών της Σχολής Ηλεκτρονικών Μηχανικών και Μηχανικών Υπολογιστών του Πολυτεχνείου Κρήτης.

Υπεύθυνος κατά την εκπόνηση της διπλωματικής εργασίας ήταν ο Αναπληρωτής Καθηγητής κύριος Matthias Bucher στον οποίο οφείλω ιδιαίτερες ευχαριστίες αρχικά για την ανάθεσή της καθώς και για την άψογη επιστημονική υποστήριξη και καθοδήγηση που μου προσέφερε.

Θερμές ευχαριστίες οφείλω στον κύριο Κωνσταντίνο Ζεκεντέ, Ερευνητή Β' του Ιδρύματος Τεχνολογίας και Έρευνας (ΙΤΕ) για την αμέριστη βοήθεια, την υποστήριξη και τις κατευθυντήριες συμβουλές που μου παρείχε καθ' όλη τη διάρκεια εκπόνησης της εργασίας. Ακόμα ευχαριστώ ιδιαιτέρως τον συνάδελφο Ηλ. Μηχανικό Μ. Βασσάκη, τον υποψήφιο Διδάκτορα του Πολυτεχνείου Κρήτης, Ν. Μακρή καθώς και την ομάδα Μικροηλεκρονικής (MRG) του ΙΗΔΛ-ΙΤΕ και ιδιαίτερα την κυρία Μ. Καγιαμπάκη. Χωρίς τη πολύτιμη αρωγή και συνεισφορά όλων τους η εκπόνηση της εργασίας αυτής δεν θα ήταν δυνατή.

Τέλος, θέλω να ευχαριστήσω την οικογένειά μου για την αμέριστη εμπιστοσύνη που ανέκαθεν μου έδειχναν.

Χανιά, Απρίλιος 2016

Κωνσταντίνος Ι. Βαμβουκάκης

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Chapter 1. Introduction

1.1 WBG Semiconductor materials

Power electronics technologies are very important in electrical energy conversion systems, where the power semiconductor devices play an crucial role. Some of the potential application areas for these WBG devices include: transportation electrification and renewable energy. Regarding renewable energy which is a major trend today, wide bandgap devices have been explored for replacement of Si insulated gate bipolar transistors (IGBTs) in photovoltaic inverters in order to improve efficiency. WBG semiconductors are well suited for these applications due to their high temperature capabilities, fast switching speeds, and low losses. The high temperature capability of these devices allow them to better withstand the harsh environmental conditions, and have relaxed cooling system requirements. In addition to this high temperature capability, the fast switching speed of these devices allows for higher frequency operation thereby resulting in the reduction of the passive components, which decreases the total size, weight, and cost of the system.

Since the birth of the first power transistor in 1947, power electronics technologies have developed with silicon (Si) material. Up until today, with the development of more than 60 years, Si power semiconductor devices fabrication process is very mature and can meet different power demands in electrical energy conversion [10]. However, compared to Si, wide bandgap (WBG) semiconductor materials have lots of advantages which are very attractive for new power electronics applications. As silicon devices are approaching its theoretical limits, wide bandgap semiconductors are naturally suitable for the next generation power electronics applications. Even though they are not yet challenging silicon's existing dominance in this market, their increasingly maturing technology is expected to lead to great commercialization success in the years to come. While SiC has been identified as a very promising material for power electronics applications, the high-performance devices based on SiC cannot become true unless a broad range of device fabrication technology has been developed for this material. During the last twenty years, a substantial amount of efforts have been spent on the research and experimental development of SiC processing technologies. Fortunately, most of the general microelectronic techniques developed by the silicon industry can be directly applied to SiC device fabrication with little or minor modification. Furthermore, specialized process technologies for SiC etching, selective doping and dopant activation, ohmic and Schottky contact structures, etc. have also been well developed.

Material properties of important semiconductors

Material	E_g [eV]	n_i [cm^{-3}]	ε_r	μ_n [$cmV^{-1}s^{-1}$]	E_c [MV/cm]	v_{sat} [10^7 cm/s]	λ [$Wcm^{-1}K^{-1}$]
Si	1.12	1.5×10^{10}	11.8	1350	0.3	1.0	1.5
Ge	0.66	2.4×10^{13}	16.0	3900	0.1	0.5	0.6
GaAs	1.4	1.8×10^{6}	12.8	8500	0.4	2.0	0.5
GaN	3.39	1.9×10^{-10}	9.0	900	3.3	2.5	1.3
3C-SiC	2.2	6.9	9.6	900	1.2	2.0	4.5
6H-SiC	3.0	2.3×10^{-6}	10	370^a 50^c	2.4	2.0	4.5
4H-SiC	3.26	8.2×10^{-9}	9.7	720^a 650^c	3.0	2.0	4.5
Diamond	5.45	1.6×10^{-27}	5.5	1900	5.6	2.7	20

Table 1.1: Properties of important semiconductor materials. [13]

A comparison of some material properties of several important semiconductors is listed in Table 1.1 above. The energy bandgap Eg between conduction band and valance band is 1.12eV for Si, while that for SiC, GaN and Diamond is 3.26eV, 3.39eV and 5.45eV respectively. A big value of E_g means that an electron is less possible to go through this band when temperature increases, allowing higher maximum operating temperature values. In terms of thermal conductivity, SiC and Diamond are much greater than Si, which means that they can transfer heat easily thus higher current densities are anticipated for SiC power devices. It is also observed that WBG materials have smaller relative permittivity ε_r and bigger saturation velocity v_{sat} than Si. Thus, smaller ε_r helps to realize power semiconductor devices with smaller inter-electrode capacitances, thereby to increase fast switching abilities. For the critical breakdown field E_c, there are much bigger values for WBG materials than Si, which indicates that for the materials with the same thickness, there are much bigger breaking voltages for WBG materials than Si.

To sum up, SiC, the material that our work is focused on, when compared to silicon, has three times wider bandgap (E_g), ten times higher critical electric field (E_c), nineteen orders of magnitude lower intrinsic carrier concentration (n_i), three times larger thermal conductivity (λ) and two times higher saturation velocity (v_{sat}). These characteristics show great potential to make power devices that can operate at higher power, higher temperature and higher frequency with lower leakage current, smaller conduction and switching losses, less stringent requirements in heat removal. From the three SiC polytypes 3C, 4H and 6H, 4H-SiC seems to be the most interesting one for the time being [13].

A quite descriptive figure for the properties of SiC follows. Properties of Silicon and GaN are also presented for comparison.

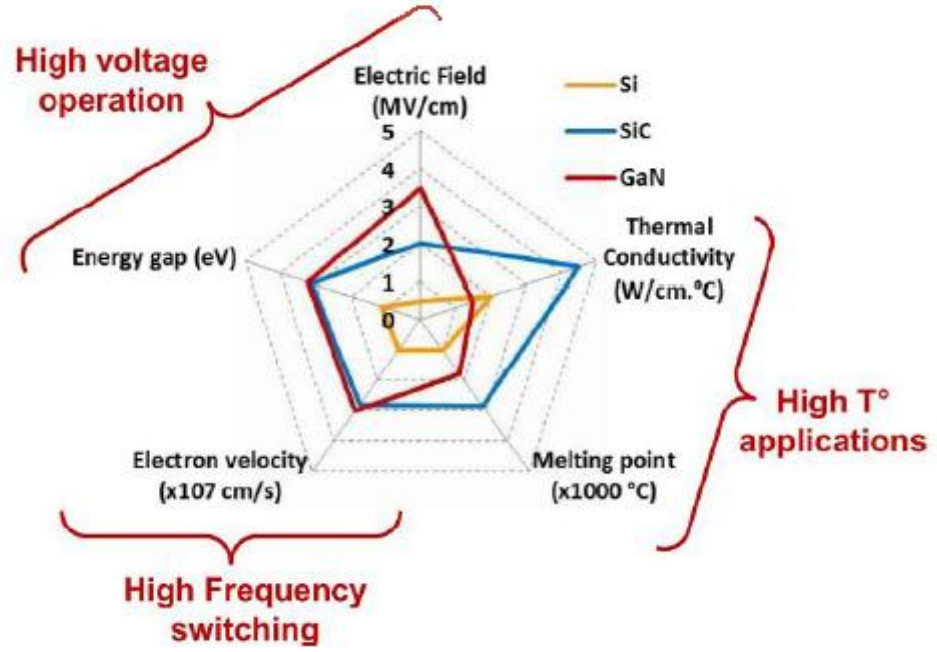


Fig. 1.1: Graphical representation of SiC, GaN and Si properties [14].

Moreover from the Table 1.1, it can be seen that diamond is an excellent candidate for power semiconductor devices, however, due to the complexity in the fabrication process, diamond power devices are not for the time being commercially available but intensive research is underway towards to the fabrication of diamond power devices.

1.2 SiC Power transistors

Silicon Carbide (SiC) is one of the earliest few materials that are recognized as semiconductors. Although SiC was named "the perfect semiconductor" by William Shockley back in 1950s, the difficulties of growing large size single crystals of SiC seriously delayed the development of SiC electronics with the first commercially available 2-inch SiC wafers introduced in the market in the beginning of the 1990's by Cree. These wafers were suffering from several micropipes per cm^2. Three and four-inch SiC wafers were also introduced after almost 10 and 15 years respectively, while today 6 inch are also commercially available. Over the years, the number of micropipes has reduced dramatically and significantly higher fabrication yields for SiC power devices are expected today than a few years ago making feasible the fabrication of SiC power devices that fully utilize the advantageous characteristics of the SiC material compared to silicon. Today, several manufactures are able to design and fabricate SiC power devices. Unfortunately, even though the material cost has been decreasing monotonically, the total cost of SiC devices is still significantly higher compared to the corresponding of the silicon counterparts. Nevertheless, it is believed that in the future, further reduction in the material cost, on the one hand, and on the other hand, lower development cost of the devices will both facilitate the replacing of silicon technology with SiC in several application areas. If the cost is investigated from the system perspective, it is obvious that, for instance, higher efficiencies using SiC power devices, can to some extent, compensate for the high device costs.

Today, the major types of power transistors under research and improvement include bipolar junction transistors (BJTs), metal-oxide-semiconductor field effect transistors (MOSFETs) and junction field effect transistors (JFETs). In many ways, BJTs are easier to fabricate than FETs, and are free from certain challenging issues, particularly with the gate oxides of MOSFETs. Many teams have been able to report low specific on-resistance, high-voltage BJTs. However, BJTs are current-controlled devices making the driving of them difficult since they require high base drive current compared to voltage-controlled FETs. This can account for substantial power dissipation in the device, and require complex and expensive input drive circuitry. JFETs and MOSFETs, on the other hand, are voltage-controlled, unipolar transistors that are low in gate drive current, and more advantageous for fast switching applications [14]. The attractiveness of SiC MOSFETs is obvious, considering the success of silicon MOS technologies and the fact that SiC is the only known wide bandgap semiconductor that can be thermally oxidized to form native SiO_2. However, with many teams making efforts in this area, several major problems still remain and limit its near-term applications, including low inversion layer electron mobility and poor gate oxide reliability. SiC power JFETs, on the other hand, offer a very promising alternative to SiC power MOSFETs by avoiding the trouble-making SiC-SiO_2 material interfaces. Detailed information about SiC JFETs is given below.

Junction Field Effect Transistor (JFET) is a voltage-controlled unipolar device which can be designed and fabricated either normally-on or normally-off. It is difficult to design normally-off JFET without significantly sacrificing the device performance (on-resistance or blocking voltage). On the other hand, normally-on device is able to handle more current density but it conducts current even when the gate bias is not applied. Therefore more complex gate drive and protection circuits are required in case of accidental failures of the gate control signal. The very first attempts to design and fabricate a SiC JFET were made in the late 1980s and the early 1990s. During that time the main research issues were dealing with developing SiC devices which would be capable of withstanding high currents and operating at high switching frequencies. The first SiC JFETs which had been fabricated in the laboratory were suffering from various problems affecting their performance. The difficulties in the fabrication process, but also the quality of the SiC material as such, all counted as development problems of SiC JFETs. During the last decade the significant improvement of the SiC

material quality, the development of 3- and 4-inch wafers and the design of high-performance JFET devices have all contributed to the fabrication of modern SiC JFETs.

Infineon Technologies and Cree Inc. introduced the first commercial SiC power devices in 2001 and 2002, which were SiC Schottky diodes [11]. The wild success of the SiC Schottky diodes led to the further development, and eventual commercialization, of the vertical trench SiC junction field-effect transistor (JFET) by SemiSouth Laboratories in 2008. The Vertical Trenched design (VTJFET) is up to now along with the so-called "Lateral-Channel JFET" (LCJFET) the two most common JFET designs. Although SemiSouth has dissolved, other companies such as Infineon and United Silicon Carbide, Inc. (USCi) have taken over the production of SiC JFETs, though choosing to focus on the depletion mode (normally-on) SiC JFET. The LCJFET has been manufactured by SiCED, which was merged with Infineon in late 2010. The SiC VTJFET can be fabricated as either a normally-OFF (Enhancement Mode-EMVTJFET) or a normally-ON (Depletion Mode-DMVTJFET) device. Enhancement mode JFETs also experience manufacturing complexity due to strict dimension requirements needed to achieve normally-off behavior. As a result, precise lithography and patterning techniques are needed. Alternatively, the depletion mode JFETs, which conduct current when no bias is applied to the gate, are a mature technology that has comparably relaxed processing requirements. Of course, since these devices are normally-on, added attention must be paid to the driving of these JFETs. In contrast to the DMVTJFET, the EMVTJFET requires a significant gate current in order to be kept in the on-state if a low on-state resistance has to be reached. The built-in voltage of the gate-source p-n junction is approximately 3 V. If the gate voltage exceeds this value, an unnecessarily high gate current flows through the gate-source junction and the VJFET operates in bipolar mode. This current is basically unproductive and will only cause additional losses in the gate.

Regarding the future perspectives of the SiC transistors, improved devices in terms of low on-state losses, high current and voltage capabilities, and/or high-temperature operation are favorable for future power electronics applications. Issues related to the long-term reliability, robustness and stability of the SiC devices are also crucial and they must be solved before mass production of these devices starts. It is believed that in the future SiC power devices having voltage ratings up to 40 kV may be a reality [11].

In the graph below we can see the progression of the commercialization of SiC devices from the first SiC Diode released by Infineon & Cree back in 2001 up to the SiC BJT by Fairchild in 2013.

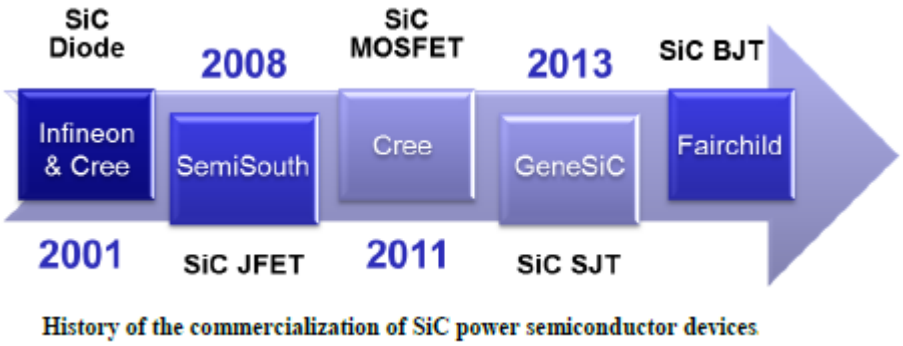


Fig. 1.2: Progression of the commercialization of SiC power semiconductors [17].

1.3 Scope of the Dissertation – Outline

The scope of the dissertation was to perform electrical characterization of the fabricated in Microelectronics Research Group of IESL-FORTH, 4H-SiC Vertical JFETs and support a research

program for the development and fabrication of such transistors. This was part of the research project “Development of new transistors and power inverter for photovoltaic systems using Silicon Carbide” which was part of the 7th general project of EU for the Research and Technological Development and particularly of the project "Synergasia". Partners and Cooperators of IESL-FORTH, in this project were the Technical University of Athens and particularly the group led by Professor Stefanos Manias, the Technical University of Crete and the group led by Associate Professor Matthias Bucher as well as the innovative Greek company RAYCAP.

The electrical characterization of the fabricated devices was a very important task as before the incorporation of the transistors in the inverter we had to be sure that the fabricated devices meet the desired specifications. The electrical characterization reveals the importance of the accuracy in the processing while is the main feedback for the process engineers as they try to optimize the performance of the transistors in the developing phase. The results of the electrical characterization of the fabricated devices are presented in this work. Prior to this, the procedure that must be followed along with the different measurement configurations are presented and explained in details. Thus a comprehensive measurements report for on wafer measurements is presented.

The thesis from now on is organized as follows.

Chapter 2. In this chapter the principle of VJFET operation is presented. The theory is presented accompanied by the formulas describing the operation of the transistors in a comprehensive way giving to the reader the chance to fully understand the laws governing the operation of the JFETs.

Chapter 3. In this chapter the structure and design of the devices that were investigated are presented. Furthermore, detailed information about their fabrication process is given, with description of all the different lithography steps.

Chapter 4. In this chapter the procedure that one has to follow in order to accomplish the on wafer electrical characterization of a sample is presented. From the on wafer state, the static characteristics can be measured. Detailed information is given for all the different measurements that must be performed as long as tips and warnings on the corresponding setups and configurations. Simultaneously, the results of the electrical characterization of the first fabricated sample that was investigated, the CB145602-P1 are presented.

Chapter 5. In this chapter the electrical characterization results of the second under test sample, the CB145602-P4 are presented.

Chapter 6. In this chapter simulations based on the JFET theory of chapter 2, are presented. Comparisons between some measured results from the two different under investigation samples and the simulated ones are carried out in order to evaluate the accordance of the measurements with the theory. The MATLAB software is used for the simulations.

Chapter 7. In this last chapter the conclusions extracted from the whole work are summarized. Mainly are included deductions as for the design, performance and applications of the samples as well as regarding their accordance with the theoretically anticipated results. In addition, suggestions for future work are given since the work covered in this dissertation has opened up a number of possibilities.

Afterwards, in Appendix 1 the reader can find a quite detailed and comprehensive report about the Capacitance-Voltage measurements procedure in a FET. The necessary configurations are presented along with warnings about the more common fatal errors than one is possible to do and involve erroneous measurements.

In Appendix 2 a compact handbook is presented. It summarizes all the formulas necessary for the calculation of critical parameters of JFET in a form that one has only to insert the input parameters expressed in their most common units for convenience and simplicity. In this way, by inserting the pure number in the equations you get easily and quickly the parameter value in its most common unit.

In Appendix 3 the MATLAB M-files used for the simulations of chapter 6 are presented.

The dissertation ends with the studied and consulted bibliography.

Chapter 2. Operation principle of JFETs

In this chapter the analytical theory describing the operation principle of a JFET is presented. This analysis is necessary as it was used for the MATLAB simulations (see chapter 6 and Appendix 3) and the comparisons between the measured and the theoretically expected (simulated) results. The formulas for the I-V characteristics in both the conduction and the blocking state as well as these for the calculation of the important JFET parameters (V_{TH}, R_{ON} etc) are presented. For quick calculation of the important JFET parameters the reader can also refer to the handbook of the Appendix 2.

2.1 Introduction – Principle of JFET operation

The present chapter reviews initially the principles of operation of VJFETs. The carrier transport mechanisms and the various operating regimes are discussed. Following, the analytical mathematical models describing the current-voltage characteristics are presented.

Device Structure

A simplified VJFET structure is shown on the right of Fig. 2.1. It is divided into two main regions: the channel region and the drift region. The depletions regions within the channel are not uniform in width because they are created from a V_{DS} bias, not a V_{GS}. On the left we can see a cross section of the transistor with its important dimensions.

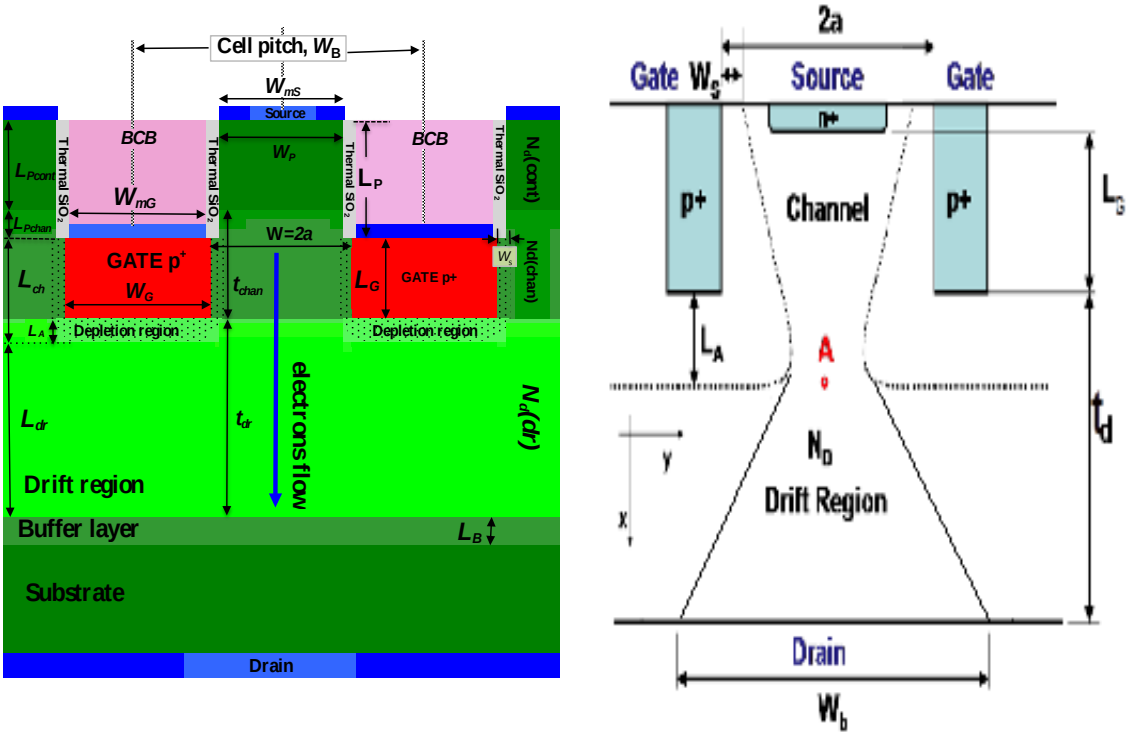


Fig. 2.1: Cross-section (left) and simplified for modeling purposes (right) JFET geometry.

i)Channel: it has a total width of W=2a and effective length L_{ch}=L_G+L_A where L_G is the gate (channel) length and L_A is the depletion layer width at point A in Fig. 2.1. The channel is usually lightly doped. While short channel lengths (L_G) minimize ohmic losses, long ones provide sufficient blocking voltages. The turn-off voltage (or threshold voltage), V_{TH}, is dependent on both the channel doping and width.

ii)Drift region: it has a total width W_b at the drain contact (unit cell width corresponding to mid-gates distance) and a length of L_{dr}-L_A where L_A is the depletion layer width near point A in Fig. 2.1.

The lightly doped n-type drift region is grown very thick ensuring high maximum blocking voltage. The drift region characteristics must be carefully designed to support the drain-gate voltages. Indeed, the maximum blocking voltage is a function of the doping concentration and the thickness of this drift region, as well as the critical electric field strength ($E_{c,br}$) of the semiconductor. For SiC, $E_{c,br}$ equals to $3\text{-}4\cdot10^6$ V/cm resulting in blocking voltage capability of about 100V for each micron of low doped or undoped drift layer thickness.

To prevent forward biasing of the gate-drain junction, the n-channel JFET must be operated with positive drain voltages for both conducting and blocking characteristics.

The resistance of the drift layer is of great importance. Including the current spreading in the drift region (see Fig.2.1), the R_{Drift} is given by the following equation [1]:

$$R_{Drift} = \frac{1}{q\mu N_{Dr} Z}\left[\frac{t_{dr} - L_A}{W_b - (2\alpha - 2L_A)}\right]\ln\left(\frac{W_b}{2\alpha - 2L_A}\right)$$

For the calculation of the total resistance, the resistance of all the different layers must be added. Thus the channel resistance (R_{ch}), the substrate resistance (R_{sub}) and that of the ohmic contacts (Source and Drain contact) should be added to the R_{Drift}.

In this way the on-resistance, R_{on}, is given by:

$$R_{on} = R_{Drift} + R_{sub} + R_{ch} + 2R_C$$

The source/drain metallization resistance R_C is considered equal for both cases. Of course, in the case of trenched devices, the resistance contributed from the mesa structure must be added for an accurate R_{on} calculation.

For power electronic engineers, the specific R_{ON} is interesting and is given in $\Omega\cdot cm^2$. It is equal to the R_{ON} value multiplied by the active area ($W_b \cdot Z$)

Device Operation Mechanisms

The vertical JFET with active gate control on both sides of the channel, can operate in four different current-voltage (I-V) modes, depending on the operating current and voltage magnitude, as well as device structure geometry. The four I-V operating modes are known as:

1.pentode-like mode,

2.triode-like mode,

3.mixed mode,

4.bipolar mode

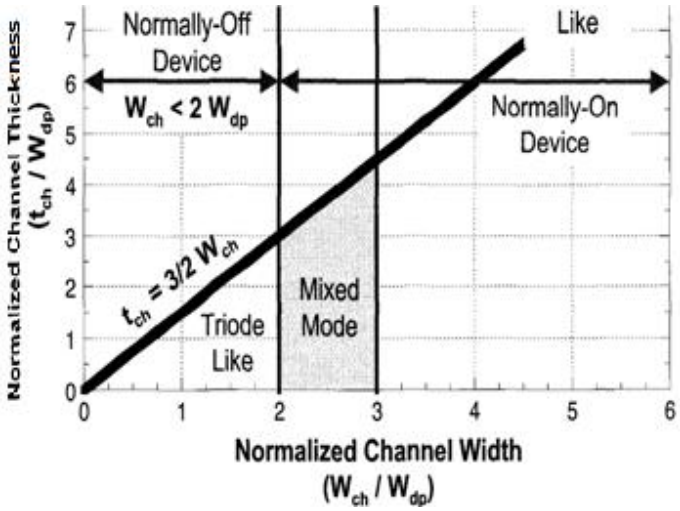


Fig. 2.2: Different I-V VJFET operation modes according to the geometry [41], (t_{ch} is L_{ch} and W_{dp}=depletion width)

The VJFET I-V characteristics are strongly dependent on device structure. The channel width (W=2α), channel length (L_{ch}), the ratio of (W/L_{ch}), and the channel doping (N_{ch}) are all essential parameters in determining the I-V characteristics of the JFET. The various modes of operation and the dependence of current on the controlling voltages can

be understood by examining the carrier and potential profiles in the channel and drift regions of both short and long channel JFETs.

Triode-like behaviours are pronounced in short gate geometries while pentode-like behaviours are more pronounced in long gate geometries.

Fig. 2.2 summarizes the effect of dimensions to the I-V operating modes of a VJFET.

Long-channel (L_G>3a) devices

Devices with long channels exhibit only pentode-like I-V characteristics. Applying a small drain voltage will subsequently cause linear current flow. This linear dependence of the current from the voltage is due to the resistive character of the channel. Note, however, that the reverse bias across the gate-channel junction is larger at the drain end of the channel than at the source end, and so the depletion layer is wider at the drain end of the device than at the source end (Fig. 2.1 right) when V_D becomes comparable to V_G. Further increasing V_D, the depletion layer at the drain becomes wider and wider until the channel pinches-off near the drain causing saturation of the current.

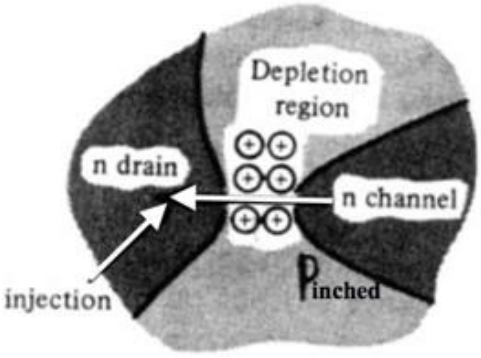


Fig. 2.3: Pinched-off area and electrons injection.

Let remind the physical image proposed by Shockley, for the current saturation for long channel devices. When channel pinch-off happens, the drain and the source are isolated from each other through the depletion region of the reversed-biased pn junction. However, the current entering the drain must exit from the source and an electron injection under high electric field through this region, is explaining the current conduction. Indeed, in the pinched-off region there is a very high field directed towards the source (for an n-channel JFET), created by the ionized donors in the pinched-off area and the accumulated electrons in the pinch-off point at the non-depleted side of the channel. Such an intense field causes the electrons flow from the channel tip in the pinch-off point to the pinched-off drain region (see Fig. 2.3). Thus, the current flowing through the pinched-off region is limited by the number of electrons that are injected into the depleted pinched-off region. Obviously, the magnitude of this current is determined only by the voltage drop across the undepleted part of the channel. By increasing further the V_D practically all the additional voltage appears across the depletion region and the pinch-off point moves slightly toward the source, shortening the length of the channel region containing free carriers. For long-channel devices this movement is small compared to the channel length with the consequence that the voltage at the pinch-off point remains V_{Dsat}. Thus, the current saturates to a value I_{Dsat} when V_D is increasing above V_{Dsat}.

On the other hand, if the gate is sufficiently reverse biased, the channel is fully pinched-off and no current flows from source to drain. At the same time, if the channel length is enough long, positive drain bias cannot lower the barrier imposed to electrons in the source (Fig. 2.4 (c)) and negligible current flows from drain to source.

Short-channel (L_G≤3α), normally-off (α<W_S) devices

VJFETs with short channel lengths and small channel widths usually exhibit triode-like I-V characteristics. The current carrier physical mechanism for V_{GS}<V_T can be explained by considering a carrier injection through a depleted area.

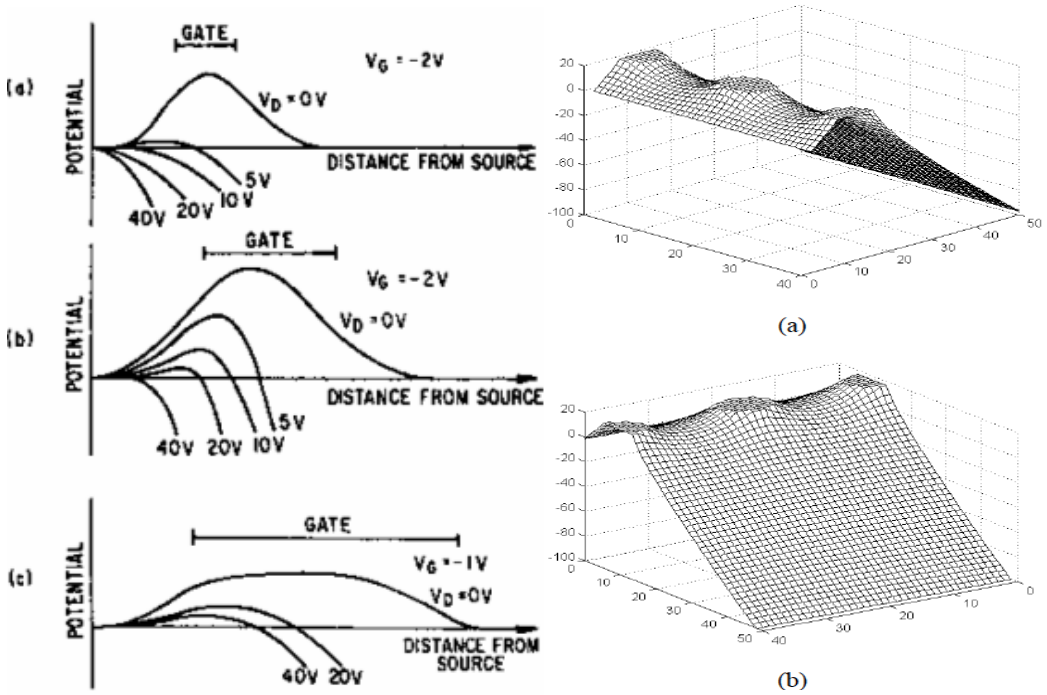


Fig. 2.4: Left: Impact of gate length on channel potential-barrier reduction by V_D for short (a), medium (b) and long (c) gates. [43] Right: Conduction-band-energy-minimum distribution (a) view from source, (b) view from drain. Three "fingers" are shown resulting in two "saddle points". [42]

Here, the channel is depleted all the way long but unlike the case of a long channel device, the carriers are blocked by a potential barrier (Fig. 2.4 [42]) whose peak and extent are controlled by both V_G and V_D. Indeed, when the channel length is small, the drain voltage has a strong influence on the potential along the source-drain axis, as shown in Fig. 2.4-*a (left)* by the rapid barrier reduction with increasing drain voltage. On the other hand, for long channel devices, the barrier height remains almost unaffected by the drain potential, as shown in Fig. 2.4-*c (left)*. Since the potential distribution is due to two voltages in perpendicular directions (biasing from V_{GS} and V_{DS}), involving potential curvatures in opposing directions, the shape of the two-dimensional potential barrier resembles a "saddle". The single peak in the distribution is referred to as the "saddle point" (Fig. 2.4 *(right)*). Obviously, the schematics in Fig. 2.4 correspond to a conduction band minimum shape along the channel. Thus, for a short, pinched-off channel device and for low V_{DS} bias levels, the potential barrier is high and the flow of carriers from source to drain small. Increasing V_D, would lower the potential barrier between the source and drain, and move the saddle point towards the source contact. With further increase in drain voltage, the saddle point potential continues to be lowered, and moves closer to the source contact and finally, a point is reached at some high drain voltage where the potential barrier is low enough and electrons are injected over this minimal potential barrier and current begins to flow in the channel.

A distinguishing characteristic of JFET operation in the pentode regime is the existence of a channel that supports current flow. In contrast, the channel in JFETs operating in the triode regime is depleted and electrons from source will flow towards the drain if the potential barrier is lowered by a positive drain bias voltage, without the existence of a physical channel.

The drain voltage (V_{DS}) at which current now begins to flow in the channel is referred to as the "blocking voltage" for a given gate voltage. Obviously, longer gates are required to obtain higher blocking gate capability while smaller channel widths also reduce the influence of the drain potential and result in higher blocking gains. The channel's potential lowering by the drain voltage, is a short-channel-effect (SCE) and it is often called "Drain Induced Barrier Lowering (DIBL)".

The parameter quantifying this gain control between the voltage across the device (V_{DS}) and the gate bias (V_{GS}) is called voltage gain (μ) and is defined as: $\mu = \left.\frac{\partial V_{DS}}{\partial V_{GS}}\right|_{I_{DS}}$

The channel width (or gate-to-gate spacing) plays a very important role in defining the blocking voltage gain. Narrower channels increase the blocking voltage capability (and voltage gain), but also decrease the current carrying capability, which results in lower output power and a higher on-state resistance.

Short and narrow channel devices ($L_G<3\alpha$, $W_S<\alpha<2W_S$) - Mixed mode operation

Mixed mode operation refers to a specialized structure, where the current-voltage characteristics exhibit neither the pentode-like mode nor the triode-like mode, but a combination of both modes ("mixed mode"), as shown graphically in fig. 2.5. The devices exhibit pentode-like I-Vs at large drain currents and low gate voltages while triode-shape I-Vs are measured at large gate voltages and low drain currents.

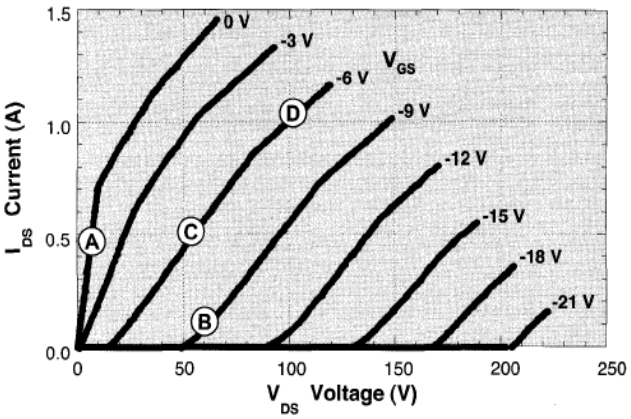


Fig. 2.5: SiC JFET I-V characteristics demonstrating mixed mode operation. [41]

Basically, mixed mode operation will occur when the ratio of the channel width to the zero-bias/single-sided depletion width (W/W_s) lies between 2 and 3, and when the ratio of the channel length to the channel width (L_{ch}/W) is less than 1.5.

Short-channel ($L_G<3\alpha$), normally-on ($\alpha>W_S$) devices

For short and wide channel JFETs, pentode operation appears if the gate bias is greater than the turn-off voltage and a triode one if the gate bias is smaller than the V_{TH}.

Note that, for short channel length devices the length of the pinched-off region is important in comparison to the total length of the channel. In this case, the saturated part of the output characteristics will be mainly controlled by the pinched-off region and more precisely by the continuous decrease of the channel resistance due to the decrease of the channel length. Therefore, the current never saturates completely but there is a continuous small increase in the saturation regime.

Bipolar mode (All geometries)

The bipolar mode of operation can occur at very low drain biases when the pn junction between the gate and the source is forward biased ($V_{GS}>0$) sufficiently so that the junction is turned on ($V_{GS}>V_{knee}$), allowing gate current to flow into the channel region. In this mode of operation, the JFET is no longer a voltage controlled, majority carrier device, but a minority carrier, current controlled current source.

In general, the bipolar mode is worthwhile in reducing the on-state resistance of the channel. Since operating in this mode primarily reduces the on-state resistance, the bipolar mode is not very beneficial when switching large voltages, where the on-state resistance is dominated by the drift region.

2.2 Analytical Description of VJFET Operation

2.2.1 Forward Conduction Operation

Below, analytical models that describe the forward JFET operation will be described.

Field Independent Mobility – Shockley Gradual Channel Theory

In the case of 4H-SiC, the condition of field independent mobility analysis is satisfied for electric fields lower than 10^4-10^5 V/cm.

If $V_{GS}<V_{TH}$ the channel is pinched-off and no carriers exist in the channel. If $V_{GS}>V_{TH}$ then a channel of mobile carriers will be formed. Application of a drain voltage causes carrier flow from source to drain. The gradual channel approximation has been proposed by Shockley for extracting analytical formulation of FETs current. The following assumptions are made: (a) the electron mobility, μ is constant and independent on the electric field and (b) the electric field, E_x, along the x (source-drain) axis, is much smaller than the electric field, E_y, along the y axis. These permit an one-dimensional calculation of the depletion width[1], W_x, of the gate junction at distance x from the source as a function of the potential, V_x, in the channel at location x:

$$W_x = \sqrt{\frac{2e}{qN_D}\left(V_x - V_{GS} + V_{bi}\right)}$$

The classic Shockley I-V relationship is [1, 5]:

$$I_D = \begin{cases} \dfrac{a^3 q^2 \mu N_D^2}{3\varepsilon}\dfrac{Z}{L_G + L_A}\left\{3\dfrac{V_A}{V_P} - 2\left[\left(\dfrac{V_A - V_{GS} + V_{bi}}{V_P}\right)^{3/2} - \left(\dfrac{-V_{GS} + V_{bi}}{V_P}\right)^{3/2}\right]\right\} & \text{if} \quad V_A - V_{GS} + V_{bi} < V_P \\ \dfrac{a^3 q^2 \mu N_D^2}{3\varepsilon}\dfrac{Z}{L_G + L_A}\left\{1 - 3\left(\dfrac{-V_{GS} + V_{bi}}{V_P}\right) + 2\left(\dfrac{-V_{GS} + V_{bi}}{V_P}\right)^{3/2}\right\} & \text{if} \quad V_A - V_{GS} + V_{bi} \geq V_P \quad \textit{saturation region} \end{cases}$$

where, Z is the source finger length, V_A and L_A are the potential and the depletion layer width at point A respectively (see Fig. 2.1) and

- $V_{bi} = \dfrac{KT}{q}\ln\left(\dfrac{N_D N_A}{n_i^2}\right)$ Built-in potential
- $V_P = \dfrac{qN_D a^2}{2\varepsilon}$ Pinch-off potential
- $V_{TH} = V_{bi} - V_P$ turn-off (or threshold) voltage
- $L_A = \sqrt{\dfrac{2\varepsilon}{qN_{D,dr}}\left(V_A - V_{GS} + V_{bi}\right)}$ Depletion width towards the drift layer

[1] The depletion width is always measured along y axis. So, the symbol W_x represents the depletion width along y-axis at the position x.

Obviously, the voltage V_A, which is an intrinsic drain voltage, is not the same as the applied from external supply, V_D. The voltage drop across the drift region resistance, the resistance of the substrate and the ohmic contact resistance has to be accounted for in the calculation of V_A:

$$V_A = V_D - I_D R_{Dr} - I_D R_{sub} - I_D R_C$$

For a quick and approximate calculation of the output current, V_A=V_D can be considered. Of course the calculation will be rough and is not recommended.

The on-resistance, R_{on}, of a power device is an important figure of merit because it determines the power dissipation in the JFET during current conduction. It is defined at small (<V_{bi}) V_D levels. The lowest on-resistance occurs when the depletion length L_A is the smallest. Usually it is assumed that this is achieved when operating at zero gate bias where the depletion width is created by only the built-in potential across the gate junction. The channel resistance as has been already mentioned is one of the main contributors of R_{on}. The channel resistance is given by:

$$R_{ch} = \frac{L_G + L_A}{2q\mu N_D Z\left(\alpha - W_S\right)}$$

From a design point of view, the on-resistance can be minimized by reducing the channel length L_{ch} and increasing the channel width 2α. However, this conflicts with achieving high blocking voltage. See Appendix 2 for the calculation of all the individual R_{on} terms.

Two important small-signal quantities are the output drain conductance (g_D) and the transconductance (g_m) defined by:

$$g_D = \left[\frac{\vartheta I_{DS}}{\vartheta V_{DS}}\right]_{V_{GS}=c^{te}} \qquad g_m = \left[\frac{\vartheta I_{DS}}{\vartheta V_{GS}}\right]_{V_{DS}=c^{te}}$$

The g_D in the linear regime is calculated from:

$$g_d = \frac{2aZq\mu N_D}{L_G + L_A}\left[1 - \left(\frac{V_A - V_{GS} + V_{bi}}{V_P}\right)^{1/2}\right] = \frac{2Zq\mu N_D}{L_G + L_A}\left(a - W_A\right) \overset{V_{bi} \succ V_D}{\cong} \frac{2aZq\mu N_D}{L_G + L_A}\left[1 - \left(\frac{-V_{GS} + V_{bi}}{V_P}\right)^{1/2}\right]$$

Obviously the g_d is zero at the saturation region while near the origin of the output characteristic is the inverse of the device resistance (R_{on}).

The g_m in the linear regime is calculated from:

$$g_m = \frac{2aZq\mu N_D}{L_G + L_A}\left[\left(\frac{V_A - V_{GS} + V_{bi}}{V_P}\right)^{1/2} - \left(\frac{-V_{GS} + V_{bi}}{V_P}\right)^{1/2}\right]$$

The g_m in the saturation regime is calculated from:

$$g_m = \frac{2aZq\mu N_D}{L_G + L_A}\left[1 - \left(\frac{-V_{GS} + V_{bi}}{V_P}\right)^{1/2}\right]$$ i.e. is equal to the g_D in linear regime.

Field Dependent Mobility

The constant mobility assumption of the previous section is valid as long as the electric field along the source-drain axis is smaller than 10^5 V/cm for SiC. This is true for devices with small width and large gate length. In devices with short and wide channels (suitable for high current handling capability) the electric field may exceed 10^5 V/cm prior to pinch-off making mandatory the accounting of the mobility field dependence.

The I-V relationship in such devices can be evaluated for a velocity-field relation of:

$$v\ (E_x) = \frac{\mu_o\ E_x}{\left[1+\left(\frac{\mu_o\ E_x}{v_{sat}}\right)^{\beta}\right]^{1/\beta}}$$

where E_x is the longitudinal electric field, v_{sat} is the carrier saturation velocity and constant β determines how abruptly carrier velocity goes from the linear region to the saturation region.

Let remind that for electrons movement in a plane vertical to the c-axis of 4H-SiC, at room temperature and for electric fields up to $4\cdot10^5$V/cm, the low field mobility μ_0 of electrons in 4H-SiC is given by the following equation [34]:

$$\mu_0 = 28 + \frac{950\left(\frac{T}{300K}\right)^{-2.4} - 28}{1+\left(\frac{T}{300K}\right)^{0.73}\left(\frac{N_D}{1.94\times10^{17}}\right)^{0.61}}$$

The reduced mobility of electrons with increasing electric field will cause a reduction of I_D for V_D values before pinch-off takes place. In these devices the output current characteristics will essentially follow the velocity-field characteristics of the carriers in the channel.

This reduction depends on V_G. If V_G is large (low I_D), the longitudinal electric field is small up to pinch-off drain voltages and the reduction of I_D due to the reduction of the mobility will be small. On the other hand, if V_G is small, the wide channel allows large drain current flow. This is accompanied by increased longitudinal electric field in the channel. Consequently, the reduction of I_D due to the mobility degradation will be higher.

As for the I-V characteristics, for the region below saturation [4, 44]:

$$I_D = \frac{a^3q^2\mu N_D^2}{3\varepsilon}\frac{Z}{L_G+L_A}\frac{\left\{3\frac{V_A}{V_P} - 2\left[\left(\frac{V_A - V_{GS}+V_{bi}}{V_P}\right)^{3/2} - \left(\frac{-V_{GS}+V_{bi}}{V_P}\right)^{3/2}\right]\right\}}{\left[1+\left(\frac{\mu_0\cdot V_A}{v_s\left(L_G+L_A\right)}\right)^{\beta}\right]^{1/\beta}}$$

where v_s=2.2•10^7cm/s and β^{300K}=1.2

The V_{Dsat} value is calculated through the following transcendental equation [4]:

$$\left(L_G+L_A\right)E_c = \sqrt{\frac{V_{bi}+V_{Dsat}-V_G}{V_p}}\left(\left(L_G+L_A\right)E_c + V_{Dsat}\right) - \frac{2}{3\sqrt{V_p}}\left[\left(V_{bi}+V_{Dsat}-V_G\right)^{3/2} - \left(V_{bi}-V_G\right)^{3/2}\right]$$

where E_C is the critical field for velocity saturation.

To obtain the saturation drain current, the solutions for V_{Dsat} can be used, so [4]:

$$I_{Dsat} = aZq\mu N_D E_c \left[1 - \left(\frac{V_{Dsat} - V_{GS} + V_{bi}}{V_P} \right)^{1/2} \right]$$

2.2.2 Forward blocking operation

For short gate (L_G<3*a*) JFETs, the blocking characteristics are of triode type with an exponential current-voltage characteristics at low currents and linear characteristics at high drain current range.

The low current regime is characterized by an exponential behavior with drain voltage reflecting the transport of carriers over a potential barrier. The exponential voltage dependence of the low current has been based, in all subsequent analysis, on the Nishizawa's [35] concept of continuous lowering of the barrier height by the drain voltage, I_D being exponentially related with the potential at the saddle point. This effect is similar to the drain-induced barrier-lowering (DIBL). Another common point for most proposed models, is that the value of barrier height Φ_b=0.5-0.6V is considered as the onset of significant current due to the static-induction effect.

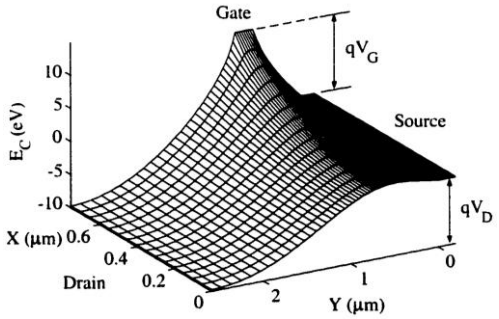


Fig. 2.6: Conduction band energy shown for the one half of the mesa. Reprinted from [36].

Speaking in terms of the potential-energy saddle shown in Fig. 2.6, while an increased drain voltage has the tendency to pull down the saddle maximum and to eventually make it vanish, the associated increased electronic current pushes it back up. So, two are the consequences of this high mobile carrier concentration: (i) the barrier height at the saddle point depends on the density of mobile carriers and, (ii) the current follows rather a linear I-V.

Several different models have been proposed for the physical mechanism of JFETs-triode-like operation.

Low current (exponential) regime

The triode characteristics reveal an exponential character at low currents. The current flow, in this case, is limited by the injection of carriers across the channel potential barrier. It can be described by the equation: $I_D = I_0 e^{-\left(q\Phi_b / kT\right)}$, where Φ_b is the minimum value of the electrostatic potential along channel axis (equivalent to a barrier height not allowing the transfer of electrons from source to drain) and the pre-exponential factor I_0 is a saturation current depending on the current transport mechanism involved.

Different models have been proposed and can be found in the literature for relating I_0 and Φ_b with transistor parameters and drain/gate voltages. Below a simple approach is presented briefly with all the necessary equations presented.

Wilamowski-Plotka model

An analytical description of carrier transport in triode operation mode was presented in [1, 37]. The potential distribution along the channel (region of potential barrier) as well as along the vertical to channel direction (y-direction from gate to gate), has been approximated by parabolas:

$$\varphi(x) = \Phi_b \left[1 - \left(2\frac{x}{L_G} - 1 \right)^2 \right] \qquad \varphi(y) = \Phi_b \left[1 - \left(2\frac{y}{W} - 1 \right)^2 \right]$$

where, Φ_b is the potential barrier height in reference to the source potential. The parabolic distribution allows the determination of an effective channel length, L_{eff}, which is the width of the barrier along x-axis as shown in Fig. 2.7 (*left*):

$$L_{eff} = 2x_b \sqrt{\frac{\pi kT}{q\Phi_b}} erf\left(\sqrt{\frac{q\Phi_b}{kT}} \right) \qquad (1)$$

where x_b is the position of saddle point ($\Phi(x)=\Phi_b$)

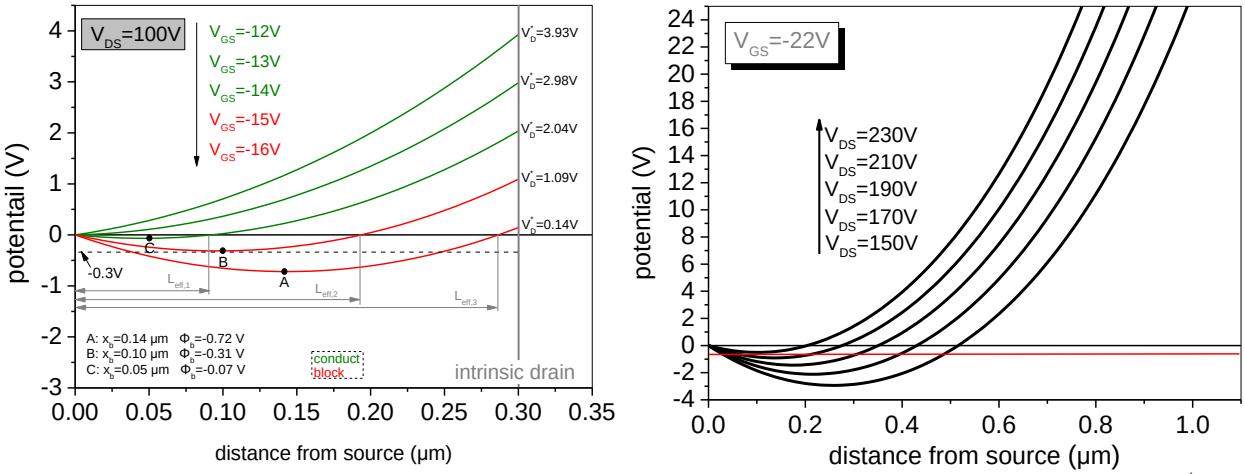


Fig. 2.7: Potential distribution (Bulucea-Rusu analytical model with use of Spirito equation for connecting V_D^* with V_{DS}) at different V_{GS} values and constant V_{DS} (left); at different V_{DS} values and constant V_{GS} (right).

Taking into account built-in potentials [36]:

$$\Phi_b = \eta \left[\left(V_G + V_{pn} \right) + \frac{1}{\mu} \left(V_D + V_{Drnn} \right) \right] + V_{Snn}$$

V_{Snn} is the built in potential Source-Drain, V_{pn}, V_{Drnn} are the gate-source and drain-source/channel build-in potentials:

$$V_{pn} = \frac{kT}{q} \ln \frac{N_{Ch} N_G}{n_i^2} \qquad (2)$$

$$V_{Snn} = \frac{kT}{q} \ln \frac{N_S}{N_{Ch}} \qquad (3)$$

$$V_{Drnn} = \frac{kT}{q} \ln \frac{N_{Ch}}{N_{Dr}}$$

The above analysis holds for the current in the middle of the channel. In actual case, the major part of current flows in the middle of the channel, where the barrier height is the lowest, but with increasing transistor current, part of this current flows on the channel side where the barrier height is larger. One can conclude that because of this current spreading effect, at higher currents, the

effective barrier height is slightly increasing with current. Below the relation for the effective current-transport area is presented.

$$A_{eff} = Z \cdot W_{eff} = ZW \frac{\sqrt{\pi}}{2} \sqrt{\frac{kT}{q\left(V_{bi} + V_G - \Phi_b\right)}} erf\left(\sqrt{\frac{q\left(V_{bi} + V_G - \Phi_b\right)}{kT}}\right) \qquad (4)$$

where W_{eff} is the effective channel width.

Thus we conclude that the drain current is given by the relation:

$$I_D = \frac{A_{eff} q D_n N_{chan}}{L_{eff} / 2} \sqrt{\frac{q\Phi_b}{\pi kT}} e^{-\left(q\Phi_b / kT\right)} \qquad (5)$$

According to Plotka and Wilamowski [35], a two dimensional analysis is required in order to determine Φ_b, L_{eff}, n and μ. The following presented analysis can be used towards this purpose.

Bulucea-Rusu model

Bulucea and Rusu [39] proposed an analytical description for the forward blocking operation. For the purpose of blocking state/low current operation modeling, the device has been divided into an intrinsic region and an extrinsic one; the boundary between the two is biased by a cosine potential along the gate-to-gate direction, the maximum value of which is set by a virtual intrinsic drain electrode (V^*_{DS} in Fig. 2.8). The intrinsic drain is a virtual point and the potential there is a linear combination of the drain-source and gate-source voltages after punchthrough. The other boundary conditions are zero voltage at the source, constant voltage along the top and bottom sides of the domain (gate-channel junctions/AB & A'B' in Fig. 2.8) and a constant voltage at the point opposite to the source, called the intrinsic drain.

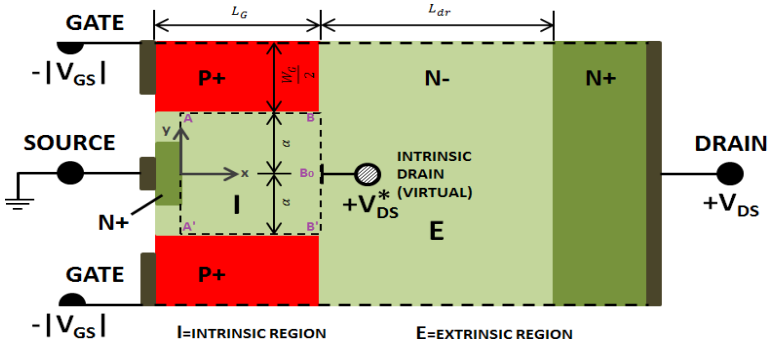


Fig. 2.8: Bulucea-Rusu configuration. Channel divided into an intrinsic region (ABB'A rectangle) and an extrinsic one (remaining). A virtual drain, (V^*_{DS}) is considered applied in B_0 while the potential along BB_0B' line is given a cosine variation from V^*_{DS} to V_G. Reprinted from [39].

The extracted potential function from the solution of the Poisson equations is given below:

$$\Phi_G = -\left|V_{GS}\right| - V_{bi} - V_{Snn} + V_P = -\left|V_{GS}\right| - V_{TH} - V_{Snn} = -\left|V_{GS}\right| - V_{TH} - \frac{kT}{q}\left[\ln\left(\frac{N_S}{N_{Ch}}\right)\right] \qquad (6)$$

where V_P pinch-off potential, V_{bi} built-in channel-gate potential, $V_{TH}=V_{bi}-V_P$ threshold voltage,

$$V_A = \frac{\mu_0}{\left(\mu_0 + 1\right)}\left[-\Phi_G - \frac{V^*_{DS}}{\left(\mu_0 - 1\right)}\right] \qquad (7)$$

$$V_B = \frac{\mu_0}{\left(\mu_0^2 - 1\right)}\left[V_{DS}^* - \frac{\left(\mu_0 - 1\right)}{\mu_0}\Phi_G\right] \quad (8)$$

$$\mu_0 = \exp\left(\frac{\pi L_G}{2a}\right) > 1 \qquad (9)$$

The factor μ_0 (*intrinsic electrostatic voltage gain)*, characterizes the relative importance of the drain with respect to the gate in controlling the electrostatic potential in the channel.

Since $\Phi(x, y)$ is symmetrical in y, its extremum Φ_b occurs along x axis and is obtained by:

$$x_b = \frac{a}{\pi}\ln\left(\frac{V_A}{V_B}\right) \qquad (10)$$

The extracted equation for the barrier potential Φ_b is:

$$\Phi_b = \Phi_G + 2\sqrt{\frac{\mu_0^2}{\left(\mu_0^2 - 1\right)\left(\mu_0 + 1\right)}\left[-\Phi_G - \frac{V_D^*}{\left(\mu_0 - 1\right)}\right]\left[V_D^* - \frac{\left(\mu_0 - 1\right)}{\mu_0}\Phi_G\right]} \qquad (11)$$

The model is mainly oriented to the analytical calculation of the barrier height Φ_b and does not propose anything concerning transfer current mechanism and therefore any analytical expression for the saturation current I_0. Furthermore, the barrier height Φ_b is calculated as a function of the virtual-intrinsic-drain-electrode potential (V^*_{DS}). In order to calculate Φ_b from the terminal properties of the device, the dependence of V^*_{DS} on V_{DS} and V_{GS} has to be known.

Nevertheless, the calculated barrier height can be employed with other models proposing a relation between the intrinsic drain voltage and the applied one, in order to calculate the current. Such a model is presented below.

Spirito model

A more analytical approach (since it gives a relation connecting the potential at the intrinsic drain with that at the output terminals) was developed in [40]. In this model, the gate regions are assumed to be cylindrical in shape as happens with planar diffusion, but with an uniform doping concentration and abrupt junction profile, to simplify the modeling (Fig. 2.9).

Because the current is always confined in a region much narrower than the channel, the I-V curves can be obtained from knowledge of the potential distribution in the rectangular region sketched in Fig. 2.9 (right).

The potential at intrinsic drain, V_{D*}, is calculated by considering that the potential distribution in the area between the gate and the drain i.e for x in the range of L_G to L_G+L_{dr} is unaffected by two-dimensional effects. Therefore, it is sufficient to calculate the potential along the lateral boundary. This is performed by resolving the Poisson equation and by assuming that (1) the drift layer is depleted completely (punchthrough condition) and (2) the potential distribution is unaffected by two-dimensional effects along the boundary $x, y=a+W_G/2$), which is reasonable for $W_G/2 >> 2R=2L_G$:

An additional assumption, is that the equipotential passing through the intrinsic drain is at distance S=T/2 below the gate (see Fig. 2.9-right). From geometrical considerations:

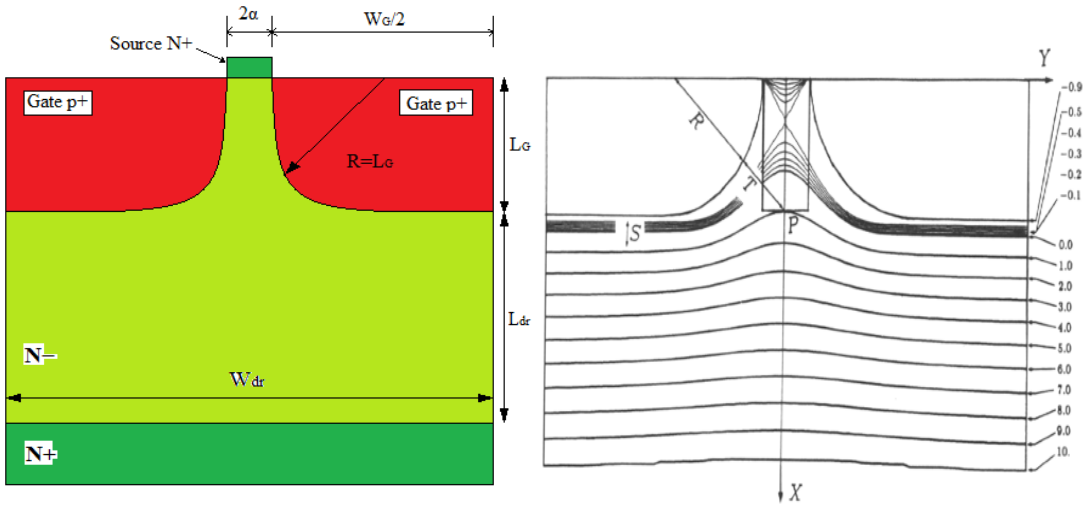


Fig. 2.9: Spirito's configuration (left). On the right, point P is the "intrinsic drain" D introduced by Bulucea & Rusu. Reprinted from [40]. Note that in this specific geometry, R corresponds to L_{Ch}, not L_G of our analysis.*

$$S = \frac{T}{2} = \frac{\sqrt{(R+a)^2 + R^2} - R}{2} = \frac{\sqrt{(L_G + a)^2 + L_G{}^2} - L_G}{2} \quad (12)$$

Therefore,

$$V_{D^*} = U(L_G + S) = -\frac{qN_{drift}}{2\varepsilon} S^2 + \left[\frac{V_{DS} - V_{GS} + V_{bi}^{'}}{L_{Dr}} + \frac{qN_{drift}}{2\varepsilon} L_{Dr} \right] S + V_{GS} - V_{bi}^{'} \qquad (13)$$

where, $V'_{bi}=V_{pn}+V_{Snn}$ (14)

By using the equation (13) which correlates V_D^* with V_{DS}, we calculate V_D^*, so the barrier height Φ_b and the abscissa x_b of the potential minimum (saddle point) can be determined. Then, the current at the exponential regime (low current part of the I-V characteristic) is calculated by employing equation (5).

Thus, an approach was presented using the Bulucea-Rusu model whilst the Spirito's equation is used for connecting V_D^* with V_{DS} for calculating the barrier height (value and position). The calculation can be performed utilizing the equations (1)-(14).

Maximum breakdown gate voltage of a VJFET

The largest drain voltage that can be supported by the JFET structure before the onset of significant current flow is determined by several factors. Firstly, it is limited by the intrinsic blocking voltage capability of the drift region as determined by the doping concentration and thickness. The blocking voltage can be obtained by using the graphs and equations provided previously. Secondly, the maximum drain voltage that can be supported without significant current flow can be limited by the applied gate bias and the blocking gain of the structure. In addition, the largest gate bias that can be applied is limited by the onset of breakdown between the gate and the source regions. The breakdown voltage between the gate and the source regions is determined by the depletion layer punch-through from the gate junction to the highly doped n^+ source region. A rough approximation is to consider that the electric field between the gate and source regions is uniform. Then, the gate-source diode breakdown can be calculated by using the following formula:

$$BV_{GS} = (L_P - L_{Cont}).E_C - V_{bi}$$

where E_C is the breakdown field. For the purposes of our estimation we used E_C =3.25MV/cm whatever the doping.

2.2.3 Capacitance model

In order to model dynamic performance of SiC JFET, usually three nonlinear capacitors are introduced to model gate-source capacitance, gate-drain capacitance and drain-source capacitance.

In a first approximation the capacitance between gate and source as well as between gate and drain are expressed by:

$$C_{GS} = \frac{\varepsilon A_{GS}}{W_s} = \frac{\varepsilon\left[2\left(L_G + L_A\right)Z\right]}{\sqrt{\frac{2\varepsilon}{qN_{chan}}\left(-V_{GS} + V_{bi}\right)}}$$

$$C_{GD} = \frac{\varepsilon A_{GD}}{L_A} = \frac{\varepsilon\left(W_B Z\right)}{\sqrt{\frac{2\varepsilon}{qN_{dr}}\left(V_A - V_{GS} + V_{bi}\right)}}$$

No formula is given for the drain-source capacitance since it can be considered negligible compared with gate-source and gate-drain capacitances. Indeed, C–V measurements have showed that C_{DS} has a value approximately 200 times less than the other device capacitances.

Chapter 3. Design and fabrication process of investigated samples

In this chapter, information is given about the structure, the design and the dimensions of the devices involved in the processed samples, as well as the fabrication procedure that was followed. Moreover in order to check the quality of the wafer itself in terms of existence of defects and micropipes, before starting any processing procedure on it, it was checked and the results are presented just below.

3.1 Quality of SiC wafer

Any commercial wafer is characterized from the major (at the bottom) and the minor (on the left) flat. In the graph below we can see on the left the schematic of our wafer and on the right a wafer photo before any process. The specific locations where defects where detected are marked, while the photos taken from them are presented subsequently.

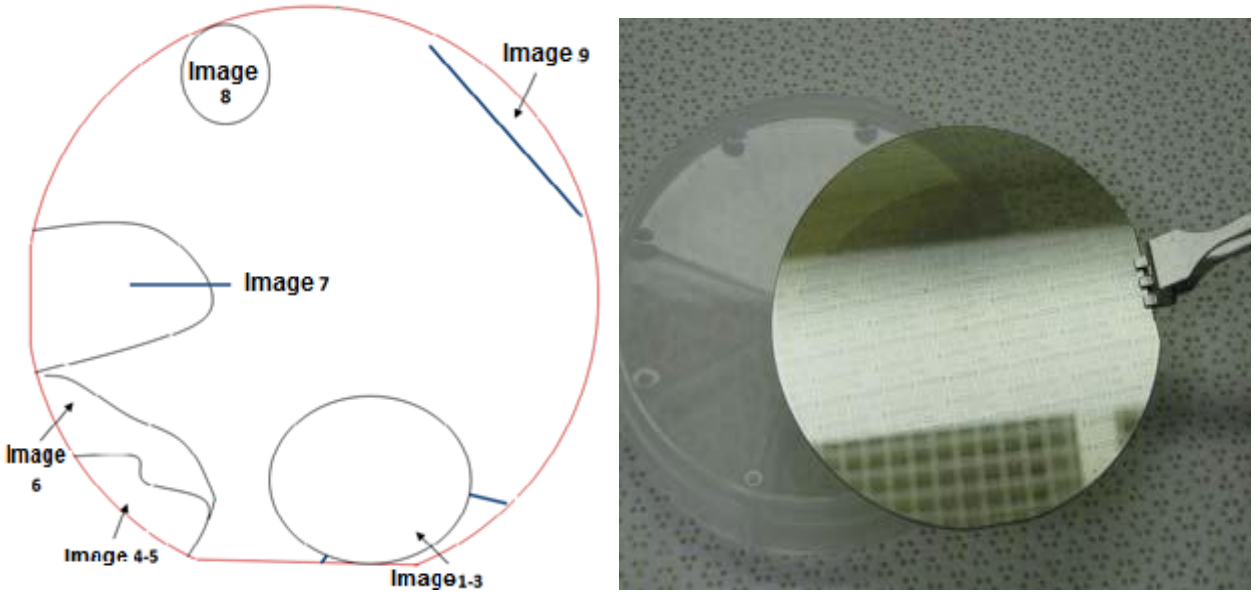


Fig. 3.1: Left: Schematic of processed wafer, Right: Initial wafer photo.

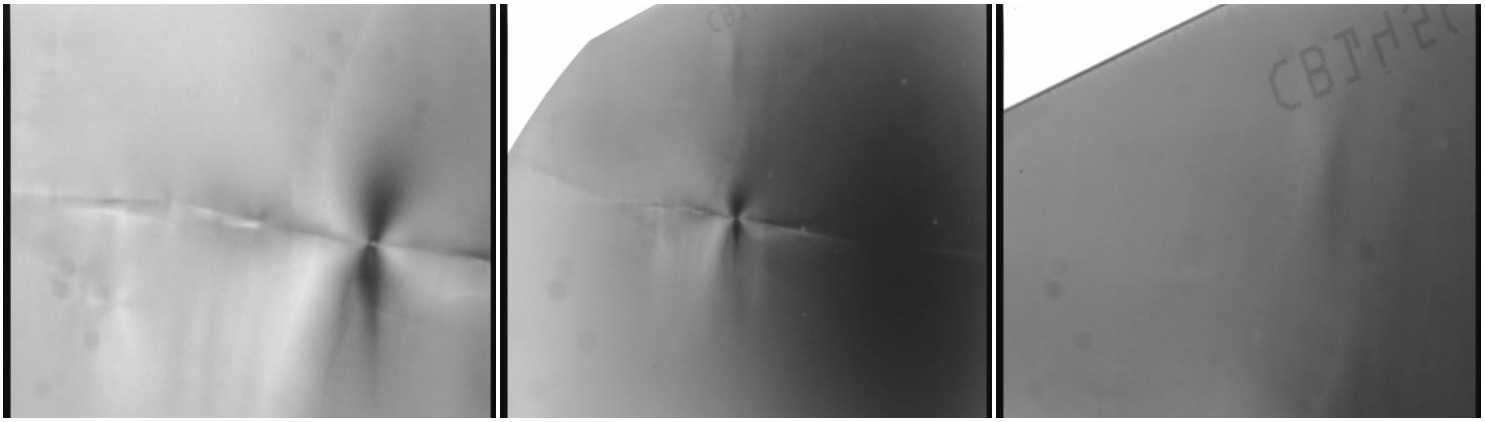


Image1: Dislocation walls and micropipes

Image 2: Micropipe

Image 3: Low angle grain boundaries

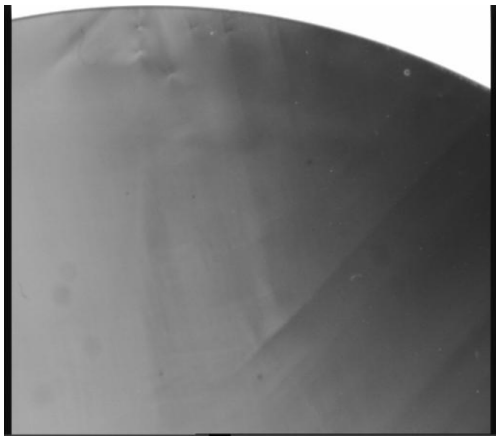


Image 4: Triangular shape formed stressed area.

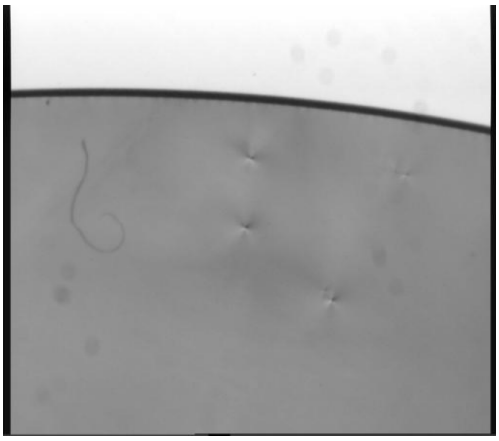


Image 5: Micropipes

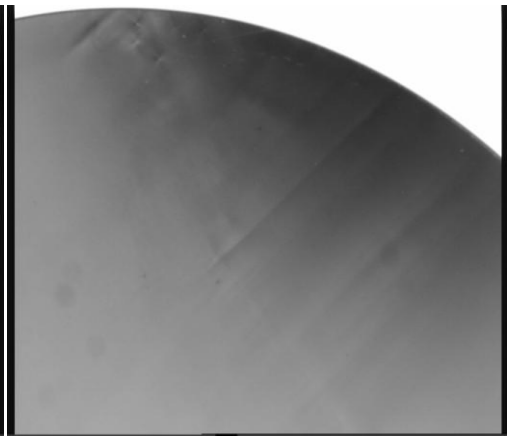


Image 6: Stressed area

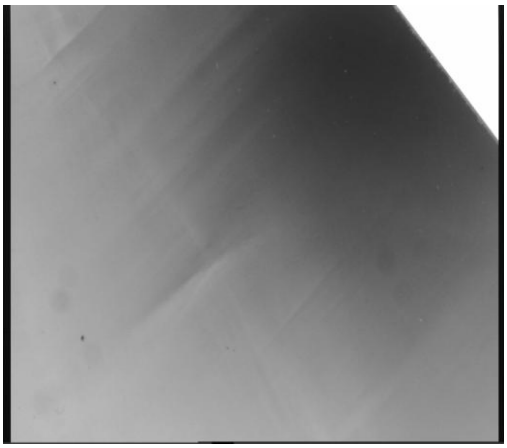


Image 7

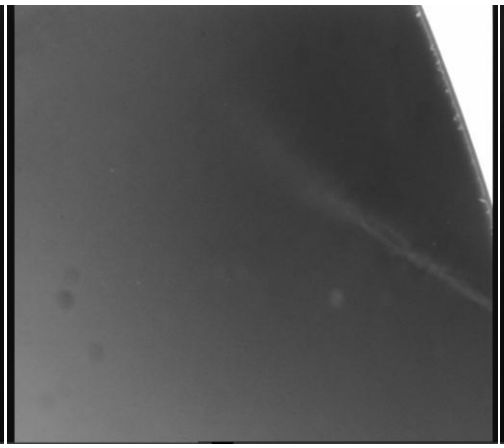


Image 8

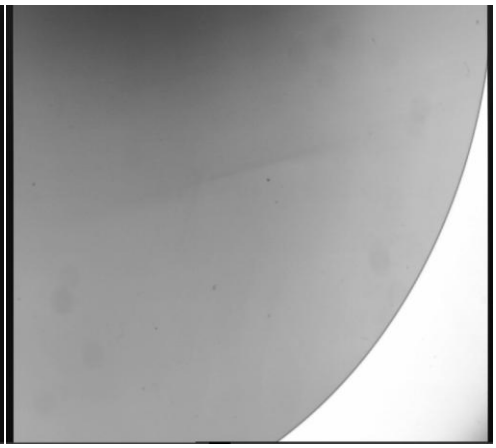


Image 9

The photos have been taken by the cross polarizer imaging technique. The cross-polarizer imaging (also known in literature as “birefringence imaging” or “x-pol imaging”) is commonly used to observe strain and imperfections of semitransparent birefringent materials and glasses. In particular it was used to observe the presence of grain boundaries and others macroscopic defects.

We observe that all the detected defects are placed in the edges of the sample. Since we know that the non-operational or bad devices are either in defective areas of the wafer or are defectively produced, the information about the quality of the wafer is very crucial. Thus, it is very important to check the placement of the processed piece on the wafer before starting the electrical characterization.

3.2 Dimensions and geometries

The self-aligned approach was more suitable for fabricating the targeted transistor with the available at FORTH technology and equipment. A set of masks based on this self-aligned approach has been designed and Fig. 3.2 shows this mask set.

The devices have 256 μm long source mesa-structures with widths of 5/4/3/2.5/2/1.5 μm separated by 4 μm wide gate trenches. Table 3.1 contains all necessary information about the dimensions and dopings that are common for both fabricated samples. The dimensions that are different for each sample are reported thereinafter in the individual characterization reports of the samples.

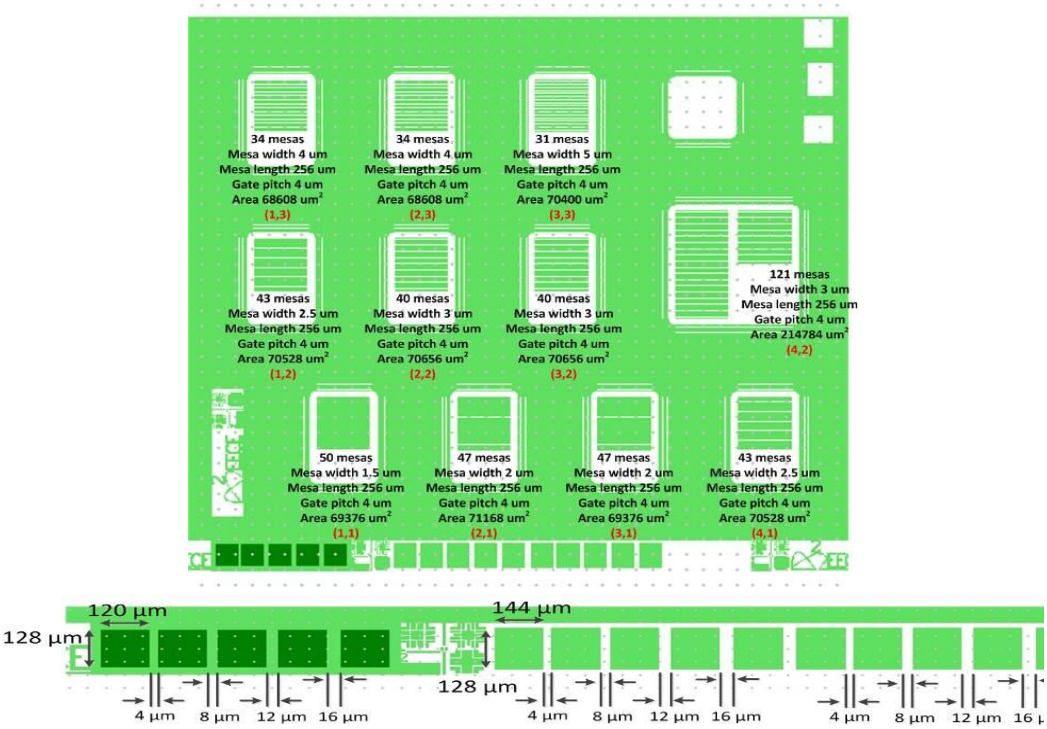


Fig. 3.2: Mask layout of one period. 11 transistors of different dimensions are involved in each period. The square on the top right corner is a diode. TLM patterns for both n-type and p-type contacts are included and are visible at the bottom of the figure.

Both n-type and p-type contact TLMs contain 5 square pads each, with 128µm square side size and distance between the pads: 4, 8, 12, 16 sµm. The two sets per period of TLM pads for the n-type contact are positioned side by side.

ρ_{sub} (Ω•cm)	L_{sub} (µm)	N_D (cm^{-3}) drift	N_A (cm^{-3}) gate	N_D (cm^{-3}) channel layer	Gate width W_g (µm)	Channel width W=2a(µm)	N_D (cm^{-3}) pillar/cont	N_{fing}
0.021	372	5.00E+15	1.00E+19	5.00E+15	4	1.5/2/2.5/3/ 4/5	1.00E+19	50/47/43/ 40/ 34/31
$R_{cont.}$ ($\Omega \cdot cm^2$)	W_{GR} (µm)	W_1 (µm)	W_2 (µm)	W_3 (µm)	W_4 (µm)	W_5 (µm)	W_6 (µm)	W_{bus} (µm)
0.0001	4	2.5	2.5	3	3.5	4	5.5	14

Table 3.1: Important values in dimensions and doping profiles.

3.3 Fabrication of the transistors

3.3.1 Transistor sample structure

A 4-inch 4H-SiC wafer (Code number: CB145602) has been used for the epitaxial growth of the JFET structure performed by ETC company (Catania, Italy). Two different pieces of the wafer were selected for the fabrication of the two samples. Wafer specifications as well as details of the epitaxial structure are given below while a cross section of the wafer in presented beside in figure 3.3.

Substrate:
Orientation: <0001>
Off-Orientation: 4° towards <11-20>
Dopant: Nitrogen
Resistivity (ohm·cm): 0.021
Diameter (mm.): min. 100
Thickness (μm): 372 +/- 0.5
MPD (cm^{-2}): <5

Epilayer I (buffer layer):
Thickness (μm) : 1
Dopant: Nitrogen
Carrier Density($1/cm^3$): $1 \cdot 10^{18}$ (SIMS)

Epilayer II
Thickness (μm) : 8
Dopant: Nitrogen
Carrier Density(cm^{-3}): $5 \cdot 10^{15}$ (SIMS)

Epilayer III
Thickness (μm) : 1.2
Dopant: Nitrogen
Carrier Density(cm^{-3}): $1 \cdot 10^{16}$ (SIMS)

Epilayer IV
Thickness (μm) : 1
Dopant: Nitrogen
Carrier Density(cm^{-3}): $1 \cdot 10^{19}$ (SIMS)

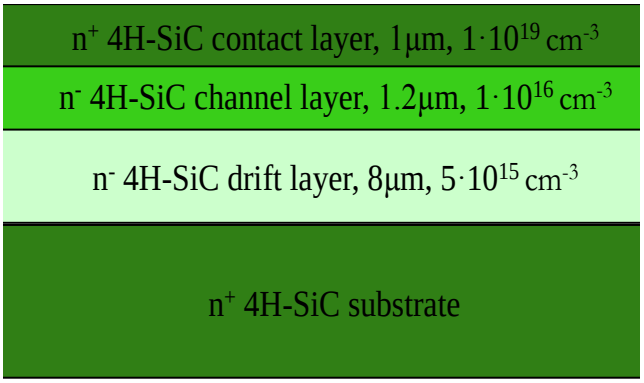


Fig. 3.3: Cross section of the initial 4H-SiC wafer.

3.3.2 Transistor fabrication

Source fingers formation – ***MASK #1***

Since the combined etching of TEOS and SiC with the same RIE conditions results very often to micromasking, it was decided to not deposit a TEOS oxide as an etching and implantation mask. In this case a thick metallization has to serve as mask for both the RIE and the gate implantation. Since the use of thick Ni resulted in adherence problems, a multilayer metal scheme has been employed Cr / Ni / Al / Ni (7nm / 80nm / 400nm / 40nm). Fig. 3.4 shows the morphology after the RIE process and the source pillars formation.

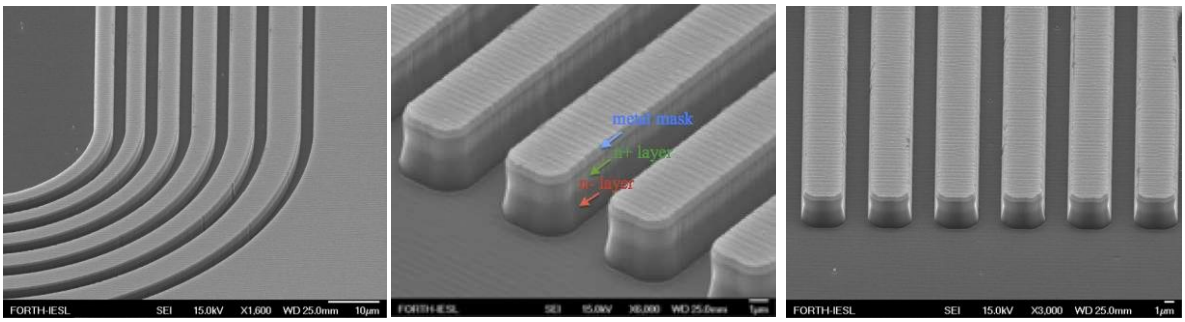
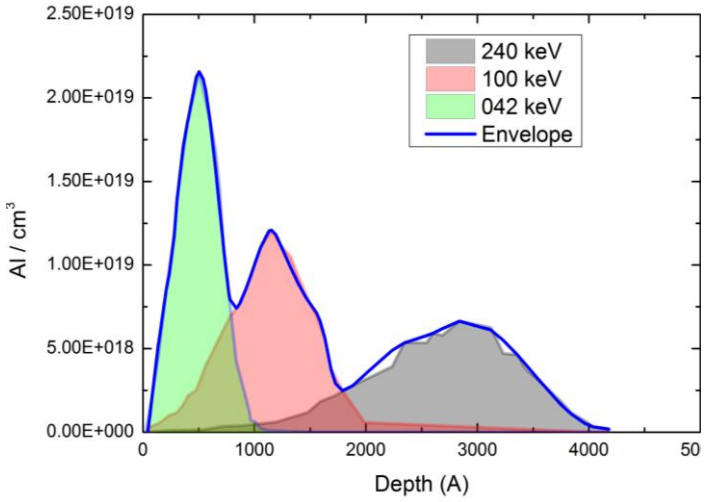


Fig. 3.4: SEM images taken after one month of source finger mesa formation.
Note the contrast difference between different conductivity areas.

Implantation of p^+ gate layer

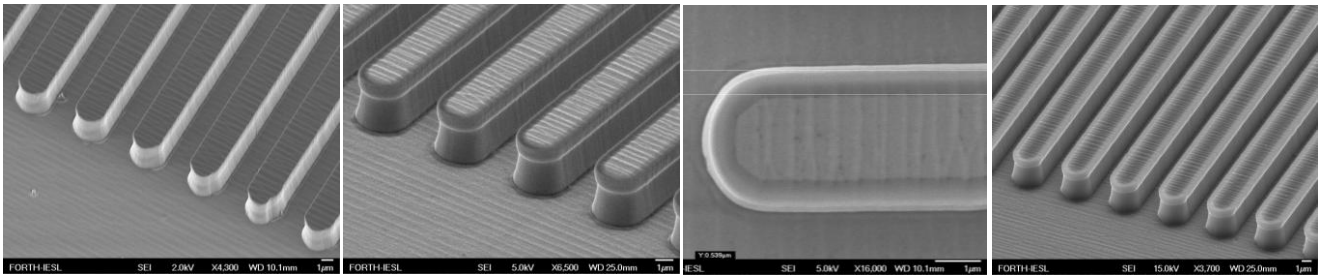
The same mask was used to form gate regions by ion implantation. Aluminium was implanted at temperature of 425 °C with normally incident ion beam. Individual implantation energies and fluencies were calculated using the SR IM 2D simulation program to form the Al profile shown in Fig. 3.5. So, the top contact p^{++} layer is anticipated to have a thickness of 80 nm while the p layer for the gate junction a thickness of less than 300 nm.

Implantation has been performed in Norway, by the group of Prof. Svensson while the subsequent steps for post-implantation annealing (metal mask removal, graphite capping layer formation and annealing at 1600 °C, graphite removal) have been performed at ACREO.



Energy (keV)	Flux (cm^{-2})
240	$1 \cdot 10^{14}$
100	$2 \cdot 10^{14}$
42	$3 \cdot 10^{14}$
Total dose	$6 \cdot 10^{14}$

Fig.3.5: Gate implantation. SRIM calculated Al distribution (Left) according to implantation conditions. (*right*).



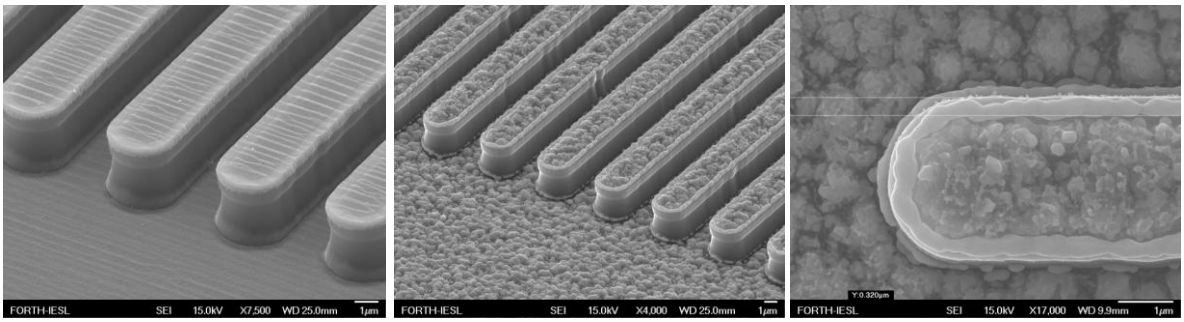
(a) (b) (c) (d)

Fig. 3.6: SEM images taken after implantation and post-implantation annealing (a), after dry oxidation (b)-(c), after horizontal oxide removal (d).

Sideskirt oxidation and horizontal oxide removal

Then, the samples were oxidized for 3 hours in wet oxygen at 1150 °C. This resulted in the formation of a 60 nm thick oxide on the Si-face and around 500 nm thick oxide on mesa-structure sidewalls (Fig. 3.6 (c)). The thick oxide film grown on the sidewalls consumes unintentionally Al-doped source-finger-sidewalls and prevents formation of a leaky gate-source p^+-n^+ SiC junction. The higher oxidation rate of the n+ layer is obvious in SEM photos (Figs. 3.6 (b), 3.7 (a). The grown oxide layer was removed from the top surfaces of mesa-structures and from the trench bottoms by anisotropic RIE (Fig. 3.6 (d)).

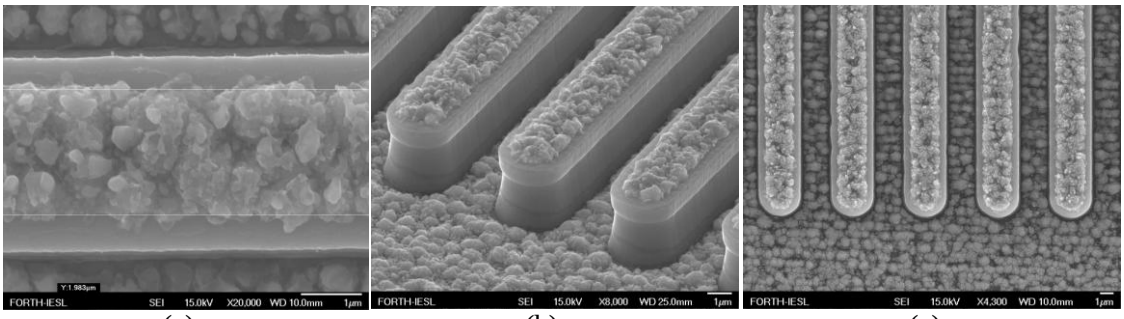
Ni self-aligned deposition, partial annealing & removal from sideskirt oxide top – ***MASK#2***



(a) (b) (c)

Fig. 3.7: SEM images taken after blanket Ni deposition (a) and after partial 750ºC RTA annealing (b)-(c).

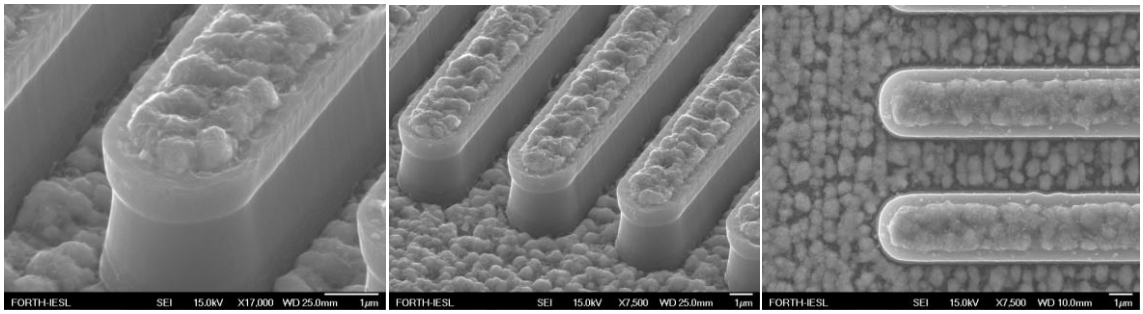
The second mask is used in this step to allow metal deposition in source-fingers and gate pad areas excluding guard rings and the area between the devices. 7 nm thick chromium adhesion layer and 200 nm thick Ni contact were deposited by e-beam evaporation and annealed at 750ºC. Note that the metallization does not cover completely the gate bus leaving a safe distance of 14 μm from the first guard ring. This intermediate annealing is needed in order to form a Ni-based alloy on top of the SiC source and unreacted Ni on top of the sideskirt oxide. As it can be seen in Fig. 3.7 (b)-(c), the Ni on top of the sideskirt oxide is not reacting with the substrate at this internediate temperature, allowing the removal of the Ni metallization on top of the sideskirt oxide but not on top of the SiC source finger. This is performed by using SPM etching [H_2SO_4:H_2O_2:H_2O in 4:1:60] etching unreacted Ni.



(a) (b) (c)

Fig. 3.8: SEM images taken after Ni-based alloy removal from the top of sideskirt oxides.

Ni-deposition on backside and RTA at 1000ºC



(a) (b) (c)

Fig. 3.9: SEM images taken after RTA at 1000ºC.

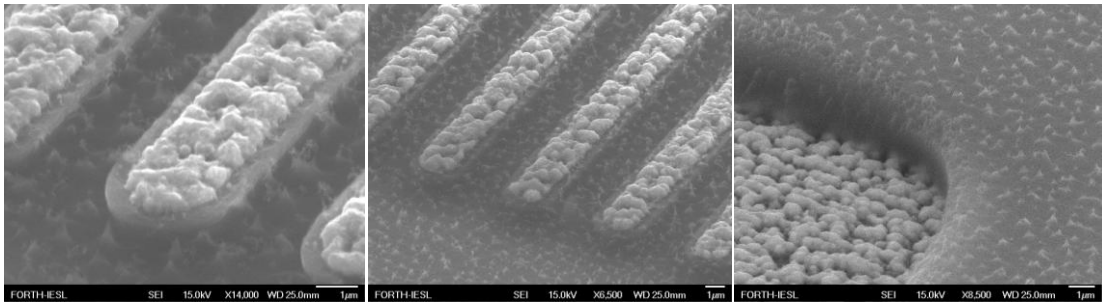
Then, a chromium (7 nm thick) and nickel (300 nm thick) blanket deposition on the back face has been performed to form the drain metallization. Following an RTA at 1000ºC in vacuum has been performed to form the ohmic alloy on both sides of the wafer.

BCB spinning and etch-back – ***MASK#3***

A BCB film has been deposited all over the surface in 3 consecutive spins resulting in a total BCB thickness of 9μm. Then, the BCB has been etched-back down to the source finger tops with pure SF_6 RIE (200W, 140mTorr, 100V DC).

Fig. 3.10 shows typical morphology of source fingers after the etch-back of the deposited BCB, which exposes the tops of source fingers to subsequent interconnect metal deposition.

Once the etch back by RIE is on the source-finger-top then, a new lithography is done in order to define the gate pad area and remove all the BCB from its top. This removal is done again with RIE. The mask used in this case is photoresist 7μm, which is enough to protect the remaining surface from the BCB removal.



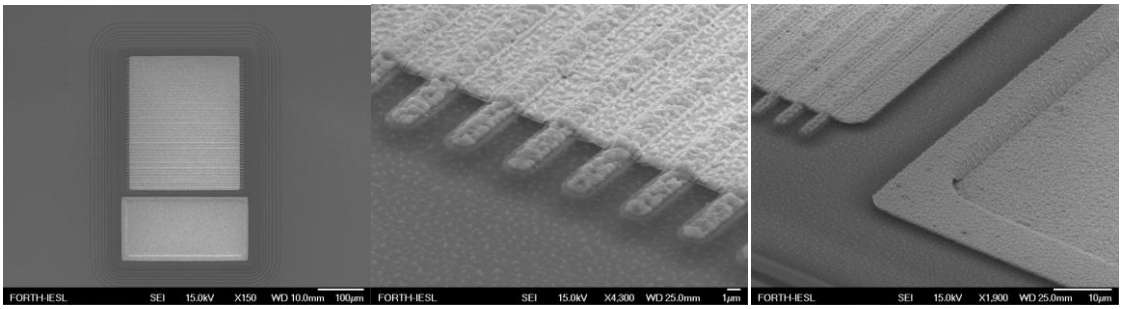
(a) (b) (c)

Fig. 3.10: SEM images taken after BCB deposition and etch-back from the source fingers (a-b) and after 2nd etch-back on the gate pad (c).

After source interconnect and gate overlay metallization - ***MASK#4***

The last lithography step (mask#4) allows the deposition of the overlay metallization on the source fingers and the gate bus pad but not the gate bus. The overlay metallization is composed by Cr(7nm)/Ni (100nm)/Au (350nm) and it is deposited by e-beam evaporation.

Fig. 3.11 shows SEM images after completion of the whole process i.e. after source interconnect deposition.



(a) (b) (c)

Fig. 3.11: SEM images taken after source interconnect and gate overlay.

Chapter 4. JFET Electrical characterization procedure- Measurement results from sample CB145602-P1

The electrical characterization involves two main fields, the static characteristics and the switching ones. The static characterization is also divided in the DC and AC characteristics. It is obvious that from the on wafer state only the static characterization is feasible while the switching can be performed once the device under test is packaged. In this chapter the measurements procedure that must be followed for the accomplishment of the on wafer static electrical characterization of a sample is described.

The goal of the electrical characterization is to extract all the parameters which are necessary to fill a specifications table summarizing briefly and concisely the important characteristics of the device. Towards this, all the different measurements that must be performed as well as the consequent necessary analysis for the parameter extraction are described. Simultaneously, the measurements results from the first fabricated sample, the CB145602-P1 are presented. In this way, the direct application of the described setups and configurations to the sample will make them more comprehensible to the reader.

This sample was the first effort for the fabrication of the desired VJFETs. Prior to this, a previous effort has been done with the fabrication of a sample (cut in 6 small dies) using the same mask as the ones presented in this work but different layout, namely different structural dimensions. This initial sample was also investigated and characterized in the early start of our work, with the evaluated results giving us important information and directions for the next efforts.

It must be mentioned that all the graphs presented from now on in our work were extracted using the OriginLab 9 software.

4.1 Transistor geometry determination.

Firstly, a recognition of the device geometry and dimensions has to be done, as well as a check of the processed piece placement of the initial wafer.

In figure 4.1 we see the placement of the processed piece on the initial 4H-SiC wafer slice. By observing again the figure 3.1 we can see that some defects were detected in that region. In this way, possible malfunctions and bad behavior of the devices can be in some extent, attributed rather to the material than the processing procedure.

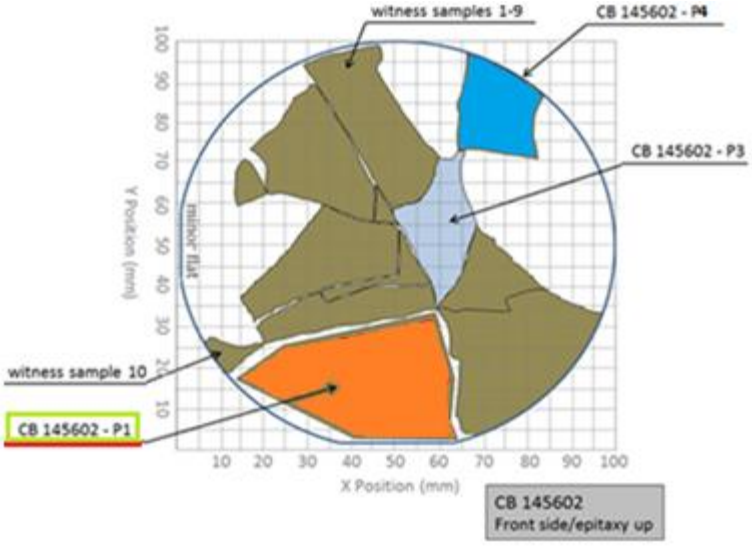


Fig. 4.1: Placement of the CB145602-P1 on the 4-inch 4H-SiC wafer slice.

For our sample, below in figure 4.2 we can see one period of the utilized mask and the code numbering of the devices and the periods. The sample consists of 75 periods. Each period involves 11

transistors, one diode and TLM patterns. The diode is designed in the mask because of its simple structure which will help us to figure out more easily any possible processing errors or malfunctions. For all the devices, except of F42, we observe that although the mesa width is elevating, the total area is approximately constant at around 7E+4um^2. This is achieved by decreasing accordingly the number of fingers (mesas). The exception F42 has more than three times greater area than the others due to the more fingers that features. Moreover the gate pitch is constant at 4um for all.

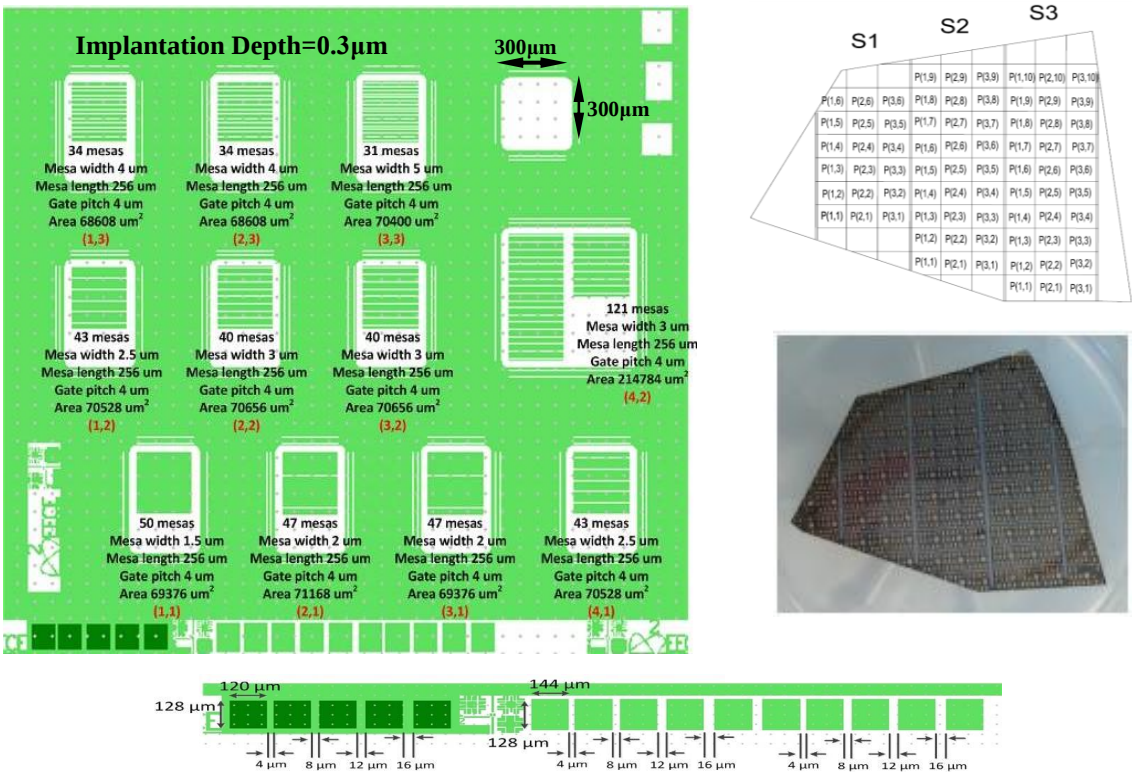


Fig. 4.2: Top left. Period of the mask. Code numbering of the devices in each period is shown. Top right. Schematic of processed sample and corresponding mask period code numbering and photo of the processed piece. Bottom. TLM patterns for both n-type (on the left) and p-type contacts (the two on the right).

A table with all important values in dimensions and doping of different parts of the device should be filled. Prior to this, SEM photos taken during the processing must be checked in order to figure out if the actual dimensions agree with the corresponding ones of the lithography mask.

Table with input values for various parts of the VJFET

ρ_{sub} (Ω•cm)	L_{sub} (µm)	L_{buf} (µm)	N_D (cm^{-3}) buffer	L_{drift} (µm)	N_D (cm^{-3}) drift	L_{chan} (µm)	$L_{pill/ch}$ (µm)
0.021	372	1	1E+18	7.4	5E+15	1.1	1.2
$L_{pill/ch2}$ (µm)	N_D (cm^{-3}) pillar/chan.	$L_{pill/con}$ (µm)	N_D (cm^{-3}) pillar/cont	Gate length L_G (µm)	N_A (cm^{-3}) gate	N_D(cm^{-3}) channel	Gate pitch W_G (µm)
0.3	1.E+16	1	1E+19	0.3	1E+19	5E+15	3
Channel width W=2a(µm)	N_{fing}		$R_{cont.}$ (Ω•cm^2)	Pillar width W_{pil} (µm)	L_{pillar}	Z (µm)	W_{GR} (µm)
2.5/3/3.5/4/5/6	50/47/43/40/34/31		0.0001	W-1	2.5µm	256	3
W_{bus} (µm)	W_1 (µm)	W_2 (µm)	W_3 (µm)	W_4 (µm)	W_5 (µm)	W_6 µm)	
13.5	3.5	3.5	4	4.5	5	6.5	

* * **L_{chan}=1.1um** (gate length/implantation depth (0.3um)+V_{bi} depletion width (0.8um))

For our sample such a table is presented above. From the SEM photos, we noted that the actual channel widths are augmented by approximately 1μm, namely the F(1,1) transistor seems to have in reality W=2.5μm, not 1.5μm. Moreover the real width of the gate pitch is W_G=3μm, not 4μm. The fact that the available SEM photos were few, does not allow us to conclude firmly to the device dimensions.

Below in figure 4.3 we see some cross section schematics helping in understanding the structure of the fabricated devices. The etching for the formation of the trenches has stop to 2.5um depth, something that led to the existence of three different doping regions in the pillar. $L_{pill/cont.}$ (1E+19), $L_{pill/ch}$ (1E+16), $L_{pill/ch2}$ (5E+15).

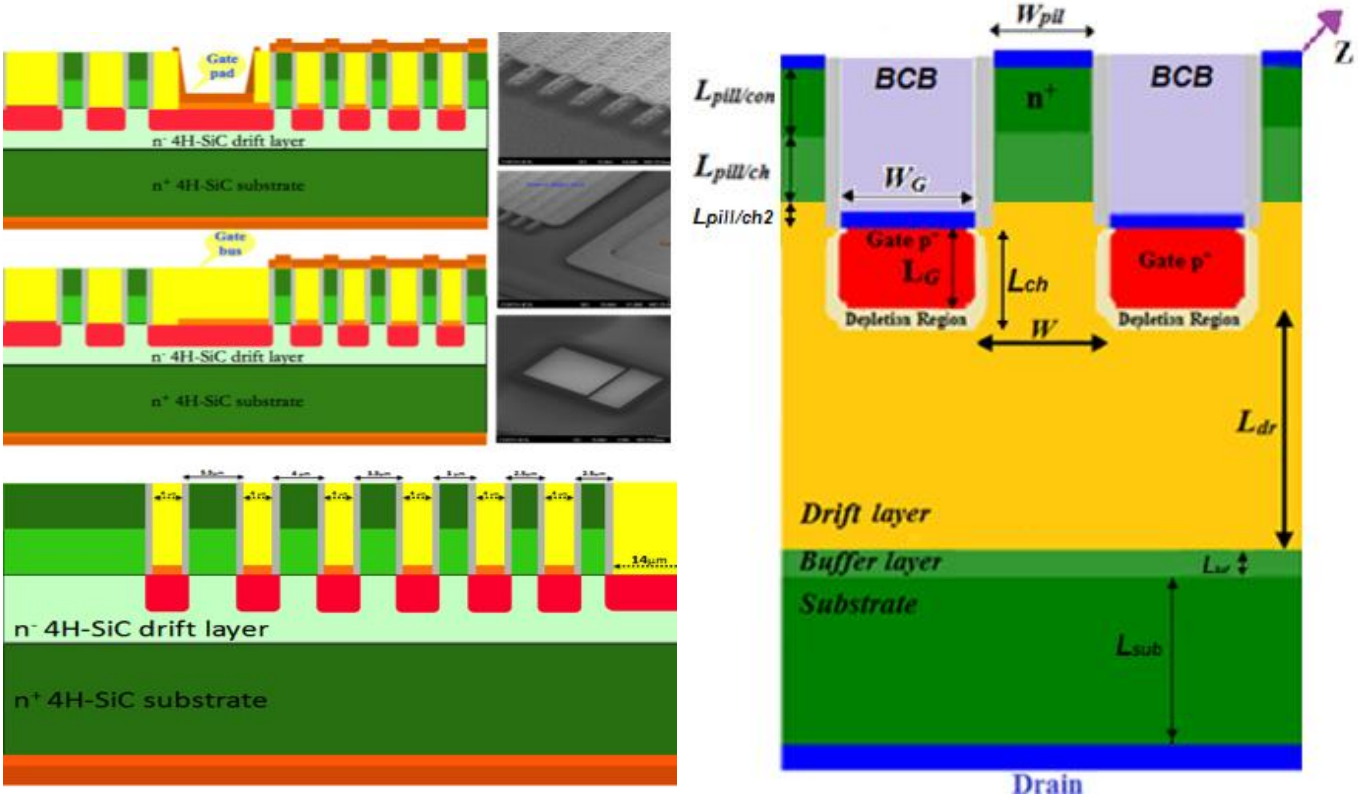


Fig. 4.3: Left: Schematic cross-sections of the complete device CB145602-P1 and corresponding SEM photos (Top). In the bottom the Guard rings and their corresponding dimensions are shown. Right: important dimension parameters

- L_{dr}=7.4 (8-0.3-0.3)μm,
- L_{chan}=1.1μm (gate length (0.3)+V_{bi} depletion width (0.8))
- L_p=2.5μm (1+1.2+0.3)

The *active area of each device* should be determined. This is the total area of multifinger sources and gates as it is assumed that the current spreads in the area below the gates too.

The *active perimeter of each device* should be determined. This is the total source length and in the case of multifinger geometry, the length of each source finger should be added.

The *Effective Source Area* should be also determined. It equals to the number of fingers times the mesa length times the mesa width.

For our sample the following table gathers the values of these parameters. The active area of all devices except F42 is $7 \cdot 10^{-4}$ cm^2 while for the F42 is $2.1 \cdot 10^{-3}$ cm^2.

	F11	F21	F31	F41	F12	F22	F32	F13	F23	F33	F42
Device Active Perimeter (mm)	12.8	12.03	12.03	11.01	11.01	10.24	10.24	8.70	8.70	7.94	30.98
Effective Source Area (10^{-4} cm^2)	1.92	2.41	2.41	2.75	2.75	3.07	3.07	3.48	3.48	3.97	9.29

4.2 Theoretical values estimation of parameters

Calculations of the expected values of different parameters by using standard semiconductor theory must be performed. Below we see the theoretically expected parameters values of all the different transistors of the sample at RT (300K). Analytically, the on resistance (R_{ON}) (for V_G=0V and V_G=2V), the threshold voltage (V_{TH}), the breakdown GS voltage (BV_{GS}), and the sheet resistance of the contact and of the gate layer (R_{sh}) are calculated. Refer to Appendix 2 for the utilized equations.

Table of Parameters Theoretical Values

F	W_{sem} (*μm*)	W_G (*μm*)	Source Area (10^{-4} cm^2)	Active Area (10^{-4} cm^2)	V_G=0V		V_G=2V		V_{TH} (V)	R_{sh} (Ω/sq) [con. layer]	R_{sh} (Ω/sq) [G layer]	BV_{GS} @RT (V)
					(Ω)	(mΩ*cm^2)	(Ω)	(mΩ*cm^2)				
11	*2.5*		*1.92*	*6.94*	6.36	4.41	5.07	3.52	-4.32			
21	*3*		*2.41*	*7.12*	5.37	3.82	4.6	3.28	-7.54			
31	*3*		*2.41*	*6.94*	5.37	3.72	4.6	3.19	-7.54			
41	*3.5*		*2.75*	*7.05*	4.96	3.5	4.41	3.11	-11.35			
12	*3.5*		*2.75*	*7.05*	4.96	3.5	4.41	3.11	-11.35			
22	*4*	*3*	*3.07*	*7.07*	4.65	3.29	4.24	2.99	-15.74	*79.6*	*265*	*484.5*
32	*4*		*3.07*	*7.07*	4.65	3.29	4.24	2.99	-15.74			
13	*5*		*3.48*	*6.86*	4.42	3.03	4.13	2.83	-26.28			
23	*5*		*3.48*	*6.86*	4.42	3.03	4.13	2.83	-26.28			
33	*6*		*3.97*	*7.04*	4.08	2.87	3.87	2.73	-39.16			
42	*4*		9.29	*21.48*	1.54	3.3	1.4	3.01	-15.74			

Table of Resistance Theoretical Values (R)

mesαW (*μm*)	*#n*	$R_{cont.D}$ (Ω)	R_{sub} (Ω)	R_{buf} (Ω)	R_{drift} (Ω)	$R_{ch.}^{1}$ (Ω)	$R_{ch.}^{2}$ (Ω)	$R_{pil.}^{1}$ (Ω)	$R_{pil.}^{2}$ (Ω)	$R_{cont.S}$ (Ω)	R_{ON} (Ohm)
2.5	*50*	0.14	1.11	0.003	2.96	1.398	0.137	0.288	0.002	0.312	6.36
3	*47*	0.14	1.08	0.003	2.53	0.956	0.121	0.255	0.002	0.277	5.37
3.5	*43*	0.14	1.09	0.003	2.35	0.77	0.114	0.24	0.002	0.260	4.96
4	*40*	0.14	1.09	0.003	2.19	0.66	0.107	0.224	0.002	0.244	4.65
4	*121*	0.05	0.36	0.001	0.72	0.217	0.035	0.074	0.001	0.081	1.54
5	*34*	0.14	1.12	0.003	2.06	0.544	0.101	0.211	0.002	0.23	4.42
6	*31*	0.14	1.09	0.003	1.89	0.461	0.092	0.193	0.002	0.21	4.08

*For the contact resistances $R_{con,D}$ and $R_{cont,S}$ the common value of 10^{-4} Ohm·cm^2 has been used.

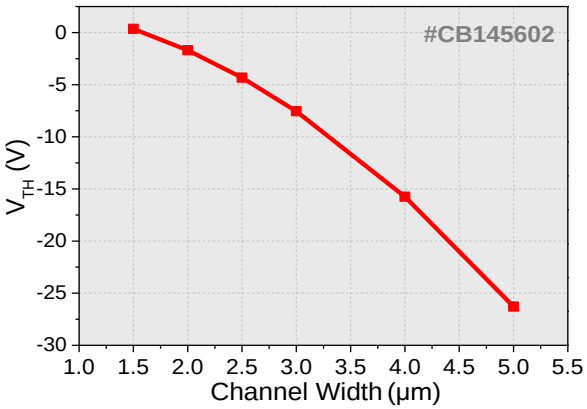


Fig. 4.4: V_{TH} in dependence on channel width.

In the table above, a detailed analysis of the R_{on} is presented. We can see all the individual resistance values which constitute the R_{on}, expressed in Ohms. The values are calculated for V_{GS}=0V. In the graph beside, we see the descending theoretical tense of the V_{TH} on the channel width.

Plan of measurements

The measurements have to follow the order given below.

The first measurements are done for all devices and test patterns of one mask period. The choice of the period to be measured, should be done by the process engineer in order to choose one with devices of best morphology and without process-related problems. The results of this step will allow drawing preliminary conclusions on the performance of fabricated devices and on the agreement to theoretical calculation.

Then, we proceed to the next I-V experiments. The statistics of the measurements is a basic aspect of the next experiments. The latter should be enough in number to make a statistics and mainly should be done in similar to the best-behaving devices of the first-measured-mask period. Nevertheless, in this selection it has to be taken into account that smaller devices and especially with small channel widths are expected to behave better. Useful parameters and the main conclusions for the fabrication process will be extracted from these measurements. Complementary graphs (histograms, mappings) can be drawn for the parameters.

From the aforementioned statistical study the best devices can be determined. The final series of measurements (pulsed, temperature-depended, high-voltage in dielectric media) are performed on these best devices. The latter allows checking the ultimate performance of the devices and determine values of parameters interesting for power electronics engineers (creation of specifications datasheet).

The majority of the measurements can be performed with a parameter analyzer which is a very versatile instrument. In some cases also an SMU or a curve tracer must be used. Of course for the capacitance measurements an LCR meter is necessary. For our measurements, presented from now on we used the following instrumentation: Keithley 4200-SCS (parameter analyzer), Keithley 2602A, Keithley 2651A (SMUs[2], measuring capability up to 10A and 50A respectively), Tektronix 370A (curve tracer), Agilent 4284A (LCR meter). The measurements were performed on an probe station manufactured by Alessi.

[2] SMU is a device that can source a voltage or current and measure itself without any extra connection. It simplifies connections to the DUT, reduces places where errors can enter the system.

Finally, special attention must be given to the contacting configuration. Four contact measurements (*Kelvin*) must be employed i.e. two probe-tips have to be used for every pad especially for low current measurements. For the measurements of a transistor, five micro-manipulators with their needles are needed with 2 needles placed on every pad of the source/drain terminals. On the contrary, there is no need for two probes on the gate terminal as it is used to apply a reverse bias. The Kelvin connection ensures the elimination of the impedance contribution of the

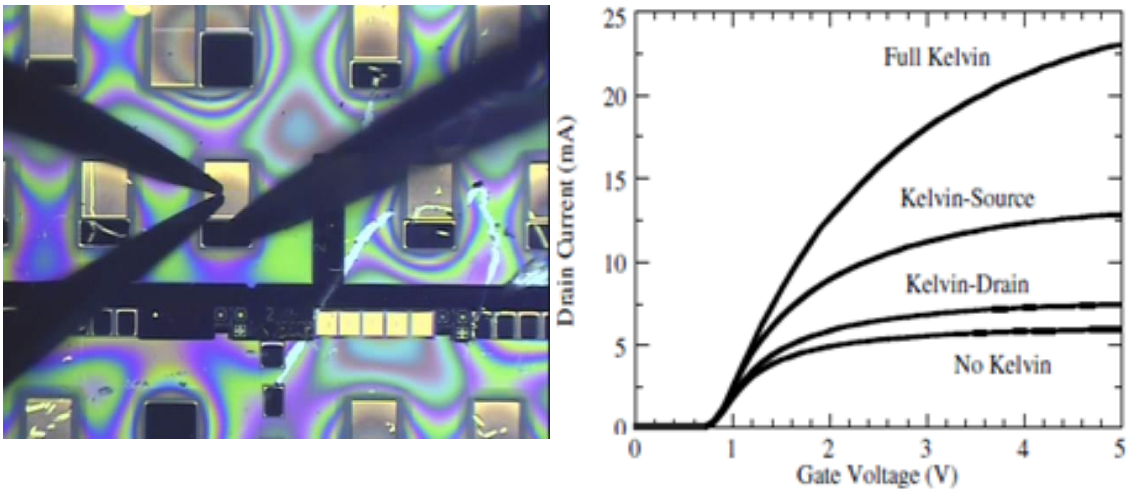


Fig. 4.5: Left- Kelvin measurements configuration.
Right- Typical Transfer characteristics with 4 different connections [2].

wiring and contact resistances.

Often, there is the perception that the Kelvin connection only in one of the terminals is adequate. This is absolutely erroneous and the graph on the right of the figure 4.5 demonstrates it. The ultimate behavior i.e. the highest current is achieved by the "full Kelvin" namely the Kelvin connection on both of the pads.

4.3 First run of measurements in one mask period

Fig. 4.6: Placement of the under investigation period on the sample.

Firstly one period is selected to be measured. It must contain devices with good morphology and such periods are usually placed in the middle of the processed sample. All the involved structures must be measured in order to check the uniformity of the material.

In the case of our sample, the red marked period **S2P25**, was selected. TLM patterns, diodes, and transistors are involved in the period and are investigated separately subsequently.

Measurements of TLM patterns

For the TLM (Transmission Line Method) patterns, the I-V measurements have to be performed up to 1-2mA range. The extracted values are the specific contact resistance r_C ($\Omega \cdot cm^2$) and the sheet resistance R_{sh} ($\Omega/\square$).

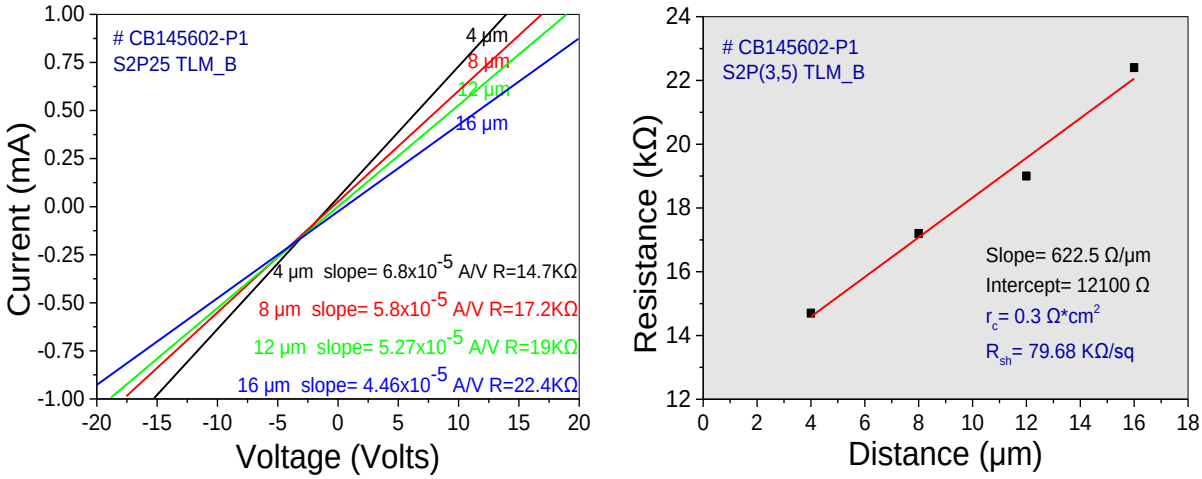


Fig. 4.7a: I-V from the different pads of the TLM pattern on p-type implanted layer (left) and the corresponding resistance vs pad distance plot from which the R_c and R_{sh} are extracted (right).

In the graph above the I-Vs as well as a graph for the resistance in dependence on the distance are presented for the period under test. In the inset one can see the extracted parameters.

The TLM patterns on n-type material were not operational due to a mask-design problem. The utilized instrument was the parameter analyzer Keithley 4200-SCS.

For the parameters extraction a graph like that on the right is necessary. The equations for the calculation of the parameters follow:

- R_{sh}=slope·Z
- R_c=intercept/2
- $r_c=R_c^2 \cdot L \cdot Z/Rsh$

.

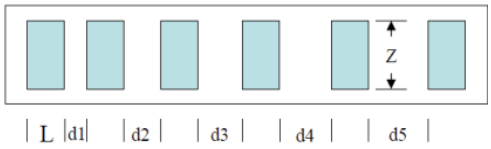


Fig. 4.7b: TLM structure

Measurements of single diodes

The forward measurements have to be performed up to a voltage corresponding to 50A/cm^2. Anyway this shouldn't be lower than 3.5V. The reverse measurements have to be done up to 200V where the leakage current value must be measured.

From the linear scale characteristics are determined: 1) the reverse breakdown voltage of the diode V_{br} (if it is lower than 200V) and 2) the differential resistance, R_{diff} (10A/cm^2 and 40A/cm^2). In the case of a breakdown in a lower than 200V bias, the room lights must be switched-off to observe any possible light spot on the diode. The differential resistance can be calculated from the slope of the linear I-V at a forward current density value of 10A/cm^2 and 40A/cm^2. If the above current densities, necessary for the R_{diff} determination, are not reached in the range of bias 0-5V, then the R_{diff} values at V=4V and 5V should be determined.

From the semi-logarithmic scale characteristics are mainly determine 1) the existence of any double barrier, 2) the leakage current, I_{leak} and 3) the knee voltage V_{knee}. The latter is extracted by taking the value at the intersection of the two linear parts of the semi-log graph (exponential and ohmic regime). The leakage current value at 200V is of common use. If V_{br}<200V, mention that I_{leak} (200V)= "∞"

In Fig. 4.8 we see the measurements and the extracted parameters of the involved in the under investigation period, diode. The parameter analyzer Keithley 4200 was used. In order to help in the detection of double barrier, in the inset of the forward graph a indicative forward measurement of a diode with double barrier is presented where the two distinct barriers are obvious.

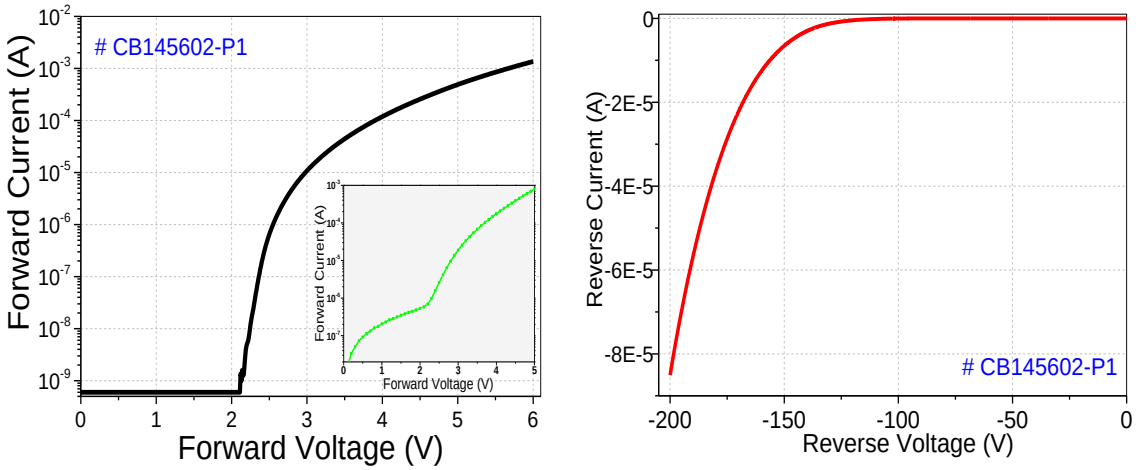


Fig. 4.8: Forward (semi-log) and Reverse (Linear) characteristics.

- V_{knee}=2.25 V, no double barrier,
- R_{diff}= 4896Ω (@ 4V), R_{diff}= 1693 Ω (@5V)
- I_{leak}=*-8.23x10^{-5} A (@200V)*

In the case of good reverse operation of the diode, C-V measurements (AC characteristic) have to be conducted with an LCR meter. During the measurement, the operator must check and be aware of the dissipation factor (ratio of the real over imaginary part of the impedance). The smaller the value of the D, the better accuracy is achieved to the measurement. The frequency is usually set to either 100kHz or 1MHz.

It must be pointed out that the C-V measurement must be performed when the power diode is blocked and the junction capacitance is mainly characterized. When the power diode is in conduction, not only capacitance is measured, but also the power device dynamic resistances and parasitic inductances.

From the C-V and particularly from the $1/C^2$-V graph, can be extracted the concentration (N_d) and the depletion width (W_d) from the following equations (1) and (2).

$$N_d = \frac{1}{q\varepsilon_o\varepsilon \mathrm{A}^2}\frac{C^3}{dC/dV} = \frac{1}{q\varepsilon_o\varepsilon \mathrm{A}^2}\frac{2}{d\left(1/C^2\right)/dV} \quad (1)$$

$$W_d = \frac{\varepsilon_o\varepsilon_r \mathrm{A}}{C} \quad (2a)$$

$$W_d = \sqrt{\frac{2\varepsilon}{qN_D}\left(V_{appl}+V_{bi}\right)} \quad (2b)$$

where: A is the area of the plates of the imaginary capacitor, namely the product of the length of the depletion region with the Z dimension, in square meters.

$\varepsilon_r = 9.66$: relative permittivity of SiC

$\varepsilon_o = 8.85 \cdot 10^{-14}$ F/cm: permittivity of vacuum

$q = 1.602 \cdot 10^{-19}$ Cb: elementary (electron) charge

It is obvious from (1) that for a uniform in-depth doping the $1/C^2$-V curve will be a straight line with a slope $d(1/C^2)/dV$. The depth at which the doping density is evaluated is obtained from eq. (2a) and (2b). The equation (2a) assumes that the capacitance of the diode can be represented by a capacitor having plates with an area equal that of the diode and spacing between them equal to the depleted width. If this image works well, the two values of W_d should be the same.

Moreover the V_{bi} (built in potential) can be extracted from the $1/C^2$-V curve. It is equal to the voltage value that the extrapolated curve intersects the x axis. The analysis of $1/C^2$-V can help in checking whether the drift layer has been influenced by the ion implantation or even a new insulating layer has been created following implantation.

Fig. 4.9 shows the results of the C-V measurements of our diode, and subsequent analysis, performed for f=1MHz. The utilized instrument is an Agilent 4284 LCR Meter. On the right we see the $1/C^2$-V curve while in the insert is presented the extracted the N_d-W profile.

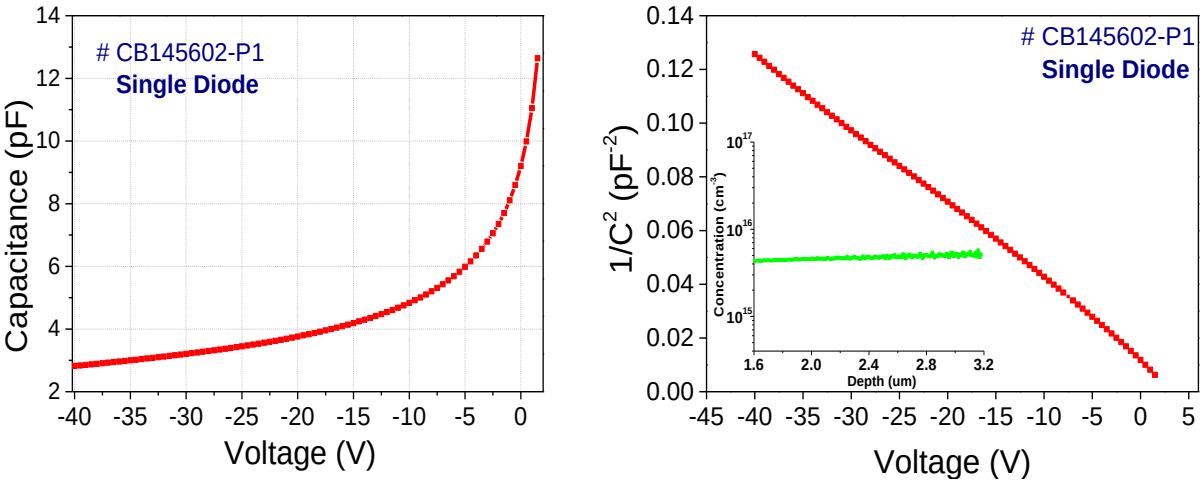


Fig. 4.9: C-V (left) and $1/C^2$(V) (right) characteristics of diode S2P25, at f=1MHz.
Doping profile of the base of 4H-SiC diode calculated from C-V in the inset (close to the nominal one).

Measurements of transistors

In order to not put the probe tips in the same device many times, a series of consecutive characteristics have to be measured. In the case of our sample, the parameter analyzer Keithley 4200 was the utilized instrument.

- **Drain-Source characteristic at V_{GS}=0, 2V and low current**

Measurements for positive and negative values of V_{DS} in order to check the "ohmicity" of the drain source contacts must be performed. The testing has to go up to enough high current values (~1mA) to be sure for the "good current conduction" in the channel of the transistor. The measurement at V_{GS}=2V is necessary for normally-off devices in order to have a large effective channel width.

A very important parameter, the specific ON resistance (R_{ON}) of the device can be extracted from this measurement since it is equal to the slope of the straight line near 0 current. Mainly, it is expressed in mΩ·cm^2 as the above is multiplied by the active area of the device.

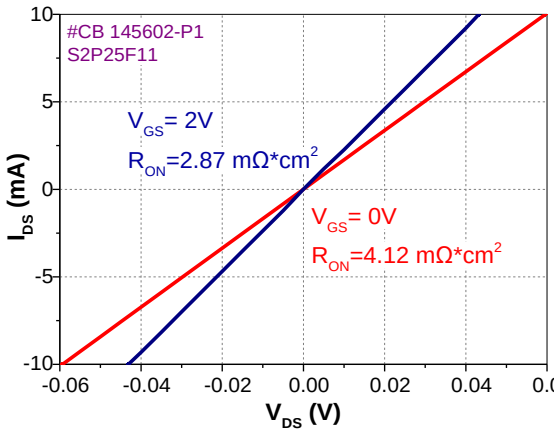


Fig. 4.10: Low current ON I_{DS}-V_{DS}

For our under test period, all the devices exhibited low R_{on} values and close enough to the theoretically expected ones. The descriptive measurement of the F11 device is shown in fig. 4.10. The extracted R_{on} values are shown within the graph. As it ws expected the R_{on} value for V_{GS}=0V is greater than the corresponding one for V_{GS}=2V.

- **Gate-Source characteristics**

From these characteristics, the quality of the gate junction can be evaluated as well as the transistors measurements conditions for the conduction (ON) and the blocking (OFF) characteristics can be extracted. Indeed, they allow determining the range of V_{GS} variation for max-forward-current and max-blocking-voltage determination purposes. The forward and reverse I-V should be drawn up to a current value corresponding to 5A/cm^2 and 15mA/cm^2 respectively.

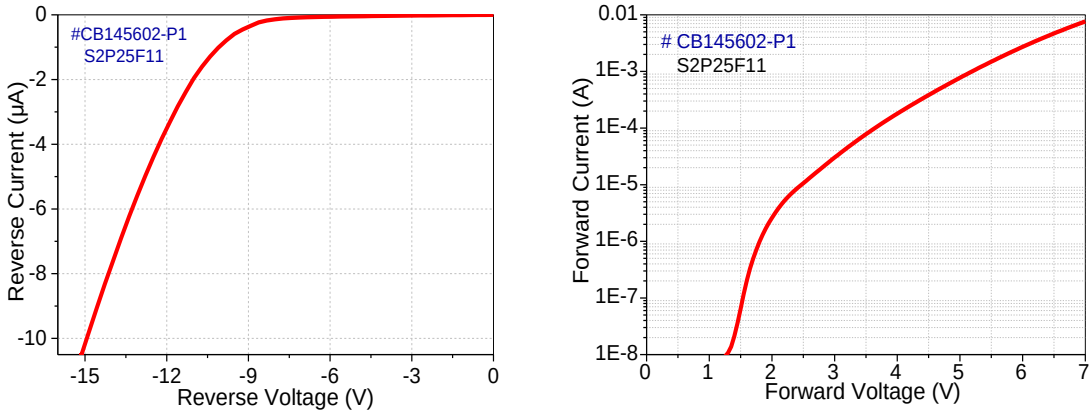


Fig. 4.11: Gate-Source DC I-V characteristics of S2P25F11.

- V_{knee}=1.92V
- No_double_barrier
- BV_{GS}(@-15mA/cm^2)=-15.1V

The *extracted values* are usually the knee voltage (V_{knee}) and the BV_{GS} namely the gate-breakdown reverse voltage. The knee voltage is extracted in the same way as for a diode. Its value will show whether the gate-source diode is controlled by the pn junction or by a Schottky-like

junction. From the semi-log graph, the possible existence of double barrier can be also noted. The gate-breakdown voltage, BV_{GS}, must be defined as the reverse voltage value which corresponds to low current density in order to avoid the stress of the transistor. A value of common use and adopted in this work is of 15mA/cm^2. However, one can meet different definitions in the bibliography.

The gate leakage current (I_{GSS}), must be determined at $V_{GS}=V_{th}$-20V, where V_{th} is the anticipated from theoretical calculations value of threshold voltage and for two V_{DS} values: 0V and 200V. The latter value is measured during the blocking voltage measurements (see later).

In fig. 4.11 the measurements and the extracted parameters for the F11 device are shown. The majority of the involved in the period devices exhibited double barrier while the extracted V_{knee} values were usually lower than 2V. As for the BV_{GS}, the best reported value was -15.1V for the F11.

- **Transfer (I_{DS}-V_{GS}) and (g_m-V_{GS}) characteristics**

The I_{DS}-V_{GS} should be measured for V_{DS}=0.1 and 1V. In the case of the linear graph, the transconductance g_m (slope of I_{DS}-V_{GS}) -V_{GS} can be also drawn (right y-axis). In the semi-log graph, the corresponding measured I_{GS} can be also drawn (right y-axis) to check directly the influence of the gate leakage to the output current. Concerning the compliance values, a current compliance which corresponds to 50A/cm^2 and 5A/cm^2 should be imposed for I_{DS} and I_{GS} values respectively.

The important parameter of the threshold (or turn-off) voltage, V_{TH}, (value of V_{GS} when I_{DS} value drops to zero) can be determined directly from the transfer characteristic as the voltage value where the linear part of the I-V intersects with the x axis). The bias at which a g_m value peak is observed (if it is clearly seen) can be also used as an alternative definition. Furthermore, another way for the extraction is by the intersection of V_{GS} axis with the linear part of the $\sqrt{I}$ -V. The curve becomes more perpendicular making the detection of the linear part easier and consequently, the V_{th} voltage extraction more accurate.

It is worthwhile to mention that in the datasheets of commercial power devices quite often the V_{TH} value is defined at a specific current value of the order of some mAmps. For a more elaborate analysis concerning the different approaches for the threshold voltage extraction, found in the literature, is recommended to refer to [27].

In the figure 4.12 below, we see the measurement for the F11 transistor of our period. From the measurements to all the involved devices, we observed that the extracted V_{TH} values are higher than the theoretically expected and the deviation becomes greater as the mesa width increases.

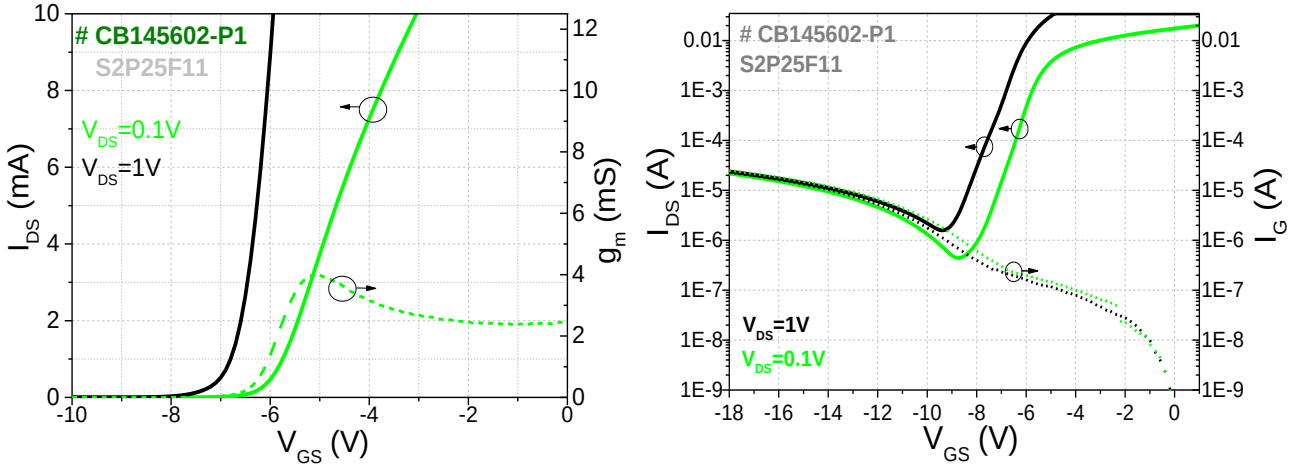


Fig. 4.12: Transfer characteristics in linear (left) and semi-log (right) graph.

It is noteworthy that from the semi-log graph on the right and particularly from its right y-axis we observe the dominance of the gate leakage current in the off state of the device.

- **Drain-source ON characteristics**

These characteristics are also known as family curves. The goal is to ascertain whether the transistor operates as expected and mainly if the OFF state is achievable at some gate voltage. Due to the latter, the measurements are usually performed only up to some tens of mA.

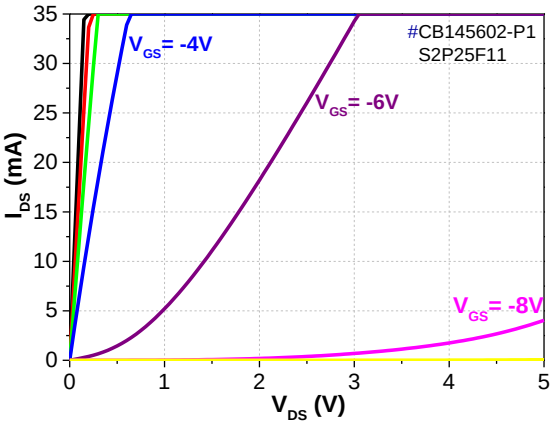


Fig. 4.13: DC ON characteristic.

Although this is not a useful measurement for extracting quantitative information, is very important for the continuity of the study.

Most of the transistors involved in our under investigation period exhibited behavior as the presented in the graph (for F11) so we deduce that the transistors operate as expected namely the OFF state is achievable.

- **Blocking Drain-Source characteristics**

For devices with edge isolation, the high voltage handling in air (>200V) is a very important device characteristic. The power density value should be limited at a value below 500W/cm^2.

The important parameter of the maximum blocking (or breakdown) voltage (BV_{DS}) on air should be measured. This is defined as the Drain-Source voltage which corresponds to 3A/cm^2 current density and V_{GS}=V_{TH}-20V. The above current densities should result to a total power dissipated through the device lower than 500W/cm^2. Otherwise, a lower value should be used. At that moment, the I_{GSS} (V_{GS}=V_{TH}-20V, V_{DS}=200V) can be determined if it is possible.

The semi-log graph allows determining with accuracy any problem of leakage current which must be measured and reported if it is possible at three different conditions, I_{leak}(V_{GS}=V_{TH}, V_{DS}=0V), I_{leak}(V_{GS}=V_{TH}-20V, V_{DS}=0V) and I_{leak}(V_{GS}=V_{TH}-20V, V_{DS}=200V). The leakage current is important because that is roughly how much current will be flowing through the device when you are close to the limits of the OFF state and that current times the applied voltage give the power that is being dissipated.

Furthermore, the semi-log graph allows the determination of the voltage gain. The voltage gain (μ) is defined as: $\mu = \left.\frac{\partial V_{DS}}{\partial V_{GS}}\right|_{I_{DS}}$. The μ is connected with the transistor dimension by the formula [2]: $\mu \approx \exp\frac{\pi L_{ch}}{W}$ where, L_{ch}=L_G+L_A (L_G the

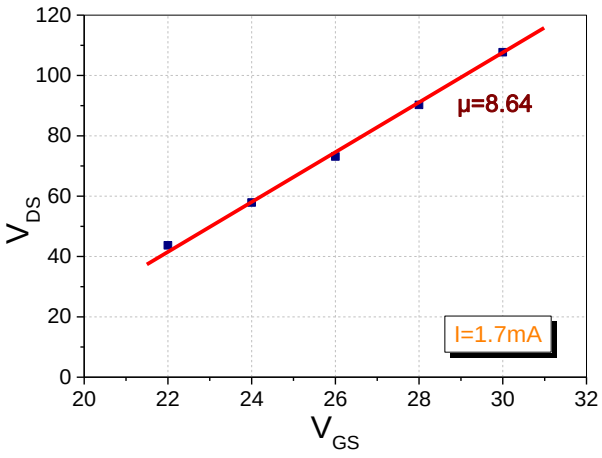


Fig. 4.14: Voltage gain determination

implanted depth and L_A the depletion width below the gate). For the definition of μ there are several approaches. The more systematic seems to be by drawing the V_{DS} (I_{DS}=0.1mA/mm) versus V_{GS} graph and determine the voltage gain from the gradient of the straight line. For a power device, usually the expected voltage gain value is higher than 40. In figure 4.14, the graph which is used for the extraction of the transistor voltage gain is presented.

In figure 4.15 below we can see the measurement for the F11 device of our period under test accompanied by the extracted parameters. The measurements are confined up to 200V (max limit of the Keithley 4200-SCS), thus the imposed current compliance was set to 1.7mA in order to limit the power density below 500W/cm^2. For measurements in higher voltage biases, another instrument (e.g. curve tracer) must be utilized.

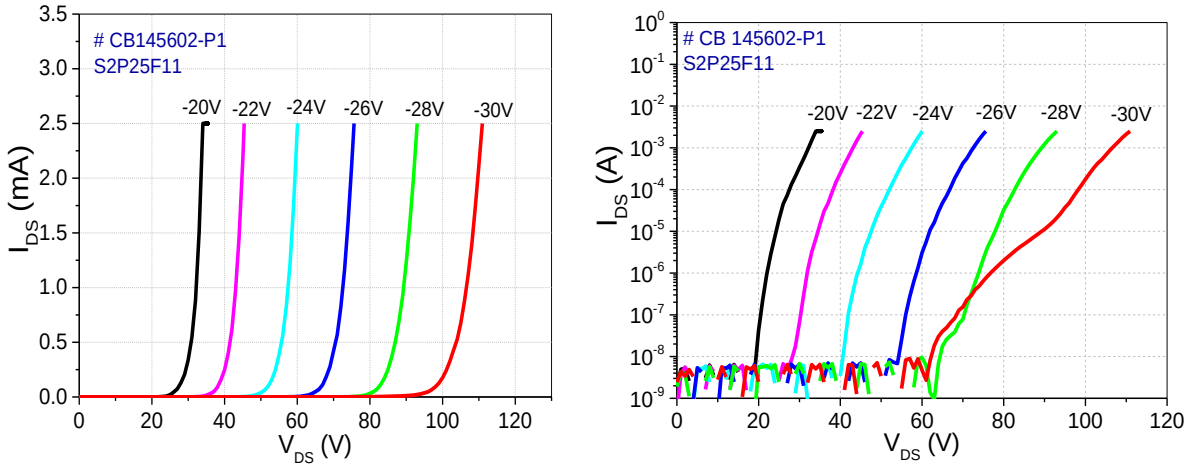


Fig. 4.15: Linear and semi-log blocking characteristics.

- $I_{leak}(V_{GS}=V_{TH}$=-7V, V_{DS}=0V)<10^{-8}A,
- $I_{leak}(V_{GS}=V_{TH}$-20V=-27V, V_{DS}=0V)<10^{-8}A,
- $I_{leak}(V_{GS}=V_{TH}$-20V=-27V, V_{DS}=200V)=∞,
- BV_{DS}=110V
- μ=8.64

Apart from the first transistor F11 the others exhibited quite lower BV_{DS} and μ values.

Analysis of results in one period

The type of analysis depends on the mask used and the different parameters values met in a mask period. Graphs giving the dependence of R_{ON}, V_{TH} or leakage currents, on the mesa width (W_{ch}), gate length (L_g) or the number of fingers (n), can give a physical insight in transistors operation and help to extract useful conclusions.

Below we see for our period, the evolution of the R_{ON} and V_{TH} as the mesa width increses. The measured black curves are accompanied by the respective theoretical ones. From the left graph, we see the decrease of the R_{ON}, in (Ω-cm^2) as the channel width increases. We also observe that the measured values are smaller than the theoretically expected. Concerning the V_{TH}, the analysis shows that it decreases (the absolute value increases) with the increase of mesa width. This is confirmed with the theory of JFET operation since the formula of threshold voltage is $V_{TH} = -\frac{qN_d\alpha^2}{2\varepsilon_s} + \frac{kT}{q}\ln\left(\frac{N_dN_a}{n_i^2}\right)$. The "α" is the half of mesa width (W=2α)

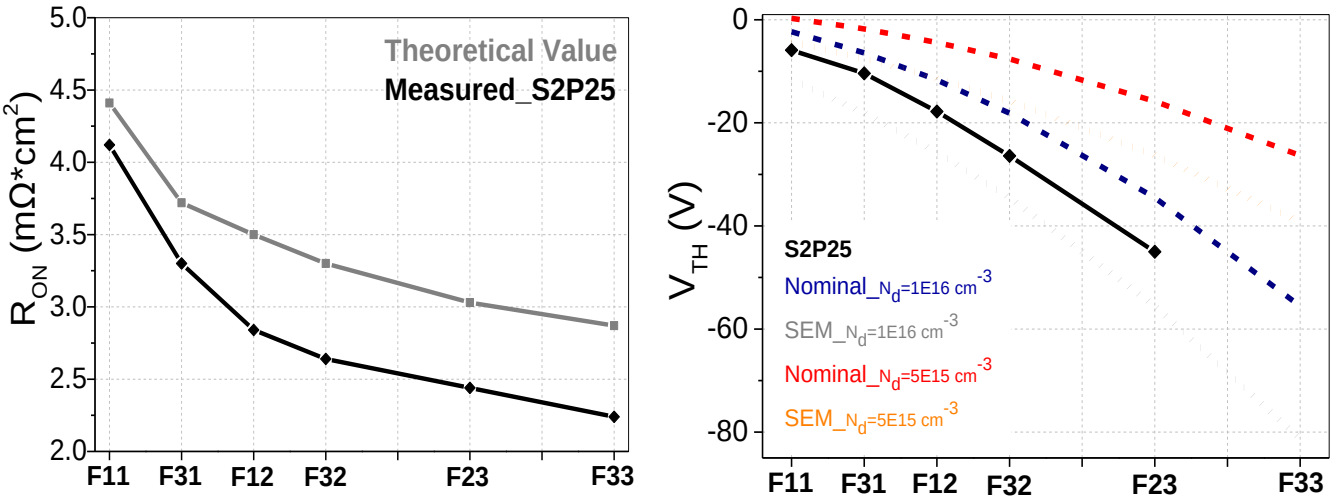


Fig. 4.16: Left- R_{ON} evolution in $m\Omega \cdot cm^2$. SEM dimensions into consideration for theoretical calculations, Right- V_{TH} evolution. Graph according to nominal and SEM dimensions as well as 2 different doping values ($1 \cdot 10^{16}$ and $5 \cdot 10^{15}$ cm^{-3})

In the right graph we see except of the curve of the period, four theoretical curves. Nominal and after SEM observation dimensions as well as two different doping concentrations are examined. We observe that the grey (N_d=1E+16 cm^{-2}, SEM dimensions) and blue (N_d=1E+16 cm^{-2}, Nominal) curves are closer to the measured black curve.

4.4 Measurements in different mask periods – Statistical study

By the end of the measurements in one mask period we are able to draw some preliminary conclusions mainly about the uniformity of the under investigation sample. It is easily understood that these conclusions are not totally reliable, thus statistical study is necessary. The devices that exhibited the greatest interest from the previous stage of measurements must be selected to be measured in several different periods.

The purpose is to draw histograms and mapping graphs for the important parameters of the devices which are going to lead us to more firm clues. The statistical sample should be big enough for trustable results but not very big for time and effort saving.

For TLMs usually the statistically investigated parameters are the R_c and R_{sh} while for the diodes, the V_{knee}, the existence of double barrier and the I_{leak} (at 200V). For the transistors usually the parameters for statistical study are: V_{knee}, BV_{GS}, R_{ON}, V_{TH} and BV_{DS}.

For our sample CB145602-P1, statistical study has been performed for 7 (among the 11 involved) transistors of each period, in 75 periods, namely 525 transistors were measured. All the different channel widths are met among these 7 devices. Moreover, statistical study has been performed for the TLM patterns as well as for the diodes although these are out of the scope of our application and therefore of our work. Below, we see the study for the TLMs, the diodes and for time saving, the study only of the F11 transistor. In the end of each parameter discussion the results from the statistical study of all the investigated devices are summarized. Apart from the periods on the edges of the sample, all the others were tested ensuring a big statistical sample. The periods in the mapping graphs without color were not tested for various reasons (sample edge, problematic measurements, etc).

➢ TLMs

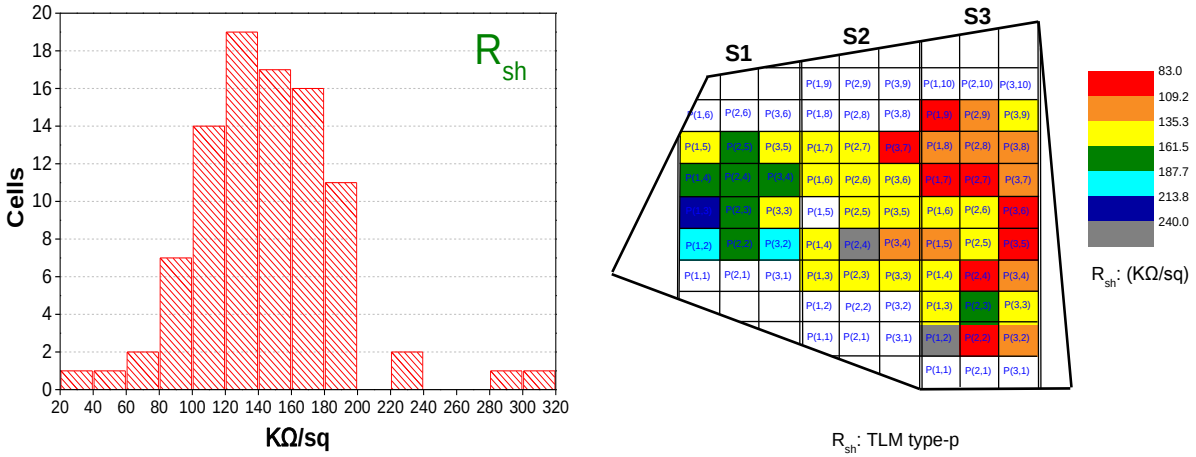


Fig. 4.17: Histogram (left) and mapping (right) of p-type gate layer sheet resistance.

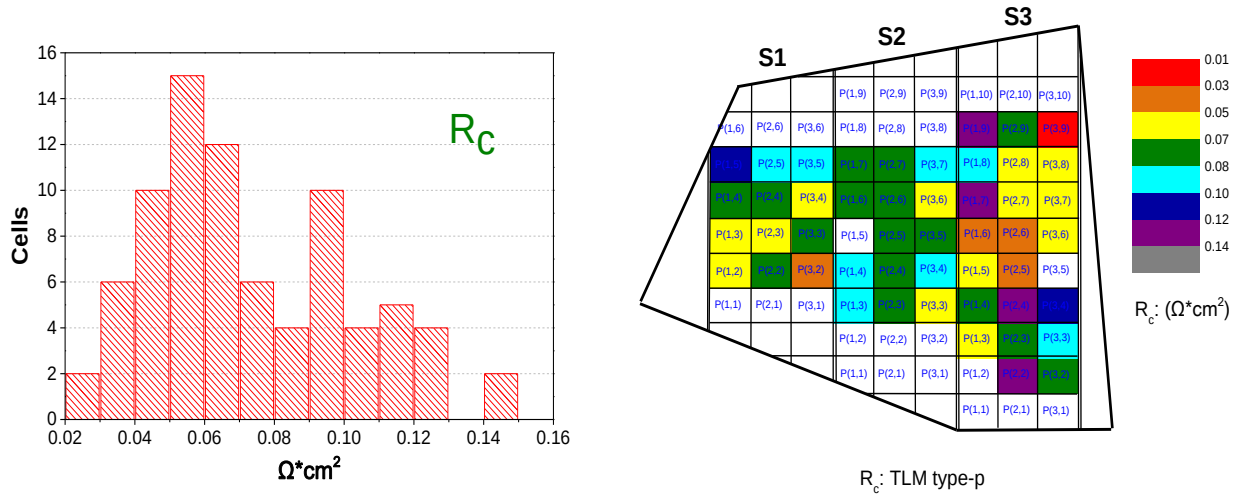


Fig. 4.18: Histogram (left) and mapping (right) of specific contact resistance of ohmic contacts on p-type layer.

In the specific sample CB145602-P1, the TLM on n-type material were not measured due to a mask fabrication error. On the other hand the measurements on p-type implanted layers indicated rather exponential than the desired and expected good linear I-V behavior, suffering from the fact that the I-Vs between different pads weren't linear but rather that of two diodes in parallel connection and "inverse orientation". By making a rough approximation of linear behavior we could extract the parameter values.

The largest part of TLMs have values of R_c which ranges from 0.04 $\Omega \cdot cm^2$ to 0.1 $\Omega \cdot cm^2$. There is no specific spatial dependence of the specific contact resistance. On the contrary there is a clear spatial dependence of the R_{sh} value with lower values (due quite probably to higher doping) on the right side of the sample. The value of R_{sh}, ranges from 80 kΩ/sq to 200kΩ/sq.

➢ Diodes

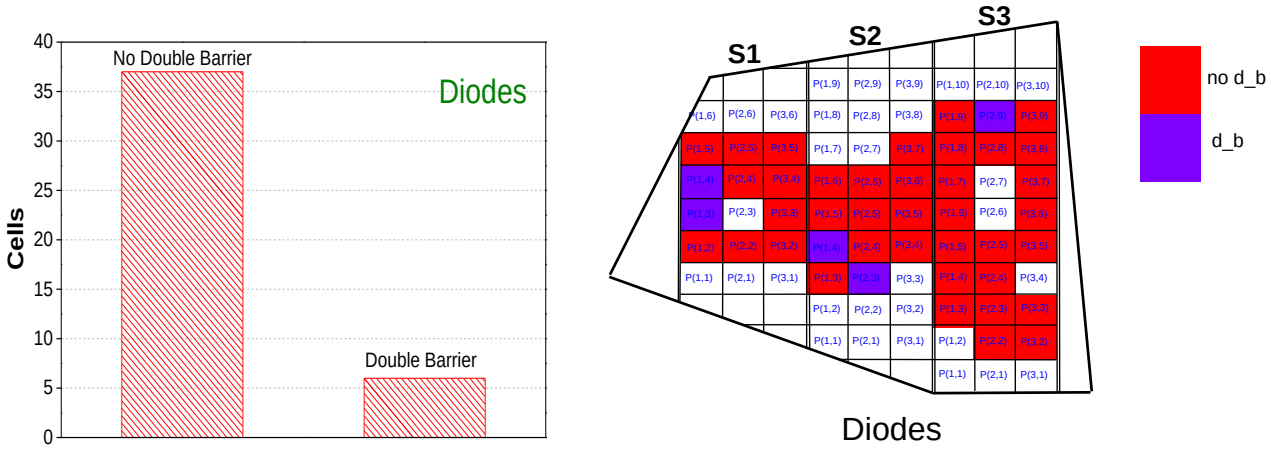


Fig. 4.19: Histogram (left) and mapping (right) of the existence or not of double barrier in the forward regime.

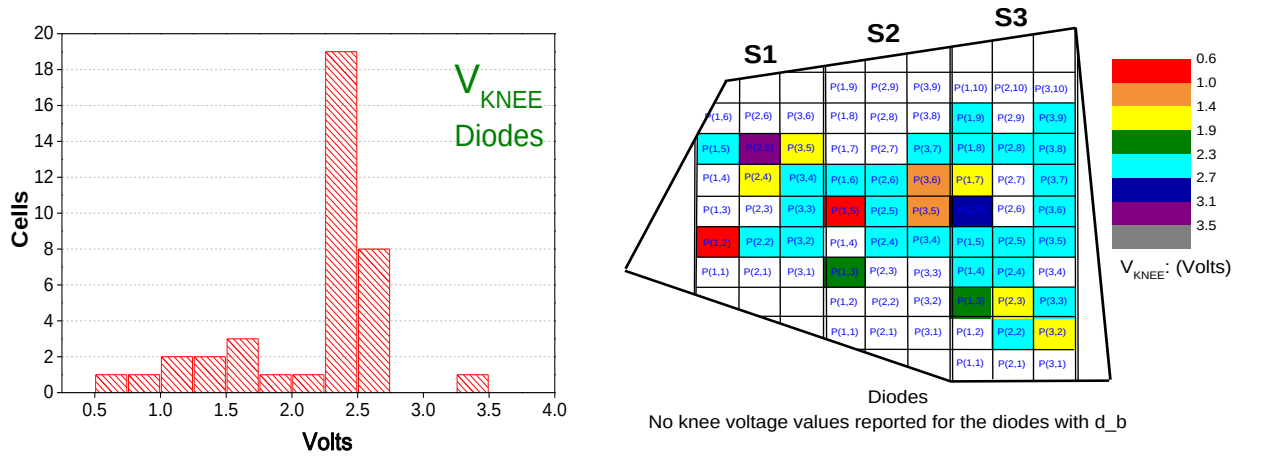


Fig. 4.20: Histogram (left) and mapping (right) of the single pn junction knee voltage

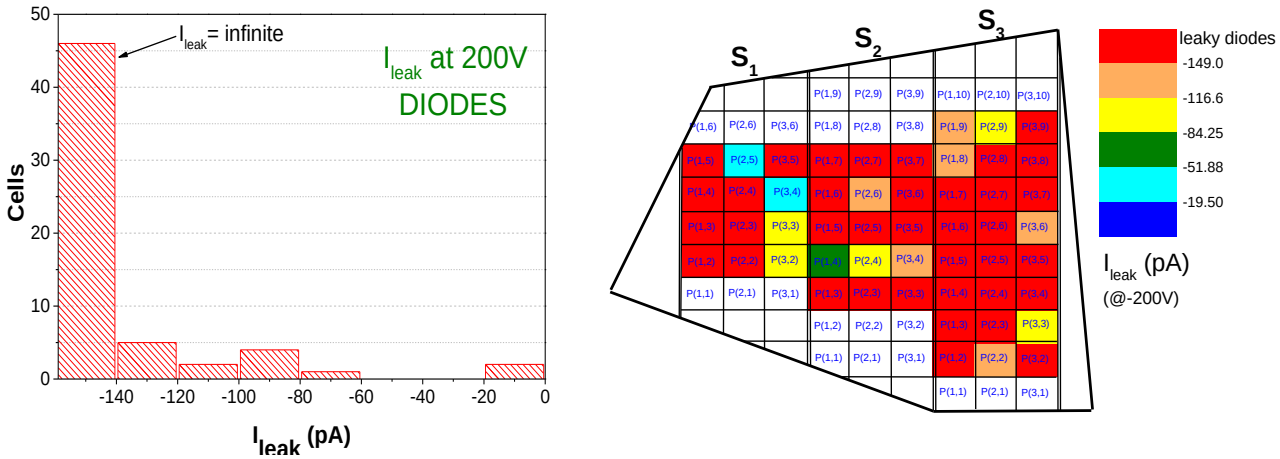


Fig. 4.21: Histogram (left) and mapping (right) of the diodes leakage current at -200V.

The vast majority of the diodes did not exhibit double barrier while the reported V_{knee} values range from 2.25V to 2.75V. Note that no V_{knee} values were reported for the diodes detected with double barrier as it would be pointless. Despite the good diodes performance in the forward regime, in the reverse the reported leakage current values were high as we can see from the graph, deducing that most of the diodes are leaky at 200V. None of the examined parameters had a specific spatial dependence.

➢ Transistors

Gate-source characteristics:

The investigated parameters are: existence of double-barrier (d_b), V_{knee} and BV_{GS}.

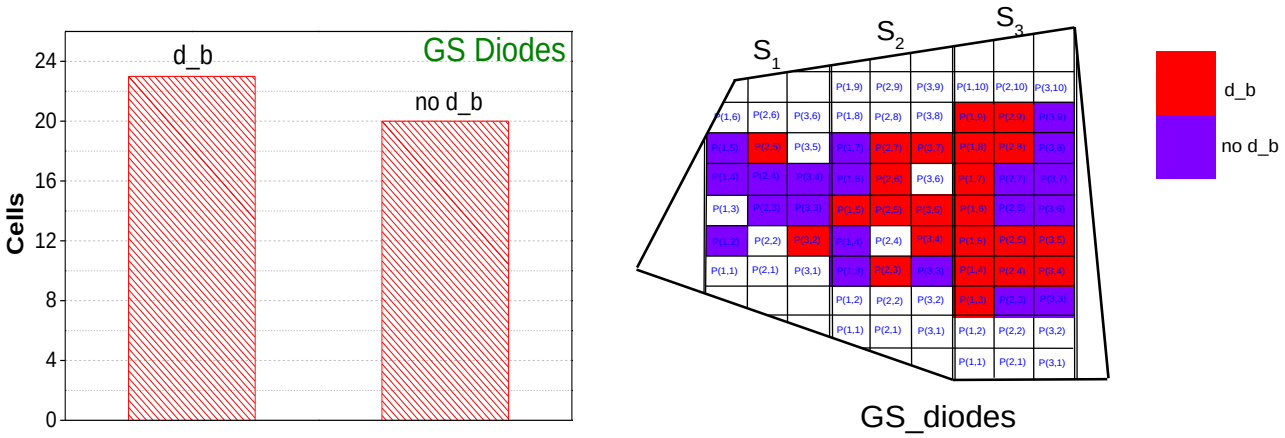


Fig. 4.22: Histogram (left) and mapping (right) of the existence or not of double barrier in the GS diodes.

We observe that 23 diodes have double barrier (d_b) whilst 20 were detected without d_b. Furthermore there is some spatial dependence with the periods between S2 and S3 regions covered with red color, namely detected with d_b.

- The same more or less trend was observed also for the rest 6 investigated devices.

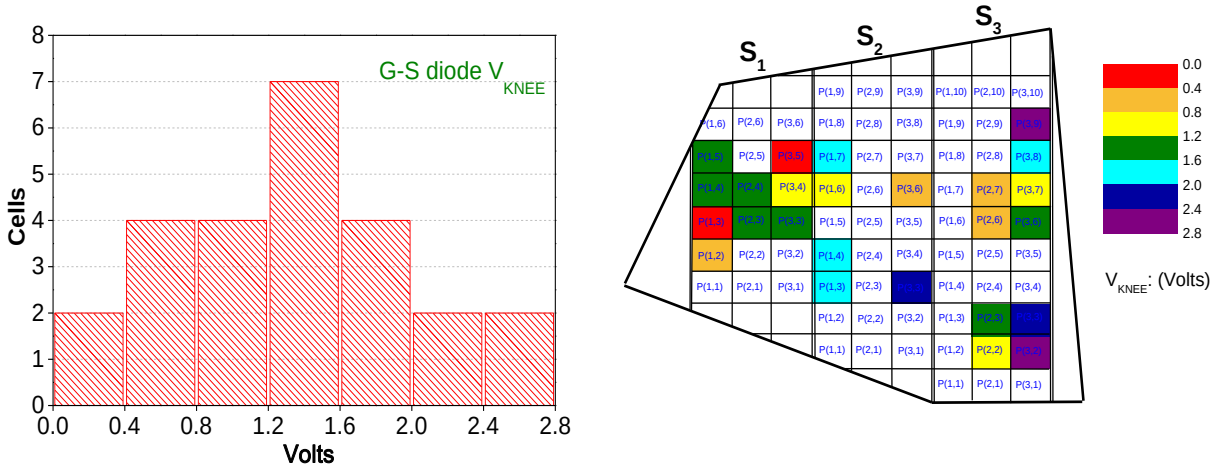


Fig. 4.23: Histogram (left) and mapping (right) of the gate-source-diode knee voltage.

No V_{knee} values are reported for the devices detected with double barrier. The largest part of the measured values ranges between 1V and 2V. For a SiC diode the expected V_{knee} value, which is a strong indicator for the forward behavior of the GS junction, is expected to be higher than 2V.

- In our case, it's notable that we observe for all the under test transistors, many values, usually more than half, lower or much lower than this value. In addition, a concentrated distribution of the values around a specific one is not observed but the distributions are characterized rather from a high dispersion. So we can deduce that the GS junction does not function properly in the forward regime.

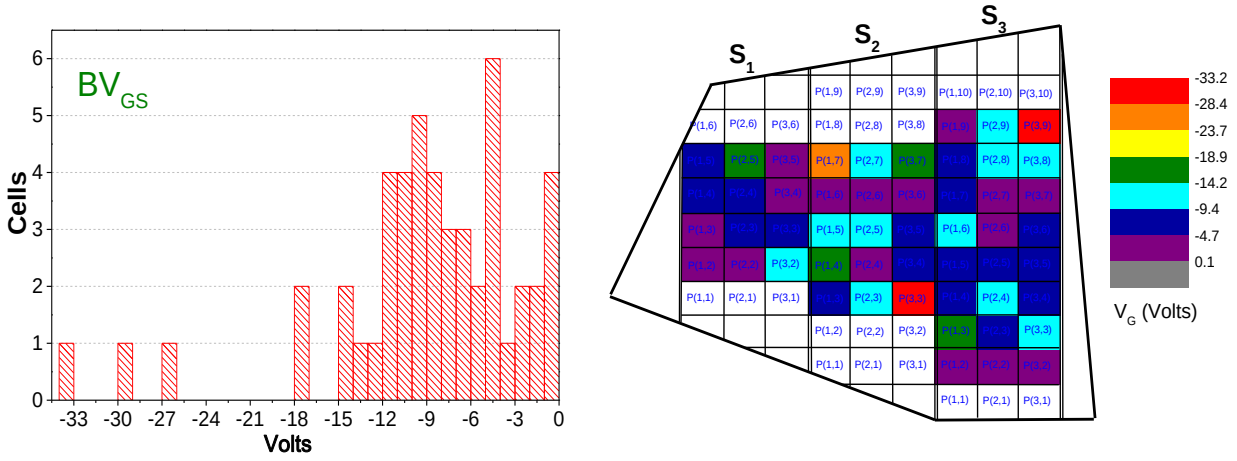


Fig. 4.24: Histogram (left) and mapping (right) of BV_{GS}

The BV_{GS} ranges mostly from 0V to -15V. It is noteworthy that the three transistors with the best BV_{GS} values were also detected with single barrier and good V_{knee} values.

- Generally from the study of all the (seven) transistors, we observed that the majority of the devices are not able to withstand significant reverse bias on the Gate Source junction with their reported values placed between -10V and 0V. Thus we can deduce the low quality of the GS junctions in the reverse regime. Taking into account the aforementioned results from the V_{knee} study we can deduce the overall low quality of the GS junction, which does not exhibit proper behavior neither in forward nor in reverse regime. The GS junction may be a quite challenging and critical fabrication step but plays a very important role for the good function of the transistor.

Drain-source ON characteristics:

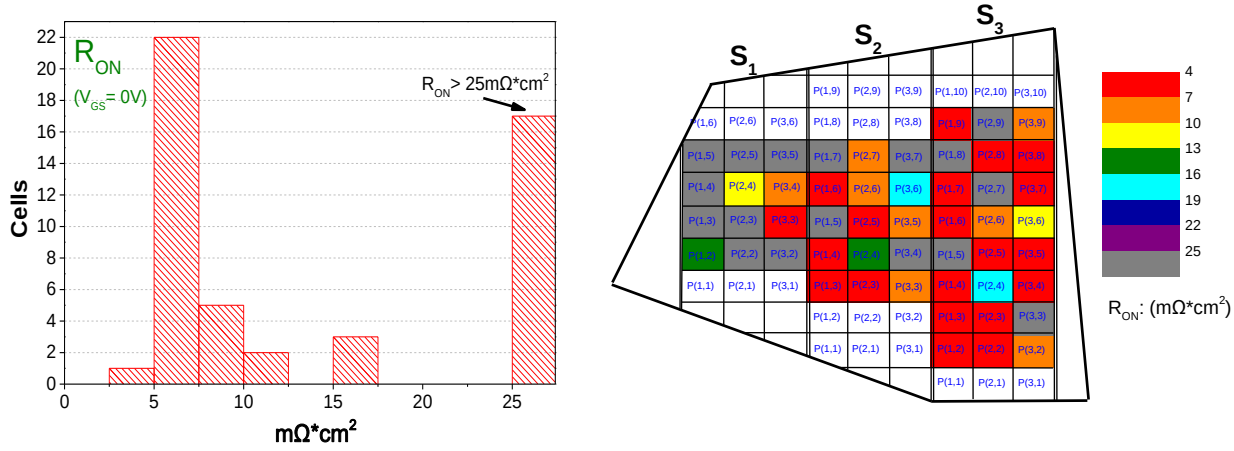


Fig. 4.25: Histogram (left) and mapping (right) of the transistors R_{ON}.

Concerning the R_{ON} value, the largest part of the transistors exhibit good behavior with values lower than $10m\Omega \cdot cm^2$. It must be mentioned that the last bar involves some quite extreme values which were mainly measured from transistors placed on the left side of the sample which is indicated by S1 in the mapping.

- From the histograms we observed that apart from the F11 device, the reported R_{ON} values are much higher than $10m\Omega \cdot cm^2$ while high dispersion characterize them. Moreover many extreme values are detected so we can say that in term of R_{ON} the devices did not exhibit the anticipated behavior.

Transfer characteristics:

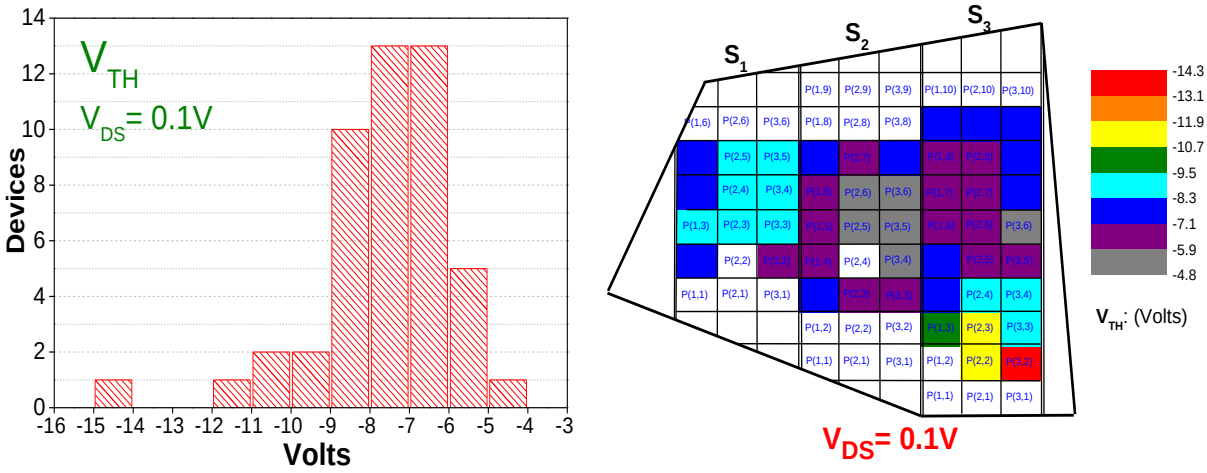


Fig. 4.26: Histogram (left) and mapping (right) of the transistors V_{TH}.

For the F11, a concentrated distribution around -7V is noted, something that can be perceived as the proof for the "real" value of V_{TH}. It is obvious in the mapping that we have a slight spatial dependence. From the inner part of the sample to the outer part, the value of V_{TH} is reduced (more negative) and the spatial dependence seems to be radial-like.

- For all the different transistors, we observed more or less concentrated distributions around a specific value. Furthermore, from the mapping graphs we often noticed some spatial dependence mainly between the S_2 and S_3 regions.

Blocking Drain-Source characteristics

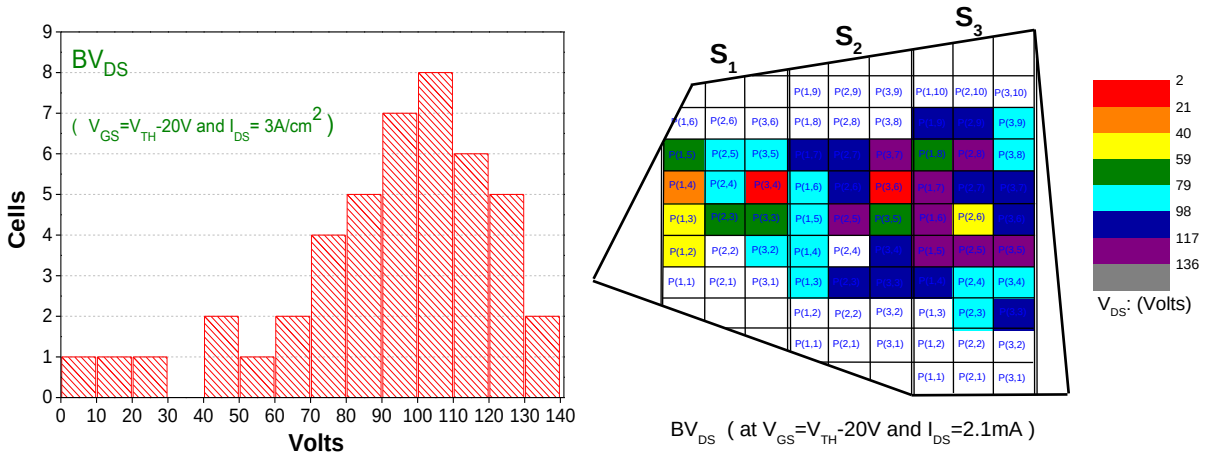


Fig. 4.27: Histogram (left) and mapping (right) of the transistors Blocking voltage.

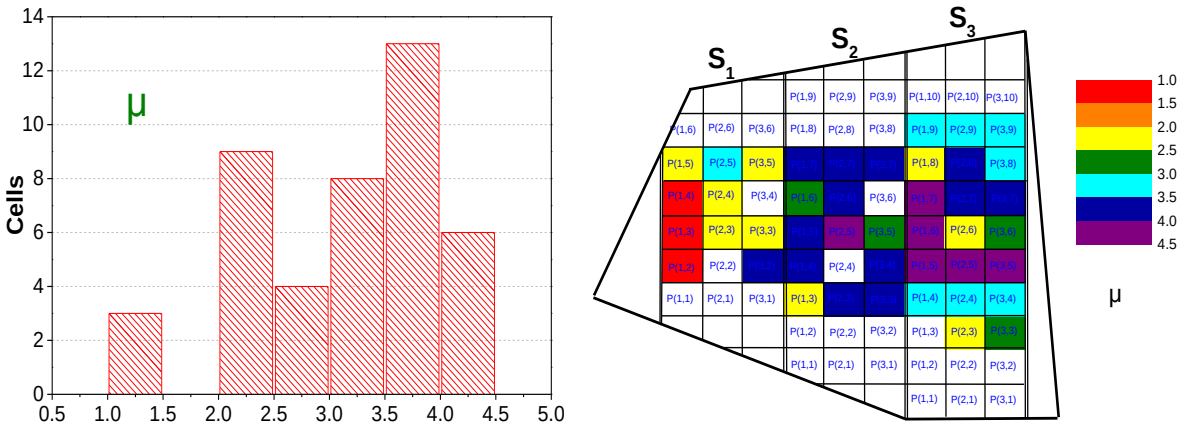


Fig. 4.28: Histogram (left) and mapping (right) of the transistors voltage gain.

The vast majority of the F11 V_{DS} values at $V_{GS}=V_{TH}$-20V and I_{DS}=3A/cm^2 are smoothly concentrated around 100V and range from 70V to 130V. There is a spatial dependence with higher effective blocking voltages towards the right side of the sample.

The voltage gain μ takes values smaller than 4.5. From the mapping we observe that the S1 region gathers transistors with lower voltage gain values in comparison with the S2 and especially the S3 where the highest reported values are placed.

- The narrowest transistor F11 exhibited the best behavior among all the under test different dimensions transistors, with the highest BV_{DS} and μ values, but provided that for a power device the acceptable gain must be higher than 40, we understand that, even F11 does not exhibit good blocking behavior.

4.5 Measurements of best devices

The final set of measurements must be performed only on the best devices of the sample.

Choice of the best transistors

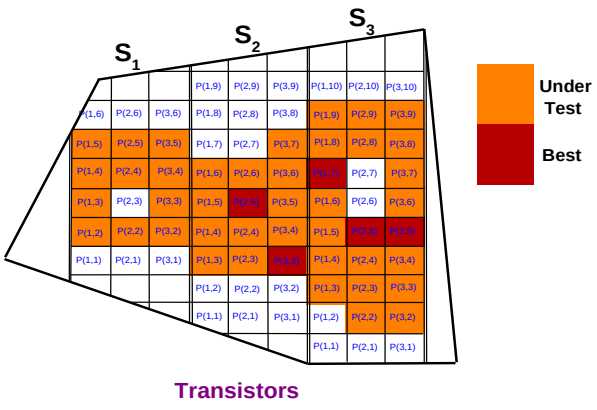


Fig. 4.29: Placement of best F11 transistors.

From the statistical study, the best devices can be determined. Concerning the transistors, the main criterion must be the V_{TH} values. They should be the closest to theoretically expected. Then, the blocking voltage follows in importance. R_{ON} is the 3rd in priority parameter followed by the GS leakage. The V_{knee} value is the last one. Thus, after detecting the devices that exhibit good behavior for each parameter, the correlations between them must be investigated in a way to choose at least 5 best devices according to the prioritization described above.

Figure 4.29 shows the mapping of the best F11 devices selected by using the above approach. After the overview of the mapping results and taking into account the aforementioned prioritization, we found all the correlations between the devices, which gave us the chance to conclude to the best 5 ones presented in the graph above. The orange cells indicate the periods where the F11 transistor was measured. The green cells indicate the

five periods where the best F11 transistors were detected. The same work is done also for the rest 6 under test transistors.

The criterion parameters of F11 are summarized in the following table.

Best devices criterion parameters

	V_{TH} (V)	BV_{DS} (V)	μ	R_{on} ($m\Omega \cdot cm^2$)	BV_{GS} (V)	d_b	V_{knee} (V)
S2P25F11	-5.6	126	4.2	6.95	-10.98	Yes	2.1
S2P33F11	-7	106	3.8	7.16	-29.74	NO	2.23
S3P17F11	-5.6	134	4.2	6.05	-9.21	Yes	2.95
S3P25F11	-6.3	126	4.1	5.43	-8.3	Yes	2.6
S3P35F11	-6.2	128	4.2	5.81	-9.03	Yes	1.75
Mean	***6.1***	***124***	***4.1***	***6.3***	***-13.5***	-	***2.3***
SD	*0.52*	*9.47*	*0.15*	*0.67*	*8.19*	-	*0.41*

- **Pulsed measurements**

Pulsed measurements must be performed on the best devices. This type of measurements allow measuring the forward (ON) drain-source characteristic at high currents and observe thus, the saturation regime. The conditions of these measurements are very important. The time off must be enough in order to let the device return in the ambient temperature. Of course high values of time off extend the duration of a measurement thus the parameter must be set to a value sufficient for the relaxation of the device but not very high. Usually time off equal to 1sec is enough while for the pulse width a value of common use is 200μsec.

In the graph below we can see the pulsed measurements for some of the best devices of our sample. Pulsed sweep was imposed on the Drain and DC step bias on the Gate. The measurement conditions follow: pulse width: 200μsec, time-off: 1sec, measurement time: 119μsec.

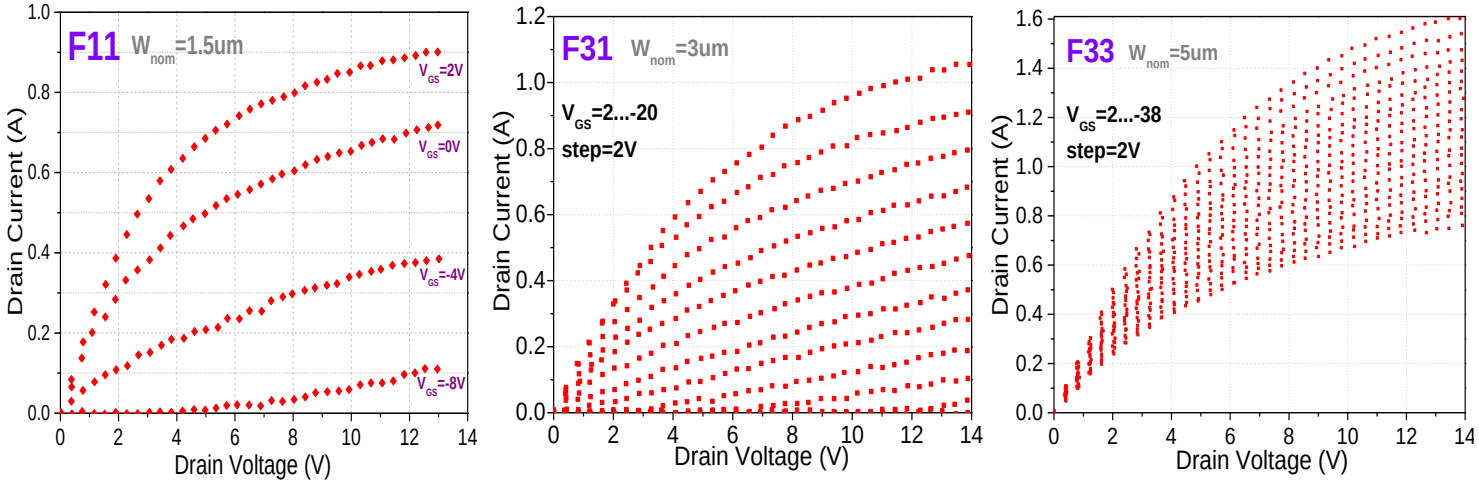


Fig. 4.30: Pulsed ON characteristics of F11, F31 and F33 transistors.

As it was expected, higher current values were observed from the pulsed measurements compared with the respective DC ones for all the different dimensions transistors. Furthermore, we clearly see that as the mesa width increases the transistor can pass greater amount of current while is more difficult to turn it off. We see that the narrowest device, the transistor F11 is turned off by a reverse bias on the gate of around -8V as well as for V_{DS}=13V, I_{DS} equals to 0.9V. On the other hand the widest transistor F33 is able to pass 1.6A for V_{DS}=13V but the turn off state is not achievable up to -38V. Two SMU instruments have been used for these measurements (SMU is a device that can source a voltage or current and measure itself without any extra connection). Particularly the Keithley 2602A and Keithley 2651A have been utilized.

- **C-V measurements**

Measurements of C_{iss} (input capacitance), C_{oss} (output capacitance) and C_{rss} (reverse transfer capacitance) have to be conducted at this point, with an LCR meter. Necessary condition for the performance of them is the OFF state of the transistor, namely the full depletion of the channel. Detailed information about these measurements as well as the corresponding circuitries can be found in Appendix 1. The measurements of these capacitance parameters $C_{iss}=C_{GD}+C_{GS}$, $C_{oss}=C_{GD}+C_{DS}$ and $C_{rss}=C_{GD}$ are mandatory since they are usually mentioned in a device datasheet as typical parameters related to switching performance.

In addition, complementary to the above, some other partial, internal capacitance parameters can be measured. These are: C_{GD}-V_{GD}, C_{GS}-V_{GS}, C_{GD}-V_{DS}, C_{GS}-V_{DS} and C_{DS}-V_{DS}. From these AC characteristics, the V_{TH} can be extracted again (check whether is equal to the respective value extracted from the transfer measurement), doping profile analysis can be performed and the correctness of the definitions of C_{iss}, C_{oss}, C_{rss} can be demonstrated. The C_{GD} capacitance is also known as Miller capacitance while the C_{DS} very often is considered as negligible and the C_{DS}-V_{DS} graph is not reported. The reason for that is the very small value of the capacitance (in comparison with the two other ones) which demands a very sensitive, noise-isolated measurement setup. Generally, the inter-electrode capacitances of WBG power devices are very small which guarantees fast switching.

During the Capacitance measurements, particular attention must be given to the values of the dissipation factor, while the frequency is usually set to either 100kHz or 1MHz. In general, higher frequency values must be preferred as they prevent the appearance of traps and defects that there are probably within the material.

In figure 31 (left), we can see the C_{iss}, C_{oss}, C_{rss} of one of the best F11 devices. The measurements conditions are in the inset of the graph. The frequency was set at f=1MHz while the gate bias for the measurements with V_{DS} sweep was equal to -15V to ensure the off state of the device.

Let’s take a more careful look to the curves. First of all we observe that all the curves exhibit a descending tense with the V_{DS} rise. Great impression causes the black curve (C_{OSS}) as we observe, beyond the V_{DS} value of around 25V, the values decrease very abruptly reaching 0 at around 30V and continue to negative capacitance values.

The origin of this phenomenon is probably the conduction in the channel leading to the negative values of C_{DS} and consequently of C_{oss}. The latter is demonstrated by the corresponding blocking graph of the transistor of the right. We observe that for V_{GS}=-15V, which holds during the

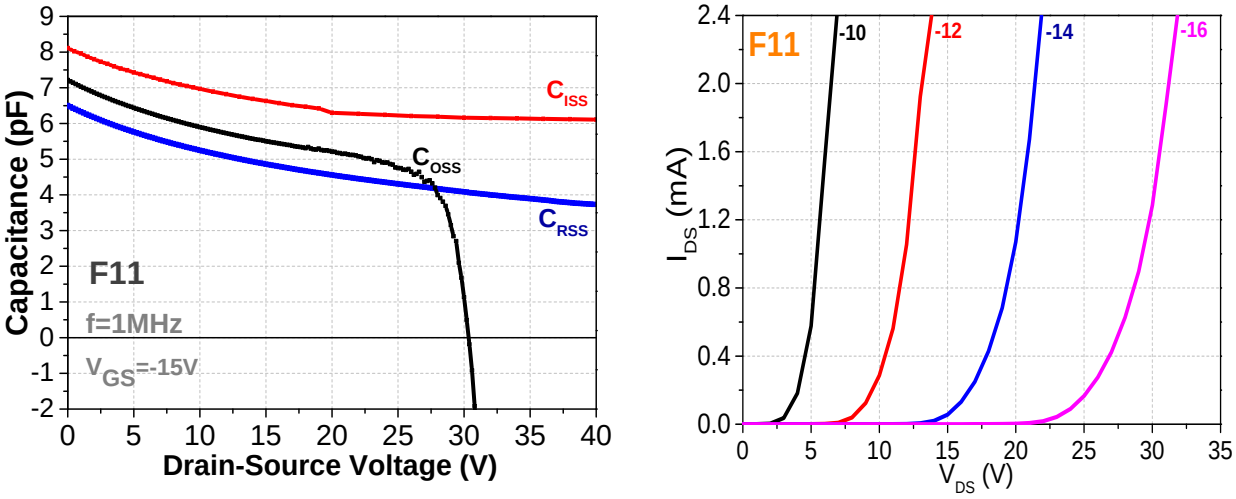


Fig. 4.31: Left- C_{ISS}, C_{OSS}, C_{RSS} measurements at f=1MHz, Right- Blocking characteristics of the device.

capacitance measurements the conduction in the channel is expected to start at around V_{DS}=25V.

The weird phenomenon of the negative capacitance values occurs with the transition to the ON state and the instrument rather measures the inductance of the device. Negative capacitance is usually a sign for strong inductive contributions to the impedance. Capacitive and inductive contributions are exclusive. You can only see one or the other, at least at fixed frequency. One solution for this problem is probably the increase somehow of the resistance (maybe by cooling).

The complementary C-V measurements were also performed for one transistor and they are presented in figure 4.32. Let's take a careful look to the capacitance curves of C_{GD} and C_{GS}. In the figure on the left, we observe the existence of three distinct capacitance behaviors. Using the image of a parallel plate capacitor $\left(C = \frac{\varepsilon_o \varepsilon A}{d}\right)$, with a spacing between the plates *d*, equal to the depleted

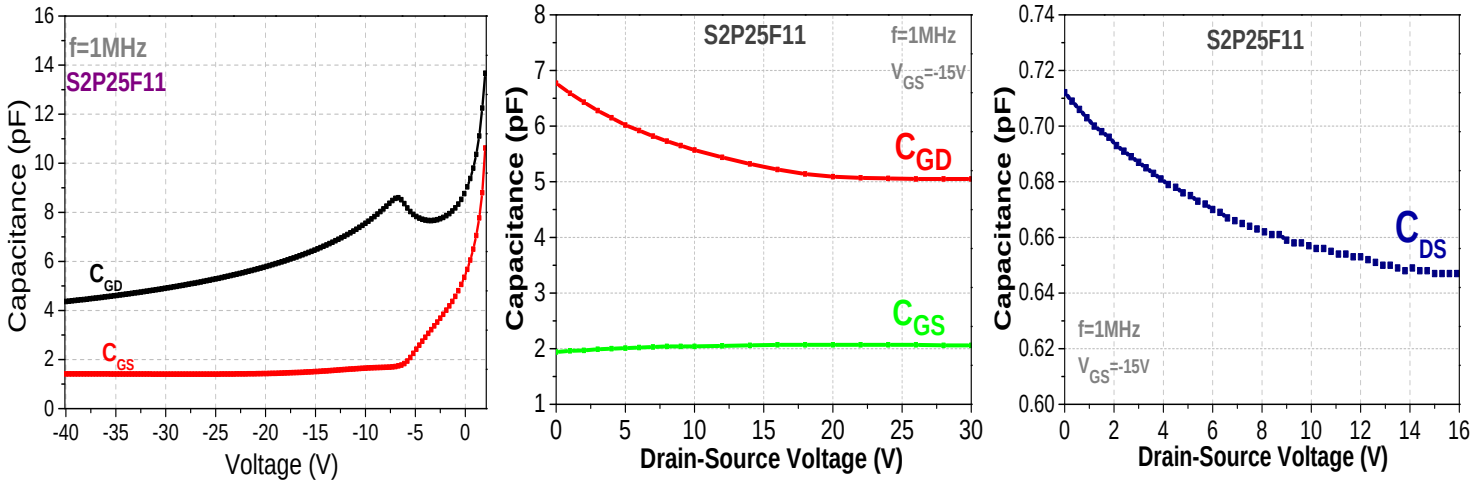


Fig. 4.32: C-V measurements at f=1MHz on the S2P25F11
Left: C_{GD}-V_{GD}, C_{GS}-V_{GS}, Middle: C_{GD}-V_{DS}, C_{GS}-V_{DS}. Right: C_{DS}-V_{DS}

width, is not straightforward as the area involved is not easily determined in all cases. Indeed, the involved depletion edge surface is not flat especially when the depletion is inside or approaching the channel. This can result to a point of inflection in the capacitance curve. The situation can be further complicated when there are two differently doped layers in the drift and channel area resulting also in an inflexion in the capacitance curve.

Particularly:

- *-40 ≤ V_{bias} ≤ ~ -7V range*:

The C_{GD} gradually decreases with the increase of the reverse voltage (absolute value), due to the increase of the depleted portion of the drift region. Indeed, increasing the reverse biasing of the involved diode leads to a consequent increase of the width of the depletion regions. This results to the decrease of the value of the capacitance. Note that C_{GS} remains continuously almost constant at ~1.7pF, because of the fully depleted channel. In addition, it's worthwhile to mention that the C_{GD} takes constantly a higher value than C_{GS} as the corresponding junction area is larger.

- *~ -7V ≤ V_{bias} ≤ ~ -5V range:*

In this area there is a competition between two phenomena, the decrease of the junction-effective-area and the decrease of the width of the corresponding depletion region. When the gate voltage reaches the threshold value around -7V, the channel opens and the gate-drain-junction-effective area decreases. The gate-source-junction-effective area decrease is due to the change of the channel-depletion-area. On the contrary, due to this transition phenomenon, the value of C_{GD} abruptly drops down because of the reduction of the effective area of the plates of the C_{GD} capacitance forming, thus, a peak at around -7V, which is the threshold voltage value.

- ~ -5 ≤ V_{bias} ≤ 2V range:

Both C_{GD} and C_{GS} increase steadily as the change of the corresponding junctions area is not any more important and the decrease of the corresponding depletion regions width is the main factor explaining the capacitance behavior.

According to the results, the V_{TH} value is around -7V, a value verified by the I-V measurements.

For elaborate analysis about the circuitries of C-V measurements, refer to Appendix 1.

As for the diodes, from the transistor C-V measurements the doping profile can be extracted using the equations (1) and (2) presented above in the diodes analysis. Nevertheless, it is more common the doping analysis in a sample to be done based on a diode measurement, as it is a simpler structure where the area of the capacitor can be easier determined, leading to more accurate results.

However we performed the extraction using the measured C_{GD} capacitance with the extracted N_D-W profile shown in figure 4.33. Great coincidence is observed with the respective graph from the diode C-V analysis (inset of right graph, fig. 4.9).

For the extraction, we focused our analysis below the V_{TH} value where the channel is totally pinched off and the depletion regions formed within the transistors extend as shown in figure 4.34 (see also fig. 4.3 (left)). We assume that the measured capacitance is attributed to three different capacitors connected in parallel. That within the channel

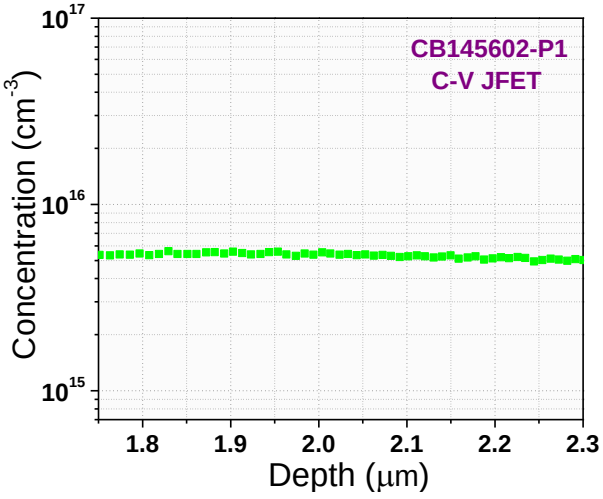


Fig. 4.33: Extracted doping profile.

C_s, that inside the drift region C_{dr} and the third one, due to the rest implanted regions (e.g. gate pad), C_{rest}. Below we see the equations for the capacitances calculation.

$$C_s = \varepsilon_o \varepsilon_r \frac{A_s}{W_s} \text{ , where } A_s = L_{ch} \cdot Z$$

$$C_{dr} = \varepsilon_o \varepsilon_r \frac{A_{dr}}{W_{dr}} \text{ , where } A_{dr} = (W_{ch} + W_G/2 + W_G/2) \cdot Z$$

$$C_{rest} = \varepsilon_o \varepsilon_r \frac{A_{rest}}{W_{rest}}$$

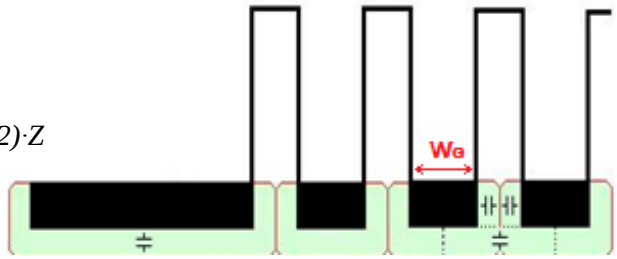


Fig. 4.34: VJFET cross section.

For the analysis, we started from the point that the pinch off occurs, the point that the channel is just strangled by the depletion area around the gates regions. We know that at this voltage the depletion width W is equal to the half width of the device channel ($W_{ch}/2$), namely $W_{rest}=W_s=W_{dr}=W_{ch}/2$. Thus, we can calculate the values of C_{dr} and C_s. C_S remains constant, regardless the further expansion of the depletion regions within the drift layer since the channel is fully depleted. Furthermore, Ag is also constant under threshold voltage.

Anytime, the capacitance contribution from the gate pad and the rest implanted regions of the JFET, C_{rest} is calculated from:

$$C_{rest}=C_{measured}-n\cdot 2\cdot C_s-(n-1)\cdot C_{dr} \qquad \textit{where } n \textit{ is the number of fingers.}$$

Thus at the threshold point, we know $C_{measured}$ from the graph (figure 4.32 (left)) and we easily calculate C_{rest} from the equation above. Since we already know that $W_{rest}=W_{ch}/2$, we can also calculate the area A_{rest}.

Afterwards, for biases more negative than V_{th}, (where C_s remains constant), we define for any applied voltage:

$$C'=C_{measured}-n\cdot 2\cdot Cs$$

N_d can be now calculated from the following equation:

$$N_d = \frac{1}{q\varepsilon_o \varepsilon A^2} \frac{C^3}{dC/dV}$$

where $C=C'$ *and* $A=(n-1)\cdot A_{dr}+A_{rest}$

Of course, the above analysis was feasible since the doping concentration of the channel was equal to the corresponding one of the drift region.

- **High temperature characterization**

Measurements at higher, than the ambient, temperatures are necessary in order to evaluate transistors real operation since in high current operation there is always a self-heating effect. Usually the measured characteristics at elevating temperature are the ON I_{DS}-V_{DS}, the Transfer and the GS characteristics.

For the purposes of on-wafer measurements, the sample must be inserted in a probe station incorporating a thermal chuck the temperature of which is regulated by a temperature controller. It is worthwhile to place a temperature sensor on the chuck in order to measure continuously the temperature on it and avoid a sudden, uncontrolled extreme rise of the temperature which can lead to the damage of the device. The supply of the coolant liquid in the thermal management unit is very important and its level must be checked frequently otherwise if the apparatus run out of it, its operation results to uncontrolled rise of the temperature on the chuck.

Below we can see the utilized equipment available in the electrical characterization lab of Technical University of Crete as well as some photos of the measurements setup and a schematic describing how the thermal management unit operates. The probe station is a Cascade Summit 10600 while the temperature controller is a Temptronic TP03000. For the I-V measurements a DC analyzer HP 4142B is used.

In the case of our sample, high temperature measurements were performed to an F11 transistor. Once the desired steady-state temperature was reached, measurements were taken quickly in order to avoid the self-heating of the device. From the I_{DS}-V_{DS} characteristics of figure 4.36 (left) we observe that the rise of temperature leads to smaller values of ON I_{DS} (negative temperature coefficient-NTC) due to a higher R_{ON} value.

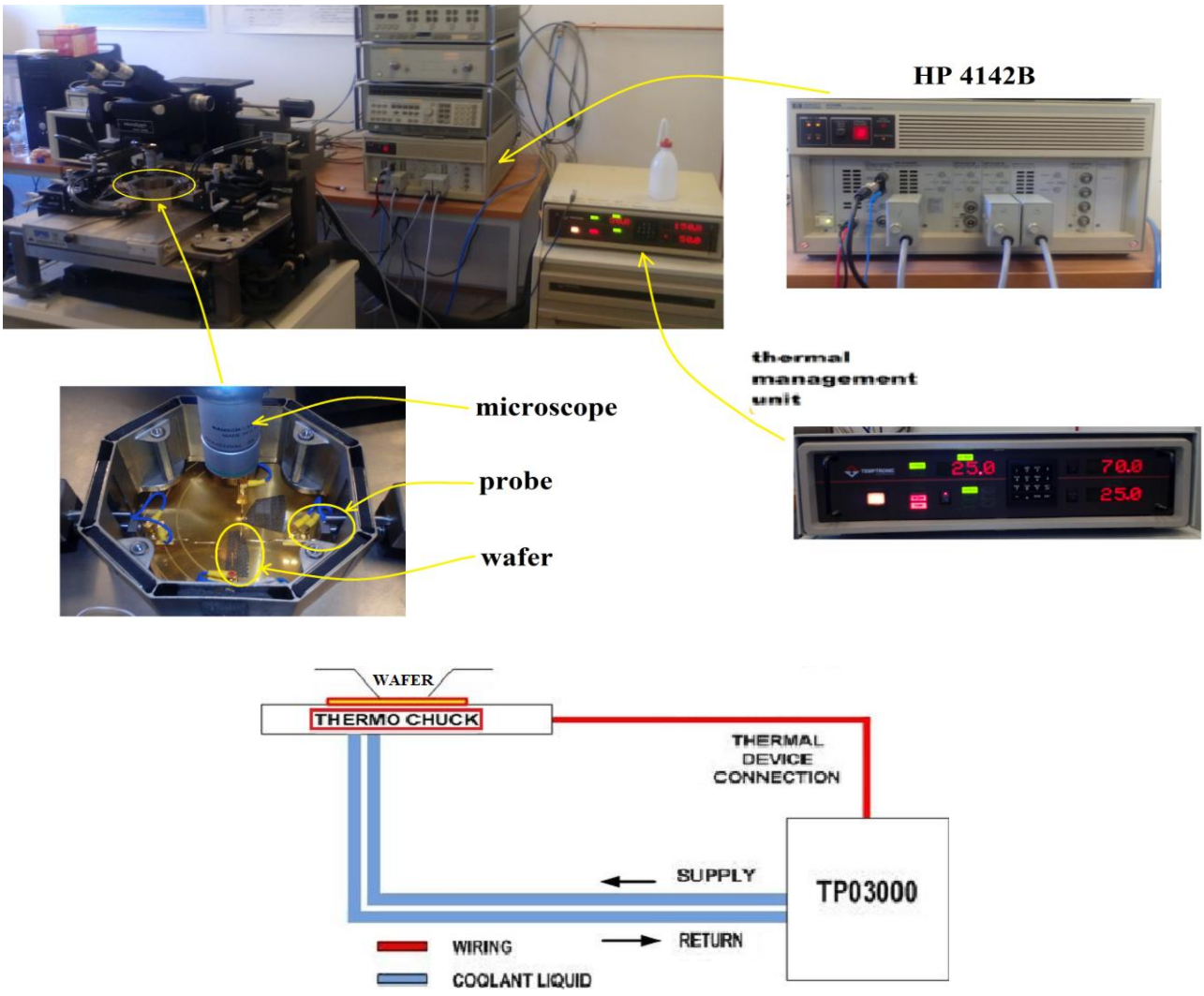


Fig. 4.35: (Top) Photos of the measurement setup,
(Bottom) Schematic of the thermal chuck and the thermal management unit.

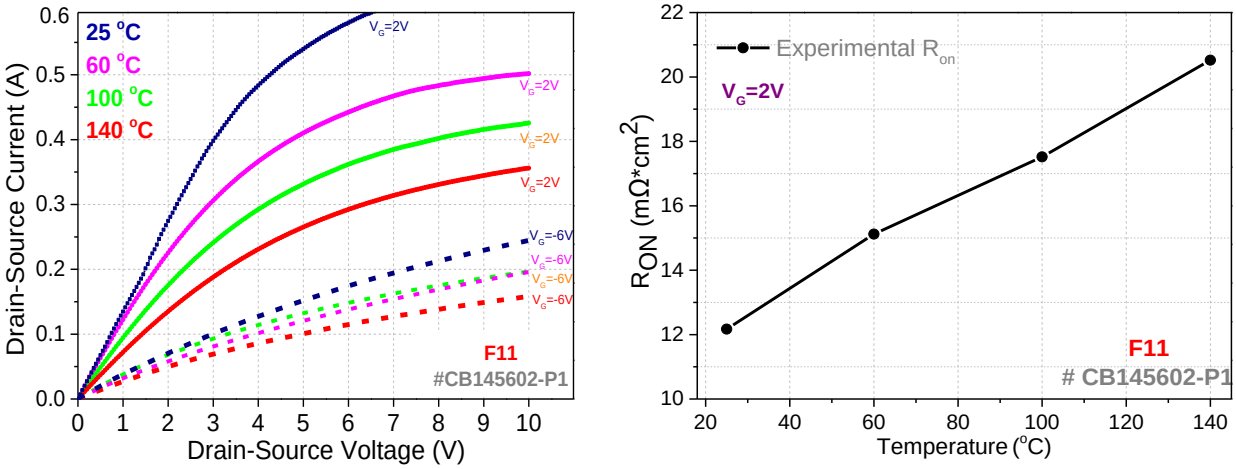


Fig. 4.36: Left: Output ON characteristics. Right: R_{ON} - T characteristic.

The latter is clearly shown on the right of figure 4.36 where the graph R_{ON}-T of the extracted R_{ON} values is presented. The increase of the R_{ON} value is attributed to a lowering of electrons mobility as the temperature increases.

From the transfer characteristics of the transistor, presented in the figure 4.38 we see the shift of the V_{TH} with the temperature rise. As we clearly observe from the V_{TH}-T extracted graph (right) the value of V_{TH} decrease with the rise of the temperature as it was expected according to the theory.

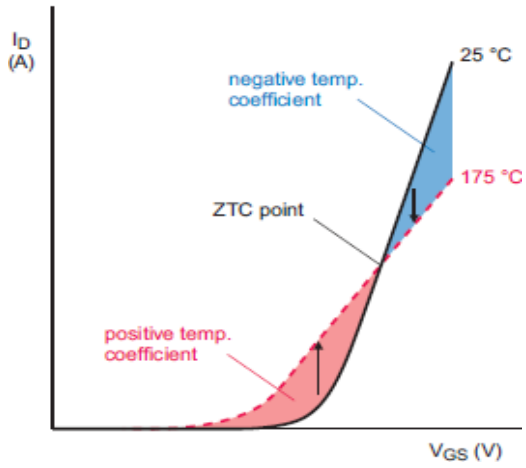


Fig. 4.37: Typical Transfer characteristic.

Furthermore from the transfer characteristics at elevating temperature, the Zero Temperature Coefficient point (ZTC) can be defined. When a JFET is turned on, there are two competing effects that determine how its current behaves with increasing temperature. The first effect deals with the reduction of threshold voltage values as the temperature rises. The JFET is turned on for smaller voltages, thereby increasing the current. In opposition, the resistance increases with increasing temperature, thereby reducing the current. The resistance increase dominates at high currents, meaning that higher temperature leads to lower

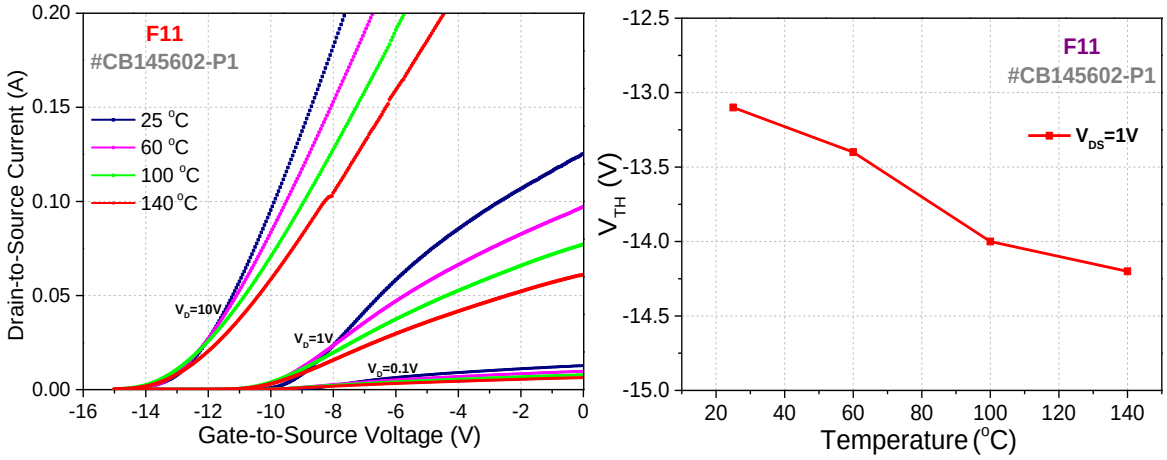


Fig. 4.38: Left- Linear Transfer Characteristics, Right- V_{TH}-T characteristics

currents. The threshold-voltage drop dominates at low currents, as we can clearly see in the transfer characteristics. For a given V_{DS}, there is a critical current below which the I_D exhibits positive temperature coefficient. Above this critical current, the I_D exhibits negative temperature coefficient. This critical current corresponds to the curve point, which is known as the Zero Temperature Coefficient (ZTC) point. The ZTC point is easily defined by the intersection of the temperature curves.

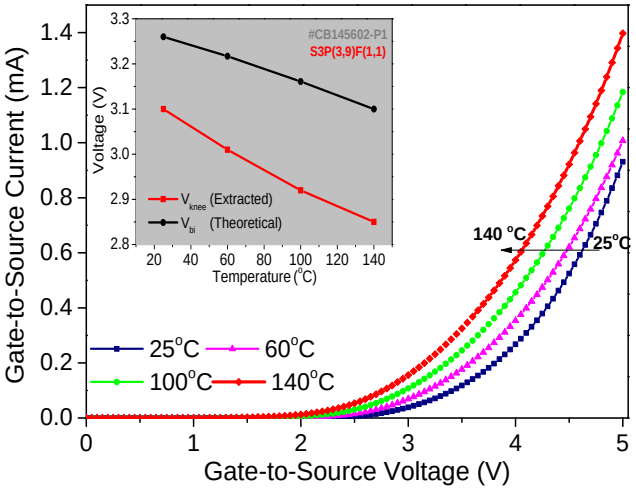


Fig. 4.39: G-S Forward I-Vs of transistor.

For our measurements the reported values follow: for V_{DS}=0.1V → ZTC≈-7.8V, for V_{DS}=1V → ZTC≈-8.2V and for V_{DS}=10V → ZTC≈-12V. The ZTC point is just an indicator for the temperature behavior of the device and is not usually mentioned in the device datasheet.

In figure 4.39 the GS transistor forward graph is presented for temperature values up to 140°C. We observe in the inset of the left graph the temperature dependence of the experimentally extracted V_{knee} values accompanied by the theoretical temperature dependence of V_{bi}. It is obvious that the rise of the temperature leads to smaller values of V_{knee} and V_{bi}. Particularly, the V_{knee} and V_{bi} shifts by 2.4 mV/°C and 1.3mV/°C respectively.

- **Blocking DC I-Vs in fluorinert**

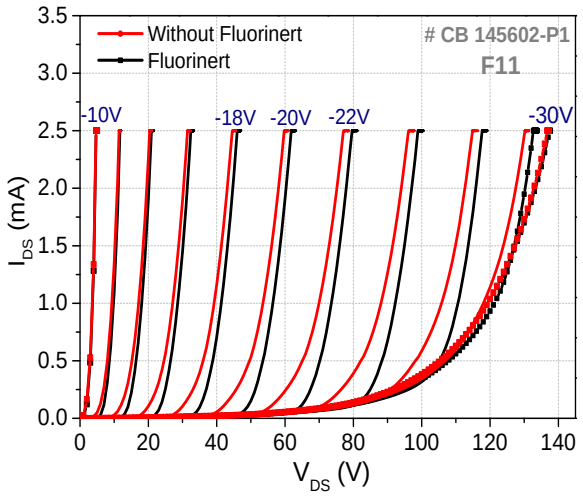


Fig. 4.40: Blocking I-Vs with and without fluorinert.

Testing in fluorinert must be performed for evaluating the max blocking characteristics, because it prevents the current leakage from the surface of the device. The *breakdown voltage* should be determined at low reverse current to avoid self-heating. A rule of thumb is to not make the measurements at a power density higher than 500W/cm^2.

If the deviation between the on air (without fluorinert) curve and the in fluorinert is great that means that the surface leakage currents are prominent.

Beside we can see this measurement performed for one of the best F11 devices with a (slightly) higher observed breakdown voltage values with fluorinert than the respective without. The same trend was noted for all the measured best devices.

Choice of the best diodes

Determining the best diodes is not a priority. The main information to obtain from the best diodes is the breakdown voltage, which is an upper limit for the corresponding transistors. The main criterion for the choice will be the leakage current @200V. Then, the existence or not of double barrier and the V_{knee} values follow in importance. The V_{knee} values for SiC diodes must be around 2.5V. Not much smaller, not much higher than this value. As in the case of the best transistors, a deeper analysis must be eventually performed on these 5 best diodes.

We did not proceed to such an analysis for our sample because we were interested rather in the transistors than the diodes, because such a device we are trying to develop for the incorporation in an inverter. Besides this was the basic motivation for this work.

However, below the last set of measurements that must be performed on the best diodes are presented. The graphs are from measurements on random devices and are indicative.

- **Reverse I-V measurements in fluorinert**

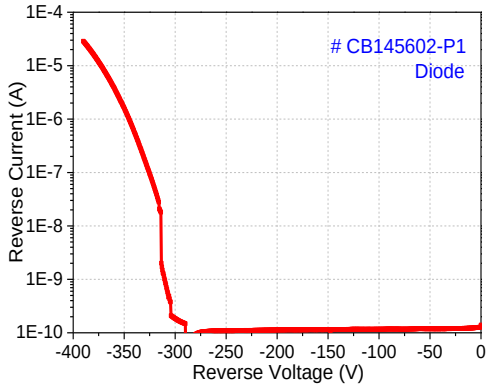


Fig. 4.41: Reverse measurement of diode.

Additional reverse measurements must be performed in fluorinert in order to evaluate the ultimate breakdown voltage values (if they are higher, in absolute values than 200V) of the device. The breakdown voltage should be determined at low reverse current to avoid self-heating of the diode. Therefore the voltage step must be set to a rather high value (e.g. 0.5V) in order to avoid the stress of the diode and the consequent self-heating which leads to degraded performance. The current compliance must be set in a value that serves the power compliance of 500W/cm^2.

- **High temperature characterization**

High temperature measurements must be performed in order to evaluate diodes real operation since in high current operation there is always a self-heating effect. From figure 4.42 where forward

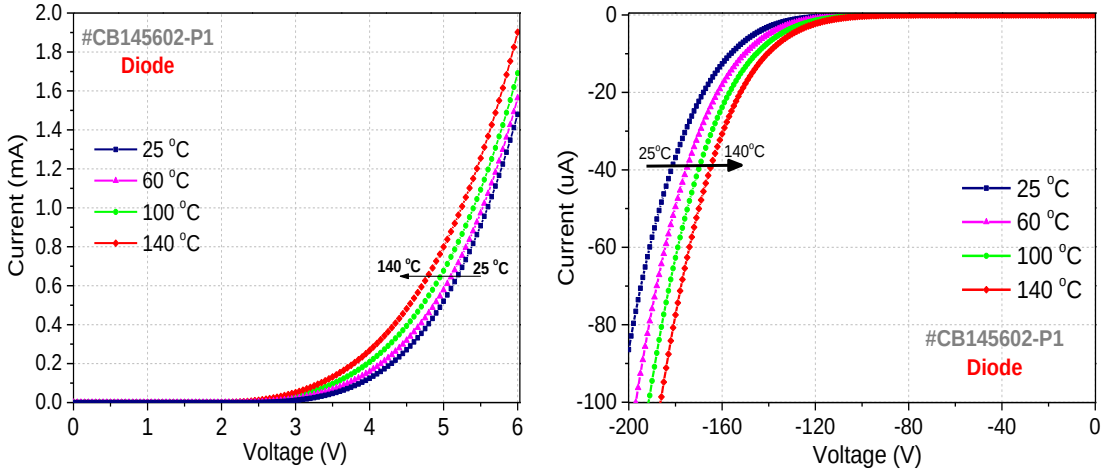


Fig. 4.42: Forward and Reverse DC Diode Characteristics

and reverse characteristics of the diode are presented, we observe how the curves deviate with the rise of the temperature. The reverse behavior of the diode deteriorates with the increase of the temperature, while the rise of temperature leads to smaller V_{knee} values. During the reverse measurement the room lights must be switched off in order to observe, as the reverse current increases, if a light spot turn up on the diode.

4.6 Specifications tables

By the end of the electrical characterization of a processed sample, all the investigated, measured and extracted parameters (specifications), must be gathered in one summarizing table, the specifications (specs) table. The construction of the latter is very important as it summarizes the great amount of the extracted information from the electrical characterization in a way that one can refer to it and find easily any of the sample parameter without reading the whole sample's measurements report. The conditions under which the parameter is measured as well as its unit must be explicitly mentioned. The reported value of the parameter can be the mean value of the five best devices measured in the last stage of the characterization.

It must be mentioned at this point that the specs table constructed by the end of the on-wafer electrical characterization of a sample is not the same as the specs table involved in a packaged device datasheet. The reason is the different goals that they serve, since the first one provide information mainly from the fabrication point of view and is addressed to process engineers while the second one is directed rather at electronic engineers. Therefore after the packaging of a sample's device (usually the best one), additional measurements/extractions and calculations have to be performed in order to fill the specs table of the packaged device datasheet.

Below we can see the specs tables for all the different under investigation devices from the sample CB145602-P1. These tables summarize the whole work that has been done for the characterization of it. The specs table of F11 transistor is extensive and involves several information because this transistor exhibited by far better behavior than the other ones of the wider mesa widths. It is something somehow expected in terms of the material, because the possibility of a defect in the material increases with the increase of the mesa width. For the latter ones the specs tables provide basic information since the interest for them is not very intense due to their not good behavior.

(T=25^{O}C unless otherwise specified) **F11** (W_{nom}=1.5um)

Parameter	Symbol	Conditions		Value	Unit
Maximum Ratings					
Max Pulsed Drain Current	I_{DPmax}	V_{GS}=2V, V_{DS}=V_{Dsat}		**0.9**	A
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*		**-13.5**	V
Off Characteristics					
Drain-Source Blocking Voltage	BV_{DS}	V_{GS}=-28V, I_{DS}= 2mA		**125**	V
Leakage Current	I_{leak}	V_{DS}=0V,V_{GS}=-28V		**38.5μ**	A
		V_{DS}=0V,V_{GS}=V_{TH}		**20.4μ**	
		V_{DS}=200V,V_{GS}=-28V		∞	
Gate Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=V_{th}-20V		**-11.6μ**	
		V_{DS}=200V, V_{GS}=-10V		∞	
Voltage Gain	μ	V_{DS}=100V, I_{per}=0.1mA/mm		**4.1**	-
ON Characteristics					
Drain-Source On-resistance	R_{ON}	V_{GS}=0V		**9.1**	Ω
				6.3	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V		*6.4*	V
		V_{DS}=1V		*6.1*	
Gate Forward Current	$I_{G,FWD}$	V_{GS}=2V		**3.39μ**	A
Knee Voltage	V_{knee}	-		**2.3**	V
Dynamic Characteristics					
Input Capacitance	C_{iss}	V_{GS}=-16V f=1MHz, osc. level=100mV	V_{DS}=0V	**8.5**	pF
			V_{DS}=40V	**6.5**	
Output Capacitance	C_{oss}		V_{DS}=0V	**7.7**	
			V_{DS}=40V	**-**	
Reverse Transfer Capacitance	C_{rss}		V_{DS}=0V	**6.5**	
			V_{DS}=40V	**3.9**	

(T=25^{O}C unless otherwise specified) **F31** (W_{nom}=2um)

Parameter	Symbol	Conditions	Value	Unit
Maximum Ratings				
Max Pulsed Drain Current	I_{DPmax}	V_{GS}=2V, V_{DS}=V_{Dsat}	**1.05**	A
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*	**-15**	V
Off Characteristics				
Drain-Source Blocking Voltage	BV_{DS}	V_{GS}=-34V, I_{DS}= 2*mA*,	**61**	V
Leakage Current	I_{leak}	V_{DS}=200V,V_{GS}=-34V	∞	A
ON Characteristics				
Drain-Source On-resistance	R_{ON}	V_{GS}=0V	**16**	Ω
			11.1	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V	**-13.3**	V
Knee Voltage	V_{knee}	-	**2.3**	V

(T=25^{O}C unless otherwise specified) **F12** (W_{nom}=2.5um)

Parameter	Symbol	Conditions	Value	Unit
Maximum Ratings				
Max Pulsed Drain Current	I_{DPmax}	V_{GS}=2V, V_{DS}=V_{Dsat}	**1.2**	A
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*	**-17.9**	V
Off Characteristics				
Drain-Source Blocking Voltage	BV_{DS}	V_{GS}=-40V, I_{DS}= 2*mA*,	**47**	V
Leakage Current	I_{leak}	V_{DS}=200V,V_{GS}=-40V	∞	A
ON Characteristics				
Drain-Source On-resistance	R_{ON}	V_{GS}=0V	**13.2**	Ω
			9.2	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V	**-22.1**	V
Knee Voltage	V_{knee}	-	**2.5**	V

(T=25^{O}C unless otherwise specified) **F32** (W_{nom}=3um)

Parameter	Symbol	Conditions	Value	Unit
Maximum Ratings				
Max Pulsed Drain Current	I_{DPmax}	V_{GS}=2V, V_{DS}=V_{Dsat}	**1.4**	A
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*	**-11.2**	V
Off Characteristics				
Drain-Source Blocking Voltage	BV_{DS}	V_{GS}=-40V, I_{DS}= 2*mA*,	**13**	V
Leakage Current	I_{leak}	V_{DS}=200V,V_{GS}=-40V	∞	A
ON Characteristics				
Drain-Source On-resistance	R_{ON}	V_{GS}=0V	**16.1**	Ω
			11.2	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V	**-29.3**	V
Knee Voltage	V_{knee}	-	**2**	V

(T=25^{O}C unless otherwise specified) **F42** (W_{nom}=3um, **#n=121**)

Parameter	Symbol	Conditions	Value	Unit
Maximum Ratings				
Max Pulsed Drain Current	I_{DPmax}	V_{GS}=2V, V_{DS}=V_{Dsat}	**2.1**	A
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*	**-7**	V
ON Characteristics				
Drain-Source On-resistance	R_{ON}	V_{GS}=0V	**196**	Ω
			136	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V	**-**	V
Knee Voltage	V_{knee}	-	**1.9**	V

(T=25^{O}C unless otherwise specified) **F23** (W_{nom}=4um)

Parameter	Symbol	Conditions	Value	Unit
Maximum Ratings				
Max Pulsed Drain Current	I_{DPmax}	V_{GS}=2V, V_{DS}=V_{Dsat}	**1.43**	A
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*	**-16.9**	V
ON Characteristics				
Drain-Source On-resistance	R_{ON}	V_{GS}=0V	**8.9**	Ω
			6.2	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V	**<-40**	V
Knee Voltage	V_{knee}	-	**2.5**	V

(T=25^{O}C unless otherwise specified) **F33** (W_{nom}=5um)

Parameter	Symbol	Conditions	Value	Unit
Maximum Ratings				
Max Pulsed Drain Current	I_{DPmax}	V_{GS}=2V, V_{DS}=V_{Dsat}	**1.6**	A
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*	**-14**	V
ON Characteristics				
Drain-Source On-resistance	R_{ON}	V_{GS}=0V	**30.7**	Ω
			21.3	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V	**<-40**	V
Knee Voltage	V_{knee}	-	**2.4**	V

By studying carefully the tables, we can summarize the performance of the sample devices in the following basic conclusions.

- Low quality of Gate-Source junction for all the transistors, especially for the reverse regime where low BV_{GS} values were reported. Consequent high values of G-S leakage current.
- Increase of the max pulsed Drain current (I_{DPmax}) with the increase of the mesa width or the area of the device (F42) but relatively low values.
- Very low blocking capability with the BV_{DS} values being except for the F11, lower than 100V.
- R_{on} values in the moderate range.

From the above, we deduce that the devices of the processed sample are away from the desired specifications for our application, therefore a new fabrication effort must be done with improved and more precise fabrication procedure and maybe new optimized structure.

4.7 Conclusions

In this chapter the typical measurements procedure that must be followed for the elaborate on wafer electrical characterization of a sample was minutely presented. Simultaneously the results of the electrical characterization of the sample CB145602-P1 were presented. From them, we observed that there are many fields (e.g. the blocking capability) where the performance of the JFETs must be optimized. For that reason a second effort has been done with the run of a new sample, the CB145602-P4 where some modifications have been done rather to the design of the device than the followed fabrication process. The characterization of the sample will reveal if we managed to vanish the observed malfunctions and get acceptable overall behavior from the JFETs. In the next chapter, this new sample is investigated elaborately.

Chapter 5. Measurement results from sample CB145602-P4

Due to the low performance that the first sample exhibited in some fields, a second one was decided to be fabricated in a new run, featuring some differentiations. The main modification that was adopted is the deeper implantation of the gate regions which now equals to 1.1um. Let us remind that for the first sample the implantation depth was equal to 0.3um.

In this chapter the measurements results from the electrical characterization of the second under investigation sample, the CB145602-P4 are presented. The proper measurements procedure, described in the previous chapter has been followed.

5.1 Transistor geometry determination.

The mask layout is the same as for the first sample CB145602-P1. Below we can see the dimensions, the shape and a photo of the processed sample which consists of 20 periods.

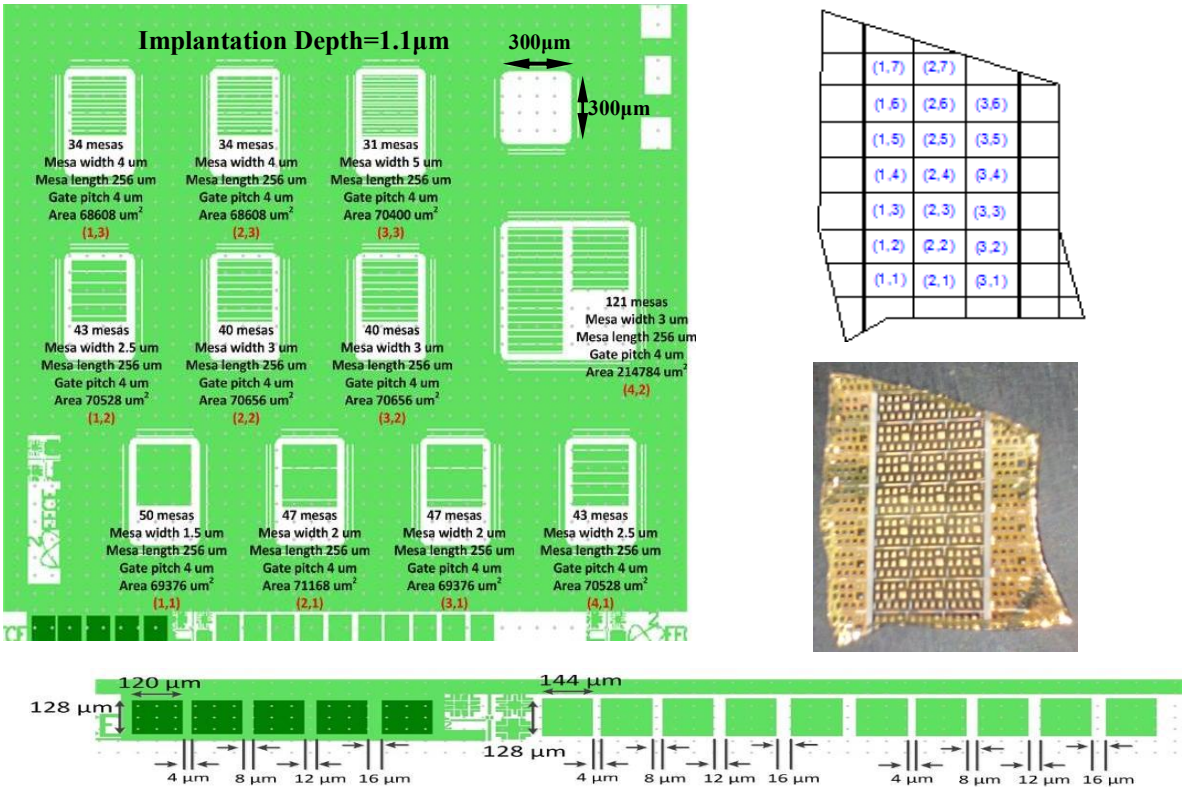


Fig. 5.1: Top left: Period of the mask. Top right: Schematic and photo of the processed sample. Bottom: TLM patterns for both n-type (on the left) and p-type contacts (on the right).

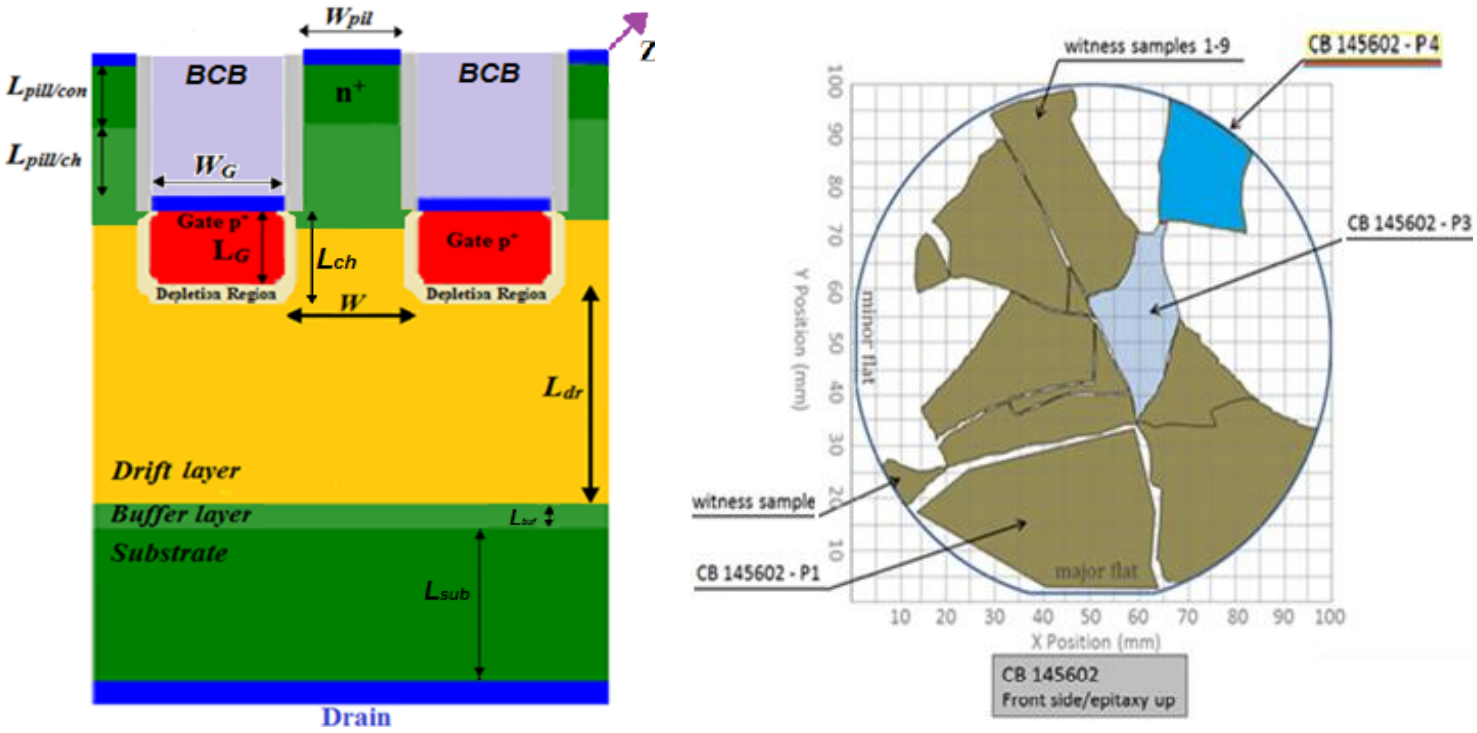


Fig. 5.2: <u>Right:</u> Position of CB145602-P4 on the 4-inch 4H-SiC wafer slice <u>Left:</u> Important dimension parameters shown.

- L_{dr}=7.1 (8-0.9) μm,
- $L_{channel}$= 1.9μm (gate length (1.1)+V_{bi} depletion width (0.8)),
- L_p=2μm (1+1)

Above we see the placement of the processed piece on the initial 4H-SiC wafer. By observing again the figure 3.1 we see that no defects were detected in that region. In this way, possible malfunctions and bad behavior of the devices must be attributed rather to the processing procedure than the material. Important dimensions are also obvious on the cross section on the right.

Below SEM images from different fabrication steps are presented.

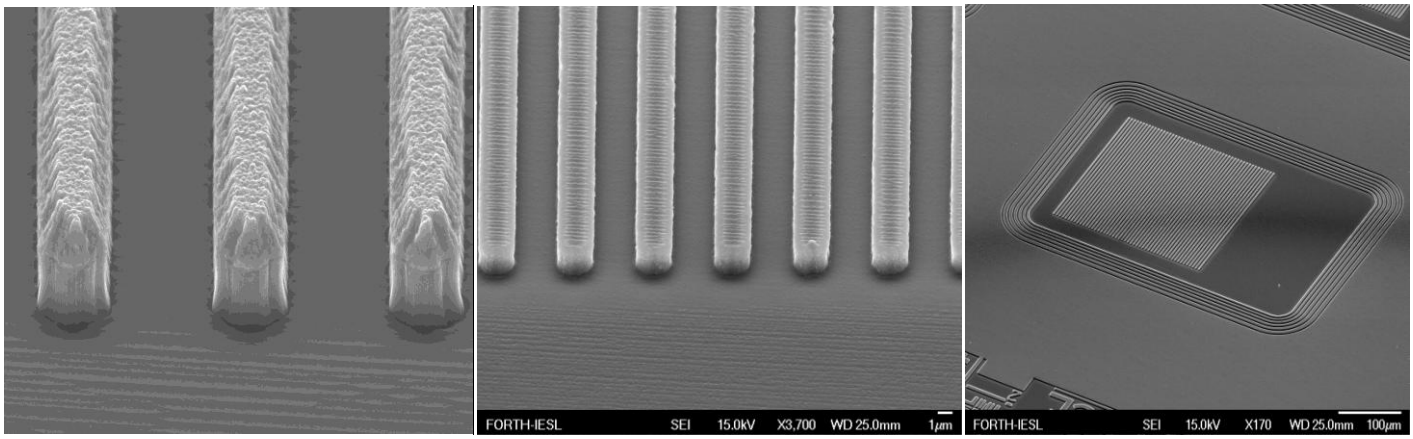


Fig. 5.3: SEM images <u>Left</u>- after the RIE etching for source finger formation. <u>Middle-Right</u>- after 3 hours oxidation.

The main modification adopted in this sample, as has been already mentioned, is the different implantation depth. Moreover the etching for the formation of the trenches has stopped at 2um depth (the respective depth for the first sample was equal to 2.5um). In this way, as we can see from the cross section graph, the channel consists of 2 different doping concentrations. In depth of 0.2μm the doping is 1E+16 cm^{-3}, whilst for the rest 0.9μm is the same as the doping of the drift region namely 1E+15cm^{-3}.

Important values in dimensions and doping of different parts of the device are shown below.

ρ_{sub} (Ω•cm)	L_{sub} (μm)	L_{buf} (μm)	N_D (cm^{-3}) buffer	L_{drift} (μm)	N_D (cm^{-3}) drift	L_{chan} (μm)	
0.021	372	1	1.00E+18	7.1	5.00E+15	1.9	
$L_{pill/ch}$ (μm)	N_D (cm^{-3}) pillar/chan	$L_{pill/con}$ (μm)	N_D (cm^{-3}) pillar/cont	Gate length L_G (μm)	N_A (cm^{-3}) gate	N_D(cm^{-3}) channel	
1	1.00E+16	1	1.00E+19	1.1	1.00E+19	1E+16 (0.2μm) 5E+15 (0.9μm)	
Channel width W=2a(μm)	N_{fing}	Gate pitch W_G (μm)	$R_{cont.}$ ($\Omega \cdot cm^2$)	Pillar width W_{pil} (μm)	L_{pillar}	Z (μm)	W_{GR} (μm)
2/2.5/3/3.5/4.5/5.5	50/47/43/40/34/31	3.5	0.0001	W-0.45	2μm	256	3.5
W_{bus} (μm)	W_1 (μm)	W_2 (μm)	W_3 (μm)	W_4 (μm)	W_5 (μm)	W_6 μm)	
13.75	3	3	3.5	4	4.5	6	

* * **L_{chan}=1.9μm** (gate length/implantation depth (1.1 μm)+V_{bi} depletion width (0.8μm))

In the table above W, W_G, W_1,W_2, …, W_6, W_{GR} are the actual dimensions calculated after the observation on the SEM photos. From the observation on them we concluded that the W and the W_1, W_2, …, W_6 in comparison with the mask dimensions, are increased approximately by 0.5μm and consequently the W_G and W_{GR} are approximately minus 0.5μm. Like the case of the first sample the available SEM photos were few, so we have to keep a prejudice on the actual dimensions.

Since the mask layout is the same, the active area, active perimeter as well as the Total finger area take the same values as for the first sample.

5.2 Theoretical values estimation of parameters

In the following table we can see the theoretically expected parameters values of all the different transistors of CB145602-P4 sample at RT (300K). Refer to Appendix 2 for the utilized equations.

Table of Parameters Theoretical Values

F	*W (μm)*	*W_G (μm)*	Source Area (10^{-4} cm^2)	Active Area (10^{-4} cm^2)	*V_G=0V*		*V_G=2V*		V_{TH} (V)	R_{sh} (Ω/sq) [con. layer]	R_{sh} (Ω/sq) [G layer]	BV_{GS} @RT (V)
					(Ω)	(mΩ*cm^2)	(Ω)	(mΩ*cm^2)				
11	*2*		*1.92*	*6.94*	**11.1**	**7.68**	**6.39**	**4.44**	**-2.53**			
21	*2.5*		*2.41*	*7.12*	**6.95**	**4.95**	**5.3**	**3.77**	**-5.65**			
31	*2.5*		*2.41*	*6.94*	**6.95**	**4.82**	**5.3**	**3.67**	**-5.65**			
41	*3*		*2.75*	*7.05*	**5.9**	**4.16**	**4.91**	**3.46**	**-9.46**			
12	*3*		*2.75*	*7.05*	**5.9**	**4.16**	**4.91**	**3.46**	**-9.46**			
22	*3.5*	*3.5*	*3.07*	*7.07*	**5.3**	**3.75**	**4.62**	**3.26**	**-13.96**	***79.6***	***72.4***	***322***
32	*3.5*		*3.07*	*7.07*	**5.3**	**3.75**	**4.62**	**3.26**	**-13.96**			
13	*4.5*		*3.48*	*6.86*	**4.81**	**3.3**	**4.39**	**3.01**	**-25.03**			
23	*4.5*		*3.48*	*6.86*	**4.81**	**3.3**	**4.39**	**3.01**	**-25.03**			
33	*5.5*		*3.97*	*7.04*	**4.35**	**3.06**	**4.06**	**2.86**	**-38.87**			
42	3.5		9.29	*21.48*	**1.75**	**3.76**	**1.53**	**3.28**	**-13.96**			

Table of Resistance Theoretical Values (R)

mesaW (*μm*)	*#n*	$R_{cont.D}$ (Ω)	R_{sub} (Ω)	R_{buf} (Ω)	R_{drift} (Ω)	$R_{ch.}^{1}$ (Ω)	$R_{ch.}^{2}$ (Ω)	$R_{pil.}^{1}$ (Ω)	$R_{pil.}^{2}$ (Ω)	$R_{cont.S}$ (Ω)	**R_{ON} (Ohm)**
2	*50*	0.142	1.11	0.003	3.70	4.860	0.53	0.300	0.003	0.390	11.1
2.5	*47*	0.139	1.08	0.003	2.85	2.298	0.36	0.255	0.003	0.332	6.95
3	*43*	0.140	1.09	0.003	2.51	1.612	0.29	0.233	0.002	0.302	5.9
3.5	*40*	0.140	1.09	0.004	2.29	1.275	0.24	0.215	0.002	0.280	5.3
4.5	*34*	0.111	0.86	0.003	1.62	0.759	0.16	0.152	0.002	0.198	4.81
5.5	*31*	0.106	0.82	0.003	1.44	0.607	0.13	0.134	0.001	0.173	4.35
3.5	*121*	0.046	0.36	0.001	0.76	0.421	0.08	0.071	0.001	0.093	1.75

For the contact resistances $R_{con,D}$ and $R_{cont,S}$ the common value of 10^{-4} Ohm·cm^2 has been used.

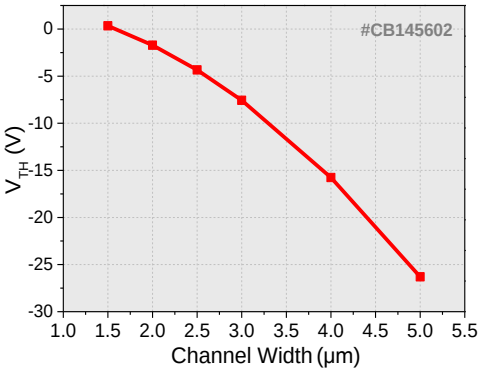


Fig. 5.4: V_{TH} dependence on channel width.

In the last table, a detailed analysis of the R_{on} is presented. We can see all the individual resistance values which constitute the R_{on}, expressed in Ohms. The values are calculated for V_{GS}=0V. In the graph beside we see the theoretical dependence of V_{TH} on channel width.

5.3 First run of measurements in one mask period

The period **P15** was selected for the first run of measurements as the involved devices seem to have good morphology.

Measurements of TLM patterns

The TLM patterns on n-type material were not operational due to a mask-design problem. The measurements on the p type TLMs revealed a bad behavior of the patterns, thus the analysis did not proceed further.

Measurements of single diodes

The extracted parameters from the measurements on the unique diode of the period are shown below. The *differential resistance* R_{diff} is determined at V=4V and 5V since the forward current density values of 10A/cm^2 (6.9mA) and 40A/cm^2 (27.8mA) are not reached.

- $V_{knee}= V_{min}=2.1V$,
- *No Double Barrier*,
- $I_{leak}=-4.36\ x10^{-8}$ *A* (@200V),
- $R_{diff}= 283286\ \Omega$ *(@4V),* $R_{diff}=757576\ \Omega$ *(@5V).*

Fig. 5.5 shows the results of the C-V measurement, and subsequent analysis, performed with the frequency set at f=1MHz. In the inset of the $1/C^2$-V graph we can see the extracted N_d-W figure.

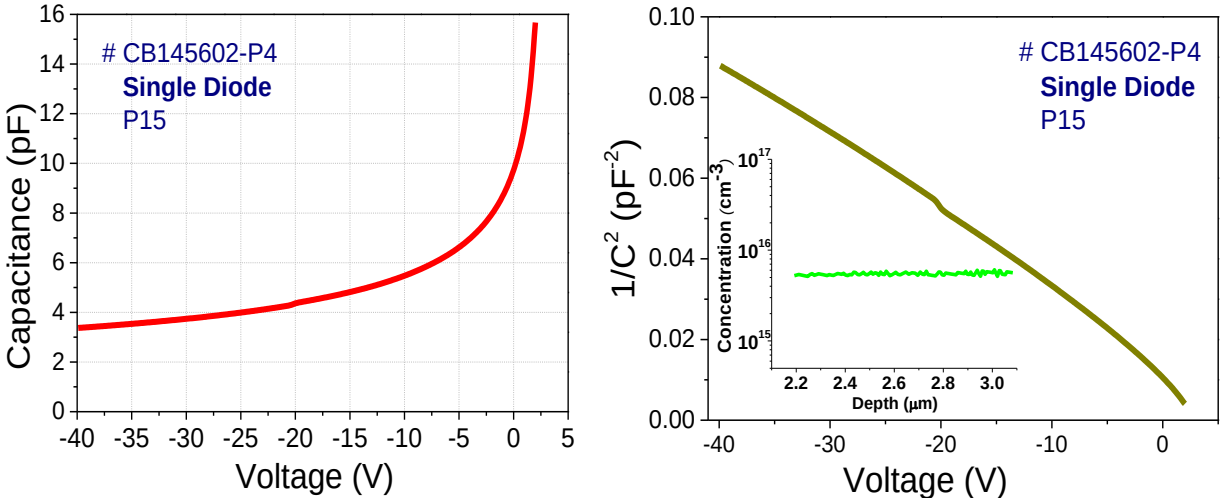


Fig. 5.5: C-V (left) and $1/C^2$(V) (right) characteristics of the single pn diode measured at f=1MHz. Doping profile f the base of 4H-SiC diode calculated from C-V, shown in the inset.

Measurements of transistors

The results from the different measurements for all the involved in the period transistors are summarized below:

- The majority of the extracted from these measurements R_{on} values were around $10m\Omega \cdot cm^2$ while only one value was abnormally very high.
- All the transistors exhibited no double barrier, but the V_{knee} values were lower than 2V. Concerning the reverse regime, the measured BV_{GS} values were characterized by high dispersion. Particularly the lowest value was equal to -0.6V while the highest was greater than -100V.
- The extarcted V_{th} values for V_{DS}=0.1V have deviation from the theoretically expected ones. It is worthwhile to mention that the F11 transistor exhibited normally-off behavior.
- All the involved in the period transistors exhibited such a behavior that allow us to conclude that the OFF state is achievable.
- We saw that the narrower the mesa width of the transistor was, the better was the blocking behavior of the device. It is notable that the F11 device exhibited (the highest) voltage gain value equal to 41. Moreover we must mention that 6 (F12, F22, F32, F13, F23, F33) among the 11 involved transistors had no voltage capability at all.

5.4 Measurements in different mask periods – Statistical study

One transistor for each different mesa (channel) width was selected as DUT in a way that 7 from the 11 involved transistors in the period were measured in several periods. This extensive statistical study helped us to draw many conclusions which are reported subsequently, and define the best devices for the last electrical characterization stage. Below, the elaborate study for one transistor, the first one, is presented for time saving. Moreover, that was the most interesting device in the study of the previous stage. The periods in the mapping graphs without color were not measured for various

reasons (sample edge, problematic measurements etc). Since the sample is a small one, all the periods of our sample were examined, thus the statistical sample was equal to 20 devices.

Statistical study has been also performed for the TLMs and the diodes of the sample but are not presented as they are out of the scope of our application.

➢ Transistors

Gate-Source characteristics:

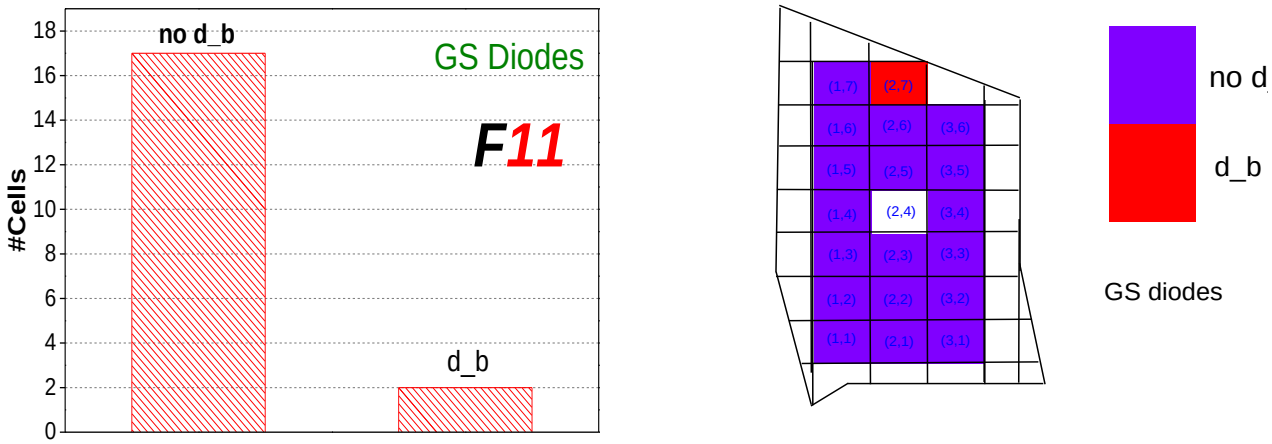


Fig. 5.6: Histogram (left) and mapping (right) of the existence or not of a double barrier in the GS diode.

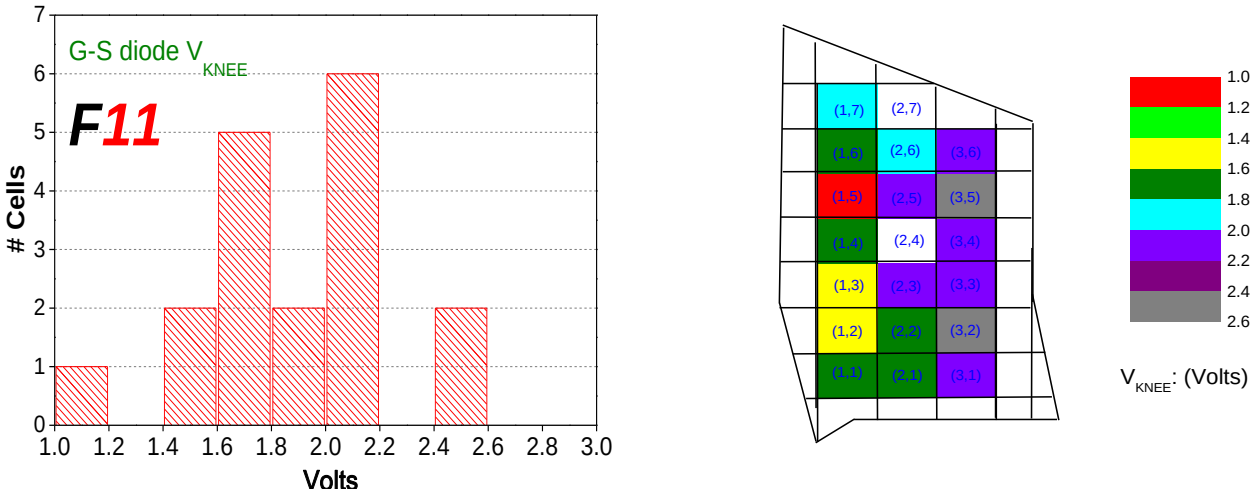


Fig. 5.7: Histogram (left) and mapping (right) of the gate-source-diode knee voltage.

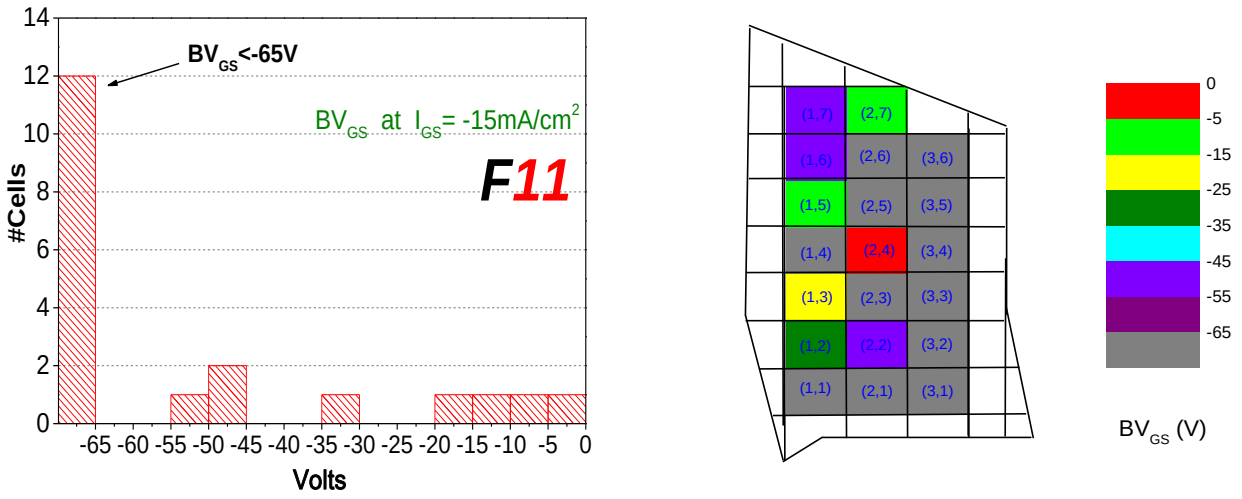


Fig. 5.8: Histogram (left) and mapping (right) of the gate-source-diode BV_{GS}

- We observe that as the mesa width increases, more devices are detected with double barrier. It's remarkable that for the F11 (narrowest) transistor only one device was detected with double barrier while for the last two JFETs F23 and F33 (widest), half the measured devices exhibited double barrier.
- Although, for a SiC diode the expected V_{knee} value is higher than 2V, many values lower than this value were reported.
- As for the BV_{GS} values namely the quality of the GS junction in the reverse regime, undoubtedly is much improved in comparison with the first sample CB145602-P1 since for all the devices many high (absolute) values were measured while for this first sample P1 the majority of the BV_{GS} values are placed in the first ten of the reverse voltage axis. It is noteworthy that more than half the F11 devices did not reach the current limit value (10.5µA) up to -65V bias, the limit of the measurement range. Thus we can deduce the satisfactory overall performance of the GS junction, which is usually a very challenging and critical fabrication step. The latter is reinforced by the results about the existence of double barrier.

By checking in the same time the BV_{GS} and the double barrier characteristics, we observed that the devices with high BV_{GS} values were also detected without double barrier.

Drain-source ON characteristics:

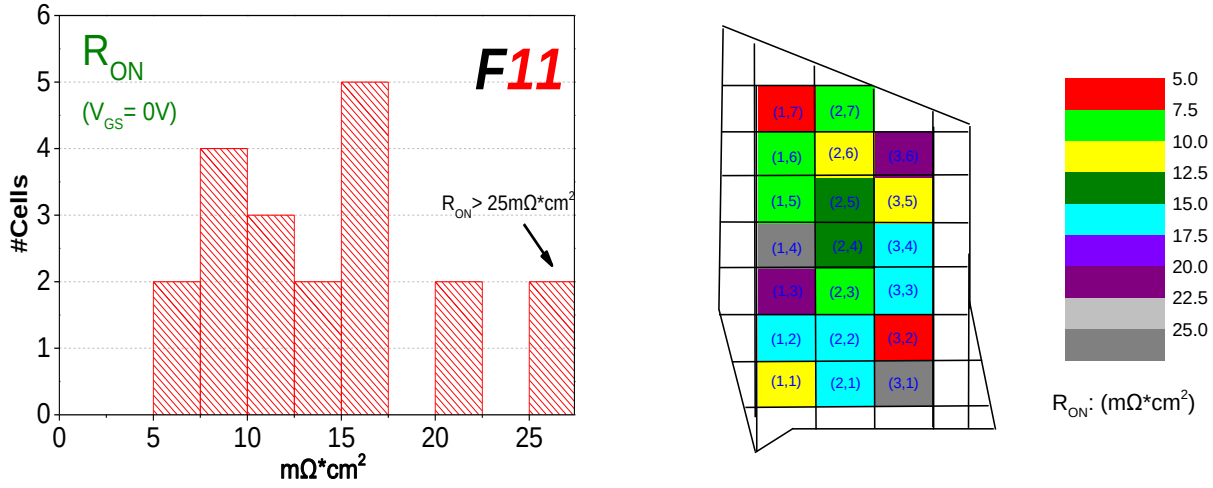


Fig. 5.9: Histogram (left) and mapping (right) of the transistors R_{ON}.

- We observe that the majority of the Ron values for the transistor F11 are higher than 10mΩ·cm^2, but generally the reported for all the under test devices values were mainly around 10mΩ·cm^2. The great improvement in comparison with the sample CB145602-P1, is that no extreme values at all have been reported and even the higher ones were lesser than 50mΩ·cm^2, entirely unlike the first sample. So we can deduce that the largest part of the transistors exhibit good behavior and they have satisfactory low Ron values. Moreover, from the mapping graphs, although the sample dimensions are small we see some spatial dependence with the lower Ron values measured from transistors placed on the bottom side of the sample. No dependence of the R_{on} on the existence of double barrier or the BV_{GS} was noticed.

Transfer characteristics:

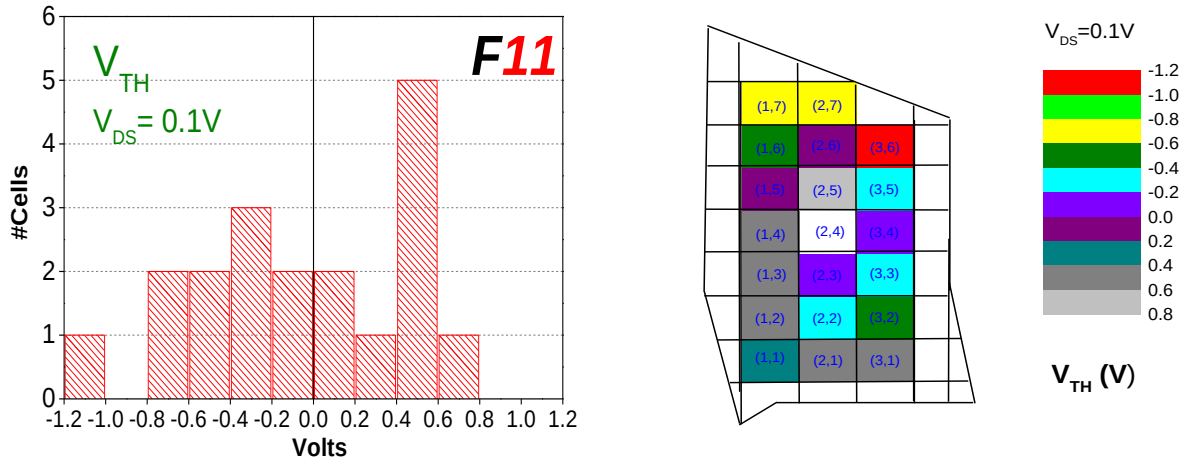


Fig. 5.10: Histogram (left) and mapping (right) of the transistors V_{TH}.

- We observe that the values are placed in a range of 2V. The same trend was observed for all the devices with the majority of the values around a specific value. This concentrated distribution can be considered as the proof for the "real" value of V_{TH}.

  Some spatial dependence was noted as for the first sample. By observing again the fig. 5.2 and the placement of the sample on the initial wafer, this dependence can be probably explained since we know from the supplier of the wafer that the regions on the edges, in a distance up to even 1cm, are not perfectly fabricated.

5.5 Measurements of best devices

Choice of the best transistors

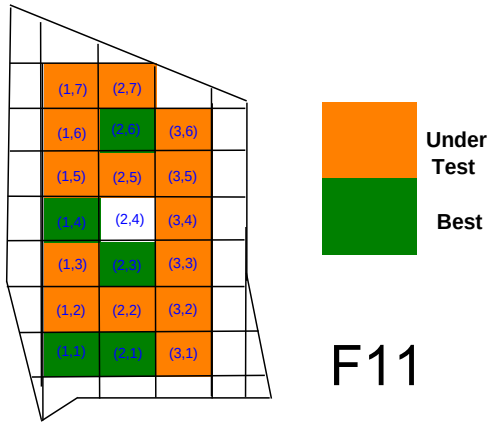


Fig. 5.11: Placement of the best F11 devices.

Based on the elaborate statistical study of the previous stage, the best devices for every different transistor according to the dimensions were defined. The characterization goes on with measurements performed selectively only on best transistors. In the graph beside we see characteristically the placement on the sample of the best F11 devices.

The orange cells indicate the periods where transistors were measured while the periods where

the measurements were not feasible are left blank. The green cells indicate the periods where the best devices were detected.

- **Pulsed measurements**

Pulsed measurements were performed to some of the best F11 (W_{nom}=1.5um), F32 (W_{nom}=3um) and F23 (W_{nom}=4um) devices. In the measurements presented below, pulsed sweep was imposed on the Drain and DC step bias on the Gate. The measurement conditions follows: pulse width: 200µsec, time-off: 1sec, measurement time: 119µsec. Keithley SMUs 2602 and 2651 were utilized.

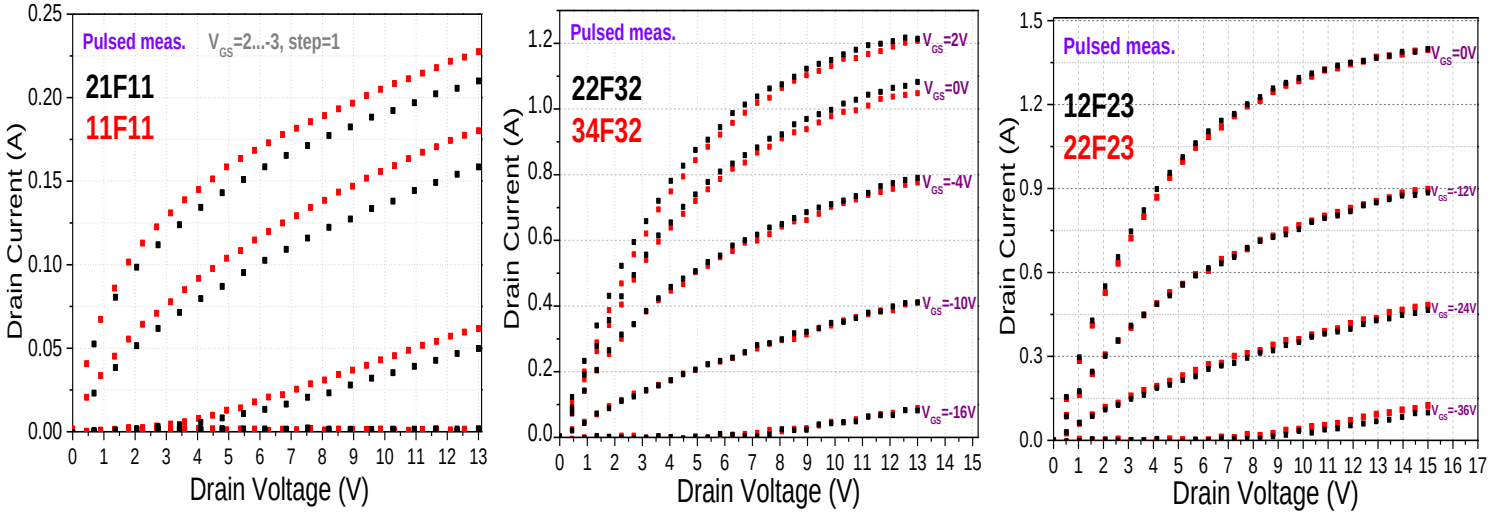


Fig. 5.12: Pulsed ON characteristics. There is obviously a large difference between the devices in terms of current value.

We clearly observe that as wider the channel is, higher current values are reached, while is more difficult to turn the JFET off. We see that the narrowest device, the transistor F11 is turned off by a reverse bias on the gate lesser than -1V despite the wider transistor F23 which is not turned off up to -36V.

- **C-V measurements**

Capacitance measurements were performed selectively to some transistors. Normal behavior was observed for all. The C_{iss}, C_{oss} and C_{rss} curves are shown characteristically for one of the best F11 devices. The measurement conditions are shown in the inset (f=1MHz, V_{GS}=-10V). Complementary, since C-V measurements were not performed during the study in one mask period, also the C_{GD}-V_{GD}, C_{GS}-V_{GS} and C_{DS}-V_{DS} measurements are presented below in the figure 5.14. All the measured capacitance values are in the order of picos (pF). It is obvious that the formulas C_{iss}= C_{GD}+C_{GS}, C_{oss}= C_{GD}+C_{DS} and C_{rss}= C_{GD} are demonstrated by the graphs.

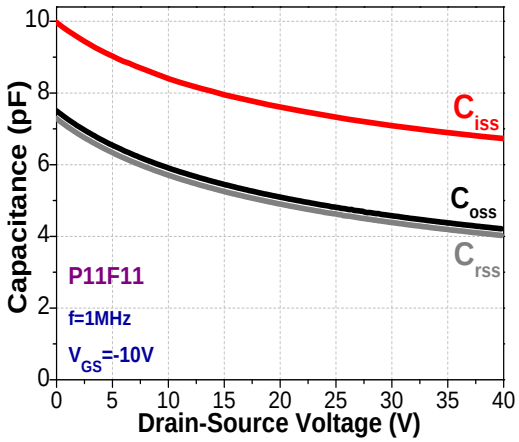


Fig. 5.13: C_{ISS}, C_{OSS} and C_{RSS} at f=1MHz.

Remarkable are the very small, almost negligible value of C_{DS}, the constant, unaffected by $V_{DS,}$ value

of C_{GS} as well as the discontinuity of the C_{GD} curve near zero voltage namely the threshold voltage of the device. Accordingly, the C_{GS} curve at this (threshold) voltage value exhibits an abrupt inflexion. The C_{GD}, unlike the C_{GS} exhibits a continuously descending tense due to the expansion of the depletion region within the drift region of the transistor.

Moreover, from the fig. 5.13 we distinguish a very small deviation between the C_{oss} and C_{rss} which differ in their definitions by the C_{DS}. This deviation is explained by the C_{DS}-V_{DS} graph and the very low value of the capacitance.

For extensive details about the C-V measurements is recommended to refer to Appendix 1.

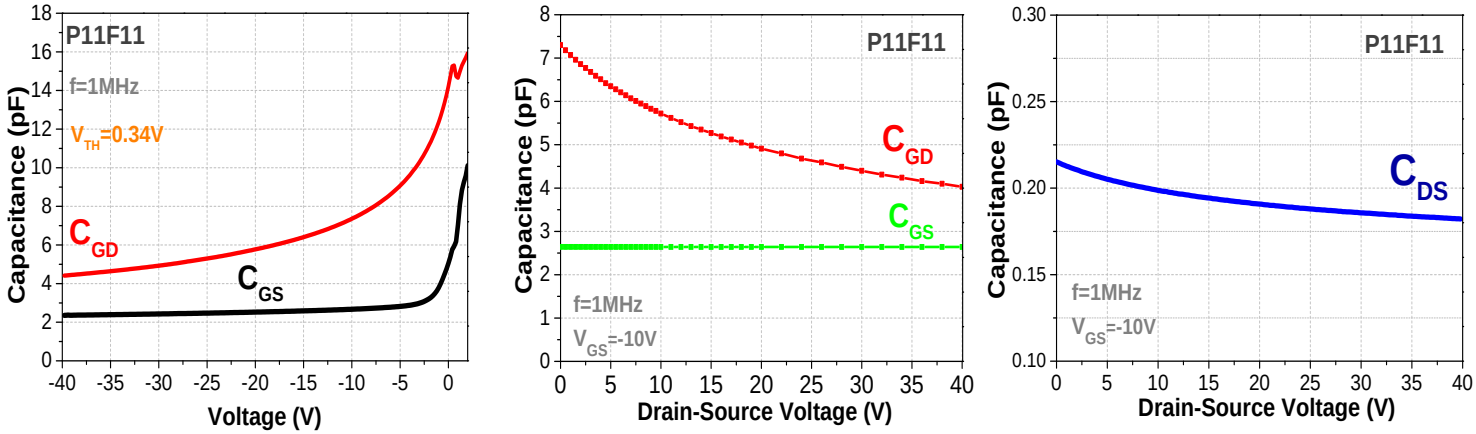


Fig. 5.14: At f=1MHz, C_{GD}-V_{GD} and C_{GS}-V_{GS}, C_{GD}-V_{DS} and C_{GS}-V_{DS}, C_{DS}-V_{DS} measurements.

- **Blocking DC I-Vs in fluorinert**

Testing in fluorinert is performed for evaluating the maximum blocking voltage which is determined at low reverse current to avoid self-heating. For these measurements a curve tracer Tektronix 370A was utilized. Below we see the measurements for one of the best for all the different under test devices.

It is obvious that the best blocking behavior as it was expected belongs to the narrowest transistor F11 (channel width=1.5um) as its blocking capability for gate voltage equal to -18V approached the value of 800V while the F23 with channel width equal to 4um can block less than 14V when biased at the Gate with -40V. It is obvious that the blocking capability is inversely proportional to the channel width.

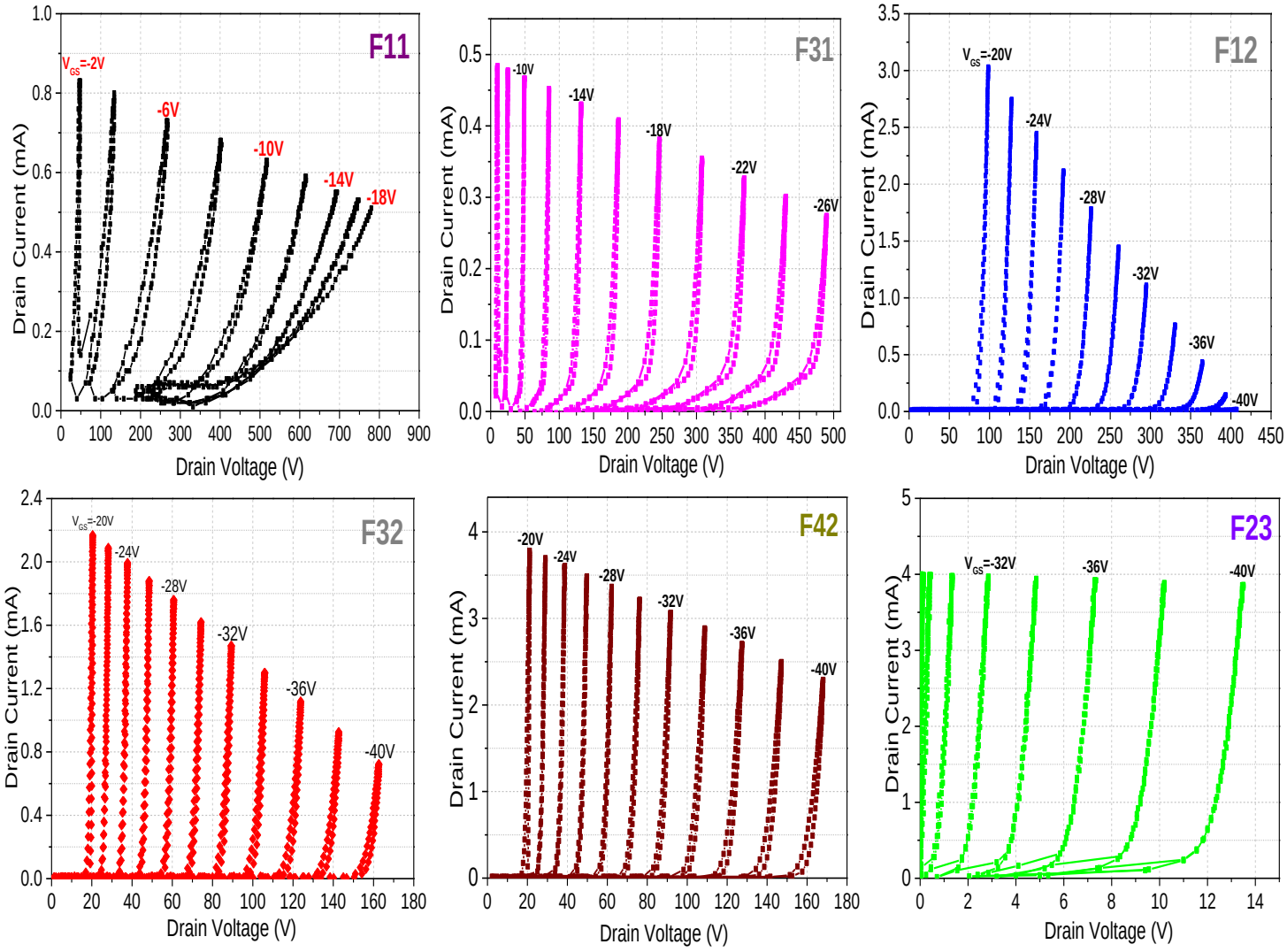
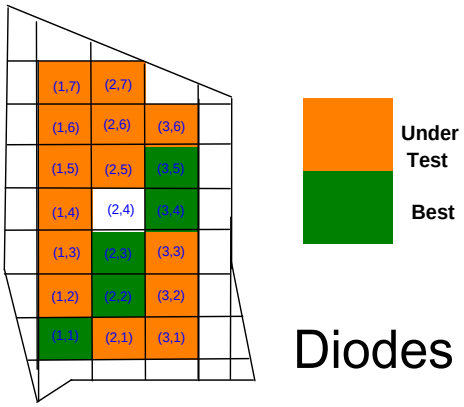


Fig. 5.15: Blocking I-V characteristics of best devices in fluorinert.

Choice of the best diodes



Although the diodes are out of the scope of our work, due to the improved performance of the transistors and the special interest that has come up, measurements have been also performed to the best diodes. These have been defined with the proposed in the previous chapter procedure are presented in the figure 5.16. The best diodes were detected in the green marked periods.

Fig. 5.16: Placement of the best Diodes.

- **Reverse I-V measurements in fluorinert**

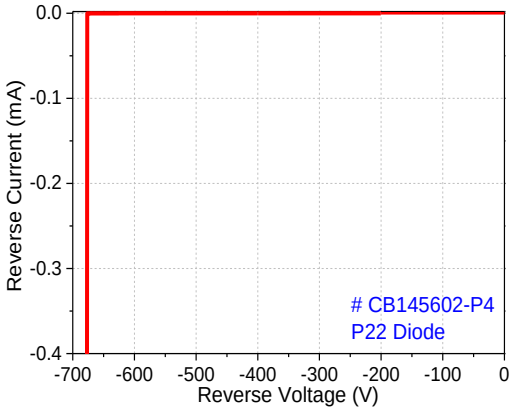


Fig. 5.17: Reverse measurement.

The electrometer Keithley 6517 is used while the compliance is set in a value that serves the power compliance of 500W/cm^2. Since the area of the square diode is 9E-4cm^2 (300um·300um), the current compliance is set to 0.9mA. In the figure we can see the reverse I-V of the best diode. Generally, the 5 best diodes exhibited blocking capability higher than -600V. The highest evaluated value is equal to -677V.

5.6 Specifications tables

The specs tables for the diode and the under test transistors are presented below and are of great importance as they summarize the great amount of the extracted information. Specs tables are filled for all the devices except of transistor F33 (the wider one) which exhibited bad behavior and there is rather no further interest about it.

The table of F11 transistor is extensive as this device exhibited better behavior than the other ones of the wider mesa widths. For the latter ones the specs tables provide basic information since the interest for them is not very intense.

For more information and instructive details about the construction of specs table refer to the respective section of the previous chapter.

Diode

Parameter	Symbol	Conditions	Value	Unit
Breakdown Voltage	V_{BR}	-	**660**	V
Leakage Current	I_{leak}	V=-200V	**-3.6n**	A
Knee Voltage	V_{knee}	-	**2.1**	V

(T=25^{O}C unless otherwise specified) **F11** (W_{nom}=1.5um)

Parameter	Symbol	Conditions		Value	Unit
Maximum Ratings					
Max Pulsed Drain Current	I_{DPmax}	V_{GS}=2V, V_{DS}=V_{Dsat}		**0.22**	A
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*		**<-65**	V
Off Characteristics					
Drain-Source Blocking Voltage	BV_{DS}	V_{GS}=-18V, I_{DS}= 0.5*mA*,		**800**	V
Leakage Current	I_{leak}	V_{DS}=0V,V_{GS}=-10V		**< E-8**	A
		V_{DS}=200V,V_{GS}=-10V		**< E-8**	
Gate Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=-20V		**< E-8**	
		V_{DS}=200V, V_{GS}=-10V		**< E-8**	
Voltage Gain	μ	V_{DS}=100V, I_{per}=0.1mA/mm		**51**	-
ON Characteristics					
Drain-Source On-resistance	R_{ON}	V_{GS}=0V		**17.7**	Ω
				12.3	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V		**0.25**	V
		V_{DS}=1V		**0.17**	
Gate Forward Current	$I_{G,FWD}$	V_{GS}=2V		**2E-7**	A
Knee Voltage	V_{knee}	-		**1.8**	V
Dynamic Characteristics					
Input Capacitance	C_{iss}	V_{GS}=-10V f=1MHz, osc. level=100mV	V_{DS}=0V	**9.9**	pF
			V_{DS}=40V	**6.6**	
Output Capacitance	C_{oss}		V_{DS}=0V	**7.4**	
			V_{DS}=40V	**4.1**	
Reverse Transfer Capacitance	C_{rss}		V_{DS}=0V	**7.3**	
			V_{DS}=40V	**3.9**	

(T=25^{O}C unless otherwise specified) **F31** (W_{nom}=2um)

Parameter	Symbol	Conditions	Value	Unit
Maximum Ratings				
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*	**-48**	V
Off Characteristics				
Drain-Source Blocking Voltage	BV_{DS}	V_{GS}=-26V, I_{DS}= 0.4*mA*,	**470**	V
Leakage Current	I_{leak}	V_{DS}=0V,V_{GS}=-24V	**<E-8**	A
		V_{DS}=200V,V_{GS}=-24V	**2.7E-6**	
Gate Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=-24V	**1.4E-7**	
		V_{DS}=200V, V_{GS}=-24V	**1.1E-8**	
Voltage Gain	μ	V_{DS}=100V, I_{per}=0.1mA/mm	**17.2**	-
ON Characteristics				
Drain-Source On-resistance	R_{ON}	V_{GS}=0V	**10.1**	Ω
			7	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V	**-3.4**	V
		V_{DS}=1V	**-3.7**	
Gate Forward Current	$I_{G,FWD}$	V_{GS}=2V	**7.6E-8**	A
Knee Voltage	V_{knee}	-	**1.9**	V

(T=25^{O}C unless otherwise specified) **F12** (W_{nom}=2.5um)

Parameter	Symbol	Conditions	Value	Unit
Maximum Ratings				
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*	**<-40**	V
Off Characteristics				
Drain-Source Blocking Voltage	BV_{DS}	V_{GS}=-28V, I_{DS}= 1*mA*,	**176**	V
Voltage Gain	μ	V_{DS}=100V, I_{per}=0.1mA/mm	**3.5**	-
ON Characteristics				
Drain-Source On-resistance	R_{ON}	V_{GS}=0V	**9.1**	Ω
			6.3	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V	**-7.4**	V
Gate Forward Current	$I_{G,FWD}$	V_{GS}=2V	**1.6μ**	A
Knee Voltage	V_{knee}	-	**2.4**	V

(T=25^{O}C unless otherwise specified) **F32** (W_{nom}=3um)

Parameter	Symbol	Conditions	Value	Unit
Maximum Ratings				
Max Pulsed Drain Current	I_{DPmax}	V_{GS}=2V, V_{DS}=V_{Dsat}	**1.21**	A
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*	**<-40**	V
Off Characteristics				
Drain-Source Blocking Voltage	BV_{DS}	V_{GS}=-34V, I_{DS}= 1*mA*,	**85.2**	V
Voltage Gain	μ	V_{DS}=100V, I_{per}=0.1mA/mm	**2.6**	-
ON Characteristics				
Drain-Source On-resistance	R_{ON}	V_{GS}=0V	**12.1**	Ω
			8.4	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V	**-13.4**	V
Gate Forward Current	$I_{G,FWD}$	V_{GS}=2V	**1.3μ**	A
Knee Voltage	V_{knee}	-	**2.4**	V

(T=25^{O}C unless otherwise specified) **F42** (W_{nom}=3um)

Parameter	Symbol	Conditions	Value	Unit
Maximum Ratings				
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*	**-36.3**	V
Off Characteristics				
Drain-Source Blocking Voltage	BV_{DS}	V_{GS}=-34V, I_{DS}= 1*mA*,	**75**	V
Voltage Gain	μ	V_{DS}=100V, I_{per}=0.1mA/mm	**2.5**	-
ON Characteristics				
Drain-Source On-resistance	R_{ON}	V_{GS}=0V	**40.4**	Ω
			28.1	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V	**-13.6**	V
Gate Forward Current	$I_{G,FWD}$	V_{GS}=2V	**1.2μ**	A
Knee Voltage	V_{knee}	-	**2.2**	V

(T=25^{O}C unless otherwise specified) **F23** (W_{nom}=4um)

Parameter	Symbol	Conditions	Value	Unit
Maximum Ratings				
Max Pulsed Drain Current	I_{DPmax}	V_{GS}=2V, V_{DS}=V_{Dsat}	**1.4**	A
Breakdown G-S Voltage	BV_{GS}	I_{GS}=15mA/cm^2 *(10.5μA)*	**<-40**	V
Off Characteristics				
Drain-Source Blocking Voltage	BV_{DS}	V_{GS}=-40V, I_{DS}= 2*mA*,	**12.7**	V
ON Characteristics				
Drain-Source On-resistance	R_{ON}	V_{GS}=0V	**8.9**	Ω
			6.2	mΩ·cm^2
Gate Threshold Voltage	V_{TH}	V_{DS}=0.1V	**-29.6**	V
Gate Forward Current	$I_{G,FWD}$	V_{GS}=2V	**1.4μ**	A
Knee Voltage	V_{knee}	-	**2.3**	V

By studying carefully the tables, we can summarize the performance of the sample devices in the following basic conclusions.

- High blocking value for the diode.
- In accordance with the diode very good blocking capability especially for the narrow devices. This is an outstanding improvement in comparison with the first sample, CB145602-P1 where low blocking values were measurements even for the transistor with the narrowest channel.
- For the F11 device (narrowest one) satisfactory values for BV_{DS} and voltage gain. The exhibited normally-off behavior is also accounted as an extra advantage.
- Good reported voltage gain values as a consequence of the blocking capability.
- Exceptional performance of the Gate-Source diode as for the reverse regime where very high (absolute) BV_{GS} values were reported. Consequently the G-S leakage current values were quite low. For the forward regime the performance can be characterized as satisfactory.
- Slightly lower max pulsed Drain current (I_{DPmax}) values in comparison with the first sample.
- Compared to the P1 sample, improved R_{on} values were measured, with the majority of them below 10 mΩ·cm^2. Unlike for the first sample, extreme R_{ON} values were not measured at all.

5.7 Conclusions

From the whole analysis above, we deduce that significant improvement to the performance of the transistors has been achieved and the majority of the malfunctions, observed in sample CB145602-P1 have disappeared in a way that the sample is approaching the desired specifications for our application. Therefore, the packaging of some of the best devices is scheduled. Of course the final stage of the characterization, namely the switching characterization will be feasible then.

Nevertheless, a new fabrication effort is underway during the writing of this work with the hope that by exploiting all the conclusions from the electrical characterization of the first two samples, the fabricated devices are going to be absolutely free of malfunctions and meet perfectly the required specifications.

Chapter 6. Comparisons between measurements and simulations

6.1 Introduction

In this chapter, our goal is to compare measured (experimental) ON results with the simulated (analytical) ones. Measured ON pulsed I-V characteristics accompanied by the simulated curves according to the JFET theory, are presented. The simulations have been performed in MATLAB software based on the theory presented in chapter 2. The study is shown for both the samples under investigation. In this way we have the chance to evaluate the accordance of the measurements with the theory.

It must be mentioned that the field dependent mobility model (FD model) has been used for the simulations instead of the conventional field-independent mobility, Shockley model (also known as Gradual Channel Approximation-GCA). According to the Shockley model, carrier mobility does not depend on electric field (E), which is a valid assumption at low electric field levels, where carrier velocity saturation does not occur. The reason for the choice of FD model is obvious in terms of accuracy. Particularly the electric field for biases 4-7 Volts reaches values of around $E = \frac{V}{l} = \frac{4V}{8um}$ $=0.5 \cdot 10^4$ V/cm and $\mathrm{E} = \frac{7V}{8um} = 0.9 \cdot 10^4\, V/cm$.

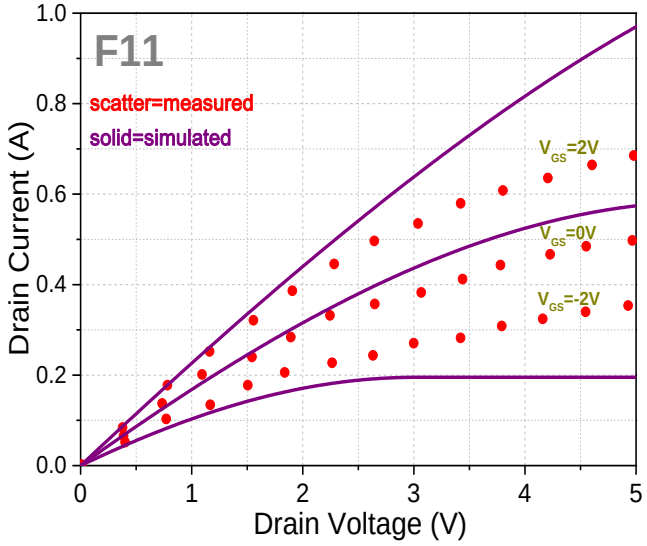
As we have already aforementioned, there is uncertainty for the actual dimensions of the fabricated devices. Of course the SEM photos observation is a strong tool helping us to determine the real dimensions provided that they are taken from different fabrication steps, with the proper angle and for various devices. Since, the available photos for our samples were few and not for many transistors, the SEM observation can be rather used as an indicator without ensuring firm deductions. Of course the reliability of this observation depends on the accuracy of the processing procedure as different deviations between the nominal and the actual channel widths can be observed even in the same sample. For that reason, using the OriginLab software, the equation giving the current I_D in dependence on the applied voltage has been fitted to the measured curves while keeping the channel width as the unknown parameter. The equation has been introduced in the Fitting Function Builder with "a" ($a=W_{ch}/2$) as parameter and the N (doping), q (elementary charge), e_s (relative permittivity), v_s (saturation velocity), Z (mesa length) and L_g (gate length) given as constants. The results extracted from this fitting procedure combined with the SEM photos observation results were used for the MATLAB simulations. Of course the only way to certainly determine the actual dimensions of a device (channel width, channel length, doping) is to cross "cut" the device (e.g. via cleaving) and measure the real dimensions from the cross sections.

It must be mentioned that the gate length values for the simulations were considered equal to the nominal ones although it is known that very often the actual gate length is greater than the expected according to the ion implantation procedure. This can be attributed to many factors with the struggling effect being the most prominent. The determination of the gate length (L_g) namely the implantation depth is a controversial matter in the literature. A rational approach says that the L_g can be calculated from the point at which the implant profile concentration becomes equal to the drift layer concentration via SIMS (Secondary Ion Mask Spectroscopy) analysis.

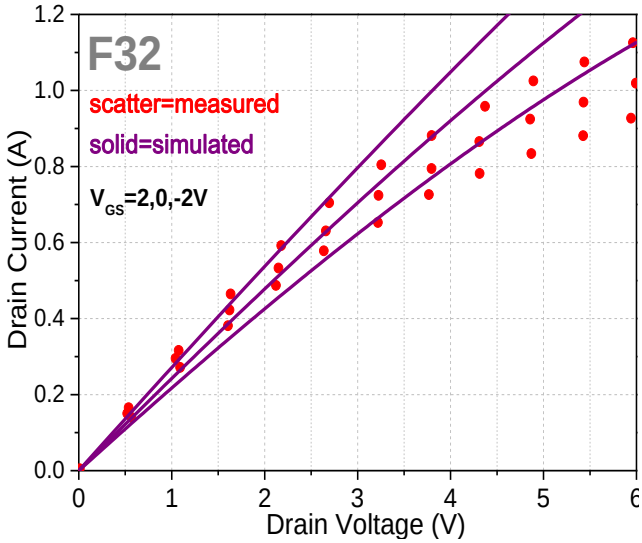
6.2 Comparisons

Below we can see for both the under test samples, some Pulsed ON I-V characteristics accompanied by the theoretical curves from the MATLAB simulations. In the captions we see the number of fingers (n), the nominal channel width (W_{nom}) and the channel width (W) used in the simulation.

- **CB145602-P1 sample**

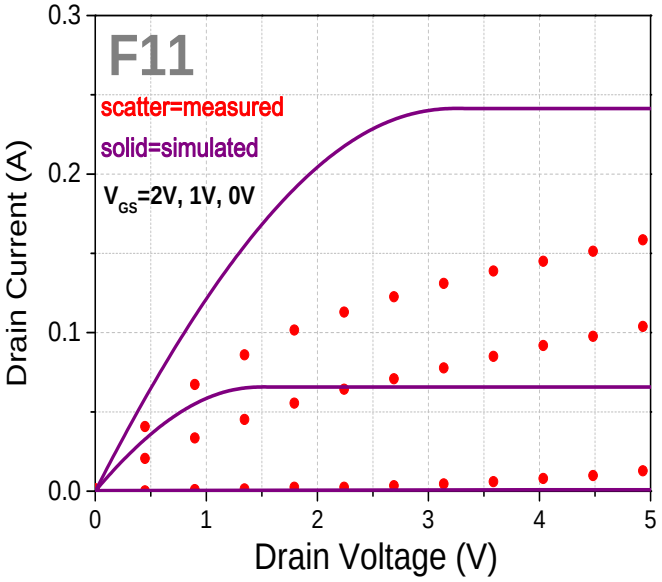


W_{nom}=1.5um (W=2.5um), #n=50

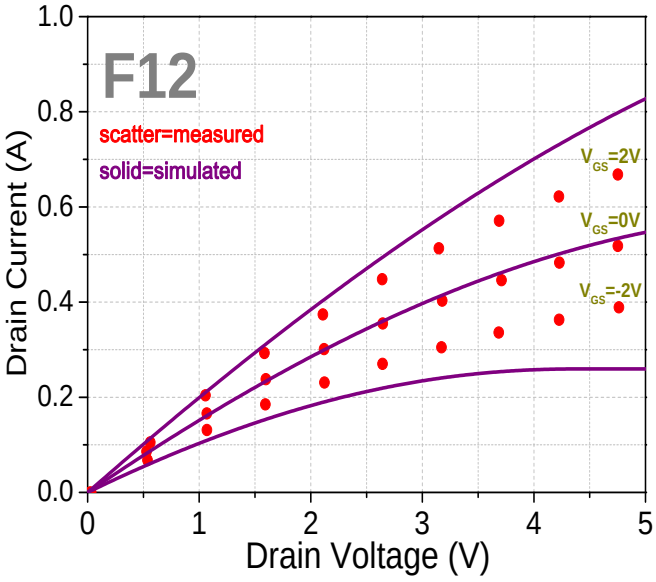


W_{nom}=3um (W=4um), #n=40

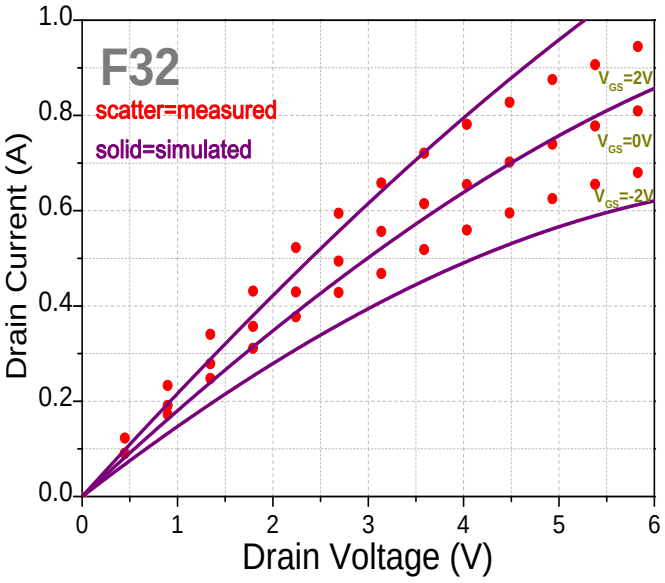
- **CB145602-P4 sample**



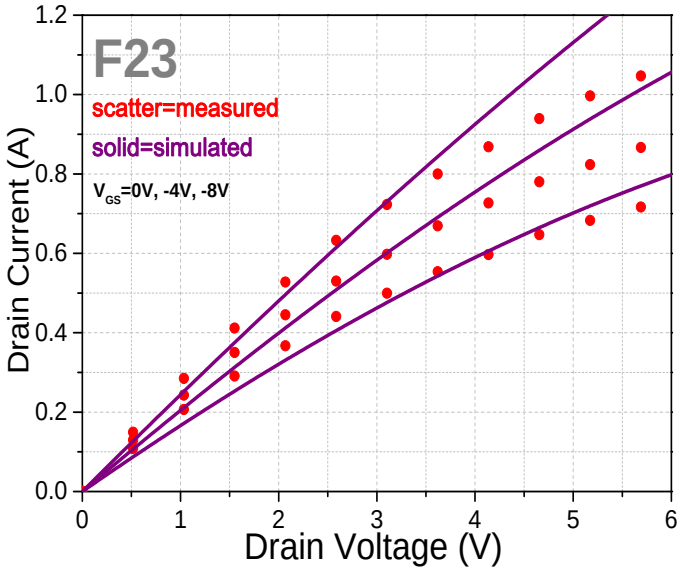
W_{nom}=W=1.5um, #n=50



W_{nom}=W=2.5um, #n=43



$W_{nom}=W=3um$, $\#n=40$



$W_{nom}=W=4um$, $\#n=34$

Conclusions:

It can be observed that the model generally predicts current values higher than the measured ones. However, the matching is significantly better than what would have been obtained with the field-independent mobility model (Shockley), which predicts significantly even larger current values. In addition, we can say that the model has the tense to predict the OFF state of the transistor for smaller (in absolute value) gate voltage values. Moreover, the coincidence between the measured and the simulated results is greater for the second sample (CB145602-P4), something that can be rather attributed to the more accurate fabrication procedure.

The model despite the observed deviations, seems to have the potentiality to give accurate results with the full knowledge of the actual dimensions and doping profiles. These can be determined confidently only by the cross cut of the device. The observed discrepancies can be at least in part attributed to the uncertainty for the doping profiles and the geometrical dimensions that have been used. May the doping profile values provided by the wafer manufacturer slightly differ spatially from the actual values. During the simulations stage we observed that any, even slight change in both channel width and doping profile (N) can influence significantly the results. The channel length also affects the results but much lesser than N and W_{ch}.

By observing only the measured results, we see once again, that higher current values are obtained for the first sample with the smaller channel length (0.3um) in comparison with the other one which features channel length equal to 1.1um.

From the analysis, another important deduction is that the SEM observation is a very useful, simple and in the same time reliable tool for the determination of the actual dimensions and in extent, the evaluation of the fabrication accuracy. Therefore, lots of photos must be taken with the proper angle during the different processing steps for many different dimensions devices. In this way one can be able to determine confidently the real dimensions without the need to cross cut any device, a peculiar procedure that also leads to the destruction of the device. Therefore, before the start of the electrical characterization procedure, particular attention must be given to the SEM photos which must be studied extensively and assiduously.

Chapter 7. Summary, Conclusions and Suggestions

7.1 Summary and conclusions

This dissertation is mainly focused on the electrical characterization of the fabricated in Microelectronics Research Group of IESL-FORTH, 4H-SiC TI-Vertical JFETs. Towards this, a measurements report is constructed where the electrical characterization procedure that must be followed is minutely presented, including the different measurements that have to be carried out and the corresponding experimental setups. Detailed information for each measurement, the necessary instrumentation, the compliances that must be imposed, tips and warnings on the configurations, as well as the parameters that are extracted are given in a simple and comprehensive way that even someone not familiar with the field of the semiconductor devices can understand. The characterization procedures are generic, so that they can be applied to the study of any future SiC JFET or with some modifications to SiC MOSFET.

In chapter 3, there is detailed information about the structure, the dimensions and the processing procedure of the fabricated samples with all the different followed steps, explained accompanied by SEM photos.

From the specifications tables filled in the end of the study for each of the samples, summarizing all the important characteristics, we observed different behavior between the samples although the only substantial differentiation is the deeper implantation depth for the second one. The operation of the second sample and particularly of the transistors with the narrowest channel width involved in this sample, seems to be close to the desired operation for the transistors that will be incorporated in the inverter according to the motivational research project. Therefore, we made the decision to package some devices, so that our study can proceed to the switching characterization while simultaneously, a new processing procedure is underway (fabrication of a third sample).

From the study of the samples we concluded to many results and noted that there are several correlations that can be done and help the processing engineers to understand the influence of many parameters on the characteristics of the device. In terms of dimensions, the channel length and width have to be controlled since they influence the trade-off between the blocking capability and the channel resistance which affects the maximum current that can pass.

The importance of a statistical study also revealed. It helps towards the formation of firm conclusions and its importance becomes greater as the uniformity of the sample increases.

Of course the theory governing the function of JFETs was necessary to be presented, so we see it chapter 2. Based on this theory in chapter 6 we observed the partly accordance of the measured and simulated ON I-V results. This study has revealed the sensitivity of the results to some parameters and the many aspects that can be studied and investigated for the analytical described model as well as for other models such as TCAD, in order to improve the accuracy and get even better coincidence.

In a few words we can say that the realized work in this dissertation can help someone to electrically characterize WBG semiconductor power devices in the proper way and in some extent to totally reveal the featured characteristics and exploit the device functionality. Of course, the simulations play an important role in contemporary semiconductor devices field, something that becomes obvious from the study of the last chapter with more effort necessary to be given towards this.

7.2 Suggestions and future work

The work covered in this dissertation has opened up a number of possibilities and aspects for future work. Some of them are presented below briefly.

- As it has been mentioned from the on wafer state the switching characteristics cannot be measured. Therefore, the encapsulation of the devices that are labeled as "best", must be performed and the electrical characterization must extend to the switching field. The important parameters that are usually defined are: turn on time t_{on}, turn off time t_{off}, turn on losses E_{on} and turn off losses E_{off}. The packaging is preferred to be done in through hole packages, e.g. TO-2xx. Moreover once the device is packaged there are some static AC characteristics that can now be measured. These are the internal gate resistance (R_g) and the package parasitic inductances. By the end of these measurements the devices can be considered as fully electrically characterized.
- In terms of simulations, with the help of SILVACO software, TCAD simulations can be performed for both the ON I-V and the blocking characteristics of the devices. Some preliminary efforts have been already done but more work has to be done on it.
- As a continuity of the latter, simulations can be also performed with the compact model developed in the electronics laboratory (TUC/ELAB) of TUC. In this way, the measured results can be compared to three different approaches, the analytical model, as has been done in chapter 6, the compact model and the TCAD model. The assessment of the accuracy of each model will be feasible and useful results can be extracted as for the more appropriate model for future simulations. Of course issues such as the simulation resources, the simulation time and the required effort must be taken into account.
- As it has been already mentioned a new fabrication effort is underway during the writing of this work with the hope that the fabricated devices are going to be absolutely free of malfunctions and meet perfectly the required specifications. A new mask has been employed to resolve issues like low output current by increasing the area of the devices and relatively low blocking voltage by employing new edge termination geometries. The great amount of information that has been extracted can help us to succeed, provided that all the gained experience will be exploited. Of course, by the end of the fabrication procedure performed by the processing engineers, the new sample must be electrically characterized in order to determine if the desired specifications are eventually met.
- Another work that can be done is the cross cut of some devices in order to measure reliably their actual dimensions and doping profiles. In this way we are going to be able to evaluate the correctness of the other approaches proposed in chapter 6 for the dimensions and doping determination (fittings and SEM photos observation).
- From the elaborate analysis that was presented about the electrical characterization procedure, one can easily understand that the necessary procedures are lengthy and the much required time is a severe drawback. The only way to reduce the characterization time is the automation of the procedures. Effort needs be done for the realization of an automatic data acquiring system which can rapidly obtain characteristics without a human intervention.
- Many perspectives can be considered as challenging, from the fabrication aspect for future work. Different geometries, structures, dimensions, doping profiles or even materials like GaN or the promising Diamond can be utilized.

- The enhanced performance of SiC devices over conventional Si has led to an increasing number of semiconductor manufacturers producing SiC devices. As a result, the last few years, many other manufacturers have joined the SiC market, such as United Silicon Carbide, Inc. The future work involves the electrical characterization of these newly released SiC transistors. Must be kept in mind that very often the characteristic of a power device does not follow the exact information given in a datasheet, especially for SiC power devices whose datasheets are often preliminary and can be updated within a few months.

Appendices

Appendix 1. FET Capacitance Voltage measurements procedure

- ***Table of Contents***

1. Symbols

Acronym	*Meaning*
FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
JFET	Junction Field Effect Transistor
VJFET	Vertical Junction Field Effect Transistor
C_{GD}	Gate-Drain Capacitance
C_{GS}	Gate-Source Capacitance
C_{DS}	Drain-Source Capacitance
C_{ISS}	Input Capacitance
C_{OSS}	Output Capacitance
C_{RSS}	Reverse Transfer Capacitance
V_{GD}	Gate-Drain Voltage
V_{GS}	Gate-Source Voltage
V_{DS}	Drain-Source Voltage
V_{TH}	Threshold Voltage
BNC	Bayonet Neill Concelman Connector
DUT	Device Under Test
H_{cur}	High current
H_{pot}	High potential
L_{cur}	Low current
L_{pot}	Low potential
DR	Depletion Region

2. General Information

Capacitance is the ability of a body to store an electrical charge. Any object that can be electrically charged exhibits capacitance. Capacitance–Voltage profiling (or C-V profiling) is a technique for characterizing semiconductor materials and devices. The applied voltage is varied, and the capacitance is measured and plotted as a function of voltage.

The depletion regions in a FET with their ionized charges inside behave like a capacitor. By varying the voltage applied to the junction it is possible to vary the depletion width. The dependence of the depletion width upon the applied voltage provides information on the semiconductor's internal characteristics, such as its doping profile and electrically active defect densities.

C–V profiling is often used in fully fabricated devices to characterize threshold voltages and other parameters during reliability and basic device testing and to model device performance. C–V measurements are done by using capacitance–voltage meters of Electronic Instrumentation. They are used to analyze the doping profiles of semiconductor devices by the obtained C–V graphs.

Generally, the LCR Meter is an instrument used to measure capacitance (C) resistance (R) or inductance (L) of a DUT. The apparatus measures directly the impedance of the device and consequently the values of C, L or R can be extracted. The principle of operation of an LCR meter is based on imposing a test voltage signal and measuring the current flowing through the DUT. According to this, the complex impedance of the DUT can be measured with a measurement circuit consisting of a signal source, a voltmeter, and an ammeter. The voltmeter and ammeter measure the vectors (magnitude and phase angle) of the signal voltage and current, respectively. Most of the conventional LCR meters have a voltage bias function and in addition to the AC test signal, a DC voltage can be applied to the DUT.

The connection principle of a DUT is illustrated in the Fig. 1. We observe that the instrument is equipped with four BNC connectors, H_{cur} (High current), H_{pot} (High potential), L_{pot} (Low potential), and L_{cur} (Low current), as measurement terminals. The generated test signal as well as the optional DC bias, are applied through the H_{cur} terminal while the current response is measured through the L_{cur}. Furthermore, the outer conductors of BNC connectors of the terminals are connected each other and joined to the guard of the apparatus.

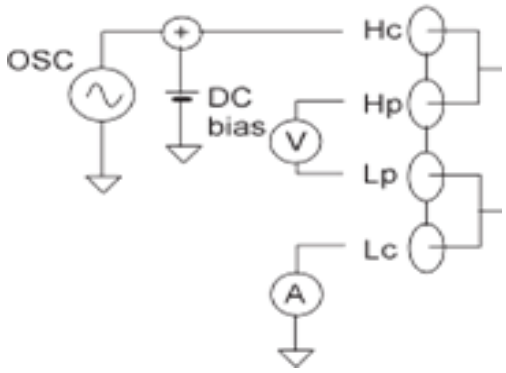


Fig.1. Principle of the connection to a DUT

There are several connection configurations used to interconnect a DUT with the measurement terminals but 3 different configurations are more common. The shielded-two terminal (2T), the three terminal (3T) and the five terminal (5T). The most suitable configuration should be selected based on the DUT's impedance and required measurement accuracy. In the graph below we can see these three more usual configurations.

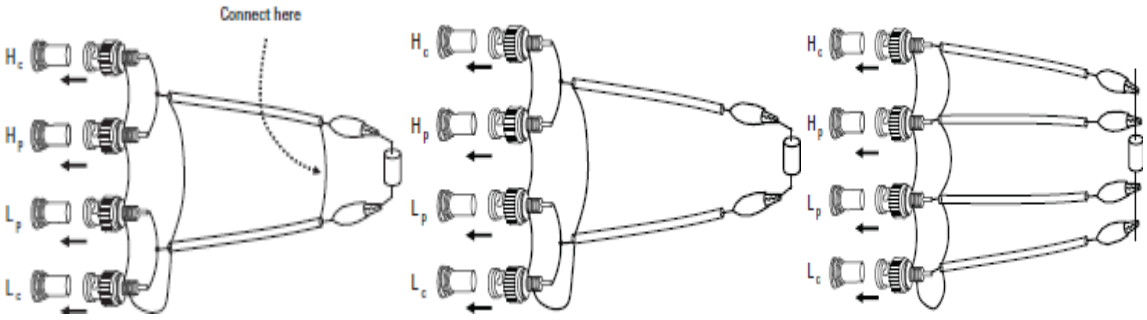


Fig.2. Shielded 2T (2 Terminals) 3T (3 Terminals) 5T (5 Terminals)

The three-terminal (3T) configuration is quite simple and versatile while ensures measurement accuracy above 10 kΩ. If the two outer conductors are connected to each other at the ends of the cables, the accuracy for the lower impedance measurement is improved a little. This configuration is called the shielded 2T configuration. The five-terminal (5T) configuration has a wider measurement range from 10mΩ to 10MΩ and is usually performed using ancillary test leads. Concerning the oscillation level (AC) of the LCR meter, it must be chosen to be quite small because the junction capacitances are very sensitive to the amplitude of the signal. A value of common use is that of 100mV.

The electrical characterization lab of IESL-MRG is equipped with the **Agilent 4284A** Precision LCR meter, which is shown on the left in the figure 3 while the LCR meter available in the Electronics Laboratory of TUC, an **Agilent E4980A** is presented on the right of the following graph. Both instruments are capable to provide DC bias up ±40V and perform measurements from 20Hz up to 1MHz (8610 selectable frequencies) **(4284A)** and 2MHz **(E4980A)**. The LCR meter is connected via GPIB to a computer where the measurement data are collected and stored via LabVIEW software.

Fig.3. Left- Agilent 4284A Precision LCR Meter, *Right*- Agilent E4980A Precision LCR Meter

3. FET Capacitance-Voltage measurements

- Introduction

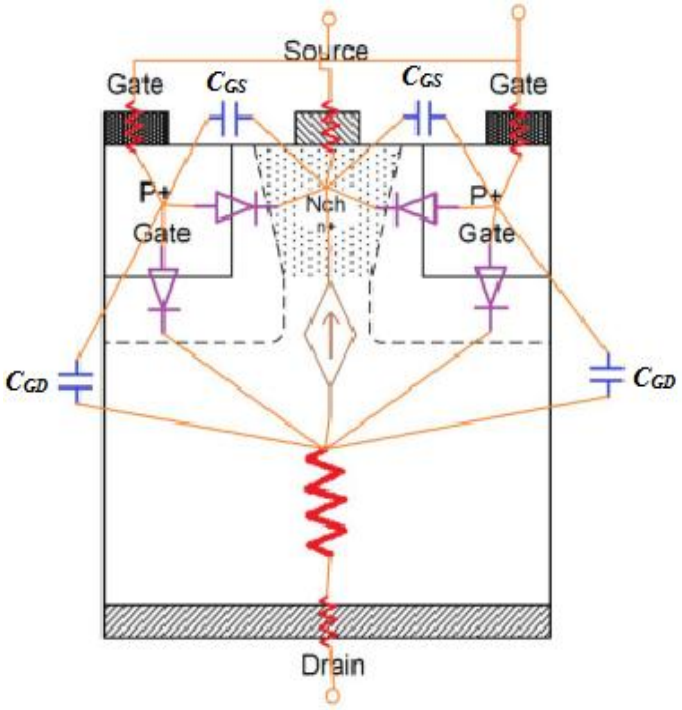
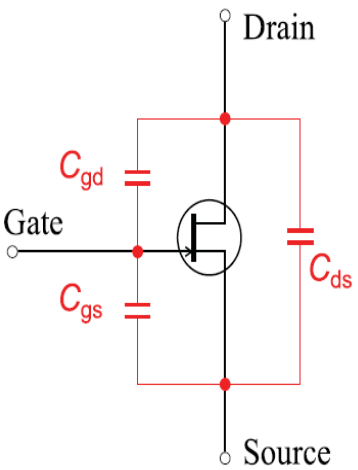


Fig.4. Electrical components within a VJFET

The depletion regions formed in a FET behave as capacitors appearing to the terminals of the transistor and vary nonlinearly with the applied voltages. Generally, the capacitances between the terminals of a semiconductor device greatly influence its switching behavior and for that reason their characterization and modeling is mandatory. From the figure 4 where we can see a cross section of a vertical JFET with the electrical components within it, we can understand how these capacitances are formed and where are they located in the device.



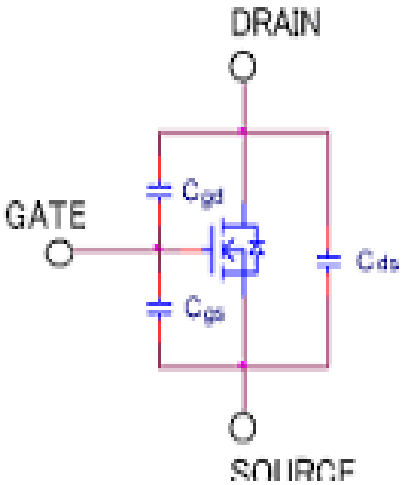


Fig.5. Intrinsic capacitances of JFET Intrinsic capacitances of MOSFET

Capacitance-voltage (C-V) testing is widely used to determine semiconductor parameters. The fundamental nature of these measurements makes them useful in a wide range of applications. Particularly in wafer processes, C-V measurements can reveal oxide thickness, oxide charges, mobile ions (contamination), and interface trap density. These measurements continue to be used after other process steps, such as lithography, etching, cleaning, dielectric and polysilicon depositions, and metallization. After devices are fully fabricated on the wafer, C-V is used to characterize threshold voltages and other parameters during reliability and basic device testing.

There are three combinations of terminals that should be used to determine the individual capacitances of a field effect transistor. They are the C_{GD} (also known as Miller capacitance), C_{GS} and C_{DS} (see figure 5) providing useful information mainly from the physical principle of operation and processing point of view. These parameters are measured either versus the corresponding voltage or the V_{DS} voltage.

Nevertheless, from the application point of view it is preferable to measure the $C_{iss}=C_{GD}+C_{GS}$ (Input Capacitance), $C_{oss}=C_{GD}+C_{DS}$ (Output Capacitance) and $C_{rss}=C_{GD}$ (reverse transfer capacitance). Indeed, in a device datasheet very often these three are reported as typical parameters related to switching performance. They provide information related to the switching, charging and driving performance. The C_{iss} is called input capacitance as both of the sum terms include the Gate terminal which is the input terminal of the FET while the C_{oss} is called output capacitance as both of the terms include the Drain terminal which is the output terminal of the device. These parameters are measured vs V_{DS} voltage.

Typically, semiconductor capacitance values range from nanofarads (nF) to picofarads (pF). Application notes provided by device manufacturers describe the power device capacitance measurement method. However, it is not a simple measurement. Many factors such as the determination of good peripheral circuit constants, measurement circuit compensation and appropriate measurement frequency as well as oscillation level have to be considered.

During the measurement the value of the dissipation factor (D) is also extracted simultaneously with the capacitance value on the LCR meter monitor. Particular attention must be given to the value of D as high values of *D* mean low capacitance measurement accuracy. Thus, high *D* is a limiting factor in the practical use of a Capacitance meter. Higher frequencies can help solve the problem. At higher frequencies the capacitive impedance is lower, resulting in a current that is higher and more easily measured.

- Measurement of individual capacitances C_{GD}, C_{GS}, C_{DS}

The H_{POT}-H_{CUR} and L_{POT}-L_{CUR} terminals are connected to the appropriate FET terminals. Always the H_{POT} and H_{CUR} are connected to the first terminal indicated by the first letter in the subscript of the involved capacitance symbol. For example for the C_{GD} measurement the H_{POT}, H_{CUR} are connected to the Gate and the L_{POT}, L_{CUR} to the Drain.

Usually many researchers perform the measurements of C_{GD}, C_{GS} and C_{DS} directly with the LCR meter by just connecting the respective terminals to the High (H) and Low (L) terminals of the apparatus while leaving the unused terminal floating. However, *this method is erroneous and introduce fatal errors to the measurements*. The Fig. 6 below shows the situation when we try to measure an unknown capacitance (C_x) of a 3-terminal device without using the AC guard and the unused terminal is floating (fig.6-left). In that case, current can flow through the other two capacitors resulting in erroneous measurement results. The best way to prevent this from occurring is the

deflection of the current flowing through C_a in order to deter it from going into the measurement node (Low terminal) and affect the measurement results. The latter can be easily achieved simply by connecting the unused terminal to the AC guard, as is clearly presented on the right of the following graph.

At this point it is very important to stress-out that the AC guard is in the same potential with the shields of the four-terminal pair connectors.

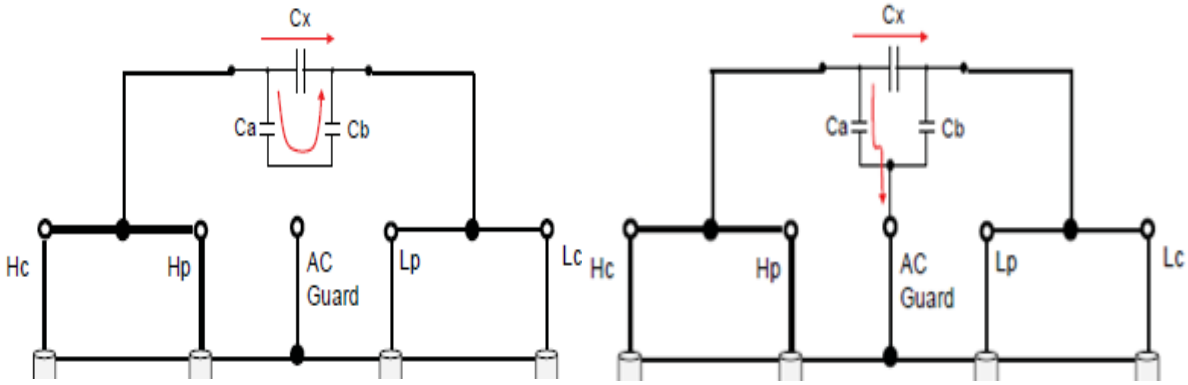


Fig.6. Measuring capacitance without using (left) / using (right) the AC guard of the instrument.

Thus, when the AC guard is connected, the current flowing through the parasitic path (C_a) does not affect the accuracy of the measurement of the unknown capacitance (C_x). Of course, a necessary condition is that the impedance of the AC guard node is much less than that of the parasitic path (C_b).

In order to demonstrate and verify the above, a test with three capacitors connected in delta on a breadboard was employed. These three capacitors can be assumed that work as the intrinsic

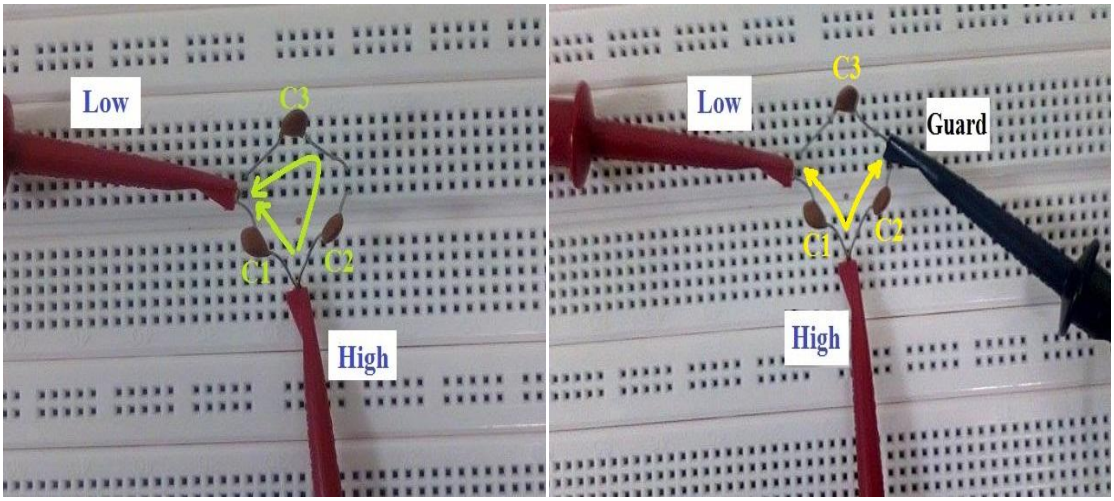


Fig.7. Testing with (*right*) and without *(left*) the use of AC Guard.

capacitances of a FET. The capacitance value of the capacitors was selected at 22pF, a value in the same order of magnitude with the respective, measured in semiconductor devices. In the pictures of figure 7, we observe the measurement setup with (right) and without (left) the use of the instrument guard terminal.

With the left circuitry the apparatus can "see" the C_1 in parallel with the C_2 and C_3, which are in series. So the expected value to be measured between the "High" and "Low" terminals is

$22+\frac{22\cdot 22}{22+22}=22+11=33pF$. Indeed the measured value on the instrument monitor is nearly 33pF. On the other hand, with the use of the guard the split AC signal flowing throw C_2 is passed in the guard and is prevented to reach the low terminal, flow through the internal ammeter and affect the measurement. In this way, the C_2 and C_3 are excluded and the apparatus is measuring the desired value of 22pF, i.e the value of the C_1 connected to the "High" and "Low" terminals. Indeed the instrument measures approximately 22pF.

Continuing the analysis on the measurements of individual capacitances, in order to measure any of the C_{GD}, C_{GS} and C_{DS} vs the corresponding voltage, the perspective terminals must be connected to the High (H_{cur}, H_{pot}) and Low (L_{pot}, L_{cur}) terminals of the apparatus and the unused terminal must be connected to the Guard. The voltage sweep is carried out by the integrated LCR power supply.

Particular mention must be done to the C_{DS}-V_{DS} measurement of a normally-on FET. In that case an extra external DC bias is needed to be applied at the Gate terminal in order to keep the transistor switched off. The latter is an absolutely necessary condition for the capacitance measurement. Moreover a resistor is necessary between the power supply and the Gate in order to block the measurement AC signal flowing into the power supply. A resistor of 100kΩ is usually adequate. Of course, the unused terminal, namely the Gate terminal must be connected to the gourd of the instrument via a capacitor in order to block the DC signal flowing into the low terminal. A common value for this electrical element is 100pF.

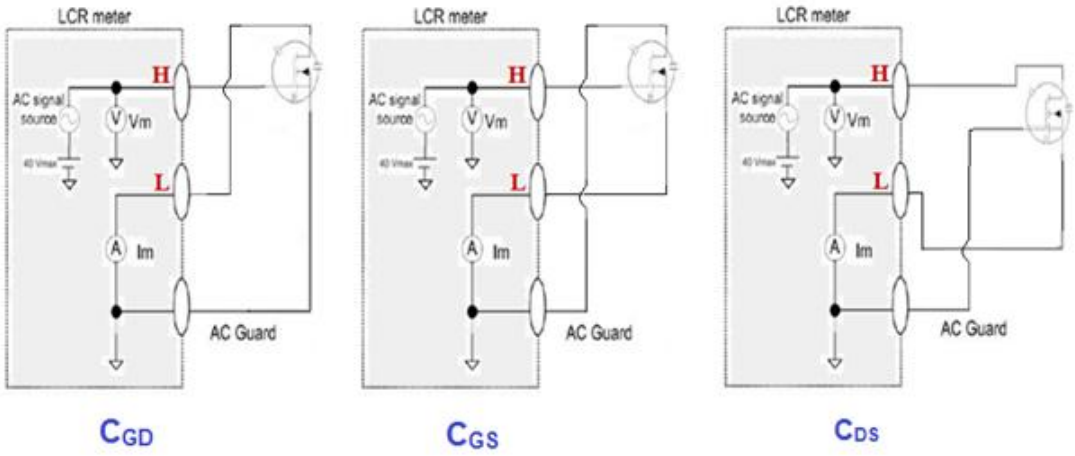


Fig.8a. Circuitries for the C_{GD}-V_{GD}, C_{GS}-V_{GS}, C_{DS}-V_{DS} measurements.

In the figure 8a above we can see the circuitries for the measurements of the individual capacitances C_{GD}, C_{GS} and C_{DS} while in the 8b below we can distinguish the modifications needed for the C_{DS}-V_{DS} measurement of a normally-on FET.

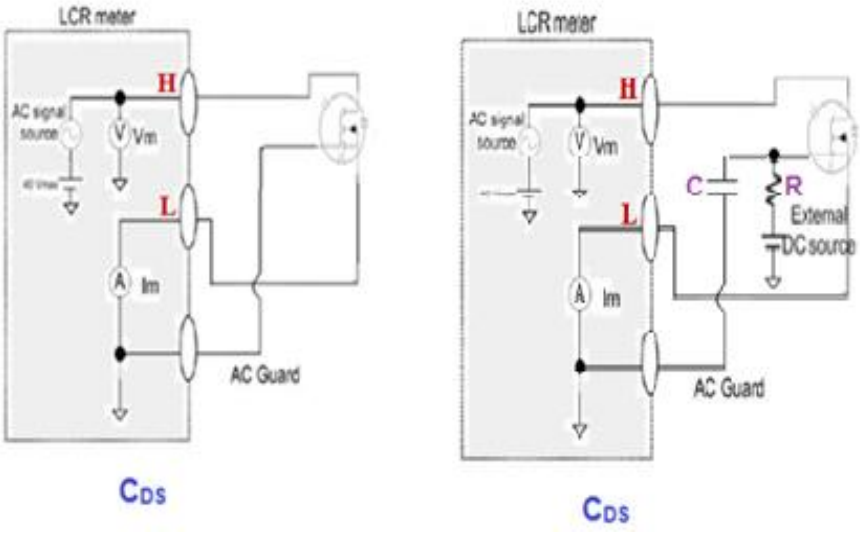


Fig.8b. Circuitries for the C_{DS}-V_{DS} measurement of a normally-off (left), normally-on (right) FET.

The C_{GD} and C_{GS} can be also measured while a variable DC voltage source is connected to the drain terminal referenced to the source, namely versus V_{DS}. For the C_{GS}-V_{DS} an extra external DC source is necessary. This modification is depicted on the right of the following figure 8c. On the left of the figure the C_{GS}-V_{GS} circuitry is presented again to make the differences more distinct. Corresponding modifications must be also done for the C_{GD}-V_{DS} measurement. The latter is essentially the C_{RSS}-V_{DS} measurement. (See below for details and circuitries). As we can see on the right of the following figure, the voltage sweep on the drain terminal, is performed by the external DC Source while the integrated DC bias (±40V) of the instrument is not used (Notice on the right graph below, the use only of the AC signal source). The utility of the capacitor and the resistor is the same as in the case of the C_{DS}-V_{DS} of normally-on FETs, described above.

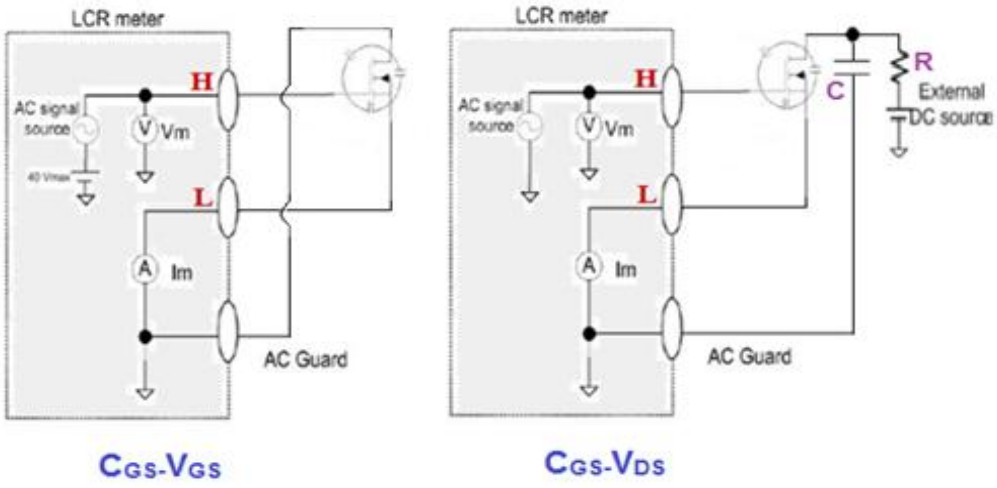


Fig.8c. Circuitries for the C_{GS}-V_{GS} (left), C_{GS}-V_{DS} (right) measurements.

- Measurement of C_{ISS}, C_{OSS}, C_{RSS}

In a device datasheet usually the C_{iss}, C_{oss} and the C_{rss} versus V_{DS} are reported as typical parameters related to switching performance. Furthermore, from the measurement of C_{iss}, C_{oss} and C_{rss} vs V_{DS} the individual capacitance parameters C_{GD}, C_{GS}, C_{DS} can be extracted. The measurements

are performed for a depleted transistor channel (OFF-state of transistor) while a variable DC voltage supply is connected to the drain terminal referenced to the source. For normally-on devices an extra bias (< V_{TH}) must be imposed to the gate terminal in order to keep the transistor off and enable the measurements.

Due to the fact that the DC voltages applied to power devices during many switching applications are in the hundreds or even thousands of volts; it is often necessary to perform these measurements up to high V_{DS} voltage values, higher than 40V namely the bias that the LCR meter is able to provide. Thus, in order to characterize the device up to high voltage values, an extra external high voltage DC source is necessary due to this inadequacy. A resistor is needed at the output of the external DC supplies in order to block the measurement AC signal flowing into the DC power supply. Usually 100 kΩ resistor is adequate for a wide range of measurements. In addition, a blocking capacitor is mandatory to superimpose the measurement AC signal on the voltage bias source and protect the LCR meter. A large capacitor is ideal to minimize measurement AC signal attenuation at the DUT terminal. Typically the appropriate blocking capacitor size is around ten times larger than the largest DUT capacitance. The capacitor type should be thin film as it has less voltage dependency. Usually 100nF capacitor is adequate for a wide range of measurements.

The circuitries for the measurement of the aforementioned capacitance parameters are presented in Figs. 9-11. For normally-on devices, the imposition of a bias (<V_{TH}) to the gate as has been described above is necessary. For normally-off devices there is no need for this biasing.

It's worthwhile at this point to emphasize that when using an external DC bias supply, its ground terminal must be connected to the ground terminal of the LCR meter in order to have accurate measurement results. Generally, all the instruments that constitute the measurement setup must have common ground.

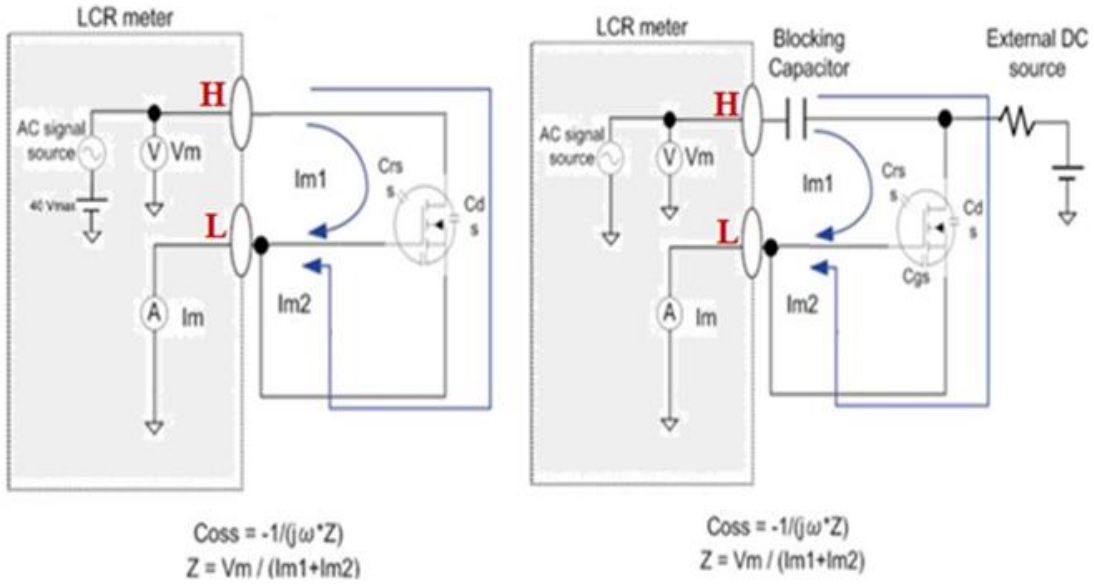


Fig.9. Circuitries for $\mathbf{C_{oss}}$ (=C_{GD}+C_{DS}) measurement. (Left) Up to 40V, (Right) Up to high voltage bias. The dashed lines square includes the internal components of the LCR meter. Images taken from [3].

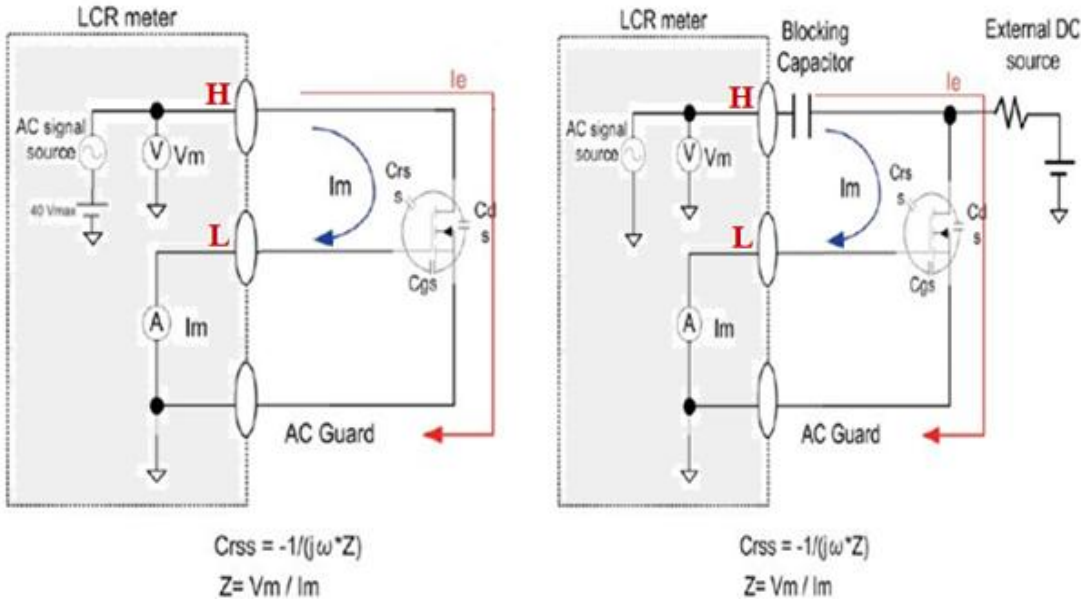


Fig.10. Circuitries for $\mathbf{C_{RSS}}$(=C_{GD}) measurement. (Left) Up to 40V, (Right) Up to high voltage bias. The dashed lines square includes the internal components of the LCR meter. Images taken from [3].

For the $\mathbf{C_{OSS}}$ (=C_{GD}+C_{DS}) measurement as we can see in the figure 9, the High (H) and low (L) ports of the LCR meter are connected to the device after shorting the gate and the source terminals using a wire. The device impedance is calculated from the applied voltage, V_m, and the measured currents I_{m1}, I_{m2} (I_m=I_{m1}+I_{m2}) flowing through C_{GD} and C_{DS} respectively. Notice on the right of the above graph, the deactivation of the integrated DC bias from the ON/OFF DC bias button of the LCR meter. The utility of the resistor and the capacitor on the right graph, is to block the measurement AC signal flowing into the power supply and the DC signal flowing into the H terminal respectively. Common values for these electrical elements are 100kΩ and 100nF.

For the $\mathbf{C_{RSS}}$ (=C_{GD}) measurement as we can see in the figure 10, High (H) and Low (L) ports of the LCR meter are connected to drain and gate terminals while source is connected to the Gourd. Since the reverse transfer capacitance, C_{rss} is equivalent to C_{GD}, we need to remove any interference from C_{DS} and C_{GS}. This is achieved with the AC guard which prevents the current flowing through C_{DS} going in the current meter. Thus any influence of the C_{DS} and C_{GS} is eliminated. The utility of the resistor and the capacitor on the right graph, is as for the C_{OSS} measurement. The C_{rss} is related with the switching speed of a device.

For the $\mathbf{C_{ISS}}$ (=C_{GD}+C_{GS}) measurement as we can see in the figure 11, an external DC Source is mandatory for the sweep even for the measurement up to few V_{DS} volts. If the DUT is a normally-on FET, the internal source of the LCR meter can be used for the bias of the Gate terminal.

Measuring the input capacitance (C_{ISS}) presents some challenges that are not present for the C_{RSS} and C_{OSS} measurements. High (H) and Low (L) ports of the LCR meter are connected to gate and source terminals respectively while an external power supply is used to bias the drain terminal. A resistor is necessary between the power supply and the drain in order to block the measurement AC signal flowing into the power supply. As it has been already mentioned, usually 100 kΩ resistor is adequate. In addition, a capacitor is necessary between drain and source terminals in order to block the DC bias while simultaneously shorting the AC measurement signal and thus, leading to the elimination of the C_{DS} influence. The capacitance value of the shorting capacitor must be higher than the C_{DS} which usually takes very low, almost negligible values (more than 100 times less than other device capacitances) so a capacitor of 100nF can be used again. The C_{ISS} is value is very critical for the switching performance of a FET.

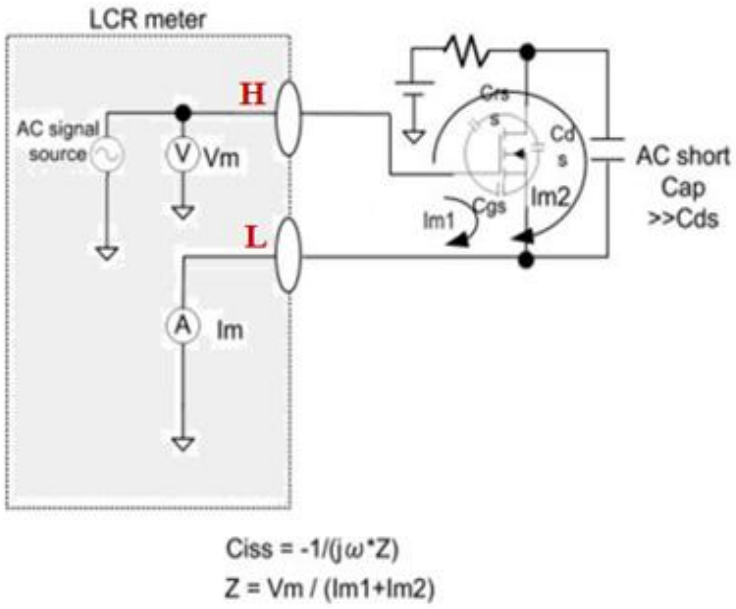


Fig.11. Circuitry for $\mathbf{C_{ISS}}$ ($=C_{GD}+C_{GS}$) measurement.
The dashed lines square includes the internal components of the LCR meter. Images taken from [3].

After constructing measurement circuitries appropriate compensation should be performed. The first is open compensation to cancel stray capacitance in the measurement path using the "open compensation" function within the LCR meter. Secondly, short compensation should be performed in order to cancel out the residual inductance of the test leads.

4. Experimental results

In order to estimate the precision of the above presented capacitance measurements configurations, the C-V measurements of two commercial devices are presented below. A normally-on packaged Si VJFET (2N4393) and a PowerMOS Transistor Philips BUK436-100A/B were the devices under test. The characterization was performed in the electrical characterization lab, in the premises of Microelectronics Research Group, IESL-FORTH. The employed instrument was an Agilent 4284A precision LCR meter. Particularly, C_{iss}, C_{oss}, C_{rss} as well as C_{GD}-V_{GD}, C_{GS}-V_{GS}, C_{GD}-V_{DS}, C_{GS}-V_{DS} and C_{DS}-V_{DS} were carried out. In the PowerMOS the C_{iss}, C_{oss}, C_{rss} were measured. The results are presented below. The conditions of the measurements are indicated in the inset of the graphs.

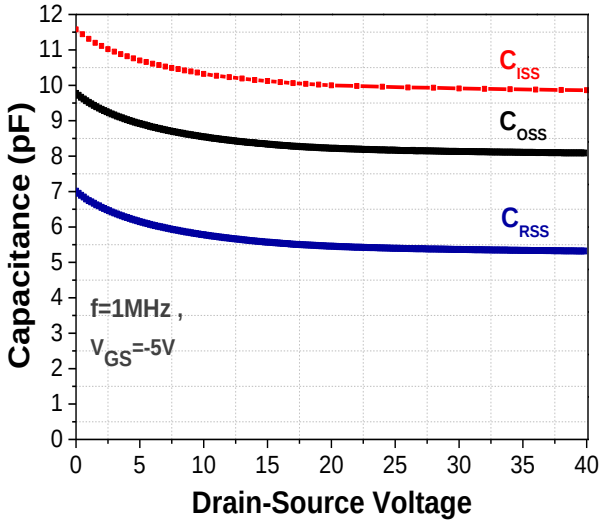


Fig.12a. **C_{ISS}, C_{OSS}** and **C_{RSS}** measurements.

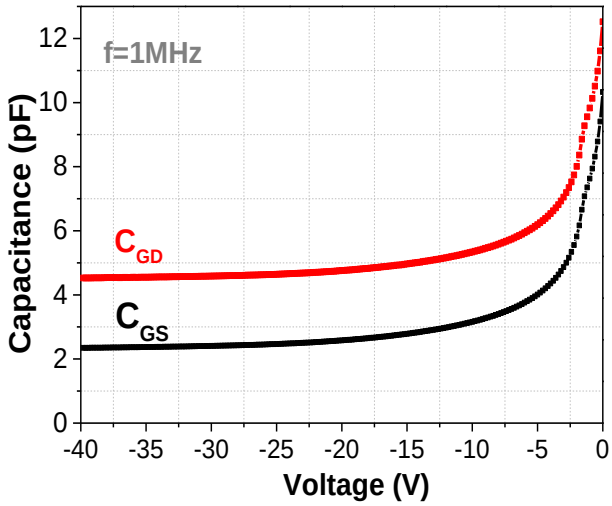


Fig.12b. **C_{GD}-V_{GD}** and **C_{GS}-V_{GS}** measurements.

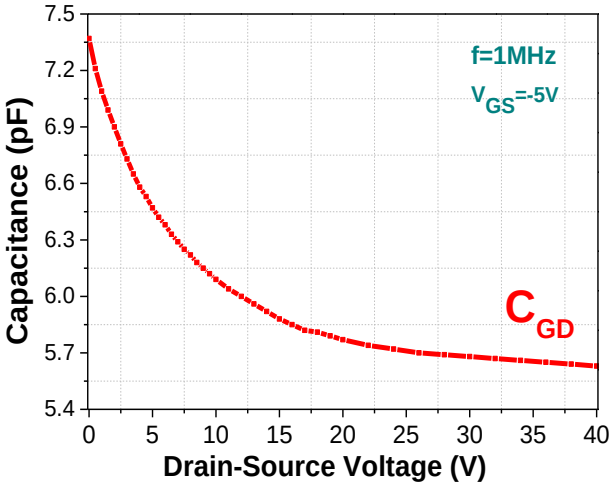


Fig.13a. C_{GD}-V_{DS} measurement.

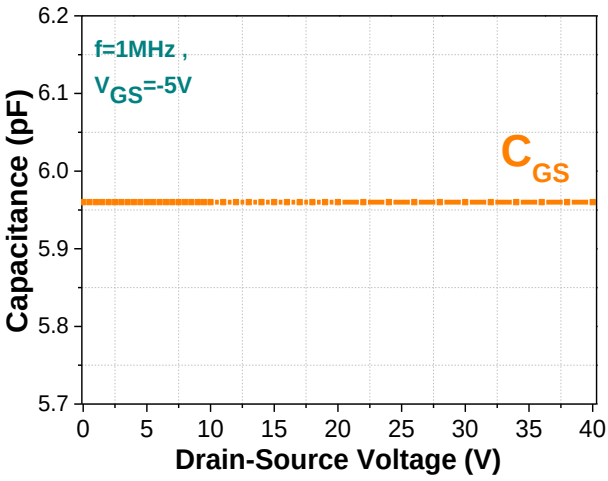


Fig.13b. C_{GS}-V_{DS} measurement.

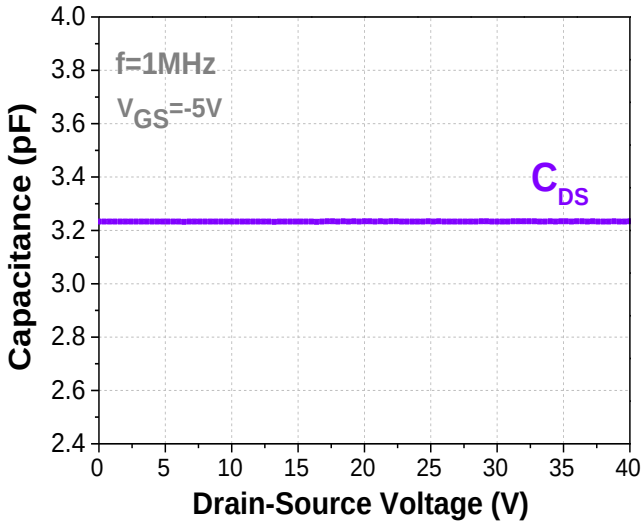


Fig.14. C_{DS}-V_{DS} measurement.

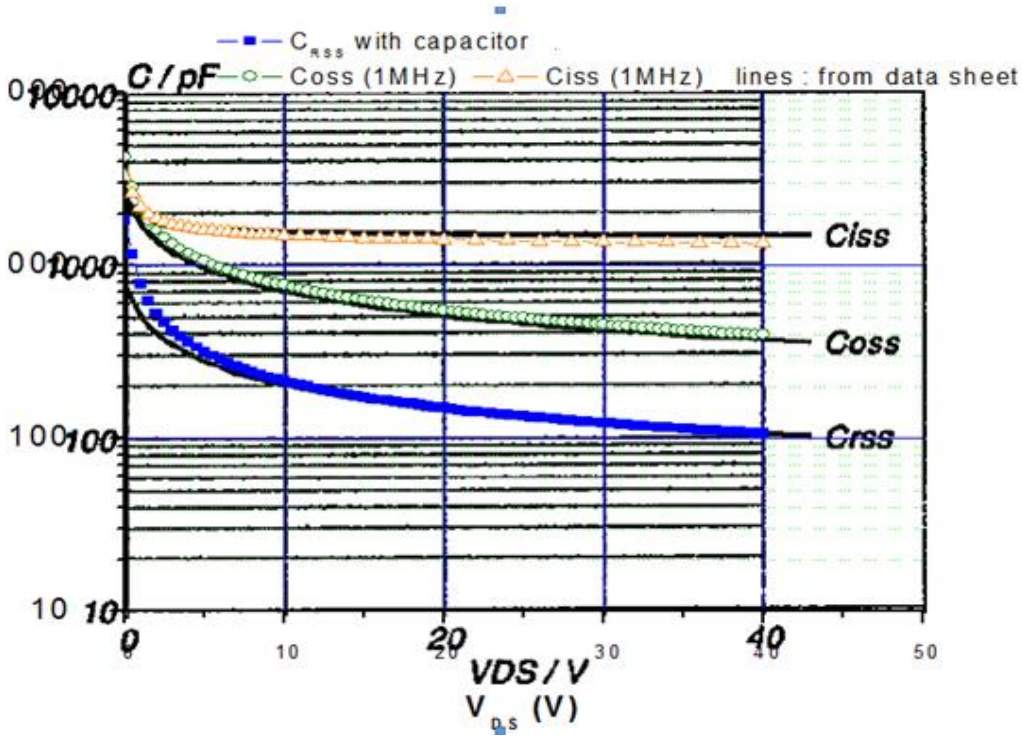


Fig.15. Typical capacitances C_{ISS}, C_{OSS}, C_{RSS} compared with the datasheet curves. Conditions: V_{GS}=0V, f=1MHz.

5. Bibliography

[1] "**Fundamentals of Semiconductor C-V Measurements**", Lee Stauffer, Keithley Instruments, Inc.

[2] "**Agilent Impedance Measurement Handbook",** A guide to measurement technology and techniques, 4th Edition

[3] **"Precise evaluation of Input, Output and Reverse Transfer Capacitances of Power devices",** Hisao Kakitani and Ryo Takeda – Agilent Technologies International, Japan Ltd.

[4] **"New technologies for wide band gap High-Power Semiconductor device characterization"**, Alan Wadsworth, Agilent Technologies APEC Session IS3.1-1

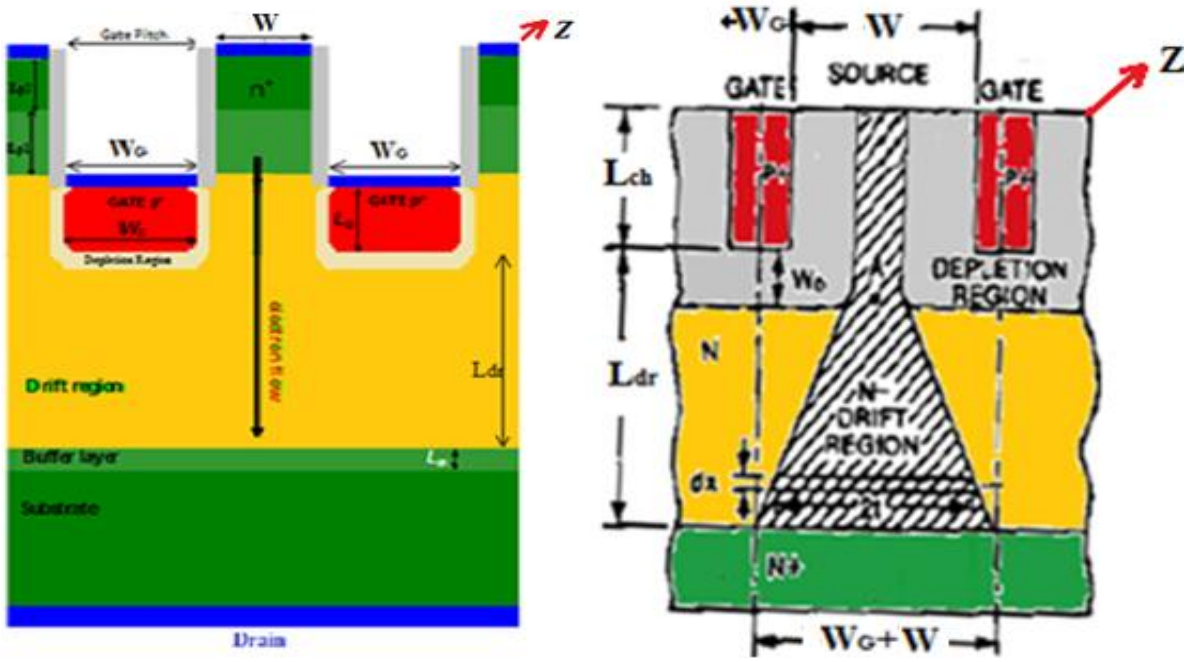
Appendix 2. Theoretical VJFET Analysis Handbook

The presented equations are in form that one has only to insert the red marked, input parameters expressed in their most common units for convenience and simplicity. In the second column we see the unit of the parameter whilst in the third column its usage is described.

In the table below all the input parameters are presented. The units in the "*Units for input*" column represent at which unit (most common) the parameter must be expressed in order to just insert the pure number in the equations and get the parameter value in its presented unit.

Input parameters

Symbol	*Meaning*	Units for input
L	*length*	*(μm)*
L_{ch}	*Channel length*	*(μm)*
L_{dr}	*Drift layer length*	*(μm)*
L_{pillar}	*Pillar total height*	*(μm)*
$L_{pillar/cont.}$	*Contact layer pillar height*	*(μm)*
N_D	*Donor dopant carrier concentration*	*(cm^{-3})*
N_A	*Acceptor dopant carrier concentration*	*(cm^{-3})*
n	*Number of fingers*	-
T	*Temperature*	*(K)*
t	*Thickness*	*(μm)*
V_A	*Voltage at point A*	*(V)*
V_D	*Drain Voltage*	*(V)*
V_G	*Gate Voltage*	*(V)*
W	*Mesa width* ($W_m=2a$)	*(μm)*
W_G	*Gate pitch*	*(μm)*
Z	*Mesa length*	*(μm)*



Cross-sections of TI-VJFET

Equations	Units	Usage/Comment
R_{ON} calculation		
1. $R_{ON} = R_{tot/finger} / n$	Ω	The finger (individual) resistances are connected in parallel.
2. $R_{tot/finger} = R_D^{cont.} + R_{sub} + R_{buf} + R_{drift} + R_{ch} + R_{pil^1} + R_{pil^2} + R_S^{cont.}$		Each finger resistance consists of the resistances of all the different layers.
3. $R = \frac{3.11\cdot10^{10} + 0.887\cdot N_D^{0.61}}{N_D\cdot T^{-2.15}} \frac{L}{(W+W_G)\cdot Z}\cdot10^4$	Ω	Substrate (R_{sub}) and buffer layer (R_{buf}) resistance calculation.
4. $R = \frac{3.11\cdot10^{10} + 0.887\cdot N_D^{0.61}}{N_D\cdot T^{-2.15}} \cdot \frac{L}{W\cdot Z}\cdot10^4$	Ω	n^- (R_{pil}^1) and n^+ (R_{pil}^2) part of the pillar resistance calculation..
5. $R_S^{cont.} = \frac{10^4}{W\cdot Z}$	Ω	Source contact ($R_S^{cont.}$) resistance calculation.
6. $R_D^{cont.} = \frac{10^4}{(W_G+W)\cdot Z}$		Drain contact ($R_D^{cont.}$) resistance calculation.
7. $R_{ch} = \frac{3.11\cdot10^{10} + 0.887\cdot N_D^{0.61}}{N_D\cdot T^{-2.15}} \cdot \frac{(L_{ch}+W_D)}{(W-2\cdot W_D)\cdot Z}\cdot10^4$	Ω	Channel (R_{ch}) resistance calculation.
8. $R_{dr} = \frac{3.11\cdot10^{10} + 0.887\cdot N_D^{0.61}}{N_D\cdot T^{-2.15}} \cdot \frac{(L_{dr}-W_D)}{Z(W_G+2W_D)} \ln\left(\frac{W+W_G}{W-2W_D}\right)\cdot10^4$	Ω	Drift layer (R_{drift}) resistance calculation.
$W_D = 3266.96\cdot10^4\sqrt{\frac{(V_{bi}-V_G)}{N_D}}$	μm	Depletion area's width at the Drain (W_D) side calculation, necessary for R_{ch} and R_{dr}.
V_{TH} calculation		
1. $V_{th} = -2.34\cdot10^{-16}\cdot N_D\cdot W^2 + 8.62\cdot10^{-5}\cdot T\cdot\ln\left(\frac{N_D\cdot N_A}{n_i^2}\right)$	V	Threshold voltage (V_{TH}) calculation.
$n_i = 3.95\cdot10^{15}\cdot T^{3/2} e^{-\frac{\left(3.267-6.5\cdot10^{-4}\cdot\frac{T^2}{T+1300}\right)\cdot5.8\cdot10^3}{T}}$	cm^{-3}	Intrinsic Carrier concentration calculation, necessary for the V_{TH} calculation.
g_m calculation		
1. $g_m = \frac{2.95\cdot10^{-6}\cdot Z\cdot T^{-2.15}}{(L_{ch}+W_D)(3.51\cdot10^{10}+N_D^{0.61})}\cdot10^{-4}\cdot\left(\sqrt{V_A+V_G+V_{bi}}-\sqrt{V_G+V_{bi}}\right)$	S	Transconductance (g_m) calculation.

$W_D = 3266.96 \cdot 10^4 \sqrt{\frac{(V_{bi} - V_G + V_D)}{N_D}}$	μm	Depletion area's width calculation at the Drain (W_D) side, necessary for g_m.
$V_{bi} = 8.63 \cdot 10^{-5} \cdot T \cdot \ln\left(\frac{N_D N_A}{n_i^2}\right)$	V	Built-in potential (V_{bi}) calculation, necessary for g_m.
$n_i = 3.95 \cdot 10^{15} \cdot T^{3/2} e^{-\frac{\left(3.267 - 6.5 \cdot 10^{-4} \cdot \frac{T^2}{T+1300}\right) \cdot 5.8 \cdot 10^3}{T}}$	cm^{-3}	Intrinsic Carrier concentration calculation, necessary for V_{bi} and consequently g_m.
$V_A = V_D - I_D \cdot R_D^{cont.} - I_D \cdot R_{sub} - I_D \cdot R_{buf} - I_D \cdot R_{dr}$	V	Calculation of potential at point A. Rough approximation → $V_A = V_D$
BV_{GS} calculation		
1. $BV_{GS} = \left(L_{pillar} - L_{pillar/cont.}\right) \cdot 3.25 \cdot 10^2 - V_{bi}$	V	Gate-Source breakdown voltage (BV_{GS}) calculation.
$V_{bi} = 8.63 \cdot 10^{-5} \cdot T \cdot \ln\left(\frac{N_D N_A}{n_i^2}\right)$	V	Built-in potential (V_{bi}) calculation, necessary for BV_{GS}.
$n_i = 3.95 \cdot 10^{15} \cdot T^{3/2} e^{-\frac{\left(3.267 - 6.5 \cdot 10^{-4} \cdot \frac{T^2}{T+1300}\right) \cdot 5.8 \cdot 10^3}{T}}$	cm^{-3}	Intrinsic Carrier concentration calculation, necessary for V_{bi} and consequently BV_{GS}.
Sheet Resistance (R_{sh}) calculation		
1. $R_{sh(cont.)} = \frac{3.11 \cdot 10^{10} + 0.89 \cdot N_D^{0.61}}{N_D \cdot T^{-2.15} \cdot t} \cdot 10^4$	(Ω/sq)	Contact layer ($R_{sh(cont.)}$) Sheet Resistance calculation.
2. $R_{sh(gate)} = \frac{3.11 \cdot 10^{10} + 0.89 \cdot N_A^{0.61}}{N_A \cdot T^{-2.15} \cdot t} \cdot 10^4$	(Ω/sq)	Gate layer ($R_{sh(gate)}$) Sheet Resistance calculation.

Below we see the initial formulas from which the presented ultimate equations have been extracted.

Calculation of R_{sub} and R_{buf}.:

$$R = \rho \frac{L}{S} \Rightarrow R = \frac{1}{q \mu N_D} \frac{L}{(W + W_G) \cdot Z}$$

Calculation of R_{pii}^1 and R_{pii}^2:

$$R = \rho \frac{L}{S} \Rightarrow R = \frac{1}{q \mu N_D} \frac{L}{W \cdot Z}$$

Calculation of R_{ch}:

$$R = \rho \frac{L}{S} \Rightarrow R_{ch} = \frac{1}{q \mu N_D} \frac{L_{ch} + W_D}{(W - 2W_D) \cdot Z}$$

Calculation of R_{dr}:

$$R = \rho \frac{L}{S} \ln\left(\frac{W_{Drain}}{W_{channel}}\right) \Rightarrow R_{dr} = \frac{1}{q\mu N_D} \cdot \frac{L_{dr} - W_D}{Z \cdot (W_G + W - (W - 2 \cdot W_D))} \cdot \ln\left(\frac{W_G + W}{W - 2 \cdot W_D}\right)$$

Calculation of V_{TH}:

$$V_{th} = -V_P + V_{bi} \Rightarrow V_{th} = -\frac{qN_D a^2}{2e_s} + \frac{kT}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

Calculation of g_m:

$$g_m = \frac{2aZq\mu N_D}{L} \cdot \left(\sqrt{\frac{V_D + V_G + V_{bi}}{V_P}} - \sqrt{\frac{V_G + V_{bi}}{V_P}}\right)$$

Calculation of BV_{GS}:

$$BV_{GS} = \left(L_{pillar} - L_{pillar/cont}\right) \cdot Ec - V_{bi}$$

Calculation of R_{sh}:

$$R_{sh} = \frac{\rho}{t} \Rightarrow R_{sh} = \frac{1}{q\mu N_D t}$$

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Appendix 3. Simulation files-MATLAB Code

Below we can see the MATLAB code for the current-voltage simulations. The codes for both the approaches of Field Dependent (FD) and Field Independent (Shockley), are presented. Next to every command of the code, the reader can find a comment (**%**) helping to understand the meaning of the calculated parameter or the command itself.

Field Dependent Mobility Approach

```
                                        %I-V_Field Dependent Operation
clc
clear all

q=1.602e-19;                    %Elementary charge
k=1.3806e-23;                   %Boltzman constant
es=8.55e-13;                    %Dielectric constant
T=300;                          %Temperature (T=300ºC)
Vs=2.2e7;                       %Saturation velocity for SiC
Ec=1e5;                         %Critical electric field for SiC

Nf=50;                          %number of fingers (fingers=50)
wch=1.5e-4;                     %channel width (wch=1.5um)
wg=4e-4;                        %gate width (wg=4um)
Z=256e-4;                       %mesa length (Z=256um)
Lg=0.3e-4;                      %gate length (Lg=0.3um)
Ldr=7.4e-4;                     %drift region length (Ldr=7.4um)
Lsub=372e-4;                    %substrate layer length (Lsub=372um)
Ng=1e19;                        %gate region doping profile (Ng=1E19cm-3)
Nch=5e15;                       %channel region doping profile (Nch=5E15cm-3)
Ndr=5e15;                       %drift region doping profile (Ndr=5E15cm-3)
Nsub=1.33e18;                   %substrate doping profile (Nsub=1.33E18cm-3)

V=zeros(100,1);                 %Matrix Initialization (100x1)
I=zeros(100,1);
Rdr=zeros(100,1);
R=zeros(100,1);
L=zeros(100,1);
Va=zeros(100,1);

a=wch/2;
Wb=wch+wg;
Nc=3.25e15*(T^1.5);                         %Effective density of states in the conduction band
Nv=4.8e15*(T^1.5);                          %Effective density of states in the valence band
Eg=3.265+0.033*((300^2)/(300+1e5)-(T^2)/(T+1e5));       %Energy bandgap
ni=sqrt(Nc*Nv)*exp(-Eg/(2*k*T*6.24e18));                %Intrinsic carrier concentration
m1=28+(950*((T/300)^(-2.4))-28)/(1+((T/300)^0.73)*((Nch/1.94e17)^(0.61)));  %channel mobility
m2=28+(950*((T/300)^(-2.4))-28)/(1+((T/300)^0.73)*((Ndr/1.94e17)^(0.61)));  %drift region mobility
Vth=-(q*Nch*(a^2))/(2*es)+(k*T/q)*log(Nch*Ng/(ni^2));       %Threshold voltage
Vbi=((k*T)/q)*log((Ng*Nch)/(ni^2));                         %Built in potential
Vp=(q*Nch*(a^2))/(2*es);                                    %Pinch-off voltage
Rcon=0.0001/((wch+wg)*Z);                   %contact resistance_Assumption for 10-4 Ohm*cm2
Rsub=((3.11*10^10+0.887*Nsub^(0.61))/(Nsub*T^(-2.15)))*Lsub/((wch+wg)*Z);%substrate resistance

VGS=-0;                 %definition of the gate voltage value for the simulation (VGS=0V)
Vgs=abs(VGS);
```

```
VA=-0.01;

for i=1:100
   VA=VA+0.01;          %sweeping the voltage of point A (VA) and accordingly calculation of Vds
   LA=sqrt(((2*es)/(q*Ndr))*(VA+Vgs+Vbi));        %drift region depletion width
   LA2=sqrt(((2*es)/(q*Nch))*(VA+Vgs+Vbi));       %channel region depletion width

     if wch>2*LA2  %necessary condition for current flow is the existence of channel,→wch>2*LA2
       Rd=(1/(q*m2*Ndr*Z))*((Ldr-LA)/(Wb-(wch-2*LA2)))*log(Wb/(wch-2*LA2));   %drift resistance
       Id=(((a^3)*(q^2)*m1*(Nch^2))/(3*es))*(Z/(Lg+LA))*((3*VA/Vp-2*((((VA+Vgs+Vbi)/Vp)^1.5)-…
           (((Vgs+Vbi)/Vp)^1.5)))/((1+((m1*VA)/(Vs*(Lg+LA)))^1.2)^(1/1.2))); %current calculation
       Vds=VA+Id*(Rd+Rcon+Rsub);        %calculation of Vds
       I(i)=Nf*Id;                       %total current
       V(i)=Vds;
       Rdr(i)=Rd;
       R(i)=Rdr(i)+Rcon+Rsub;                %Total resistance
     end
     L(i)=LA;
     Va(i)=VA;
end
     plot(V,I,'k')        %plot current in dependence on Vds
     hold on;


%ATTENTION!

%for positive gate-source voltage values (VGS>0), the sign of "Vgs" inside the for loop must be
%changed from "+Vgs" to "-Vgs".

%The values marked in grey are random and must be changed according to the dimensions and
%the structure of the simulated device. These values are noted in the comments (%) in brackets.
```

Field Independent Mobility (Shockley) Approach

```
                    %I-V_Field Independent Operation-Shockley Model (GCA)
clc
clear all

q=1.602e-19;              %Elementary charge
k=1.3806e-23;             %Boltzman constant
es=8.55e-13;              %Dielectric constant
T=300;                    %Temperature (T=300ºC)

Nf=50;                    %number of fingers (fingers=50)
wch=1.5e-4;               %channel width (wch=1.5um)
wg=4e-4;                  %gate width (wg=4um)
Z=256e-4;                 %mesa length (Z=256um)
Lg=0.3e-4;                %gate length (Lg=0.3um)
Ldr=7.4e-4;               %drift region length (Ldr=7.4um)
Lsub=372e-4;              %substrate layer length (Lsub=372um)
Ng=1e19;                  %gate region doping profile (Ng=1E19cm^-3)
Nch=5e15;                 %channel region doping profile  (Nch=5E15cm^-3)
Ndr=5e15;                 %drift region doping profile (Ndr=5E15cm^-3)
Nsub=1.33e18;             %substrate doping profile (Nsub=1.33E18cm^-3)

V=zeros(100,1);           %Matrix Initialization (100x1)
I=zeros(100,1);
Rdr=zeros(100,1);
R=zeros(100,1);
L=zeros(100,1);
Va=zeros(100,1);

a=wch/2;
Wb=wch+wg;
Nc=3.25e15*(T^1.5);                  %Effective density of states in the conduction band
Nv=4.8e15*(T^1.5);                   %Effective density of states in the valence band
Eg=3.267+0.033*((300^2)/(300+1e5)-(T^2)/(T+1e5));     %Energy bandgap
ni=sqrt(Nc*Nv)*exp(-Eg/(2*k*T*6.24e18));              %Intrinsic carrier concentration
m1=28+(950*((T/300)^(-2.4))-28)/(1+((T/300)^0.73)*((Nch/1.94e17)^(0.61)));  %channel mobility
m2=28+(950*((T/300)^(-2.4))-28)/(1+((T/300)^0.73)*((Ndr/1.94e17)^(0.61)));  %drift region mobility
Vth=-(q*Nch*(a^2))/(2*es)+(k*T/q)*log(Nch*Ng/(ni^2));        %Threshold voltage
Vbi=((k*T)/q)*log((Ng*Nch)/(ni^2));                          %Built in potential
Vp=(q*Nch*(a^2))/(2*es);                                     %Pinch-off voltage
Rcon=0.0001/((wch+wg)*Z);                %contact resistance_Assumption for 10^-4 Ohm*cm^2
Rsub=((3.11*10^10+0.887*Nsub^(0.61))/(Nsub*T^(-2.15)))*Lsub/((wch+wg)*Z); %substrate resistance

VGS=-0;                   %definition of the gate voltage value for the simulation (VGS=0V)
Vgs=abs(VGS);
VA=-0.01;

for i=1:100
   VA=VA+0.01;      %sweeping the voltage of point A (VA) and accordingly calculation of Vds
   LA=sqrt(((2*es)/(q*Ndr))*(VA+Vgs+Vbi));       %drift region depletion width
   LA2=sqrt(((2*es)/(q*Nch))*(VA+Vgs+Vbi));      %channel region depletion width

   if wch>2*LA2 %necessary condition for current flow is the existence of channel→wch>2*LA2
        Rd=(((1/(q*m2*Ndr*Z))*((Ldr-LA)/(Wb-(wch-2*LA2)))*log(Wb/(wch-2*LA2)))); %drift resistance
          if VA+Vgs+Vbi<Vp
            Id=(((a^3)*(q^2)*m1*(Nch^2))/(3*es))*(Z/(Lg+LA))*(3*VA/Vp-2*((((VA+Vgs+Vbi)/Vp)^1.5)…
                -(((Vgs+Vbi)/Vp)^1.5)));     %current calculation
          elseif VA+Vgs+Vbi>=Vp
```

```
            Id=(((a^3)*(q^2)*m1*(Nch^2))/(3*es))*(Z/(Lg+LA))*(1-3*(( Vgs+Vbi)/Vp)+2*(((Vgs+Vbi)…
                /Vp)^1.5)));                    %current calculation
          end
        I(i)=Nf*Id;                             %total current
        Vds=VA+Id*Rd+Id*Rcon+Id*Rsub;           %calculation of Vds
        V(i)=Vds;
        Rdr(i)=Rd;
        R(i)=Rdr(i)+Rcon+Rsub;                  %Total resistance
    end
    L(i)=LA;
    Va(i)=VA;
end
    plot(V,I)       %plot current in dependence on Vds
    hold on;


%ATTENTION!

%for positive gate-source voltage values (VGS>0), the sign of "Vgs" inside the for loop must be
%changed from "+Vgs" to "-Vgs".

%The values marked in grey are random and must be changed according to the dimensions and
%the structure of the simulated device. These values are noted in the comments in brackets.
```

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1) "4H-SiC VJFETs with self-aligned contacts"

K. Zekentes**,** A. Stavrinidis, G. Konstantinidis, M. Kayambaki, K. Vamvoukakis, E. Vassakis, K. Va ssilevski, Alton.B. Horsfall, N.G. Wright, P. Brosselard, S.Niu, M. Lazar, D. Planson, D. Tournier, N. Camara
Mat. Sci. Forum. *821-823* (2015) (Proc. of ECSCRM'14, Sept 2014, Grenoble, France) pp793-796

2) "Modelling of 4H-SiC VJFETs with self-aligned contacts"

K. Zekentes**,** K. Vassilevski, A. Stavrinidis, G. Konstantinidis, M. Kayambaki, K. Vamvoukakis, E. Vassakis, H. Peyre, N. Makris, M. Bucher, P. Schmid, D. Stefanakis, D. Tassis
(Proc. of ICSCRM'15, Oct. 2015, Catania, Italy)

3) "Electrical characterization procedure of power transistors: Application in the case of 4H-SiC VJFETs"

M. Vassakis, K. Vamvoukakis, M. Bucher, L. Liu, K. Zekentes

Proceedings of "37th Workshop on Compound Semiconductor Device and Integrated Circuits (WOCSDICE 2014)", Delphi, Greece, June 2014, p. 85

4) "TCAD simulations of 4H-SiC VJFETs"

D. Stefanakis, M. Vassakis, K. Vamvoukakis, L. Liu, D. Tassis, K. Zekentes

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5) "Electrical characterization of 4H-SiC VJFETs"

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