Technical University of Crete
Department of Electronic & Computer Engineering

Master Thesis

"System Level Analysis of a Direct-Conversion WiMAX Receiver at 5.3 GHz and Corresponding Mixer Design"

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Chania 2008

ACKNOWLEDGEMENTS

In the following paragraphs, I would like to acknowledge all the people, who helped me, each of them in his/ her own unique way, to accomplish my thesis.

First of all, I would like to acknowledge my supervising Professor Matthias Bucher for the assignment of this thesis, for his continuous support and guidance, and for his ideas that in essence have been implemented in this project. Also, I would like to thank both Professors Konstantinos Balas and Konstantinos Kalaitzakis for their participation in the three-party committee.

Special thanks should be directed to some people whose contribution to the overall work was significant. George Konstantopoulos motivated me to deal with the analog RF electronics research area and offered me his help, when needed. Many thanks should be also directed to the Electronics Laboratory fellow students, Nikolaos Makris, George Papoutsoglou, Athanasios Tsapras and Nikolaos Mavredakis.

Moreover, I would like to thank my friends and Georgia Nikolaou for their psychological support, especially in times of utter desperation.

Above all, I want to thank my beloved family to whom I owe my principles and values, for their love, sacrifices, companion, patience and support during my academic years

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CHAPTER 1: INTRODUCTION

1.1 Motivation

In recent years, wireless technology has emerged and taken the place of wired communications. Several technologies, such as WLAN, WiMAX, UWB, are used to cover the increasing demands in transfer rate and distance coverage.

Although Wireless Local Area Networks (WLAN), is still the dominating technology, covering distances of about 100 m and providing data rates of 54 Mbps, the need for more capacity (~70 Mbps) and longest coverage (~50 km), has rendered Worldwide Interoperability for Microwave Access (WiMAX) as the most promising technology in the immediate future.

Significant research is being dedicated to WiMAX, and the first networks are already in use covering the frequency bands in the range of 2.5 to 3.5 GHz. Therefore, the need for cost-effective, integrated transceivers, which comply with the requirements of the Wireless Metropolitan Area Network (WMAN) protocol, covering higher frequency bands, above 5 GHz, becomes even higher.

Based on the above motivations we present a system level analysis of a direct-conversion WiMAX receiver at 5.3 GHz, which can accommodate both fixed and mobile broadband applications. Furthermore, the circuit design of the corresponding downconversion mixer is presented.

The design is performed with a 0.25um SiGe BiCMOS technology. While the receiver presented in this work is implemented using MOS transistors only, the bipolars are used for the implementation of the power amplifier of the transmitter (not presented here).

1.2 WiMAX Overview

In 1998, the Institute of Electrical and Electronics Engineers (IEEE) formed a group called 802.16 to develop a standard for what was called a wireless metropolitan area network, or wireless MAN. Originally, this group focused on developing solutions in the 10GHz to 66GHz band, with the primary application being delivering high-speed connections to businesses that could not obtain fiber. After completing this standard, the group started work on extending and modifying it to work in both licensed and license-exempt frequencies in the 2 GHz to 11 GHz range, which would

enable non line of sight (NLOS) deployments. This amendment, IEEE 802.16a, was completed in 2003. Further revisions to 802.16a were made and completed in 2004. This revised standard, IEEE 802.16-2004, replaces 802.16, 802.16a, and 802.16c with a single standard, which has also been adopted as the basis for HIPERMAN (high-performance metropolitan area network) by ETSI (European Telecommunications Standards Institute). In 2003, the 802.16 group began working on enhancements to the specifications to allow vehicular mobility applications. That revision, 802.16e, was completed in December 2005 and was published formally as IEEE 802.16e-2005 [1].

There are two fundamentally different types of broadband wireless services. The first type attempts to provide a set of services similar to that of the traditional fixed-line broadband but using wireless as the medium of transmission. This type, called fixed wireless broadband, can be thought of as a competitive alternative to DSL or cable modem. The second type of broadband wireless, called mobile broadband, offers the additional functionality of portability, nomadicity, and mobility. Mobile broadband attempts to bring broadband applications to new user experience scenarios and hence can offer the end user a very different value proposition. WiMAX technology is designed to accommodate both fixed and mobile broadband applications.

Applications using a fixed wireless solution can be classified as point-to-point or point-to-multipoint. Point-to-point applications include interbuilding connectivity within a campus and microwave backhaul. Point-to-multipoint applications include broadband for residential, small office/home office (SOHO), and small- to medium-enterprise (SME) marketsT1 or fractional T1-like services to businesses, and wireless backhaul for Wi-Fi hotspots.

Clearly, one of the largest applications of WiMAX in the near future is likely to be broadband access for residential, SOHO, and SME markets. Broadband services provided using fixed WiMAX could include high-speed Internet access, telephony services using voice over IP, and a host of other Internet-based applications. Fixed wireless offers several advantages over traditional wired solutions. These advantages include lower entry and deployment costs; faster and easier deployment and revenue realization; ability to build out the network as needed; lower operational costs for network maintenance, management, and operation; and independence from the incumbent carriers.

The bandwidth and reach of WiMAX make it suitable for the following potential applications:

- Connecting WiFi hotspots with each other and to other parts of the Internet
- Providing a wireless alternative to cable and DSL for last mile broadband access
- Providing high-speed data and communications services
- Providing nomadic connectivity

A WiMAX system consists of two parts:

A WiMAX tower and a WiMAX receiver. The WiMAX tower, similar in concept with a cellular phone tower can cover a very large area as big as ~8000 square km. The receiver and antenna could be a small box, such as a PCMCIA card, or they could be built into a laptop, the way WiFi is. A WiMAX tower station can connect directly to the Internet using a high-bandwidth, wired connection (for example, a T3 line). It can also connect to another WiMAX tower using a line-of-sight, microwave link. This connection to a second tower (often referred to as a backhaul), along with the ability of a single tower to cover up to 8,000 square km, is what allows WiMAX to provide coverage to remote rural areas.

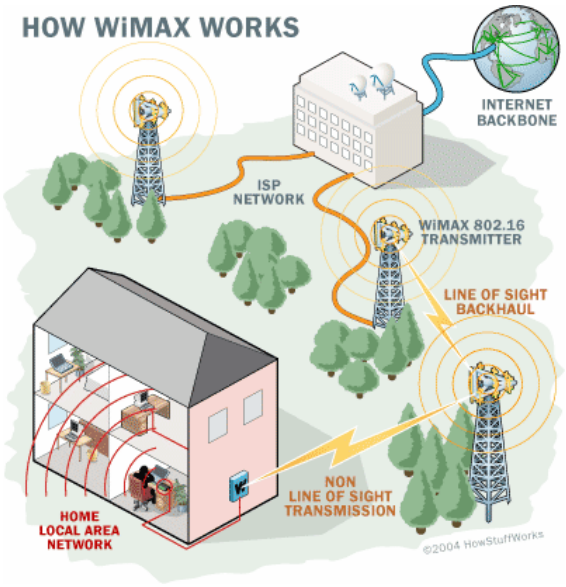


Figure 1

How WiMAX works

What the above Figure points out is that WiMAX actually can provide two forms of wireless service:

- There is the non-line-of-sight, WiFi sort of service, where a small antenna on your computer connects to the tower. In this mode, WiMAX uses a lower frequency range, 2 GHz to 11 GHz (similar to WiFi). Lower-wavelength transmissions are not as easily disrupted by physical obstructions -- they are better able to diffract, or bend, around obstacles.
- There is line-of-sight service, where a fixed dish antenna points straight at the WiMAX tower from a rooftop or pole. The line-of-sight connection is stronger and more stable, so it's able to send a lot of data with fewer errors. Line-of-sight transmissions use higher frequencies, with ranges reaching a possible 66 GHz. At higher frequencies, there is less interference and much more bandwidth.

The fastest WiFi connection can transmit up to 54 megabits per second under optimal conditions. WiMAX should be able to handle up to 70 megabits per second. Even once those 70 megabits is split up between several dozen businesses or a few hundred home users, it will provide at least the equivalent of cable-modem transfer rates to each user.

WiFi's range is about 30 m while WiMAX can provide a 50 km coverage with wireless access, under ideal conditions. The increased range is due to the frequencies used and the power of the transmitter. Of course, at that distance, terrain, weather and large buildings will act to reduce the maximum range in some circumstances, but the potential is there to cover large distances.

1.3 Block Diagram

The process that has been followed is presented in Figure 2. Once the system level analysis is done, the specifications for each of the receiver’s blocks are derived. If these specifications comply with the WiMAX standard requirements, then we may proceed to the mixer design. In case of a disagreement, then we have to go back to the system level analysis and resimulate. Upon completion of the mixer design, we have to check whether the specifications of the mixer block agree with the equivalent specifications that resulted during the system level analysis, or not. Unless they agree

the mixer design has to be reconsidered. In case of an agreement, we may continue with the statistical analysis and the integration of the mixer design.

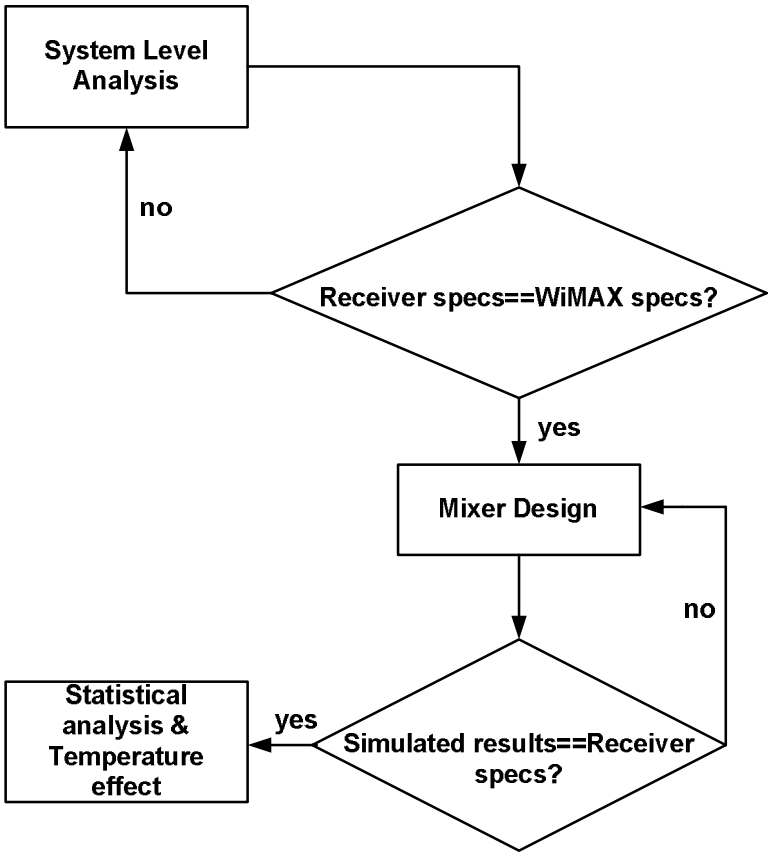


Figure 2
Block diagram

1.4 Thesis Overview

The thesis is separated in five chapters. In the second chapter, receiver architectures are presented together with their advantages and disadvantages. Design issues are considered and the overall receiver architecture is presented. Measurements concerning the figures of merit of the individual receiver blocks, i.e. noise figure (NF), phase noise, linearity, conversion gain (CG), are also presented. Finally, the specifications of the low noise amplifier, the mixer, the voltage controlled oscillator, the filters and the voltage gain amplifier are presented.

In the third chapter, the mixer topologies and their operation are described. The trade-offs resulting among the figures of merit are discussed and optimization techniques are presented.

A mixer design guide is presented in chapter four. Specifically, the mixer design process in Advanced Design System (ADS) 2006 is given in detail and the simulation results for the CG, the NF, and the linearity are shown. These have to be in compliance with the specifications that have derived from the system level analysis. Moreover, a statistical analysis together with the effect of the temperature on mixer's performance is carried out.

Eventually, chapter five entails a comparison with previously published mixer topologies, in the frequency range of 5 GHz, as well as the final mixer's specifications, i.e. transistors' width/length.

CHAPTER 2: RECEIVER ARCHITECTURE

2.1 Receiver Architectures

Receiver architectures may be separated into two categories. Heterodyne receivers and homodyne receivers. Each of the architectures experiences some advantages and some disadvantages, which are going to be analytically discussed further on. It is up to the application and its specifications, which of the two, the designer will choose to implement.

2.1.1 Heterodyne Receivers

In heterodyne [2] (hetero – different, dyne – to mix) architectures, the radio frequency (RF) signal is translated to an intermediate frequency (IF) signal, a lower frequency signal. This is carried out by means of a mixer, which in this chapter, is viewed as a simple analog multiplier. To bring the center frequency from w_1 (RF) to w_2 (IF), the signal is first mixed with a sinusoid $A_0 \cos w_0 t$, where $w_0 = w_1 - w_2$. After the mixing process, two bands are yielding. The first one around w_2 and the second one around $2w_1 - w_2$. A low pass filter then removes the latter. Because of its typical high noise, the mixer component is preceded by a low noise amplifier (LNA). The sinusoid is generated by a local oscillator with $w_{LO} = w_0$.

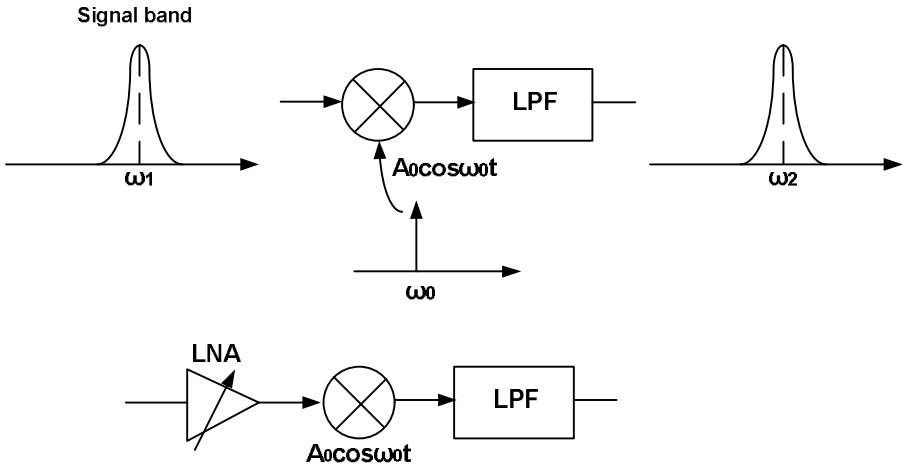


Figure 3

Simple Heterodyne Downconversion

2.1.1.1 Problem of Image

The principal consideration as far as the choice of the LO and the IF frequency is concerned, is the "image frequency". A simple analog multiplier does not preserve the polarity of the difference between its two input frequencies, i.e. for $x_1(t) = A_1 \cos w_1 t$ and $x_2(t) = A_2 \cos w_2 t$, the low pass filtered product of $x_1(t)$ and $x_2(t)$ is of the form $\cos(w_1 - w_2)t$, no different from $\cos(w_2 - w_1)t$. Thus, in a heterodyne architecture, the bands symmetrically located above and below the LO frequency are downconverted to the same center frequency (Figure 4). If the band of interest is centered around $w_1 = (w_{LO} - w_{IF})$, then the image is around $2w_{LO} - w_1 (= w_{LO} + w_{IF})$

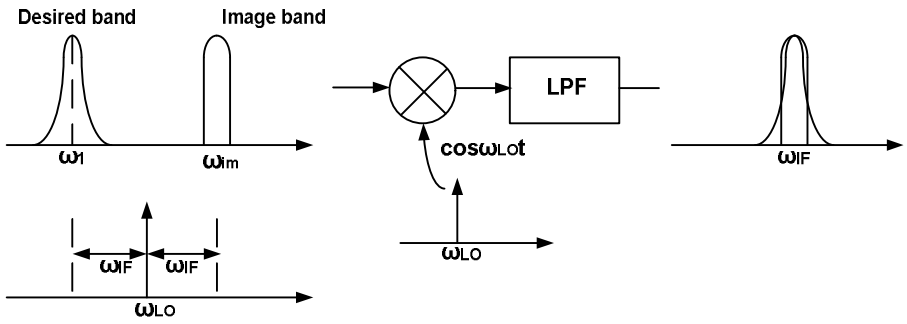


Figure 4
Problem of image in heterodyne reception

The problem of image is a serious one. While each wireless standard imposes constraints upon the signal emissions by its own users, it may have no control over the signals in other bands. The image power could therefore be much higher than that of the desired signal, requiring proper image rejection.

The most common approach to suppressing the image is through the use of an image reject filter, placed before the mixer. As depicted in Figure 5, the filter is designed to have a relatively small loss in the desired band and a large attenuation in the image band, two requirements that can be simultaneously met if $2w_{IF}$ is sufficiently large.

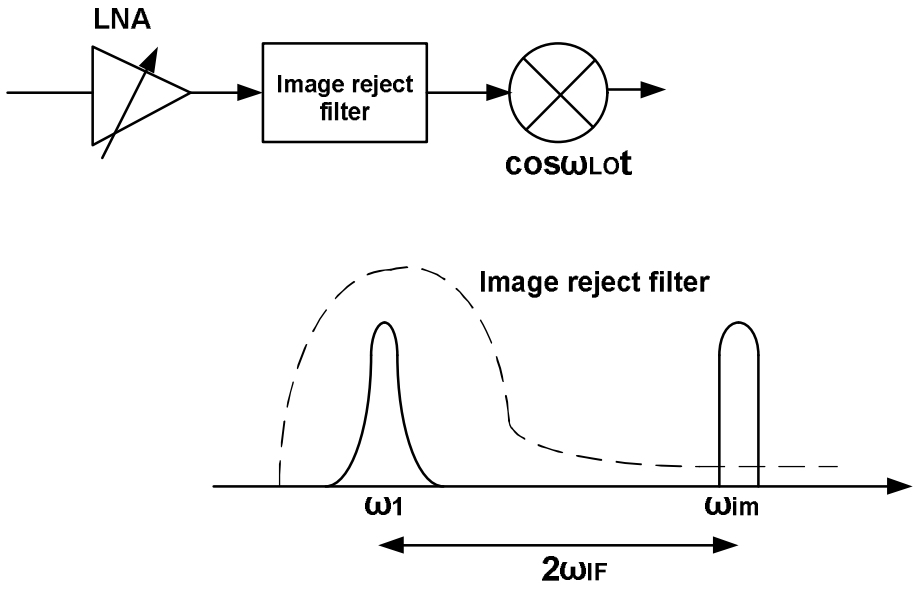


Figure 5
Image rejection by means of a filter

2.1.2 Homodyne Receivers

In contrast to heterodyne architectures, homodyne (homo – same, dyne – to mix) receivers perform direct-conversion (zero IF), entailing different issues from the heterodyne architectures [2].

Shown in Figure 6 is a simple homodyne receiver, where the LO frequency is equal to the input carrier frequency. The simplicity of this architecture offers an important advantage over the heterodyne counterpart. The problem of image does not exist since $w_{IF} = 0$. Thus, an image filter is not required and the complexity of the entire chain is reduced.

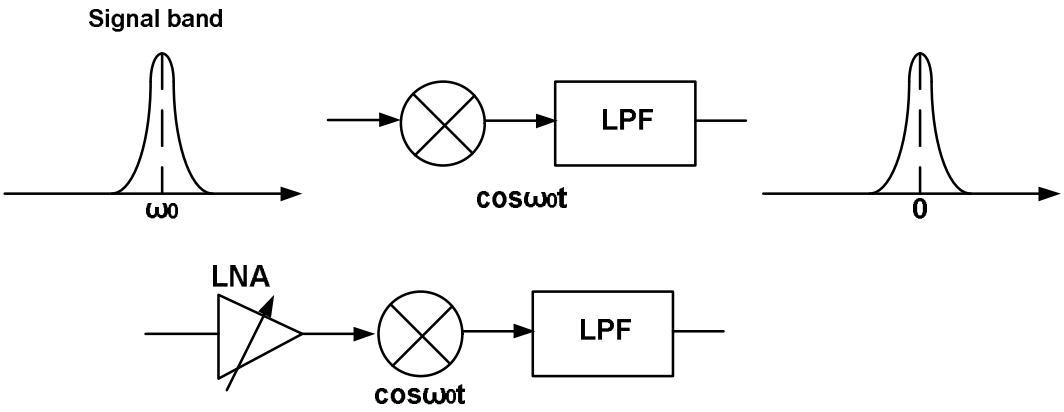


Figure 6

Simple homodyne receiver

Though, direct conversion has some drawbacks which are not present in heterodyne architectures.

2.1.2.1 Channel Selection

Rejection of out-of-channel interferers by an active filter is more difficult than by a passive filter, fundamentally because active filters exhibit much more severe noise-linearity-power trade-offs than do their passive counterparts. There are three choices as far as rejection is concerned.

A low-pass filter could be used prior to the amplifier stage, in order to suppress out-of-channel interferers, allowing A_1 (Figure 7a) being a nonlinear, high-gain amplifier and the analog-to-digital (ADC) converter to have a moderate dynamic range. However, the low-pass filter imposes tight noise-linearity trade-offs.

The second permutation shown in Figure 7b, relaxes the low pass filter (LPF) noise requirements while demanding a higher performance in the amplifier. A linearized one-stage differential amplifier may be employed here to provide some gain before channel filtering. Furthermore, another amplifier may be interposed between the LPF and the ADC to overcome the noise of the latter.

The third permutation, Figure 7c, suggests the possibility of channel filtering in the digital domain. In this case the ADC must achieve a high linearity, so as to digitize the signal with minimal intermodulation of interferers, as well as exhibit a thermal and quantization noise floor well below the signal level.

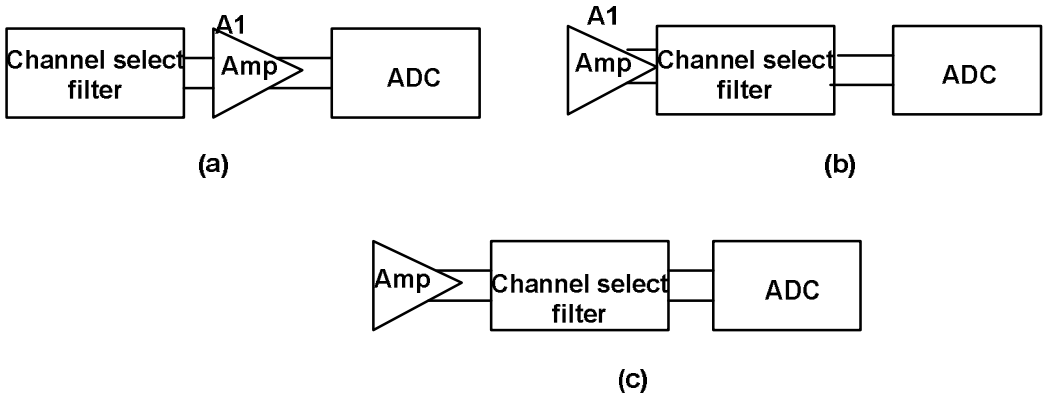


Figure 7

Three permutations of baseband functions

2.1.2.2 DC Offsets

Since in a homodyne topology the downconverted band extends to zero frequency, extraneous offset voltages can corrupt the signal and, more importantly, saturate the following stages. Figure 8 shows the origin and impact of offsets.

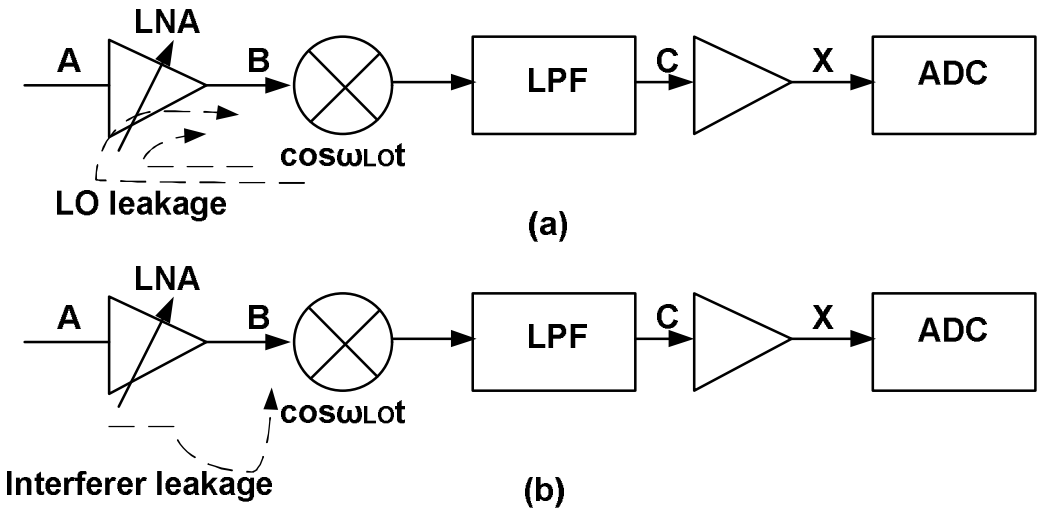


Figure 8

Self mixing of (a) LO signal, (b) a strong interferer

First the isolation between the LO port and the inputs of the mixer and the LNA is not infinite; that is, a finite amount of feedthrough exists from the LO port to nodes A and B (Figure 8a). The leakage signal is mixed with the LO signal, producing a DC component at point C (self-mixing). The same happens if a strong interferer flows from the LNA or the mixer to the LO port and is multiplied by itself.

The overall gain from the antenna to point X is about 80-100 dB, so that the attenuated input signal is amplified to a level that can be digitized by a low cost and power ADC. Typically 25-30 dB is contributed by the LNA/mixer combination.

If the LO signal leaks to the antenna and is radiated and subsequently reflected by moving objects back to the receiver, it may be difficult to distinguish the time-varying offset from the actual signal.

In heterodyne architectures, the offset problem is much less serious. This is because the LO frequency differs from the carrier frequency. Thus, the self-mixing phenomenon may occur only for interferers. In such a case, the DC offset may be removed due to the fact that the IF signal is not centered around zero frequency, as happens in homodyne receivers.

2.1.2.3 Flicker Noise

As mentioned earlier, the gain through the front-end LNA and mixer is typically around 30 dB, yielding baseband signals in the range of tens of microvolt. The input noise of the following stages is therefore still critical. In particular, since the downconverted spectrum extends to zero frequency, the $1/f$ flicker noise of devices substantially corrupts the signal, a severe problem in MOS implementations. So, it is desirable to achieve a relatively high gain in the RF range.

The effect of flicker noise can be reduced by a combination of techniques. As the stages following the mixer operate in lower frequencies, they can incorporate very large devices to minimize the magnitude of the flicker noise. Moreover, periodic offset cancellation also lowers noise. In addition, the downconverted signal and hence the noise can be high-pass filtered.

2.1.2.4 LO Leakage

In addition to introducing DC offsets, leakage of the LO signal to the antenna and radiation creates interference in the band of other receivers using the same wireless standard. The design of the wireless standard and the regulations of the federal communications commission (FCC), impose upper bounds on the amount of in-band radiation.

2.2 Proposed Architecture

In this paragraph the receiver requirements, resulting from the IEEE 802.16 standard are presented, together with the proposed receiver architecture. Moreover, the simulation process is described and the derived simulation results are shown. Finally, the specifications of the individual components are exported. The objective is to comply with them, while proceeding to the mixer circuit design, which will be presented in chapters 3 and 4.

2.2.1 Receiver Requirements

Receiver requirements determined by the WirelessMAN (WMAN) protocol deal with the signal to noise ratio (SNR), the noise figure (NF), the adjacent and alternate channel rejection, the receiver maximum input signal, the maximum tolerable signal and the image rejection

Table 1 depicts the minimum SNR for different types of modulation and coding rates. We see that going from 16 to 64 QAM modulations, the respective SNR increases.

Modulation	**Coding rate**	**Receiver SNR [dB]**
BPSK	½	6.4
QPSK	½	9.4
	¾	11.2
16-QAM	½	16.4
	¾	18.2
64-QAM	2/3	22.7
	¾	24.4

Table 1

Receiver SNR assumptions

The adjacent and nonadjacent channel rejection are presented in Table 2

Modulation/Coding	**Adjacent channel interference [dB]**	**Nonadjacent channel rejection [dB]**
16-QAM/ ¾	-11	-30
64-QAM/ ¾	-4	-23

Table 2

Adjacent and nonadjacent channel rejection

The minimum sensitivity the receiver should have is given in Table 3 [3].

Modulation	**Coding rate**	**Sensitivity [dBm]**
QPSK	½	-80
	¾	-78
16-QAM	½	-73
	¾	-71
64-QAM	2/3	-66
	¾	-65

Table 3

Receiver Sensitivity

The receiver shall be capable of decoding a maximum on-channel signal of 30 dBm and tolerate a maximum signal of 0 dBm without damage. The receiver shall also provide a minimum image rejection of 60 dB and introduce a maximum NF of 7 dB[1].

The receiver bands used in WiMAX are the 10-66 GHz licensed bands and the frequencies below 11 GHz. In the second category, the bands around 2.5 to 3.5 GHz and 5 to 6 GHz are mainly used.

2.2.2 Receiver overview – Design flow

The homodyne architecture (Figure 9) is used. The direct conversion architecture enhances image rejection, compared to the heterodyne architecture. Moreover, direct conversion decreases receiver complexity, since the usage of an image-reject filter is unnecessary. This in turn reduces the number of the receiver blocks, thus relaxing the specifications of the individual components.

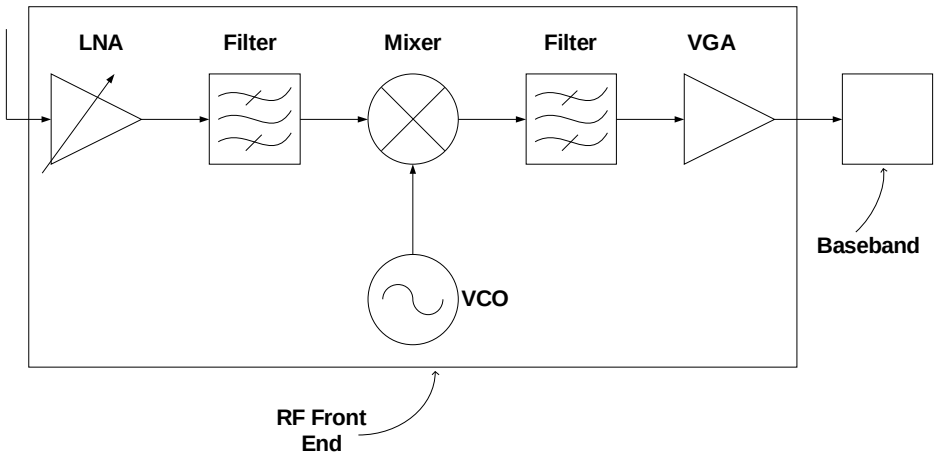


Figure 9

Direct-conversion receiver

The RF front-end consists of a low-noise amplifier (LNA), two band-pass filters, a mixer, a voltage controlled oscillator (VCO) and a voltage gain amplifier (VGA).

The RF signal, received by the antenna, modulated with 64-QAM with a coding rate of 3/4, is about -65 dBm (Table 3). It is centered around 5.3 GHz and should firstly be amplified by a LNA, because of the attenuation it has undergone during transmission. Subsequently, a band-pass filter isolates the out-of-channel interferers as well as cuts-off the frequency bands below 10 MHz or above 20 MHz (bandwidth of the WiMAX signal). Next, the signal passes through the mixer stage, where downconversion occurs. The local oscillator (LO) signal feeding the mixer is produced by a VCO, giving a signal at a power of -5 dBm, much stronger than the RF signal. The LO signal is centered at 5.29 GHz. The resulting signal is a pass-band signal of 10 MHz, filtered and amplified by a VGA, before being demodulated.

2.2.3 Receiver Simulation – System Level Analysis

The first stages of the chain (LNA and mixer) are the main contributors to the overall noise figure, whereas the latter stages (VGA) are mainly responsible for the linearity. The receiver's noise figure is also affected by the VCO phase noise at various offsets from the fundamental frequency. A parametric analysis is carried out to acquire the specifications of the individual blocks.

The analysis is performed in Advanced Design System (ADS) 2006. Each of the blocks, i.e. LNA, VCO, mixer, VGA, is described by a behavioural model available also within ADS, and contains the basic figures such as noise figure and phase noise, gain, insertion loss, linearity etc, as shown below.

Low noise amplifier

- S21, forward transmission gain
- TOI, 3rd order intercept point
- NF, noise figure, in dB

Band pass filter Chebyshev

- Fcenter, center passband frequency
- BWpass, passband edge-to-edge width
- Apass, attenuation at passband edges, in dB
- BWpass, stopband edge-to-edge width, in dB
- Astop, attenuation at stopband edges
- IL, passband insertion loss, in dB

Mixer

- SideBand, specify the sideband/image option for the mixer
- ConvGain, conversion gain
- NF, noise figure, in dB
- TOI, 3rd order intercept point

Voltage-controlled oscillator with phase noise

- Freq, the LO center frequency
- P, LO output power
- Phase Noise, phase noise data

Voltage gain amplifier

- S21, forward transmission gain

- TOI, 3rd order intercept point
- NF, noise figure, in dB

A harmonic balance (HB) noise controller provides the opportunity of evaluating the phase noise effect on the overall noise figure. The VCO phase noise is calculated for four different offsets. The aim is to keep the total noise figure lower than the aforementioned 7 dB required by the WMAN protocol. A two-tone HB simulation is performed to obtain the total noise figure of the receiver versus the phase noise of the VCO, for different values of the noise figure of the LNA.

2.2.4 Simulation Results-Specifications

The simulation results for the system level analysis are given below. The RF signal is a signal of -65 dBm at 5.3 GHz, whereas the LO signal is centered at 5.29 GHz at a power of -4 dBm. The IF signal, resulting from the mixing of the RF and the LO signal, is about -1 dBm at 10 MHz. Except for the signals at the fundamental frequencies, undesired interfering signals at multiple frequencies are also present at the output of each stage (RF, LO, IF).

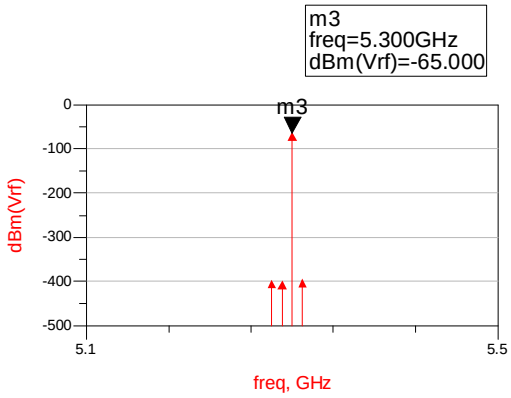


Figure 10

RF signal

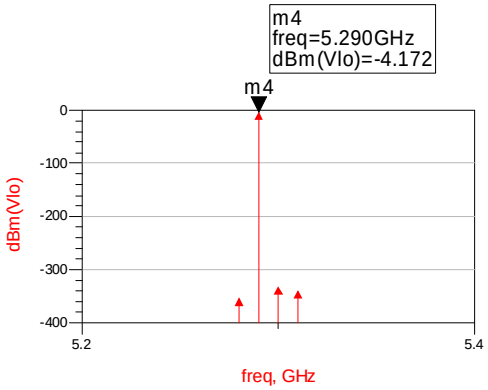


Figure 11

LO signal

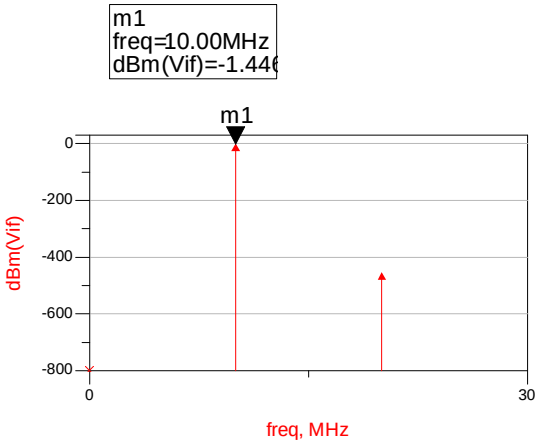
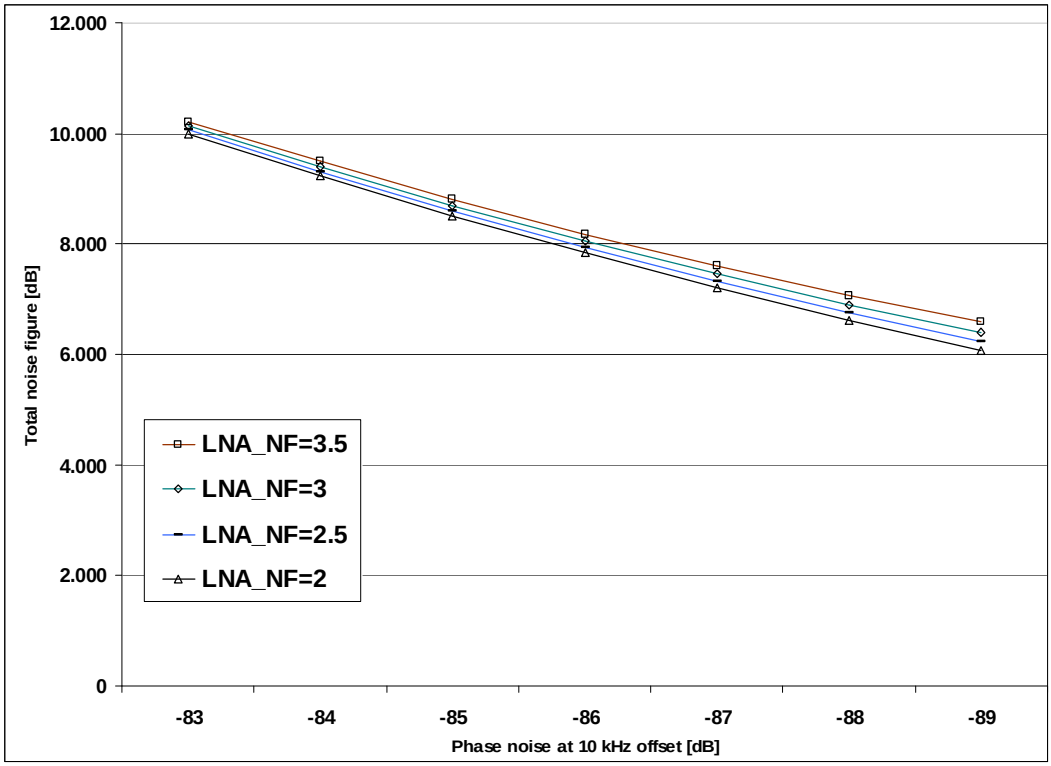


Figure 12

IF signal

The total noise figure in respect to the VCO phase noise at four different offsets from the central frequency of 5.29 GHz, and for several values of the LNA noise figure is demonstrated in Figure 13. The phase noise is swept from -83 to -89 dB, for the 10 kHz offset. For an offset of 100 kHz it is swept from -105 to -110 dB, while for an offset of 600 kHz it varies from -120 to -125 dB. Finally for a frequency offset of 1 MHz, the phase noise is swept from -125 to -130 dB. The noise figure of the LNA is swept from 3.5 to 2 dB with a step of 0.5 dB. Observing the resulting figures, we conclude that in order to preserve that the total noise figure of the receiver remains under the acceptable value of 7 dB, the phase noise for a frequency offset of 10 kHz, 100 kHz, 600 kHz and 1 MHz should be -88 dB, -110 dB, -125 dB and -130

dB, respectively. The corresponding maximum value for the noise figure of the LNA is 3 dB.



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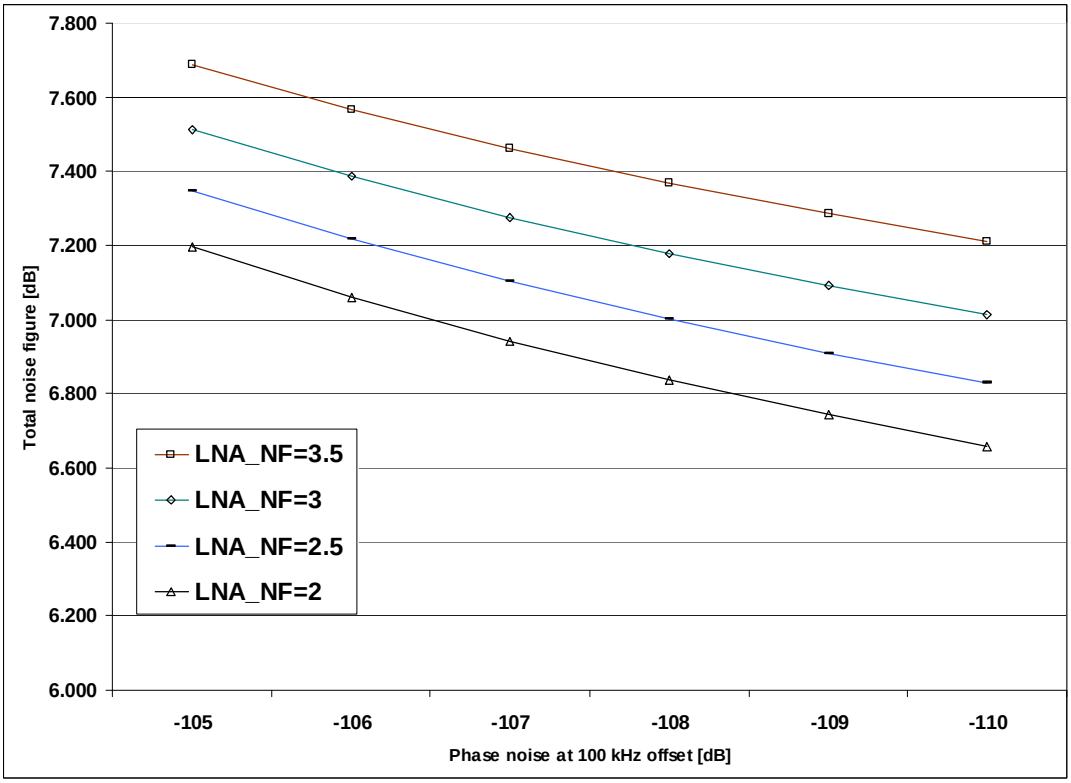

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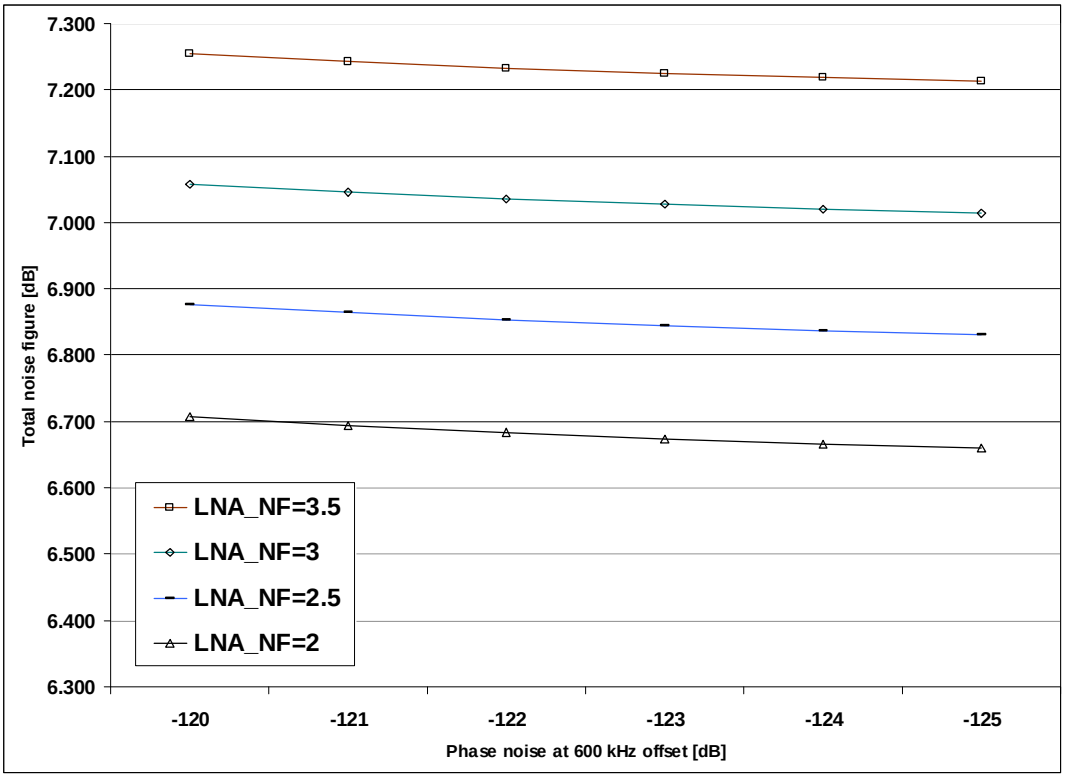

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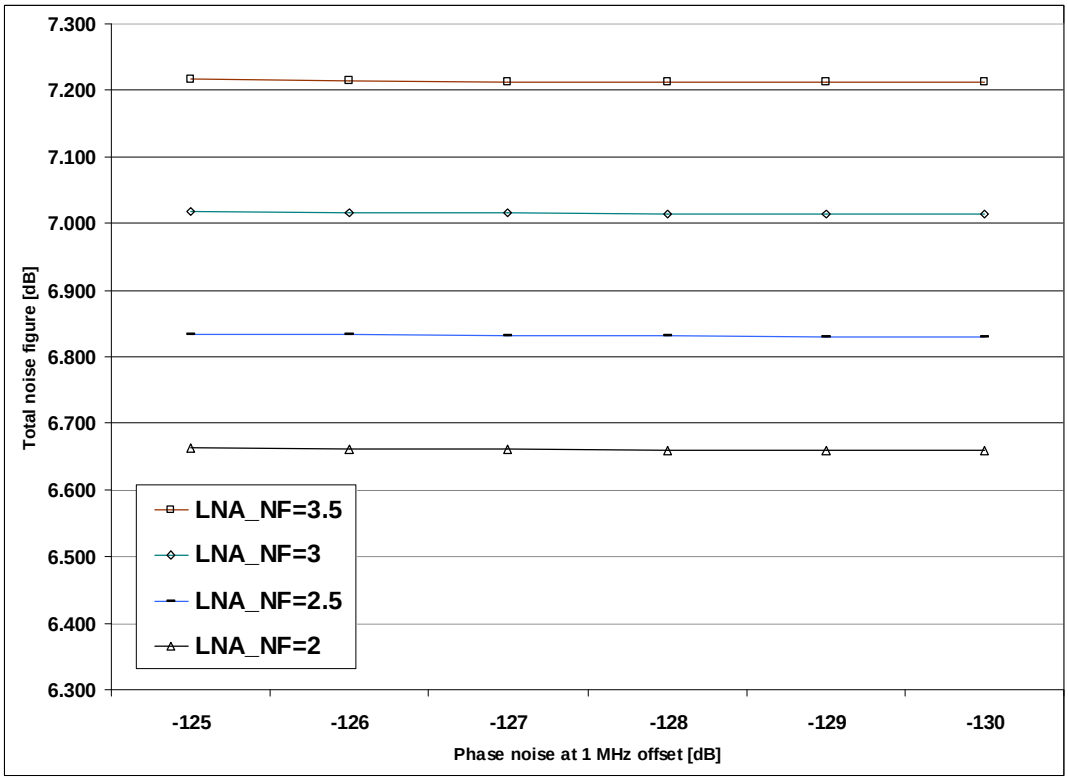


(d)

Figure 13

(a) NF vs. phase noise @ 10 kHz, (b) NF vs. phase noise @ 100 kHz, (c) NF vs. phase noise @ 600 kHz, (d) NF vs. phase noise @ 1 MHz

The VCO phase noise power in dBc (dB with respect to carrier), as well as the noise figure, the conversion gain and the input 3rd order intercept point of the remaining components are presented in Table 4. While proceeding to the mixer design we have to consider that its specifications have to be in compliance with the specifications presented in Table 4. Thus, its conversion gain should be 8 dB at least, its noise figure 6 dB maximum, and its IIP3 6 dBm.

	LNA	**Filter**	**Mixer**	**VCO**	**VGA**
NF [dB]	3	2	6	-	5
CG [dB]	18		8	-	40
IIP3 [dBm]	-7		6	-	12
Phase noise [dBc]	-	-	-	-88 @ 10 kHz, -110 @ 100 kHz, -125 @ 600 kHz,-130 @ 1 MHz	-

Table 4

Receiver specifications

CHAPTER 3: INTEGRATED MIXERS

3.1 Basics of Mixers

It is widely known that signal processing in digital receivers, either digital or analog, is performed in baseband frequencies. Thus, existence of circuits performing frequency translation from frequency of transmission and reception to baseband frequency is necessary. These circuits are called mixers and perform frequency translation among baseband, RF and IF frequencies. Because of its location and its operation, the mixer is the most critical block in the receiver chain. Integrated mixers are in essence multiple input circuits. Except for the useful signal, mixers also have a second input, the strong signal coming from a local oscillator (Figure 14). The objective is the mixing of these signals. It goes without doubt that mixers are not autonomous circuits but always need occurrence of local oscillators. There are two basic types of mixers: passive and active, the pros and cons of which are going to be discussed below.

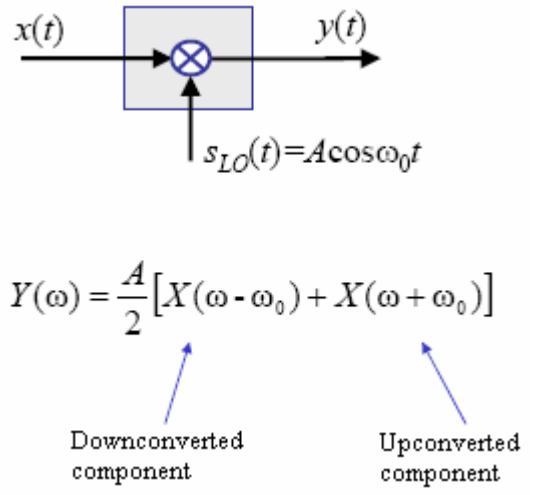


Figure 14

Mixer operation

3.2 Mixer Categories

There are two basic categories of mixers, passive and active mixers. Passive mixers include passive components (resistors, capacitors, diodes). In contrast, using the term “active mixers”, we refer to mixers including active elements, such as bipolar and MOS transistors or even operational amplifiers. What differs passive from active mixers is the current consumption. Thus, in passive mixers the transistors are not flown from DC currents and usually can be thought of, as resistors controlled by

voltage (operating in active region), whereas in active mixers transistors operate in saturation region. It is worth saying that active mixers may also include passive components.

3.2.1 Passive Mixers

The simplest passive mixer topology is shown in Figure 15. Signal $V_{LO}(t)$ is strong enough so that the diode D is on for half of its period. The diode's conductivity voltage has to be overpassed, so that the current flows through D. Thus a bias voltage V_{bias} may be used for proper diode biasing.

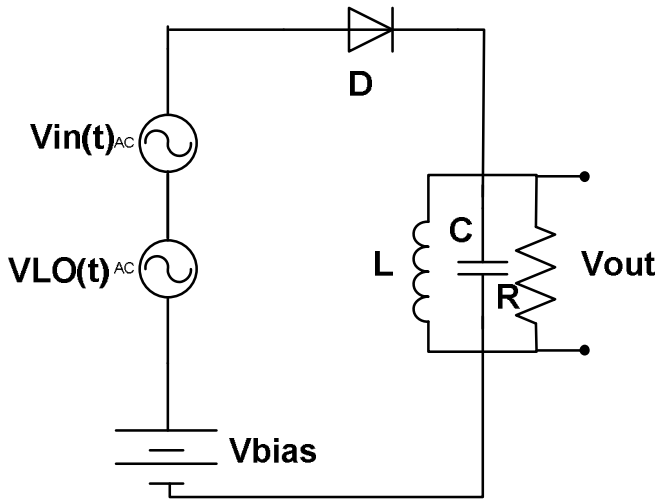


Figure 15

Simple passive diode mixer topology

The useful signal $V_{in}(t)$ appears at the output periodically and specifically during half of the LO period. Supposing low frequency operation and strong LO signal, this voltage may be described by the above equation:

$$\begin{aligned} &V_{out}(t) = u(t) \cdot V_{in}(t) \\ &, where \\ &u(t) = 1 when V_{LO}(t) \geq 0 \\ &u(t) = 0 when V_{LO}(t) \leq 0 \end{aligned} \tag{1}$$

At the mixer output the signal resulting from the mixing between the input and the LO signal appears. The useful signal frequency will be either the sum or the difference of the two signal frequencies. The LC resonating circuit in Figure 15 is

used to create maximum output resistance at the desired frequency and to cut off harmonics inevitably produced during the mixing process.

The above topology exploits the useful signal only during half of the LO signal period resulting in low conversion gain. A more efficient topology is the ring mixer topology, presented in Figure 16. Diodes actually operate as switches controlled by the LO signal. Nodes A and B are virtual grounds of the LO signal, while nodes C and D are virtual grounds of the input signal. During the first half of the LO period, where node C experiences a higher potential than node D, diodes D1 and D2 are on, whereas D3 and D4 are off. During the second half, operation is reversed with diodes D3, D4 being on and D1, D2 being off. When D1 and D2 are on, node A is considered as an open-circuit. As a result, portion of the input current flows to the output, depending on transformers quality, spiral ratio and output resistance. During the other half of the LO signal period, node A acts as a virtual ground and an equal input current portion with different sign appears at the output.

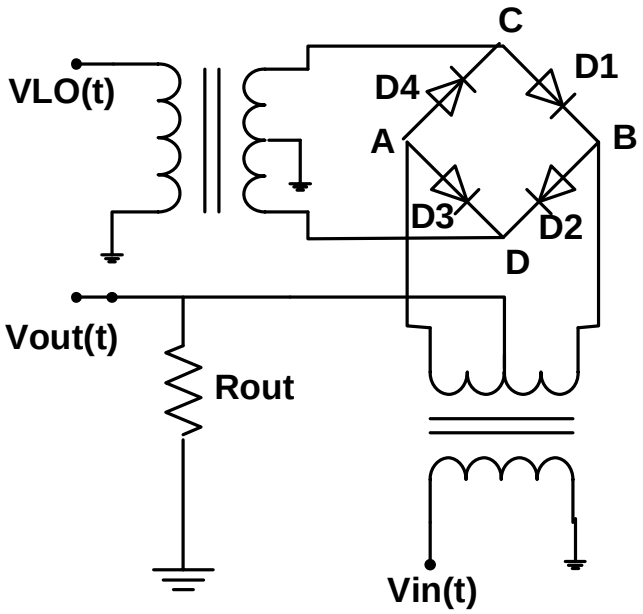


Figure 16

Passive diode ring mixer topology

Once again, supposing low frequency operation and strong LO signal the voltage at the mixer output is:

$$V_{out}(t) = A \cdot u(t) \cdot V_{in}(t)$$
$$, where$$
$$u(t) = 1 when V_{LO}(t) \geq 0 \qquad (2)$$
$$u(t) = -1 when V_{LO}(t) \leq 0$$

In diode ring mixer topology, the conversion gain is higher than that of the simple diode mixer, due to the fact that the mixer exploits the input signal all over the LO signal period.

Except for the diode mixers, there are also passive mixers that use MOS transistors. Shown in Figure 17 is a simple single-ended mixer topology, in which transistor M operates in its linear region. The input signal passes to the output according to whether M is on or off. In such a case the input signal is present at the output only during half of the period. The LC circuit is used to cut-off harmonics appearing at the output.

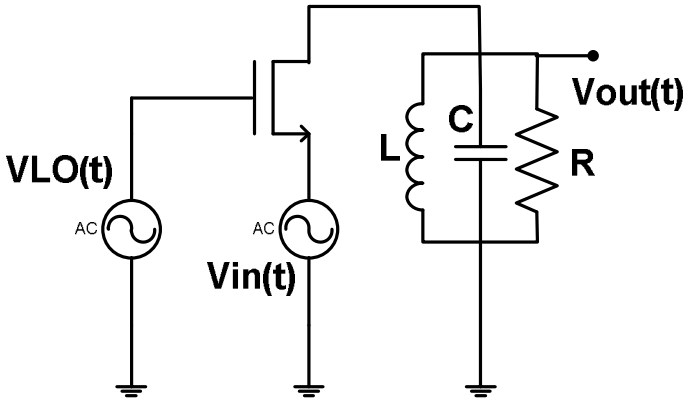


Figure 17

Single ended passive mixer

In the fully differential passive mixer topology (Figure 18), the input signal is always present at the output given that one of the transistor pairs M1, M2 and M3, M4 will be always on in presence of a strong LO signal.

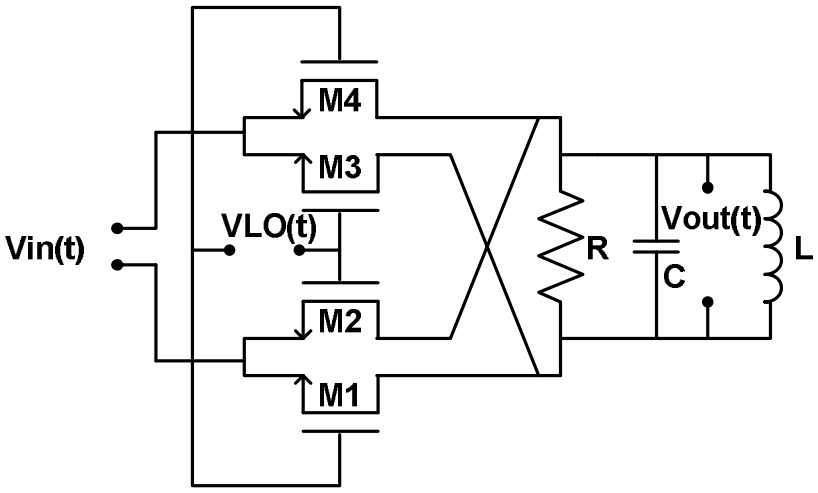


Figure 18

Fully differential passive mixer

The most important advantage of passive mixers, compared to active mixers, is their high performance as far as linearity is concerned. This mainly occurs to passive mixers using MOS transistors, rather than those using diodes. This is due to the fact that diodes experience nonlinearities High linearity in passive MOS mixers may also be justified because of their low gain levels.

3.2.2 Active Mixers

Active mixers, which exhibit DC current consumption, are usually preferred in communication applications. This is because of their high conversion gain, which allows better performance, and decreases noise contribution in mixer as well as at stages preceding it. Active mixers operate in the saturation region experiencing nonlinearities, a fact that renders them unsuitable for applications where linearity is the main concern. Nevertheless, modern communication systems demand high gain and noise specifications and are less austere in linearity performance, making active mixers the appropriate choice for use.

The simplest active mixer topology is shown in Figure 19. Transistors M1 and M2 operating in saturation, are controlled by the RF and the LO signals, respectively. Transistor M1 creates an AC current in drain. The role of M2 is to switch and control this current flow, to the output. The AC current in M1 gate is:

$$I_{M_1} = g_{m_1} V_{in} \tag{3}$$

where g_{m_1} is the transconductance of M1.

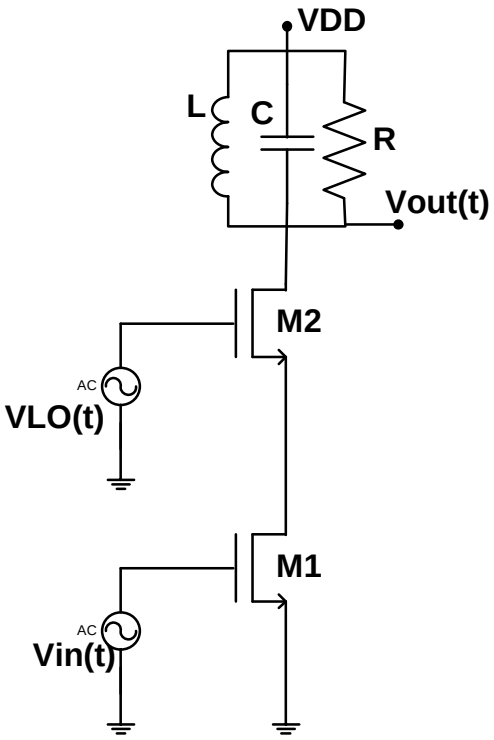


Figure 19

Simple active mixer topology

The conversion gain is given by:

$$CG = \frac{V_{out}}{V_{in}} = \frac{1}{p} g_{m_1} R_{out} \quad (4)$$

where R_{out} is the output resistance, while $\frac{1}{p}$ coefficient arises from the switching operation of M2, in presence of a powerful LO signal.

From the above equation it is obvious that active mixers may present high gain, depending on the consumption and the values of the passive elements used. The circuit presented in Figure 19, is a single-ended-input, single-ended-output topology, experiencing severe problems due to asymmetries. The first differential and symmetric topologies of active mixers were proposed by Gilbert and are presented below.

3.3 Gilbert Cell Mixer

Gilbert cell mixer [4] is a fully symmetric, differential output topology, widely used in mixer design. Differential output is preferred for higher gain and more immunity to RF to IF feedthrough. The single-ended differential output topology,

called single-balanced mixer is shown in Figure 20. Transistor M3 acts as a transconductor converting the input RF voltage into current. I_{RF} is diffused periodically at output, depending on which of the transistors M1 and M2 is on or off. When the LO signal is strong enough, only one of them may be on. In the LO+ phase, the AC output voltage is given by $I_{RF}R_1$, while it is $-I_{RF}R_2$ in the LO- phase. Therefore, the effect of the switching is to multiply I_{RF} with a square wave alternating between -1 and +1 at the frequency of the local oscillator. This can be described mathematically as [5]:

$V_{IF} = V_{RF}\cos(w_{RF}t) \times g_{m3} \times square(w_{LO}t)$, where g_{m3} is the transconductance of M3. Substituting for the Fourier series expansion of the square wave gives

$$V_{IF} = V_{RF} g_{m3} R \cos(w_{RF}t) \times \frac{4}{p}\left[\cos(w_{LO}t) + \frac{1}{3}\cos(3w_{LO}t) + ...\right]$$
$$= \frac{2V_{RF} g_{m3} R}{p}\cos(w_{IF}t) + ... \qquad (5)$$

, where $R = R1 = R2$.

The above equations demonstrate how the commutating action of M1 and M2 downconverts the RF signals.

Resistive loads can be replaced with LC tanks but this is impractical for downconversion (large LC needed). Conversion gain is given by:

$$CG = \frac{V_{out}}{V_{in}} = \frac{2}{p} g_{m3} R_{out} \qquad (6)$$

$$g_{m3} = \frac{1}{2} K \frac{4I_{D3}/K - 2V^2_{RF}}{\sqrt{4I_{D3}/K - V^2_{RF}}} \qquad (7)$$

The main drawback of the single-balanced Gilbert cell mixer is the high LO to IF feedthrough depicted in the following figure.

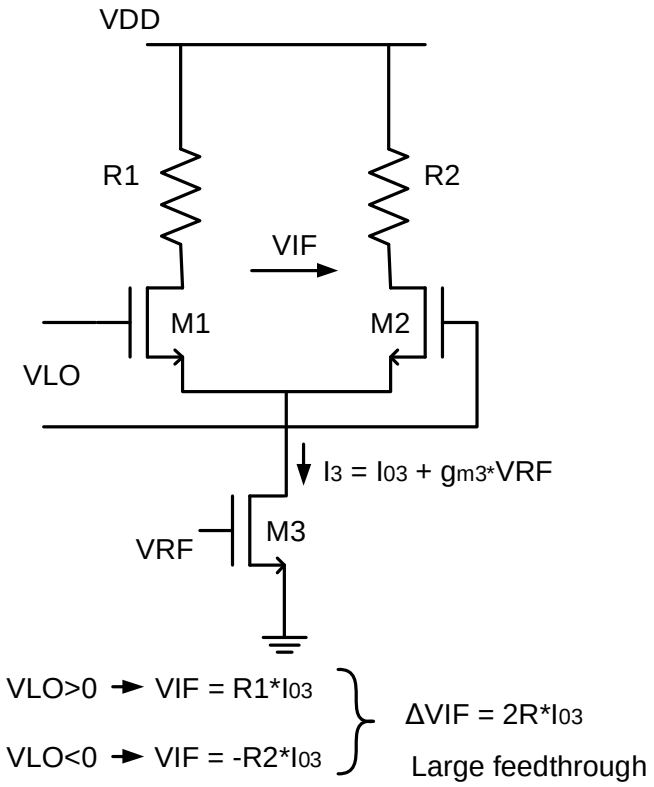


Figure 20

Single balanced Gilbert cell mixer

The double-balanced mixer topology, demonstrated in Figure 21, almost cancels the LO to IF feedthrough. The input stage, also called transconductance stage, consists of a differential pair M1 and M2, in which the RF differential signal is applied. This stage converts the RF input voltage to an output current. The current flows to the mixer output through the switching transistors M3, M4, M5, M6, which manage current in a way that it appears to the output with a phase difference of 180°. This demands a powerful LO signal so that switching is done simultaneously. The LO to IF feedthrough in the double-balanced architecture is almost zero.

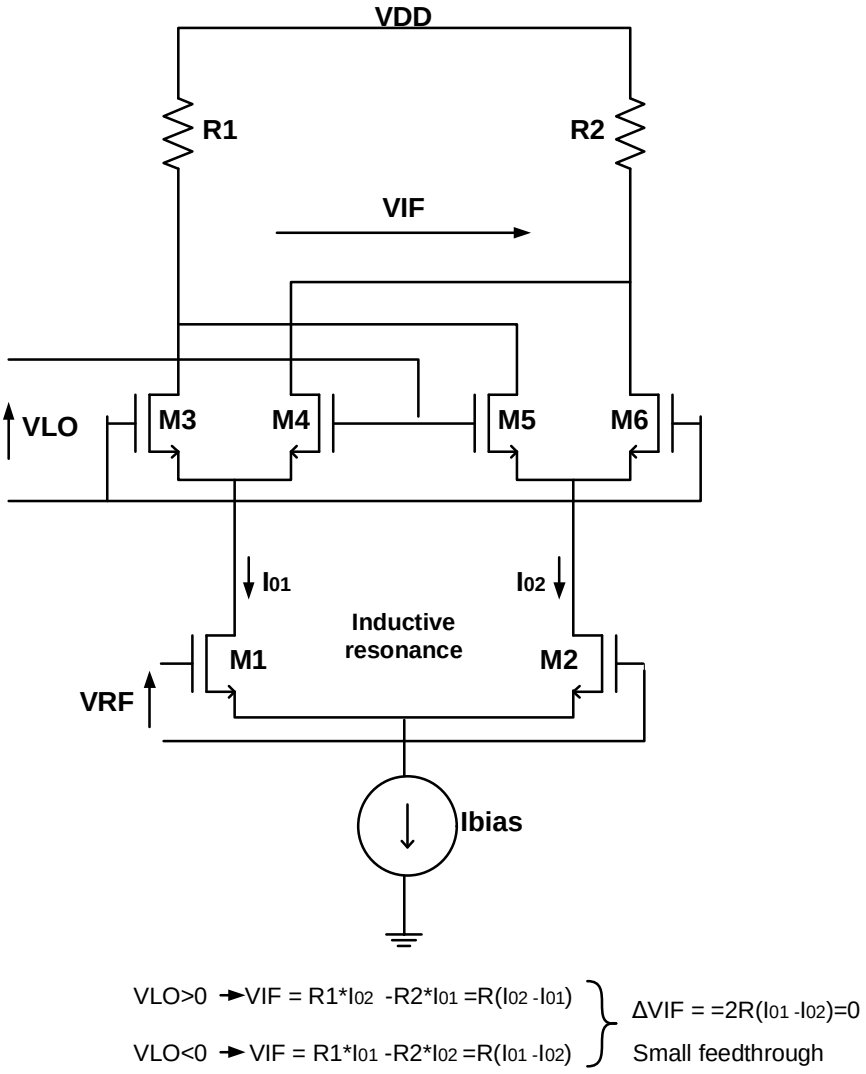


Figure 21

Double balanced Gilbert cell mixer

The conversion gain of the double-balanced mixer is the same as that of the single-balanced. It should be mentioned that except for the AC voltages of the input and LO signals, DC voltages are also applied for proper mixer biasing according to the specifications that should be met.

The following analysis suggests that the Gilbert type mixers have two main stages: the input or transconductance stage and the switching stage. The transconductance stage converts the RF signal into a current and provides the mixer's conversion gain together with the IF load. If the switching stage can be assumed to have more or less ideal switching, then the transconductance stage sets the limit of the mixer's linearity. Therefore, it is important to design an input stage that is as linear as

possible. The switching stage provides the frequency translation via its commutating action.

3.4 Figures of Merit

The Gilbert cell mixer is extensively used in modern communication systems because of the gain it provides together with its low noise contribution. In this paragraph, the main figures of merit, that characterize a mixer, are presented. Conversion gain, noise figure, port-to-port isolation and linearity issues are discussed. The trade-offs appearing among them, during the schematic design, are also cited.

3.4.1 Conversion Gain

The input and output of the mixer are in different frequencies, RF and IF respectively. Thus the term conversion gain instead of gain is used to describe the gain seen when the input signal appears at the output [4]. Conversion gain is defined as the ratio of power or voltage at the output to the power or voltage at the input. The conversion gain of the Gilbert cell mixer is described by equations (6) and (7) supposing strong LO signal and low frequencies for the RF and LO signals. Practically, these equations impress maximum conversion gain that designers may succeed. Sinusoidal kind and limited power of the LO signal actually diminish gain, as parasitic paths also do. In equation (7), $K = m_0 C_{OX} W_1 / L_1$ and it is assumed that M1 and M2 are well matched so that $W_1 = W_2$ and $L_1 = L_2$. Talking about the double-balanced Gilbert mixer, the transconductance of the RF input differential pair is maximum for small input voltages and is given by [5]:

$$g_{m\max} = \sqrt{m_0 C_{OX} W_2 / L_2 I_{SS}} \qquad (8)$$

Since the input stage of the mixer is basically formed by a differential pair, equation (8) brings to light trade-offs in the design of mixers that are common to all differential pair circuits. In order to increase the conversion gain of the mixer, one has to increase g_m. This may be achieved either by increasing the bias current, or by changing the dimensions of M1 and M2 (for the double-balance mixer). This of course trades-off with higher power consumption.

Another disadvantage of increasing bias current is that transistors M3 to M7 will take longer to switch on and off. Improper switching can be modelled by a

Fourier series expansion that has many more terms than that of the ideal square wave in equation (5). Furthermore, the coefficient of the component in the fundamental frequency will be lower than $4/\pi$, in equation (5). Thus, improper switching may lead to lower conversion gain and linearity.

The conversion gain of the mixer greatly affects the overall gain of the receiver. Beside that, the conversion gain also affects linearity as well as noise of communication systems. This illustrates that no figure of merit can be considered in isolation. So proper design should take into account the trade-offs arising from this.

3.4.2 Isolation

It is generally desirable to minimize interaction among the RF, IF and LO ports, especially at the high operating frequencies of the mixer. Since the LO signal power is quite large compared to the RF signal power, any LO leakage to the mixer input port and subsequently to the stages preceding it (LNA, filter), may deteriorate the overall receiver performance. Thus the LO to RF isolation plays a significant role in mixer design. The LO feedthrough to the RF port depends on capacitive coupling between the LO and the RF ports. Balanced non-overlapping switching will help greatly cancel out any LO feedthrough from the LO+ and LO- inputs. Capacitive coupling between the LO and the RF ports have to be kept to a minimum, and this is strongly a layout issue. To acquire high isolation, the LO and mixer cores in layout should be a distance away. On the other hand, the LO to IF isolation is a less significant matter since the LO and IF frequency are far apart in downconversion. Therefore, signal splitting is easy to be achieved by filtering.

3.4.3 Linearity

Linearity expresses how linear a system is, that is whether the output power in predetermined frequencies, is confined for a given input or not. Nonlinearities of a circuit may be separated into two categories: harmonic distortion and intermodulation distortion [4][5].

Harmonic distortion refers to cases in which the circuit input comprises of a sinusoid, and has to do with harmonics produced in multiple frequencies compared to the input frequency. Intermodulation appears when more than one sinusoidal signals of close frequencies are present at circuit's input. The mixer's output contains a signal

in the fundamental frequency and signals at multiple frequencies. Intermodulation, rather than harmonic distortion is the main problem that designers have to face.

Let's consider a downconversion mixer with two tones of close frequencies, let's say f_1 and f_2 and of same power, P. Even though at the mixer's input port only these two tones exist, at the mixer output port except for the expected products at frequencies $|f_{LO} - f_1|$ and $|f_{LO} - f_2|$, there also exist some other tones. These are very close to the desired products and their frequencies are $f_{LO} - (2f_1 - f_2)$ and $f_{LO} - (2f_2 - f_1)$. The third order products produced, fall within the useful frequency band, given that f_1 and f_2 are close enough. The two-tone third-order intercept point is also used to characterize mixer linearity. A two-tone intermodulation test is a commonly used, practical way to evaluate mixer performance because it mimics the real world scenario in which both a desired signal and a potential interferer feed a mixer input. Ideally, each of the two superposed RF inputs would be translated without interacting with each other. Of course, practical mixers will always exhibit some intermodulation effects.

As a measure of the degree of departure from linear mixing behaviour, one can plot the desired output and the 3rd order intermodulation output as a function of the input RF level. The 3rd order intercept point is the extrapolated intersection of these two curves. In general, the higher the intercept the more linear the mixer. Of course, one ought to specify whether the intercept point is input or output referred, to perform fair comparisons among mixers. Additionally, it is common to abbreviate the 3rd order intercept point as IP3, or perhaps IIP3 or OIP3 (for input and output third order intercept point, respectively). These definitions are summarized in Figure 22.

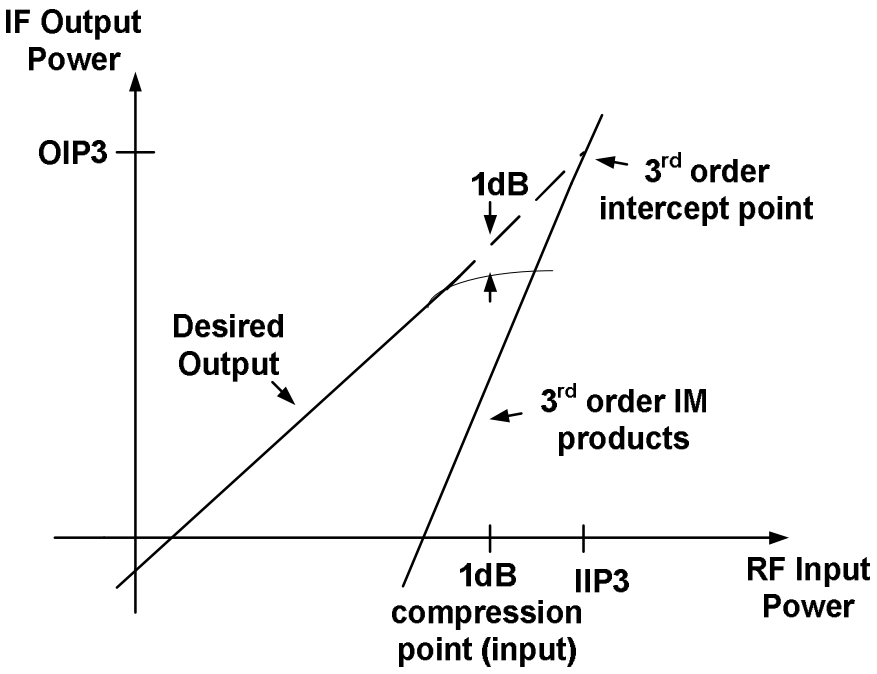


Figure 22

Definition of mixer linearity parameters

In general, the relationship between the transistor's current, I and the gain-source voltage, V_{GS} is given by:

$$I = K\frac{(V_{GS}-V_{th})^2}{1+q(V_{GS}-V_{th})} \tag{9}$$

where K is a constant depending on the technology and the transistor dimensions, proportional to the transistor width. The parameter θ models the source series resistance, the mobility degradation because of the vertical field and the short-channel effects such as velocity saturation.

Referring to Figure 23, the large signal behaviour of the switching pair is described by [6]:

$$I_0 = I_1 - I_2 = K\frac{(V_{GS1}-V_{th})^2}{1+q(V_{GS1}-V_{th})} - K\frac{(V_{GS2}-V_{th})^2}{1+q(V_{GS2}-V_{th})} \tag{10}$$

$$V_{in} = V_{GS1} - V_{GS2} \tag{11}$$

$$I_B = I_1 + I_2 = k\frac{(V_{GS1}-V_{th})^2}{1+q(V_{GS1}-V_{th})} + k\frac{(V_{GS2}-V_{th})^2}{1+q(V_{GS2}-V_{th})} \tag{12}$$

Combining the above equations, the equation describing the differential pair is given by:

$$V_{in} = F(I_0) = \frac{q^2}{K} I_o + \sqrt{(\frac{q^2}{2K}(I_B + I_0))^2 + \frac{2q^2}{K}(I_B + I_0)} - \sqrt{(\frac{q^2}{2K}(I_B - I_0))^2 + \frac{2q^2}{K}(I_B - I_0)} \tag{13}$$

Using Taylor series we can calculate the output current I_0 as a function of the input voltage V_{in} as follows:

$$I_0 = f^{-1}(V_{in}) = c_1 V_{in} + c_3 V^3{}_{in} + c_5 V^5{}_{in} + \ldots \tag{14}$$

From (12) and (13) we end up to the following equations:

$$c_1 = (\frac{q^2 I_B}{8} + \frac{K}{2})\sqrt{\frac{I_B}{K}(\frac{q^2 I_B}{K} + 8)} - (1 + \frac{q^2 I_B}{8K}) q I_B \cong \sqrt{2KI_B}\,\big|_{q \to 0} \tag{15}$$

$$c_3 = q\,\frac{4q^3 c_1^3 - 20q^2 K c_1^2 + 32q K^2 c_1 - 16K^3}{32q^2 K I_B + 4q^2 I^2{}_B + 32q K c_1} \cong \frac{K^{3/2}}{2\sqrt{2I_B}}\Big|_{q \to 0} \tag{16}$$

The input 3rd order intercept point, IIP_3, is given by [6]:

$$IIP_3 = dB_{20}\sqrt{\frac{4c_1}{3c_3}} \cong dB_{20}\sqrt{\frac{16I_B}{3K^3}} \tag{17}$$

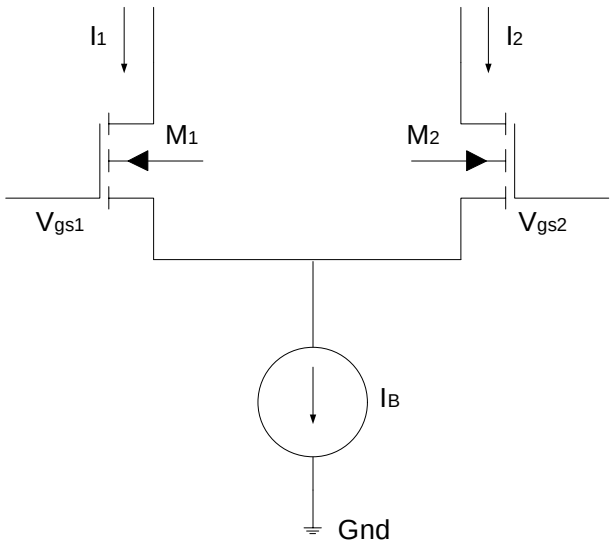


Figure 23

Differential pair

In CAD tools, the method used to calculate the nonlinearities in integrated mixers, is the harmonic balanced (HB) method. HB uses the time and frequency domain, exploiting the circuit's pseudo-linear nature and giving accurate results. When lots of harmonics are used then the whole process becomes time-consuming.

Another parameter denoting linearity is the 1 dB compression point (Figure 22). It is the value of the RF signal at which a calibrated departure from the ideal linear curve occurs. One may specify either the input or output signal strength at which this compression occurs. As a rule of thumb, the 1 dB compression point is an estimate of the largest signal that can be processed by the receiver, and hence sets the upper bound on the dynamic range of the mixer.

The linearity of the whole mixer is limited by the linearity of the input transconductance stage since the switching stage does not introduce significant nonlinearities. Therefore, attempts to improve the linearity of the mixer generally focus on improving the linearity of the input transconductance stage. This can be achieved by source degeneration. The passive components (either resistors or inductors) at the source nodes of the input transistors, greatly affect linearity (Figure 24).

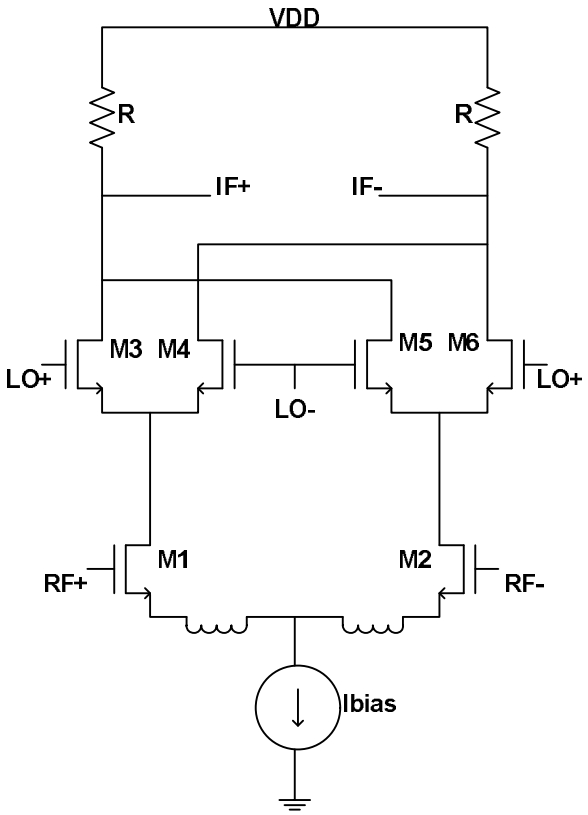


Figure 24

Source degeneration

3.4.4 Noise Figure

Noise figure is the signal-to-noise ratio (SNR) at the input (RF) port divided by the SNR at the output (IF) port.

$$NF = \frac{(SNR)_{IN}}{(SNR)_{OUT}} \tag{18}$$

The total input referred noise of the RF receiver determines the smallest signal that can be processed by the receiver, setting a lower band on the dynamic range of the receiver. Since the RF receivers have to process weak signals, it is crucial to minimize the noise figure of the front-end building blocks. It should be noticed that in a typical mixer, there are actually two input frequencies that will generate a given intermediate frequency. One is the desired RF signal and the other is the image signal, as we have already described. In mixers, these two signals are usually referred as sidebands.

The IF signal is simply the absolute difference between the RF and the LO signal. Hence, signals, which are above and beyond the LO frequency by an offset equal to IF, will produce IF outputs at the same frequency. The two input frequencies are therefore separated by $2w_{IF}$, where w_{IF} is the IF frequency. As a numerical example, the receiver's RF signal is at 5300 MHz and we wish to tune to a signal at 10 MHz by selecting a LO signal of 5290 MHz. Apart from the desired RF input at 5300 MHz, an image signal at 5280 MHz will also produce a component at the IF frequency of 10 MHz.

Two types of noise figure have been defined for mixers: single-sideband (SSB) and double-sideband (DSB). In the single-sideband noise figure, the desired signal spectrum resides in only one side of the LO frequency (heterodyne systems), whereas in the double-balanced noise figure, the input signal resides on both sides of the LO frequency (homodyne architectures). As shown in Figure 25, the SSB NF of a mixer is 3 dB higher than the DSB if the signal and the image bands experience equal gain at the RF port. This happens because the SSB as well as the DSB NF have the same IF noise but in the SSB case the signal power resides in only one sideband. SSB noise figure is applicable in heterodyne receivers, where the LO signal is apart a certain offset frequency from the RF signal. On the other hand, in the direct-conversion receivers the LO and RF signals' frequencies are close, since the RF

channel has to be downconverted to baseband. Thus, DSB noise figure is applicable in homodyne architectures.

In most communication systems, NF refers to the SSB NF, rather than the DSB NF. Representative values for the noise figure vary from 5-15 dB, depending on the application and the technology used.

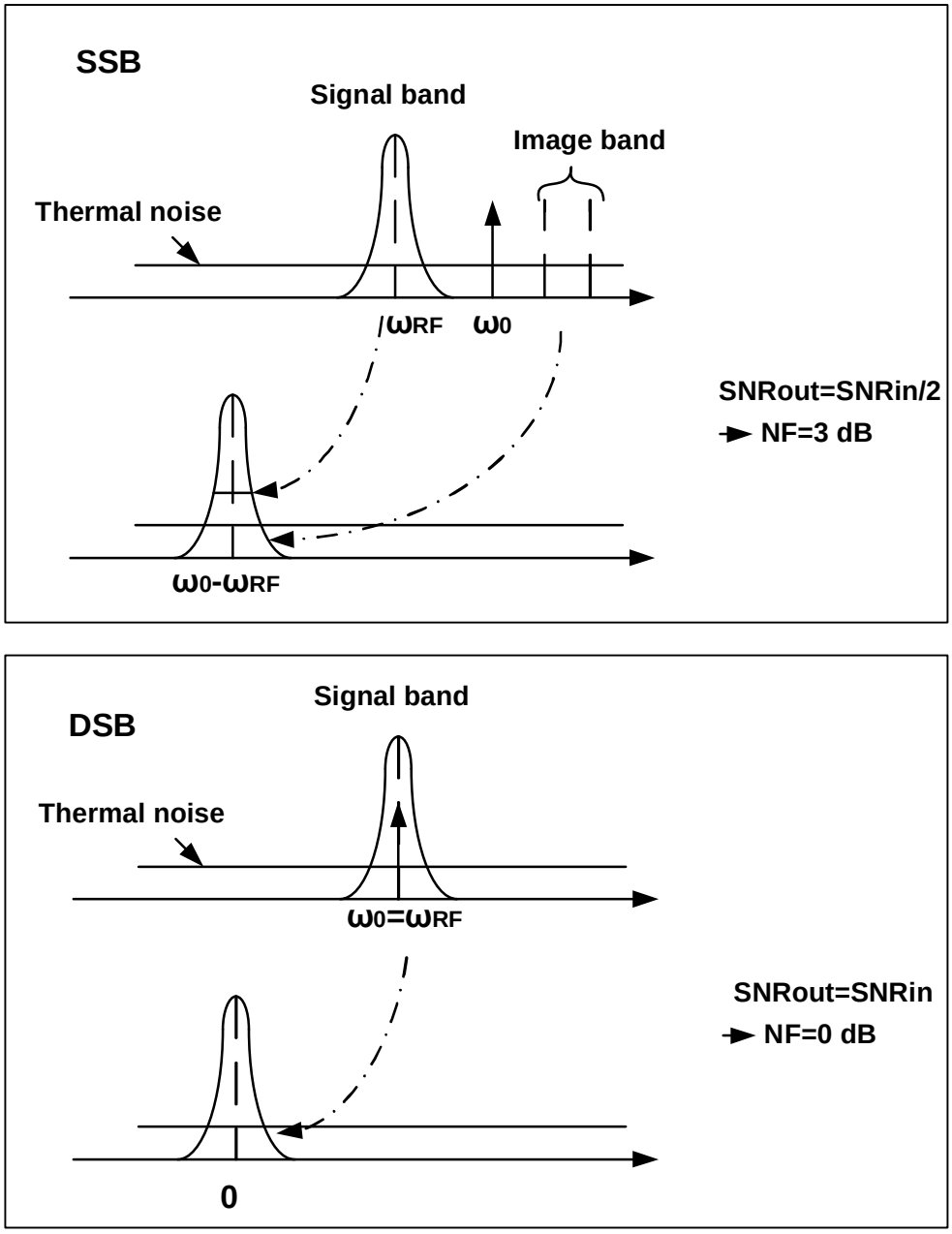


Figure 25

SSB vs. DSB Noise Figure

Noise in mixers is often determined by the transconductance stage. However, the switching action of the differential pair provides frequency translation not only for the desired signal but also for the noise – a phenomenon called noise folding. Next the sources of noise in the Gilbert type mixer are presented.

3.4.4.1 Noise due to the load

The noise contribution of the mixer load depends on the load used. If the load is a resistor, R, then the white noise spectral density at the output is given by [5]:

$$U^2_n = 4KTR \tag{19}$$

To find the input referred noise due to the resistor, we have to divide (19) by the conversion gain of the mixer, given by $2g_mR/p$, where g_m is the transconductance of the RF input differential pair. It is extremely important to consider flicker noise at the output of the mixer, especially when upconversion occurs. Flicker noise in such a case could seriously damage the desired signal. If the load resistors are made of polysilicon, then they should be free of flicker noise. However, if active loads are used, then flicker noise could become a serious problem. Generally, if active loads are used, then PMOS instead of NMOS transistors should be preferred.

3.4.4.2 Noise due to the input transconductor

Noise in the input stage is indistinguishable from the desired signal. Therefore it will be translated in frequency by the LO signal in exactly the same way as the useful RF signal. When considering the thermal noise contribution of the transconductance stage, in the interests of simplicity let's consider the single-balanced Gilbert cell mixer of Figure 22. The input referred drain current thermal noise of the input stage is [5]:

$$U_n^2 = \frac{4KTg}{g_{m3}} \tag{20}$$

The output thermal noise contribution of M3 is simply found by multiplying equation (20) with the conversion gain. The effects of the multiple LO harmonics must be taken into account. The output thermal noise contribution is:

$$U^2_n = \frac{4KTg}{g_{m3}}\left(\frac{2}{p}g_{m1}R\right)^2\left(1+\frac{1}{3^2}+\frac{1}{5^2}+...\right) \tag{21}$$

Due to the switching action of the mixer, the desired and the image signals are multiplied by a square wave, at the RF input. The Fourier expansion of the LO signal contains odd harmonic at $3w_{LO}$,$5w_{LO}$ etc. These products will be downconverted to the desired IF.

Omitting the noise contribution of the higher order LO harmonics, may lead in mistakes when evaluating the noise of the input stage. The exact number of the harmonics that should be evaluated in equation (21) is determined by the bandwidth of the RF stage of the mixer. The higher the bandwidth, the higher the frequency at which the thermal noise occurs. Since the amplitude of the LO harmonics decreases with increasing frequency, their noise contribution diminishes as well.

The RF input stage does not produce flicker noise at the output in the frequency band of signal. In fact, flicker noise from the RF input stage is up-converted to the LO frequency and does not appear at baseband.

3.4.4.3 Noise due to the switching stage

Once again, let's consider the single-balanced Gilbert cell mixer. A critical problem of the switches is their flicker noise. Flicker noise is at a much lower frequency than the LO that drives their gates. It can be modelled as a slowly varying offset voltage at the gate of either M1 or M2 that either advances or delays the instance at which the transistor switches. The output current noise contribution from the flicker noise is [5]:

$$i_n = \frac{4i_{d3}}{S_{LO}T_{LO}}u_{nLO} \tag{22}$$

, where S_{LO} is the slope of the LO waveform at a zero crossing, T_{LO} is the period of the LO and U_{nLO} is the flicker noise of the switches M1 and M2. To find the overall input referred noise due to equation (22) at the gate of M3, we have to divide equation (22) by the conversion transconductance.

$$U_{ni} = \frac{2I_{D1}}{g_{m3}S_{LO}T_{LO}}U_{nLO} \tag{23}$$

For a classical square law MOSFET:

$$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_T} \tag{24}$$

While for a short channel device this becomes:

$$\frac{g_m}{I_D} = \frac{1}{V_{GS} - V_T} \tag{25}$$

Thus, for a short channel MOSFET, equation (23) becomes:

$$U_{ni} = \frac{2(V_{GS} - V_T)}{S_{LO} T_{LO}} U_{nLO} \tag{26}$$

Equation (26) suggests several ways to reduce the flicker noise contribution of the switches. Increasing the LO amplitude promotes faster switching (larger S_{LO}) and hence reduces the effect of flicker noise of M1 and M2. However, a larger LO drive runs the risk of generating spikes at the drain of M3, which can change the bias conditions of M3, or couple through the RF input. Another way to decrease the noise contribution of the switches is by reducing the LO frequency (larger T_{LO}). However, this will increase the IF frequency and the receiver should be able to cope with such a change. Alternatively, the gate overdrive voltage could be reduced, but this trade offs with linearity of the mixer.

According to a more recent approach, two major mechanisms generate the flicker noise of the switching pair devices [7][12]. The first one is the direct mechanism, due to the finite slope of the switching pair transistors. The LO switches generate noise pulse trains by the direct mechanism and the DC average of noise pulse trains is the output flicker-noise current, given by [7][12]:

$$i_{o,n(dir)} = \frac{(4I \times V_n)}{(S \times T)} \tag{27}$$

$$V_n = \sqrt{2 \times \frac{K_f}{W_{eff} L_{eff} C_{ox} f}} \tag{28}$$

Where I is the bias current for the RF transconductance stage, T is the LO period, Vn is the equivalent flicker noise of the switching pair, and S is the slope of the LO signal. Weff and Leff are also the effective width and length, Cox is the oxide capacitance, f is frequency, and Kf is a process parameter.

From (27), it is worth noticing that the low frequency noise at the gate of switch, Vn, appears at the output directly, and the output flicker noise current is decreased if the product of the slope of the LO signal and its period increase. From (28), Vn is inversely proportional to the device area. In order to decrease flicker noise in the direct mechanism, a popular method is to reduce the width of the noise pulses, which can be implemented by reducing the value of Vn. To reduce the value of Vn,

the size of the switching pairs need to be increased. Though, large switching devices increase the parasitic capacitance of the switching pairs, resulting in the indirect translation of the flicker noise to the output. In the indirect mechanism, flicker noise mainly depends on the tail capacitance of the node between the LO switches and the RF transconductance stage. When a sine wave LO is applied to the mixer, the average of the output noise current, stemming from the indirect mechanism is [12]:

$$i_{o,n} = \frac{2C_p}{T} V_n \times \frac{\left(C_p w_{LO}\right)^2}{g^2{}_{ms} + \left(C_p w_{LO}\right)^2} \tag{29}$$

Where Cp is the tail capacitance of the node between the LO switches and the RF transconductance stage, T is the LO period, g_{ms} is the transconductance of the LO switches and Vn is the equivalent flicker noise of the switching pair. According to (29), the tail capacitance should be small enough to decrease the effect of the indirect mechanism.

3.5 Improvement Techniques

Several techniques have been proposed in order to improve the overall mixer performance, including all figures of merit, i.e. the conversion gain, the noise figure and the linearity. It is up to the application, which of them shall be used, while designing the mixer block. In this paragraph, three of these techniques are going to be presented and analyzed. The current bleeding technique and the inductive resonance technique as well as their combination.

3.5.1 Current Bleeding Technique

The current bleeding technique is widely used in integrated mixer optimization because it can improve gain, noise and linearity, simultaneously. The main characteristic of the technique is that different currents appear at the input and the switching stage. In this way, each of the stages may be optimized separately, as far as current consumption is concerned, which, in turn, results in an overall performance improvement in comparison with conventional mixers [4][12].

The input stage transistors may consume strong currents, so that gain and linearity increase, while the switching stage transistors demand less current in order to accomplish an instantaneous switching action. Instantaneous switching action leads to

a minimum time decrement, in which all of the switching stage transistors are on. Ideally, at each time only one of them should be on. If we succeed this, noise contribution of the switching stage at mixer output decreases, while at the same time linearity of mixer and hence of the receiver chain significantly improves.

The current bleeding technique is presented in Figure 26. A current source is used at the source nodes of the switching stage transistors, which "absorbs" part of the input stage current. Thus, the current flowing at the switching stage is the difference between the input stage current and the bleeding current I_{BL}.

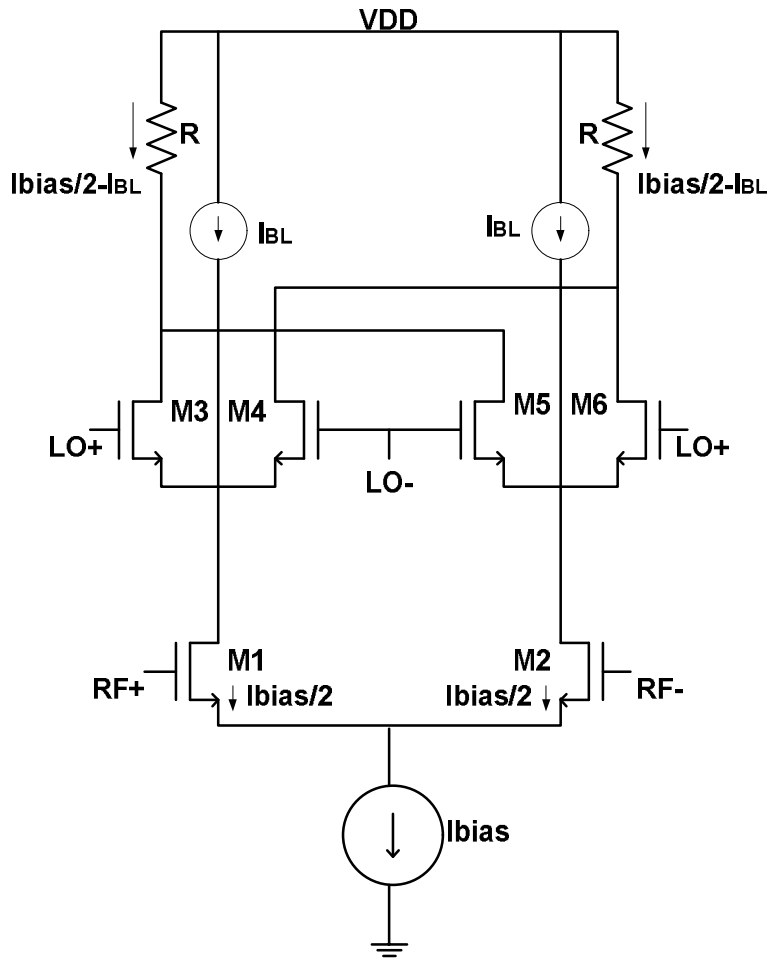


Figure 26

Current bleeding technique

An additional advantage of this technique is that reducing the DC bias current of the switching stage, the voltage fall at the output resistors becomes smaller so that the voltage margin at the output gets higher. It is clear that the output resistors may be increased, without "strangling" the operation of the switching stage, resulting in mixer's conversion gain increment.

3.5.2 Inductive Resonance Technique

One of the most limiting factors in integrated mixer design is the parasitic capacitances (C_P) appearing at the source nodes of the switching transistors, as depicted in Figure 27. The capacitance C_P destroys mixer performance, affecting all noise, gain and linearity. So, usage of a capacitive neutralization technique is necessary [4][12].

The problem can be solved if we place an inductor, L, between the source nodes of the switching stage transistors. The inductor's value is chosen so that it resonates with the parasitic capacitance at these nodes in the desired frequency of the RF input signal. In practice, the inductor and its quality factor are selected in a way that the resonance characteristic, which results, is broadband and covers a wide band around the RF frequency.

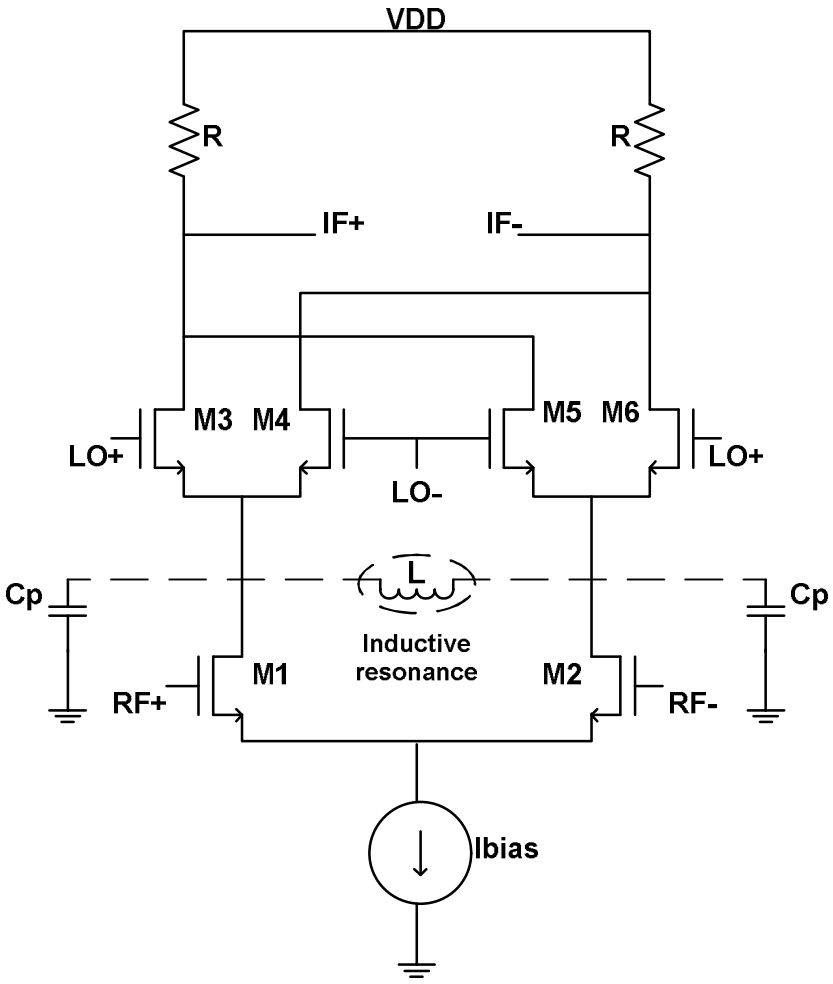


Figure 27

Inductive resonance technique

The existence of this resonant circuit at the sources of the switching transistors means that the AC current that comes from the input stage is not grounded through the parasitic pathways, but is "obliged" to flow via the switching stage. The result is that the mixer approaches its low frequency operation, which in turn translates to significant conversion gain increase. If we wanted to succeed a similar gain without using this technique, extremely large bias current should be consumed by the switching stage. This approach keeps gain high enough, but increases the consumed power and destroys mixer performance referring to linearity and noise. In practice, usage of the integrated inductor, L, provides the designers the ability to perform mixer designs with exceptional performance and very small bias current. Obviously, this is an important assignment since the high frequency mixer topologies suffer from high power consumptions.

The inductor resonance technique also improves Gilbert cell mixer's linearity. It has been proved that, when mixer linearity is confined by the switching stage non-linearity, interaction between the non-linearities of the input stage and the switching stage, results in linearity improvement, compared to the linearity of the switching stage alone. Based on this observation, we can realize that usage of the integrated inductor "discourages" the intermodulation products of the input stage to flow through the parasitic pathways. On the contrary, these products flow through the switching stage interacting with the intermodulation products, produced by this stage, resulting in performance improvement, as far as linearity is concerned.

Except for gain and linearity, which are tremendously improved via the inductor resonance technique, noise improvement is also obtained.

3.5.3 Current Bleeding technique with Inductive Resonance

Even if the current bleeding technique can reduce the bias current of the LO switches, flicker noise is still generated by the indirect mechanism. The tail capacitance Cp is still needed to be reduced. The best way to reduce the tail capacitance is to minimize the size of the LO switches and RF transconductance stages. However, CMOS transistors suffer from high intrinsic flicker noise, which is inversely proportional to the device area. Therefore, one inductor (Lp) is connected between the common source node of the LO switches, as shown in Figure 28, to

resonate the tail capacitance out. In practice, this is a combination of the current bleeding technique and the inductive resonance technique [12].

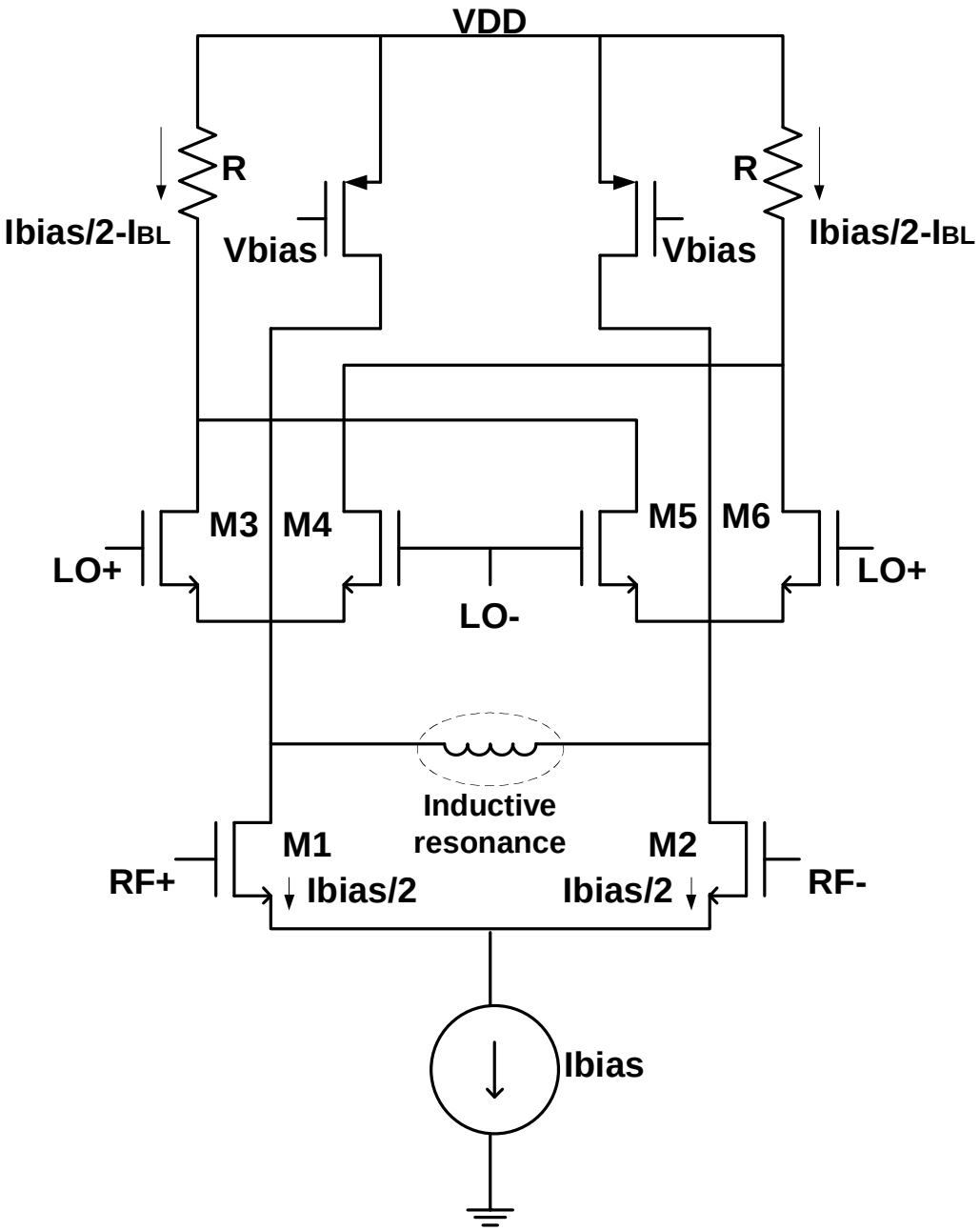


Figure 28

Current bleeding technique with on inductor

CHAPTER 4: MIXER SIMULATION - RESULTS

4.1 Design Flow

In this chapter, we present the steps that should be followed during the mixer design. Firstly, the design kit that was used is presented and transistors' characteristics are shown. What comes next is the mixer bias network, which comprises of a current mirror. Conversion gain, linearity, isolation and noise measurements are presented. The optimized simulation results are shown and a Monte Carlo statistical analysis is performed in order to evaluate the impact of the transistors' variations in mixer's performance. Eventually, the effect of temperature variation in mixer performance is also studied.

4.2 Design Kit

The technology that is used in Gilbert cell mixer design is the IHP BiCMOS SGB25 at 0.25 um, based on the BSIM3 model. For NMOS transistors, the short channel voltage threshold is about 0.58 V, while for PMOS transistors it is -0.5 V. The supply voltage is 2.5 V. Other useful parameters that have been extracted are given in Table 5.

V_{T_0}	0,58
g	0,56
f	0.85
I_{spec}	4.27e-7
k_p	2.47e-4
C_{ox}	5.95e-3
m_0	4.15e-2

Table 5

IHP 0.25 um

It should be mentioned that the supported design kit for ADS does not include inductors. Thus, inductors provided by ADS cad tool have been used. Their quality factor and their series resistance have been extracted from the corresponding Cadence design kit. What follows is a NMOS transistor's DC analysis, in order to extract

transistor's parameters, such as V_{T_0}, $V_{DSAT,}$ g_m and to compare the design kit model with the simulated results.

Depicted in Figure 29 is a DC analysis of a NMOS transistor. The source node is grounded, while the gate and drain are biased with voltages VGS and VDS, respectively. The current that flows through the transistor can be estimated by a prober. If we want to model the body effect, a source-to-substrate potential should be applied. This will increase the threshold voltage V_T and reduce the current for a given V_{GS}.

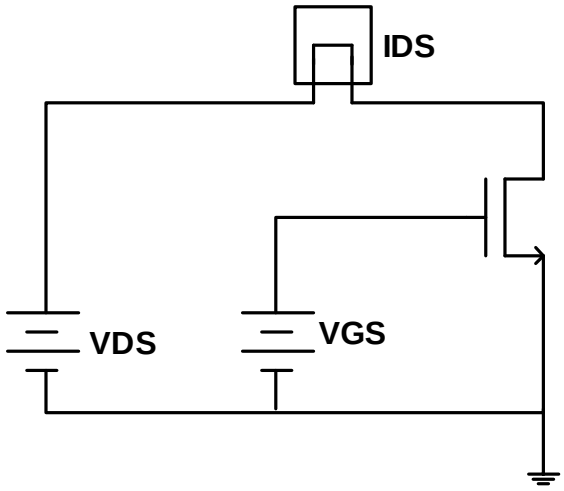
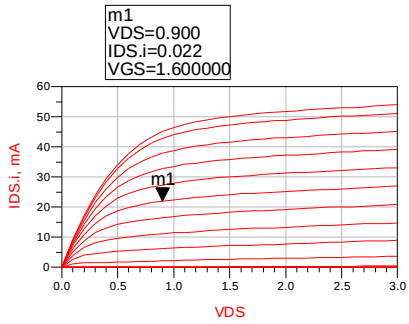
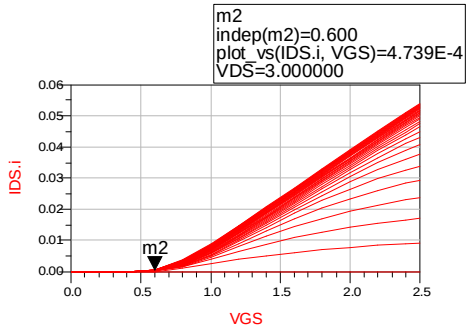


Figure 29
NMOS DC Simulation

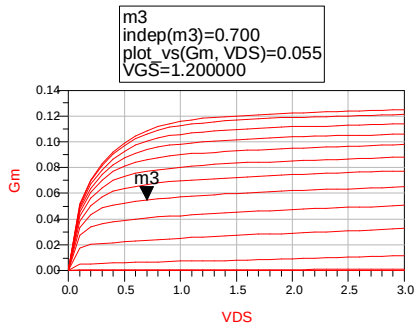
The output current I_{DS}, in respect to the drain-to-source voltage V_{DS}, is given in Figure 30a. Figure 30b shows the relationship between I_{DS} and V_{GS}, confirming that the threshold voltage V_T is about 0.6 V. The transconductance g_m versus V_{DS} is depicted in Figure 30c.



(a)



(b)



(c)

Figure 30

(a) IDS vs. VDS, (b) IDS vs. VGS, (c) Gm vs. VDS

4.3 Device Width and Biasing

We need a width W, which will provide high transconductance, saturation at low VDS and low noise. Large widths are preferred for noise. The optimum width for noise can be estimated as:

$$W_{opt} = \frac{1}{3wLC_{ox}R_{gen}} \tag{30}$$

Substituting $w = 2p\,f$, $f = 5.3GHz$, $L = 0.24um$, $C_{ox} = 5.95e^{-3}A$, $R_{gen} = 50Ohm$, we get: $W_{opt} = 140um$. Large widths also require larger bias to obtain high g_m, increasing power consumption. We should also investigate the minimum current required to keep the transistors in saturation ($V_{DS} > V_{DSAT}$), something beneficial for most active circuit implementation.

To evaluate the device I-V characteristic, we use the differential amplifier, shown below. It is the simple single-balanced Gilbert mixer, as we have previously seen.

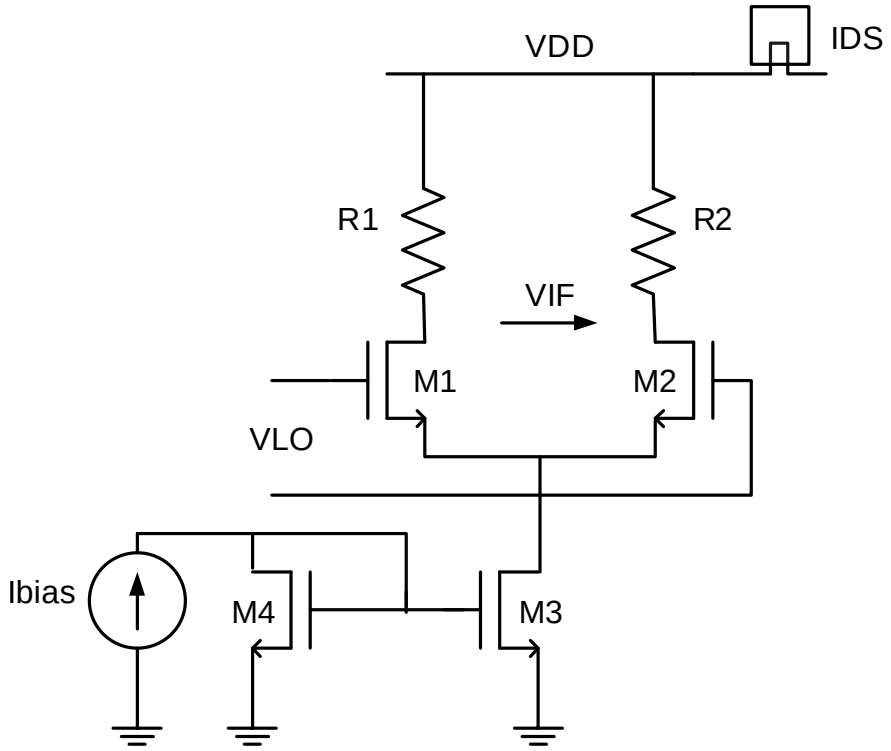
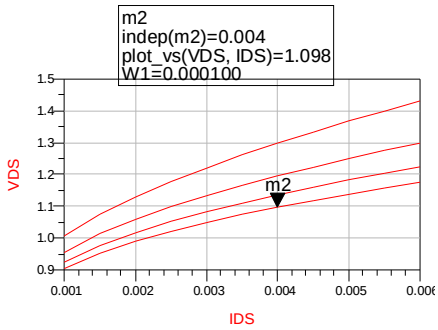


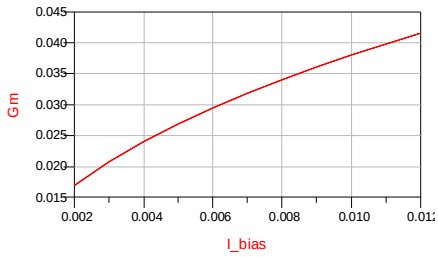
Figure 31

Diff amp

From the DC simulation that was performed, it is clear (from Figure 32a) that I_{DS} should be at least 2 mA, so that the device operates in saturation. Thus, using Kirchhoff's current law and considering that the transistors are fully symmetric, the minimum bias current, I_{bias} that will be used in the following simulations should be 4 mA. Demonstrated in figure 32b, transconductance increases with I_{bias}.



(a)



(b)

Figure 32

(a) VDS vs. IDS, (b) Gm vs. Ibias

In the single-balanced mixer, shown in Figure 20, the bias circuit is represented by an ideal current source that provides a constant current value. In the following simulations, this ideal current source has been substituted by a current mirror circuit. The current mirror is an element with at least three terminals, as shown in figure 33.

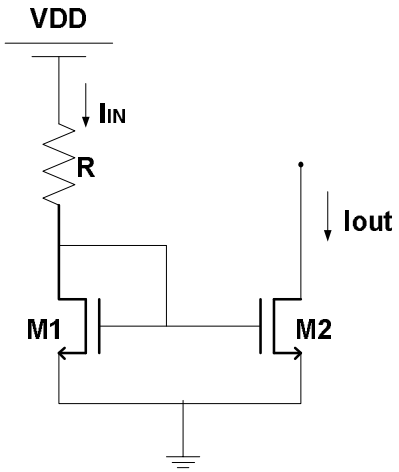


Figure 33

Simple current mirror

The common terminal is connected to a power supply, and the input current is connected to the input terminal. Ideally, the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the term current mirror. Under ideal conditions, the current mirror is independent of the input frequency and the output current is independent of the voltage between the output and common terminals. In practice, real transistor-level current mirrors suffer many deviations from this ideal behavior.

- The gain of a real current mirror is never independent of the input frequency.
- The output resistance, R, directly affects the current mirror's performance. Increasing the output resistance reduces the dependency of the output current on the output voltage, which is desirable.
- The gain error, ε, appears either there is perfect matching (systematic error), or there is mismatch (random error).
- The voltage drop, V_{IN} at the input terminal, reduces the available voltage across the input current source. Minimizing V_{IN} is important.
- A positive output voltage, V_{OUT} is required to make the output current mainly depend on the input current. This is summarized by the $V_{OUT(\min)}$, that allows the output device(s) to operate in the active region. Minimizing $V_{OUT(\min)}$ maximizes the range of the output voltages, for which the output resistance is almost constant.

The current mirror that has been used in mixer design is shown in figure 34. Transistors M1 and M2 form a simple current mirror, and the relationship between their current is given by:

$$I_d = \frac{(\frac{W}{L})_2}{(\frac{W}{L})_1} I_{ref} \tag{31}$$

where I_d is the output current and I_{ref} is the input current. I_{ref} depends on resistor's value, R. Assuming that $L_1 = L_2$, we get: $I_d = \frac{W_2}{W_1} I_{ref}$. Thus, it is the transistors' width that determines the output current given that their length is equivalent.

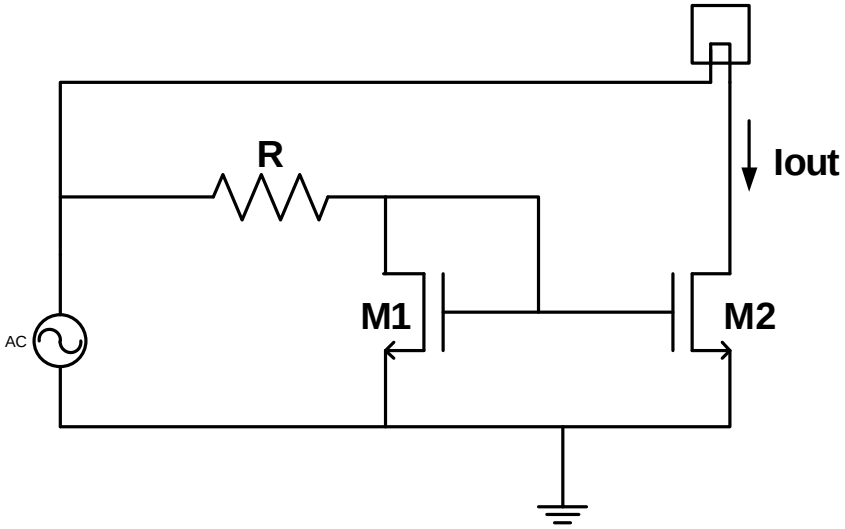


Figure 34

Current mirror

To evaluate the desired current an AC analysis is performed for frequencies varying from 1 GHz to 6 GHz. From the graph below, and assuming that $W_3 = W_2$ =200 um, we obtain that for an output current of about 10 mA and for a frequency close to 5.5 GHz, the resistor's value should be 140 Ohm. If we change the ratio of W_2 to W_3 let's say to 2, keeping the output current at 10 mA, resistor's value would become 280 Ohm.

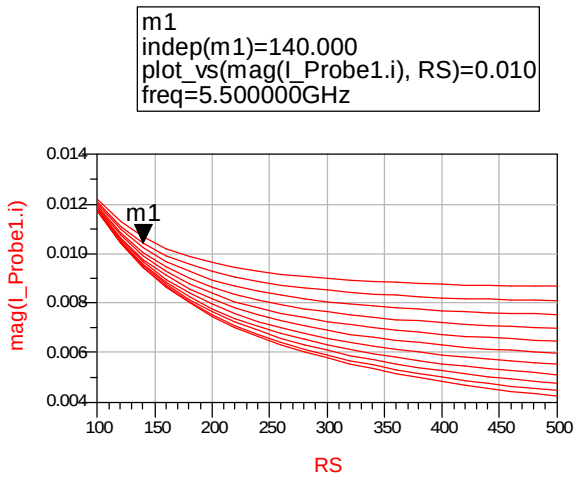


Figure 35

AC simulation results

4.4 Conversion Gain Results

Conversion gain is a key parameter in downconversion mixers, since the signal received by the antenna needs amplification. The mixer circuit that is used in this simulation and in those following is the double-balanced Gilbert cell mixer, depicted in Figure 21. The simulations that have been performed are harmonic balance (HB) simulations, so that the effect of intermodulation is taken into account.

The whole circuit comprises of three basic stages: the current mirror stage, the input or transconductance stage and the differential stage. An RF input signal at 5.3 GHz is applied at the input stage, whereas two signals of equal frequencies (5.29 GHz) and same amplitude with a phase shift of 180° are applied at the differential stage. The differential output signal is converted to a single-ended signal via a differential to single-ended converter. This fact makes extraction of simulation results quite easier. A thorough study of how the variation of several parameters affects the mixer's conversion gain follows.

- Preserving the LO amplitude voltage, VLO, constant at 0.5 V, we first vary the RF signal's amplitude Vref_RF.

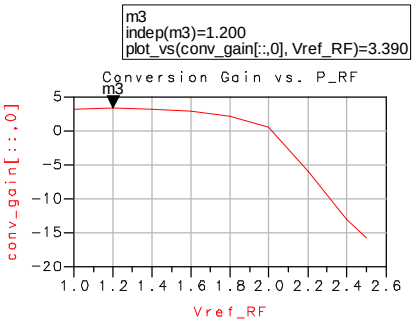


Figure 36

Conversion gain vs. Vref_RF

- Next, for Vref_RF=1.2 V, we vary the AC swing voltage Vref_LO.

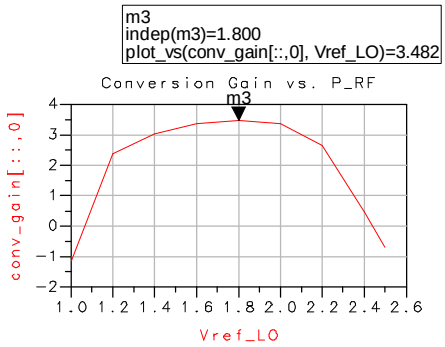


Figure 37

Conversion gain vs. Vref_LO

- To ensure that VLO optimum is 0.5 V, we plot the conversion gain versus VLO, keeping Vref_LO at 1.8 V.

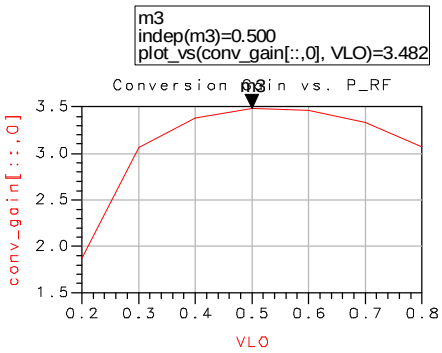


Figure 38

Conversion gain vs. VLO

- The width of the transistors of the input and the differential stage is equal and varied in order to obtain maximum conversion gain. During simulation, the width of the current mirror stage transistors is kept constant at 200 um. From Figure 39, it is obvious that W1 and W2 optimum is 250 um.

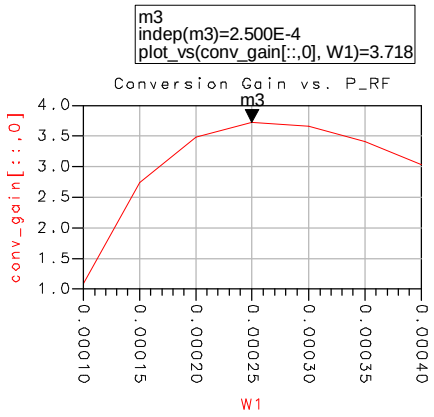


Figure 39

Conversion gain vs. Transistor width

- The relationship between the bias current and the conversion gain is depicted in figure 40. We first find the optimum resistance and then from the current mirror circuit we evaluate the corresponding bias current. The optimum resistor value is 150 Ohm and the respective current value is 10 mA.

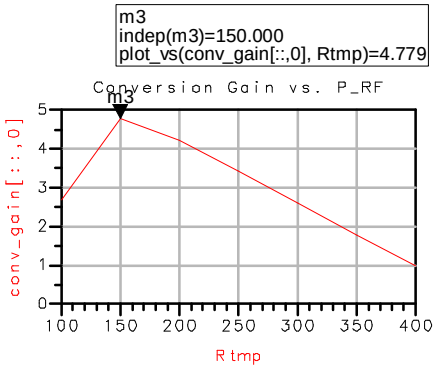


Figure 40

Conversion gain vs. Bias current

- Finally, sweeping the output resistance, we get Figure 41. It is obvious that the maximum conversion gain is obtained for Rout=200 Ohm.

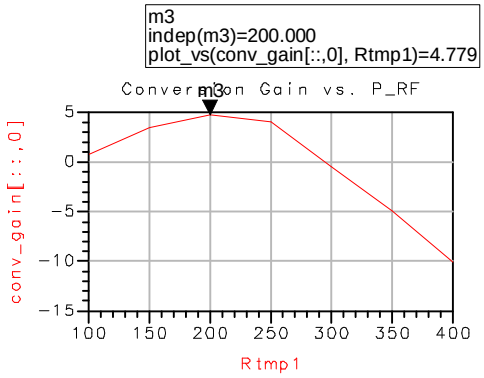


Figure 41

Conversion gain vs. Output resistance

As a conclusion, one can verify that the conversion gain is indeed proportional to the bias current and the width of the input stage transistors, since these parameters increase the transconductance of the input stage.

4.5 Linearity Results

The Gilbert Cell mixer using the source degeneration technique is depicted in Figure 42.

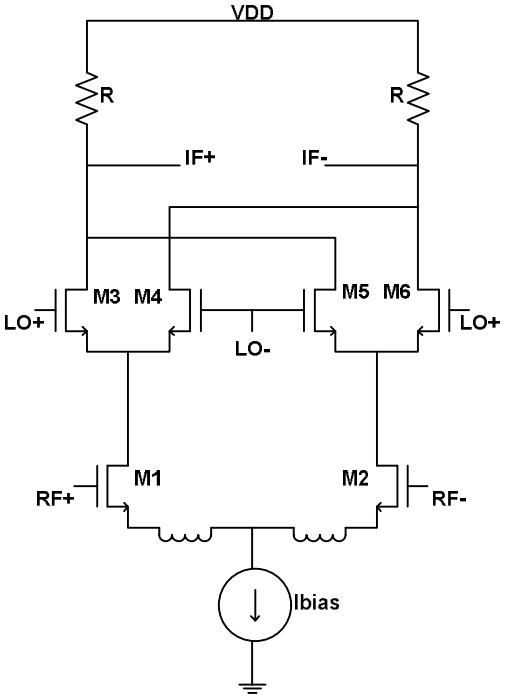
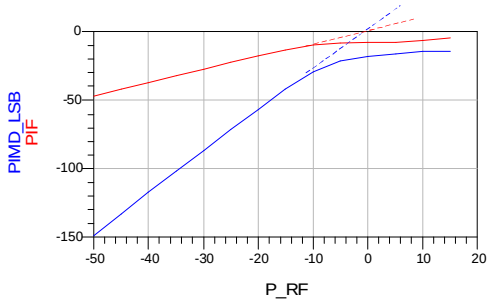


Figure 42

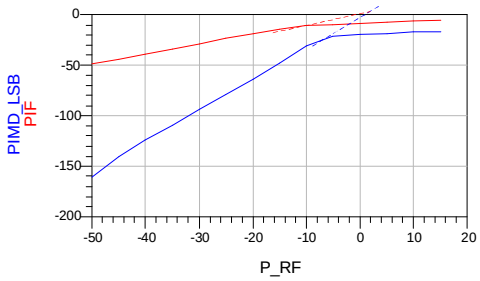
Gilbert Cell mixer with source degeneration

In our analysis, we use two input frequencies for the RF signal. One at RF+Fspacing/2 and RF-Fspacing/2. Setting Fspacing=20 KHz, we get an input tone at 5300.010 MHz and another one at 5299.99 MHz. The third order products at 2f2-f1 and 2f1-f2 will be generated at frequencies 5300.03 MHz and 5299.97 MHz, respectively. These may fall within the filter bandwidth of the IF filter, after mixing with the LO signal and thus cause interference to the desired signal. The undesired signals will be at 10.03 MHz and 9.99 MHz, respectively.

Figure 43 presents the simulated results for the 3rd order intercept point, with and without applying the source degeneration technique, for several values of the inductor, L.



(a)



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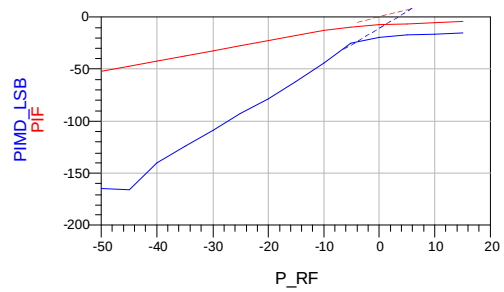

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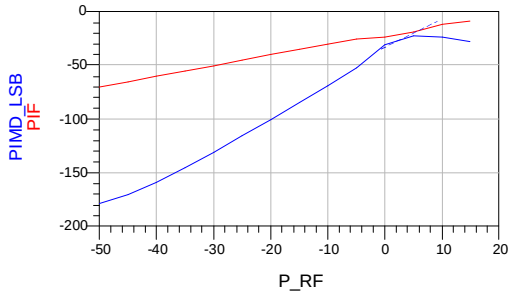
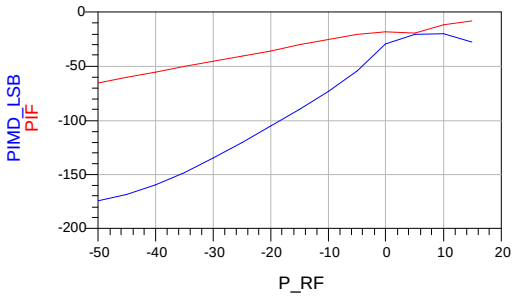


(d)

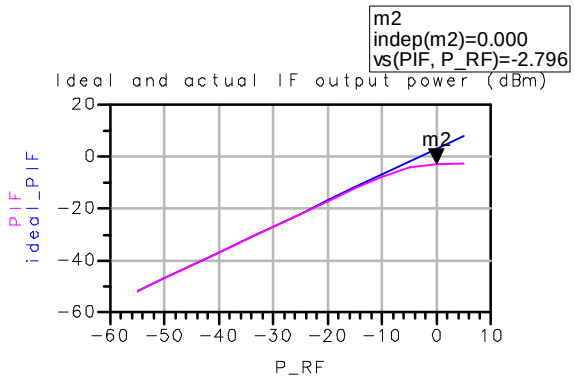


(e)

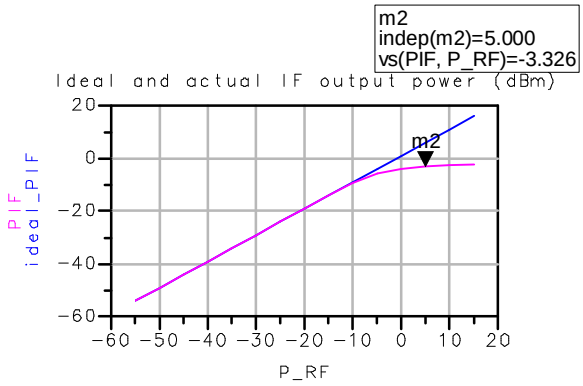
Figure 43

(a) IIP3 without source degeneration, (b) IIP3 for L=0.5 nH,
(c) IIP3 for L=1nH, (d) IIP3 for L=5 nH, (e) IIP3 for L=7 nH

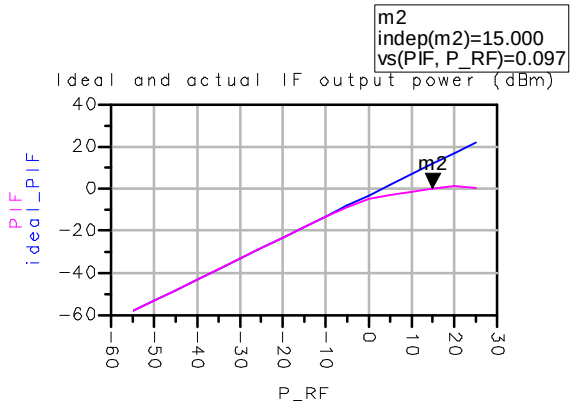
As far as the 1 dB compression point is concerned, the analysis that is performed entails both usage of source degeneration and not, so that comparisons can be done.



(a)



(b)



(c)

Figure 44

(a) 1 dB compression point without source degeneration,

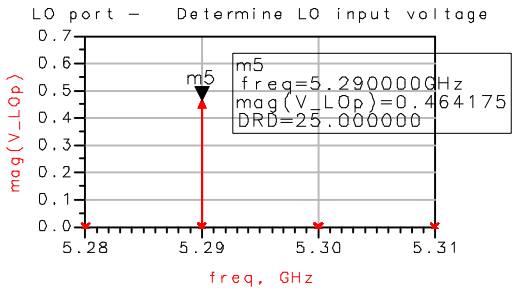
(b) 1 dB compression point for L=0.5 nH, (c) 1 dB compression point for L=1 nH

Indeed, the simulated results agree with the theoretical background. Linearity can be improved via source degeneration. More specifically, as inductance increases, linearity also improves. The trade-off in such a case is that the higher the inductance, the more the corresponding impedance seen by the circuit, a fact that deteriorates noise figure, as we will see next. As a rule of thumb, the intercept point should be 10 dBm below 1 dB compression point. This is clearly shown in the above figures.

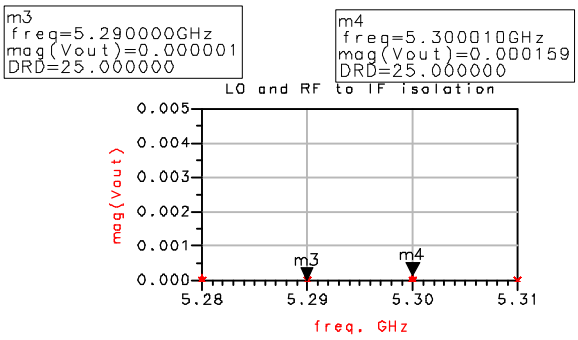
4.6 Port-to-Port Isolation – LO Feedthrough Results

As previously mentioned, the LO to RF feedthrough, may worsen the overall receiver performance, since it affects not only the mixer but also the LNA block. The LO to IF feedthrough on the other hand, plays a less significant role since, in direct conversion receivers, the frequencies of the LO and the IF signal are far apart. The simulated results are presented below.

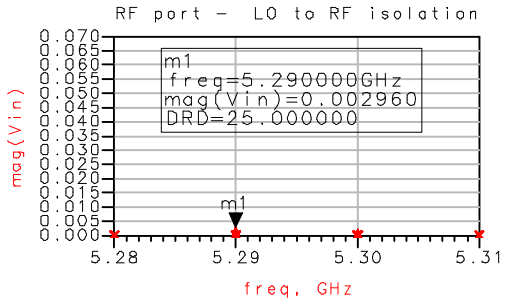
Figure 45a demonstrates the magnitude of the LO signal. Figure 45b depicts the LO and RF to IF feedthrough, while figure 45c presents the LO to IF feedthrough. Table 6 confirms that the LO to IF feedthrough is cancelled due to the double-balanced Gilbert cell mixer architecture. The main problem, which is the LO to RF feedthrough can be reduced by careful layout design. The LO to RF feedthrough value is about -44 dBm. In practice, this is the value which results as the subtraction between the injected LO power appearing at the RF port minus the LO power. It should be noticed that RD is the output resistance.



(a)



(b)



(c)

Figure 45

(a) LO signal magnitude, (b) LO and RF to IF isolation,

(c) LO to RF isolation

DRD	LO2IF	LO2RF	RF2IF	percent
5	-120.133	-43.932	-31.207	2.5
10	-120.194	-43.923	-31.122	5
15	-120.269	-43.913	-31.015	7.5
20	-120.360	-43.902	-30.883	10
25	-120.488	-43.890	-30.720	12.5

Table 6

Feedthrough in dBm

4.7 Noise Figure Results

First we will see how the output load and some other critical parameters affect the mixer's noise performance.

- Starting with the transistors' width, we observe that the minimum noise figure is obtained for W=200 um.

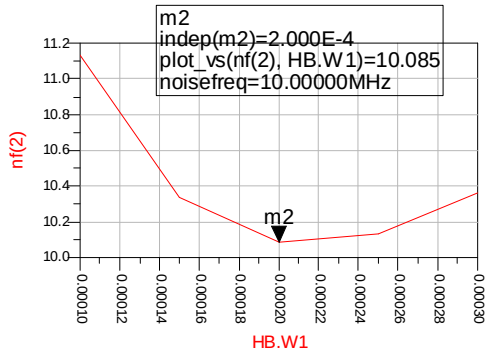


Figure 46

NF vs. transistors width

- Increasing the output resistance deteriorates noise. The minimum noise figure is obtained for R=200 Ohm.

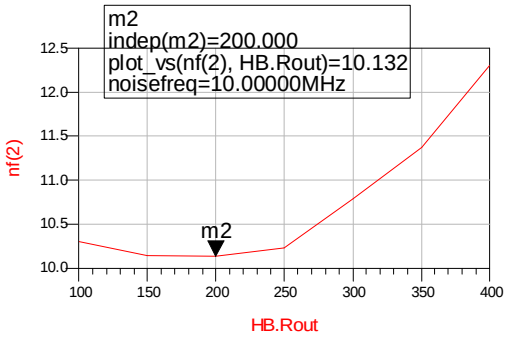


Figure 47

NF vs. output load

- The DC LO voltage is of major importance, as well. As VLO increases, noise figure falls.

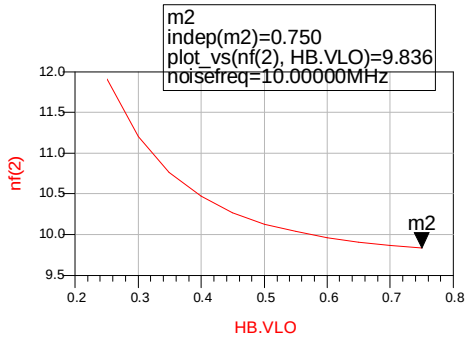


Figure 48

NF vs. VLO

4.8 Applying the Optimization Techniques

Applying the current bleeding technique and the inductive resonance technique in the mixer circuit, significantly improves the overall mixer performance. The circuit for the current bleeding technique (Figure 49) is equivalent with that of the Figure 26, with the current sources being substituted by two PMOS transistors.

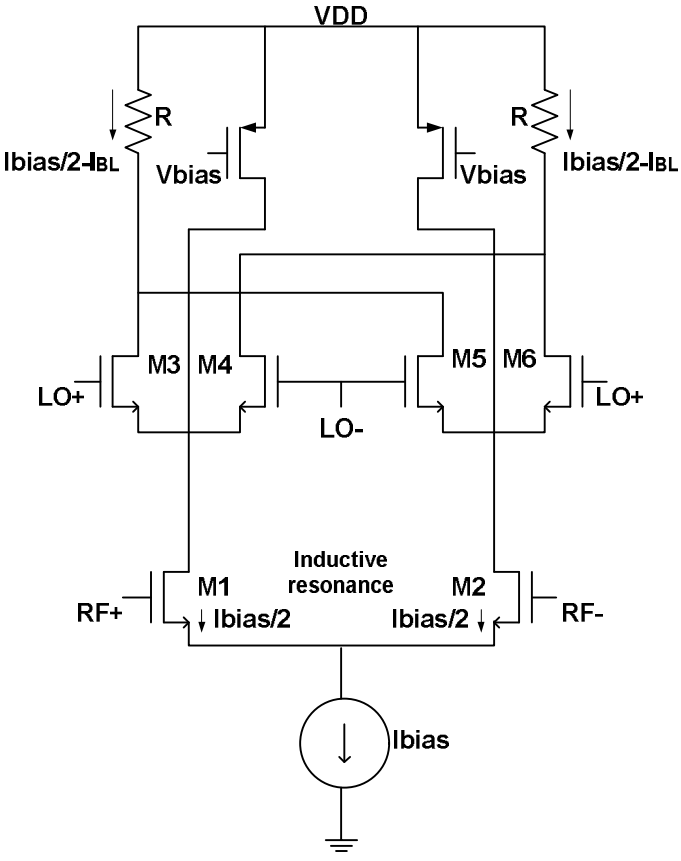
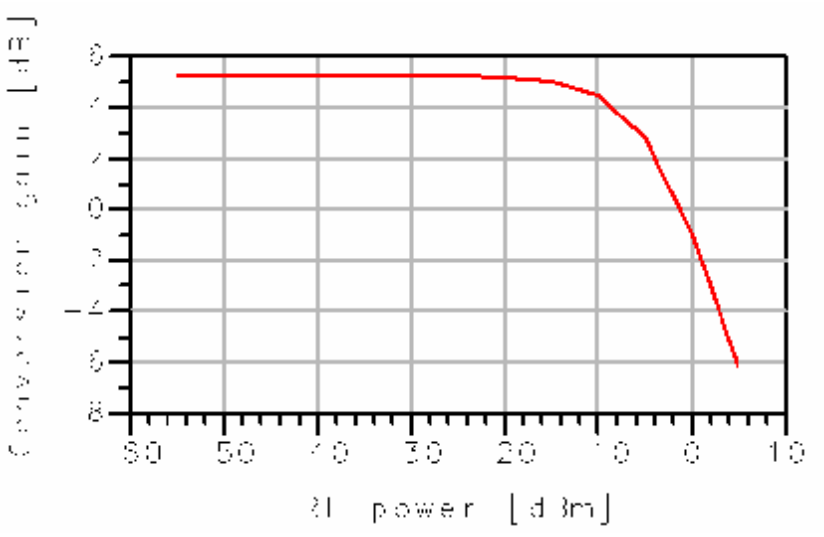


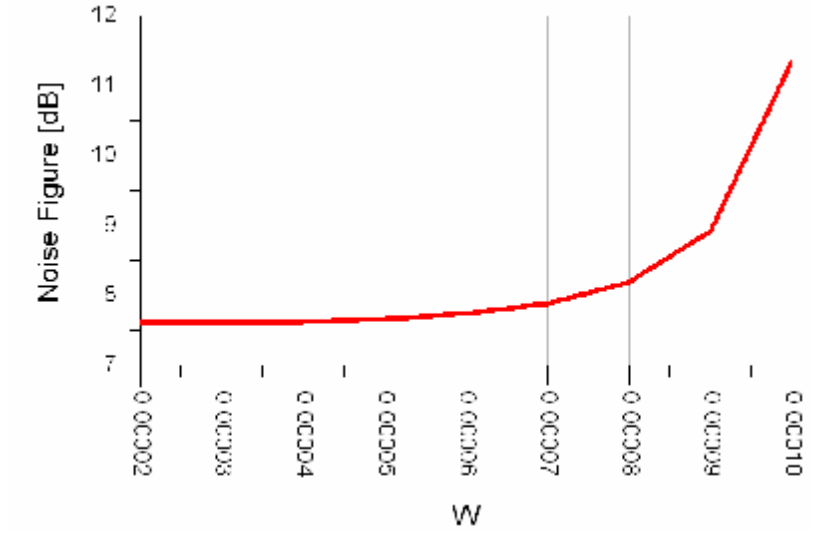
Figure 49

Current bleeding technique with PMOS transistors

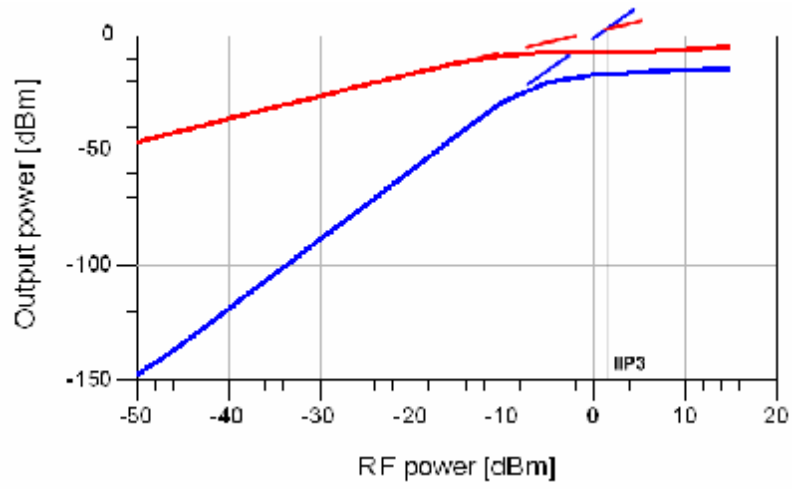
The figures of merit for the current bleeding technique and the inductive resonance technique are shown in Figures 50 and 51, respectively. Although both of them improve the mixer's performance, using an inductor in the source terminals of the switching transistors succeeds higher conversion gain and lower noise figure than using two PMOS transistors connected to the source nodes of the switching transistors. Moreover the combination of the current bleeding technique and the inductive resonance technique has been used, and the corresponding results for the conversion gain, the noise figure and the linearity are presented in Figure 52. Table 7 contains the aggregate results for the figures of merit, for each of the optimization techniques.



(a)

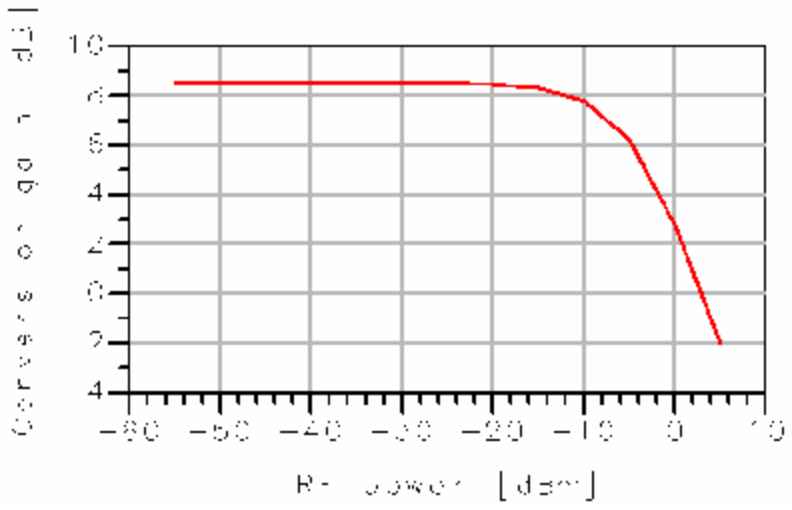


(b)

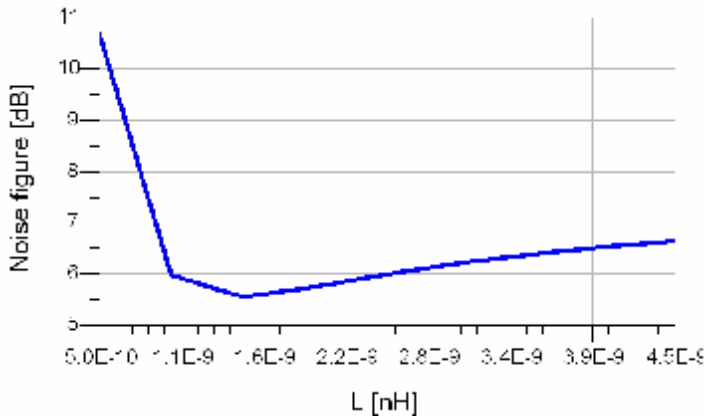


(c)

Figure 50
(a) CG vs. RF power, (b) NF vs. width W,
(c) Output power vs. RF power, for Current Bleeding Technique



(a)



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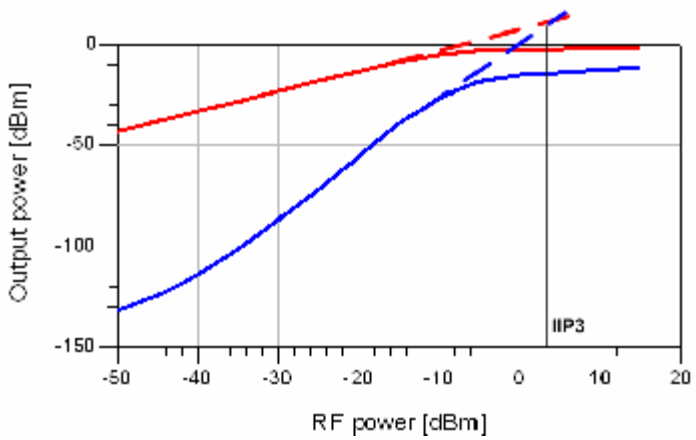
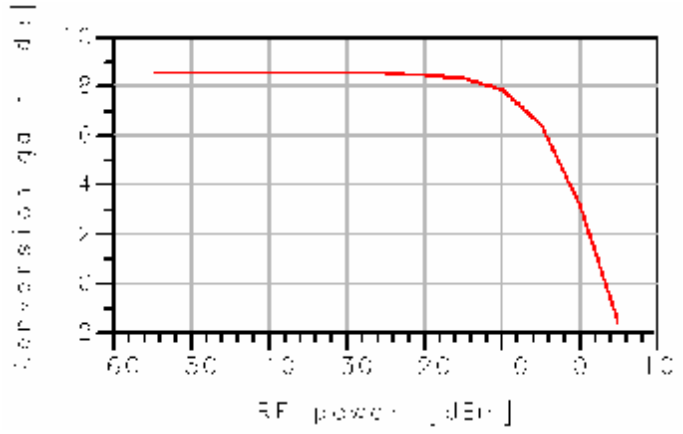


(c)

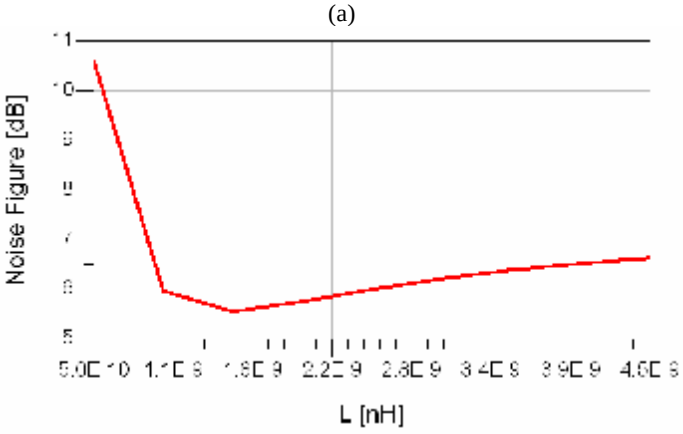
Figure 51

(a) CG vs. RF power, (b) NF vs. inductance L,

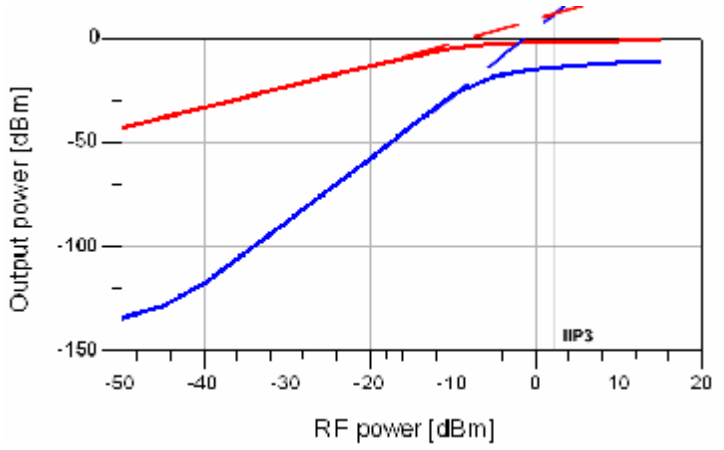
(c) Output power vs. RF power, for Inductive Resonance Technique



(a)



(b)



(c)

Figure 52

(a) CG vs. RF power, (b) NF vs. inductance L,
(c) Output power vs. RF power, for Current Bleeding with Inductive Resonance Technique

Method used	**CG [dB]**	**NF [dB]**	**IIP3 [dBm]**
Current bleeding	5.259	7.613	1
Inductive resonance	8.533	5.542	3
Current bleeding with one inductor	8.538	5.548	2

Table 7

Optimized figures of merit

4.9 Monte Carlo Simulation

The need for a statistical characterization of the mixer circuit, under random variations in the parameters of the design model, renders Monte Carlo simulation usage, necessary. The MOS parameters that undergo variation follow a Gaussian distribution (Figure 53) with a mean value and a standard deviation (Table 8). Except for the MOS parameters, the inductance (L) of the inductor used is also taken into account during Monte Carlo simulation.

Parameter	Mean value	Variation
Vth0	1	+/-0.03
Rsh	1	+/-0.11
Tox	1	+/-0.033
Cgdo	1	+/-0.25
Cgso	1	+/-0.25
Lint	1	+/-0.27
Wint	1	+/-0.56
L	1.5	+/-0.03

Table 8

Parameters' variations

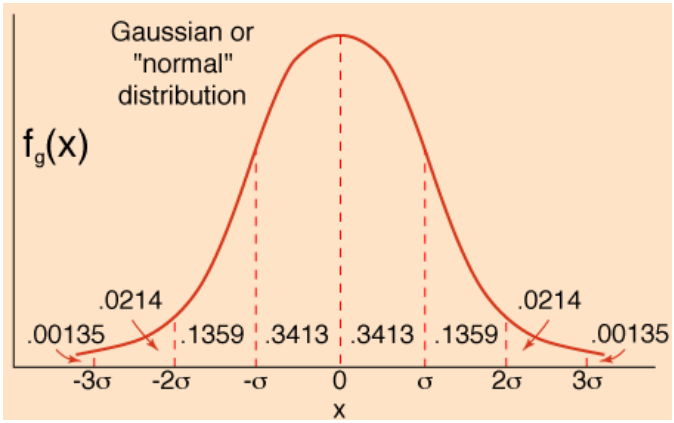


Figure 53

Gaussian distribution

The Monte Carlo method calculates the varying parameters for the transistors and the inductor, based on the process statistics and limited to a standard deviation of 3σ. The simulation is done with the typical case model. All the figures of merit are computed and the resulting histograms demonstrate the percentage of the simulations, for which each figure of merit has a specific value. These histograms are presented below.

What comes next is a thorough analysis of how the Monte Carlo simulation operates together with the way that the proper number of the simulation trials is evaluated. First of all, some terms that are going to used further on, such as Yield, Confidence level and error, should be specified.

Yield is the unit of measure for the statistical design. It is defined as the ratio of the number of designs that pass the performance specifications to the total number

of designs that are produced. It may also be thought of, as the probability that a given design sample will pass the specifications.

Confidence level is the area under a normal Gaussian curve over a given number of standard deviations. Common values for confidence level are shown in the following table.

Standard deviations	Confidence level
σ	68.3%
2σ	95.4%
3σ	99.7%

Table 9
Standard deviations – Confidence level

Error is the absolute difference between the actual yield, Y and the yield estimate, $\overline{Y}$ given by: $e = \left| Y - \overline{Y} \right|$

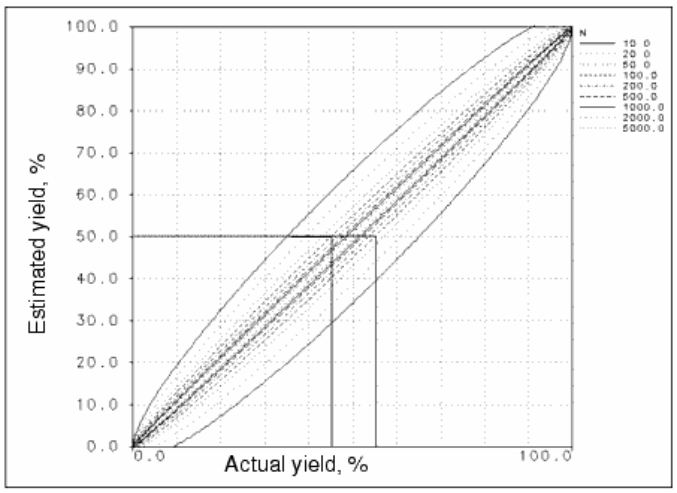
The sample or trial size, N, is then calculated from: $N = \left(\frac{C_s}{e} \right)^2 \mathbf{g} \mathrm{Y} \left(1 - \mathrm{Y} \right)$, where C_s is the confidence level, expressed as a number of standard deviations. For example, for a 95.4% confidence level ($C_s = 2$), an error of +-2% and a yield of 80%, N=1600 trials.

Figure 54 may also be helpful in determining the accuracy of a yield analysis. The three graphs plot the error bounds of the actual yield versus the estimated yield for various values of *N* (number of trials).

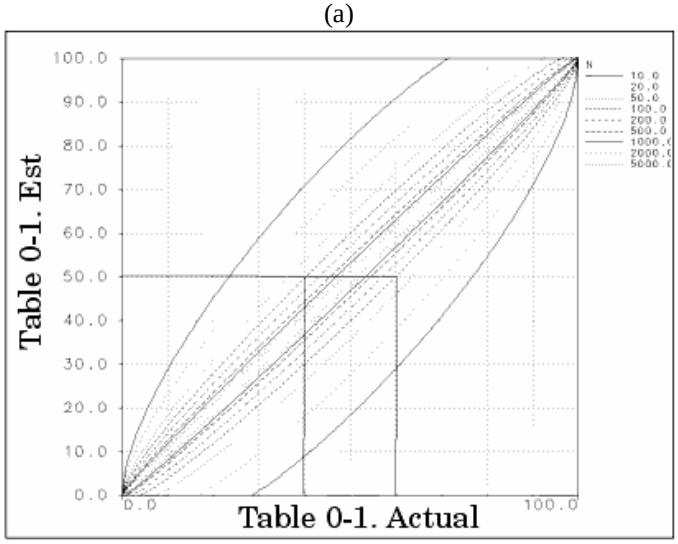
Figure 54a plots the error bounds with a confidence interval of one standard deviation, or 68.3% confidence level. Figure 54b plots the error bounds with a confidence interval of two standard deviations, or 95.4% confidence level. Figure 54c plots the error bounds with a confidence interval of three standard deviations, or 99.7% confidence level.

Suppose we run a yield analysis on our design using 100 trials and the estimated yield is 50%. Referring to the graph in Figure 54a, the lower bound on the actual yield is 45% and the upper bound is 55%. From Figure 54b, for 100 trials and an estimated yield of 50%, the lower bound on the actual yield is 40% and the upper bound is 60%. Finally, from Figure 54c, for 100 trials and an estimated yield of 50%, the lower bound on the actual yield is about 35% and the upper bound is about 65%.

Thus if we performed a yield analysis using 100 trials, and the estimated yield was 50%, we have a 68.3% probability (confidence) that the actual yield is between 45% and 55%. We also have a 95.4% probability that the actual yield is between 40% and 60%, and a probability of 99.7% that the actual yield is between 35% and 65%



(a)



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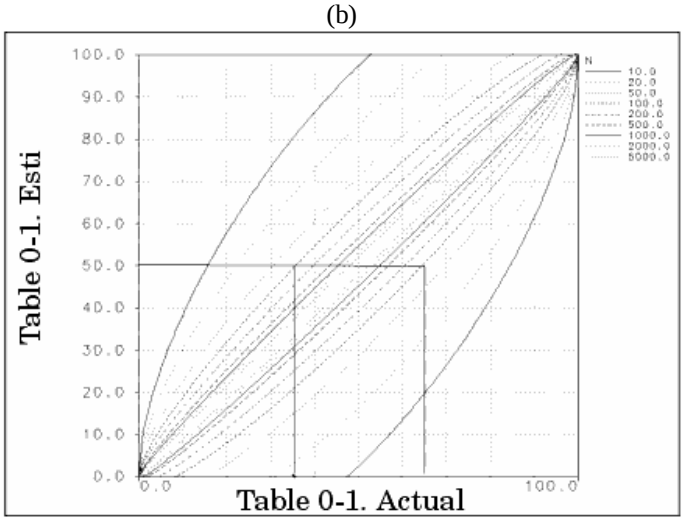


(c)

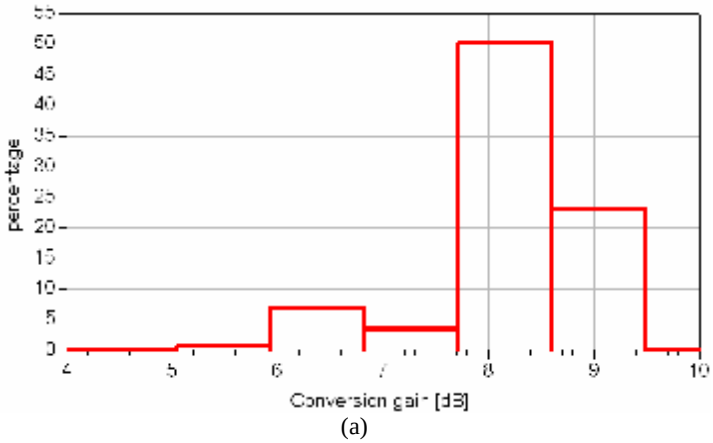
Figure 54
Estimated yield vs. actual yield for (a) σ, (b) 2σ, (c) 3σ

For a confidence level of a 99% and an actual yield of 90%(this is the best case as it includes most of the possible combinations), Table 10 demonstrates the low and high estimated yield as well as the number of trials for certain error values.

Error +/- %	Estimated yield		Number of trials
	Low	High	
1.0	89	91	5967
2.0	88	92	1491
3.0	87	93	663
4.0	86	94	372
5.0	85	95	238
6.0	84	96	165
7.0	83	97	121
8.0	82	98	93
9.0	81	99	73
10.0	80	100	59

Table 10
Number of trials needed for a 99% confidence level

The resulting histograms deriving from the statistical analysis are shown in Figure 55. The mean value of the conversion gain, the noise figure and the OIP3 are 8.5 dB, 6 dB and 4 dBm, respectively.



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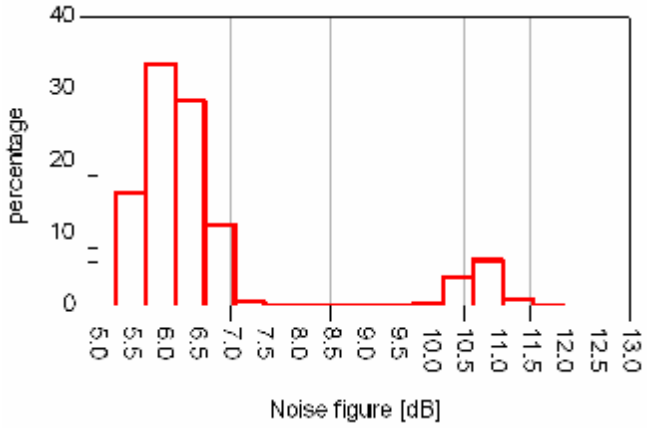

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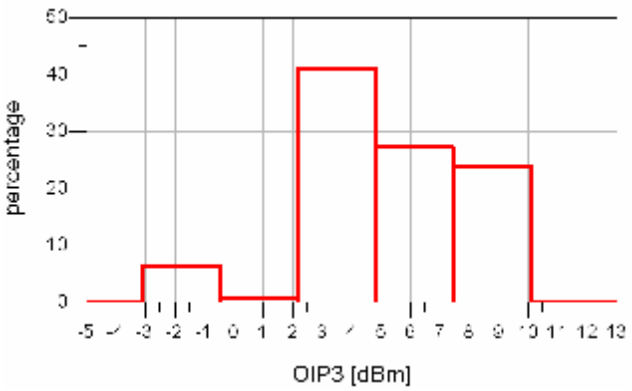


(c)

Figure 55
Monte Carlo analysis for (a) CG, (b) NF, (c) OIP3

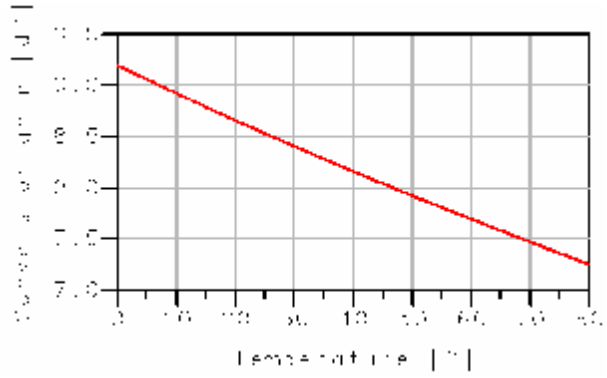
4.10 Temperature Effect on Mixer Performance

Temperature is a key parameter in mixer design, as it significantly affects conversion gain, as well as noise figure and linearity. A temperature sweep from 0 to 80 degrees Celsius is performed to study the mixer's behaviour under extreme conditions.

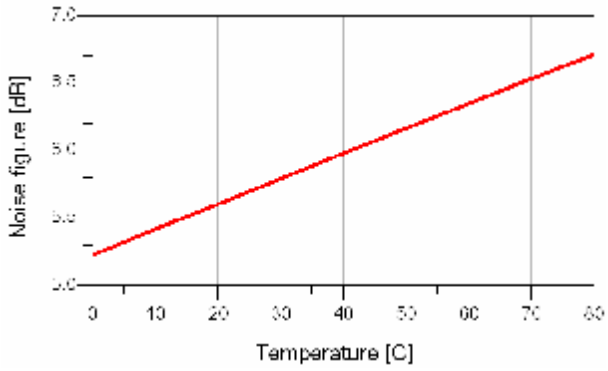
As far as conversion gain is concerned, mobility falls as temperature rises. This leads to smaller transconductance, for the same current, which in turn, results in gain reduction (Fig. 56a).

Temperature increase deteriorates the mixer's noise performance, due to the direct temperature dependence of thermal noise of resistors and transistors. Specifically, the noise due to the load resistors increases. This, together with the input referred drain current thermal noise of the input stage, increases the overall noise figure (Fig. 56b).

On the contrary, linearity improves with temperature increase, as shown in Fig. 56c.



(a)



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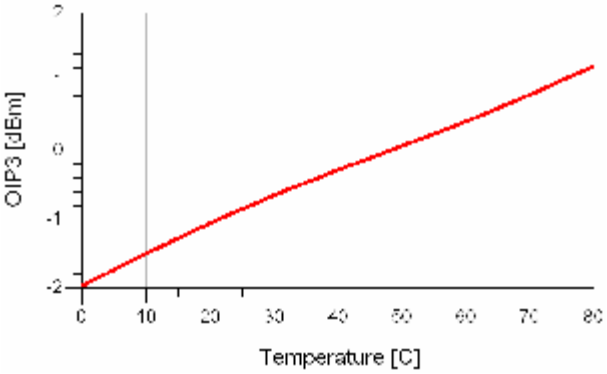

(c)

Figure 56
(a) CG, (b) NF, (c) OIP3 vs. temperature

4.11 Mixer Topology

Depending on the application, the mixer may be designed so that it succeeds best performance for specific figure(s) of merit. Talking about the WiMAX receiver, the mixer should have high conversion gain and low noise figure, whereas linearity is a matter of secondary importance. Going back to Table 7, it is the inductive resonance technique that succeeds the optimum results. So the Gilbert cell mixer with the inductive resonance technique is the dominant mixer architecture, eventually.

Applying the source degeneration technique may improve linearity but at the same time the conversion gain as well as the noise figure deteriorates. Thus, usage of the degenerated inductors is not suggested, since it adds noise to the mixer.

Table 11 presents the parameters of the transistors and the passive elements used, whereas Table 12 illustrates the final specifications of the Gilbert cell mixer.

	Transistor width/length
M1, M2	250u/0.24u
M3, M4, M5, M6	250u/0.24u
	Resistors [Ohm]
R	200
	Inductance [H]
L	1.5 n

Table 11

Mixer's parameters

Parameter	**Value**
Bias voltage	2.5 Volt
Differential LO amplitude	0.5 Volt
Power consumption	12.5 mW
Conversion Gain	8.5 dB
1 dB compression point	15 dBm
IIP3	3 dBm
NF@10MHz	5.403 dB
LO to RF	-44 dB

Table 12

Mixer Specifications

CHAPTER 5: CONCLUSIONS–FUTURE WORK

5.1 Mixer Comparison

Finally, we compare our results with other published work on mixers occupying frequencies close to 5 GHz. The conversion gain and the noise figure of the designed mixer are fairly good, while its linearity and power consumption are moderate, as shown in Table 13. The values correspond to a simulation temperature of 25° C.

Ref.	VDD [V]	Power Consumption [mW]	Freq. [GHz]	CG [dB]	NF [dB]	IIP3 [dBm]
This work	2.5	12.5	5.3	8.5	5.4	3
[8]	2.7	52.38	5.15-5.825	7.83	7.1	6.6
[9]	1.8	11.16	5.725-5.825	-2.75	11.8	5.1
[10]	1.5	6.9	5.8	7	14.3	-2.94
[11]	1.5	4.5	5.15-5.35	6.6	9	-5.4
[12]	1.8	7	5.2	16.2	9.8	-5

Table 13 Comparison with other mixer topologies

5.2 Conclusions – Future Work

This work deals with the system level analysis of a direct-conversion WiMAX receiver at 5.3 GHz and the corresponding Gilbert cell down-conversion mixer design, implemented in a 0.25um SiGe BiCMOS technology. This work exemplifies a top-down system and block-level design approach. Note that, particularly at the beginning of this work, the bibliography for WiMAX receivers was still very scarce and only more recently, has gained high attention due to the increased commercial interest in WiMAX based communication systems. Still, the literature referring to WiMAX systems at 5.3 GHz remains very limited.

The system level parametric investigation, resulted in specifications for each block, namely conversion gain, linearity, noise figure, phase noise and insertion loss of the LNA, VCO, mixer, VGA and filters.

The topology of the mixer based on Gilbert cell was analyzed in detail. The impact of current bleeding and inductive resonance techniques were analyzed. The best trade-off among performance and complexity is found with inductive resonance,

while the current bleeding does not impact performance in a significant way and is therefore discarded in the final mixer design.

The mixer complies well with the specifications derived from the system level behavioural modelling. More specifically, the mixer's conversion gain is 8.5 dB, the noise figure is 5.4 dB, and the input 3^{rd} order intercept point is 3 dBm. The above values are achieved at the cost of a power consumption of 12.5 mW. Temperature and statistical analyses confirm the robustness of the mixer's design.

Further work will be dedicated to investigating the impact of mismatch on the noise performance of the mixer. Further work should also be dedicated to the full system simulation including the other blocks, namely LNA, VCO and PLL, VGA and filters, as well as the impact of packaging. Also, layout would confer additional insight in the design of the entire receiver. Moreover, integrated multi-standard and multi-range, single chip receiver design is of ever increasing interest. While these extensions are clearly beyond the scope of the present work, they illustrate the complexity but also the challenges in achieving integrated receivers at multi-GHz frequencies. This work will be further pursued by the research group at TUC.

Finally, the present investigation resulted in the composition of a paper submitted for publication to the 15th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), 2008.

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SYSTEM LEVEL ANALYSIS OF A DIRECT-CONVERSION WIMAX RECEIVER AT 5.3 GHZ AND CORRESPONDING MIXER DESIGN

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KEYWORDS: WiMAX RECEIVER, SYSTEM LEVEL ANALYSIS, INTEGRATED CIRCUITS, GILBERT CELL MIXER DESIGN, MIXER OPTIMIZATION

ABSTRACT: The growing demand for WiMAX integrated circuits has motivated the system level analysis of a direct-conversion receiver at 5.3 GHz and the corresponding mixer circuit design. The specifications set by the IEEE WirelessMAN 802.16 protocol are met. The corresponding mixer circuit is designed in a 0.25um SiGe BiCMOS technology. Inductive resonance technique is used to succeed optimum conversion gain, as well as minimum noise figure and maximum linearity. The double-balanced Gilbert Cell mixer experiences a conversion gain of 8.5 dB, a noise figure of 5.4 dB and a input 3rd order intercept point of 3 dBm, while consuming 12.5 mW. The mixer's overall performance is exceptional compared to other published work.

INTRODUCTION

Although Wireless Local Area Network (WLAN) is still the dominating technology in wireless transfer, the need for more capacity and greater coverage (~50 km) at high transfer rates (~70 Mbps) has rendered Worldwide Interoperability for Microwave Access (WiMAX) one of the most promising technologies in the immediate future.

Significant research is being dedicated to WiMAX, and the first networks are already in use covering the frequency bands in the range of 2.5 to 3.5 GHz. Therefore, the need for cost-effective, integrated transceivers, which comply with the requirements of the Wireless Metropolitan Area Network (WMAN) protocol, covering higher frequency bands, above 5 GHz, becomes even higher.

Based on the above motivations we present a system level analysis of a direct-conversion WiMAX receiver at 5.3 GHz, which can accommodate both fixed and mobile broadband applications. Furthermore, the circuit design of the corresponding downconversion mixer is presented.

The design is performed with a 0.25um SiGe BiCMOS technology. While the receiver presented in this work is implemented using MOS transistors only, the bipolars are used for the implementation of the power amplifier of the transmitter (not presented here).

The fourth revision of WMAN, 802.16d [1], defines the requirements for the receiver. The occupied frequencies can be in the range of 2 – 11 GHz. Table 1 lists the minimum receiver sensitivity for different modulation schemes [2]. The maximum noise figure (NF) of the receiver is limited to 7 dB.

TABLE 1. Receiver sensitivity for IEEE 802.16

		Minimum Sensitivity [dBm]
QPSK	1/2	-80
	3/4	-78
16-QAM	1/2	-73
	3/4	-71
64-QAM	2/3	-66
	3/4	-65

RECEIVER ARCHITECTURE

The homodyne receiver architecture (Fig. 1) is used. The direct conversion architecture enhances image rejection, compared to the heterodyne architecture. Moreover, direct conversion decreases receiver complexity, since the usage of an image-reject filter is unnecessary. This in turn reduces the number of the receiver blocks, thus relaxing the specifications of the individual components.

The RF front-end consists of a low-noise amplifier (LNA), two band-pass filters, a mixer, a voltage controlled oscillator (VCO) and a voltage gain amplifier (VGA).

The RF signal, received by the antenna, modulated with 64-QAM with a coding rate of 3/4, is about -65 dBm (Table 1). It is centered around 5.3 GHz and should firstly be amplified by a LNA, because of the attenuation it has undergone during transmission. Subsequently, a band-pass filter isolates the out-of-channel interferers as well as cuts-off the frequency bands below 10 MHz or above 20 MHz (bandwidth of the WiMAX signal). Next, the signal passes through the mixer stage, where downconversion occurs. The local oscillator (LO) signal feeding the mixer is produced by a VCO, giving a signal at a power of -5 dBm, much stronger than the RF signal. The LO signal is centered at 5.29 GHz. The resulting signal is a pass-band signal of 10 MHz, filtered and amplified by a VGA, before being demodulated.

The first stages of the chain (LNA and mixer) are the main contributors to the overall noise figure, whereas the latter stages (VGA) are mainly responsible for the linearity. The receiver's noise figure is also affected by the VCO phase noise at various offsets from the fundamental frequency. A parametric analysis is carried out to acquire the specifications of the individual blocks. The analysis is performed in Advanced Design System (ADS) 2006. Each of the blocks, i.e. LNA, VCO, mixer, VGA, is described by a behavioural model available also within ADS, and contains the basic figures such as noise figure and phase noise, gain, insertion loss, linearity etc. A harmonic balance (HB) noise controller provides the opportunity of evaluating the phase noise effect on the overall noise figure. The VCO phase noise is calculated for four different offsets. The aim is to keep the total noise figure lower than the aforementioned 7 dB required by the WMAN protocol. A two-tone HB simulation is performed to obtain the total noise figure of the receiver versus the phase noise of the VCO, for different values of the noise figure of the LNA. The result for a frequency offset of 10 kHz is depicted in Fig. 2. This analysis shows that the noise of the receiver fulfils the receiver's specification in case of a phase noise lower than -88dB and a noise figure of the LNA lower than 3 dB. Similar analysis is repeated at offsets of 100 kHz, 600 kHz and 1 MHz.

The VCO phase noise power in dBc (dB with respect to carrier), as well as the noise figure, the conversion gain and the input 3rd order intercept point of the remaining components are presented in Table 2. The total conversion gain is 66 dB. Thus, the resulting baseband signal at 10 MHz is about 1 dBm. The overall noise figure is 6.89 dB, an acceptable value.

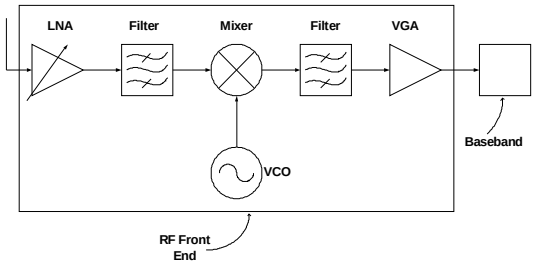


Fig. 1. Direct-conversion receiver

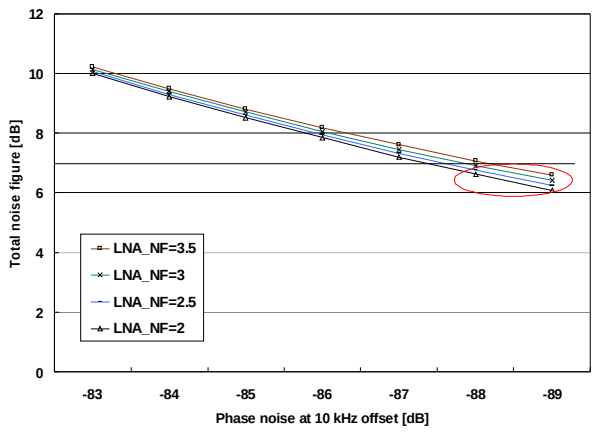


Fig.2. NF vs. phase noise at 10 kHz offset

TABLE 2. Receiver specifications

	CG [dB]	NF [dB]	IIP3 [dBm]	Phase Noise [dB]	
LNA	18	3	-7	-	
Filter	0	2	-	-	
Mixer	8	6	6	-	
VCO	0	-	-	10kHz	-88
				100kHz	-110
				600kHz	-125
				1MHz	-130
Filter	0	2	-	-	
VGA	40	10	12	-	

Next, we proceed with the design of the mixer, according to the above specifications.

MIXER DESIGN

The mixers are of great significance in a wireless system because of their operation and their location in the entire receiver chain. They are responsible for the frequency translation of the RF signal to an intermediate frequency (IF), in heterodyne architectures, or to baseband, in homodyne architectures. The design of RF CMOS mixers is not simple since a low noise figure, a moderate conversion gain and a high linearity should be obtained simultaneously.

Gilbert Cell Mixer

The mixer circuit that is widely used in wireless communications is the Gilbert-type mixer. It is a fully symmetric, differential output topology, which is preferred over other topologies because of its higher gain and immunity to feedthrough from RF to IF. As depicted in Fig. 3, the double-balanced Gilbert cell mixer consists of two stages. The input or transconductance stage is composed of transistors M1 and M2, while M3 to M6 form the switching stage.

The input stage performs a voltage to current conversion of the RF signal. This current flows to the mixer output through the switching transistors M3 to M6, which manage current in a way that it appears to the output with a phase difference of 180°. This demands a powerful LO signal so that switching is done simultaneously. The effect of the switching is to multiply the AC current with a square wave alternating between -1 and +1 at the frequency of the local oscillator.

The double-balanced architecture is used instead of the single-ended one, because it suppresses the LO to IF feedthrough.

The AC current at the mixer output is delivered to the load, which may be passive (resistors) or active (transistors), where it is converted to voltage.

Polysilicon resistors, which are free of flicker noise, are usually preferred [3].

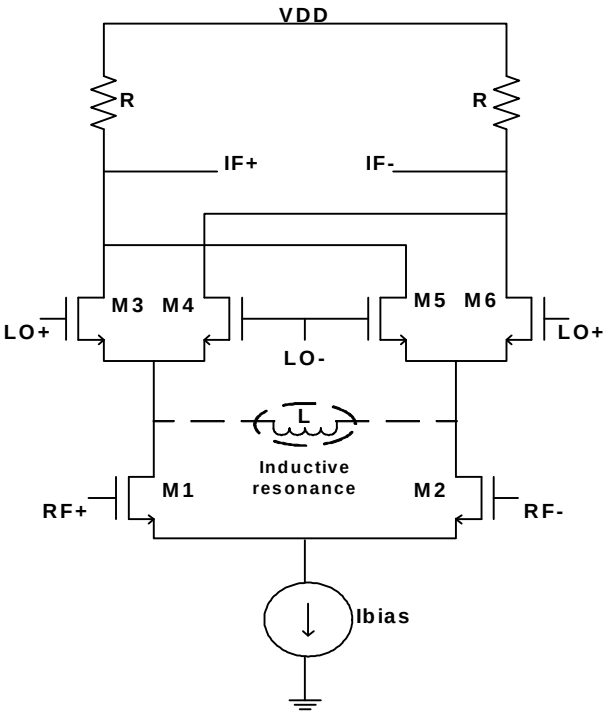


Fig.3. Schematic of the Gilbert cell mixer with inductive resonance technique

Figures of Merit

During mixer design, suitable trade-offs among the different figures of merit need to be achieved. No single figure of merit can be considered independently of others. In the following, conversion gain, linearity and noise figure are examined, as well as their interdependences.

Conversion Gain.

The signals at the input and the output of the mixer are at different frequencies, RF and IF, respectively. Thus the term conversion gain, instead of gain, is used to describe the gain seen when the input signal appears at the output. Conversion gain [4] equals to:

$$CG = \frac{2}{p} G_m R \tag{1}$$

where

$$G_m = \frac{1}{2} K \frac{4I_{bias} / K - 2V^2_{RF}}{\sqrt{4I_{bias} / K - V^2_{RF}}} \tag{2}$$

The transconductance is maximum for small input voltages, where $V_{RF+} = V_{RF-}$ and $V_{RF} = 0$. Supposing that M1 and M2 are well matched, this maximum transconductance is:

$$G_{m\max} = \sqrt{m_0 \cdot C_{OX} \cdot W_2 / L_2 \cdot I_{bias}} \tag{3}$$

Increment of conversion gain may be achieved by either increasing bias current or the dimensions of transistors M1, M2. This trades off with higher power consumption.

Linearity.

As a measure of the degree of departure from linear mixing behaviour, one can plot the desired output and the 3rd intermodulation output as a function of the input RF level. The 3rd order intercept point [5] is the extrapolated intersection of these two curves, given by:

$$IIP_3 = dB_{20} \sqrt{\frac{16 I_{bias}}{3K^3}} \tag{4}$$

where K is a constant depending on the technology and the transistor dimensions and is proportional to the transistor's width.

The above equation demonstrates that linearity also increases as bias current increases.

Another parameter denoting linearity is the 1 dB compression point. As a rule of thumb, the intercept point should be about 10 dBm below the 1 dB compression point.

A commonly used technique to increase linearity is source degeneration. However, while indeed linearity is improved, the mixer's noise performance is degraded due to the presence of resistances. Therefore, this technique is not used.

Noise Figure.

The total input referred noise of the RF receiver determines the smallest signal that can be processed by the receiver, setting a lower band on the dynamic range of the receiver. Two types of noise figure have been defined for mixers: single-sideband (SSB) and double-sideband (DSB). In direct-conversion receivers, the LO signal is at the same frequency as the RF signal, since the RF channel has to be downconverted to baseband. Thus, DSB figure is applicable in homodyne architectures.

The white noise spectral density due to the load is given by [4]:

$$U^2_n = 4kTR \tag{5}$$

where k is the Boltzmann's constant and T is the absolute temperature in Kelvin.

The input referred drain current thermal noise of the input stage is [5]:

$$U_n^2 = \frac{4kTg}{G_m} \tag{6}$$

Flicker noise is important since we deal with a zero-IF receiver. Flicker noise in loads competes the useful signal deteriorating the mixer's noise performance. However, flicker noise is not present at the transconductance stage since it is unconverted to w_{LO}

during frequency translation. On the other hand, $1/f$ noise appears at the output through the switching stage and through an indirect mechanism, which stems from the parasitic capacitance viewed at the source nodes of the switching transistors [3].

Inductive Resonance Technique

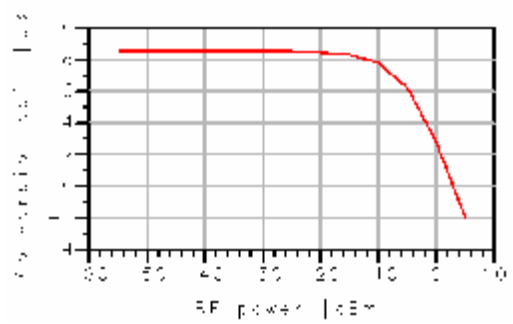
Several techniques have been proposed to improve the overall mixer performance. In this paper, the inductive resonance technique is used with satisfactory results. Fig. 4 depicts the CG, the NF and the IIP3, applying the optimization technique in the Gilbert cell mixer.

One of the most limiting factors in mixer design is the parasitic capacitance appearing at the source nodes of the switching transistors, affecting noise, gain and linearity. Thus, usage of a capacitive neutralization technique is necessary (Fig. 3).

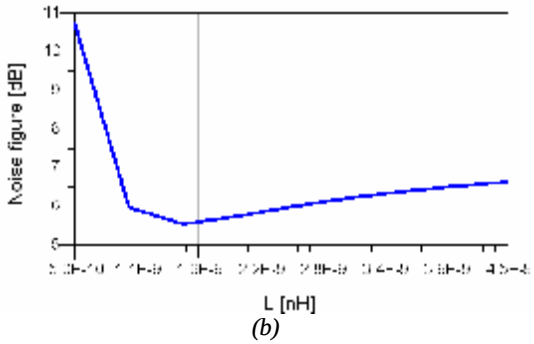
The problem can be solved if we place an inductor, between the source nodes of the switching stage transistors. The inductor's value is chosen so that it resonates with the parasitic capacitance at these nodes, at the desired frequency of the RF input signal.

The purpose is to prevent current from flowing to ground through the parasitic pathways but rather drive it to the output via the switching stage.

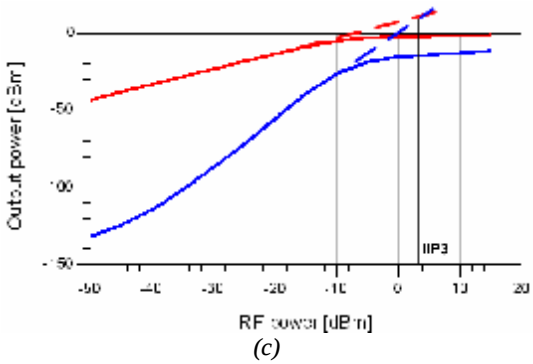
The appropriate value for the inductor is 1.5 nH with an equivalent quality factor of 15 and a series resistance of 3 Ohm.



(a)



(b)



(c)

Fig.4. (a) CG vs. RF power, (b) NF vs. inductance L, (c) Output power vs. RF power

TABLE 3. Mixer's parameters

	Transistor width/length
M1, M2	250u/0.24u
M3, M4, M5, M6	250u/0.24u
	Resistors [Ohm]
R	200
	Inductance [H]
L	1.5 n

The mixer's bias circuit is a current mirror, multiplying the input current, which is 5 mA, with the desired current gain. The supply voltage is 2.5 V and the differential LO signal amplitude is 0.5 V.

The above graphs result for specific values of the mixer's parameters presented in Table 3.

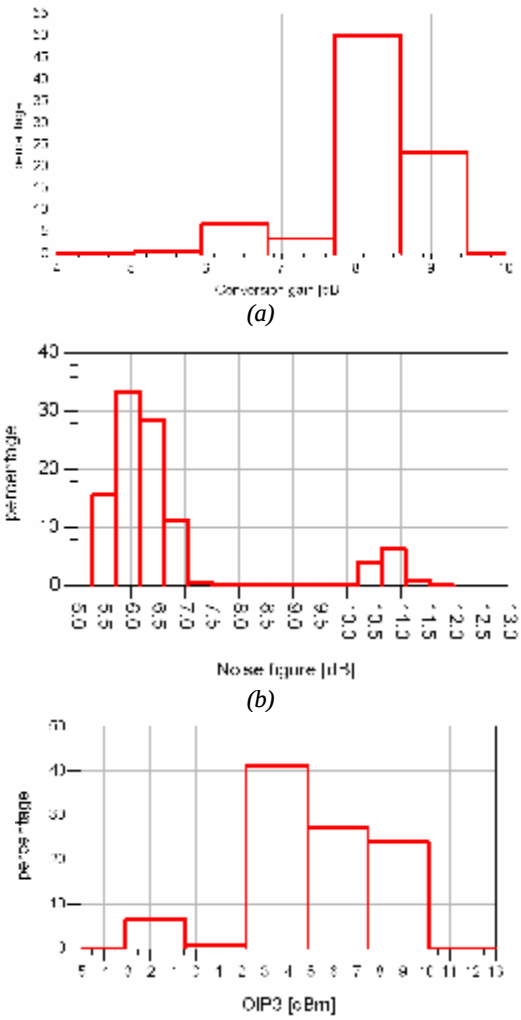
Statistical Analysis

The random process variations in CMOS technology manufacturing require a statistical analysis of the circuits (Monte Carlo simulation). In the SiGe BiCMOS design kit used, the parameters of the transistor's model (BSIM3v3), namely VTH0, RSH, CGDO, CGSO, TOX, LINT, WINT are described by statistically independent Gaussian distributions. Furthermore, the inductor's value L is also subject to a Gaussian distribution.

For a confidence level (the area under a normal Gaussian curve over a given number of standard deviations) of 99% (3σ) and an actual yield (the ratio of the number of designs that pass the performance specifications to the total number of designs that are produced) of 90%, with an error of ±2%, the proper number of trials is 1491.

The histograms that result, for all figures of merit, are shown in Fig. 5.

Note that evaluation of device-to-device mismatch might be a further important effect, particularly in view of upconversion of flicker noise. Investigation of mismatch is still underway.



(a)

(b)

(c)

Fig.5. Monte Carlo analysis for (a) CG, (b) NF, (c) OIP3

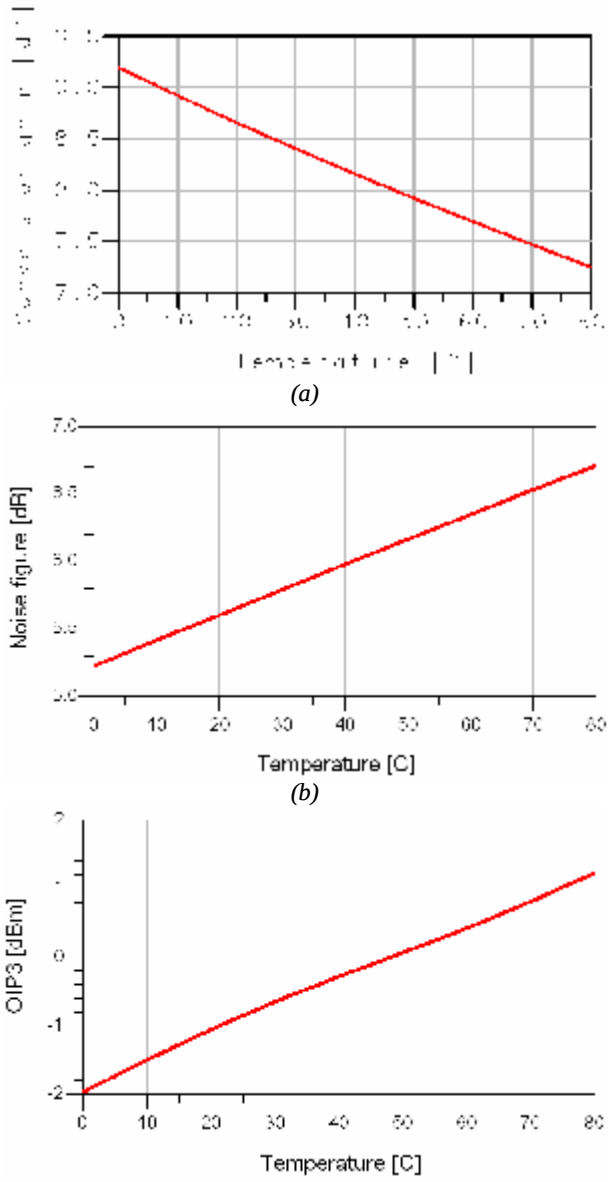
Temperature Effect on Mixer Performance

Temperature is a key parameter in mixer design, as it significantly affects conversion gain, as well as noise figure and linearity. A temperature sweep from 0 to 80 degrees Celsius is performed to study the mixer's behaviour under extreme conditions.

As far as conversion gain is concerned, mobility falls as temperature rises. This leads to smaller transconductance, for the same current, which in turn, results in gain reduction (Fig. 6a).

Temperature increase deteriorates the mixer's noise performance, due to the direct temperature dependence of thermal noise of resistors and transistors. Specifically, the noise due to the load resistors increases. This, together with the input referred drain current thermal noise of the input stage, increases the overall noise figure (Fig. 6b).

On the contrary, linearity improves with temperature increase, as shown in Fig. 6c.



(a)

(b)

(c)

Fig.6. (a) CG, (b) NF, (c) OIP3 vs. temperature

Mixer Comparison

Finally, we compare our results with other published work on mixers occupying frequencies close to 5.3 GHz. The conversion gain and the noise figure of the designed mixer are fairly good, while its linearity and power consumption are moderate, as shown in Table 4. The values correspond to a simulation temperature of 25° C.

TABLE 4. Comparison with other mixer topologies

Ref.	VDD [V]	Power Consumption [mW]	Freq. [GHz]	CG [dB]	NF [dB]	IIP3 [dBm]
This work	2.5	12.5	5.3	8.5	5.4	3
[6]	2.7	52.38	5.15-5.825	7.83	7.1	6.6
[7]	1.8	11.16	5.725-5.825	-2.75	11.8	5.1
[8]	1.5	6.9	5.8	7	14.3	-2.94
[9]	1.5	4.5	5.15-5.35	6.6	9	-5.4

CONCLUSIONS

This work deals with the system level analysis of a direct-conversion WiMAX receiver at 5.3 GHz and the corresponding Gilbert cell mixer design, implemented in a 0.25um SiGe BiCMOS technology. This paper exemplifies a top-down system and block-level design approach.

The system level parametric investigation results in specifications for each block, namely conversion gain, linearity, noise figure, phase noise and insertion loss of the LNA, VCO, mixer, VGA and filters.

The mixer complies well with the specifications derived from system level behavioural modelling. More specifically, the mixer's conversion gain is 8.5 dB, the noise figure is 5.4 dB, and the input 3rd order intercept point is 3 dBm. The above values are achieved at the cost of a power consumption of 12.5 mW. Temperature and statistical analyses confirm the robustness of the mixer's design. Further work will be dedicated to investigating the impact of mismatch on the noise performance of the mixer. Results of this investigation are expected to be available in the final version of the paper, if accepted.

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