TECHNICAL UNIVERSITY OF CRETE

School of Electrical & Computer Engineering

Design of Micropower Operational Transconductance Amplifiers for High Total Ionizing Dose (TID) Effects and Aspects of Implementation of a Dedicated 65 nm CMOS TID-Process Design Kit

MSc Diploma Thesis

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Acknowledgements

Firstly, I would like to thank Associate Professor Matthias Bucher for giving me the chance to work on such an interesting and innovative project for my MSc diploma thesis and for our long term cooperation and collaboration in different projects. I would like to sincerely thank Professor Aggelos Bletsas and Professor Spyridon Vlassis for their participation in my MSc Thesis Committee.

Secondly, I would like to thank all members of the Electronics Laboratory of Technical University of Crete, former and present, and especially Nikolaos Gouvatsos, Loukas Chevas, Aristeidis Nikolaou and Nikolaos Makris.

Last but not least, I would like to thank my family and my dog Aria for their unconditional love and support throughout the years.

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Chapter 1

Introduction

All microelectronic parts intended for space, avionics, military and nuclear physics applications pose strict requirements for radiation hardness. Radiation hardness is the ability of components and circuits to withstand damages and alterations caused by high levels of ionizing radiation, which may lead to malfunction. Ionization of materials is caused by the interaction of high energy photons or charged particles (i.e. protons, electrons, or energetic heavy ions) with the atoms of the material. Photon-induced ionization damage is initiated when electron-hole-pairs (ehps) are generated along the track of secondary electrons emitted via photon-material interactions. Protons and other charged particles, also, generate ehps that lead to ionization damage. [1] In other words, the effects of ionizing radiation are due to positive trapped charges and creation of interface traps in oxides. [2]

In the past, the demand for radiation hardened circuit designs led to the development of the so called radiation hardened technologies. Radiation hardened technologies are dedicated manufacturing processes that were developed specifically for aerospace applications. Lockheed–Martin, Manassas, VA, and Honeywell Solid State Electronics Center, Plymouth, MN, are two specialized rad-hard foundries that successfully provided hardened components for space electronics. Several studies were presented for the development of such technologies. In [3] a technique is presented for optimizing the radiation hardness of parts produced by a Si-gate CMOS process. In [4] techniques for optimized dry oxide processes are presented for improving CMOS radiation hardness. Using rad-hard processes was a traditional method of achieving radiation hardness in space-qualified electronics for many decades. However, the inherent added complexity of these specialty processes combined with their low-volume demand has led to an inevitable gap (2 generations) in the performance of available components compared to common commercial parts. [5] Another disadvantage of dedicated rad-hard technologies is the prohibitive costs due to the low-volume demand.

While many space systems will continue to depend on radiation-hardened components from rad-hard foundries to meet their requirements, many commercial and military aerospace applications can make effective use of rad-tolerant and rad-hard components using commercial foundries. [5] CMOS radiation-hardened by design (RHBD) methodologies were introduced in

that direction, as an alternative to rad-hard processes. The increasing demand for higher system performance is responsible for the shift toward the use of commercial foundry CMOS processes for space applications. The availability of advanced CMOS technologies has, also, resulted in the use of such technologies throughout the spectrum of the aforementioned applications.

CMOS radiation-hardened by design methodologies rely on circuit level design techniques to alleviate the performance degradation due to ionizing radiation. In [6] a probabilistic analysis technique has been presented that effectively identifies the origins of a variety of transients generated within a voltage controlled oscillator (VCO). In this case, additional output buffers were needed towards an effective RHBD VCO. In [7] an instrumentation amplifier (IA) designed in 180 nm bulk CMOS used to amplify fine signals of sensors is presented. The RHBD IA contains additional sub-circuits to ensure stable voltage supply. Another RHBD technique includes using guard banding around NMOS or PMOS (or both) transistors that can reduce the susceptibility of CMOS circuits to latch-up. In addition, the use of edge-less MOSFETS (i.e. Enclosed Gate (EG) MOSFETS) in the place of conventional bulk MOSFETS eliminates the excessive radiation-induced edge leakage. [5] In [8] three static RAM cells are presented designed to be rad-hard, including also the use of EG MOSFETS. All RHBD techniques discussed increase the required area and power.

The key concern for aerospace and nuclear physics applications is the impact of total ionizing dose (TID) on CMOS device performance, which may degrade critical device operating characteristics such as leakage currents, threshold voltage (V_{th}), sub-threshold slope (n), carrier mobility (μ) and transconductance (g_m). [9] Previous work has proven that the effects of total ionizing dose on devices fabricated in deep sub-micron bulk CMOS processes show little change in threshold voltage and transconductance, but the leakage current increases significantly. However, there is an exponential dependence on the threshold voltage in the weak inversion current equation, which means that even small changes (shifts that may be considered negligible at nominal supply voltages) may have a more pronounced effect in ultra low power circuits. So, the most common effects of total dose damage in bulk silicon CMOS technologies can have a substantial effect on the operating characteristics of circuits in the sub-threshold region. [10], [11] In devices hit just by a single ion, g_m and I_{ds} (drain current) decrease, due to formation of a physically damaged oxide region around the ion hit spot, whose size is estimated around 0.2 μm. This is comparable with the MOSFET width and so it is able to hamper the current conduction. [10] Furthermore, very thin gate oxide of deep sub-micron technologies (5 nm for a 250 nm technology) is inherently more radiation tolerant than the one of older technologies. In [12] it is shown that threshold voltage shifts, sub-threshold slope and transconductance degradation after 30 Mrad(SiO_2) are small enough to be tolerable in circuit design. In [13] several issues affecting the radiation hardness of shallow trench isolation (STI) are discussed, which is used as the device isolation process of choice. In modern processes, the predominant TID effect is due to trapped positive charge in the STI oxides. Consequently, STI does not prevent post irradiation leakage in deep sub-micron technologies.

Moreover, in high energy physics (HEP) experiments, such as the High-Luminosity Large

Hadron Collider (HL-LHC) at CERN, high TID levels up to 1 Grad (SiO_2) are expected, where front-end electronics such as particle detectors are designed in bulk silicon CMOS. [14] Standard radiation hardness test methods that work well for MOS devices at lower dose levels are not easily applied in the characterization and qualification of devices for use in environments with multi-Mrad or Grad TID requirements. Special attention in testing and analysis is required to ensure that all possible failure mechanisms are evaluated. [15]

Fully radiation-hardened electronics fabricated in dedicated rad-hard processes have provided reliable aerospace systems in decades. However, it is shown that using a RHBD design approach in combination with radiation tolerant commercial CMOS foundry processes is likely to meet the ASIC requirements of many applications, while delivering enhanced performance compared to dedicated radiation hardened based electronics. The qualification of commercial CMOS foundry processes is an issue that must be addressed if use in aerospace applications is intended.

In case of modern VLSI integrated circuits (ICs), a common test approach is based on choosing and controlling the conditions of IC's operation under irradiation to be the simplest possible and measuring selected electric parameters, i.e. output voltages, input/output currents etc. Static and dynamic operation of ICs under total ionizing dose (TID) effects usually leads to various estimations of radiation hardness levels. The downside of this approach is that the majority of radiation test facilities are not specialized for conducting IC radiation tests with accuracy and precision. [16]

A behavioral modeling technique has been developed for creating TID-aware behavioral models of voltage feedback op-amps without the creation of an underlying SPICE macro-model. This type of sensitivity analysis can be particularly useful for determining which portion of a circuit is most affected by TID and where to more effectively harden a system against TID degradation. [17] As also in [18] an original technique for TID testing of complex VLSI circuits (microprocessors) based on combined use of parametric and functional control is presented. In the latter case, the resulting dependencies obtained in radiation experiments are qualitatively confirmed by circuit simulation. This approach limits the conclusions to specific circuit topologies and chip families.

The scope of this work is to provide insight in the way high TID phenomena affect micropower analog CMOS design, as well as to show the effectiveness of inversion-level based techniques for radiation hardened design.

In the present work, a dedicated 65 nm CMOS TID-Process Design Kit is presented in Chapter 2. This TID-PDK allows the designer to choose models that account for effects of ultra high TID levels, namely 100, 200 and 500 Mrad(SiO2), established for TID experiments carried out at three different temperatures (-30, 0 and 25 °). This TID-PDK is an expansion to a commercial CMOS foundry 65 nm general purpose process. The expanded version of 65 nm bulk CMOS PDK is developed at Technical University of Crete (TUC) for the European Organization for Nuclear Research (CERN). An inversion coefficient based design methodology is also discussed in Chapter 2, as the design methodology of choice for this work. Finally, the

scaling of important design parameters (i.e. threshold voltage (V_{th})) under high TID levels is presented.

In Chapter 3, we discuss the concept of operational transconductance amplifiers (OTAs) and selected criteria used for bench-marking the performance of such amplifiers are explained. The chosen performance criteria discussed are Voltage Gain, Gain Bandwidth (GBW), Phase, Phase Margin (PM), Slew Rate (SR) and Power dissipation (PD).

In Chapter 4, we thoroughly present the design procedure of two selected OTAs. We investigate the impact of TID effects on analog circuit performance based on the two operational transconductance amplifiers (OTAs), designed using an Inversion Coefficient (IC) based technique. The first is a current mirror OTA and the second a folded cascode OTA. The comparison is made between the selected performance criteria for each OTA in pre-rad and post-rad conditions under three TID levels (100, 200 and 500 Mrad(SiO_2) for three temperatures (-30, 0 and 25 °). The circuits were designed in Virtuoso ADE by Cadence and simulated with Cadence Spectre simulator.

Finally, in Chapter 5 we conclude with an attempt to explain the performance degradation of the two OTA configurations in terms of model parameter degradation, implemented in the established TID-PDK.

Chapter 2

Dedicated 65 nm CMOS TID-Process Design Kit & Aspects of Implementation

In this chapter we will discuss the procedure followed towards the implementation of a Dedicated 65 nm CMOS TID-Process Design Kit that accounts for Total Ionization Dose phenomena. We will discuss step by step the system integration procedure, together with the functionality and evaluation strategies. Secondly, we will present a popular design methodology based on inversion coefficient (IC) for Analog, Digital and Mixed signal design. Finally, we will discuss the effect of TID on specific, important design parameters, that the aforementioned design methodology exploits. This chapter provides the fundamentals towards TID immune circuits.

2.1 Implementation of a Dedicated 65 nm CMOS TID-Process Design Kit

The Dedicated 65 nm CMOS TID-Process Design Kit is the product of collaboration between Technical University of Crete (TUC) and European Organization for Nuclear Research(CERN). The experiment conducted began with the fabrication of MOSTs in foundry 65nm CMOS Process Design Kit (PDK) and later the irradiation of MOSTs using an X-ray source (up to 500 Mrad(SiO_2) at a high dose rate $\simeq 9\,Mrad\,per\,hour$) under high bias conditions ($|V_{gs}| = |V_{ds}| = 1.2V$) at $-30^o\,C$, $0^o\,C$ and $25^o\,C$. The biasing conditions of the experiment are thought to be the worst case scenario, according to CERN, and especially at $25^o\,C$. Finally, DC measurements were performed after the irradiation of MOSTs at every TID level without any annealing effects. The TID damage effects are treated as ageing effects. The experiment and the measurements took place in CERN, Switzerland and the Dedicated 65 nm CMOS TID-Process Design Kit was developed in TUC, Greece. The TID-PDK is widely used by CERN for the upcoming HL-LHC

upgrade and by more than fifty Institutions and Universities around the world in collaboration with CERN.

The 65nm dedicated CMOS TID-Process Design Kit includes several types of MOST models developed in BSIM4 (version 4.5) or BSIM6. The Design Kit namely includes models for standard V_T NMOS and PMOS, High V_T NMOS and PMOS and Low V_T NMOS and PMOS. [19], [20], [21] It, also, includes models for standard V_T Enclosed-Gate NMOS and PMOS, High V_T Enclosed-Gate NMOS and PMOS and Low V_T Enclosed-Gate NMOS and PMOS. [22], [23] In Figure 2.1 the layout of an Enclosed Gate MOSFET is shown for comparison with the layout of a planar MOSFET.

The parameter extraction procedure was based on the foundry BSIM4 (version 4.5) MOSFET models. The TID models were meant as an expansion of the foundry Design Kit. All models included were developed by the in-house modelling team of Electronics Laboratory in Technical University of Crete.

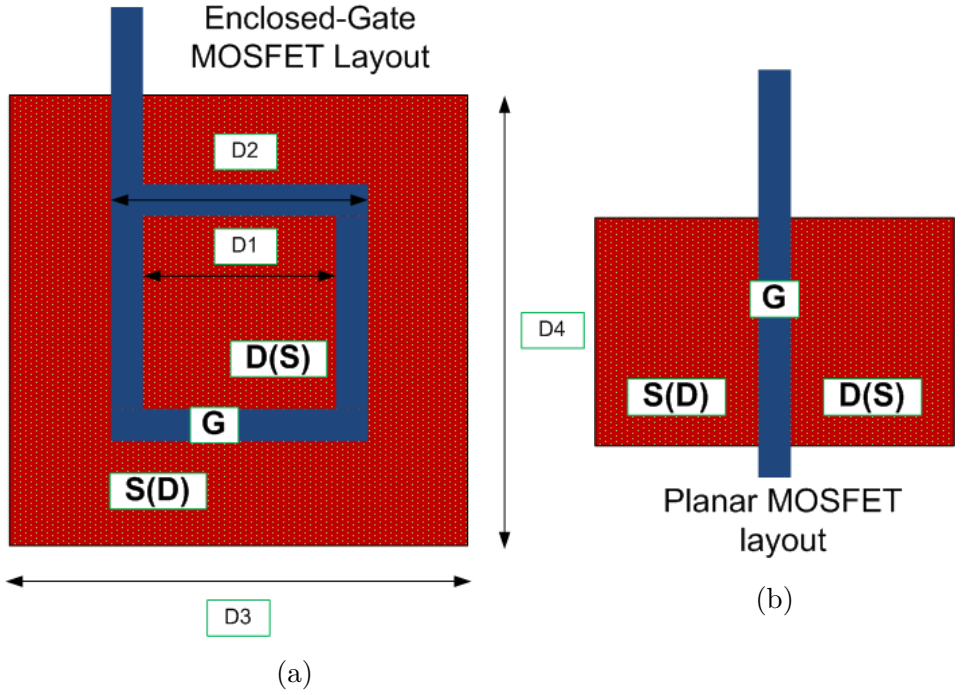


Figure 2.1: (a) Enclosed Gate (EG) MOSFET layout (b) standard (STD) MOSFET layout

The 65nm dedicated CMOS TID-Process Design Kit accounts for three levels of Total Ionizing Dose, 100Mrad(SiO_2), 200Mrad(SiO_2) and 500Mrad(SiO_2). For every TID level three separate models were developed for three specific temperatures, namely $-30^o\,C$, $0^o\,C$ and $25^o\,C$. For each category of MOSTs, i.e. standard V_T NMOS and PMOS, nine separate models were extracted. Following the parameter extraction procedure, each model, i.e. 100Mrad(SiO_2) model for $-30^o\,C$ was transferred to spectre language file format (.scs). The implementation of the models extends to Noise and DC mismatch. All functionality tests and evaluation of the new models took place in Virtuoso by Cadence ADE using the Cadence Spectre Simulator.

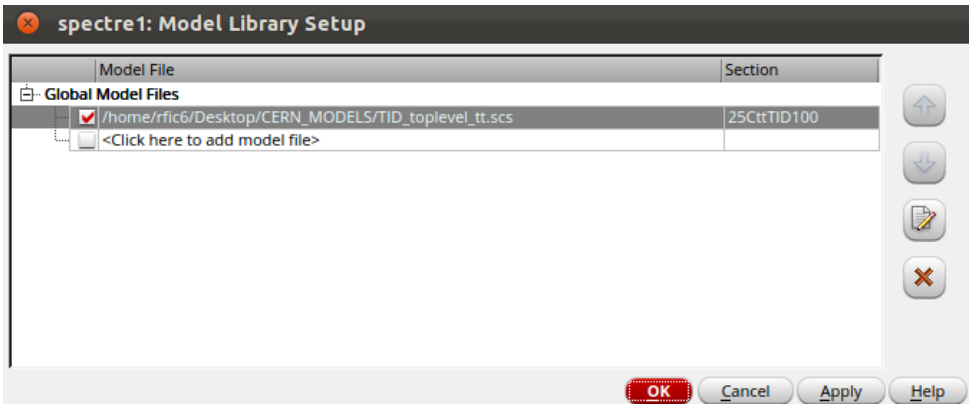


Figure 2.2: Spectre Model Library Setup Menu.

It is common knowledge among IC designers' community that when a library component is placed in an active design, Spectre simulator loads the default models for this component upon simulation. The Dedicated 65nm CMOS TID-Process Design Kit needs to be declared manually upon simulation. However, the implementation proposed by TUC gives the advantage of testing pre-existing circuit designs in 65nm foundry Design Kit under ultra high TID. This was made possible by maintaining the section names in new .scs files the same as in foundry Design Kit. This means that each foundry Design Kit component can be simulated unchanged throughout a TID effects study in terms of component symbols. To further enhance the convenience of designers toplevel.scs files were produced. Each file contains the nine models for a certain type of device, which were mentioned previously, and all other sections from foundry models needed to preserve functionality. In Figure 2.2 the declaration of a TID model is shown, where TID_toplevel_tt.scs is the toplevel.scs that corresponds to standard V_T NMOS and PMOS model cards. In Section drop down menu, the designer chooses the desired model in terms of temperature and TID level. At this point we must denote that the simulation temperature should be changed manually according to the chosen model.

In the case of Enclosed Gate MOSTs, a foundry model did not exist neither for standard V_T, High V_T nor Low V_T Enclosed-Gate MOSTs. All models, including ones for the pre-irradiation case (PreRad), were ab initio developed in TUC. The models are scalable and they are developed in the BSIM6 model, in contrast with the BSIM4 models that are binned models.

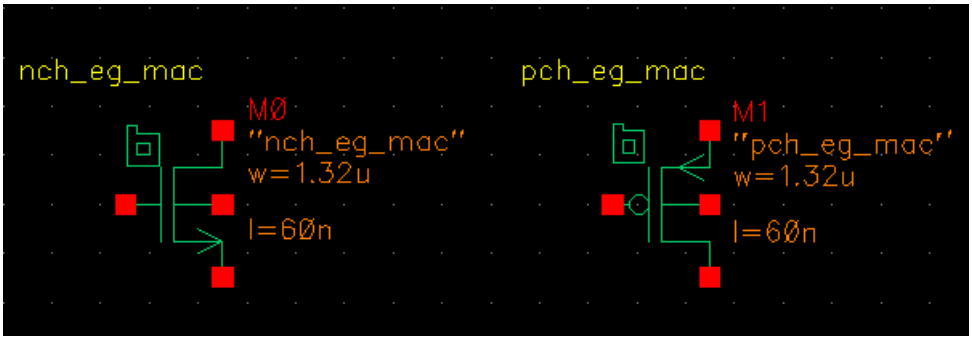


Figure 2.3: Enclosed Gate N- and PMOST Component Symbols.

Another issue to address was the absence of component symbols for the Enclosed Gate MOSTs. New symbols were designed for incorporation in the foundry PDK and they are presented in Figure 2.3. To set the component description format (CDF) information for these particular new library components, the CDF editor was used to define all instance parameters for each new symbol and to connect the models developed with the symbols. Default values were given to all parameters and new SKILL callback functions have been developed to perform instance parameter checking and automated width calculation from channel length, which is proposed to the user. This happens because we use planar MOSFET's model, BSIM6, to model Enclosed Gate MOSTs. In order to do that efficiently, we need to use a width that it is electrically equivalent to Enclosed Gate MOSFET's dimensions which are interdependent. [26] The callbacks were incorporated in the initialization file (.il) of the $65\,nm$ foundry PDK. This was mandatory due to fact that SKILL callback function foundry PDK files are encrypted, meaning that no changes could be done in any way. In Appendix A, an example of a SKILL callback function used is given for controlling the user-inserted EG width instance value and producing the prompt messages for illegal values.

2.1.1 PDK Evaluation in three steps

The PDK was evaluated in three steps:

Step 1:
DC & CV simulations of NMOSTs & PMOSTs in different temperature and TID levels for various width and channel length dimensions. Our goals were to confirm that the models are fully operational, to determine the compatibility of the new models with the foundry PDK and to investigate for possible discontinuities of the models along the transitions between bins, using parameter extraction methods. Several parameters were extracted such as slope factor (n), threshold voltage (V_{th}), mutual transconductance (g_m), electron mobility (μ) etc. Due to large amounts of data for the parameter extraction procedure, a more efficient solution was introduced, which is the simulation automation via Cadence Ocean scripts. In addition, Spectre Accelerated Parallel Simulator (APS) was used for the parameter extraction procedure, which is suitable for performing simulations demanding faster convergence goals. Appendix B, shows an example of how the parameter extraction procedure took place by presenting the extraction of slope factor for NMOSTs.

Step 2:
Transient simulations using different stage inverter-based ring oscillators (ROs) in order to determine problems that could be caused due to convergence issues from the MOST models. The performance of oscillators under TID is a very important topic as denoted by several publications such as [24], where different technology node designs are compared, including SOI MOSTs

and [25], where two types of ring oscillators are analyzed in terms of TID. A qualitative analysis on the impact of TID, 100Mrad(SiO_2), 200Mrad(SiO_2) and 500Mrad(SiO_2) for $-30^o\,C$, $0^o\,C$ and $25^o\,C$ for two 11-stage ring oscillators is shown in the following Figures. One RO employs standard V_T NMOS and PMOS devices (see Appendix C) and the second employs standard V_T EG NMOS and PMOS devices. Both ROs employ the same narrow-short geometries for NMOS and PMOS, $1.32\,um$ and $2.64\,um$ channel width respectively and channel length equal to $60\,nm$. The dimensions for NMOS devices were chosen based on the narrowest and shortest device available for EG NMOSTs. [26] This choice proves to be very helpful for immediate performance comparison between the two different layout schemes.

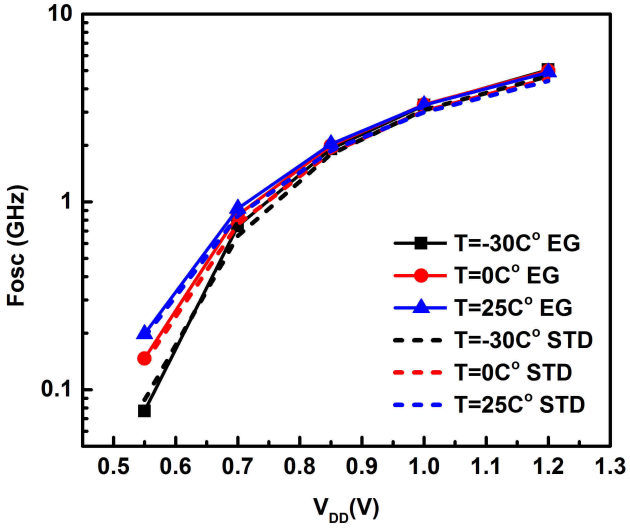
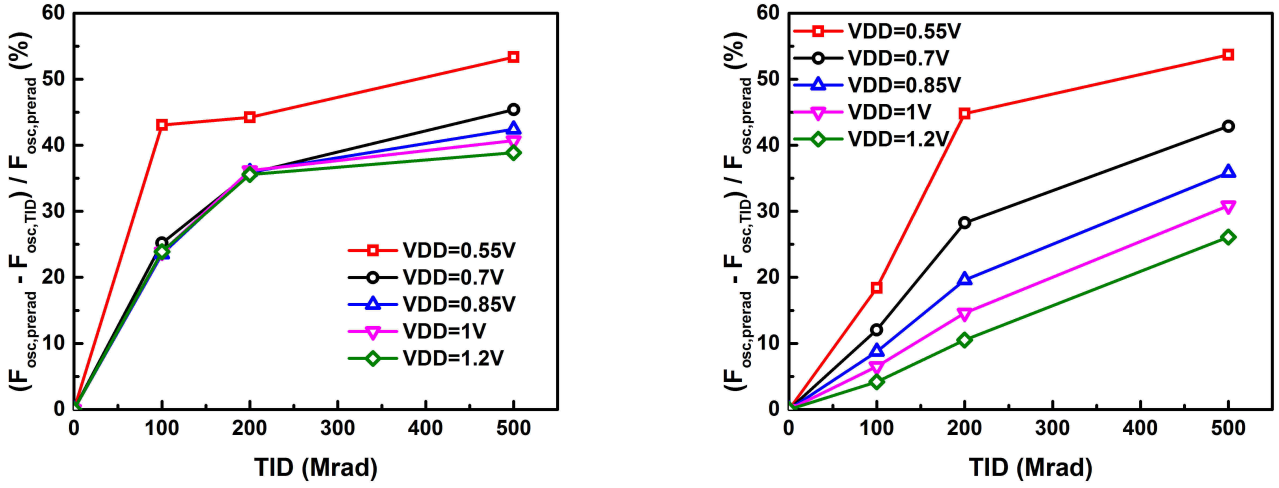
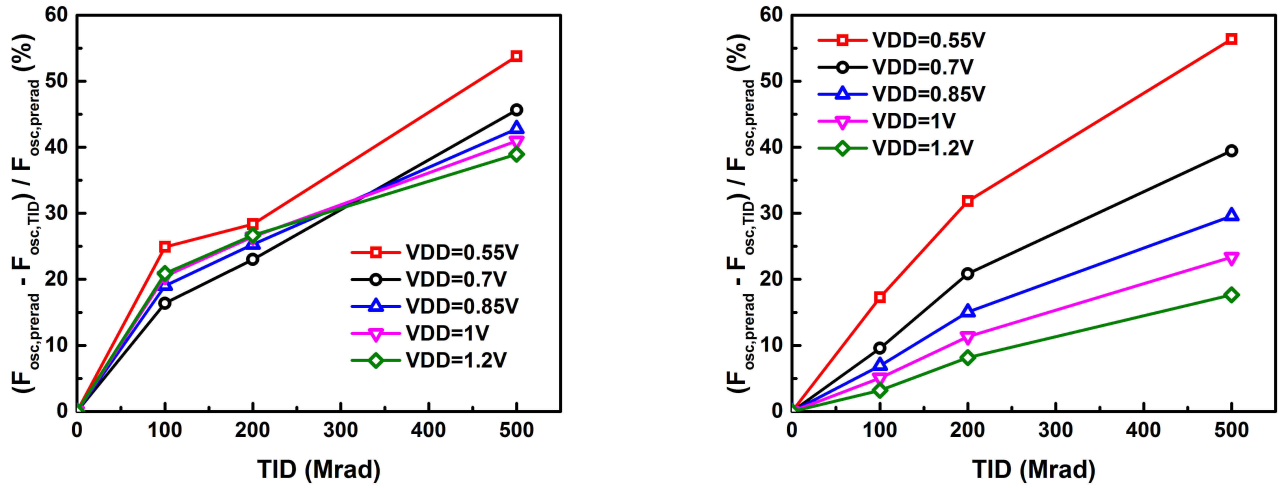


Figure 2.4: PreRad F_{OSC} versus V_{DD} for STD and EG layout STD V_T MOSTs.



(a) (b)

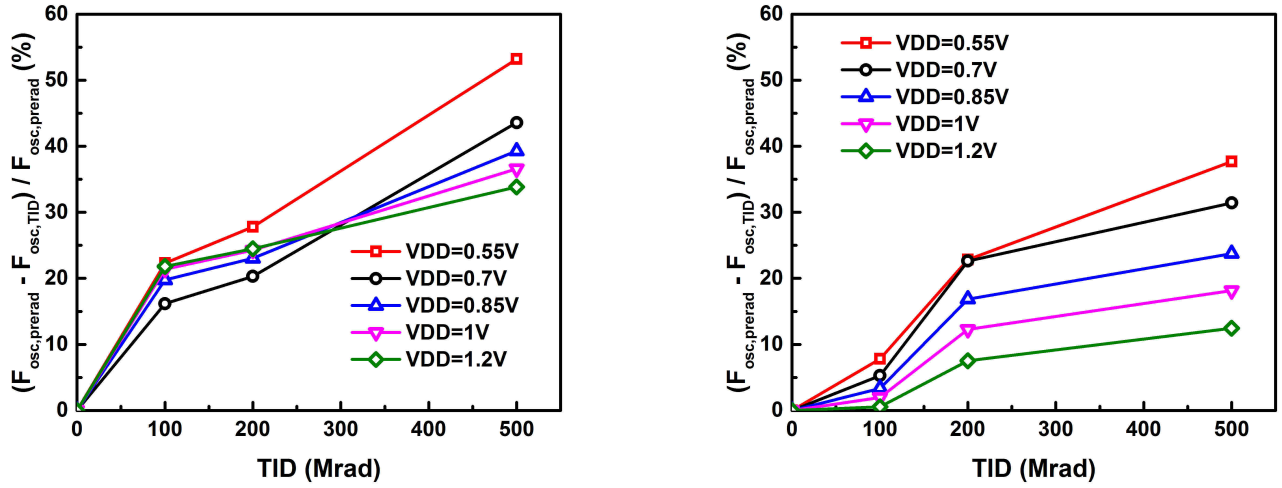
Figure 2.5: Deviation of oscillation frequency from PreRad versus TID Doses for different bias conditions ($V_{DD} = 0.55, 0.7, 0.85, 1, 1.2V$) for STD (a) and EG (b) layout MOSTs for $T = 25^oC$.



(a) (b)

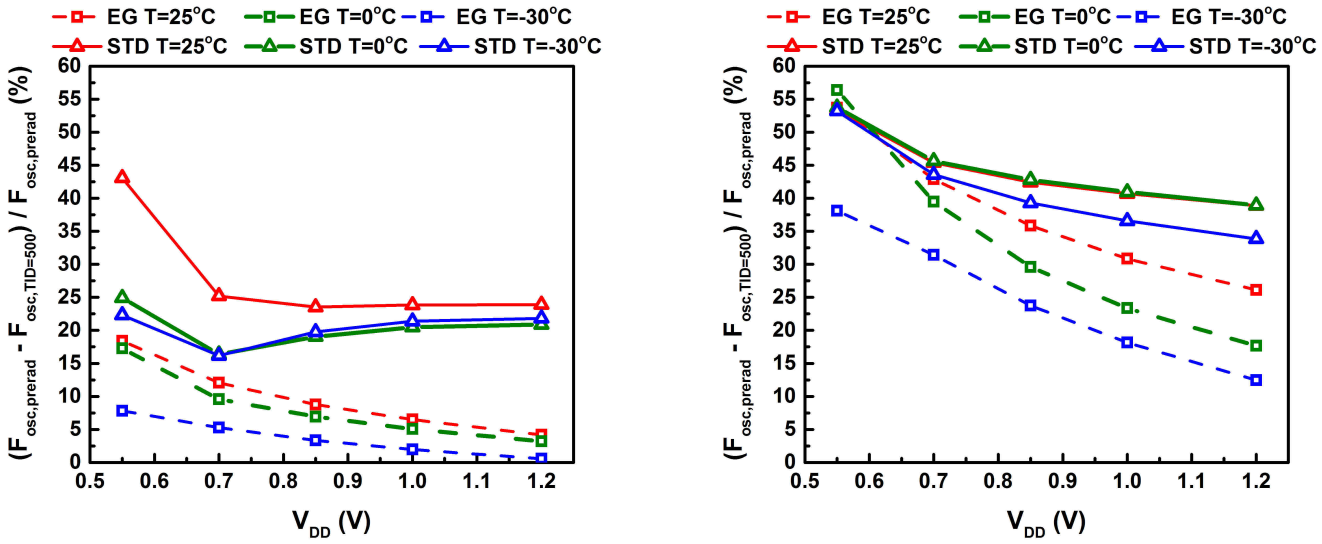
Figure 2.6: Deviation of oscillation frequency from PreRad versus TID levels for different bias conditions ($V_{DD} = 0.55, 0.7, 0.85, 1, 1.2V$) for (a) STD and (b) EG layout MOSTs for $T = 0^oC$.

In Figure 2.4 the oscillation frequency (F_{OSC}) is demonstrated versus different supply voltages for PreRad conditions for all temperatures, for STD and EG layout MOSTs. In the whole range of supply voltages the oscillation frequency decreases as temperature drops. Both types of MOSTs exhibit similar oscillation frequencies. For supply voltages greater than $0.7\,V$ the oscillation frequency is linearly dependent on V_{DD}.



(a) (b)

Figure 2.7: Deviation of oscillation frequency from PreRad versus TID Doses for different bias conditions ($V_{DD} = 0.55, 0.7, 0.85, 1, 1.2V$) for (a) STD and (b) EG layout MOSTs for $T = -30^oC$.



(a) (b)

Figure 2.8: Deviation of oscillation frequency from prerad versus V_{DD} for STD and EG layout MOSTs under different temperature conditions ($T = -30, 0, 25^oC$) for (a) TID= 100 Mrad(SiO_2) and (b) TID= 500 Mrad(SiO_2).

The percentile deviation of oscillation frequency, $(F_{osc,TID} - F_{osc,prerad})/F_{osc,prerad}$, from PreRad for different supply voltages and temperatures versus TID are presented in Figure 2.7, 2.8 and 2.7. For all supply voltages, as TID increases, the deviation increases reaching more than 50% for TID= 500 Mrad(SiO_2) and VDD= 0.55 V. For EG layout MOSTs the deviation of F_{osc} systematically decreases as V_{DD} increases.

In Figure 2.8, the deviation of oscillation frequency versus V_{DD} for different temperatures and device layout for TID= 100 Mrad(SiO_2) and 500 Mrad(SiO_2) is presented. In STD devices, the deviation for TID= 500 Mrad(SiO_2) decreases as V_{DD} increases. On the other hand, the deviation for TID= 100 Mrad(SiO_2), converges to approximately 25 % as V_{DD} increases, after a decrease, especially in low temperatures. For TID= 500 Mrad(SiO_2), STD and EG devices for temperatures above 0^oC demonstrate a deviation near 55 %. The rate of decrease with V_{DD} is quite rapid for EG. In STD devices the deviation does not drop more than 35 % for $T = -30^oC$, where for EG devices, the deviation in the same conditions is slightly more than 10 %.

Step 3:

AC, DC & Transient simulation of OTAs in order to further evaluate models' performance and investigate OTA behavior in different Temperatures and TID levels. Operational Transconductance Amplifier design, which is the third step, is the main subject on this MSc Thesis that will be thoroughly investigated in following Chapters.

2.2 Inversion Coefficient Design Methodology

Inversion Coefficient Design Methodology is a methodology employing a design-oriented parameter extraction procedure for critical analog design parameters using the inversion coefficient (IC). Transistor operation is divided into three regions, namely weak, moderate and strong inversion, as defined in equation 2.1. The IC based design technique is thoroughly explained and used in [27], [28] and [29].

$$IC = \frac{ID}{I_o \frac{W}{L}} \begin{cases} IC < 0.1 & \text{Weak Inversion} \\ 0.1 \leq IC \leq 10 & \text{Moderate Inversion} \\ IC > 10 & \text{Strong Inversion} \end{cases} \tag{2.1}$$

From equation 2.1 there are three main observations:

• In case of IC increase, while drain current and channel length are fixed, ratio W/L, width and gate oxide capacitance must drop inversely.

• In case of channel length increase, while drain current and IC are fixed, width must increase directly to keep ratio W/L constant. So, gate oxide capacitance increases.

• In case of drain current increase, while maintaining IC and channel length fixed, ratio W/L, width, and gate oxide capacitance all increase directly with drain current.

The IC methodology in [29] aids in selecting the appropriate drain current, IC and channel length for optimal trade offs in transconductance efficiency, drain-source resistance, gain, bandwidth, thermal and flicker noise, mismatch and saturation voltage. In addition, this methodology can be used from weak to strong inversion, producing accurate results.

The most important functions used in IC based design methodology are transconductance efficiency, intrinsic gain and saturation voltage.

Transconductance efficiency can be calculated as follows:

$$\frac{g_m}{I_D} = \frac{G(IC)}{n\,U_T} \tag{2.2}$$

where $G(IC) = \frac{1}{1/2+\sqrt{1/4+IC}}$, n is slope factor and $U_T = \frac{kT}{q}$ is thermal voltage, where k is Boltzmann's constant, T is the temperature in $Kelvin$ and q is the elementary charge.

Transconductance efficiency is a very critical metric, which defines the current consumption and power dissipation in case of the amplifier design. A higher value is a better choice for every design in terms of current consumption and power dissipation.

Intrinsic gain can be expressed in terms of IC as follows:

$$A_v = \frac{g_m}{g_{ds}} = \frac{g_m}{I_D}\frac{I_D}{g_{ds}} = \frac{G(IC)}{n\,U_T}\,V_A \simeq \frac{1}{\eta} \tag{2.3}$$

where g_m is mutual transconductance, I_D is drain current, g_{ds} is drain source transconductance, n is the slope factor, U_T is the thermal voltage, V_A is the Early voltage and η is the DIBL factor. Intrinsic gain is the maximum voltage gain provided by a single transistor.

Saturation voltage can be expressed, also, in terms of IC as follows:

$$V_{DS,sat} = 2\,U_T\sqrt{1/4 + IC} + 3\,U_T \tag{2.4}$$

where $U_T = \frac{k\,T}{q}$ is the thermal voltage, k is Boltzmann's constant, T is the temperature in $Kelvin$ and q is elementary charge.
Saturation voltage is very useful in headroom allocation and is indicative of available output voltage swing.

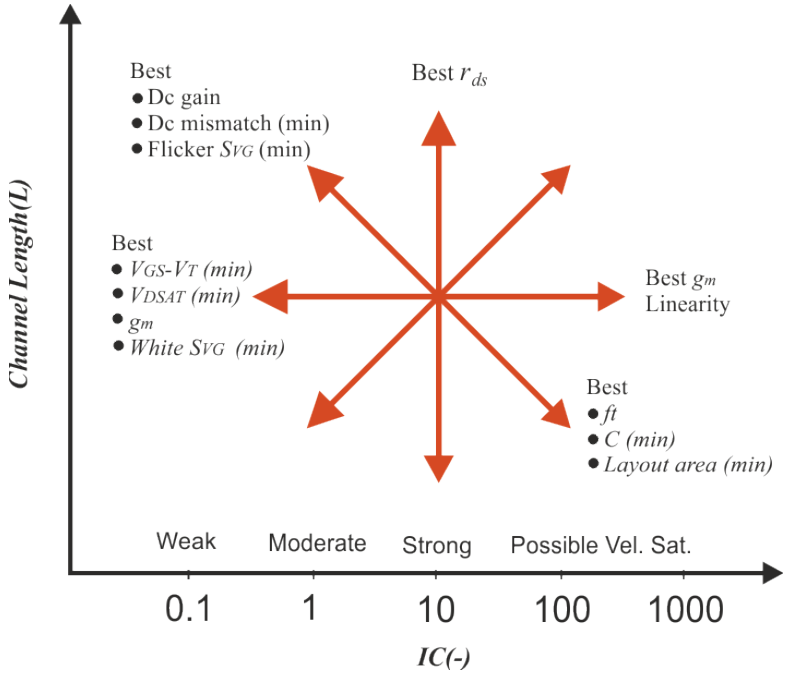


Figure 2.9: MOSFET operation plane.

This methodology takes into consideration that each MOSFET that operates in saturation, operates with a certain drain current, IC and certain channel length. For a fixed drain current, the selection of an IC and a certain channel length pinpoints a position on the MOSFET operation plane that is depicted for a fixed drain current in Figure 2.9. Operating in weak inversion results in high transconductance, low thermal gate referred noise, low saturation voltage. These trade offs come together with large device dimensions. Operating in strong inversion results in high transconductance linearity, low drain referred thermal noise that comes with small dimension devices. On one hand, operating at low inversion levels and long channel devices results in optimal DC mismatch, low flicker noise with large W/L ratios. On the other

hand, operating at high inversion levels and short channel lengths results in high bandwidth, low capacitances, small layout area with small W/L ratios. [29] Moderate inversion is suitable for low voltage, low power design allowing a relatively adequate bandwidth. Width is not discussed but is implicitly involved and easily calculated.

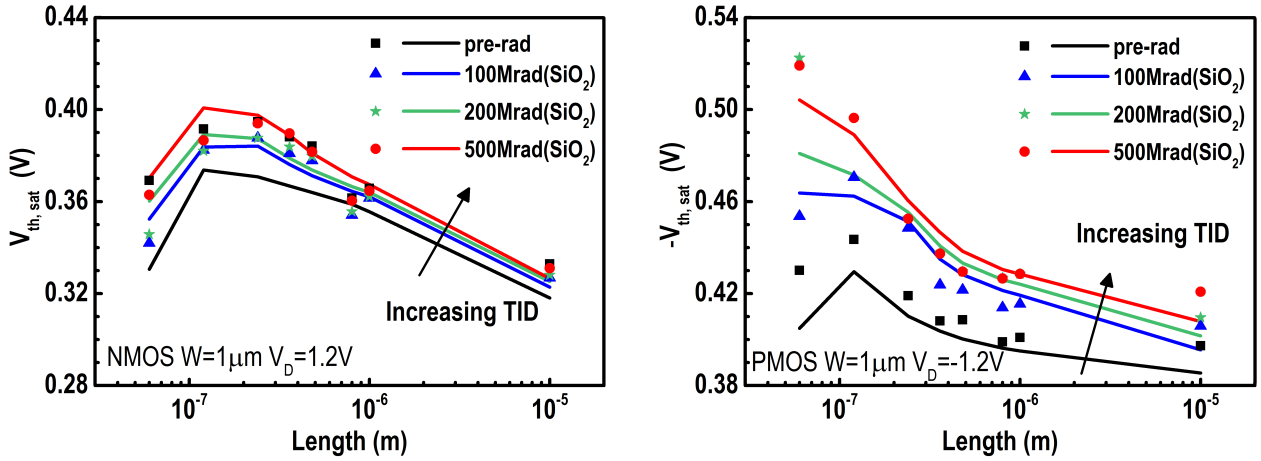
These performance trade offs should be considered in every design procedure. By using the IC based design methodology, design time is reduced by eliminating the otherwise iterative sizing process and moreover DC mismatch is included. The usefulness of the methodology is the categorization of device operation characteristics and the straightforward mathematical approach.

2.3 Analog Design Parameter Scaling For TID levels

In this section we will discuss the evolution of analog design parameters calculated with the available TID level models for $25^o\,C$. It is important to study these parameters because they are essential for the application of the IC based methodology explained in the previous section.

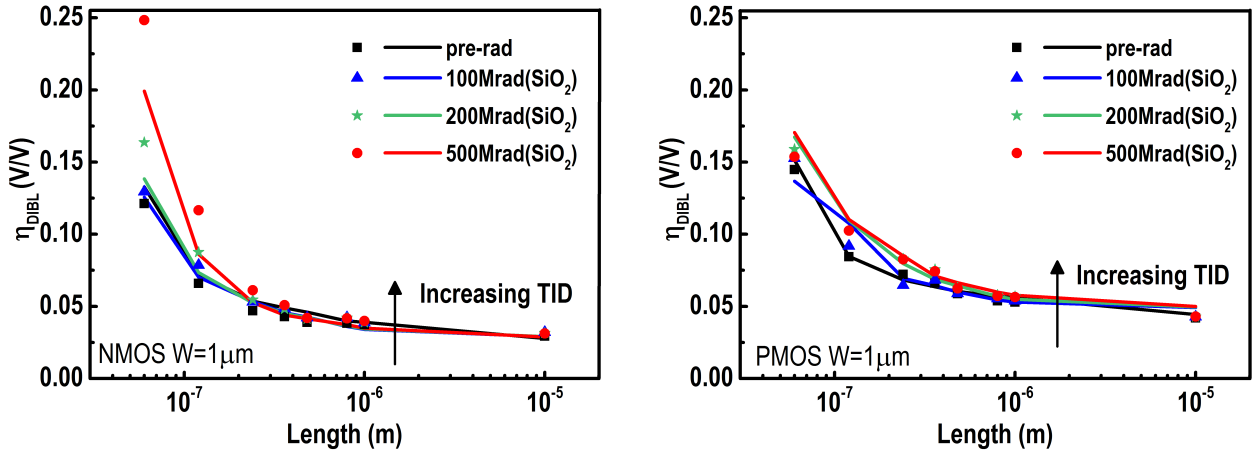
The scaling of analog design parameters such as threshold voltage V_{th}, slope factor n, Drain Induced Barrier Lowering (DIBL) factor η, Early voltage V_A and technology current I_o versus the channel length under different TID conditions is demonstrated in the following Figures for both NMOS and PMOS devices, for $Width = 1\,um$ at 25°.

In Figure 2.10a and 2.10b threshold voltage scaling is shown for NMOS and PMOS devices, respectively. Threshold voltage is extracted using a constant current criterion $I_{(T,N)} = 100\,nA\,(W/L)$ for NMOS devices and $I_{(T,P)} = -25\,nA(W/L)$. From both Figures we can observe that in narrower channel length transistors V_{th} variations are immense. This phenomenon is more pronounced for PMOS devices that exhibit grave variations with TID effects throughout the range of lengths shown. The increase of V_{th} with TID in short channel PMOS devices is more pronounced.



(a) (b)

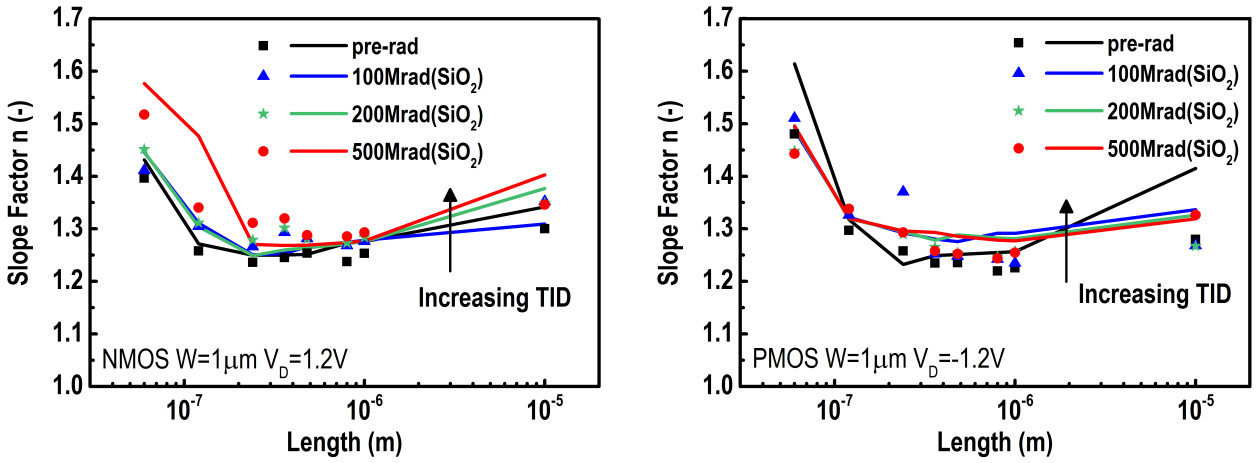
Figure 2.10: Scaling of threshold voltage V_{th} (a) NMOS (b) PMOS with $W = 1\,um$ at $25^o\,C$. [30]



(a) (b)

Figure 2.11: Scaling of DIBL factor η (a) NMOS (b) PMOS with $W = 1\,um$ at $25^o\,C$. [30]

In Figure 2.11a and 2.11b DIBL factor scaling is shown for NMOS and PMOS devices, respectively. DIBL factor is extracted with equation $\eta = (-\delta V_T)/(\delta V_{DS})$. For both Figures we could say that DIBL factor increases due to TID effects but it shows limited variation. The increase is more pronounced for short length NMOS devices.

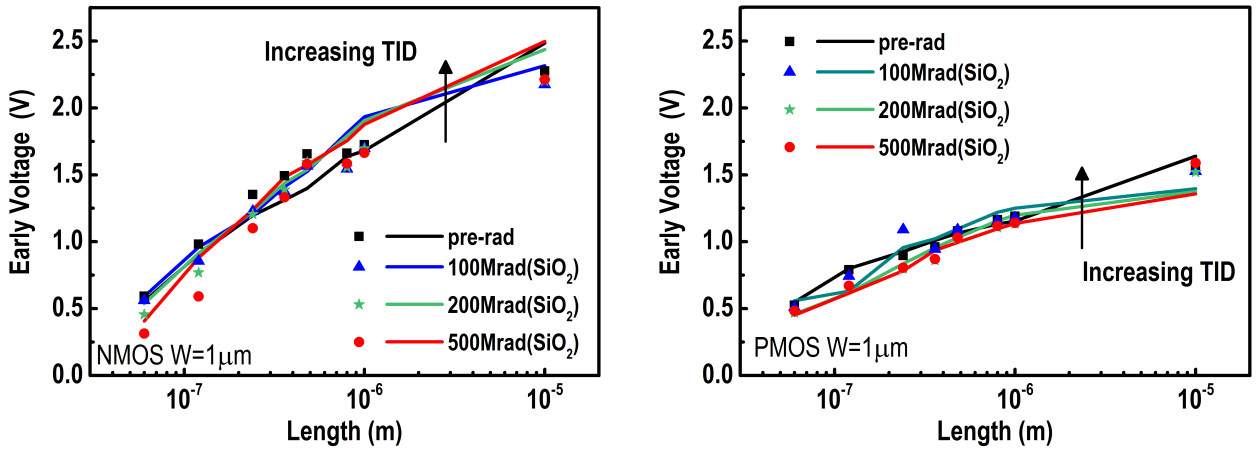


(a) (b)

Figure 2.12: Scaling of slope factor (a) NMOS (b) PMOS with $W = 1\,um$ at $25^o\,C$. [30]

In Figure 2.12a and 2.12b slope factor scaling is shown for NMOS and PMOS devices, respectively. Slope factor is calculated in saturation and weak inversion as $n = I_D/g_m\,U_T$.

In Figure 2.13a and 2.14a Early voltage scaling is shown for NMOS and PMOS devices, respectively. Early voltage is extracted in moderate inversion employing the equation $V_A = n\,U_T/[G(IC)\,\eta]$, where $U_T = \frac{kT}{q}$ is the thermal voltage, $G(IC) = 1/[\sqrt{(0.25 + IC)} + 1/2]$ is the normalized transconductance [31] and η is the DIBL factor. Early voltage shows little variation, as shown in both Figures.

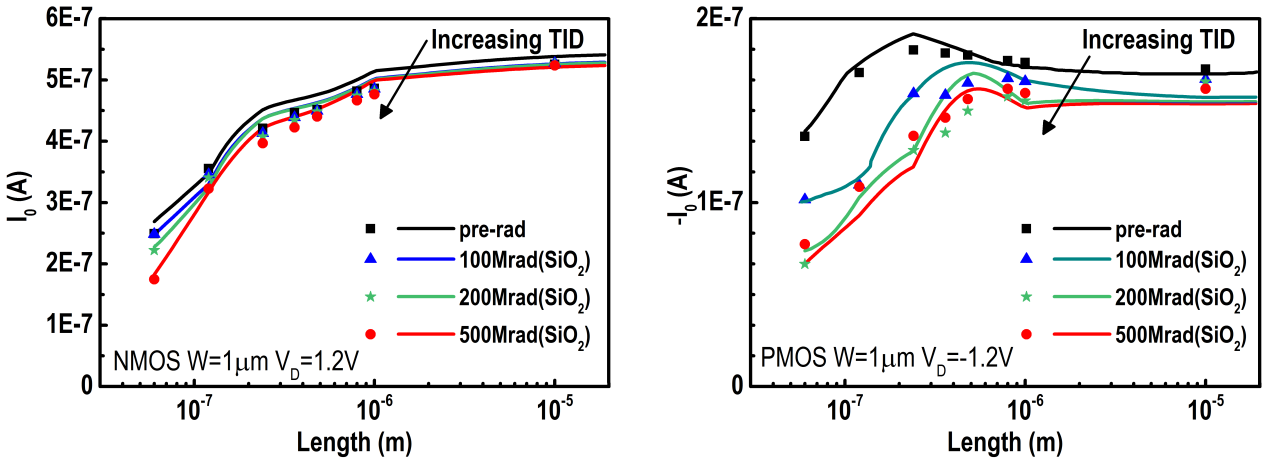


(a) (b)

Figure 2.13: Scaling of Early voltage (a) NMOS (b) PMOS with $W = 1\,um$ at $25^o\,C$. [30]

In Figure 2.14a and 2.14b technology current scaling is shown for NMOS and PMOS devices, respectively. Technology current I_o decreases significantly as the length decreases due to velocity saturation; for PMOS devices, this degradation is grave at high TID. However, channel width dependencies may be equally pronounced, as explained in [21] and [32].The technology current is defined as $I_o = 2\,n\,\mu\,C_{ox}\,U_T^2$, where n is slope factor, μ is carrier mobility, C_{ox} is oxide capacitance and $U_T = \frac{kT}{q}$ is thermal voltage.

At this point it is obvious that together with the guidelines of IC design methodology, the evolution under TID of important design parameters should be studied and accounted for. [33]



(a) (b)

Figure 2.14: Scaling of technology current (a) NMOS (b) PMOS with $W = 1\,um$ at $25^o\,C$. [30]

Chapter 3

Operational Transconductance Amplifiers

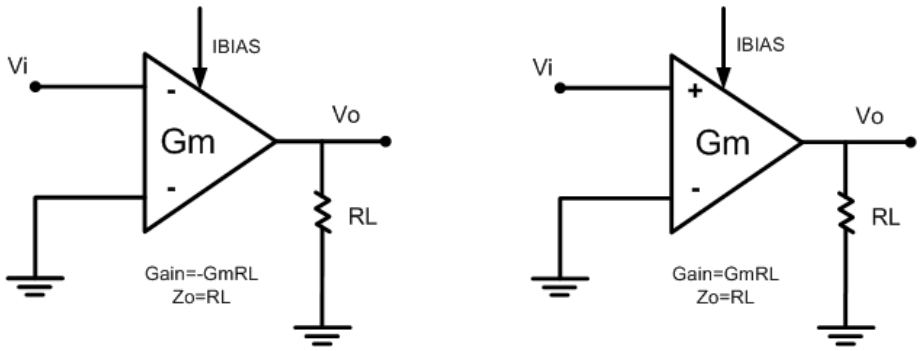
3.1 Operational Transconductance Amplifier Concept

Operational Transconductance Amplifiers ($OTAs$) are analog circuits widely used both in Analog and Mixed-signal applications, as will be discussed in this section. Due to their versatility in terms of design and performance, they became very popular amongst other amplifiers. The traits that make OTAs attractive are their fast speed, compared to their counteparts, the operational amplifiers (op-amps), and their bias-dependent transconductance "tunability". [34] Specifically, an Operational Transconductance Amplifier (OTA) acts as a voltage controlled current source ($VCCS$). An ideal OTA provides infinite bandwidth, large input signals and infinite output impedance. An OTA can be met in single input topologies, but is mostly implemented with differential input structures. In the latter case, the output current of an ideal differential input OTA can be expressed as:

$$i_{out} = (v_1 - v_2)g_m \tag{3.1}$$

where g_m is the transconductance of the input transistors, v_1 and v_2 are the positive and the negative voltage input signals, assuming that the input and output impedances are infinite. Furthermore, it can be implemented with either a single-ended output or a differential output.

An OTA is encountered in many configurations but the basic ones are the inverting and the non-inverting, as seen respectively in Figure 3.1a and Figure 3.1b. It is also used in closed-loop and in open-loop configurations.



(a) inverting configuration (b) non-inverting configuration

Figure 3.1: Symbolic representation of OTA (a) inverting configuration and (b) non-inverting configuration

The "tunability" of an OTA derives from the fact that the transconductance g_m of the input differential pair can be chosen as such to allow tuning of several decades if transistors are operated in weak inversion, as g_m is a function of the amplifier bias current I_{BIAS}. A linear dependence on I_{BIAS} is achieved by operating the input differential pair transistors in weak inversion. Voltage gain is ,also, controlled by transistor dimensions and the bias current I_{BIAS}.

Additionally, an OTA can be considered as a low-pass, first-order filter with a 3_dB cut-off frequency given by the following equation:

$$f_{\_3dB} = \frac{g_m}{2\pi C_L} \tag{3.2}$$

where g_m is the transconductance of the input transistors, C_L the output load capacitance.

When used in open-loop configurations, excess phase ϕ_E is given by the following equation:

$$\phi_E = \frac{\omega}{BW} \tag{3.3}$$

where ω is the angular frequency and BW is the OTA bandwidth. [34]

In reality OTAs are characterised by limited input range, for reasons of linearity, finite bandwidth, finite signal-to-noise ratio and, lastly, finite output impedance. Popular linearisation techniques for OTAs are (a) attenuation (b) non-linear terms cancellation and (c) source degeneration, as mentioned in [34]. These techniques can be performed at the expense of transconductance gain and frequency response. Output impedance can be increased by the use of cascode structures, leading to the decrease of output voltage swing. [35] It is apparent that according to application, a circuit designer faces many challenges and several trade-off choices. All the above, are considered together with the challenges imposed by modern CMOS technologies that require low voltage, low power supply.

Apart from all the challenges and trade offs, OTAs can be used in linear and non-linear systems. In [36], a CMOS highly linear digitally programmable operational transconductance amplifier (DPOTA) in 90 nm is presented. The DPOTA proposed is used for implementing a Fourth-Order Low pass filter for portable biomedical applications. In [37], a linear input range

extension technique is presented for OTAs used in Low-Voltage Gm-C filters (Current mode filters). In [38], they propose an OTA used as the active element for programmable nonlinear continuous-time function synthesis.

Another advantage of the OTAs is that they are suitable for both, low and high frequency applications. In [39], several OTA topologies are proposed for low frequency biomedical applications. They show that OTAs can be used as active filters with very low cut-off frequencies (of the order of a few Hertz). On the other hand, in [40] a feedforward-regulated cascode OTA is reported with a bandwidth of 10 GHz. This is possible due to inherently low internal node impedances that make OTAs relatively wideband. Further minimizing internal node impedances and excess phase can be used for high frequency applications. Internal node impedances together with parasitic capacitances, they can cause non-zero transconductance phase shift, meaning excess phase ϕ_E, especially in closed-loop configurations, which leads to circuit instability.

Because of the aforementioned wide variety of applications, it is mandatory to study the Operational Transconductance Amplifier (OTA) in terms of performance under high Total Ionizing Dose (Mrad(SiO_2)) effects.

3.2 Operational Transconductance Amplifier Performance Criteria

In this section we will discuss the non-ideal characteristics of an OTA and the simulation testbenches used for circuit design evaluation. The non-ideal behavior of OTAs includes finite differential voltage gain, finite unity gain bandwidth, phase margin, slew rate, input DC offset and total input referred noise.

3.2.1 Gain & Gain Bandwidth

Gain and gain bandwidth are two interwoven features of an OTA, as will be discussed in this section.

In an ideal common source (CS) amplifier, Figure 3.2, the transconductance required to achieve a gain bandwidth product (GBP), in Hertz, for a given load capacitance, C_L, can be expressed by the following equation [41]:

$$g_m = 2\,\pi\,\mathrm{GBP}\,C_L \tag{3.4}$$

Assuming that the Early voltage, V_A, is proportional to the transistor channel length, meaning $V_A = V_E\ \ L$, the following equation can be used to determine the absolute value of the intrinsic dc voltage gain:

$$A_o = \frac{g_m}{g_{ds}} = \frac{g_m}{I_D}\,V_E\,L \tag{3.5}$$

where V_E is the Early voltage factor.

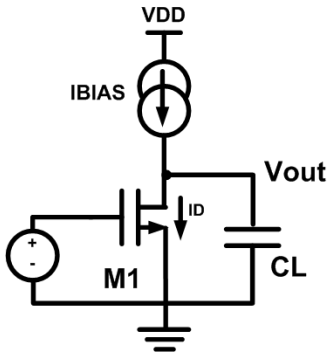


Figure 3.2: Ideal common source amplifier (CS amplifier)

Equation 3.4 can be expressed, also, as a function of drain current I_D. In the case of the ideal CS amplifier I_D equals I_{BIAS}.

$$\text{GBP} = \frac{g_m}{2\pi C_L} \tag{3.6}$$

$$\text{GBP} = \frac{g_m}{I_D}\frac{I_D}{2\pi C_L} \tag{3.7}$$

Considering equations 3.5 and 3.7, a direct connection between Gain Bandwidth Product (GBP) and Gain is evident through the value of g_m/I_D, a useful metric discussed in a previous chapter.

In Figure 3.3, a typical magnitude gain plot of an OTA is shown using both possible numerical representations V/V and dB (decibels). A characteristic feature of OTAs is the single high impedance dominant pole that can, also, be seen in Figure 3.3. The term gain of an OTA refers to the low frequency gain that is limited by the dominant pole. Extending the aforementioned analysis of the ideal common source amplifier to an OTA, thte gain bandwidth product is depicted in Figure 3.3. It is important to stress that the term gain bandwidth is often used to refer to unity gain bandwidth/frequency, which is the bandwidth/frequency where gain is equal to $0\,dB$. On the other hand, the term GBP is used to refer to the product of gain at a given frequency with the given frequency. The choice of frequency is the characteristic that creates the distinction between these terms.

The testbench to simulate the AC behavior of an OTA is presented, in Figure 3.4. Specifically, this testbench is used to simulate the open-loop gain, gain bandwidth and phase margin, as will be discussed in the following section.

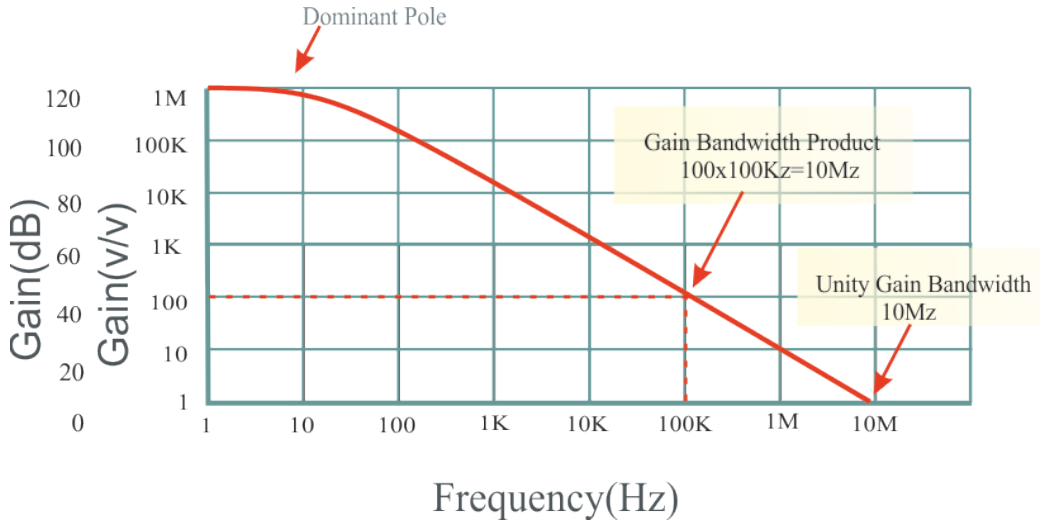


Figure 3.3: Magnitude gain plot.

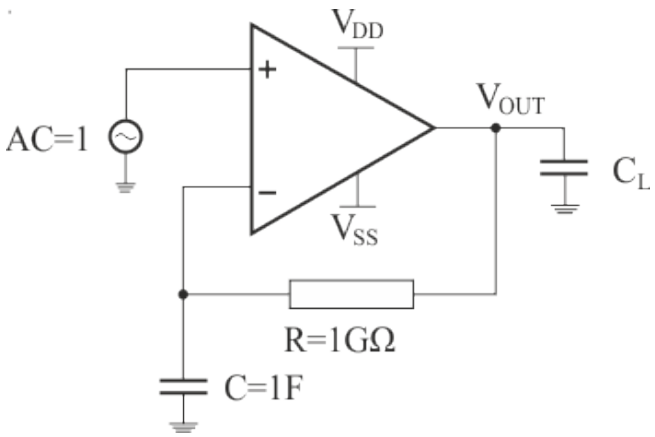


Figure 3.4: Simulation testbench for AC characterization.

3.2.2 Phase Margin

Phase margin (PM) by definition is the change in open-loop phase that causes a closed-loop system to become unstable. In other words, PM is the difference in phase between $-180°$ and the phase at the unity gain frequency (cross over frequency, where gain is 0 dB). So, PM can be expressed as:

$$\text{PM} = 180° + \langle H(j\omega) \tag{3.8}$$

where ω (rad/sec) is the angular cross over frequency.

If the phase $\langle H(j\omega)$ at the frequency where $H(j\omega) = 1$ of is greater than $-180°$, giving a positive PM that ensures the closed-loop system stability. [42] In other words, when the closed-loop gain equals to unity and the phase shift equals to $-180°$ is the fine line between oscillation and stability. In Figure 3.5, the calculation procedure of PM is depicted graphically.

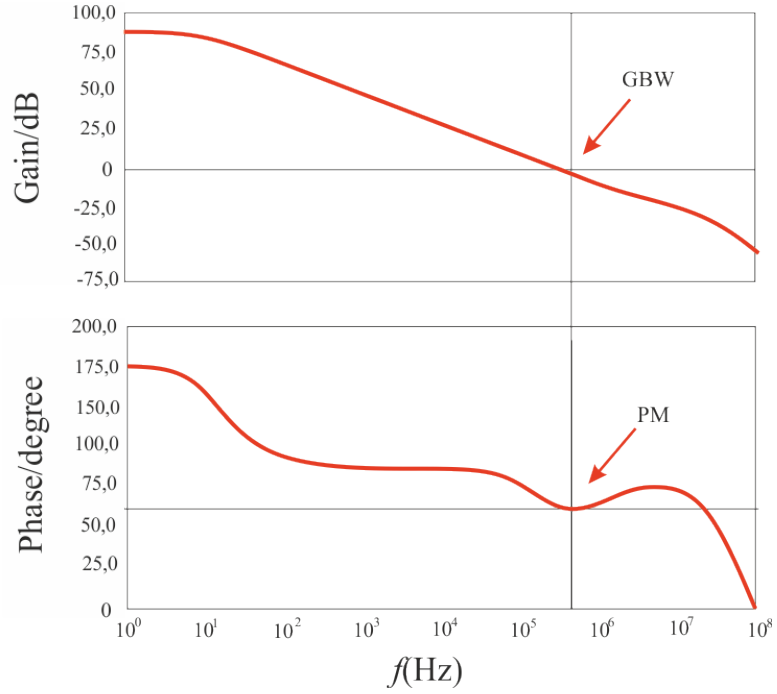


Figure 3.5: Phase Margin Calculation.

In a good OTA design, there should be one dominant pole and the secondary pole should be at a frequency well above the cross over frequency. Phase margin can be considered basically a measure of how the secondary pole can affect the stability of the circuit. An acceptable PM is considered to be 60° in order to account for any possible technology process variations. The higher the PM is, the more stable the circuit/system is. Finally, one of the critical trade offs for PM is the capacitive load, because when the capacitive load increases, PM decreases.

3.2.3 Slew Rate

A critical circuit performance criterion is the slew rate (SR). SR is connected to the speed of a circuit and, by definition, is the maximum rate of the rise/fall of the output voltage of an OTA. If the output voltage of the OTA must change, SR denotes the period of time required for the output voltage to change.

Slew rate performance of the CMOS OTA depends on the value of the bias current I_{BIAS} and the capacitance from the output node to ac ground. In other words, slew rate in the CMOS OTA is determined by the amount of current that can be sourced/sunk into the output capacitance. In order to increase the value of SR, I_{BIAS} should be increased. [43] Slew rate can be expressed with the following equation:

$$SR = \frac{\Delta Vout}{\Delta t} = \frac{I_{BIAS}}{C_L} \tag{3.9}$$

where $Vout$ is the OTA output voltage.

Returning to equation 3.7, we can substitute the second fraction with equation 3.9, as

follows:

$$\text{GBP} \simeq \frac{g_m}{I_D} SR \tag{3.10}$$

Equation 3.10 proves that the g_m/I_D metric equals to the ratio of GBP to SR, which is a very useful mathematical relation for the design of an OTA.

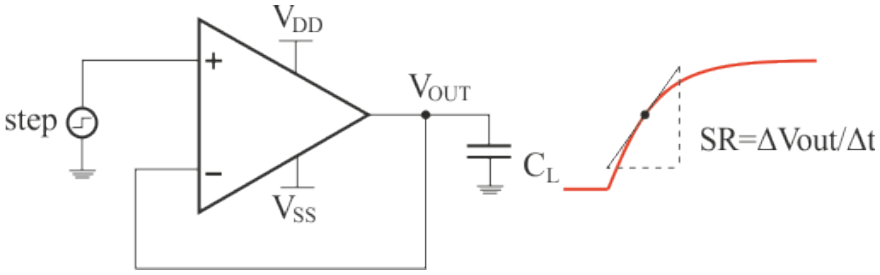


Figure 3.6: Slew Rate testbench schematic

For the simulation setup of SR, the OTA must be converted into a unity gain buffer as depicted in Figure 3.6. The input, as shown, is a pulse with an amplitude i.e. 1 Volt and an appropriately, according to design, chosen period. Slew rate being equal to slope, is measured between 20% and 80% (or 10% and 90%) of the settled output voltage.

3.2.4 Total Input Referred Noise

Noise analysis is a very crucial step in OTA design process, as it is a critical performance criterion in many applications, especially in biomedical applications. Total Input referred Noise is the equivalent noise at the input of an amplifier, expressed in $V/\sqrt{Hz}$ or $Vrms$.

For the design process it is mainly preferred to represent channel noise of a single transistor, as an equivalent noise voltage source being in series with the gate. The other equivalent is a noise current source connected in parallel between drain and source. Consequently, the power spectral density (PSD) of the noise voltage source in series with the gate can be expressed by the following equation:

$$\frac{\overline{vg^2}}{\Delta f} = \frac{\overline{id^2}}{g_m^2 \Delta f} \tag{3.11}$$

where g_m is transistor's mutual conductance.

Keeping the same approach, flicker noise and thermal noise of a single transistor can be expressed, respectively, in equations 3.12 and 3.13 as noise voltage source's components:

$$\frac{\overline{vg^2}}{\Delta f} = \frac{K_F}{WLC'_{ox}} \frac{1}{f} \tag{3.12}$$

where K_F is flicker noise parameter, W is transistor's width, L is transistor's length and C'_{ox} is oxide capacitance per area (F/m^2).

$$\frac{\overline{vg^2}}{\Delta f} = \frac{4kT\gamma}{g_m} \tag{3.13}$$

where k is Boltzmann's constant, T is the absolute temperature in $Kelvin$, γ is the excess noise factor and g_m is transistor's mutual conductance.

In order to calculate the equivalent noise voltage at the input of an OTA, we first need to calculate the noise current at the output (AC ground) by adding the contributions of the uncorrelated currents. Small-signal analysis leads us to the following equation for the PSD of the output noise current:

$$\frac{\overline{i_{no}^2}}{\Delta f} = \frac{1}{\Delta f} \sum_{n=1}^{N} \overline{i_{ni}^2} \tag{3.14}$$

Equation 3.14 holds under the assumption that the output conductances (g_{ds}) of all transistors are considerably lower than the source transconductances (g_{ms}). With this simplification, the magnitudes of the current transfer functions of the channel noise currents to the output are slightly smaller than unity. To refer to the input, we assume that the noise at the input can be represented by the equivalent input noise voltage, for which the PSD is expressed by the following equation:

$$\frac{\overline{i_{ni}^2}}{\Delta f} = \frac{1}{\Delta f} \frac{1}{g_m^2} \sum_{n=1}^{N} \overline{i_{ni}^2} \tag{3.15}$$

where g_m is the input transistor's mutual transconductance.

Each channel noise current should be replaced with its expression associated with both thermal and flicker noise components, presented respectively in equation 3.12 and equation 3.13. [41] [44]

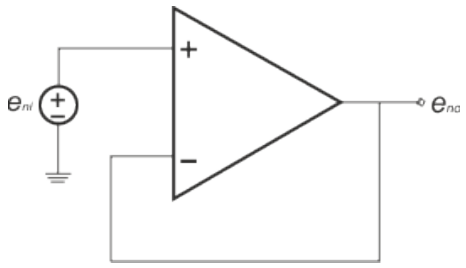


Figure 3.7: Total Input Referred Noise testbench.

Figure 3.7, the circuit configuration for noise simulations in presented. Once more, the given circuit should be converted to unity gain buffer to perform the noise analysis.

Chapter 4

Design of CMOS Operational Transconductance Amplifiers

In this chapter, we will discuss the design procedure followed for both operational transconductance amplifiers (OTAs) under investigation. The two OTAs will be referenced as Current mirror OTA and Folded cascode OTA. The topologies for the Current mirror OTA and the Folded Cascode OTA are depicted, respectively, in Figure 4.1 and Figure 4.19. Both OTAs were implemented in Cadence Virtuoso ADE in 65 nm CMOS technology. The inversion coefficient design technique is used, in which the MOSFET operation in saturation mode is divided into weak, moderate and strong inversion regions as defined in previous chapter. They were designed with a similar sizing strategy, adapted to the 65 nm CMOS technology that calls for low voltage supply and low power consumption. Supply voltages for either designs are VDD=1.2 V and VSS=0 V.

In the following section, we will discuss how the IC based design technique is employed, combined with Total Ionizing Dose (TID) effects integrated in the 65nm TID-PDK. Simulation results will be presented addressing the impact of high TID effects on selected OTA performance criteria.

4.1 Current mirror OTA

For the Current Mirror OTA, the biasing stage consists of a 1:1 NMOS current mirror formed by transistor instances M5 and M6. The gain stage includes an NMOS differential pair, comprised of transistor instances M1 and M2 of equal sizing. Two 1:1 PMOS current mirrors of equal sizing (M7-M8, M9-M10) function as active loads for the differential pair. Finally, a 1:1 NMOS current mirror (M3-M4) is present in the output stage of the amplifier. All supply voltages, VDD and VSS, were kept constant and the reference current provided to the biasing stage is, also, kept constant with a value of I_{BIAS}= 50 uA.

The reference current provided to the biasing stage is mirrored through transistors M5-

M6. Respectively, transistor M6 provides to the differential pair biasing current equal to the reference current. The output drain current of the differential pair transistors is equal to half of the reference current and each current is mirrored through the PMOS current mirrors (M7-M8, M9-M10). The output of current mirror M7-M8 is directly connected to the output stage of the amplifier. The output of the current mirror M9-M10 is passed to the output stage via the NMOS current mirror M3-M4, creating a complementary signal path.

The Current Mirror OTA (CM OTA) was not designed in the original 65nm Design Kit that doesn't account for any TID effects, instead it was directly designed with the integrated model for 100 Mrad(SiO_2) and the initial design/simulation temperature was 25°.

For the CM OTA the power dissipation was chosen to be 180 uW (150 uA for a 1.2 voltage supply) and the corresponding current for each branch is shown in Figure 4.1. The OTA was, also, designed to meet certain specifications. The output load capacitor (C_L) was chosen with a value of 400 fF, low frequency gain was chosen to be 30 dB, unity gain bandwidth was chosen to be greater than 150 MHz, slew rate was chosen to be greater than 100 $V/usec$, input noise was chosen to be lower than 20 uV/$\sqrt{Hz}$ at 1 Hz.

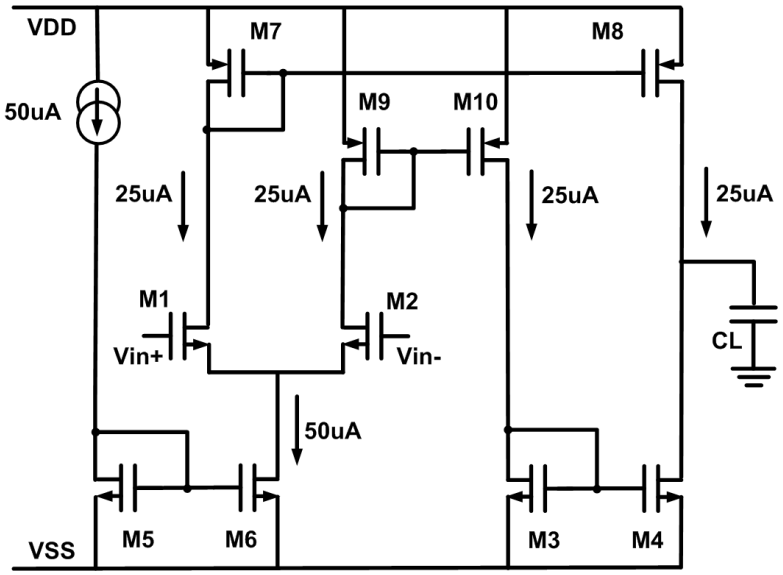


Figure 4.1: Current Mirror OTA.

The technology current for the the model version of 100 Mrad(SiO_2) at 25°C is $I_{o,n} = 250\,nA$ for nmos devices and $I_{o,p} = 100\,nA$ for pmos devices.

First step in the design process was to size the 1:1 input current mirror used for the CM OTA input biasing. The nmos current mirror is not in the signal path, so the only consideration was to operate it in moderate inversion for a low $V_{DS,sat}$, meaning a low headroom requirement. The dimensions were chosen, also, to account for mismatch effects. The two transistors were sized to have an $IC = 3.3$, which is in moderate inversion, and leads us to $Width = 60\,um$ for the chosen $Length = 1\,um$. This current mirror provides additional stability to the input differential pair. This is because the selected dimensions are such that would alleviate any biasing instabilities caused by the current mirror design, due to process and mismatch variations

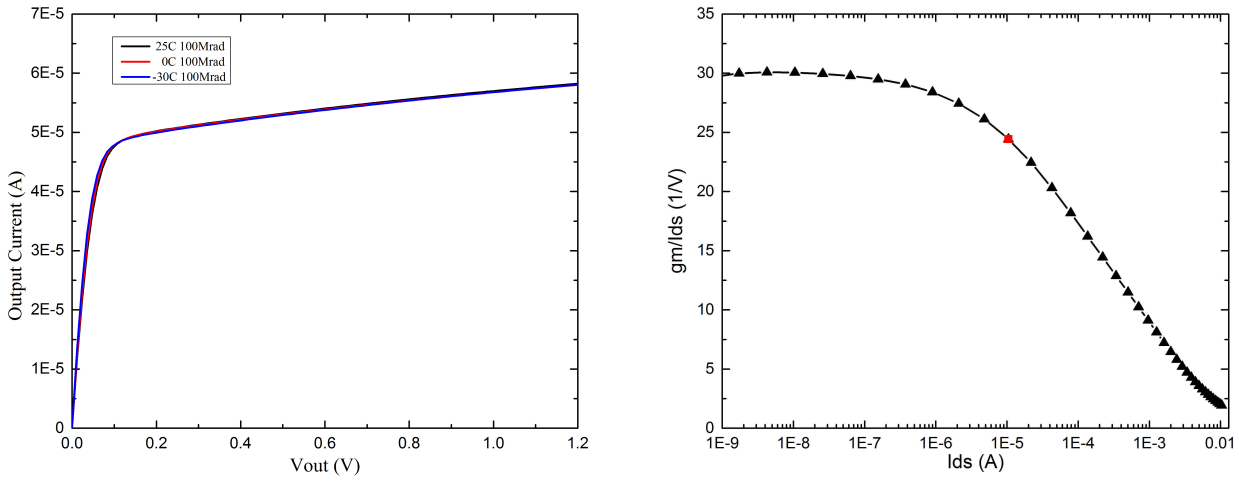
but, most importantly, from any changes due to TID effects, that are detrimental in smaller dimensions. In Figure 4.2a, the output response of the current mirror in question is presented. The output conductance exceeds the expected one for a wide-long device. There are two possible causes for the positive slope of the output current, one is the overestimation of short channel effect model parameters and the other is the overestimation of drain induced threshold shift (DITS) model parameters, both were inherited from the original design kit. The same behavior was observed, also, in longer devices. Transistors M5-M6 contribute negligibly to the output noise current, since they generate a common-mode current.

For the nmos input differential pair, an $IC = 0.4$ is chosen that, places them in moderate inversion operation. This choice leads to $Width = 30\,um$, given $Length = 120\,nm$. Consequently, the corresponding mutual conductance is equal to $500\,uS$. At this point, we can theoretically calculate Slew Rate and Unity Gain Bandwidth using, respectively, equations 3.9 and 3.10. The equations' results are $UGB \simeq 199\,MHz$ and $SR \simeq 125\,V/usec$, which are acceptable according to the specifications. In Figure 4.2b, the extraction of metric g_m/I_{ds} for the transistor dimensions mentioned is presented for $V_{ds} = 1.2\,V$.

For the pmos current mirrors, that are active loads for the differential pair, an $IC = 18.75$ was chosen. This choice leads to $Width = 2\,um$, given $Length = 150\,nm$. To account for mismatch in such dimensions, strong inversion was used for better matching. The current mirrors are responsible for the secondary pole of the OTA, and their f_{-3dB} frequency can be calculated by the following equation:

$$f_{-3dB} = \frac{g_{m,7}}{2\pi(2C_{gs,7} + 2C_{gb,7} + C_{db,1} + C_{db,7})} \tag{4.1}$$

where $g_{m,7}$ is the transconductance of the M7 pmos mirror input device, $C_{db,1}$ is the drain–body capacitance of M1 connected to M7, and $C_{db,7}$ is the drain–body capacitance of M7. $C_{gs,7}$=$C_{gs,8}$ and $C_{gb,7}$=$C_{gb,8}$ are the gate–source and gate–body capacitances of M7 and the output device M8. [27], [28] Employing equation 4.1 for the chosen pmos dimensions, we get a pole at $\simeq 170\,MHz$. The dominant pole is placed at $\simeq 4\,MHz$. The distance between the dominant pole and the secondary pole is significant and so a competent phase margin is achieved ($\simeq 82°$).



(a) (b)

Figure 4.2: Design process (a) current mirror output current vs output voltage (b) g_m/I_{ds} vs I_{ds} of input devices for $V_{ds} = 1.2\,V$.

The final structure to size is the output nmos current mirror (M3-M4). An $IC = 16.75$ is chosen that places them in strong inversion operation. The dimensions deriving are $Width = 2.4\,um$ for a given $Length = 400\,nm$. To account for mismatch in such dimensions, strong inversion was used as appropriate region of operation.

Type	*Instance*	*Width*	*Length*	*IC*
Nmos	M1=M2	30 um	120 nm	0.4
Nmos	M3=M4	2.4 um	400 nm	16.75
Nmos	M5=M6	60 um	1 um	3.3
Pmos	M7=M8	2 um	150 nm	18.75
Pmos	M9=M10	2 um	150 nm	18.75

Table 4.1: Current mirror OTA sizing.

In table 4.1, all device dimensions are listed together with the Inversion Coefficient chosen for the CM OTA design using model for 100 Mrad(SiO_2) at $25°\,C$.

Considering, device dimensions we can calculate the gain (V/V) of the CM OTA using the following equation that corresponds to topology:

$$A_V = \frac{g_{m,1}}{g_{ds,4} + g_{ds,8}} \tag{4.2}$$

where $g_{ds,4}$ is the drain output transconductance of output nmos transistor M4 and $g_{ds,8}$ is the drain output transconductance of output pmos transistor M8.

So, gain is equal to $57\,V/V$ that translates to $\simeq 33dB$. The value is very close to the one targeted and slightly better.

Finally, to conclude the design procedure, noise specifications are analyzed. An analysis, also, is performed to ensure that Input DC offset has an acceptable value. In Figure 4.3, the noise summary of the CM OTA is presented. From the summary we can see that the noisiest devices in CM OTA design are the devices closest to the output (M3-M4, M8 and M10), which are relatively small devices in strong inversion. The total input referred noise at a window of operation between $1\,Hz$ and $600\,kHz$, where the low frequency gain is maximum, is equal to $57\,uVrms$, which is acceptable according to initial specifications. The simulation was performed using the original design kit model card for noise analysis at $25°\,C$.

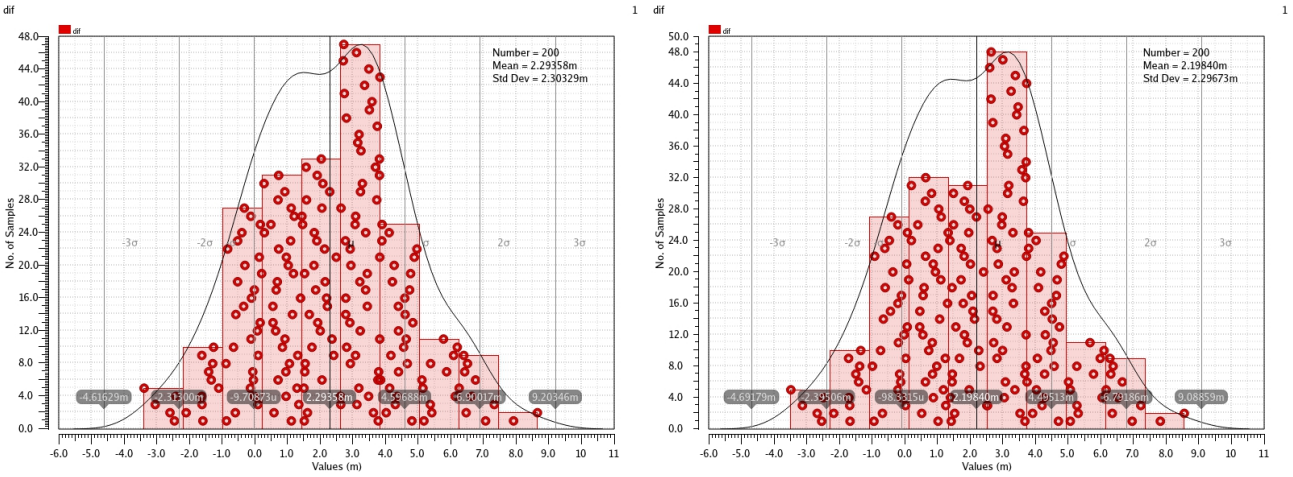
Window Expressions Info Help cadence

Device	Param	Noise Contribution	% Of Total
/M4	fn	2.42334e-10	16.69
/M3	fn	2.27485e-10	14.71
/M8	fn	2.02171e-10	11.62
/M10	fn	1.89783e-10	10.24
/M7	fn	1.84043e-10	9.63
/M9	fn	1.71703e-10	8.38
/M1	fn	1.29609e-10	4.77
/M2	fn	1.29474e-10	4.76
/M1	id	1.18649e-10	4.00
/M2	id	1.18526e-10	3.99
/M8	id	9.05685e-11	2.33
/M10	id	8.50188e-11	2.05
/M7	id	7.8909e-11	1.77
/M4	id	7.84175e-11	1.75
/M9	id	7.36182e-11	1.54
/M3	id	7.36124e-11	1.54
/M8	rs	1.17391e-11	0.04
/M4	rs	1.15459e-11	0.04
/M10	rs	1.10198e-11	0.03
/M3	rs	1.08384e-11	0.03

Integrated Noise Summary (in A) Sorted By Noise Contributors
Total Summarized Noise = 5.93192e-10
Total Input Referred Noise = 5.70889e-05
The above noise summary info is for noise data

Figure 4.3: Noise Summary for CM OTA.

In order to calculate the Input DC offset of the CM OTA, Monte Carlo analysis is required. Input DC offset is equal to the standard deviation of the difference of dc voltages at the input differential pair. In an ideal OTA design, when voltage inputs are equal, the output should be zero. In actual designs this is not the case. In Figure 4.4a, Figure 4.4b and Figure 4.5, the simulated input DC offset is shown for three temperatures, respectively, $-30°\,C$, $0°\,C$ and $25°\,C$. The model used for the Monte Carlo analysis comes from the foundry $65\,nm$ Design Kit. The value of standard deviation in all three is approximately $2.3\,mV$, meaning that there is no temperature scaling of input DC offset and that the value is acceptable at all temperatures.



(a) (b)

Figure 4.4: Input DC offset for (a) $-30°\,C$ and (b) $0°\,C$ (foundry $65\,nm$ Design Kit).

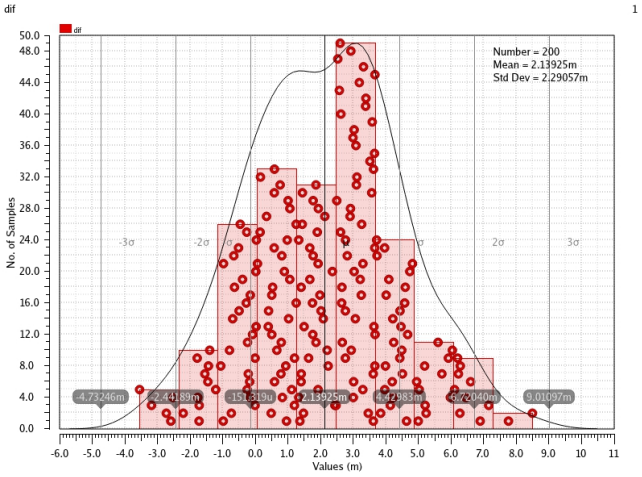
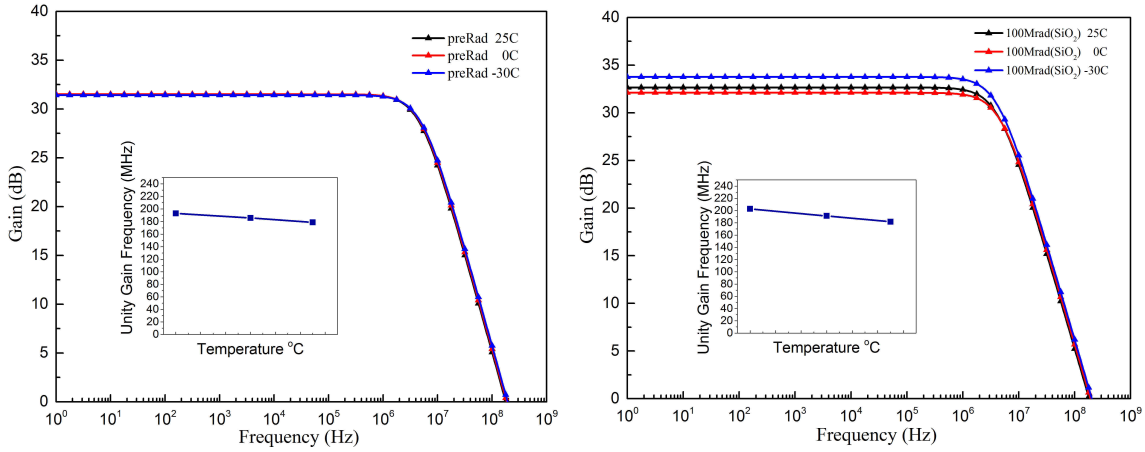


Figure 4.5: Input DC offset for $25°\,C$ (foundry $65\,nm$ Design Kit).

4.1.1 Performance Criteria of CM OTA Under High TID

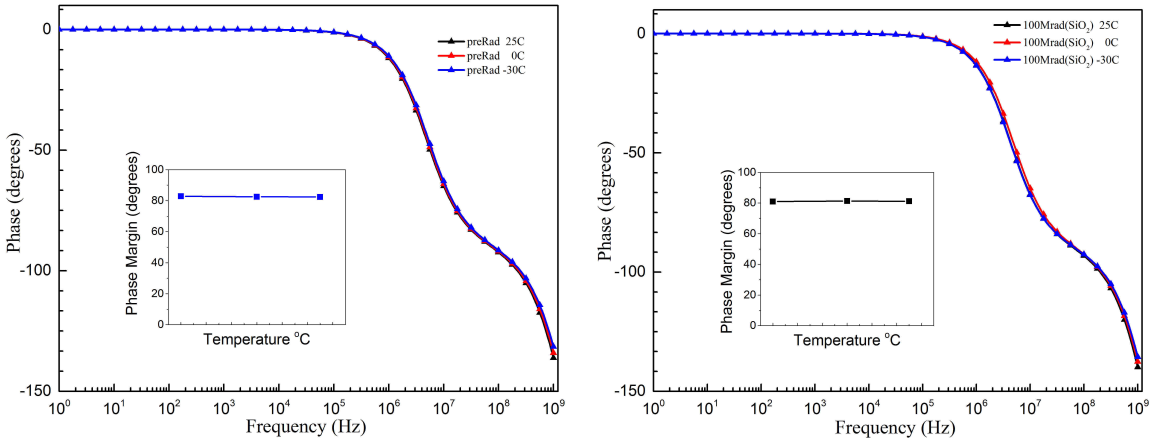
In this section we will discuss the performance criteria that defined the specifications for the design procedure for the CM OTA and we will see the impact of High TID levels on CM OTA performance criteria.

Figures 4.6 to 4.9 present the evolution of voltage gain (dB) and phase (°) for PreRad conditions, for TID of 100 Mrad(SiO_2), TID of 200 Mrad(SiO_2) and TID of 500 Mrad(SiO_2). Each performance criterion is shown for each TID level at three temperatures, namely $-30^o\,C$, $0^o\,C$ and $25^o\,C$.



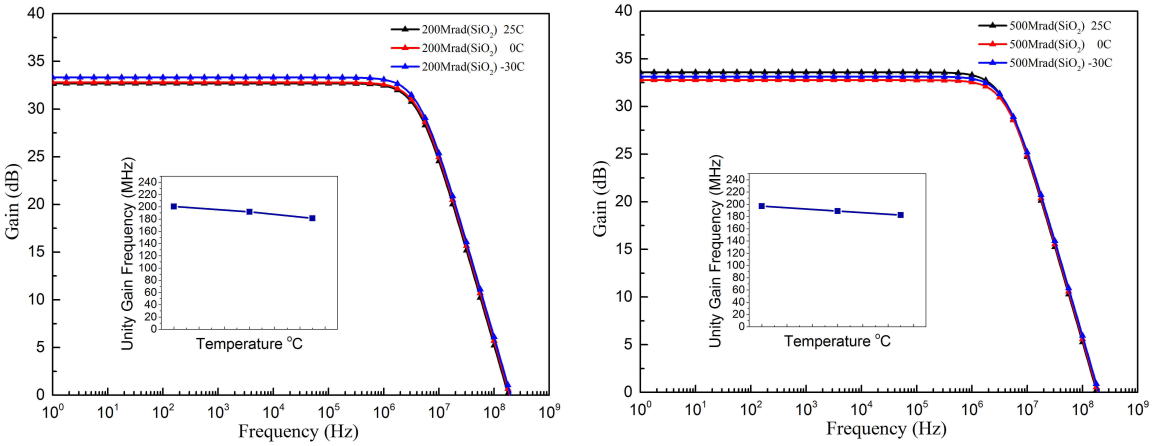
(a) (b)

Figure 4.6: Voltage gain (dB) for (a) PreRad (b) 100 Mrad(SiO_2)



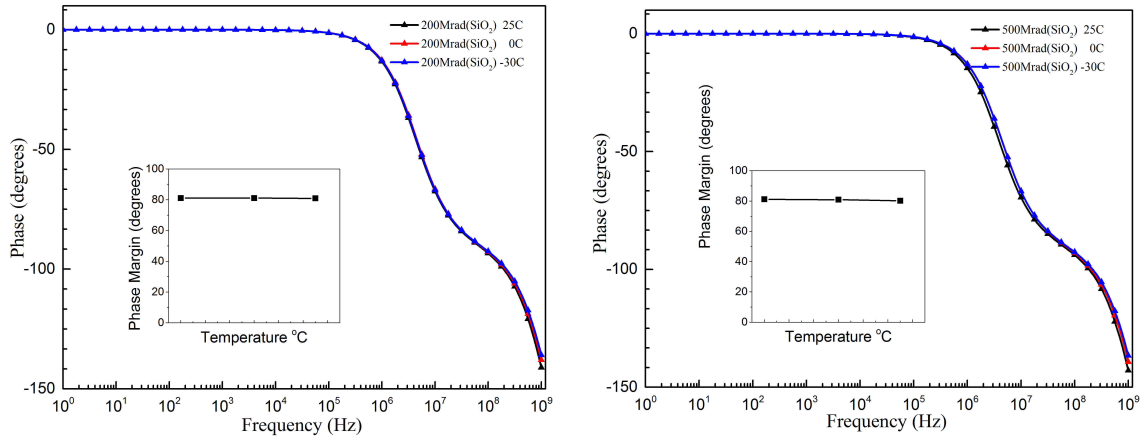
(a) (b)

Figure 4.7: Phase (°) for (a) PreRad (b) 100 Mrad(SiO_2)



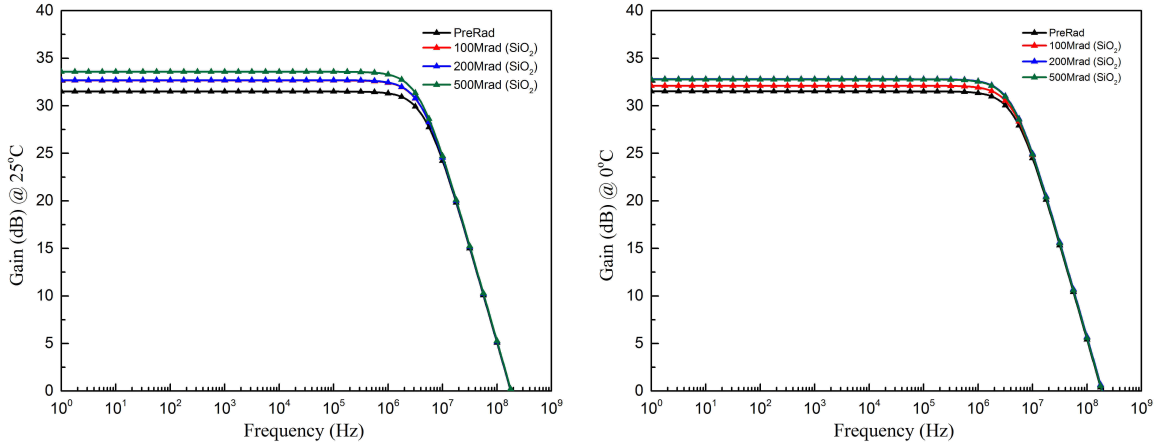
(a) (b)

Figure 4.8: Voltage gain (dB) for (a) 200 Mrad(SiO_2) (b) 500 Mrad(SiO_2)



(a) (b)

Figure 4.9: Phase (°) for (a) 200 Mrad(SiO_2) (b) 500 Mrad(SiO_2)



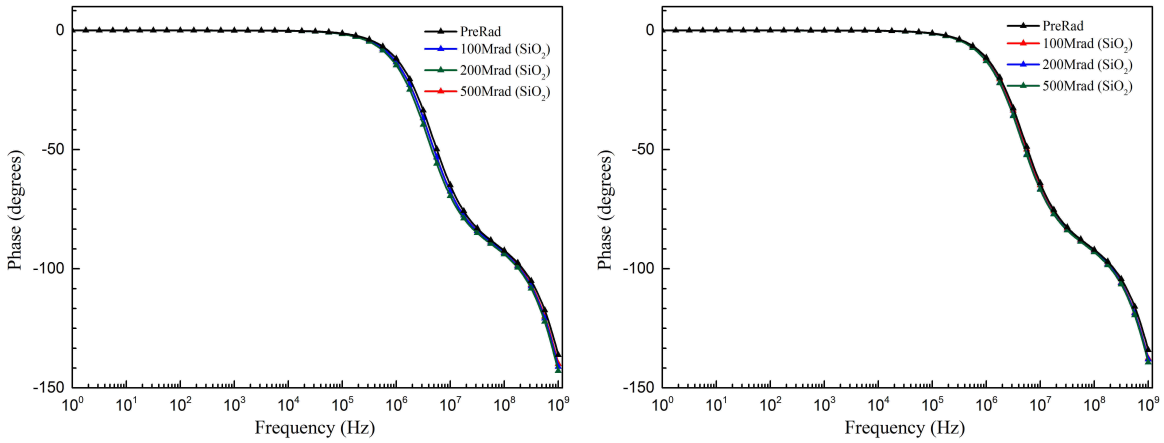
(a) (b)

Figure 4.10: TID voltage gain scaling at (a) $25^o\,C$(b) $0^o\,C$

Figures 4.10 to 4.12 present the evolution of voltage gain (dB) and phase (°) for PreRad conditions, TID of 100 Mrad(SiO_2), TID of 200 Mrad(SiO_2) and for TID of 500 Mrad(SiO_2) from the standpoint of temperature of $-30^o\,C$, $0^o\,C$ and $25^o\,C$. For each temperature, all TID levels are presented in the same Figure.

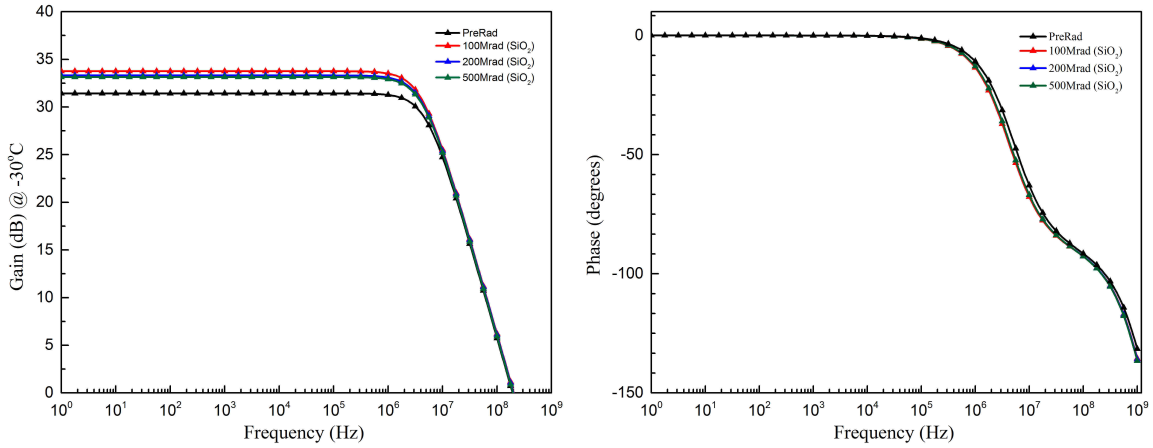
In Figure 4.10a and Figure 4.11a voltage gain (dB) and phase (°) TID scaling is shown for $25^o\,C$. Voltage gain exhibits fluctuations (equal to 1dB) between 100 Mrad(SiO_2) and 500 Mrad(SiO_2) and phase remains unchanged due to TID scaling. In Figure 4.10b and Figure 4.11b voltage gain (dB) and phase (°) TID scaling is shown for $0^o\,C$. Voltage gain exhibits fluctuations (less than 1dB) between minimum and maximum value and phase remains unchanged due to TID scaling. In Figure 4.12a and Figure 4.12b voltage gain (dB) and phase (°) TID scaling is shown for $-30^o\,C$. Voltage gain and phase remain unchanged due to TID scaling. In Figure 4.6a and Figure 4.7a voltage gain (dB) and phase (°) is shown for PreRad conditions. Both criteria remain unchanged due to temperature scaling. In Figure 4.6b and Figure 4.7b voltage

gain (dB) and phase (°) are shown for 100 Mrad(SiO_2). Voltage gain exhibits a small increase at -30^o but phase remains unchanged due to temperature scaling. In Figure 4.8a and Figure 4.9a voltage gain (dB) and phase (°) are shown for 200 Mrad(SiO_2). Voltage gain exhibits no significant fluctuations and phase remains unchanged due to temperature scaling. In Figure 4.8b and Figure 4.9b Voltage gain (dB) and phase (°) are shown for 500 Mrad(SiO_2). Voltage gain exhibits fluctuations (less than $\simeq 1dB$) between minimum and maximum value and phase remains unchanged due to temperature scaling.



(a) (b)

Figure 4.11: TID phase scaling at (a) $25^o\,C$(b) $0^o\,C$



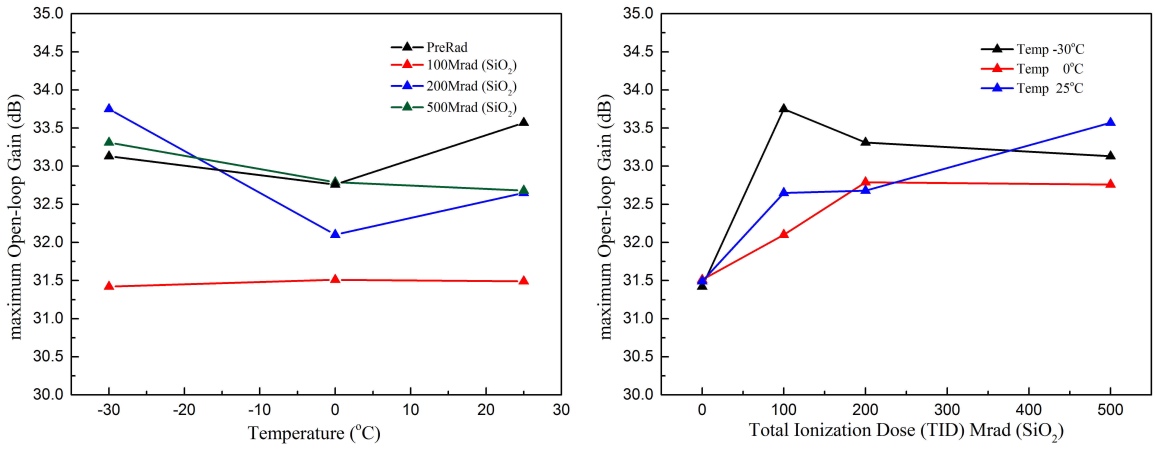
(a) (b)

Figure 4.12: Temperature $-30^o\,C$ (a) voltage gain scaling (b) phase scaling

4.2 Comparison Study of Current Mirror OTA under TID

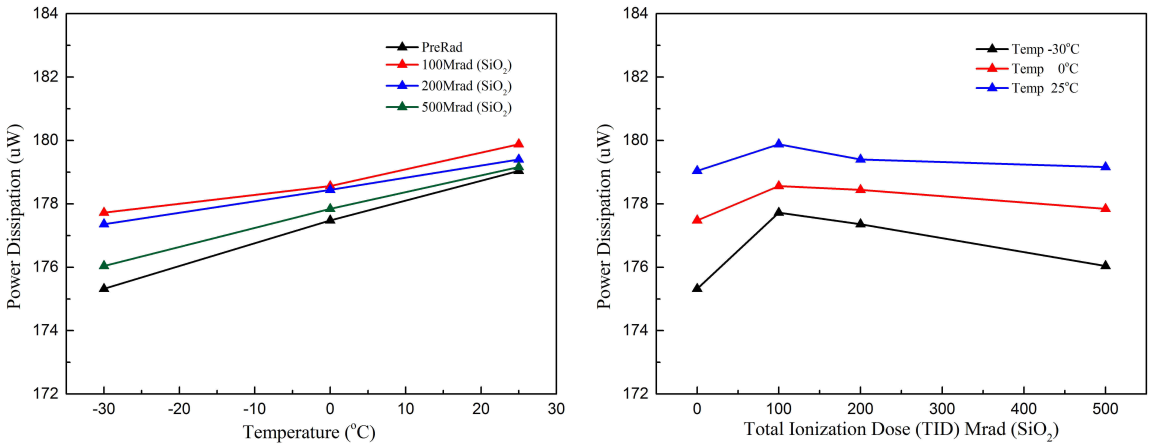
In this section we will discuss in detail the simulation results for the CM OTA. Comparative graphs for Temperature and TID (SiO_2) levels will be presented for all performance criteria. The graphs presented in the previous section are indicative on how robust the CM OTA design is. By closer inspection, though, in these graphs, we can make some observations on how the performance criteria are trending due to TID (SiO_2) levels; despite the fact that there isn't any grave degradation of the selected criteria. In all graphs the PreRad case is shown for reference even though the CM OTA design was implemented directly with the 100 Mrad(SiO_2) model.

Low frequency, maximum Open-loop Gain as stated, is presented in Figure 4.13. In Figure 4.13a we can see that for every TID (SiO_2) level the fluctuation due to temperature scaling for Low Frequency Gain is marginal. The case of 200 Mrad(SiO_2) does not follow the trend that both 100 Mrad(SiO_2) and 500 Mrad(SiO_2) follow. In terms of TID Mrad(SiO_2) levels, Gain shows an increase for each temperature with the increase of TID, with a minimum value of $1\,dB$. At 100 Mrad(SiO_2) the value variation in more pronounced and the value at $-30^o\,C$ seems to be grater. Meaning that designing in $0^o\,C$ or $25^o\,C$ is more critical.



(a) (b)

Figure 4.13: Maximum Open-loop Gain scaling with (a) Temperature $^o\,C$(b) TID level Mrad(SiO_2)

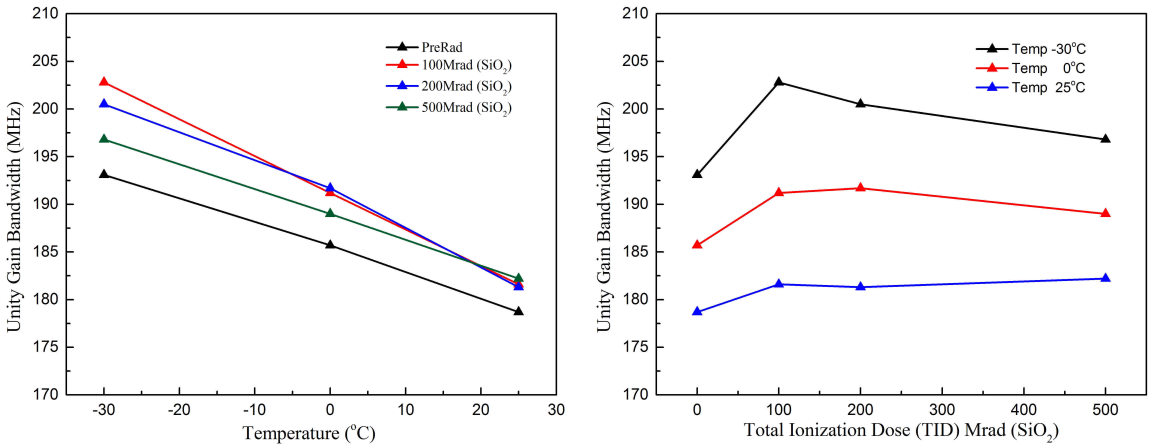


(a) (b)

Figure 4.14: Power dissipation scaling with (a) Temperature ^{o}C(b) TID level Mrad(SiO_2)

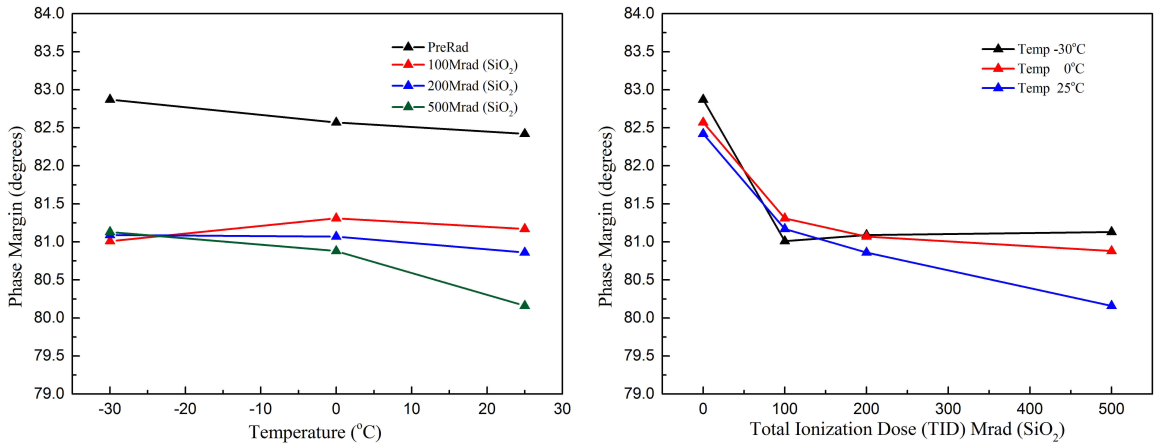
In Figure 4.14a we can observe a slight increase in power dissipation for all TID levels. The case of 500 Mrad (SiO_2) shows a decreased power dissipation compared to 100 (SiO_2) and 200 (SiO_2). In Figure 4.14b we can observe the adverse, with the increase of TID a slight decrease can be seen for Power Dissipation, at every temperature. Power dissipation decreases with the decrease of temperature. At this point we can say that the inversion coefficient of each device remains practically the same. As TID level increases, technology current I_o decreases and combined with the decrease in power dissipation, we can confidently say that the IC of each device stays practically the same.

In Figure 4.15a unity gain bandwidth (UGB) is presented vs temperature. We can see that for every TID level, as temperature increases, UGB decreases almost 15 MHz reaching 25^{o}C. As TID increases we observe bandwidth compression that wasn't previously apparent. For the case of UGB versus TID Levels at every temperature shown in Figure 4.15b, we can observe that there is no significant UGB scaling with TID levels.



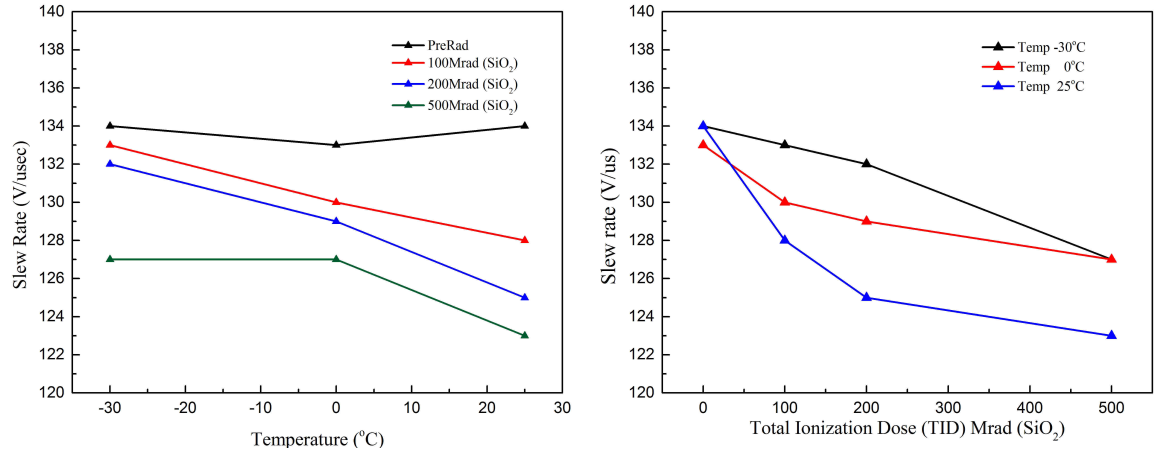
(a) (b)

Figure 4.15: Unity gain bandwidth scaling with (a) Temperature ^{o}C(b) TID level Mrad(SiO_2)



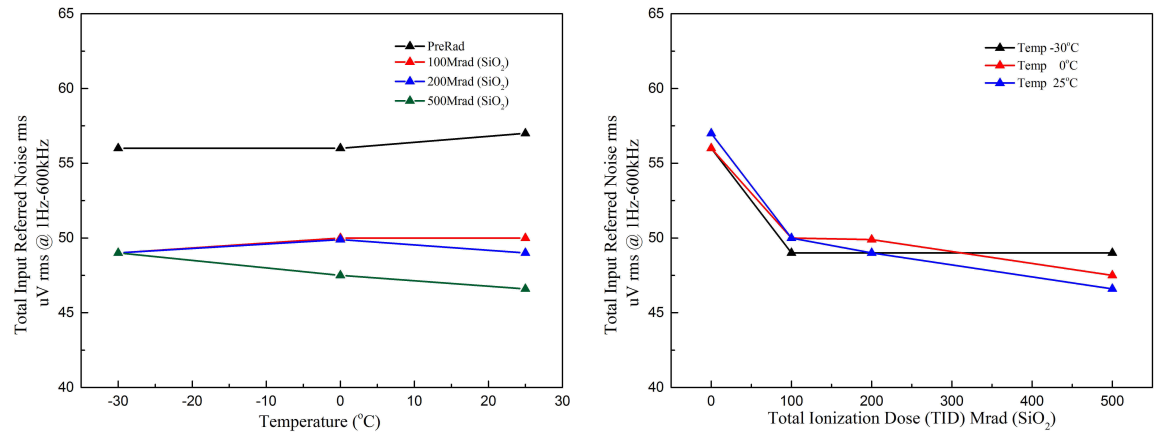
(a) (b)

Figure 4.16: Phase margin scaling with (a) Temperature ^{o}C(b) TID level Mrad(SiO_2)



(a) (b)

Figure 4.17: Slew rate scaling with (a) Temperature ^{o}C(b) TID level Mrad(SiO_2)



(a) (b)

Figure 4.18: Total input referred noise scaling with (a) Temperature ^{o}C(b) TID level Mrad(SiO_2)

Figure 4.16a shows the temperature scaling of phase margin. We can see that phase margin degrades with the increase of temperature, a fact that is more pronounced for the case of 500 Mrad (SiO_2). Figure 4.16b shows that at every temperature phase margin degrades with TID levels.

In Figure 4.17a, slew rate is presented versus temperature. We can observe that SR follows the degradation of drain currents with temperature and the decrease is more pronounced for 500 Mrad (SiO_2). In Figure 4.17b, we can observe that as TID level increases for all temperatures SR decreases. At this point we should mention that all simulation results were performed with fixed output load capacitance, C_L. Any possible TID effects on C_L are not accounted for.

Finally, in Figure 4.18, total input referred noise remains unchanged in terms of temperature and TID levels.

4.3 Folded cascode OTA

For the Folded Cascode OTA, the biasing stage consists of an NMOS low-voltage, cascode current mirror (M13-M14, M16-M17 cascode transistors). The gain stage consists of an NMOS differential pair (M1-M2), biased through transistor M15, the current of which is mirrored off of M13-M14 pair to M15. Transistors M11 and cascode M12 are current-fed by cascode transistor M17 and act as reference current sources to the M3-M4 PMOS pair, which act similarly as current sources. PMOS pair M3-M4 is connected directly to the differential pair and the folded cascode transistors M7-M8. Transistor M8 together with an NMOS low-voltage, cascode current mirror (M5-M6, M9-M10 cascode transistors) form the output stage of the OTA. The current mirror at the output creates a complementary signal path through transistor M7. [28]

All supply voltages, VDD and VSS, are kept constant. All biasing voltages, Vbias1, Vbias2 and VinCM, are kept constant and the reference current provided to the biasing stage is also kept constant with a value of $I_{BIAS} = 25\,uA$.

Folded cascode OTA (FC OTA) was not designed in the original 65nm Design Kit that doesn't account for any TID effects and it was directly implemented with the integrated model for 100 Mrad(SiO_2) and the initial design/simulation temperature is 25°. The technology current for the the model version of 100 Mrad(SiO_2) at 25° is $I_{o,n} = 250\,nA$ for nmos devices and $I_{o,p} = 100\,nA$ for pmos devices.

For the FC OTA the power dissipation was chosen to be 240 uW (200 uA in 1.2 Voltage Supply) and the corresponding current for each branch is shown in Figure 4.19. The OTA was designed to meet certain similar specifications similarly with the case of the CM OTA. The output load capacitor (C_L) is chosen with a value of 400 fF, low frequency gain was chosen to be 40 dB, unity gain bandwidth was chosen to be greater than 300 MHz, slew rate was chosen to be greater than 100 $V/usec$, input noise was chosen to be lower than 10 uV/$\sqrt{Hz}$ at 1 Hz.

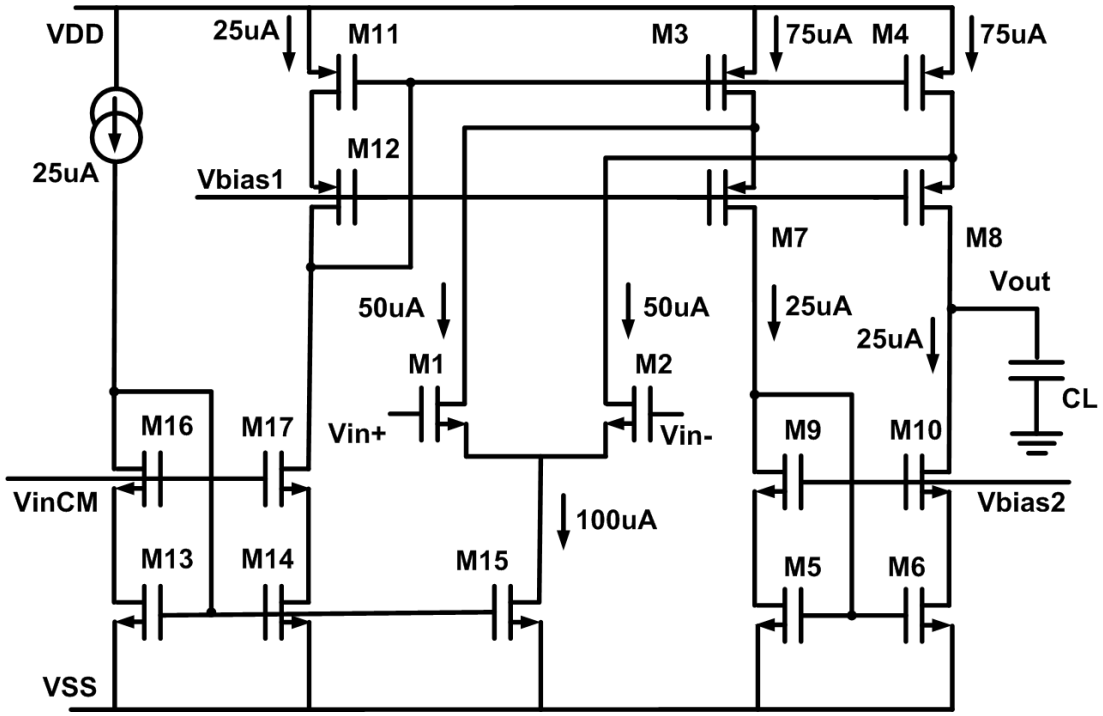
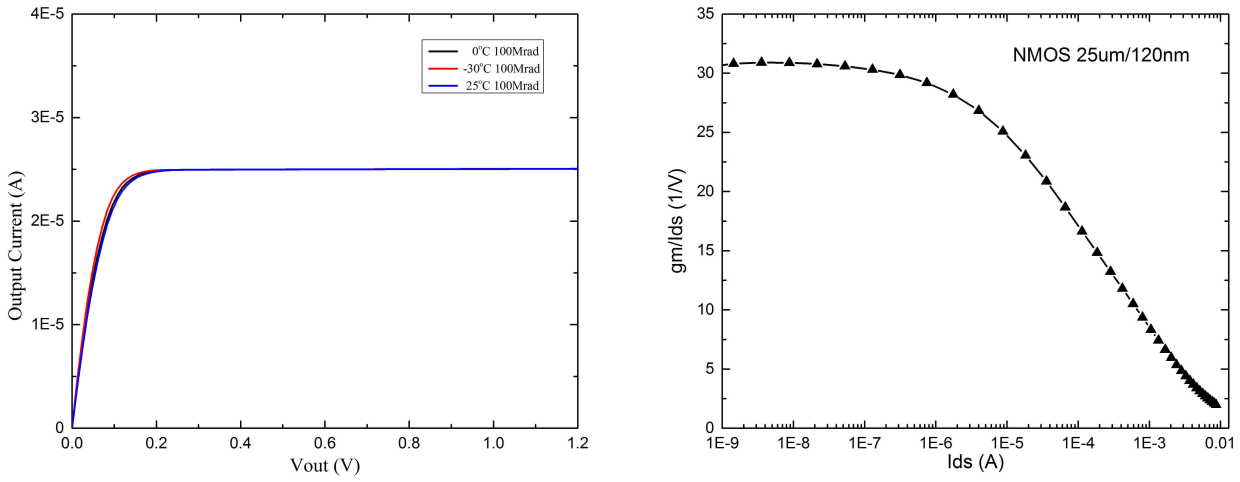


Figure 4.19: Folded Cascode OTA.

First step in the designing process is to size the input low-voltage, cascode current mirror used for the FC OTA input biasing and the source follower device M15. The input biasing nmos current mirror is not in signal path, as also mentioned in CM OTA design. Due to cascode configuration, higher operation voltage than a conventional current mirror is needed. In order to minimize the headroom requirement, all devices are chosen to operate in moderate inversion. Specifically, for cascode pair M16-M17 an $IC = 1$ is chosen that leads to $Width = 104\,um$, given $Length = 1\,um$. For the rail pair M13-M14 an $IC = 9.5$ is chosen that leads to $Width = 10.5\,um$, given $Length = 1\,um$. All devices were chosen to have a $Length = 1\,um$ to alleviate local mismatch effects, because cascode current mirror is susceptible to threshold mismatch. For device M15 an $IC = 9.5$ is chosen, leading to $Width = 42\,um$, given $Length = 1\,um$. Voltage $VinCM$ ensures operation in saturation for M16 and M17 devices. [45] Voltage $VinCM$ is equal to $600\,mV$ and provides a low, cascode gate voltage for cascode devices M16 and M17. When the FC OTA inputs are at a common mode voltage equal to $600\,mV$, the bias current of the M15 is replicated from the current of M13, because both devices have equal drain-source voltages. [28] In Figure 4.20a, the output response of the cascode current mirror is presented. We can observe that in the case of the cascode current mirror the output conductance is lower than that of a conventional current mirror, as expected. This current mirror provides additional biasing stability to the input differential pair, so the dimensions are such that would alleviate any biasing instabilities due to process and mismatch variations, but most importantly any changes due to TID effects, that are more detrimental in smaller dimensions.



(a) (b)

Figure 4.20: Design process (a) cascode current mirror output current vs output voltage (b) g_m/I_{ds} vs I_{ds} of input devices for $V_{ds} = 1.2\,Volt$.

For the nmos input differential pair, an $IC = 1$ is chosen, which places the device operation in the center of moderate inversion. [46] This choice leads to $Width = 25\,um$, given $Length = 120\,nm$. Consequently, the corresponding mutual conductance is equal to $850\,uS$. In Figure 4.20b, the extraction of metric g_m/I_{ds} of the transistor dimensions mentioned is presented for $V_{ds} = 1.2\,Volt$. The moderate inversion choice minimizes input referred thermal noise and helps these devices dominate in FC OTA noise. M1 and M2 have equal inversion coefficients, sizing, and transconductances. [28]

Rail devices M5 and M6 operate with $25\,uA$ each and an $IC = 10$, at the upper edge of moderate inversion. The M7-M8 and M9-M10 cascode pair devices operate with $25\,uA$, with an $IC = 1$ and $IC = 1.85$, respectively. The devices comprising each pair have equal dimensions and ICs. Each device in PMOS pair M7-M8 has $Width = 28\,um$, given $Length = 120\,nm$. Each device in NMOS pair M9-M10 has $Width = 6.4\,um$, given $Length = 120\,nm$. $Vbias1 = 600\,mV$ and $Vbias2 = 470\,mV$ provide respectively low voltage gate biasing to pair M7-M8 and pair M9-M10 along with device M12. These cascode devices contribute negligible noise because their transconductances are low. M12 is of equal dimensions, drain current and IC as pair M7-M8 to ensure the accurate replication of bias currents. Rail PMOS pair M3-M4 devices operate at a supply current of $75\,uA$ and $IC = 2.1$ with $Width = 28.8\,um$, given $Length = 120\,nm$. These devices that operate in moderate inversion aid in noise reduction. Device M11 operates with a current of $25\,uA$ which is one third of the current that pair M3-M4 operates. In order to ensure the bias current replication, the dimensions of transistor M11 are equal to one third of the pair in question, leading to $Width = 9.6\,um$, given $Length = 120\,nm$ and an $IC = 3$.

In table 4.2, all device dimensions are listed together with the inversion coefficient chosen for the FC OTA design using model for 100 Mrad(SiO_2) at $25°\,C$.

At this point, we can theoretically calculate slew rate with the aid of equation 3.9. $SR \simeq$

Type	*Instance*	*Width*	*Length*	*IC*
Nmos	M1=M2	25 um	120 nm	0.95
Pmos	M3=M4	28.8 um	120 nm	2.1
Nmos	M5=M6	1.2 um	120 nm	10
Pmos	M7=M8	28 um	120 nm	1
Nmos	M9=M10	6.4 um	120 nm	1.85
Pmos	M11	9.6 um	120 nm	3
Pmos	M12	28 um	120 nm	1
Nmos	M13=M14	10.5 um	1 um	9.5
Nmos	M15	42 um	1 um	9.5
Nmos	M16=M17	104 um	1 um	1

Table 4.2: Folded Cascode OTA

$125\,V/usec$ is acceptable according to specifications. It is important to say that for SR calculation the current taken into consideration is the output current of the FC OTA, which is $2\,I_{ds,10} = 50\,uA$, instead of the tail current that equals $100\,uA$.

Cascode devices M8 and M10 strongly influence the FC OTA output resistance, voltage gain, and transconductance bandwidth. The low frequency voltage gain of the amplifier is given by the following equation:

$$A_V = g_{m,1}(r_{out,8}||r_{out,10}) \tag{4.3}$$

where $g_{m,1}$ is the transconductance of input nmos transistor M1, $r_{out,8}$ is the output resistance of output pmos transistor M8 and $r_{out,10}$ is the output resistance of output pmos transistor M10.

Equation 4.3 can be expressed, also, as follows:

$$A_V = \frac{g_{m,1}}{I_{ds,1}} I_{ds,1}(r_{out,8}||r_{out,10}) = \frac{I_{ds,1}}{n_1\,U_T(\sqrt{IC_1 + 0.25} + 0.5)}(r_{out,8}||r_{out,10}) \tag{4.4}$$

In order to fully understand the complexity of the design and the influence of each device, we will provide the equations for $r_{out,8}$ of transistor M8 and $r_{out,10}$ of transistor M10.

$$r_{out,8} = r_{ds,8}\,[1 + \frac{g_{ms,8}}{g_{ds,2} + g_{ds,4}}] \tag{4.5}$$

where $g_{ds,8}$ is the drain output transconductance of output pmos transistor M8, $g_{ds,2}$ is the drain output transconductance of input transistor M2, $g_{ds,4}$ is the drain output transconductance of rail pmos transistor M4 and $g_{ms,8}$ is the source output transconductance transistor M8.

$$r_{out,10} = r_{ds,10}\,[1 + \frac{g_{ms,10}}{g_{ds,6}}] \tag{4.6}$$

where $g_{ds,10}$ is the drain output transconductance of output nmos transistor M10, $g_{ds,6}$ is the drain output transconductance of rail transistor M6 and $g_{ms,10}$ is the source output transconductance transistor M10.

So, gain equals $126\,V/V$ that translates to $\simeq 42dB$. The value is very close to the one targeted.

The pole with the lowest frequency is considered for the evaluation of the FC OTA. The pole of the FC OTA is placed at the drain of transistors M7-M8 and their f_{-3dB} frequency can be calculated by the following equation:

$$f_{-3dB} = \frac{g_{m,7}}{2\pi(C_{gs,7} + C_{sb,7} + C_{db,1} + C_{gd,1} + C_{db,3} + C_{gd,3})} \tag{4.7}$$

where $g_{m,7}$ is the transconductance of the M7 pmos mirror input device, $C_{gs,7}$ and $C_{sb,7}$ is the gate-source transconductance and source-bulk transconductance of transistor M7, $C_{db,1}$ and $C_{gd,1}$ is the drain–bulk capacitance and gate-drain capacitance of M1, $C_{db,3}$ and $C_{gd,3}$ is the drain–bulk capacitance and gate-drain capacitance of M3. [28]

The design procedure of the Folded Cascode OTA is more intricate, in contrast with the Current Mirror OTA being simpler with fewer restrictions in sizing.

Finally, to conclude the design procedure noise specifications are considered. Also, Input DC offset is simulated in order to ensure an acceptable value. In Figure 4.21, the noise summary of the FC OTA is presented. From the summary we can see that the noisiest devices in FC OTA design are rail device M4, output cascode device M8 and the input differential pair M1-M2. The total input referred noise at a window of operation between $1\,Hz$ and $1\,MHz$, where the low frequency gain is maximum, is equal to $22.75\,uVrms$, which is acceptable according to initial specifications. The simulation was performed using the original design kit model card for noise analysis at $25^\circ C$.

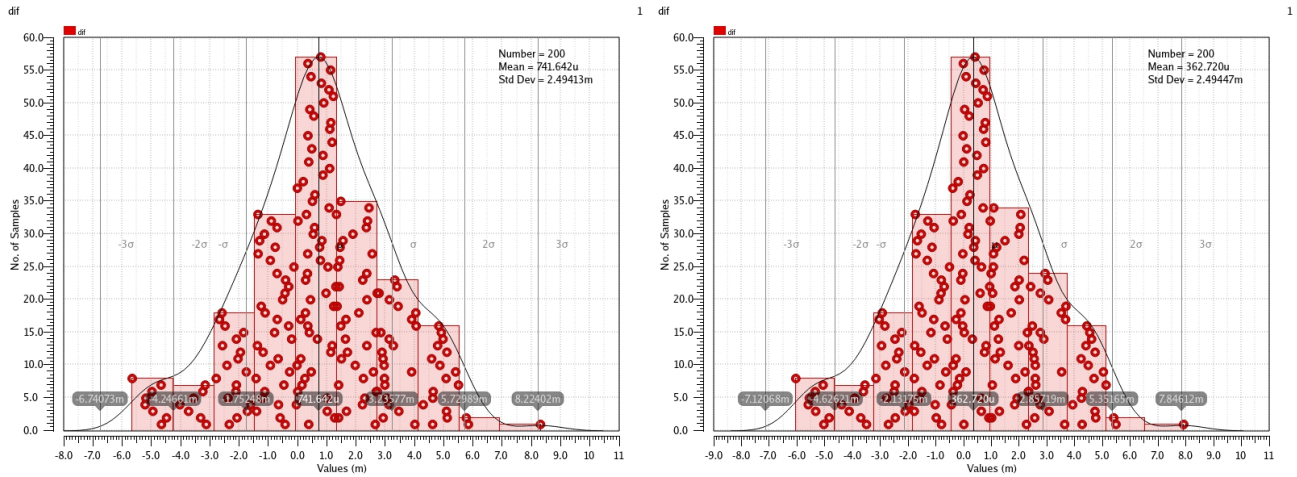
Window Expressions Info Help cadence

Device	Param	Noise Contribution	% Of Total
/M8	fn	2.92141e-16	26.74
/M4	fn	2.6952e-16	22.76
/M1	fn	2.31656e-16	16.81
/M0	fn	2.30667e-16	16.67
/M2	fn	1.50568e-16	7.10
/M3	fn	1.43278e-16	6.43
/M5	fn	6.83521e-17	1.46
/M6	fn	6.35795e-17	1.27
/M7	fn	3.86874e-17	0.47
/M30	fn	1.32085e-17	0.05
/M10	fn	1.25763e-17	0.05
/M9	fn	1.18818e-17	0.04
/M8	id	1.00716e-17	0.03
/M4	id	9.30517e-18	0.03
/M1	id	8.71355e-18	0.02
/M0	id	8.71277e-18	0.02
/M2	id	4.74097e-18	0.01
/M15	fn	4.72047e-18	0.01
/M3	id	4.42736e-18	0.01
/M16	fn	4.14709e-18	0.01
/M5	id	1.96885e-18	0.00
/M6	id	1.79058e-18	0.00
/M7	id	1.33756e-18	0.00
/M30	id	9.62894e-19	0.00
/M10	id	8.46776e-19	0.00
/M8	rs	8.08868e-19	0.00
/M9	id	7.93499e-19	0.00
/M2	rs	7.54306e-19	0.00

Spot Noise Summary (in A/sqrt(Hz)) at 1K Hz Sorted By Noise Contributors
Total Summarized Noise = 5.6496e-16
Total Input Referred Noise = 2.27287e-07
The above noise summary info is for noise data

Figure 4.21: Noise Summary for FC OTA.

In order to calculate the Input DC offset of the FC OTA, Monte Carlo analysis is required. In Figure 4.22a, Figure 4.22b and Figure 4.23, the simulated input DC offset is shown for three temperatures, respectively, $-30°\,C$, $0°\,C$ and $25°\,C$. The model used for the Monte Carlo analysis comes from the foundry $65\,nm$ Design Kit. The value of standard deviation in all three is approximately $2.5\,mV$, meaning that there is no temperature scaling of Input DC offset. Such value is acceptable for this FC OTA design choices.



(a) (b)

Figure 4.22: FC OTA input DC offset for (a) $-30°\,C$ and (b) $0°\,C$ (foundry $65\,nm$ Design Kit).

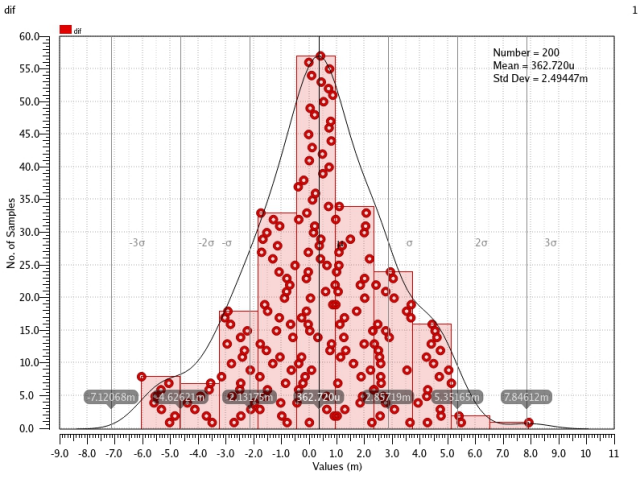


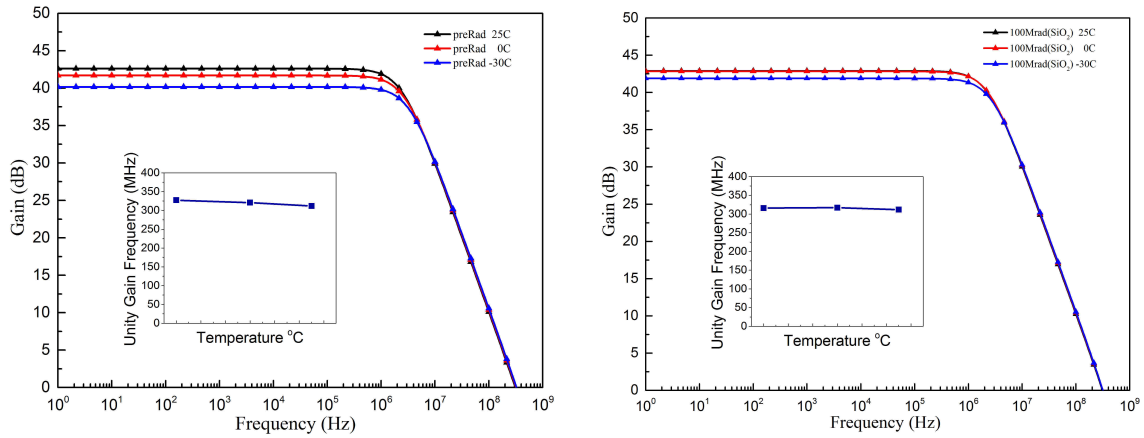
Figure 4.23: FC OTA input DC offset for $25° C$ (foundry $65\,nm$ Design Kit).

4.3.1 Performance Criteria of FC OTA Under High TID

In this section we will discuss the performance criteria that defined the specifications for the design procedure for the FC OTA and we will see the impact of High TID levels on FC OTA performance criteria.

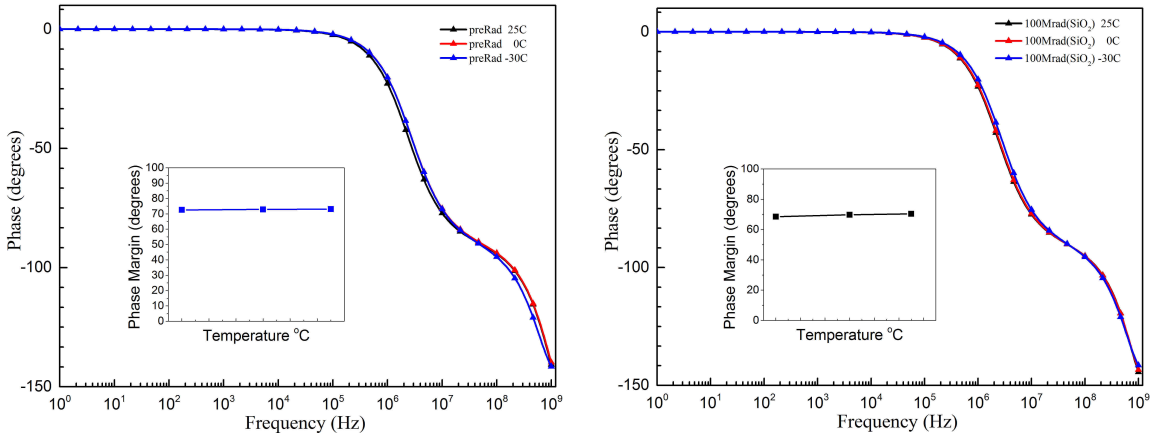
Figures 4.24 to 4.27 present the evolution of voltage gain (dB) and phase (°) for PreRad conditions, for TID of 100 Mrad(SiO_2), for TID of 200 Mrad(SiO_2) and for TID of 500 Mrad(SiO_2). Each performance criterion is shown for each TID level in three temperatures, namely $-30^o\,C$, $0^o\,C$ and $25^o\,C$.

In Figure 4.24a and Figure 4.25a voltage gain (dB) and phase (°) is shown for PreRad. Voltage gain exhibits a $2.5\,dB$ difference between minimum and maximum value, which is for $-30^o\,C$ and $25^o\,C$ respectively. Phase exhibits insignificant fluctuations due to temperature scaling. In Figure 4.24b and Figure 4.25b voltage gain (dB) and phase (°) is shown for 100 Mrad(SiO_2). Voltage gain exhibits a $0.5\,dB$ difference between minimum and maximum value, which is for $-30^o\,C$ and $25^o\,C$ respectively. Phase remains unchanged due to temperature scaling.



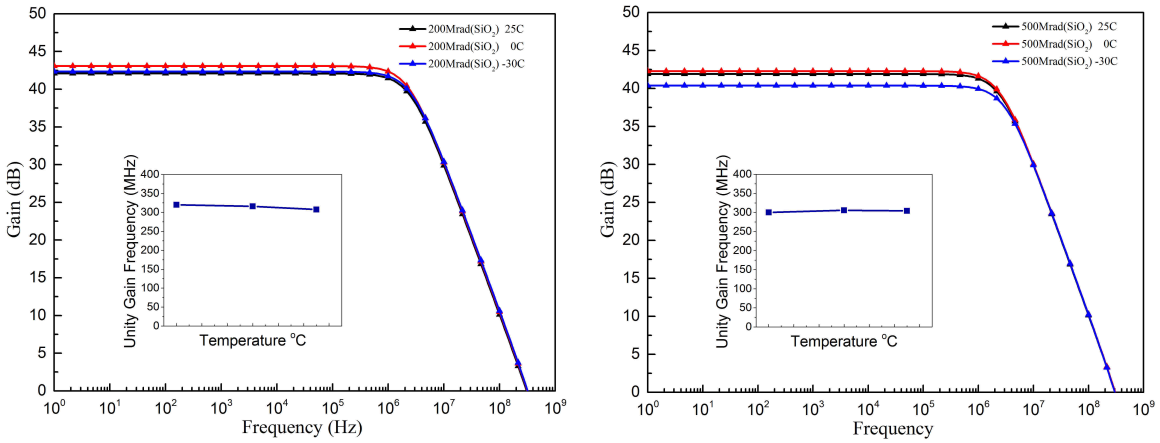
(a) (b)

Figure 4.24: Voltage gain (dB) for (a) PreRad (b) 100 Mrad(SiO_2)



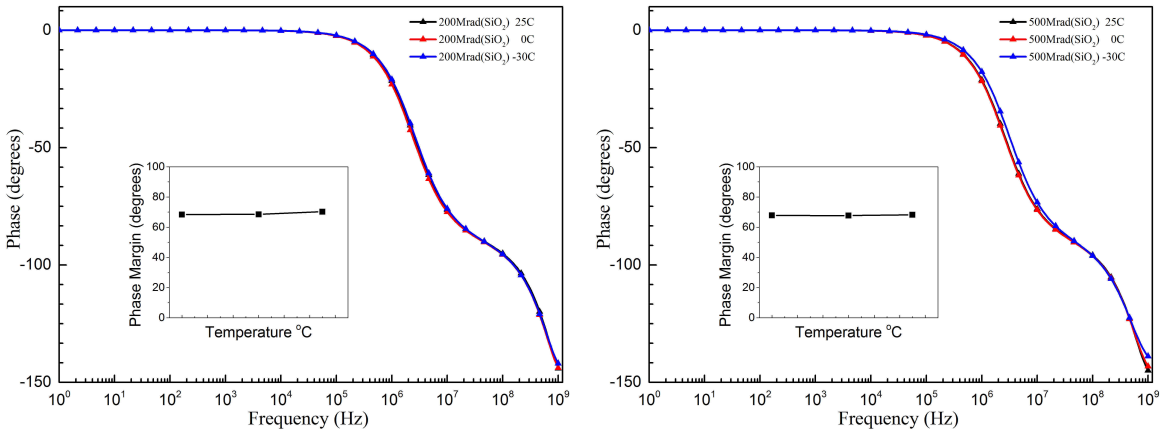
(a) (b)

Figure 4.25: Phase (°) for (a) PreRad (b) 100 Mrad(SiO_2)



(a) (b)

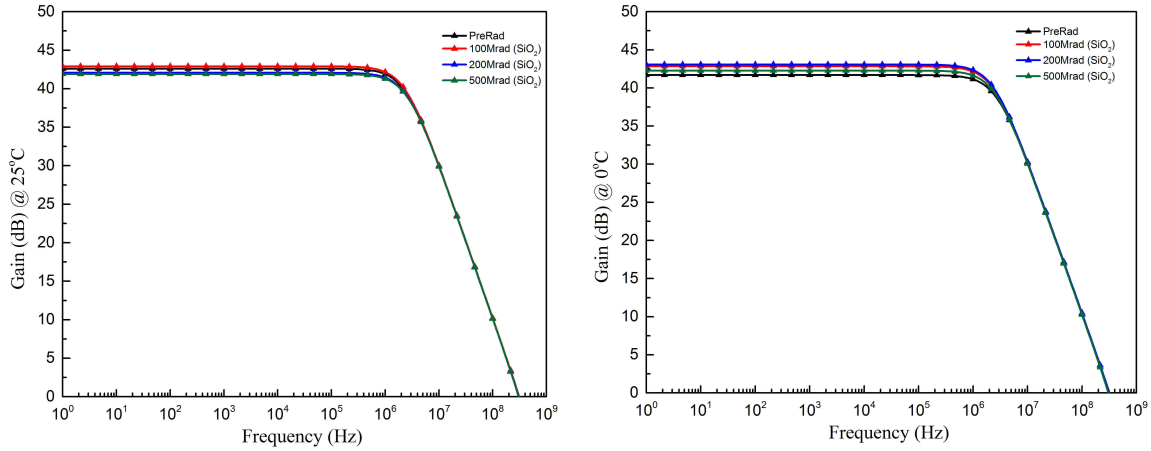
Figure 4.26: Voltage gain (dB) for (a) 200 Mrad(SiO_2) (b) 500 Mrad(SiO_2)



(a) (b)

Figure 4.27: Phase (°) for (a) 200 Mrad(SiO_2) (b) 500 Mrad(SiO_2)

In Figure 4.26a and Figure 4.27a Voltage Gain (dB) and Phase (°) is shown for 200Mrad(SiO_2). Voltage Gain exhibits a less than 1 dB difference between minimum and maximum value, which is for $0^o\,C$. Phase shows no change due to temperature scaling. In Figure 4.26b and Figure 4.27b Voltage Gain (dB) and Phase (°) is shown for 500Mrad(SiO_2). Voltage gain exhibits a 2 dB difference between minimum and maximum value, which is for $0^o\,C$. Phase shows no change due to temperature scaling.



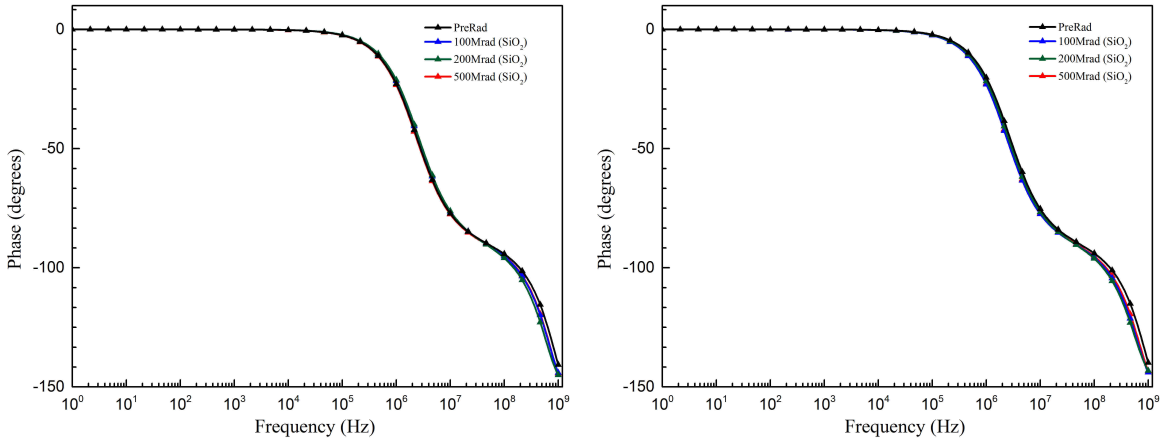
(a) (b)

Figure 4.28: TID (SiO_2) voltage gain scaling at (a) $25^o\,C$(b) $0^o\,C$

Figures 4.28 to 4.30 present the evolution of voltage gain (dB) and phase (°) for PreRad conditions, for TID of 100 Mrad(SiO_2), for TID of 200 Mrad(SiO_2) and for TID of 500 Mrad(SiO_2) from the standpoint of temperature of $-30^o\,C$, $0^o\,C$ and $25^o\,C$. For each temperature, all TID levels are presented in the same Figure.

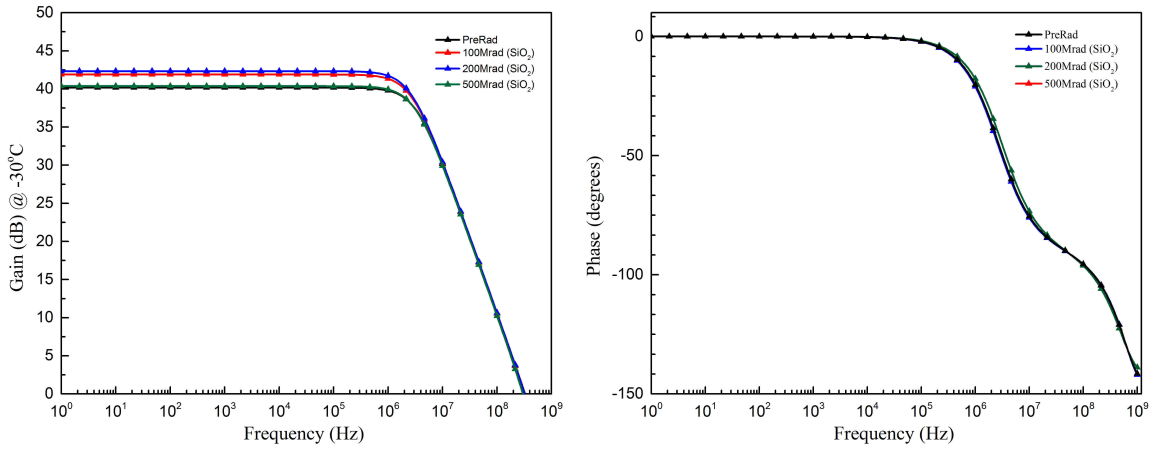
In Figure 4.28a and Figure 4.29a voltage gain (dB) and phase (°) TID scaling is shown for $25^o\,C$. Voltage gain exhibits no significant fluctuations (less than 1 dB) between 100 Mrad(SiO_2) and 500 Mrad(SiO_2) and Phase remains unchanged due to TID scaling. In Figure

4.28b and Figure 4.29b Voltage gain (dB) and phase (°) TID scaling is shown for $0^o\,C$. Voltage gain exhibits fluctuations (less than $1\,dB$) between minimum and maximum value and Phase remains unchanged due to TID scaling. In Figure 4.30a and Figure 4.30b Voltage gain (dB) and Phase (°) TID scaling is shown for $-30^o\,C$. Voltage gain exhibits a $2\,dB$ difference between minimum and maximum value, which is for 500 Mrad(SiO_2) and 200 Mrad(SiO_2) respectively. Phase is still unchanged due to TID scaling.



(a) (b)

Figure 4.29: TID (SiO_2) phase scaling at (a) $25^o\,C$(b) $0^o\,C$



(a) (b)

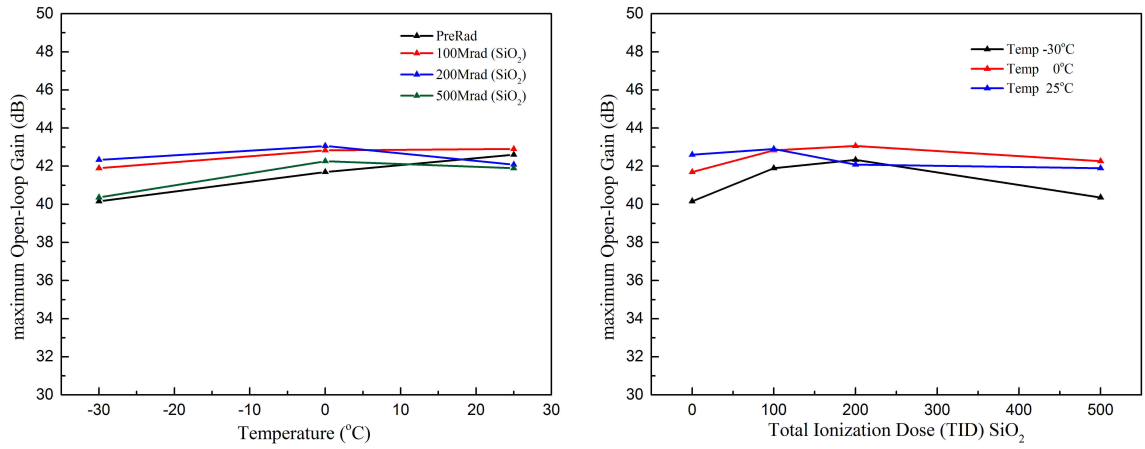
Figure 4.30: Temperature $-30^o\,C$ (a) Voltage gain scaling (b) Phase scaling

4.4 Comparison Study under TID for FC OTA

In this section we will discuss in detail the simulation results for the FC OTA. Comparative graphs for Temperature and TID (SiO_2) levels will be presented for all performance criteria, as seen for CM OTA. The graphs presented in previous section are indicative on how robust the FC OTA design is and in this section we will how robust a FC OTA is compared to the

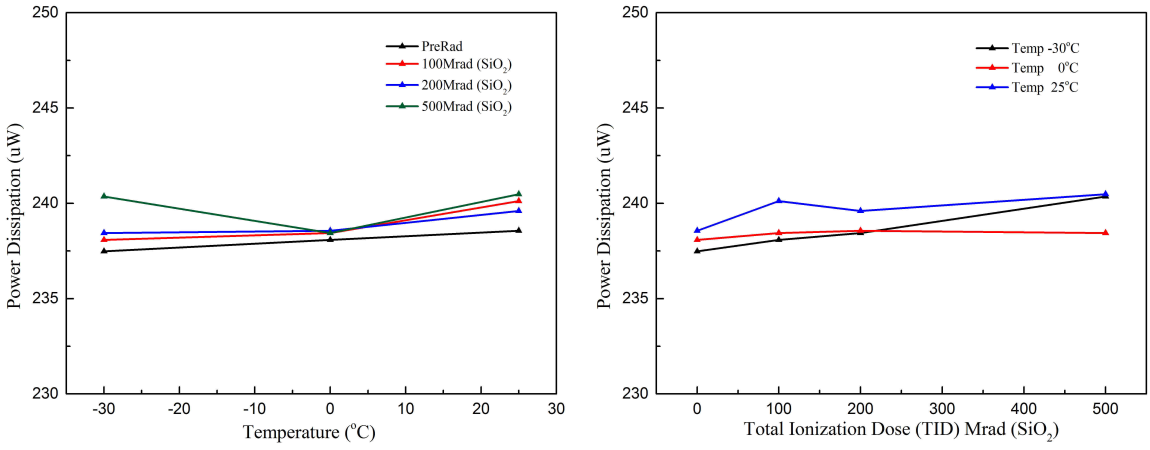
CM OTA (Balanced). Observations on how the performance criteria are trending due to TID (SiO_2) levels will be discussed; despite the fact that there isn't any grave degradation of the selected criteria, just as for the CM OTA. In all graphs PreRad case is shown for reference even though the FC OTA design was implemented directly with the 100 Mrad(SiO_2) model.

Maximum Open-loop gain is presented in Figure 4.31. In Figure 4.31a we can see that for every TID (SiO_2) level the fluctuation due to temperature scaling for low frequency gain is marginal. All TID levels, 100 Mrad(SiO_2), 200 Mrad(SiO_2) and 500 Mrad(SiO_2) follow this trend in temperature scaling graph. In terms of TID Mrad(SiO_2) levels, low frequency gain shows a marginal decrease for each temperature with the increase of TID.



(a) (b)

Figure 4.31: Maximum Open-loop Gain scaling with (a) Temperature ^oC(b) TID level Mrad(SiO_2)



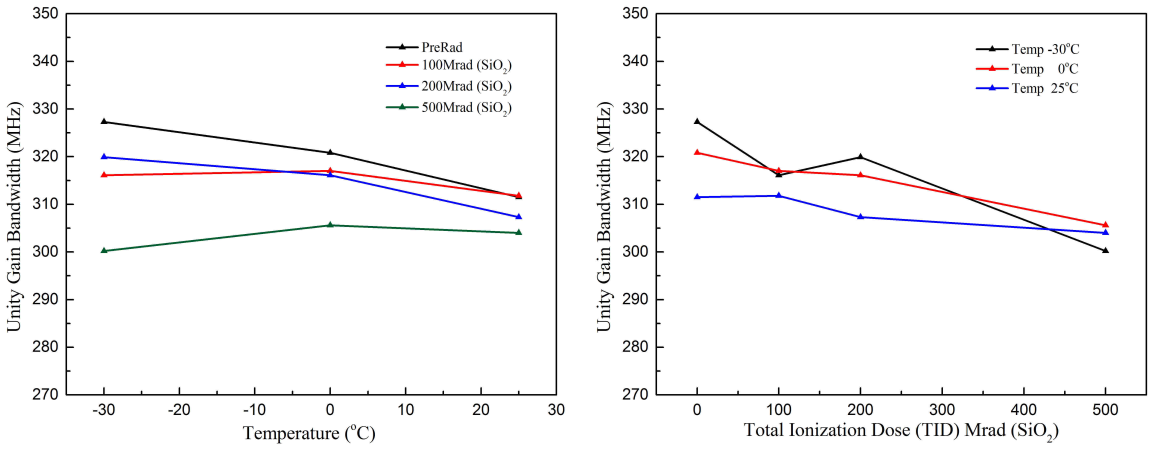
(a) (b)

Figure 4.32: Power dissipation scaling with (a) Temperature ^oC(b) TID level Mrad(SiO_2)

In Figure 4.32a we can observe a slight increase in power dissipation for all TID levels. The case of 500 Mrad(SiO_2) shows an increased Power Dissipation compared to 100 Mrad(SiO_2)

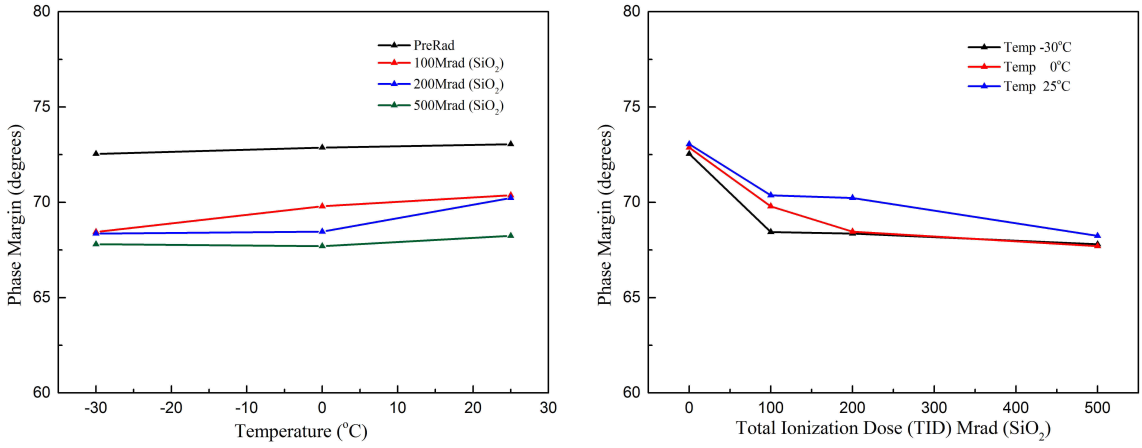
and 200 Mrad(SiO_2), especially at $-30^o\,C$. In Figure 4.31b we can observe that the increase of TID causes a marginal increase in power dissipation in every temperature. Power dissipation is decreased with decreased temperature. At this point we can say, also, that the inversion coefficient of each device remains practically the same.

In Figure 4.33a UGB is presented vs temperature. We can see that for every TID level as temperature increases UGB decreases marginally. [47] As TID increases we observe as bandwidth compression, that wasn't previously apparent. For the case of UGB versus TID Levels in every temperature shown in Figure 4.33b, we can say there is a marginal decrease in UGB scaling with TID levels in each temperature depicted.



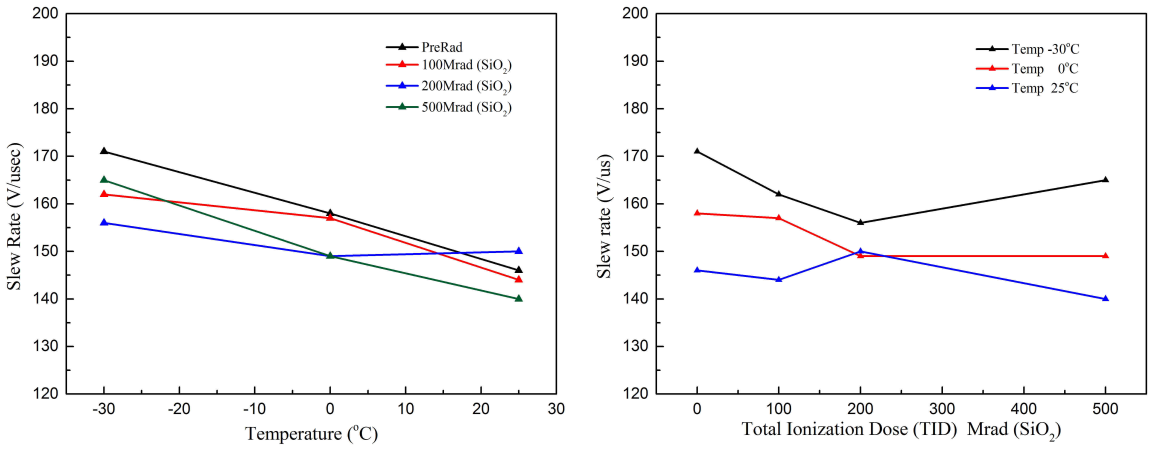
(a) (b)

Figure 4.33: Unity gain bandwidth scaling with (a) Temperature $^o\,C$(b) TID level Mrad(SiO_2)



(a) (b)

Figure 4.34: Phase margin scaling with (a) Temperature $^o\,C$(b) TID level Mrad(SiO_2)

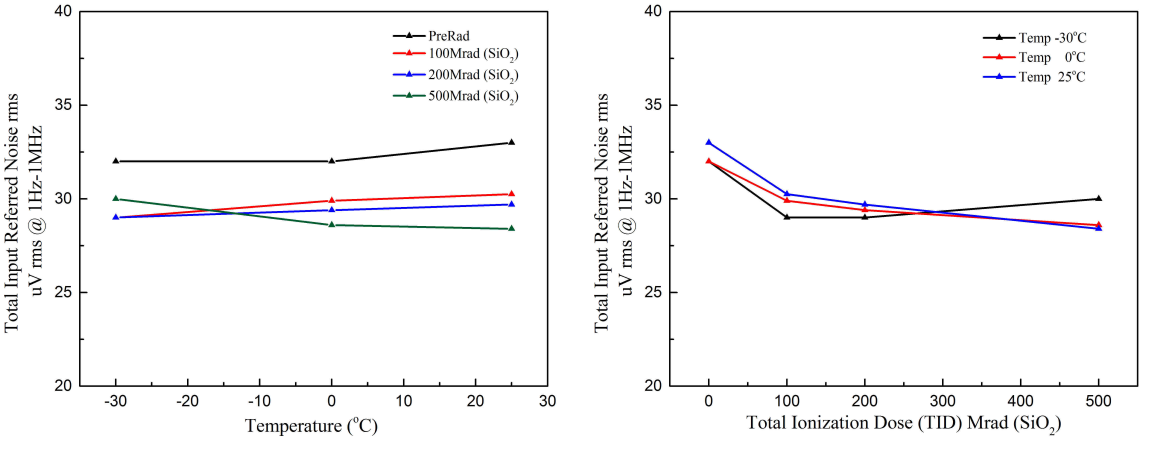


(a) (b)

Figure 4.35: Slew rate scaling with (a) Temperature ^{o}C(b) TID level Mrad(SiO_2)

Figure 4.34a shows the temperature scaling of phase margin. We can see that phase margin remains unchanged with temperature. Figure 4.34b exhibits exactly the same trend but in this case versus TID levels. This proves that FC OTA design is more stable in comparison with the CM OTA, as expected due to robust cascode current mirrors.

In Figure 4.35a, slew rate is presented versus temperature. We can observe that SR degrades with temperature and the decrease is more pronounced for 500 Mrad(SiO_2). In Figure 4.35b, we can observe that as TID level increases for all temperatures SR has marginal fluctuations. At this point we should mention that all simulation results were performed with fixed output load capacitance, C_L. Any possible TID effects on C_L are not accounted for. Finally, in Figure 4.36 total input referred noise we could say that remains unchanged in terms of temperature and for TID levels, too.



(a) (b)

Figure 4.36: Total input referred noise scaling with (a) Temperature ^{o}C(b) TID level Mrad(SiO_2)

Chapter 5

Conclusions

The Design procedure for Both OTAs presented and analyzed, was made possible with the combination of the Dedicated 65 nm CMOS TID-Process Design Kit and the employment of IC design methodology.

On one hand, the Dedicated 65 nm CMOS TID-Process Design Kit provided the opportunity to study the evolution of several critical design parameters under high total ionizing doses, giving the ability to predict the performance degradation of the amplifiers. Embedding of TID effects in device models in TID-PDK enables the in-depth study of the TID effects in any type of circuit using conventional design methods. This leads to unprecedented flexibility for the designers. On the other hand, the IC design methodology aided the design process in terms of time, accuracy and predictability of the design, which would be otherwise a time-consuming, trial and error procedure. The dedicated PDK provides the opportunity to design at specific TID level and temperature, avoiding any speculative or empirical approaches towards the possible degradation in circuits.

In this work we concentrated on TID effects research and all main results and conclusions can not be extended to transient radiation effects (TRE), displacement damage (DD) or single event effects (SEE). In addition, conclusions are reduced to the specific $65\,nm$ foundry process under investigation. In the case of the CM OTA, the design made use of as many different geometries as possible from different bins. This choice was not made solely to prove the functionality of the Dedicated 65 nm CMOS TID-Process Design Kit. This scheme was used as proof of concept for the use of shorter channel length devices that could be used in circuit design for high TID levels. The range of channel lengths used varies between $120\,nm$ and $1\,um$. Furthermore, we have shown that moderate inversion could be used for effective designs under high TID levels and strong inversion could, also, be used under certain conditions, upon design specifications. In both operation regions the variations of parameters such as Early voltage, $g_m/\,I_D$ metric etc shows not significant variation for the geometries selected.

In the case of FC OTA, the design was based on previous knowledge by the CM OTA. Consequently, short channel geometries were used with overall device area such that no significant variation due to TID effects exists. To enhance this scheme, only moderate inversion was used.

This provides us with an important conclusion, which is that the width scaling of design parameters is extremely important for TID immune circuit design. The design with narrow -short devices is not advisable due to excess TID degradation. As long as the device is adequately electrically stable, short channel length can be used.

Both OTAs were proven to be extremely stable. FC OTA was proven to demonstrate better results due to biasing stability provided by the low voltage, cascode current mirror of the input. The design guidelines for both designs, as far as performance characteristics are concerned, are identical for both topologies. Voltage gain shows insignificant changes with temperature for all TID levels but as TID levels increase voltage gain drops. Unity gain bandwidth and slew rate decrease with increasing temperature and increasing TID levels. Power dissipation shows minor fluctuations in both cases, while phase margin demonstrates insignificant fluctuations with a tendency to decrease.

The results presented indicate that by simply providing sufficient margins in design performance criteria, functionality at high TID can be achieved without employing the use of any additional radiation hardening by design (RHBD) techniques.

Chapter 6

Author's Publications

1. A. Nikolaou, L. Chevas, **A. Papadopoulou**, N. Makris, M. Bucher, G. Borghello, F. Faccio, "Forward and Reverse Operation of Enclosed-Gate MOSFETs and Sensitivity to High Total Ionizing Dose.", 25th IEEE Int. Conf. Mixed Design of Integrated Circuits and Systems (MIXDES), pp. 306-309, Rzeszow, Poland, June 21-23, 2018.

2.**A. Papadopoulou**, N. Makris, L. Chevas, A. Nikolaou, M. Bucher, "Design of Micropower Operational Transconductance Amplifiers for High Total Ionizing Dose Effects.", 8th IEEE International Conference on Modern Circuits and System Technologies (MOCAST), Thessaloniki, Greece,13-15 May, 2019.

3. **A. Papadopoulou**, L.Chevas, A.Nikolaou, N. Makris, M.Bucher, "Weak Inversion Ring Oscillator Design Study in 65nm CMOS technology under Total Ionizing Dose Effects", 7th International Conference Micro&Nano 2108, Thessaloniki, Greece, 5-7 November 2018 (poster presentation)

4. A. Nikolaou, M. Bucher, N. Makris, **A. Papadopoulou**, L. Chevas, G. Borghello, H. D. Koch, F. Faccio, "Modeling of High Total Ionizing Dose (TID) Effects for Enclosed Layout Transistors in 65 nm Bulk CMOS", 41th IEEE Int. Semiconductor Conference (CAS2018), Sinaia, Romania, 10-12 Oct, 2018.

5. L. Chevas, A. Nikolaou, M. Bucher, N. Makris, **A. Papadopoulou**, A. Zografos, G. Borghello, H.D. Koch, F. Faccio, "Investigation of scaling and temperature effects in total ionizing dose (TID) experiments in 65nm CMOS", 25th Int. Conf. Mixed Design of Integrated Circuits and Systems (MIXDES), Gdansk, Poland, June 21-23, 2018.

6. A. Nikolaou, M. Bucher, N. Makris, **A. Papadopoulou**, L. Chevas, G. Borghello, H. D. Koch, K. Kloukinas, T. S. Poikela, F. Faccio, "Extending a 65 nm CMOS Process Design Kit for High Total Ionizing Dose Effects", IEEE Int. Conf. on Modern Circuits and Systems Technologies (MOCAST), pp. 1-4, Thessaloniki, Greece, May 7-9, 2018.

7. M. Bucher, A. Nikolaou, **A. Papadopoulou**, N. Makris, L. Chevas, G. Borghello, H. D. Koch, F. Faccio, "Total Ionizing Dose Effects on Analog Performance of 65 nm Bulk CMOS with Enclosed-Gate and Standard Layout", 31st IEEE Int. Conf. on Microelectronic Test

Structures (ICMTS), pp. 1-6, Austin, Texas, Mar. 19-22, 2018.

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Appendix A

SKILL Callback - EG Width

SKILL callback function for controlling the instance value of Enclosed Gate width and producing the prompt messages for illegal values. The minimum and maximum dimensions are used for demonstration and do not correspond to the actual PDK.

```
procedure( MeCallback()

tmpwid = evalstring(cdfgData->w->value);

        if( (tmpwid && (typep(tmpwid)!='flonum))
        then
            artError("Width value must be a floating point number.
              Set to default.\n" );
            cdfgData->w->value = cdfgData->w->defValue;
        );if

        if( (tmpwid < evalstring(cdfgData->w->defValue))
        then
            artError("Width value is less than minimum (2u).
              Setting Width to minimum allowed.\n" );
            cdfgData->w->value = cdfgData->w->defValue;
        );if

        if( (tmpwid > 800e-6)
        then
            artError("Width value exceeds maximum available width
              (800u). Setting width to default .\n");
            cdfgData->w->value = "800u";
        );if

) ;end MeCallback
```

Appendix B

Ocean Script - Extraction of Slope factor n NMOS

Slope factor for NMOSTs is extracted for several geometries and especially for bin crossover geometries. In the following Ocean script slope factor is extracted for 500 Mrad SiO_2 at $0^o C$.

```
Width=list(120e-9 140e-9 180e-9 220e-9 300e-9 320e-9  359e-9 361e-9
  500e-9 599e-9 601e-9 700e-9 800e-9 900e-9 999e-9 1001e-9 4e-6 6e-6
  8e-6 9.999e-6 10.001e-6 19.999e-6 20.001e-6 25e-6 100e-6 500e-6
  800e-6 900e-6)
Len = list( 60e-9 70e-9 80e-9 90e-9 119e-9 121e-9  130e-9 150e-9
  170e-9 190e-9 239e-9 241e-9 260e-9 300e-9 500e-9 700e-9 900e-9
  999e-9 1.001e-6 3e-6 6e-6 8e-6 9.999e-6 10.001e-6 15e-6 16e-6
  18e-6 19e-6 20e-6)

foreach(val1 Width
foreach(val Len
simulator( 'aps )
design("/home/rfic6/simulation/parameter_extraction_nmos/spectre/schematic
  /netlist/netlist")
resultsDir(sprintf(nil
  "/home/rfic6/simulation/parameter_extraction_nmos/spectre/schematic

   /sf_0C_500M/sf_nmos_0C_L=%g_W=%g" val val1))
modelFile(
     '("/home/rfic6/Desktop/T0C_TID500v01.scs" "tt")
     '("/home/rfic6/Desktop/T0C_TID500v01.scs" "stnoise")
)
analysis('dc ?saveOppoint t  ?param "VG"  ?start "0"
                ?stop "1.2"  ?step "30m"  )
```

```
desVar(    "Len" val       )
desVar(    "Width" val1    )
desVar(    "Vd" 1.2        )
desVar(    "VG" 0.15       )
envOption(
        'analysisOrder   list("dc")
)
option( 'temp   "0.0"
)
save( 'i "/M0/D" )
temp( 0.0 )
run()
)
)
win = newWindow()
foreach(val1 Width
my_xv = '()
my_yv = '()
foreach( val Len
openResults( sprintf(nil
 "/home/rfic6/simulation/parameter_extraction_nmos/spectre/schematic/

 sf_0C_500M/sf_nmos_0C_L=%g_W=%g" val val1))
selectResults('dcOp)

my_xv=cons( val my_xv)

slope_factor = (1 / ymax(deriv((ln(IS("/M0/D")) 0.023538))))
 m_yv=cons( slope_factor my_yv)
)
awvPlotList( win list(my_yv)  my_xv )
)
```

Appendix C

11-stage inverter-based ring oscillator (RO)

The Cadence Virtuoso schematic presented below is the RO designed with STD MOSTs.

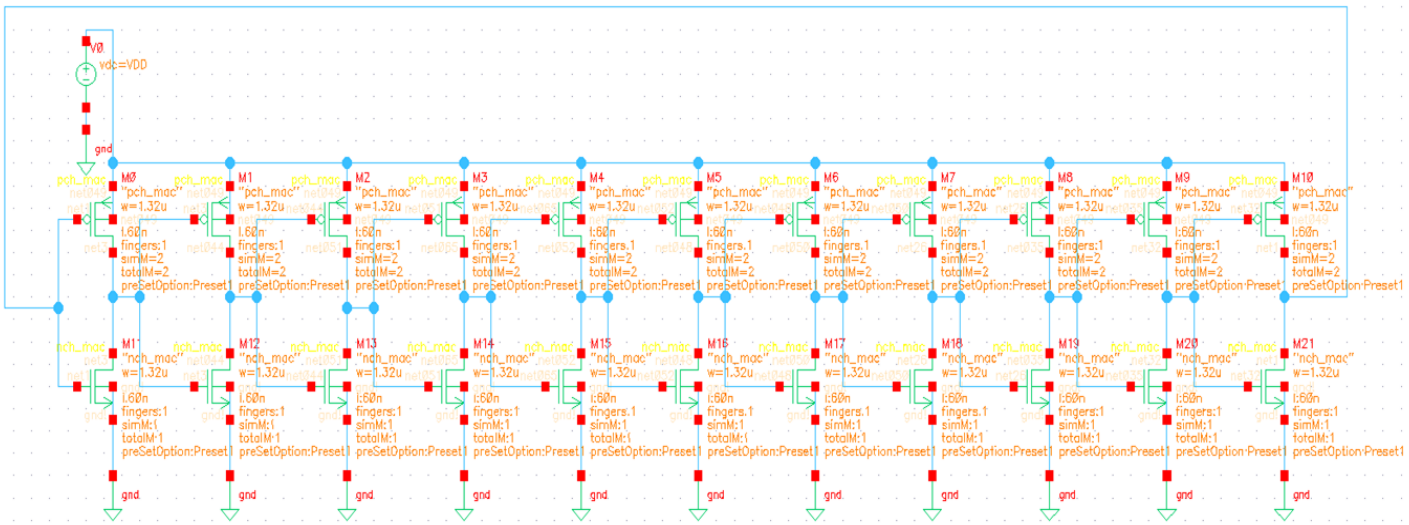

Figure C.1: Ring Oscillator with STD MOSTs