Compact Modeling and Parameter Determination for Junction FETs with Temperature Dependence

Diploma Thesis

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Abstract

In the ever-evolving landscape of semiconductor technology, the n-type Junction Field Effect Transistor (JFET) plays a significant role in a variety of applications. This thesis presents a comprehensive investigation of an n-JFET, specifically focusing on the SK30A model, with a keen emphasis on its temperature-dependent behaviors.

The cornerstone of this study lies in a meticulous characterization of the SK30A n-JFET under diverse temperature conditions, spanning from 25 degrees to 114 degrees Celsius. This approach enabled an in-depth exploration of the temperature-induced effects on the JFET's performance and crucial operational parameters. Specifically, we analyzed how the threshold voltage, drain current, and transconductance are influenced by the fluctuations in temperature, leading to a rich understanding of their intertwined relationships.

In addition, this study conducted an examination of the operational regions of the JFET, specifically the linear and saturation regions, which are pivotal to the design and operation of analog circuits. Furthermore, the sub-threshold and threshold regions were inspected, providing insight into the JFET's transition from the off-state to the on-state, an aspect that plays a critical role in low power applications.

Through this comprehensive analysis, the thesis underscores the profound impact of temperature on the JFET's performance, thereby highlighting the significance of considering temperature variations in the design and application of such devices. These findings foster a holistic understanding of the temperature-sensitive behaviors of n-JFETs, and lay the groundwork for future research and practical applications in the field of electronics.

Ultimately, this thesis illuminates how the interplay of temperature and core operational parameters shapes the performance of an n-JFET, opening up new avenues for refining device efficiency and reliability in a broad range of electronic systems.

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Chapter 1

Introduction

Field-effect transistors (FETs) have been at the core of modern electronic devices, playing a crucial role in the development of integrated circuits and microelectronics. Among the various types of FETs, junction FETs (JFETs) have been a prominent transistor technology, often utilized in analog applications such as amplifiers, oscillators, and filters due to their inherent advantages.

JFETs offer several advantages over other transistor technologies, such as metal-oxide-semiconductor FETs (MOSFETs). JFETs are characterized by their low noise, making them ideal for high-sensitivity applications like instrumentation and audio amplification. The advantage is that at zero Vgs, they are already "on", i.e. they don't need a separate biasing circuit to provide gate voltage. They are also considered to be 'normally-on' devices (depletion mode devices), which can be advantageous in specific circuits, as they do not require a separate biasing circuit for the gate of the transistor. However, they require a negative gate voltage to switch off, which may make their use for digital switching cumbersome. Note that enhancement mode JFETs have also been proposed (with limited voltage range).

This property can help reduce power consumption in certain scenarios.

The study of JFETs remains relevant today due to their unique characteristics and continuous development of new materials, device structures, and manufacturing techniques. An essential facet of JFET study lies in understanding the temperature dependence of various device parameters, crucial for creating robust circuits capable of consistent performance over diverse operating conditions.

Historically, JFETs predate MOSFETs, with the first JFET being developed in the late 1950s, around a decade before the introduction of MOSFETs. JFETs gained significant popularity in the early days of semiconductor technology, as they were less complex to manufacture and had better performance in certain areas compared to MOSFETs. However, with the advancements in MOSFET technol-

ogy and the ever-increasing demand for digital electronics, MOSFETs gradually overtook JFETs in terms of market share.

Despite this shift in the industry, JFETs continue to hold a niche position in the field of analog electronics. Their low noise, high input impedance, and unique voltage-controlled characteristics make them suitable for applications where signal integrity and precise control are of utmost importance. Furthermore, the development of novel materials and device structures, such as double-gate JFETs, has opened up new possibilities for improving the performance of JFETs and expanding their range of applications.

A notable breakthrough in our research is the development and use of the charge- based model. This model grants profound insight into JFET behavior, offering a detailed understanding of device operations under and around the threshold voltage, and analyzing the impact of various parameters on its performance. The model's capacity to portray these operations with high precision makes it an indispensable tool for JFET analysis. An integral part of this research is to observe how the transistor behaves under varying temperatures, an aspect covered extensively in this thesis.

Temperature dependence assumes critical importance in evaluating properties like carrier low-field mobility, intrinsic carrier concentration, and bandgap energy within JFETs. These properties not only vary significantly with temperature but also have substantial implications on the operational behavior of the devices. Understanding and modeling these temperature effects is crucial for predicting and optimizing JFET performance under different environmental conditions.

For instance, the n-channel JFET model from TU GRAZ, although comprehensive for operations above the threshold voltage in both linear and saturation modes, fails to cover what happens below and around the threshold. A more recent contribution in this domain is the model developed at TUC [1], which leverages charge-based modeling and offers the added advantage of covering scenarios even with positive gate voltage (i.e 0.5 V).

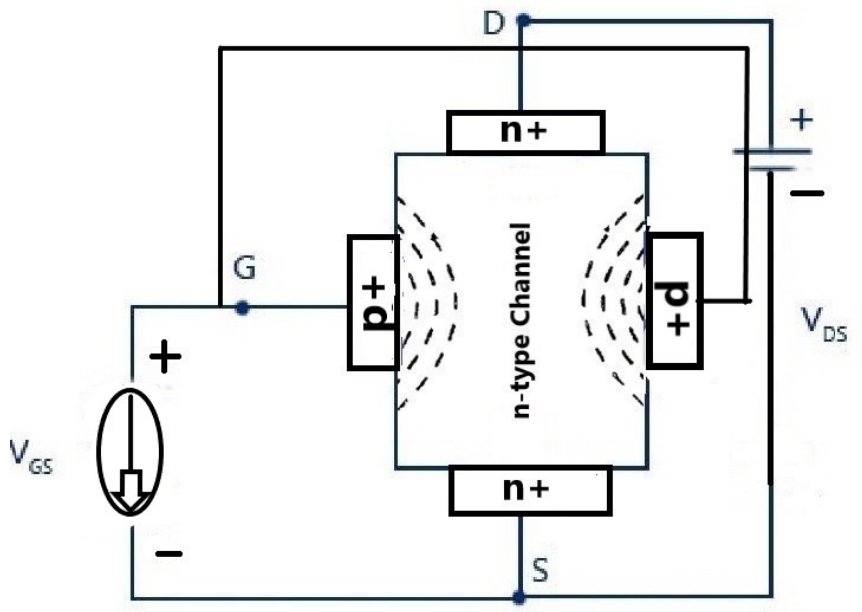
In this thesis, we delve into the complexities of JFETs, focusing on the charge-based model, along with other useful literature, as a key to understanding device behavior and analyzing the impact of various parameters on its performance. By doing that, we managed to have a better understanding of JFET technology and its significance in contemporary electronics.

Chapter 2

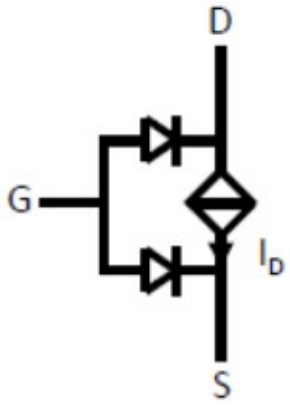
Charge-Based Model of the Junction FET

2.1 Basic n-channel JFET structure and regions of interest

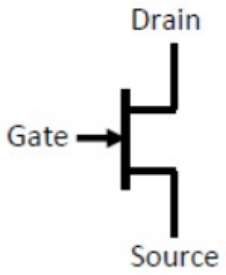
The junction field-effect transistor (JFET) is a fundamental device in the field of microelectronics. In particular, an n-channel JFET consists of an n+-type channel where two regions of highly doped n-type material are diffused, creating the source (S) and drain (D) terminals. The source and drain regions are connected by an n-type channel, which facilitates the flow of electric current.



(a) Representation of an n-channel JFET



(b) Model of a large signal JFET



(c) Circuit symbol of an n-JFET

Figure 2.1: Representation of the structure of an n-channel JFET (a), approximate model of a large signal (b), which includes, channel current source ID, controlled by voltages Vgs, Vds, and diodes between gate and channel. Normally this diode is distributed over the entire channel length, and does not exist only at the source and drain. But the figure gives a good basis for explaining what happens to the gate diodes relative to the channel (which are not included in the load model, which only covers the channel ID current. The same symbol and large-signal model is used for single- and double-gate JFETs. Finally, we have the cirvuit symbol for our JFET (c)

The gate is characterized by its ability to control the flow of charge carriers in the n-channel and thus modulate the current flow from source to drain.

In the case of the n-channel JFET, when a voltage is applied between the drain and the source, electrons, which are the majority carriers, flow from the source to the drain through the n-channel. The gate voltage can then be adjusted to control this current flow. A unique property of JFETs is that they are 'normally-on' devices. That is, they require a specific gate voltage, typically negative for n-channel JFETs, to switch off or reduce the current flow.

The fabrication material for the semiconductor is usually silicon, due to its optimal properties and compatibility with the established manufacturing processes in the semiconductor industry.

Contrastingly, a p-channel JFET has the opposite construction, with the main body being a p-type semiconductor and the source and drain regions being p+-type. In this configuration, holes are the majority carriers, and they flow from the source to the drain when a voltage is applied.
In this thesis, our primary focus lay on the linear and saturation modes of a Junction Field-Effect Transistor (JFET). Nonetheless, we also achieved comprehensive understanding of the other operating regions.

The sub-threshold region, where the JFET operates below the threshold voltage, is of significant interest. In this region, the gate voltage V_G is less than the threshold voltage V_{th}, and the drain current I_D is exponentially dependent on the gate voltage. The drain current in this region is minimal, primarily due to diffusion rather than drift. This region is paramount for low-power applications, where power consumption minimization is necessary.

We also investigated the threshold region. This region indicates the JFET's operational mode when the gate voltage V_G is near the threshold voltage V_{th}. It signifies the transition of the JFET from the off-state (sub-threshold) to the on-state (linear or saturation).

Our focus then shifted to the linear region. This state of operation depicts the JFET's behavior similar to that of a resistor, the value of which can be controlled by adjusting the gate-source voltage V_G. As V_G increases, the channel narrows, effectively increasing the 'resistance', thereby reducing the drain current I_D for a given drain-source voltage V_{DS}. Conversely, as V_G decreases (moves closer to the source potential), the channel widens, decreasing the 'resistance', and thereby increasing the drain current I_D for a given V_{DS}.

Lastly, the saturation region, which was the region from which we extracted our parameters, was examined. In the saturation region, the drain current I_D reaches its maximum value and essentially becomes independent of the drain-source voltage V_{DS}, provided that the gate-source voltage V_G is held constant. In this state, the channel has been 'pinched-off', rendering the JFET fully 'on' or conducting.

The saturation region is particularly relevant for analog applications such as amplification, where the transistor's ability to modulate the drain current I_D us-

ing the gate-source voltage V_G is critical. In this region, the JFET exhibits high input impedance and is capable of providing gain, hence functioning as an effective transconductance device. These attributes, combined with their linear characteristics, render JFETs a desirable choice for various applications in amplification and switching circuits.

2.2 Basic effects modeled

The Charge-based model includes modelling of the following physical effects:

- Threshold voltage V_{th}: The threshold voltage V_{th}= V_{bi} - V_p is a function of the built-in voltage and the pinch-off voltage. The built-in voltage depends on the work function of the gate to channel material, meaning that it depends on gate doping N_A and channel doping N_D. The pinch-off voltage depends on the channel doping and channel thickness, meaning that it depends on T_{sc} and N_D. Changes in doping leads to different pinch-off voltage, and built-in voltage and ultimately changes threshold voltage. Usual values for threshold voltage are negative for the so-called depletion mode devices.
- Vertical filed effect (Gate control effect): With the usage of the vertical field effect we can control the channel, meaning the depletion regions. This is the voltage applied between the gate and source of the JFET. As V_G decreases towards V_{th}, the depletion region around the gate expands and the channel resistance increases, causing the channel to close around threshold voltage.
- Lateral field effect (Drain control effect): The lateral field effect is responsible for the creation of the drift and diffusion current. We use the term diffusion current for low level, and drift current for high level. We reach saturation when VD_{sat}= V_G - $V_{th} > 0$. These two effects combined make the transistor operate as field effect device.
- Temperature dependence: The impact of temperature variations on device parameters such as carrier low-field mobility, energy gap, and intrinsic carrier concentration. Here we will notice the device's behavior in four different temperatures, which are 25, 50.5, 77.6 and 114 ° C.

2.3 Basic definitions

At this point its very useful to define some basic parameters that are being used throughout all of the equations listed below. These are:

$$q = 1.602 \times 10^{-19}\ [\mathrm{C}] \quad \textit{Magnitude of electron charge} \tag{2.1}$$

$$k = 1.3807 \times 10^{-23}\ [\mathrm{JK}^{-1}] \quad \textit{Boltzmann Constant} \tag{2.2}$$

$$T_{ref} = 300 \text{ [K]} \quad \textit{Reference Temperature} \tag{2.3}$$

$$U_T = \frac{kT}{q} \quad \textit{Thermal Voltage} \tag{2.4}$$

$$\varepsilon_{sc} = \varepsilon_r \times \varepsilon_0 \quad \textit{Semiconductor permittivity} \tag{2.5}$$

2.3.1 Voltages applied to JFET

The basic voltages applied to a JFET are the gate-to-source voltage (V_{GS}), the drain-to-source voltage (V_{DS}). These voltages are crucial in controlling the current flow in the device and determining the operating region of the JFET.

- V_{GS}: The gate-to-source voltage controls the depletion region width of the JFET and determines whether the device is in the on or off state. A more negative V_{GS} narrows the channel, reducing the current flow, while a more positive V_{GS} widens the channel, allowing for more current flow.
- V_{DS}: The drain-to-source voltage is the voltage difference between the drain and source terminals. This voltage determines the current flow through the channel and influences the JFET's operating region (cutoff, triode, or saturation).

2.3.2 Threshold voltage

$$V_{th} \cong V_{bi} - V_p. \tag{2.6}$$

The threshold voltage is the gate-to-source voltage at which the JFET channel begins to conduct. For a JFET to be in the on-state, the gate-to-source voltage must be greater than the threshold voltage.

2.3.3 Pinch-off voltage

$$V_p = \frac{Q_f^2}{b} = \frac{qT_{sc}^2 N_d}{8\varepsilon_{sc}} \tag{2.7}$$

The Q_f term is for the total charge of the channel, or else the fixed charge, and its described as: $Q_f = qT_{sc}N_D$

2.3.4 Built-in potential

$$V_{bi} = U_T \ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{2.8}$$

The built-in potential is the potential difference between the p-type and n-type sides of the junction at equilibrium. It results from the difference in work functions between the gate and channel materials and determines the width of the depletion region.

2.4 Descriptive model equations

2.4.1 Total charge density

$$\begin{aligned} Q_{sc} = Q_f + Q_m &= \sqrt{b(\Psi_o - \Psi_s)} \Leftrightarrow \\ Q_f q_{sc} = Q_f(1 + q_m) &= \sqrt{bU_T(\psi_o - \psi_s)} \Leftrightarrow \\ q_{sc} = 1 + q_m &= \sqrt{\frac{\psi_o - \psi_s}{v_p}} \end{aligned} \tag{2.9}$$

Where $q_{sc} = Q_{sc}/Q_f$ is the normalized total local charge ranging from 1 (deep depletion) to 0 (flat band condition), q_m is the normalized mobile charge ranging from 0 (deep depletion) to -1 (flat band condition), ψ_0 and ψ_s are the normalized potentials at the center of the channel and at the interface between the channel and the gate, respectively, and $v_p = v_p/U_T$ is the normalized pinch-off voltage.

2.4.2 Lambert W function

$$L_W(z) \cong \ln(1+z)\left(1 - \frac{\ln\left(1 + \ln(1+z)\right)}{2 + \ln(1+z)}\right) \tag{2.10}$$

This is our basic formula which will help us solve the charge-based model.Our most descriptive equation needs to be in a format that can be solved by Lambert.

2.4.3 Potentials at the center of the channel and at the interface between the channel and the gate

$$\begin{aligned} \Psi_o =& \Psi_s + V_p - U_T L_W\left(v_{ni} e^{(\psi_s + v_p - v)}\right) \Leftrightarrow \\ \psi_o =& \psi_s + v_p - L_W\left(v_{ni} e^{(\psi_s + v_p - v)}\right) \end{aligned} \tag{2.11}$$

2.4.4 Mobile charge

$$\begin{aligned} V_g - V - V_{bi} =& -\frac{Q_{sc}^2}{b} + U_T \ln\left(-\frac{Q_{sc}^2}{Q_f^2} + 1\right) \Leftrightarrow \\ U_T\left(v_g - v - v_{bi}\right) =& -\frac{Q_f^2}{b} q_{sc}^2 + U_T \ln\left(-\frac{Q_f^2 q_{sc}^2}{Q_f^2} + 1\right) \Leftrightarrow \\ v_g - v - v_{bi} =& -v_p q_{sc}^2 + \ln\left(-q_{sc}^2 + 1\right) \end{aligned} \tag{2.12}$$

This is the relationship between voltage and fixed charge.

2.4.5 Charge-Voltage relationship

$$v_g - v - v_{bi} + v_p = -v_p q_m(q_m + 2) + \ln\left(-q_m(q_m + 2)\right) \tag{2.13}$$

Upon substituting $q_{sc} = q_m + 1$, (2.12) may be rewritten as above. This is the equation that we solve with the help of Lambert. We need to be able to have our voltages as input and from there solving this equation, to solve for the charge and then we can calculate current. This is the relationship between voltage and mobile charge.

2.4.6 Drain current

The derivative of (2.13) in normalized quantities is expressed as,

$$dv = \left[2v_p\left(q_m + 1\right) - \frac{2\left(q_m + 1\right)}{q_m\left(q_m + 2\right)}\right] dq_m \tag{2.14}$$

The first term of the right hand side of (2.14) is the drift term and the second is the diffusion term.
The drain current is obtained by integrating the mobile charge along the channel:

$$I_{ds} = -\mu\frac{W}{L}\int_{V_s}^{V_d} Q_m dv = -\mu\frac{W}{L}\int_{v_s}^{v_d} Q_f q_m U_T dv \tag{2.15}$$

$$= -I_{spec}\int_{v_s}^{v_d} q_m dv. \tag{2.16}$$

Substituting dv in (2.18) with (2.14) and integrating, the current becomes,

$$I_{ds} = I_{spec}\,(i_{ms} - i_{md}) \tag{2.17}$$
$$i_{ds} = i_{ms} - i_{md} \tag{2.18}$$

where I_{spec} is the specific current,and its described by: $I_{spec} = (\mu \frac{W}{L} Q_f U_T)$

2.4.7 Normalized current

With i_m being evaluated at source and drain,

$$i_m = \frac{2}{3} v_p q_m^3 + v_p q_m^2 - 2q_m + 2ln(q_m + 2) \tag{2.19}$$

Interestingly, we note that the diffusion term in (2.14) tends to $1/q_m$ when $q_m \to 0$. So, (2.14) becomes,

$$dv \cong \left[2v_p\,(q_m + 1) - \frac{1}{q_m} \right] dq_m \tag{2.20}$$

Performing the integration in (2.16) using (2.20), i_m is approximated as,

$$i_m \cong \frac{2}{3} v_p q_m^3 + v_p q_m^2 - q_m \tag{2.21}$$

Note: The drain current obtained using (2.21) instead of (2.29) deviates less than 1% in all regions of operation (sub- to above- threshold and linear to saturation) which fully justifies this simplification.

2.4.8 Solving the charge-voltage relationship using Lambert function

We start with the equation (2.13):

$$v_g - v - v_{bi} + v_p = -v_p q_m (q_m + 2) + \ln\left(-q_m (q_m + 2)\right)$$

We first define a new variable a as:

$$a = -q_m (q_m + 2) \tag{2.22}$$

Substituting this in the above equation, we get:

$$v_g - v - v_{b_i} + v_p = v_p \cdot \alpha + \ln(a) \tag{2.23}$$

Taking the exponent of both sides, we get:

$$e^{v_g - v - v_{b_i} + v_p} = a \cdot e^{v_p \cdot \alpha} \tag{2.24}$$

Multiplying both sides by v_p, we get:

$$v_p \cdot e^{v_g - v - v_{b_i} + v_p} = a \cdot v_p \cdot e^{v_p \cdot \alpha} \tag{2.25}$$

Defining a new function f as:

$$f(x) = x \cdot e^{v_p \cdot \alpha} \tag{2.26}$$

We can rewrite the above equation as:

$$av_p = f^{-1}\left(f(av_p)\right) = f^{-1}(v_p e^{v_g - v - v_{b_i} + v_p}) \tag{2.27}$$

Using the Lambert W function, we get:

$$av_p = \mathrm{L_w}(v_p e^{v_g - v - v_{b_i} + v_p}) \tag{2.28}$$

Substituting the value of a, we get:

$$-v_p q_m(q_m + 2) = \mathrm{L_w}(v_p \cdot e^{v_g - v - v_{b_i} + v_p}) \tag{2.29}$$

We can simplify this further by using equation (2.6):

$$q_m^2 + 2q_m = -\frac{1}{v_p}\,\mathrm{L_w}(v_p e^{v_g - v - v_{th}}) \tag{2.30}$$

Finally, we can rewrite this equation as a quadratic equation in q_m as:

$$q_m^2 + 2q_m + \frac{1}{v_p}\,\mathrm{L_w}(v_p e^{v_g - v - v_{th}}) = 0 \tag{2.31}$$

Note: This is the desired equation
Solutions to this are:

$$q_m = -1 - \sqrt{1 - \frac{1}{v_p}\,\mathrm{L_w}(v_p e^{v_g - v - v_{th}})} \tag{2.32}$$

and

$$q_m = -1 + \sqrt{1 - \frac{1}{v_p}\,\mathrm{L_w}(v_p e^{v_g - v - v_{th}})} \tag{2.33}$$

As acceptable solution we pick the one that states: $-1 < q_m < 0$. We do the same procedure as before for both source and drain, so we calculate L_{ws}, L_{wd}, q_{ms}, q_{md}, i_{ms}, i_{md} respectively.

2.5 Temperature Dependence

2.5.1 Energy gap

The energy gap is the energy difference between the valence band and the conduction band in a material. In simple terms, it represents the energy required to excite an electron from the valence band (where it is bound to an atom) to the conduction band (where it is free to move and contribute to electrical conduction).

As the temperature increases, the energy gap decreases slightly due to thermal expansion effects. This dependency can affect the behavior of JFETs and other semiconductor devices.

$E_g(T)$ can be expressed as:

$$E_g(T) = E_g(0) - \frac{\alpha_{\mathrm{temp}} T^2}{T + \beta_{\mathrm{temp}}} \tag{2.34}$$

where $E_g(0)$ is the energy gap at absolute zero temperature. For silicon, $E_g(0) = 1.12$ eV, $\alpha_{\mathrm{temp}} = 4.73 \times 10^{-4}$ eV/K^2, and $\beta_{\mathrm{temp}} = 636$ K.

2.5.2 Intrinsic carrier concentration

The intrinsic carrier concentration, n_i, is temperature-dependent and varies with temperature. As temperature increases, the number of thermally generated carriers also increases, leading to an increase in n_i. The temperature dependence of n_i is typically modeled by the following equation:

$$n_i = \sqrt{N_c N_v \left(\frac{T}{300}\right)^3} \exp\left(\frac{-E_g}{2k_B T}\right) \tag{2.35}$$

where T is the temperature in Kelvin, E_g is the bandgap energy in electron volts (eV), k_B is the Boltzmann constant in joules per Kelvin (J/K), N_c is the effective density of states in the conduction band, and N_v is the effective density of states in the valence band. At $T_{\text{ref}} = 300\,\text{K}$, $N_c = 2.78 \times 10^{19}\,\text{cm}^{-3}$ and $N_v = 9.84 \times 10^{18}\,\text{cm}^{-3}$.

NAME	DESCRIPTION	UNITS	RANGE
U_T	Thermal Voltage	V	-
N_c	Conduction Band Effective Density of States	m^{-3}	>0
N_v	Valence Band Effective Density of States	m^{-3}	>0
$\mu_0(T)$	Carrier Low-Field Mobility	m^2 / Vs	-
$n_i(T)$	Intrinsic Carrier Concentration	m^{-3}	>0
E_g	Energy Gap	eV	>0

Table 2.1: Temperature Related Parameters

2.5.3 Carrier low-field mobility(μ)

The carrier low-field mobility depends on temperature change. The mobility of carriers in a semiconductor material is affected by various scattering mechanisms, which in turn depend on temperature. At high temperatures, the scattering mechanisms become more prominent, resulting in a decrease in carrier mobility. On the other hand, at low temperatures, the scattering mechanisms become less prominent, resulting in an increase in carrier mobility. Therefore, the low field mobility of carriers in a semiconductor material varies with temperature.

The equation used to describe carrier low-field mobility is the following:

$$\mu(T) = \mu_0 \left(\frac{T}{T_{nom}}\right)^{-a} \tag{2.36}$$

where μ_0 is the carrier low-field mobility at the reference temperature T_{norm}, and a is the temperature coefficient.

We are given the values of μ_0, and a in the paper by J.M.Dorkel and PH.Leturcq[2], for lowly-doped silicon JFETs, where μ_0=800 at T_{ref}=300 K and a=1.9. Mobility of the semiconductor is also dependent on the doping and increases with increased doping as described in [3].

2.5.4 Field dependent mobility

$$\mu_{\text{eff}} = \frac{\mu(T)}{1 + \theta \cdot |q_G|}$$

where θ is the parameter for field-dependent mobility reduction. We calculate q_G as following:

$$q_G = \frac{Q_G}{-w \cdot L \cdot Q_f} = \frac{d+e}{e+f}$$

We further analyze d, e, f with the following formulas:

$$\begin{aligned} d &= 3\left[q_{md}^3 + q_{md}^2 \cdot q_{ms} + q_{md} \cdot q_{ms}^2 + q_{ms}^3\right], \\ e &= 4\left[q_{md}^2 + q_{md} \cdot q_{ms} + q_{ms}^2\right], \\ f &= 6\left[q_{md} + q_{ms}\right], \\ q_G \text{ in saturation} &= -\frac{q_{ms}\left(3 \cdot q_{ms} + 4\right)}{4 \cdot q_{ms} + 6}, \\ q_G \text{ in linear mode} &= -q_{ms} \end{aligned}$$

The above expression constitutes a simple way to consistently model a reduction of mobility at higher charge conditions to account for a non-ideal behavior. Total gate charge q_G is indicative of the vertical field (single-gate channel) accounting for mobile charge dependence along the channel. Note that the model is consistent with series-connected devices.

This field dependent mobility μ_{eff} will replace mobility in 2.36, where $I_{spec} = \mu \frac{W}{L} Q_f U_T$

Chapter 3

Modelling Approach

3.1 Device under test and measurements

Within the context of this thesis, an n-JFET, specifically the widely used SK30A model, is employed, presenting a unique challenge in acquiring temperature-dependent characterization. In this regard, special recognition is extended to Nikos Makris for his invaluable assistance in measuring the device and extracting the experimental data utilized throughout this project.

The measurements of the JFET were conducted using a bespoke setup that included a range of specialized tools:

- A shielded RF probe station (Cascade Microsystems 10000) equipped with a thermal chuck.
- Temptronic TP03000A temperature controller.
- A specially designed setup to accommodate the packaged JFET on the chuck.
- HP 4142B DC Parameter Analyzer equipped with four SMUs (source-measurement units) and Kelvin-type force-sense cabling.
- IC-CAP measurement software, developed by Keysight.

During the course of this project, the JFET is subjected to measurements across a range of gate voltage values, spanning from 0.2 Volts down to -2 Volts (VG = 0.2, 0, -0.2, -0.4, -0.6, -0.8, -1, -1.2, -1.4, -1.6, -1.8, -2 V). Additionally, the drain voltage values are explored from linear to saturation regions, encompassing VD = 0.05, 0.2, 0.5, 1, 1.5, 2, 2.5, and 5 V.

3.2 I/V characteristics

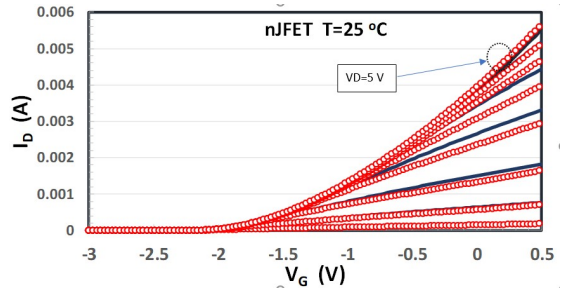
In this section typical I-V characteristics , of an n-type JFET , are presented. Because the device we used is a factory device we had to make assumptions for

basic values, for our data to fit the model at the best of our abilities. In the following table i demonstrate the values we used for the characterizations that follow.

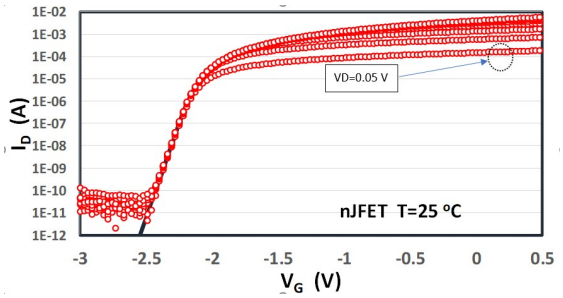
NAME	DESCRIPTION	VALUE	UNITS
W	Channel Width	3.9×10^{-5}	m
L	Channel Length	1×10^{-6}	m
T_{sc}	Channel Thickness	600×10^{-9}	m
N_D	Channel Doping Concentration	4.43×10^{16}	cm^{-3}
N_A	Gate Doping Concentration	2×10^{19}	cm^{-3}
$\mu(T)$	Carrier low-field mobility at T = 25° C	800	m^2 / Vs
θ	Field-dependent mobility reduction	1.76	-
α_{temp}	Temperature coefficient	1.9	-

Table 3.1: Parameters estimated to fit our data

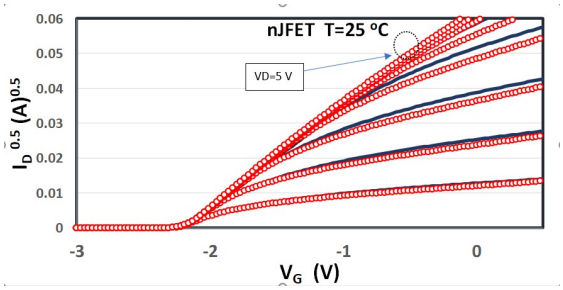
Figure 3.1 (a, b, and c) presents the comparison between measured and modeled I_D versus V_G characteristics across various Drain Voltages from linear to saturation mode ($V_D = 0.05$, 0.2, 0.5, 1, 1.5, 2, 2.5, and 5 V) at at temperature of $T = 25°$ C (298.15 K).
Figure 3.2 (a, b, and c) illustrates the measured and modeled I_D versus V_G characteristics at a temperature of $T = 50.5°$ C (323.65 K).
Figure 3.3 (a, b, and c) showcases the measured and modeled I_D versus V_G characteristics at a temperature of $T = 77.6°$ C (350.75 K).
Figure 3.4 (a, b, and c) exhibits the measured and modeled I_D versus V_G characteristics at a temperature of $T = 114°$ C (387.15 K).



(a) $I_D - V_G$

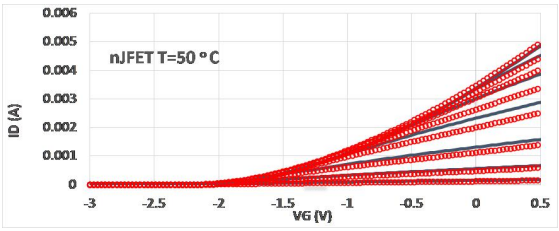


(b) $logI_D - V_G$

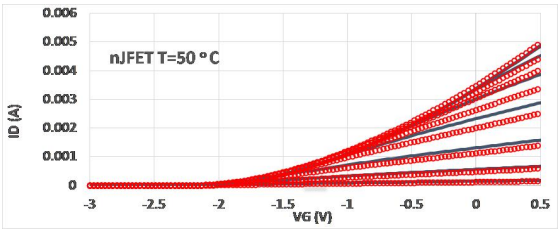


(c) $\sqrt{I_D} - V_G$

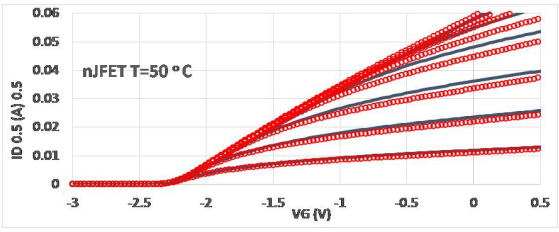
Figure 3.1: Typical I_D-V_G characteristics of an n-JFET for all drain voltages from linear to saturation modes ($V_D = 0.05$ V-$V_D = 5$ V) . Drain current is depicted in both linear (a) and logarithmic scale (b), as well as a square root (c). All graphs are for a temperature of 25° C (298.15 K). Measurements: markers. Model:lines.



(a) $I_D - V_G$

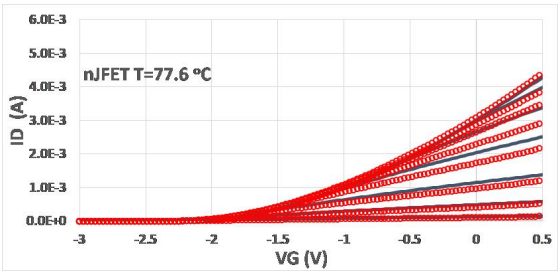


(b) $logI_D - V_G$

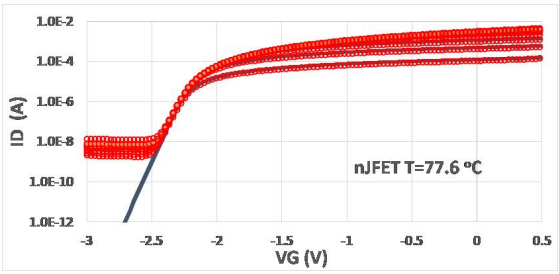


(c) $\sqrt{I_D} - V_G$

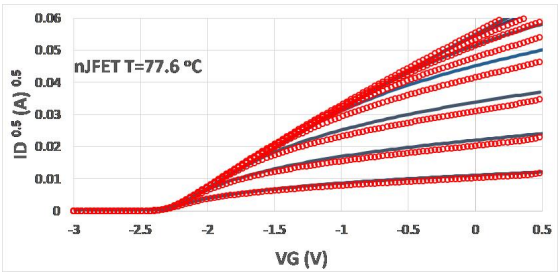
Figure 3.2: Typical I_D-V_G characteristics of an n-JFET for all drain voltages from linear to saturation modes (V_D = 0.05 V-V_D = 5 V) . Drain current is depicted in both linear (a) and logarithmic scale (b), as well as a square root (c). All graphs are for a temperature of 50.5° C (323.65 K). Measurements: markers. Model:lines.



(a) $I_D - V_G$

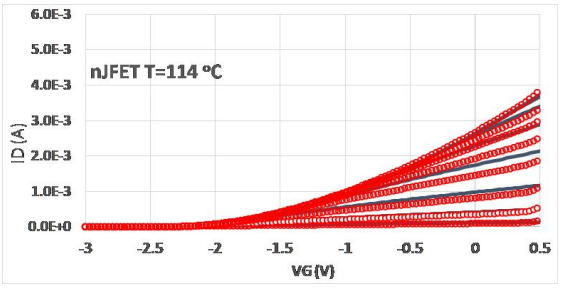


(b) $logI_D - V_G$

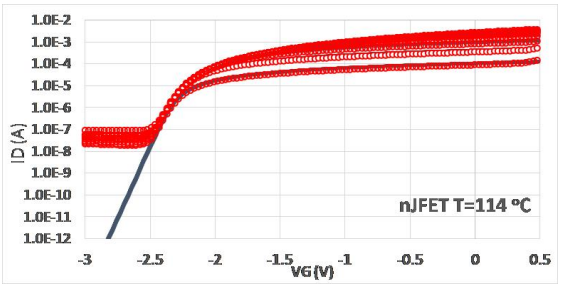


(c) $\sqrt{I_D} - V_G$

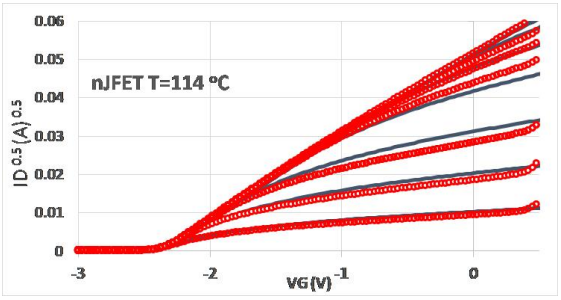
Figure 3.3: Typical I_D-V_G characteristics of an n-JFET for all drain voltages from linear to saturation modes (V_D = 0.05 V-V_D = 5 V) . Drain current is depicted in both linear (a) and logarithmic scale (b), as well as a square root (c). All graphs are for a temperature of 77.6° C (350.75 K). Measurements: markers. Model:lines.



(a) $I_D - V_G$



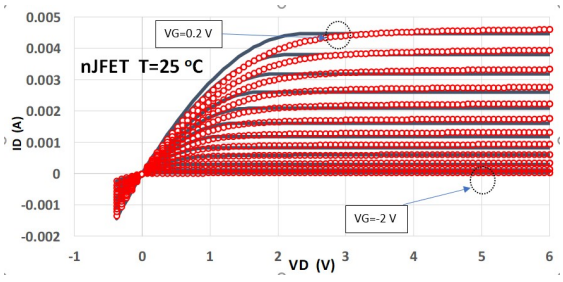
(b) $logI_D - V_G$



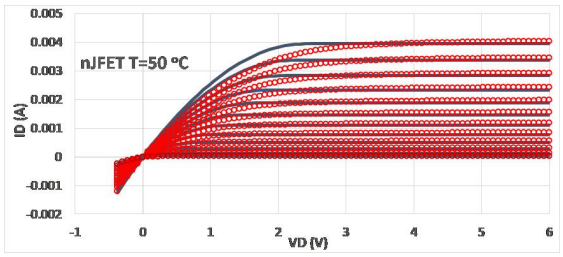
(c) $\sqrt{I_D} - V_G$

Figure 3.4: I_D-V_G characteristics of an n-JFET for all drain voltages from linear to saturation modes ($V_D = 0.05$ V-$V_D = 5$ V) . Drain current is depicted in both linear (a) and logarithmic scale (b), as well as a square root (c). All graphs are for a temperature of 114° C (387.15 K). Measurements: markers. Model:lines.

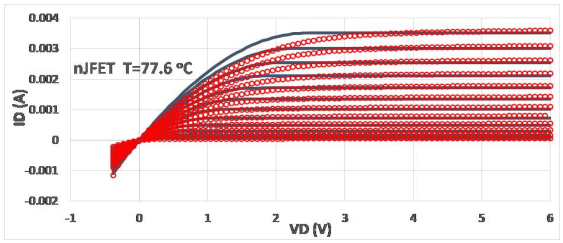
Figure 3.5 presents the measured and modeled characteristics of I_D versus V_D for various Gate Voltages, including both positive and negative values (-2, -1.8, -1.6, -1.4, -1.2, -1, -0.8, -0.6, -0.4, -0.2, 0, 0.2). These measurements were conducted at different temperatures: $T = 25°$ C (298.15 K) (a), 50.5° C (323.65 K) (b), 77.6° C (350.75 K) (c), and 114° C (387.15 K) (d).



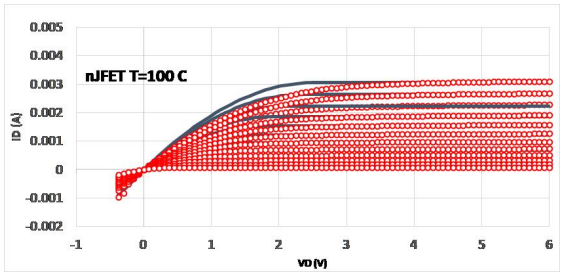
(a) I_D-V_D, $T = 25°$ C (298.15 K)



(b) I_D-V_D, $T = 50°$ C (323.65 K)



(c) I_D-V_D, $T = 77.6°$ C (350.75 K)



(d) I_D-V_D, $T = 114°$ C (387.15 K)

Figure 3.5: Typical I_D-V_D characteristics of an n-JFET for all gate voltages. Drain current is depicted in linear scale. Measurements: markers. Model:lines.

3.3 Transconductances

The transconductance-to-current ratio($G_m \cdot U_T/I_D$), stands as a significant metric in evaluating the efficiency of a semiconductor device, particularly in generating transconductance given a specific current. This ratio is an essential parameter in analog circuit design, providing a quantifiable means to assess the performance and efficiency of the device.

Transconductance, symbolized as G_m, is a vital parameter inherent to Field-Effect Transistors (FETs), inclusive of Junction Field-Effect Transistors (JFETs). It essentially quantifies the sensitivity of the output current to changes in the input voltage, given that all other conditions remain constant. Within the context of JFET operation, transconductance illustrates the variations in drain current resultant from modifications in the gate-source voltage.

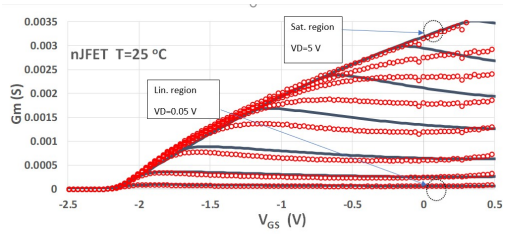
The graphical representation of transconductance versus gate-source voltage (G_m-V_G) is essential as it shows the responsiveness of the device to input voltage alterations.
A higher value of transconductance denotes a more responsive or sensitive device. This property is particularly advantageous in amplification applications, where the amplification factor bears a direct relation to the transconductance.

Transconductance, for both measurements and model is calculated as the derivative of Drain Current divided by the derivative of Gate Voltage which is constant throughout all the Drain Voltages.The unit for G_m is Siemens (S). The dimensionless parameter $G_m \cdot U_T/I_D$ is calculated from the average transconductance value ((G_m) extracted from both our measurementsa and our model multiplied with the thermal voltage(Ut) for each temperature, divided with the normalized current.
Next we display the formula for transconductance for both gate and drain.

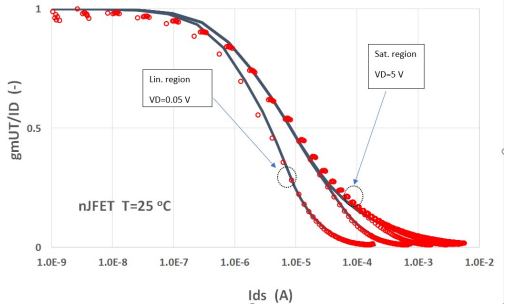
$$G_m = \frac{d(ID)}{d(Vg)} \tag{3.1}$$

$$GD_s = \frac{d(ID)}{d(V_D)} \tag{3.2}$$

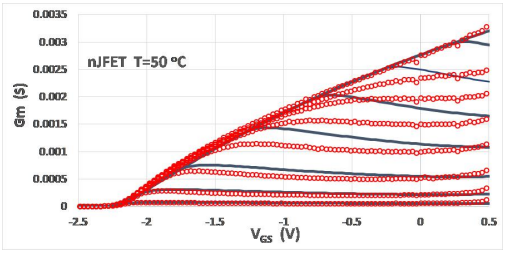
Figure 3.6 presents the transistor operating in both linear (V_D= 0.05 V) and saturation mode (V_D=5 V), including the all the interim values of (V_D).



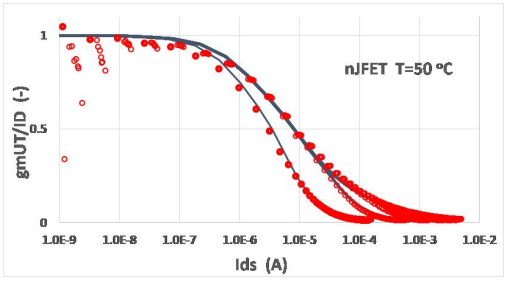
(a) G_m-V_G, $T = 25°$ C (298.15 K)



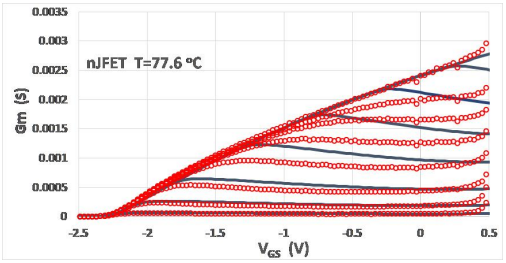
(b) $G_m \cdot U_T/I_D$, $T = 25°$ C (298.15 K)



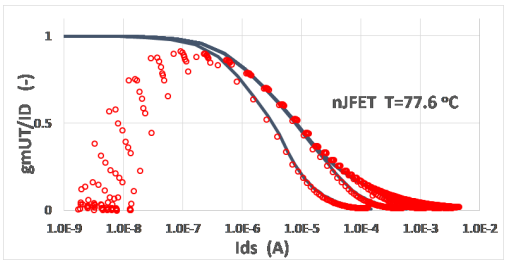
(c) G_m-V_G, $T = 50°$ C (323.65 K)



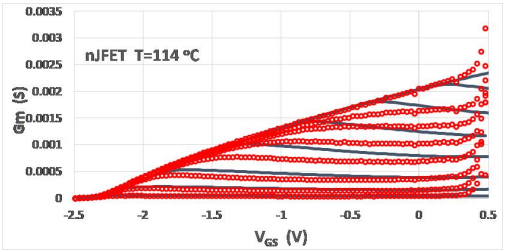
(d) $G_m \cdot U_T/I_D$,$T = 50°$ C (323.65 K)



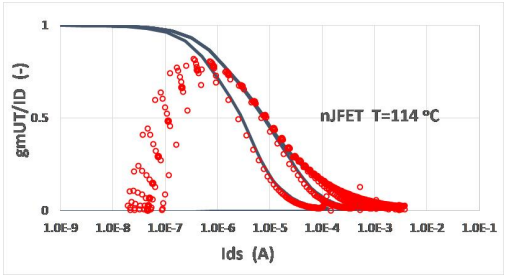
(e) G_m-V_G, $T = 77.6°$ C (350.75 K)



(f) $G_m \cdot U_T/I_D$, $T = 77.6°$ C (350.75 K)



(g) G_m-V_G, $T = 114°$ C (387.15 K)



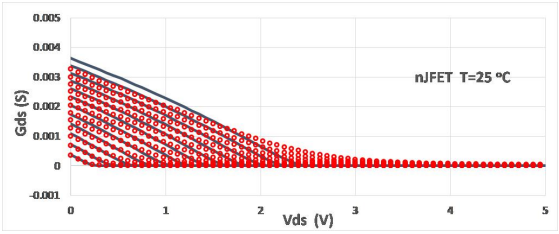
(h) $G_m \cdot U_T/I_D$, $T = 114°$ C (387.15 K)

Figure 3.6: Gate transconductance G_m vs. gate voltage V_G (a,c,e,g) and normalized gate transconductance-to-current ratio vs. Drain current(b,d,f,h). Measurements: markers. Model:lines.

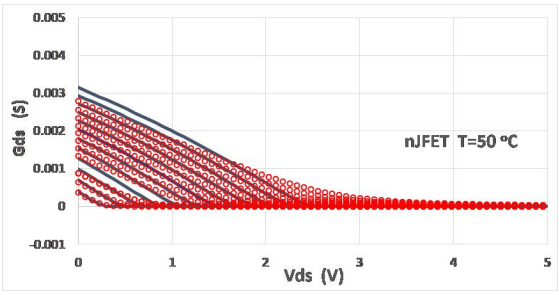
Note: In analyzing the above diagrams, a notable observation emerges when examining the ratio of $G_m \cdot U_T/I_D$ with respect to increasing temperature. While our model exhibits ideal behavior, the collected data deviates from the expected model response. This discrepancy is attributed to the presence of leakage current, which serves as an indication of gate leakage. The leakage current commences at a relatively low level of approximately 80 pA and progressively escalates to 2 nA and 20 nA as the temperature rises. We see the reverse-biased junction leakage in $I_D - V_G$ at very low current levels, which increases with temperature. This is a limitation of the device, not the model. Our model simply does not cover junction leakage, either forward- or reverse-biased.

The same holds for the forward-biased junction at high V_G. At increased temperature, the forward-biased junction starts to show leakage, which again is not covered in the present model.

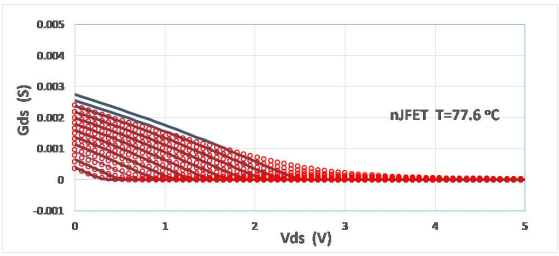
Now, on the other hand, the G_{ds}-V_D graph explores the output conductance, represented as 'G_{ds},' against the drain voltage (V_D), as we can see on Figure 3.7. Output conductance is the reciprocal of the output resistance, and in the context of a JFET, it pertains to changes in drain current (Id) relative to changes in drain-source voltage (V_D). A lower output conductance is often desired for voltage amplification applications since it signifies a more stable output current against changes in the output voltage.



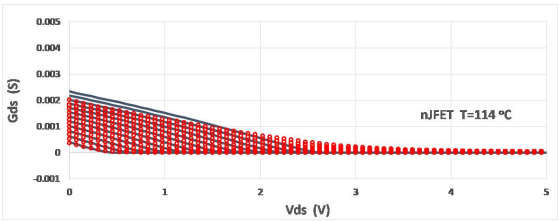
(a) G_{DS}-V_{DS}, $T = 25^{\circ}$ C (298.15 K)



(b) G_{DS}-V_{DS}, $T = 50^{\circ}$ C (323.65 K)



(c) G_{DS}-V_{DS}, $T = 77.6^{\circ}$ C (350.75 K)



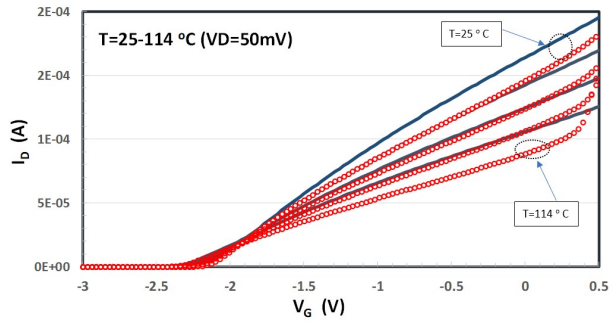
(d) G_{DS}-V_{DS}, $T = 114^{\circ}$ (387.15 K)

Figure 3.7: Typical G_{DS}-V_{DS} characteristics of an n-JFET for all gate voltages ($V_G = 0.2$ V,.., $V_G = -2$ V) . Measurements: markers. Model:lines.

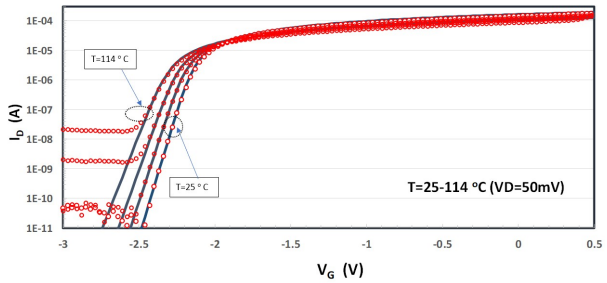
3.4 Temperature dependence

One great aspect of our thesis is how our device would operate in different enviromental conditions. In this section, we will observe how our transistor behaves throughout all the different temperatures in both linear and saturation mode. Firstly we will depict how the n-JFET operates in linear mode below and around threshold.

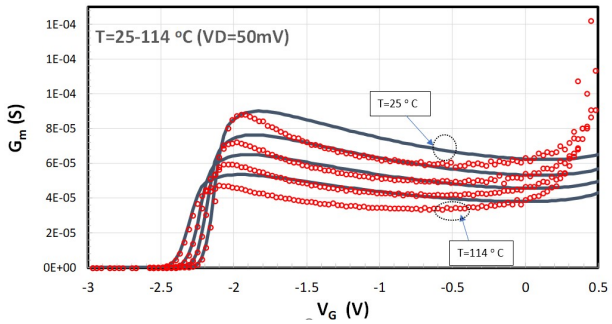
Figure 3.8 shows drain current versus gate voltage in both linear (a), and logarithmic scale (b), across the range of temperatures, while (c) demonstrates the transconductance in terms of V_G.



(a) $I_D - V_G$



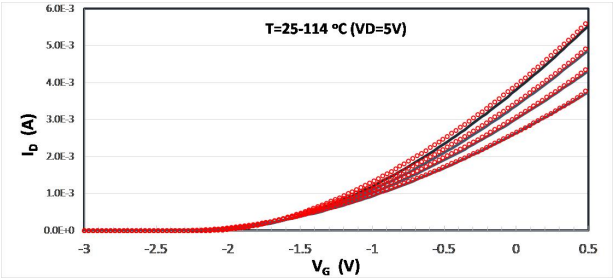
(b) $logI_D - V_G$



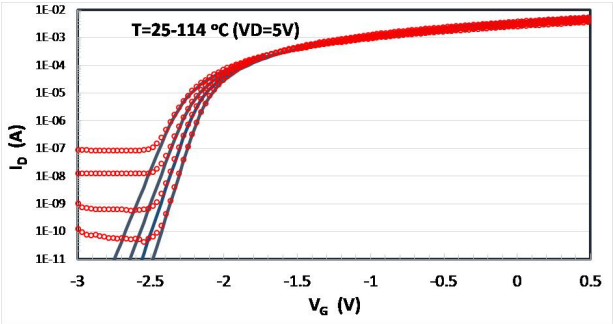
(c) G_M- V_G

Figure 3.8: I_D-V_G characteristics across the spectrum of temperatures in linear mode($V_D = 0.05$ V). Drain current is depicted in both linear (a) and logarithmic scale (b). We also demonstrate transconductance over V_G . Measurements: markers. Model: lines.

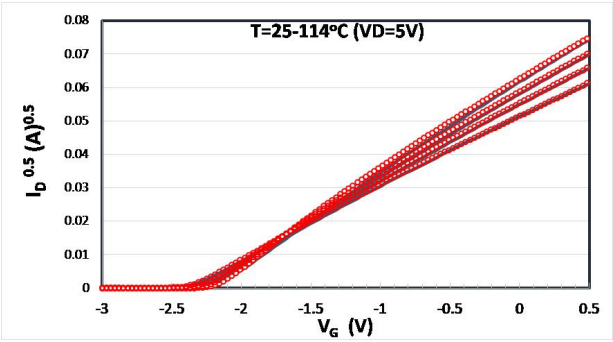
Next we will record the transistor's behavior in the saturation region. Figure 3.9 shows the current in saturation ($V_D = 5$ V),in linear (a) and logarithmic scale (b), as well as the square root of the current (c) in terms of V_G.



(a) $I_D - V_G$



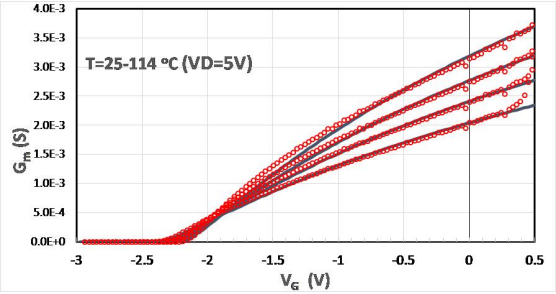
(b) $logI_D - V_G$



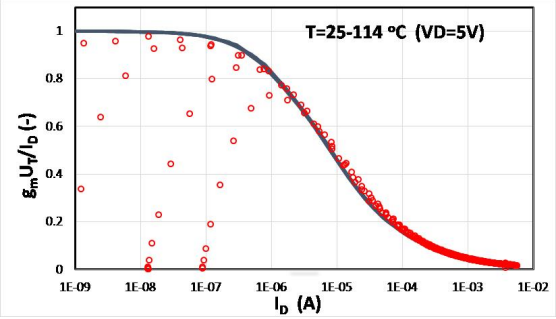
(c) $\sqrt{I_D} - V_G$

Figure 3.9: I_D-V_G characteristics across the spectrum of temperatures in saturation mode (V_D = 5 V). Drain current is depicted in linear (a) and logarithmic scale (b). We also demonstrate the $\sqrt{I_D}$ over V_G. Measurements: markers. Model:lines.

Next we will show the transconductance to gate voltage and the ratio $G_m \cdot U_T/I_D$ in saturation for all our temperatures.



(a) $G_M - V_G$



(b) $logI_D - V_G$

Figure 3.10: Typical $G_M - V_G$ of an n-JFET for all temperatures(a). The ratio $G_m \cdot U_T/I_D$ over V_G across all values of temperature (b). Measurements: markers. Model:lines.

3.5 Parameter extraction

In this section we will explain and provide context on how we extracted Threshold Voltage as well as the mobility for our device across our range of temperatures.

3.5.1 Threshold Voltage

In saturation we can calculate threshold voltage as following:

$$\begin{aligned} \frac{G_m U_T}{I_{ds}} &= \frac{G_{spec} U_T}{I_{spec}} \frac{g_m}{i_{ds}} = \frac{g_m}{i_{ds}} \\ &= \frac{1}{1 - v_p \left(\frac{2}{3} \left(q_{ms}^2 + q_{ms} q_{md} + q_{md}^2 \right) + q_{ms} + q_{md} \right)} \end{aligned} \tag{3.3}$$

In saturation, the drain side is considered fully depleted, so $q_{md} \approx 0$, (3.3) becomes:

$$\left. \frac{g_m}{i_{ds}} \right|_{sat} = \frac{1}{1 - v_p \left((2/3) q_{ms}^2 + q_{ms} \right)} \tag{3.4}$$

In saturation and at that point, only the first-order mobile charge term in (3.4) is important and setting $qm, \mathrm{th} = -\frac{1}{vp}$, we obtain:

$$\left.\frac{g_m}{i_{ds}}\right|_{v_{th}} \cong \frac{1}{1 - v_p q_{ms,th}} = \frac{1}{2} \tag{3.5}$$

This particular condition, $gm/ids \approx 1/2$, corresponds to the threshold condition. Therefore, we will create the following diagram, which is Figure 3.11, and we will depict $G_m \cdot U_T/I_D$ versus V_G. At the point where $G_m \cdot U_T/I_D$ =1/2 we will find the corresponding Gate Voltage for both our model and our data.

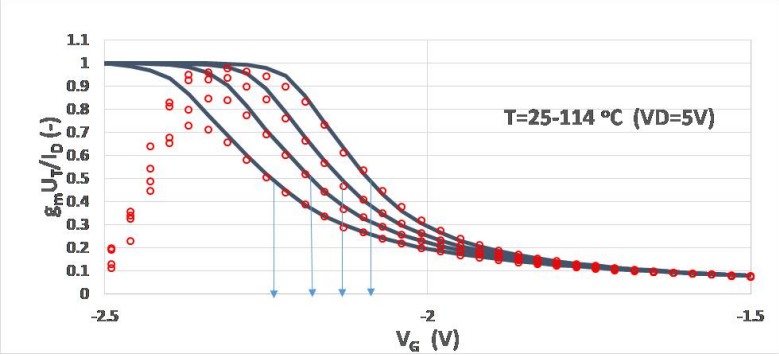


Figure 3.11: $G_m \cdot U_T/I_D$ versus V_G

After we pinpoint the gate voltage that corresponds to this value of $Gm \cdot UT/I_D$, we interpolate between the lower and higher value to obtain threshold voltage. The formula for the interpolation is the following:

$$V_{\mathrm{th}} = V_{\mathrm{g\_2}} + \left(\frac{1/2 - \mathrm{gmUt/Id\_2}}{\mathrm{gmUt/Id\_1} - \mathrm{gmUt/Id\_2}}\right) \cdot (V_{\mathrm{g\_1}} - V_{\mathrm{g\_2}}) \tag{3.6}$$

We do the same for all the different temperatures and we come up with the diagram below:

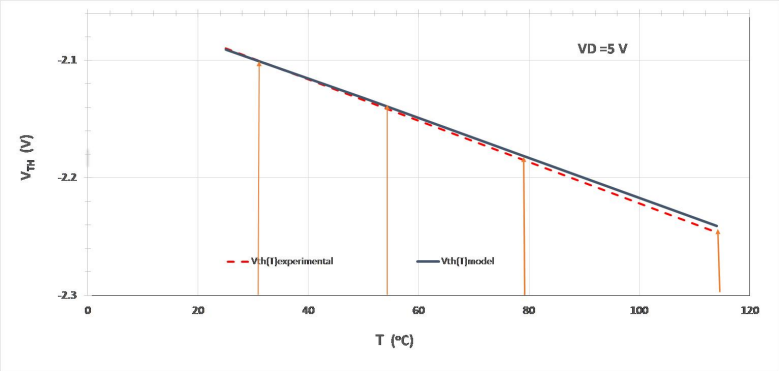


Figure 3.12: V_{th} versus T

What we can observe from the diagram is that V_{th} decreases as the temperature rises. It changes with temperature due to the increase in the intrinsic carrier concentration (number of free electrons and holes) in the semiconductor. As temperature rises, more electron-hole pairs are thermally generated, and hence impacts the threshold voltage.

As the temperature rises, we have a lower energy barrier for electrons to cross from the source to the channel, effectively reducing the threshold voltage.

This temperature dependence of the threshold voltage is a critical aspect of FET behavior and must be taken into account in the design and analysis of electronic devices, particularly for devices operating in environments with large temperature variations.

3.5.2 Carrier low-field mobility

The change of carrier low-field mobility with increasing temperature is a critical factor in the performance of electronic devices, as it impacts device parameters like threshold voltage, transconductance, and drain current, among others.

We will extract mobility from the $d(I_D^{0.5})/d(V_G)$ diagram which is the following:

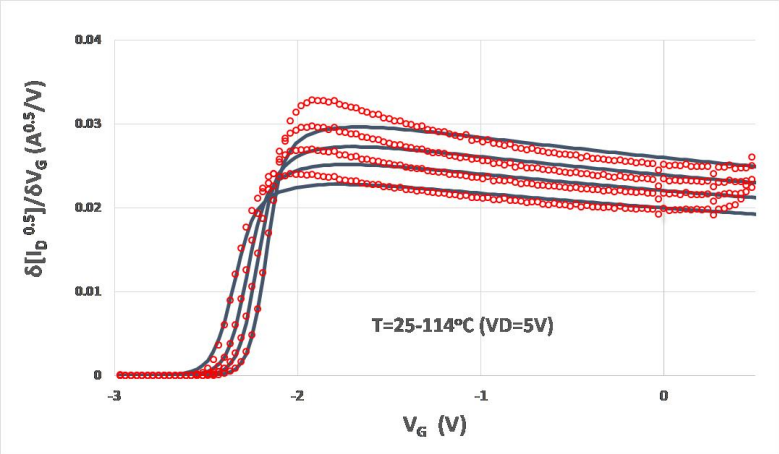


Figure 3.13: $d(I_D^{0.5})/d(V_G)$, in saturation for all temperatures

First, we will find the value of A at gate voltage of $V_G = V_{\text{th}} + 1$ for both our model and data. Next, mobility can be derived from the following formula: $\mu = \frac{A^2}{2\left(\frac{\varepsilon_{\text{SC}}}{T_{\text{SC}}}\right)\frac{W}{L}}$.

Finally, we can obtain the mobility versus temperature, and we depict it here:

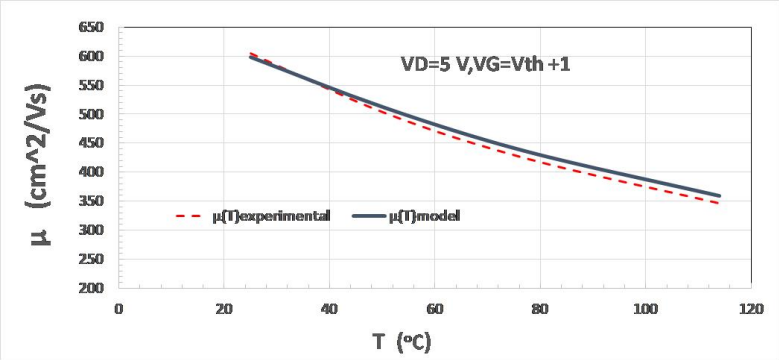


Figure 3.14: $\mu(T)$ versus T, in saturation for all temperatures, at V_G= V_{th} +1

Chapter 4

Conclusions and future work

This thesis presented a detailed analysis and characterization of the n-JFET, specifically the widely utilized SK30A model, considering various temperature conditions. The development and application of an analytical model was a crucial point of this work, successfully predicting the JFET's behavior across a broad temperature spectrum. The model's successful alignment with experimental data, particularly within the linear and saturation regions of operation, confirmed its robustness and predictive reliability.

Notably, this study unveiled the impact of temperature on essential parameters such as the threshold voltage, drain current, and transconductance. These phenomena are of immense importance when designing JFET-based circuits for environments with broad temperature ranges.

However, the model as developed in this thesis is based on analytical equations and would require conversion to Verilog-A based code for execution in circuit simulators. This would then be recognized as a compact model. It is noteworthy that this conversion process is straightforward and would greatly enhance the usability of the model in practical electronic system design.

Furthermore, both transcapacitances and noise aspects have been developed analytically. For transcapacitances, an analytical model for total node charges exists, and additional temperature effects do not need to be considered since they are adequately covered in the DC model. The same holds true for the thermal noise model. Inclusion of these aspects would greatly enrich the comprehensiveness of the model.

Lastly, a discussion on parasitic effects, primarily the gate-to-channel leakage, was included in this work. This aspect emerged as a significant limiting factor at high temperatures. Moreover, it might also be beneficial to consider the effect of series resistance at the source and drain, in future iterations of the model.

Experimental data as a function of temperature would be required to validate the considerations above. Future works could focus on the generation and utilization of such data for model validation and refinement. In summary, this thesis

provides a significant contribution to the understanding of temperature-dependent behavior of n-JFETs and paves the way for future research to refine and extend the model for more practical and comprehensive applicability.

While the research conducted in this thesis provides a substantial foundation for understanding the temperature-dependent behavior of n-JFETs, it also reveals several directions for future investigation. The proposed temperature dependence could be implemented in the online tool JFETlab [4],[5],[6],[7] which also is a development of the TUC group.

First, the developed model in its current state is based on analytical equations. To be fully considered as a "compact" model,it needs to be translated into Verilog-A code. Future work could focus on compacting the model, which would facilitate its incorporation into circuit simulators and broaden its applicability in the design of complex electronic systems.

Second, the model could be expanded to include the effects of noise. Noise analysis is a vital aspect of analog circuit design, especially in applications such as amplifiers and oscillators where noise can significantly degrade the performance. Incorporating noise analysis into the model would add an extra dimension to its predictive capabilities, enhancing its utility in practical circuit design.

Lastly, the model could be improved by integrating the consideration of transcapacitances. Transcapacitances play a key role in the dynamic behavior of JFETs, impacting frequency response and transient behavior. Inclusion of transcapacitance effects would therefore provide a more comprehensive picture of the JFET's behavior, especially in AC and transient operation.

In summary, while the developed model provides a solid foundation for understanding the temperature-dependent behaviors of n-JFETs, there is ample scope for its further refinement and extension. The incorporation of these additional factors would significantly enrich the model, making it an even more powerful tool for predicting the performance of n-JFETs under a variety of operating conditions.

Appendix A

Appendix TU Graz

This Appendix presents the classical equations for a double-gate JFET as they are presented in an online tool from Technical University of Graz [1]. Note that these equations are valid for above-threshold operation, and two separate equations are used to describe linear mode and saturation modes of operation.

The expression for the drain current of an n-channel JFET in the linear regime is,

$$I_D = I_p \left[\frac{V_D}{V_p} - \frac{2}{3} \left(\frac{V_{bi} + V_D - V_G}{V_p} \right)^{3/2} + \frac{2}{3} \left(\frac{V_{bi} - V_G}{V_p} \right)^{3/2} \right] \tag{A.1}$$

In the saturation regime, the current is,

$$I_D = I_p \left[\frac{1}{3} - \frac{V_{bi} - V_G}{V_p} + \frac{2}{3} \left(\frac{V_{bi} - V_G}{V_p} \right)^{3/2} \right] \tag{A.2}$$

where,

$$I_p = \frac{\mu_n {N_D}^2 Z e^2 h^3}{2 L \epsilon_r \epsilon_0} \tag{A.3}$$

$$V_p = \frac{e N_D h^2}{2 \epsilon_r \epsilon_0} \tag{A.4}$$

$$e V_{bi} = k_B T \ln \left(\frac{N_A N_D}{{n_i}^2} \right) \tag{A.5}$$

$$n_i = \sqrt{N_c N_v \left(\frac{T}{300} \right)^3} \exp \left(\frac{-E_g}{2 k_B T} \right) \tag{A.6}$$

These expressions are valid assuming that the pn junction is reverse biased. For an n-channel JFET, $V_G < 0$ and $V_D > 0$ in this regime.

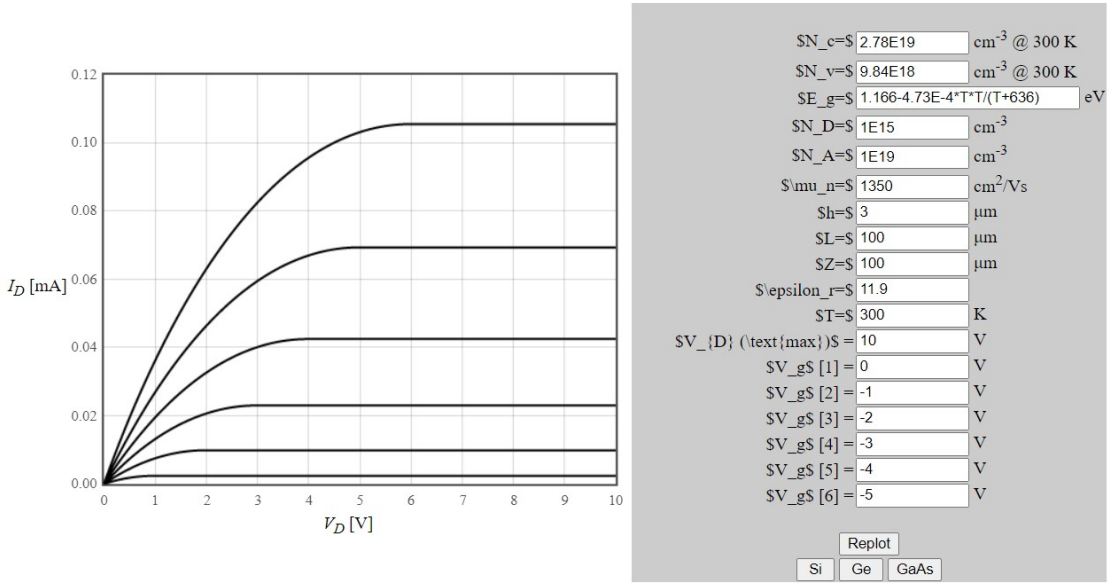


Figure A.1: Output characteristic and parameter table from TU GRAZ fora silicon n-channel JFET.

Note that in the present thesis, the notations used are: $z = W$, $h = T_{sc}$, $\varepsilon_{sc} = \epsilon_r \epsilon_0$, $q = e$, and $I_p = I_{\text{spec}}$.

What is also worth mentioning is the difference between some core variables of our model. V_p as defined here is four times V_p as defined in 2.17. Also, $I_p = I_{\text{spec}} \frac{N_D T_{sc}^2}{U_T 2\varepsilon_{sc}}$.

Based on this, we have the following results for $T = 300$ K:

$E_g = 1.12$ eV, $n_i = 6.41 \times 10^9$ cm^{-3}, $V_{bi} = 0.856$ V, $I_p = 444$ mA, and $V_p = 6.84$ V.

Reference:

[1] PHT.301 Physics of Semiconductor Devices, n-channel JFET, Technical University Graz, Austria. [Online Available:] `https://lampx.tugraz.at/~hadley/psd/L9/njfet.php`

Appendix B

Documentation

The Charge-based Model Equations for Simulation of Double-Gate Junction FETs

Technical Report

B.1 Introduction

The charge-based model is a scalable and compact simulation model built on fundamental physical properties of the n-JFET structure. This report aims to provide a thorough understanding of the charge-based model equations for JFET simulation. The model captures the key physical phenomena governing the operation of these devices, including the effects of temperature, doping, and geometric factors. The charge-based model presented in this documentation is built upon rigorous theoretical foundations, with a focus on accuracy and computational efficiency. It has bee extensively validate against experimental data and TCAD simulations as provided in [2,],[1],[5], demonstrating its suitability for a wide range of applications.

B.2 Geometry related parameters

NAME	DESCRIPTION	UNITS	DEFAULT VALUE
L	Channel Length	um	1
W	Channel Width	um	1
T_{sc}	Channel Thickness	nm	500

Table B.1: Geometry Related Parameters

B.3 Material related parameters

NAME	DESCRIPTION	UNITS	DEFAULT VALUE AT T=300 K
N_D	Channel Doping Concentration	m^{-3}	4.43 $\times 10^{16}$
N_A	Gate Doping Concentration	m^{-3}	2×10^{19}
ε_r	Material Relative Permittivity	-	11.9
β_{temp}	beta(Eg)	K	636
α_{temp}	alpha(Eg)	eV/K	4.73×10^{-4}

Table B.2: Geometry Related Parameters

B.4 Temperature Dependence

NAME	DESCRIPTION	UNITS	DEFAULT VALUE AT T=300 K
U_T	Thermal Voltage	V	0.025
N_c	Conduction Band Effective Density of States	m^{-3}	2.8×10^{19}
N_v	Valence Band Effective Density of States	m^{-3}	9.8×10^{18}
$\mu_0(T)$	Carrier Low Field Mobility	cm^2/Vs	809.45
$n_i(T)$	Intrinsic Carrier Concentration	cm^{-3}	5.51×10^{9}
E_g	Energy Gap	eV	1.12

Table B.3: Geometry Related Parameters

B.4.1 Carrier low-field mobility

$$\mu(T) = \mu_0 \left(\frac{T}{T_{nom}} \right)^a \tag{B.1}$$

where μ_0 is the carrier low-field mobility at the reference temperature T_{nom}, and a is the temperature coefficient.

B.5 Basic Model Equations

B.6 Basic Definitions

$$q = 1.602 \times 10^{-19}\ [\mathrm{C}] \quad \textit{Magnitude of electron charge} \tag{B.2}$$

$$k = 1.3807 \times 10^{-23}\ [\mathrm{JK}^{-1}] \quad \textit{Boltzmann Constant} \tag{B.3}$$

$$T_{ref} = 300\ [\mathrm{K}] \quad \textit{Reference Temperature} \tag{B.4}$$

$$U_T = \frac{kT}{q} \quad \textit{Thermal Voltage} \tag{B.5}$$

$$\varepsilon_{sc} = \varepsilon_r \times \varepsilon_0 \quad \textit{Semiconductor permittivity} \tag{B.6}$$

B.6.1 Gate-source voltage

V_{GS}: The gate-to-source voltage controls the depletion region width of the JFET and determines whether the device is in the on or off state. A more negative V_{GS} narrows the channel, reducing the current flow, while a more positive V_{GS} widens the channel, allowing for more current flow.

B.6.2 Drain-source voltage

V_{DS}: The drain-to-source voltage is the voltage difference between the drain and source terminals. This voltage determines the current flow through the channel and influences the JFET's operating region (cutoff, triode, or saturation).

B.6.3 Pinch-off voltage

$$V_p = \frac{Q_f^2}{b} = \frac{qT_{sc}^2 N_d}{8\varepsilon_{sc}} \tag{B.7}$$

The Q_f term is for the total charge of the channel, or else the fixed charge, and its described as: $Q_f = qT_{sc}N_D$.

B.6.4 Intrinsic carrier concentration

The intrinsic carrier concentration, n_i, is temperature-dependent and varies with temperature. As temperature increases, the number of thermally generated carriers also increases, leading to an increase in n_i. The temperature dependence of n_i is typically modeled by the following equation:

$$n_i = \sqrt{N_c N_v \left(\frac{T}{300}\right)^3} \exp\left(\frac{-E_g}{2k_B T}\right) \tag{B.8}$$

B.6.5 Energy Gap

The $E_g(T)$ can be expressed as:

$$E_g(T) = E_g(0) - \frac{\alpha_{\text{temp}} T^2}{T + \beta_{\text{temp}}} \tag{B.9}$$

where $E_g(0)$ is the energy gap at absolute zero temperature.

B.6.6 Built-in Potential

$$V_{bi} = U_T \ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{B.10}$$

The built-in potential is the potential difference between the p-type and n-type sides of the junction at equilibrium. It results from the difference in work functions between the gate and channel materials and determines the width of the depletion region.

B.6.7 Threshold Voltage

$$V_{th} \cong V_{bi} - V_p. \tag{B.11}$$

The threshold voltage is the gate-to-source voltage at which the JFET channel begins to conduct.

B.7 Descriptive Equations

B.7.1 The total charge density is defined as:

$$\begin{aligned} Q_{sc} = Q_f + Q_m = \sqrt{b(\Psi_o - \Psi_s)} \Leftrightarrow \\ Q_f q_{sc} = Q_f(1 + q_m) = \sqrt{bU_T(\psi_o - \psi_s)} \Leftrightarrow \\ q_{sc} = 1 + q_m = \sqrt{\frac{\psi_o - \psi_s}{v_p}} \end{aligned} \tag{B.12}$$

Where $q_{sc} = Q_{sc}/Q_f$ is the normalized total local charge ranging from 1 (deep depletion) to 0 (flat band condition), q_m is the normalized mobile charge ranging from 0 (deep depletion) to -1 (flat band condition), ψ_0 and ψ_s are the normalized potentials at the center of the channel and at the interface between the channel and the gate, respectively, and $v_p = v_p/U_T$ is the normalized pinch-off voltage.

B.7.2 Potentials at the center of the channel and at the interface between the channel and the gate

$$\begin{aligned} \Psi_o =& \Psi_s + V_p - U_T L_W \left(v_{ni} e^{(\psi_s + v_p - v)}\right) \Leftrightarrow \\ \psi_o =& \psi_s + v_p - L_W \left(v_{ni} e^{(\psi_s + v_p - v)}\right) \end{aligned} \tag{B.13}$$

B.7.3 Mobile charge

$$V_g - V - V_{bi} = -\frac{Q_{sc}^2}{b} + U_T \ln\left(-\frac{Q_{sc}^2}{Q_f^2} + 1\right) \Leftrightarrow \tag{B.14}$$

$$U_T\left(v_g - v - v_{bi}\right) = -\frac{Q_f^2}{b} q_{sc}^2 + U_T \ln\left(-\frac{Q_f^2 q_{sc}^2}{Q_f^2} + 1\right) \Leftrightarrow \tag{B.15}$$

$$v_g - v - v_{bi} = -v_p q_{sc}^2 + \ln\left(-q_{sc}^2 + 1\right) \tag{B.16}$$

B.7.4 Charge-Voltage relationship

$$(v_g - v - v_{bi} + v_p) = (-v_p q_m(q_m + 2) + \ln(-q_m(q_m + 2))) \tag{B.17}$$

B.7.5 Lambert W function

$$L_W(z) \cong \ln(1 + z)\left(1 - \frac{\ln\left(1 + \ln(1 + z)\right)}{2 + \ln(1 + z)}\right) \tag{B.18}$$

This is our basic formula which will help us solve the charge-based model. Our most descriptive equation needs to be in a format that can be solved by Lambert.

B.7.6 Solving the charge-voltage relationship using Lambert function

Solutions to the charge-voltage relationship are:

$$q_m = -1 - \sqrt{1 - \frac{1}{v_p}\,\mathrm{L_w}(v_p e^{v_g - v - v_{th}})} \tag{B.19}$$

and

$$q_m = -1 + \sqrt{1 - \frac{1}{v_p}\,\mathrm{L_w}(v_p e^{v_g - v - v_{th}})} \tag{B.20}$$

We calculate number (18), by keeping $-1 < q_m < 0$. We do the same procedure as before for both source and drain, so we calculate L_{ws}, L_{wd}, q_{ms}, q_{md}, i_{ms}, i_{md} respectively.

B.7.7 Field dependent mobility

$$\mu_{\text{eff}} = \frac{\mu(T)}{1 + \theta \cdot |q_G|}$$

where θ is the parameter for field-dependent mobility reduction. We calculate q_G as following:

$$q_G = \frac{Q_G}{-w \cdot L \cdot Q_f} = \frac{d + e}{e + f}$$

We further analyze d, e, f with the following formulas:

$$\begin{aligned}
d &= 3\left[q_{md}^3 + q_{md}^2 \cdot q_{ms} + q_{md} \cdot q_{ms}^2 + q_{ms}^3\right], \\
e &= 4\left[q_{md}^2 + q_{md} \cdot q_{ms} + q_{ms}^2\right], \\
f &= 6\left[q_{md} + q_{ms}\right], \\
q_G \text{ in saturation} &= -\frac{q_{ms}\,(3 \cdot q_{ms} + 4)}{4 \cdot q_{ms} + 6}, \\
q_G \text{ in linear mode} &= -q_{ms}
\end{aligned}$$

The above expression constitutes a simple way to consistently model a reduction of mobility at higher charge conditions to account for a non-ideal behavior. Total gate charge q_G is indicative of the vertical field (single-gate channel) accounting for mobile charge dependence along the channel. Note that the model is consistent with series-connected devices.

This field dependent mobility μ_{eff} will replace carrier low-field mobility, where $I_{spec} = \mu \frac{W}{L} Q_f U_T$

B.7.8 Drain Current

$$I_{ds} = I_{spec}\,(i_{ms} - i_{md}) \tag{B.21}$$
$$i_{ds} = i_{ms} - i_{md} \tag{B.22}$$

B.7.9 Normalized current

$$i_m \cong \frac{2}{3} v_p q_m^3 + v_p q_m^2 - q_m \tag{B.23}$$

Appendix C

SK30A Toshiba JFET

At the end of this thesis paper we will attach the SK30A dataset of the transistor we have used.

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[7] N. Makris, M. Bucher, L. Chevas, F. Jazaeri, and J.-M. Sallese, "Free carrier mobility, series resistance, and threshold voltage extraction in junction fets," *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4658–4661, 2020.

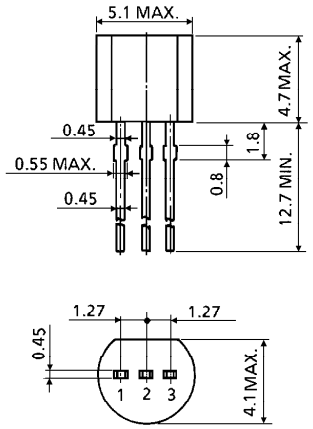
TOSHIBA FIELD EFFECT TRANSISTOR SILICON N CHANNEL JUNCTION TYPE

2SK30ATM

LOW NOISE PRE-AMPLIFIER, TONE CONTROL AMPLIFIER AND DC-AC HIGH INPUT IMPEDANCE AMPLIFIER CIRCUIT APPLICATIONS

- High Breakdown Voltage : $V_{GDS} = -50V$
- High Input Impedance : $I_{GSS} = -1nA$ (Max.) ($V_{GS} = -30V$)
- Low Noise : NF = 0.5dB (Typ.) ($V_{DS} = 15V$, $V_{GS} = 0$, $R_G = 100k\Omega$, f = 120Hz)

Unit in mm



1. SOURCE
2. GATE
3. DRAIN

JEDEC	TO-92
EIAJ	SC-43
TOSHIBA	2-5F1C

Weight : 0.21g (Typ.)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Gate-Drain Voltage	V_{GDS}	−50	V
Gate Current	I_G	10	mA
Drain Power Dissipation	P_D	100	mW
Junction Temperature	T_j	125	°C
Storage Temperature Range	T_{stg}	−55~125	°C

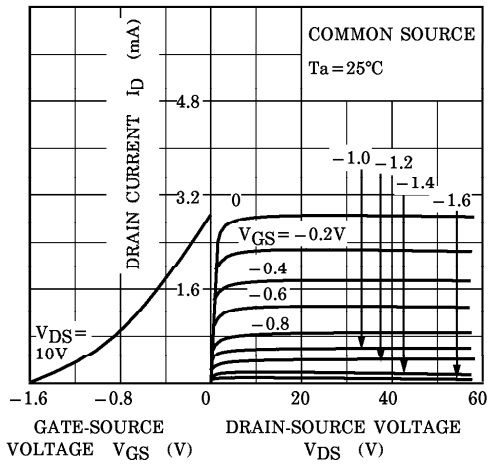
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Cut-off Current	I_{GSS}	$V_{GS} = -30V$, $V_{DS} = 0$	—	—	−1.0	nA
Gate-Drain Breakdown Voltage	$V_{(BR)GDS}$	$V_{DS} = 0$, $I_G = -100\mu A$	−50	—	—	V
Drain Current	I_{DSS} (Note)	$V_{DS} = 10V$, $V_{GS} = 0$	0.3	—	6.5	mA
Gate-Source Cut-off Voltage	$V_{GS(OFF)}$	$V_{DS} = 10V$, $I_D = 0.1\mu A$	−0.4	—	−5.0	V
Forward Transfer Admittance	$\|Y_{fs}\|$	$V_{DS} = 10V$, $V_{GS} = 0$, f = 1kHz	1.2	—	—	mS
Input Capacitance	C_{iss}	$V_{GS} = 0$, $V_{DS} = 0$, f = 1MHz	—	8.2	—	pF
Reverse Transfer Capacitance	C_{rss}	$V_{GD} = -10V$, $V_{DS} = 0$, f = 1MHz	—	2.6	—	pF
Noise Figure	NF	$V_{DS} = 15V$, $V_{GS} = 0$, $R_G = 100k\Omega$, f = 120Hz	—	0.5	5.0	dB

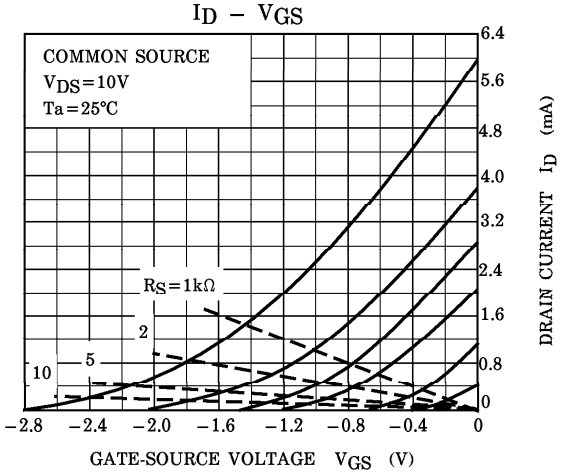
Note : I_{DSS} Classification R : 0.30~0.75, O : 0.60~1.40, Y : 1.20~3.00, GR : 2.60~6.50

961001EAA2

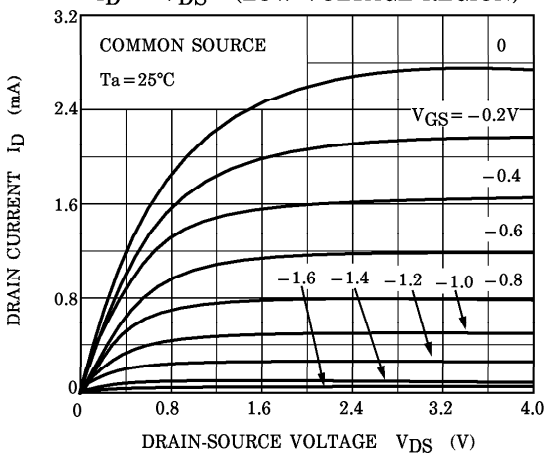
STATIC CHARACTERISTICS



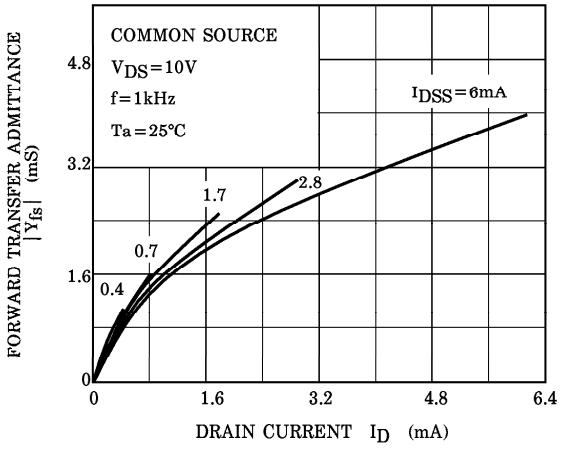
I_D – V_{GS}



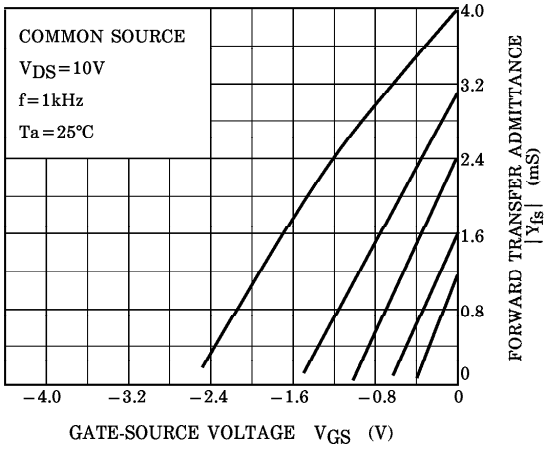
I_D – V_{DS} (LOW VOLTAGE REGION)



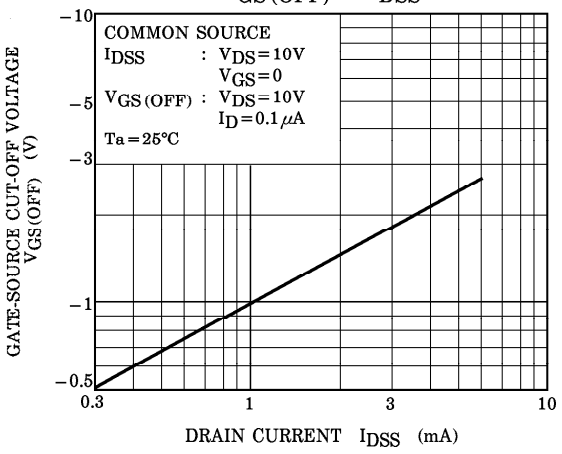
$|Y_{fs}|$ – I_D



$|Y_{fs}|$ – V_{GS}



$V_{GS(OFF)}$ – I_{DSS}



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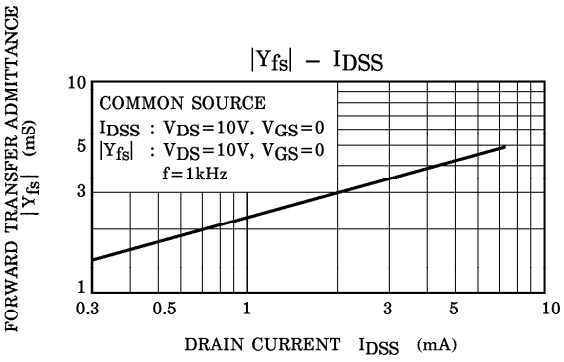
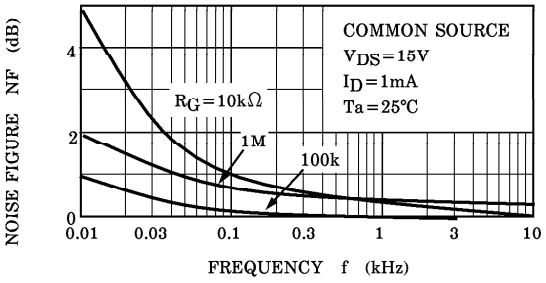
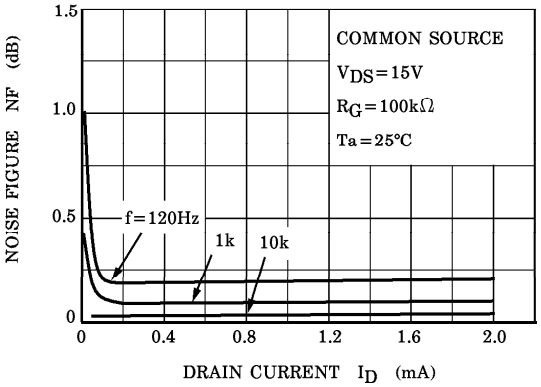
$|Y_{fs}|$ – I_{DSS}



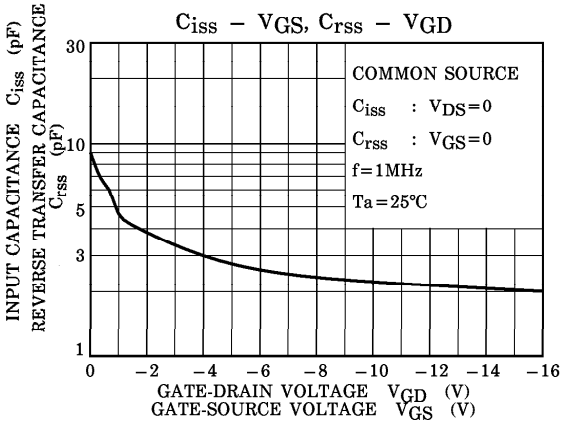
NF – f



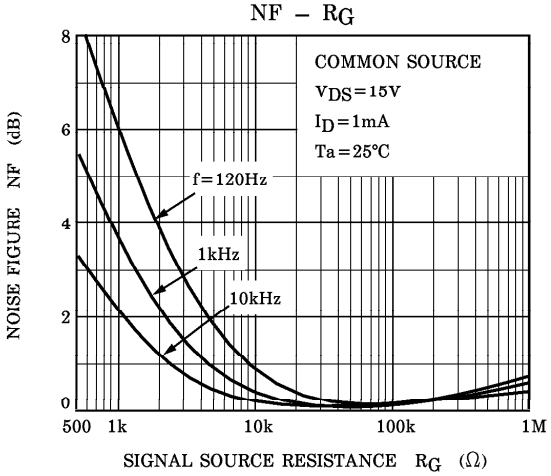
NF – I_D



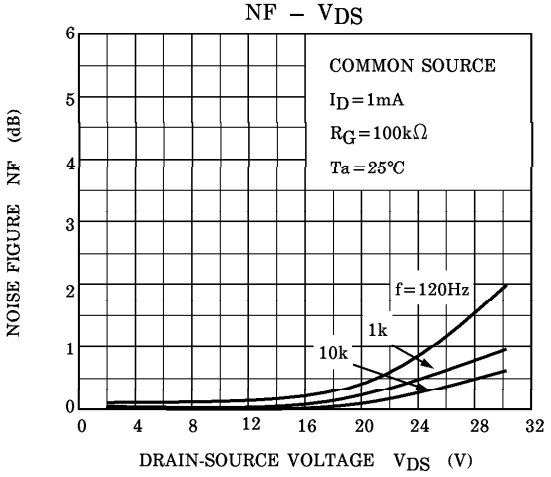
C_{iss} – V_{GS}, C_{rss} – V_{GD}



NF – R_G



NF – V_{DS}



P_D – Ta