Characterization and Modeling of High Total Ionizing Dose Effects and Low Frequency Noise in Standard CMOS Technology

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Abstract

CMOS (Complementary Metal Oxide Semiconductor) technology continues to be the dominant technology for constructing integrated circuits (ICs or chips), presenting advantages such as: reliability low cost, low power consumption and most important scalability. Moore's law, which predicted that the number of devices in a chip will double every 18 to 24 months, fulfilled over the years by scaling down the feature size in CMOS technology. In early CMOS transistors channel length where in micrometer range whereas today the feature size standard bulk CMOS processes is under 65m. Electronics operating in extreme conditions like space environments and high- energy physics (HEP) systems, are expected to present significant performance degradation due to their exposure to ionizing radiation. The forthcoming update of the Large Hadron Collider (LHC) at CERN, aims to increase the rate of collisions (luminosity) by a factor of 10; as a result, electronics in the innermost locations of the detector, closer to the collision sites, are expected to be exposed to a cumulative ionizing dose up to 1Grad. Commercial non radiation-hardened CMOS processes, in 130 or 65nm nodes, because of the thin gate oxides, are proven to be advantageous in suppressing TID related degradation effects. Additionally, MOS transistors with enclosed gate layout, commonly abbreviated as EG MOSFETs, due to the absence of shallow trench isolation (STI) field oxide, are expected to exhibit enhanced resilience to TID effects as well as improved mismatch and low frequency noise characteristics.

Performance in standard CMOS designs can be limited by the presence of Low frequency noise (LFN). $1/f$ and towards ultra deep nano-scale processes RTS (random telegraph signal) noise, are the two basic mechanisms forming the LFN spectrum in lower frequencies. CMOS image sensors, multilevel flash memories and RF Voltage controlled oscillators (VCOs) are some of the designs that are deep affected by the presence of LFN. In the latter, $1/f$ noise is unconverted into phase noise. LFN is related with the trapping detrapping mechanism of free charges at or near the Si/SiO_2 interface. One trap rises a random telegraph signal in time domain which corresponds to a Lorentzian spectrum. A sufficient large uniformed distributed number of traps, will trigger the superposition of several Lorentzian spectra that is perceived as $1/f$ noise. In smaller devices RTS components dominate the LFN PSD.

In the context of this thesis the effect of high TID and LFN on standard bulk CMOS technologies, of 65 and 180nm respectively, will be examined in detail. In both cases, MOS transistors with standard and and enclosed gate layouts will be studied.

1 Introduction

1.1 TID and $1/f$ noise impact on CMOS technology

From MOSFETs to bipolar ICs, oxides and insulators are key components for various number of electronic devices. Electronics in harsh radiation environments, such as space or high-energy particle accelerators, are expected to exhibit significant charge build up to insulator oxides leading to performance degradation and failure. The High-Luminosity Large Hadron Collider (HL-LHC) project at CERN aims to increase the luminosity of the LHC by a factor of 10. Electronics in the innermost locations of the detector, close to the collision point, are expected to be exposed to a cumulative total ionizing dose (TID) of radiation up to 1Grad for 10 years of operation [43]. Advanced bulk CMOS technologies with thinner gate oxides are considered to be more resistant to radiation exposure. Additionally, the use of specific layout techniques, such as enclosed gate (EG) transistors, is proven to be advantageous in suppressing radiation induced effects [67].

Noise is generated in all semiconductor devices and is perceived as spontaneous random fluctuations in current or in voltage. In Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), noise behavior is dominated primarily by two noise sources: thermal noise and low frequency (LFN) or $1/f$ noise. Other noise sources that are sometimes present on the power spectrum of a MOS device are generation-recombination noise or random telegraph signal (RTS) noise and shot noise. RTS noise and $1/f$ noise are the two noise sources that compose the power spectral density of LFN, and they are associated with the trapping detrapping mechanism of free charges at or near the Si/SiO_2 interface. One trap rises a random telegraph signal in time domain which corresponds to a Lorentzian spectrum. A sufficient large uniformed distributed number of traps, will trigger the superposition of several Lorentzian spectra that is perceived as $1/f$ noise [46]. In smaller devices RTS components dominate the LFN PSD. Over the last years the aggressive reduction of the physical size of MOSFETs, established the use of CMOS technology in radio-frequency (RF) and high-speed integrated circuits (ICs). In analog design, noise determines the minimum AC signal that can be processed by an analog circuit whereas in applications like multilevel-shell flash memories, CMOS image sensors and voltage controlled oscillators (VCOs), the impact of RTS noise is crucial.

This thesis provides an extensive analysis, based on characterization and modeling, of hight TID effects and LFN on standard CMOS processes of 65 and 180nm respectively. On both technology nodes, MOSFETs of standard and enclosed gate layout are examined. Both effects are studied with respect to the charge based modeling approach which is an essential tool that can provide both solid understanding and accurate prediction of how ionization after TID exposure and $1/f$ noise mechanisms interact with MOSFETs.

1.2 Thesis structure

The context of this thesis is organized as follows: in current Section a brief introduction about noise impact and total ionizing dose effects on MOS transistor was presented. In Section 2, the basic MOSFETs structure and operation along with the special characteristics of MOSFETs with enclosed gate layout, will be demonstrated. In Section 3, high TID impact on MOS transistors will be discussed in detail. Basic degradation mechanisms that arise after exposure on high doses of ionizing radiation will be discussed in detail. Section 4, the charge base modeling approach of $1/f$ noise will be analyzed thoroughly. Both carrier number fluctuation (ΔN) and mobility fluctuation ($\Delta\mu$) effects forming the LFN spectrum will be expressed with respect to the inversion charge densities ($q_{s,d}$) at the source and drain end of the device channel. Charge based expressions will be used to predict both mean value and variance behavior of LFN in all operating regions, from linear to saturation and all the range from weak to strong inversion. In Section 5, the procedures followed on both TID and LFN experiments will be described in detail. Additionally, results in the form of extracted models versus measured data will be presented in all cases. It should be pointed out that a direct comparison between standard and enclosed gate MOS transistors of the same technology, regarding their performance versus TID and LFN will be provided. Finally in Section 6, conclusions will be drawn.

2 Device structure and physical operation

2.1 Basic MOSFET structure

The MOS transistor is a field effect device, where the current flow in the longitudinal direction, from drain to source terminal in the so called "channel region", is modulated by the voltage applied at the gate. In Figure 2.1 typical structure of an nMOSFET is depicted. The four terminals of a MOSFET are: Gate (G), Source (S), Drain (D) and Body or Bulk (B).

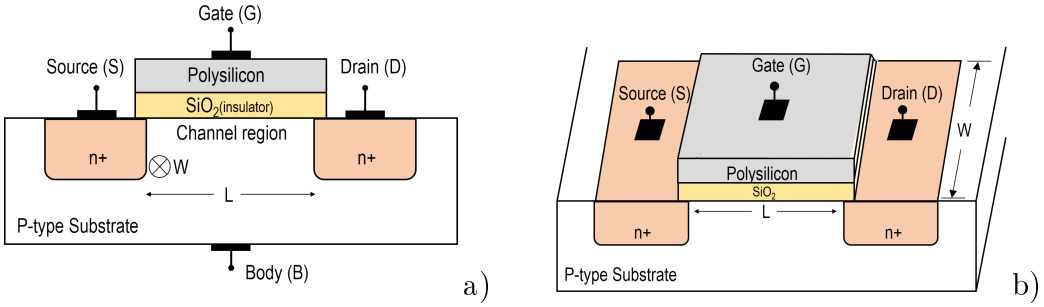


Figure 2.1: Cross-section (a) and 3D representation (b) of an n-type MOS transistor

NMOS transistor is fabricated in a p-type local substrate and consists of two highly doped n-type diffusion regions, drain D and source S. The dimension, of the gate along the source-drain path is called length L, whereas W is the width. The surface between drain and source regions is covered with a thin layer of silicon dioxide (SiO_2), which is an excellent electrical insulator, while a layer of polycrystalline silicon(or aluminum in older technologies) is deposited on top of the dielectric of the gate. The transistor structure is completely symmetrical with respect to source and drain. Their role is defined by terminal voltages which establish the direction of carriers flow.

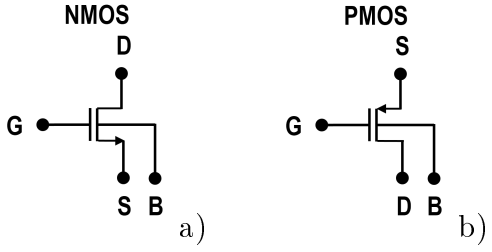


Figure 2.2: Circuit symbols of n- and p-type MOSFETs

P-type MOSFETs, have a similar structure with n-type MOSFETs and they are fabricated in the same substrate. They have opposite doping types, with p+ drain and p+ source diffusions placed in a local substrate called n-type well. In a pMOSFET the minority carriers are the positive holes whereas in an nMOSFET the negative electrons. In figure 2.2 the circuit symbols of both n- and p-type MOSFETs are depicted.

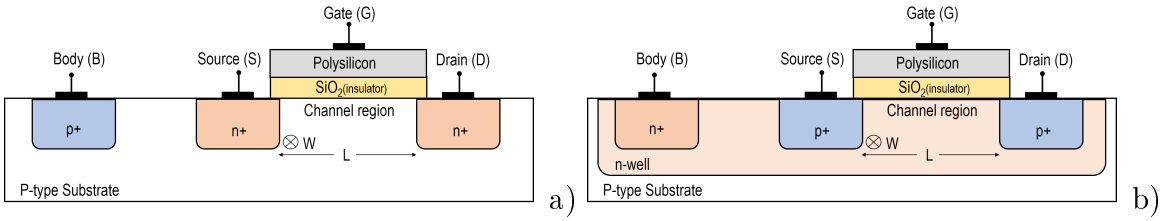


Figure 2.3: Cross section of an n- (a) and p- (b) type MOSFET. Substrate connection is also depicted

The potential of the substrate that the device is fabricated influences the device characteristics. In an nMOSFET the substrate is usually connected to the most negative supply of the system, usually the ground, and the actual connection is implemented through a p+ diffusion region, as illustrated in Figure 2.3 (a). The n-type local substrate of a pMOSFET is tied to the most positive supply voltage through an n+ diffusion region (Figure 2.3 (b)) .

2.2 MOSFET operation

2.2.1 Basic charge model definitions

In this section the basic charge definitions deriving from principal transistor physics and operation will be presented. This analysis will be focused on n-type MOSFET device intrinsic part. Drain voltage V_D, source voltage V_S and gate voltage V_G are defined with respect to the local substrate.

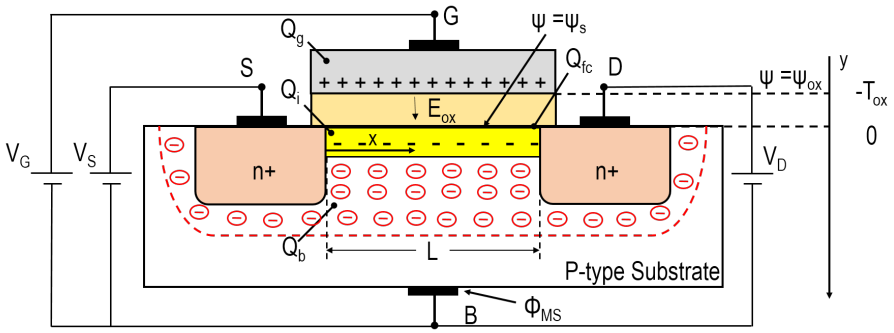


Figure 2.4: Cross section of an n-type MOSFET in inversion

For zero electric field at the silicon surface, the two back-to-back diodes formed by the pn junctions between the p-type substrate and the n+ drain and source regions,

prevent current flow when a voltage V_{DS} is applied. When gate voltage increases from zero, free holes are repelled from the surface leaving negatively charged p-doping atoms behind. Consequently, a depletion region is formed having a fixed negative charge of density Q_b per unit area. As gate voltage increases further, negative electrons are attracted to the surface forming an n-type channel, or inversion layer, corresponds to the yellow area depicted in Figure 2.4. Q_i is the negative mobile inversion charge that will carry the the drain-to-source current. The total silicon charge density under the surface is given by

$$Q_{si} \triangleq Q_b + Q_i. \tag{2.1}$$

Fixed interface charge component Q_{fc} will be assumed to be independent to gate voltage variations. Electrostatic potential Ψ values varying from $\Psi = \Psi_s$ (surface potential), at silicon surface (z=0), to $\Psi = 0$, at the position in the bulk area where it is not affected by gate voltage. The electric field in the oxide is:

$$E_{ox} = \frac{V_G - \Phi_{MS} - \Psi_s}{T_{ox}}, \tag{2.2}$$

where Φ_{MS} is the the work function potential created from the contact of gate and substrate materials.

When applying different voltages in drain and source terminals the uniformity of the channel breaks. As a result, the introduced term channel voltage V_{ch} varies monotonically from $V_{ch} = V_S$, at the source end of the channel ($x = 0$), to $V_{ch} = V_D$, at the drain end of the channel ($x = L$). At this point is very useful to define the thermal voltage

$$U_T \triangleq \frac{kT}{q}, \tag{2.3}$$

where $k = 1.3086\,10^{-23} J/K$ is the Boltzmann's constant, $q = 1.602\,10^{-19} C$ is the magnitude of electron charge and T is the absolute temperature in K. Its value at $27\,^oC$ is $25.8\,mV$.

2.2.2 Regions of inversion

In the current section a fundamental classification between the different inversion levels of the MOSFET will be established. Since surface potential Ψ_s increases with gate voltage V_G, by applying Gauss law and including the fixed charge Q_{fc}, the electric field E_{ox} given by (2.2) can be expressed as:

$$Q_{si} + Q_{fc} = -\epsilon_{ox} E_{ox} = -\epsilon_{ox} \frac{V_G - \Phi_{MS} - \Psi_s}{T_{ox}} = -C_{ox} \left(V_G - \Phi_{MS} - \Psi_s\right), \tag{2.4}$$

where $C_{ox} = \epsilon_{ox}/T_{ox}$ ($\epsilon_{ox} = 3.45\,10^{-11} F/m$). Based on the gradual channel approximation, silicon charge density Q_{si} can be calculated from:

$$Q_{si} = -\frac{\epsilon_{si} U_T}{L_D} F(\Psi_s,\, 2\Phi_F + V_{ch}), \tag{2.5}$$

where $\epsilon_{si} = 1.04\,10^{-10} F/m$ is the permittivity of silicon dioxide and constant L_D, the so called extrinsic Debye length, is given by

$$L_D \triangleq \sqrt{\frac{\epsilon_{si} U_T}{2qN_{sub}}}. \tag{2.6}$$

N_{sub} is the concentration of doping atoms in the substrate of the device. By introducing (2.5) in (2.4) the following can be obtained:

$$\frac{\epsilon_{si} U_T}{L_D} F(\Psi_s,\, 2\Phi_F + V_{ch}) - Q_{fc} = C_{ox}\left(V_G - \Phi_{MS} - \Psi_s\right) \Longleftrightarrow$$

$$\frac{\epsilon_{si}}{C_{ox} L_D} F(\Psi_s,\, 2\Phi_F + V_{ch}) - \frac{Q_{fc}}{C_{ox} U_T} = \frac{V_G - \Phi_{MS} - \Psi_s}{U_T} \Longleftrightarrow$$

$$\frac{V_G - \Phi_{MS} + \frac{Q_{fc}}{C_{ox}}}{U_T} = \frac{\epsilon_{si}}{C_{ox} L_D} F(\Psi_s,\, 2\Phi_F + V_{ch}) + \frac{\Psi_s}{U_T}. \tag{2.7}$$

Expression (2.7) describes surface potential Ψ_s as a function of gate voltage V_G. Function F is defined as:

$$F(\Psi_s,\, 2\Phi_F + V_{ch}) \triangleq \sqrt{\left(e^{\frac{\Psi_s}{U_T}} - 1\right) e^{\frac{2\Phi_F + V_{ch}}{U_T}} + \left(e^{\frac{-\Psi_s}{U_T}} - 1\right) + \frac{\Psi_s}{U_T}}. \tag{2.8}$$

Fermi potential Φ_F, with typical values varying from $13U_T$ to $18U_T$, can be expressed as

$$\Phi_F = U_T\, ln\left(\frac{N_{sub}}{n_i}\right), \tag{2.9}$$

where n_i is the intrinsic carrier concentration of the silicon substrate. $n_i \cong 1.19\,10^{10} cm^{-3}$ at ambient temperature of $27\,^oC$. Figure 2.5 shows function F versus normalized surface potential Ψ_s/U_T, for different values of channel voltage V_{ch} and $2\Phi_F = 28U_T$.

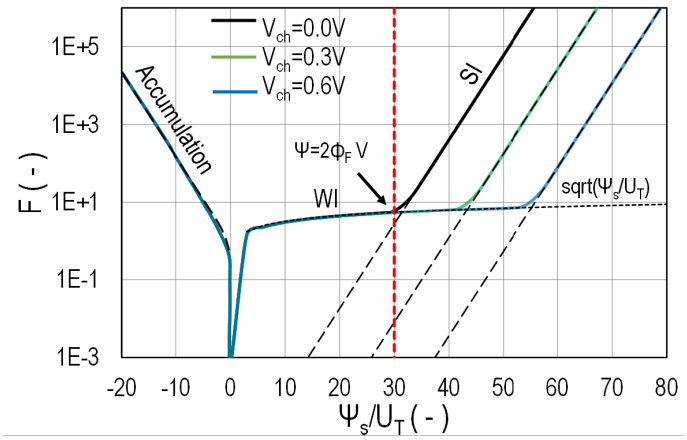


Figure 2.5: Function F versus normalized surface potential Ψ_s/U_T for 3 different values of $2\Phi_F + V_{ch}$

For negative values of Ψ_s holes accumulate exponentially. If $\Psi_s = 0$ then F becomes zero. As a result $Q_{si} = 0$; the silicon is neutral up to the surface. This is called flat-band situation and (2.7) becomes:

$$\frac{V_G - \Phi_{MS} + \frac{Q_{fc}}{C_{ox}}}{U_T} = 0 \Longleftrightarrow$$

$$V_G = V_{fb} \triangleq \Phi_{MS} - \frac{Q_{fc}}{C_{ox}}. \tag{2.10}$$

V_{fb} is the gate voltage value necessary to obtain the flat-band situation. For $0 < \Psi_s \ll 2\Phi_F + V_{ch}$, fixed depletion charge term dominates and Q_{si} increases with the square root of Ψ_s/U_T. This situation is called weak inversion (WI) and silicon charge density Q_{si} can be obtain from:

$$Q_{si}(Weak\,Inversion) \cong Q_b = -\frac{\epsilon_{si} U_T}{L_D} \sqrt{\frac{\Psi_s}{U_T}} = \gamma C_{ox} \sqrt{\Psi_s}, \tag{2.11}$$

where γ is the substrate modulation factor, given by

$$\gamma \triangleq \frac{\epsilon_{si}}{L_D C_{ox}} \sqrt{U_T}. \tag{2.12}$$

By introducing (2.6) in (2.12) the following can be obtained:

$$\gamma = \frac{\sqrt{2q\epsilon_{si} N_{sub}}}{C_{ox}}. \tag{2.13}$$

When Ψ_s exceeds $2\Phi_F + V_{ch}$, Q_{si} increases rapidly with Ψ_s due to the contribution of mobile charge term. This situation is defined as strong inversion (SI).

2.2.3 Threshold voltage function

By using relations (2.4) and (2.10), silicon charge density Q_{si} can be related to flat-band voltage V_{fb} as follows:

$$Q_{si} + Q_{fc} = -C_{ox} \left(V_G - \Phi_{MS} - \Psi_s\right) \Longleftrightarrow$$

$$\frac{Q_{si}}{C_{ox}} + \frac{Q_{fc}}{C_{ox}} = -(V_G - \Phi_{MS} - \Psi_s) \Longleftrightarrow$$

$$\frac{Q_{si}}{C_{ox}} = -V_G + \Phi_{MS} - \frac{Q_{fc}}{C_{ox}} + \Psi_s \Longleftrightarrow$$

$$\frac{Q_{si}}{C_{ox}} = -V_G + V_{fb} + \Psi_s \Longleftrightarrow$$

$$Q_{si} = -C_{ox}(V_G - V_{fb} - \Psi_s). \tag{2.14}$$

From (2.1) inversion charge Q_i can be expressed as the difference between the total silicon charge Q_{si} minus depletion charge Q_b

$$Q_i = Q_{si} - Q_b \tag{2.15}$$

and by substituting (2.11) and (2.14) in (2.15) the following can be obtained:

$$Q_i = -C_{ox}(V_G - V_{fb} - \Psi_s - \gamma\sqrt{\Psi_s}) = -C_{ox}(V_G - V_{TB}), \tag{2.16}$$

where V_{TB} is called threshold voltage function, which depends on the process, and it is given by

$$V_{TB} \triangleq V_{fb} + \Psi_s + \gamma\sqrt{\Psi_s}. \tag{2.17}$$

Threshold voltage can be defined as the value of gate voltage V_G where the inversion charge Q_i equals to zero. Hence, threshold voltage denotes the value of gate voltage where channel formation begins.

2.2.4 Slope factor

Slope factor or weak inversion slope n is defined as the first derivative of threshold voltage function versus surface potential,

$$n \triangleq \frac{\partial V_{TB}}{\partial \Psi_s} = 1 + \frac{\gamma}{2\sqrt{\Psi_s}}, \tag{2.18}$$

with nominal values always above unity, varying from 1.2 to 1.7 depending on the process.

2.2.5 Pinch-off potential

For a given value of gate voltage, inversion charge becomes zero for a specific value of surface potential $\Psi_s = \Psi_p$, called pinch-off surface potential. For $Q_i = 0$ equation (2.16) becomes:

$$V_G \triangleq V_{fb} + \Psi_p + \gamma\sqrt{\Psi_p}. \tag{2.19}$$

Pinch-off potential cannot be extracted directly from measurable characteristics of a transistor and therefore it is related to a specific value of channel voltage V_{ch} called pinch-off voltage V_p. Using strong inversion approximation that assumes that surface potential is constantly larger than $2\Phi_F + V_{ch}$, pinch-off voltage can be obtained from:

$$V_p = \Psi_p - 2\Phi_F. \tag{2.20}$$

An effective approximation of V_p could also be:

$$V_p \cong \frac{V_G - V_{T0}}{n}, \tag{2.21}$$

where V_{T0} is the threshold voltage of the device.

2.2.6 Carrier mobility

In a silicon semiconductor, typical mobility values at $T = 300K$ for low doping concentration are [2]:

$$\mu_n \cong 1350 \, \frac{cm^2}{V.s} \tag{2.22}$$

$$\mu_p \cong 480 \, \frac{cm^2}{V.s} \tag{2.23}$$

where μ_n and μ_p is the electron and hole mobility respectively. The three major scattering mechanisms that influence mobility are Coulomb, phonon and surface-roughness scattering; thus, the channel mobility μ can be calculated from [5]:

$$\frac{1}{\mu} = \frac{1}{\mu_c} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}. \tag{2.24}$$

Coefficients μ_c, μ_{ph} and μ_{sr} are the mobilities derive from the three different mechanisms mentioned above.

2.3 Voltage-inversion charge relation

In this section the basic expression that correlates inversion charge and channel voltage will be defined. Normalization of voltages and charges is realized as described next. All voltages are normalized to U_T and represented by lowercase letters:

$$\frac{V}{v} = \frac{\Phi}{\varphi} = \frac{\Psi}{\psi} = U_T. \tag{2.25}$$

Charges are normalized to specific charge Q_{spec} which is defined by

$$Q_{spec} \triangleq -2nU_T C_{ox}. \tag{2.26}$$

Hence, normalized inversion charge q_i is given by

$$q_i = \frac{Q_i}{Q_{spec}}. \tag{2.27}$$

The basic charge-voltage relationship of a MOSFET is:

$$2q_i + lnq_i = v_p - v_{ch}, \tag{2.28}$$

where v_p and v_{ch} are the normalized pinch-off and channel potentials respectively. In weak inversion linear term becomes negligible since $q_i << 1$. Instead, in strong inversion

$q_i >> 1$; thus the logarithmic term becomes negligible. In either case, mobile charge can be approximated by the flowing equations:

$$q_i(Weak\,Inversion) = exp(v_p - v_{ch}) \tag{2.29}$$

and

$$q_i(Strong\,Inversion) = \frac{v_p - v_{ch}}{2}. \tag{2.30}$$

2.4 Drain current model

Drift and diffusion are the two major mechanisms responsible of current flow on semiconductors. In a MOSFET, if x is the horizontal position in the channel measured from source end ($x = L$ at drain end), then drain current equation is given by

$$I_D = \mu W \left(\underbrace{-Q_i \frac{d\Psi_s}{dx}}_{drift} + \underbrace{U_T \frac{dQ_i}{dx}}_{diffusion} \right), \tag{2.31}$$

where μ is the equivalent mobility of electrons. The first term represents the drift component of the current and the second term the diffusion component. Typically the concentration n_p of electrons in the channel can be expressed as

$$n_p = n_i\, exp\left(\frac{\Psi_s - \Phi_F - V_{ch}}{U_T} \right) \tag{2.32}$$

and according to the charge sheet approximation, where the whole mobile charge Q_i is assumed to be at surface potential Ψ_s, the following can be obtained:

$$Q_i \propto n_p. \tag{2.33}$$

Differentiation of equation (2.32) results into:

$$\frac{dQ_i}{dx} = \frac{1}{U_T} \left(\frac{d\Psi_s}{dx} - \frac{dV_{ch}}{dx} \right) \underbrace{n_i\, exp\left(\frac{\Psi_s - \Phi_F - V_{ch}}{U_T} \right)}_{Q_i} \Longleftrightarrow$$

$$\frac{dQ_i}{dx} = \frac{Q_i}{U_T} \left(\frac{d\Psi_s}{dx} - \frac{dV_{ch}}{dx} \right). \tag{2.34}$$

Thus, equation (2.31) can be rewritten as

$$I_D = \mu W(-Q_i) \frac{dV_{ch}}{dx}. \tag{2.35}$$

Integrating over the length of the channel and because

$$\int_0^L I_D dx = I_D L, \tag{2.36}$$

we have

$$I_D = \mu \frac{W}{L} \int_{V_S}^{V_D} -Q_i dV_{ch} = \beta \int_{V_S}^{V_D} \frac{-Q_i}{C_{ox}} dV_{ch}, \tag{2.37}$$

where

$$\beta \triangleq \mu C_{ox} \frac{W}{L}. \tag{2.38}$$

Equation (2.31) states that drain current can be obtained from $Q_i(V_{ch})$ function precisely in all levels of inversion. Furthermore, this result is independent of the shape of $Q_i(V_{ch})$ function. Integral (2.37) can be transformed into

$$I_D = \beta \int_{V_S}^{\infty} \frac{-Q_i}{C_{ox}} dV_{ch} - \beta \int_{V_D}^{\infty} \frac{-Q_i}{C_{ox}} dV_{ch} = I_F - I_R, \tag{2.39}$$

where I_F is the forward current and I_R is the reverse current. Figure 2.6 shows the decomposition of drain current into forward and reverse components. I_F is controlled by V_P and V_S whereas I_R depends only on V_P and V_D. Consequently, drain current is the superposition of independent and symmetrical effects of drain and source potentials.

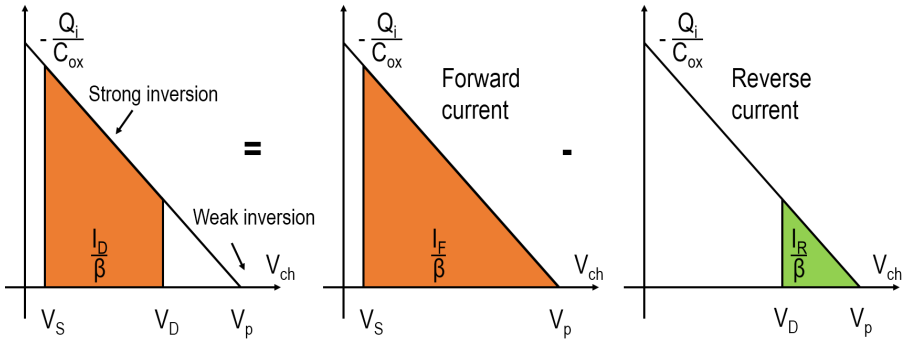


Figure 2.6: Forward and reverse drain current components

2.5 Current-inversion charge relation

I_{spec} is the specific current of a MOSFET and is defined as

$$I_{spec} \triangleq I_0 \frac{W}{L}, \tag{2.40}$$

where $I_0 = 2n\mu C_{ox} U_T^2$ is the technology current. All currents are normalized to I_{spec} according to

$$\frac{I_D}{i_d} = \frac{I_F}{i_f} = \frac{I_R}{i_r} = I_{spec}. \tag{2.41}$$

By normalizing charge and voltages in (2.37) drain current can be expressed as

$$I_D = U_T \beta \int_{V_S}^{V_D} \frac{-Q_{spec}\left(\frac{Q_i}{Q_{spec}}\right)}{C_{ox}} d\frac{V_{ch}}{U_T} \Longleftrightarrow$$

$$I_D = \frac{-Q_{spec}\beta U_T}{C_{ox}} \int_{v_s}^{v_d} q_i dv_{ch} \Longleftrightarrow$$

$$I_D = I_{spec} \int_{v_s}^{v_d} q_i dv_{ch}. \tag{2.42}$$

Additionally, normalized forward i_f and reverse i_r current components can be expressed as

$$i_{f,r} = \int_{v_{s,d}}^{\infty} q_i dv_{ch}. \tag{2.43}$$

From voltage-inversion charge relation (2.28) the following can be obtained:

$$\frac{dv_{ch}}{dq_i} = \frac{d\left(v_p - 2q_i - lnq_i\right)}{dq_i} \Longleftrightarrow$$

$$\frac{dv_{ch}}{dq_i} = -2 - \frac{1}{q_i} \tag{2.44}$$

and when introduced in (2.43) yields

$$i_{f,r} = \int_0^{q_{s,d}} (2q_i + 1) dq_i = q_{s,d}^2 + q_{s,d} \tag{2.45}$$

where q_s and q_d are the normalized charges at source and drain side of the channel respectively, and can be defined by

$$q_{s,d} \triangleq \frac{-Q_{iS,D}}{Q_{spec}}. \tag{2.46}$$

Furthermore, parameters q_s and q_d can be calculated by inverting (2.45) :

$$q_{s,d} = \frac{\sqrt{1+4i_{f,r}}-1}{2}. \tag{2.47}$$

When (2.28) is applied at the two ends of the channel, can be transformed into

$$2q_{s,d} + lnq_{s,d} = v_p - v_{s,d} \tag{2.48}$$

and drain current expression (2.39) can be expressed in terms of normalized inversion charges as

$$I_D = I_{spec}\left(q_s^2 + q_s - q_d^2 - q_d\right). \tag{2.49}$$

2.6 Modes of operation

Bias situation of source and drain terminals with respect to pinch-off voltage V_p, determine the mode of operation of a MOSFET. Figure 2.6 shows an instance of $Q_i(V_{ch})$ function where channel sides near both terminals are strongly inverted. Furthermore, since both V_S and V_D potentials values are below V_p the transistor is in linear mode. If drain voltage is increased above pinch-off voltage, the channel inversion charge at the drain end of the channel becomes nearly zero; the transistor is still in strong inversion but in forward saturation (Figure 2.7). In this case reverse current component becomes negligible and drain current does not increased significantly any more. Note that at increasing V_{DS} values the drain depletion region width widens due to increasing reverse bias between drain and drain side of the channel.

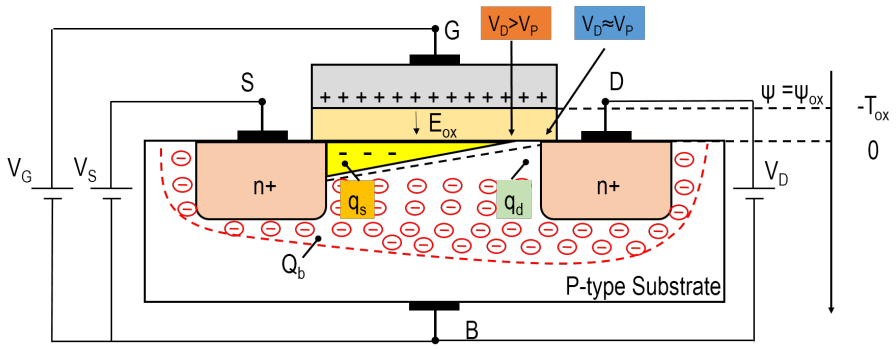


Figure 2.7: Cross section of an n-type MOSFET in strong inversion and forward saturation ($V_D > V_P, V_S < V_P$) . At drain end of the channel normalized inversion charge q_d is almost zero

When both V_S and V_D exceed V_P, inversion charge value in both sides of the channel becomes relatively small and the transistor operates in weak inversion. Drain to source saturation voltage is given by

$$V_{Dsat}(Strong\,Inversion) = V_P - V_S \tag{2.50}$$

and

$$V_{Dsat}(Weak\,Inversion) \backsimeq 3 \ldots 4U_T. \tag{2.51}$$

Figure 2.8 represents the modes of operation with respect to V_S, V_D and V_P voltages, for a positive pinch-off voltage value. Dashed line ($V_S = V_D$) separates forward from reverse mode. In reverse mode, $V_S > V_D$ and therefore $I_D < 0$. In reverse saturation, forward current component becomes negligible and $I_D = -I_R$. In deep week inversion when drain current value is sufficiently small, the transistor is considered to be blocked.

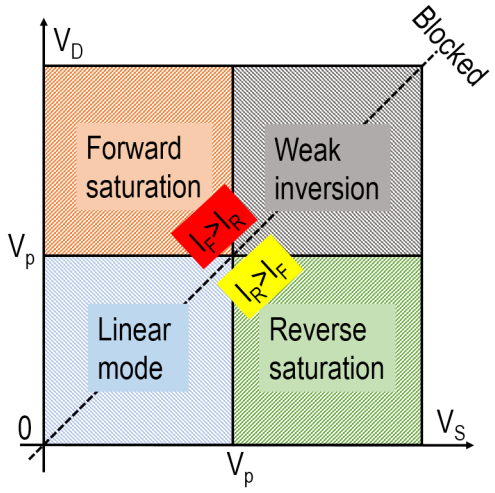


Figure 2.8: Modes of operation of a MOSFET

2.7 Inversion coefficient

Inversion coefficient IC is a numerical measure of the inversion level of the MOSFET and it is defined by

$$IC \triangleq max(i_f, i_r). \tag{2.52}$$

Values of IC less than 0.1 correspond to weak inversion and values above 10 in strong inversion. For values between 0.1 and 10 the transistor is operating in the transition region called moderate inversion (MI). It should be mentioned that in this case both linear and logarithmic terms of relation (2.28) are significant. In Figure 2.9 the different levels of inversion with respect to IC are shown.

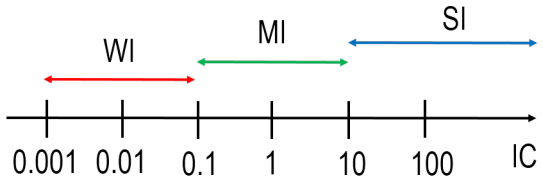


Figure 2.9: Inversion levels of the channel in terms of inversion coefficient (IC)

2.8 Transconductances model

In a MOSFET drain current is controlled by the voltages applied in the four terminals. Small variations in V_D,V_S, V_G and V_B values will cause I_D value to fluctuate respectively. The small-signal parameter describing this effect is called transconductance. Source, gate, drain and bulk transconductances can be defined as

$$g_{ms,d} \triangleq (-,+)\frac{\vartheta I_D}{\vartheta V_{S,D}},\ g_m \triangleq \frac{\vartheta I_D}{\vartheta V_G},\ g_{mb} \triangleq \frac{\vartheta I_D}{\vartheta V_{BS}}. \tag{2.53}$$

Hence, the total increment in drain current ΔI_D is expressed as

$$\Delta I_D = g_m \Delta V_G - g_{ms}\Delta V_S + g_{md}\Delta V_D + g_{mb}\Delta V_B. \tag{2.54}$$

Transconductances are related to normalized inversion charges as:

$$g_{ms,d} = Y_{spec} q_{s,d} \tag{2.55}$$

and

$$g_m = \frac{g_{ms} - g_{md}}{n} = \frac{Y_{spec}}{n} (q_s - q_d) \tag{2.56}$$

where

$$Y_{spec} = \frac{I_{spec}}{U_T}. \tag{2.57}$$

Using expressions (2.47), (2.55) and (2.57) the following can be obtained:

$$q_{s,d} = \frac{g_{ms,d}}{Y_{spec}} = \frac{g_{ms,d} U_T}{I_{spec}} = i_{f,r} \frac{g_{ms,d} U_T}{I_D} = \frac{\sqrt{1 + 4i_{f,r}} - 1}{2} \Longleftrightarrow$$

$$q_{s,d} = \frac{\left(\sqrt{1 + 4i_{f,r}} - 1\right)\left(\sqrt{1 + 4i_{f,r}} + 1\right)}{2\left(\sqrt{1 + 4i_{f,r}} + 1\right)} \Longleftrightarrow$$

$$G(i_{f,r}) = \frac{g_{ms,d} U_T}{I_D} = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + i_{f,r}}}. \tag{2.58}$$

In terms of inversion coefficient IC (2.58) can be rewritten as:

$$G(IC) = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + IC}} \tag{2.59}$$

and gate transconductance-to-current ration can be expressed as

$$\frac{g_m U_T}{I_D} = \frac{1}{n} G(IC). \tag{2.60}$$

2.9 Typical I-V characteristics

In this section typical I-V and characteristics and related transconductances, of an n-type MOSFET with $W/L = 1um/60nm$ are presented. Figure 2.10(a, b) shows the measured I_D versus V_G characteristics in both linear ($V_{DS} = 0.02V$) and saturation ($V_{DS} = 1.2V$) modes from weak to strong inversion. Drain current is depicted on both linear (a) and logarithmic (b) scale. In Figure 2.10(c) output characteristic I_D versus V_D is shown for the same device. In Figure 2.11 gate transconductance vs. gate voltage (a), normalized transconductance-to-current ration vs. drain current (b) and channel and output conductance (c) are also presented. Output characteristics are evaluated for two different gate voltage values $V_{GS} = 0.8\,and\,1.2V$.

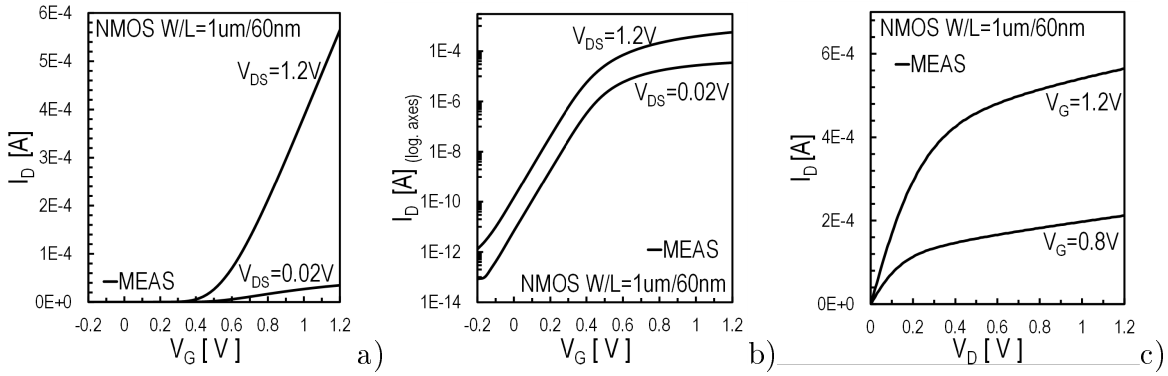


Figure 2.10: Typical measured transfer characteristics of an nMOS with $W/L = 1um/60nm$ in linear ($V_{DS} = 0.02V$) and saturation ($V_{DS} = 1.2V$) modes. Drain current is shown on both linear (a) and logarithmic (b) scale. Output characteristic $I_D - V_D$ of the same transistor are shown (c), for two different gate voltage values $V_{GS} = 0.8\,\&\,1.2V$

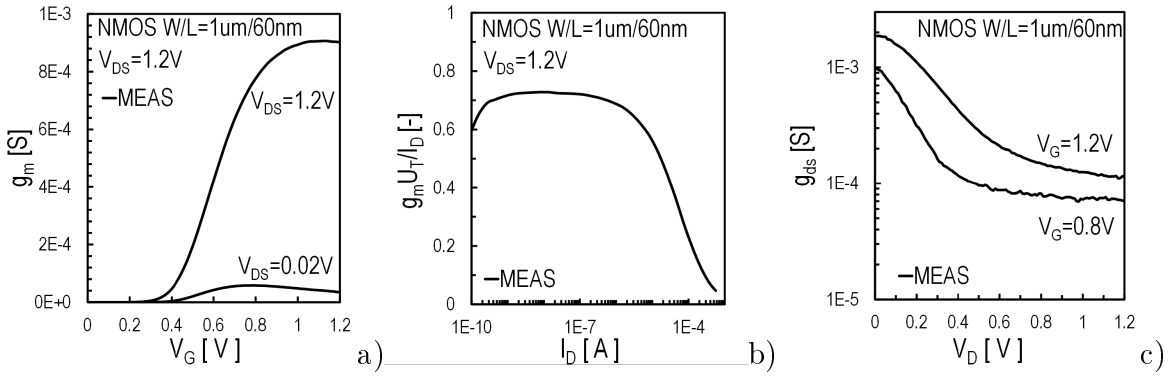


Figure 2.11: Gate transconductance vs. gate voltage (a) and normalized transconductance-to-current ration vs. drain current (b) for an nMOS with $W/L = 1um/60nm$. $V_{DS} = 0.05V$ for linear and $V_{DS} = 1.2V$ for saturation mode. Output conductance (c) is also depicted.

2.10 Short channel effects

So far the analysis was based on the assumption that the channel length of the device is relatively long and short channel effects were excluded. Such effects appear when the device dimensions shrink and specifically when the channel length dimension is reduced to become comparable to the depletion width dimension. Basic short channel effects are: Velocity saturation (VS), Channel length modulation (CLM) and Drain-induced barrier lowering (DIBL).

2.10.1 Velocity saturation

When the lateral electric field E_x reaches a specific value E_c, called critical field, carrier drift velocity v_{drift} saturates towards a maximum value v_{sat}. This effect is called velocity saturation and is responsible for drain current and source transconductance degradation in short channel devices [1]. Figure 2.10 shows the channel divided into a non saturated region and a velocity saturated region (VSR) near the drain terminal.

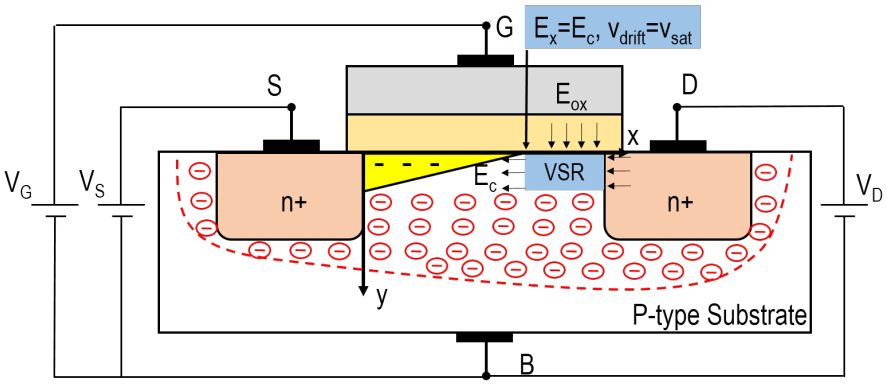


Figure 2.12: Cross section of a short-channel n-type MOSFET where velocity saturation region VSR is depicted

In this section a simplified model proposed in [1] in order to capture the impact of VS on drain current will be presented. Parameter λ_c introduced in [6] accounts for VS effect according to

$$\lambda_c \triangleq \frac{L_{sat}}{L}, \tag{2.61}$$

where L_{sat} is the portion of the channel over which the carrier drift velocity saturates. Typically λ_c tends to zero for long-channel devices. Channel length L_{sat} is defined as [7]

$$L_{sat} \triangleq \frac{2\mu_z U_T}{v_{sat}}, \tag{2.62}$$

where μ_z is the low longitudinal field mobility depending on vertical field E_z. As described in Section 2.6, without VS, drain current saturates when $q_d = 0$. On the contrary, when VS is present drain current saturates as soon as q_d reaches a saturated value q_{dsat}. This value denotes the inversion charge at the drain end of the channel necessary to sustain drain current when carrier velocity is saturated near the drain terminal. In this case (2.49) can be written as

$$i_{dsat} = q_s^2 + q_s - q_{dsat}^2 - q_{dsat}. \tag{2.63}$$

In terms of λ_c drain current is given by [1]

$$i_{dsat} \triangleq \frac{2q_{dsat}}{\lambda_c}. \tag{2.64}$$

Using expressions (2.63) and (2.64) the following can be obtained

$$i_{dsat} = \frac{4\left(q_S + q_s^2\right)}{2 + \lambda_c + \sqrt{4\left(1+\lambda_c\right) + \lambda_c^2\left(1+q_s^2\right)^2}}. \tag{2.65}$$

Equation (2.65) can be inverted and normalized inversion charge at the source end of the channel, q_s, can be expressed as

$$q_s = \frac{\sqrt{\left(i_{dsat}\lambda_c + 1\right)^2 + 4i_{dsat}}}{2} - \frac{1}{2}. \tag{2.66}$$

By neglecting velocity saturation effect ($\lambda_c = 0$)in (2.65), the basic current-inversion charge relation, referring to a long-channel MOST operating in forward saturation mode, can be obtained:

$$i_{dsat} = q_s + q_s^2. \tag{2.67}$$

2.10.2 Channel length modulation

So far channel length L is assumed to be equal to the distance between source and drain terminals. However, at both ends of the channel, potential barriers introduced by source and drain junctions create space charge regions of length $l_{S,D}$. In strong inversion and forward (reverse) saturation the drain (source) depletion-region widens. As a result, the actual length of the electrical channel is reduced to [1, 4]

$$L = L - (l_S + l_D) \tag{2.68}$$

causing drain current increment. This effect is called channel length modulation (CLM).

2.10.3 Drain-induced barrier lowering

In short-channel devices source and drain terminals are closer resulting into a deeper depletion area under the inversion region. With increasing V_{DS} the depth of the depletion area increases further. Deeper channel depletion region is accompanied by increasing surface potential which attracts more carriers into the channel. Consequently, drain current is increased causing threshold voltage value V_{TO} to decrease [3, 4]. This effect is commonly referred as DIBL (Drain-induced barrier lowering).

2.11 Modeling approach

Equations (2.21), (2.40), (2.41), (2.48) and (2.65) comprise an EKV-type [8] model proposed in [22], than can be used in order to extract a set of parameters (I_0, V_{TO}, n, λ_c) that predict accurately the transfer characteristics and related transconductances of a saturated MOSFET. I_0 may be extracted from the longest- and widest-channel device available and scaled for other devices according to their geometry. I_D is equal to I_0 when $\frac{g_m U_T}{I_D} = 0.618 \left(\frac{g_m U_T}{I_D} \mid_{max} \right)$ [9]. Threshold voltage parameter V_{TO} is extracted from the I_D versus V_G characteristics, slope factor n from the maximum $g_m U_T / I_D$ vs. I_D plateau in weak inversion according to

$$n = \frac{1}{\left(\frac{g_m U_T}{I_D} \mid_{max} \right)} \tag{2.69}$$

and λ_c by fitting the model in strong inversion. Figure 2.13(a) shows the extraction of slope factor n of a short-channel nMOS. In Figure 2.13(b), the relation of parameter λ_c to the intersection of the weak and strong inversion asymptotes of the normalized transconductance-to-current ration is presented.

In Figures 2.14 and 2.15, the above model is adapted to the transfer characteristics and transconductances of long- ($L = 10um$) and short- ($L = 60nm$) channel nMOSFETs, of a standard 65nm bulk CMOS process. The transistors are operating in saturation ($V_{DS} = 1.2V$). Parameter λ_c present higher values for short channel devices where the effect of velocity saturation effect is expected to be most pronounced. The model with $\lambda_c = 0$ is demonstrated in all cases.

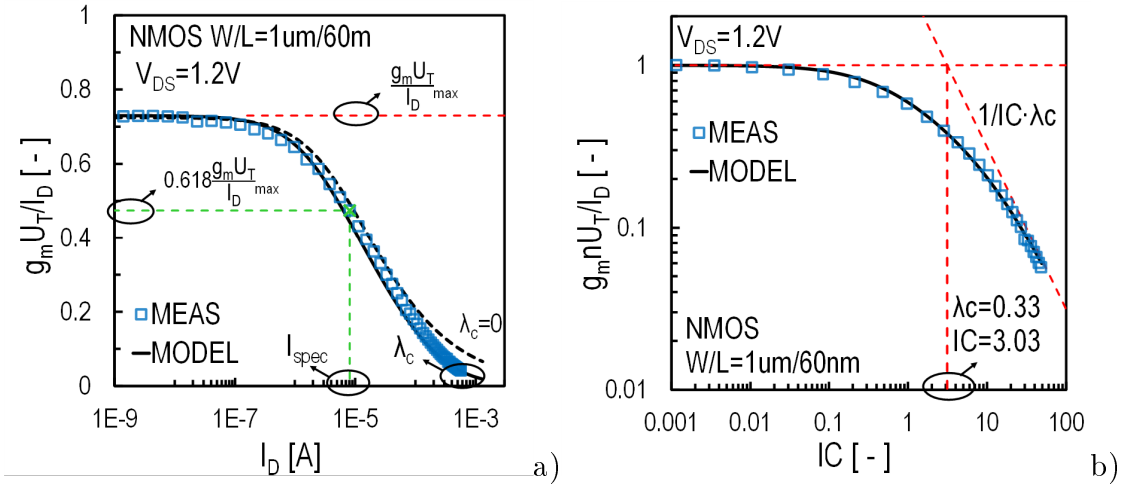


Figure 2.13: Extraction of slope factor slope factor n (a) and normalized transconductance efficiency vs. IC (b), for short- channel nMOSTs in saturation ($V_{DS} = 1.2V$). Markers: measurements, solid lines: model with VS, black dashed lines: model without VS. Asymptotes (red dashed) and extracted parameter λ_c are shown

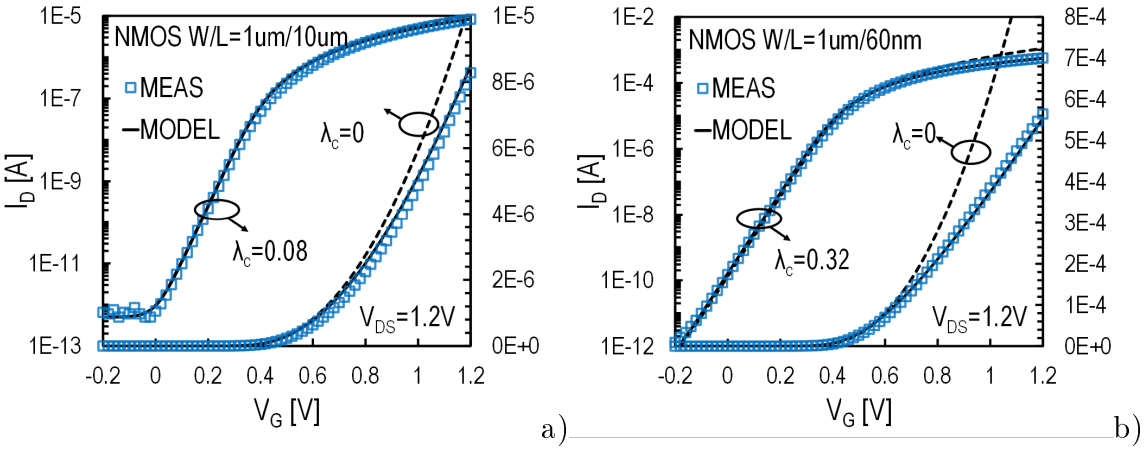


Figure 2.14: Transfer characteristics of long- (a) and short- (b) channel nMOSFETs in saturation ($V_{DS} = 1.2V$). Markers: measurements, solid lines: model with VS, dashed lines: model without VS

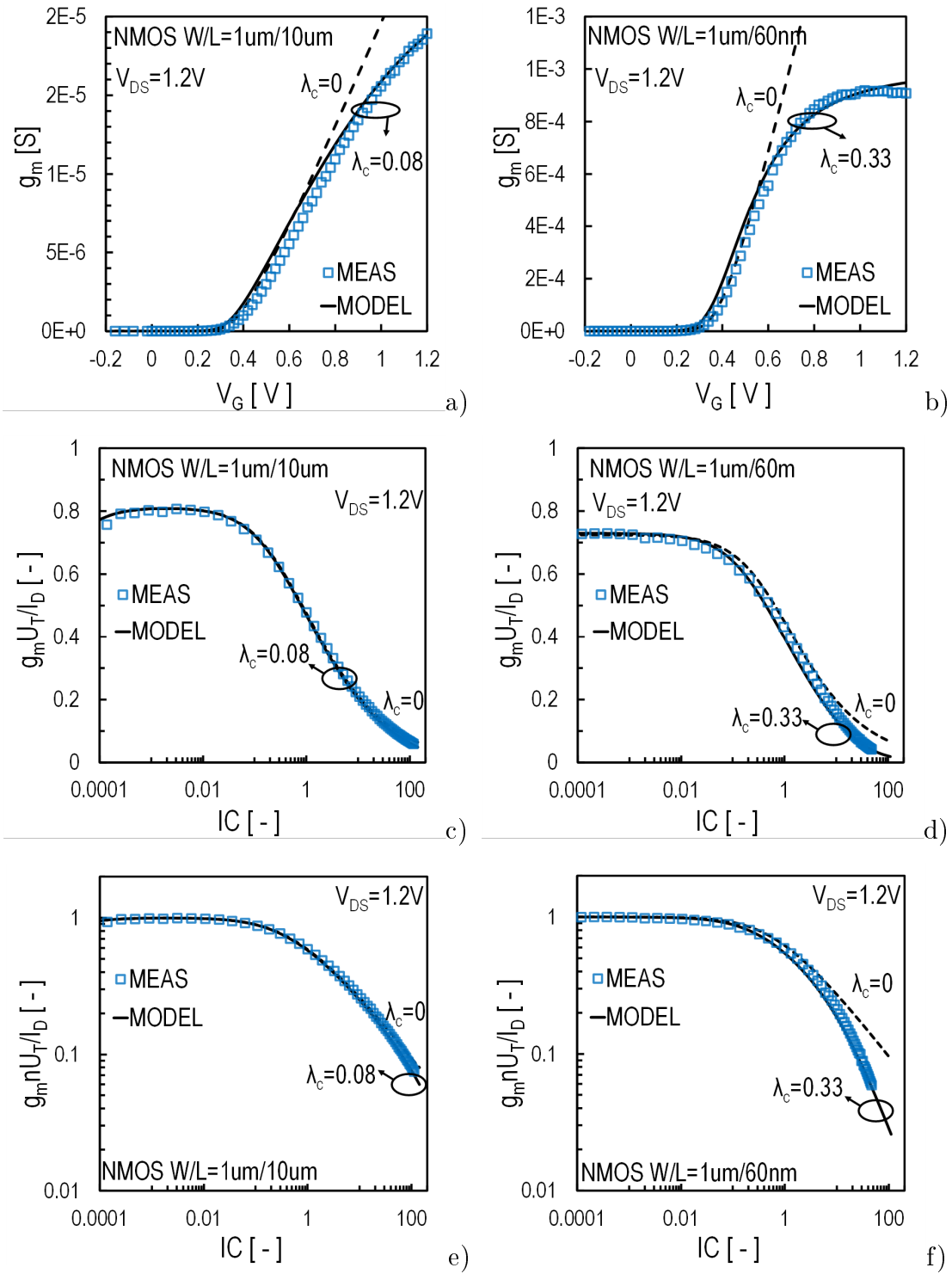


Figure 2.15: Gate transconductance g_m vs. gate voltage V_G (a, b) and normalized gate (c, d) and source (d, e) transconductance-to-current ratio vs. inversion coefficient IC, for long-($L = 10um$) and short-($L = 60nm$) channel nMOSFETs in saturation ($V_{DS} = 1.2V$). Markers: measurements, solid lines: model with VS, dashed lines: model without VS

2.12 Enclosed gate MOSFETs

Shallow trench isolation (STI) has been identified as a source of increased leakage in subthreshold operation of MOSFETs [10]. Additionally, the STI effect has been shown to adversely impact $1/f$ noise and random telegraph noise (RTN) [11, 12]. Enclosed gate transistors have been prominently used due to their immunity to ionizing radiation [11]. They are advantageous in suppressing the edge effect, or lateral conduction related to STI, and consequently show improved matching behavior in weak inversion[13]. In Figure 2.16 the basic layout of an enclosed gate (EG) MOSFET, is presented.

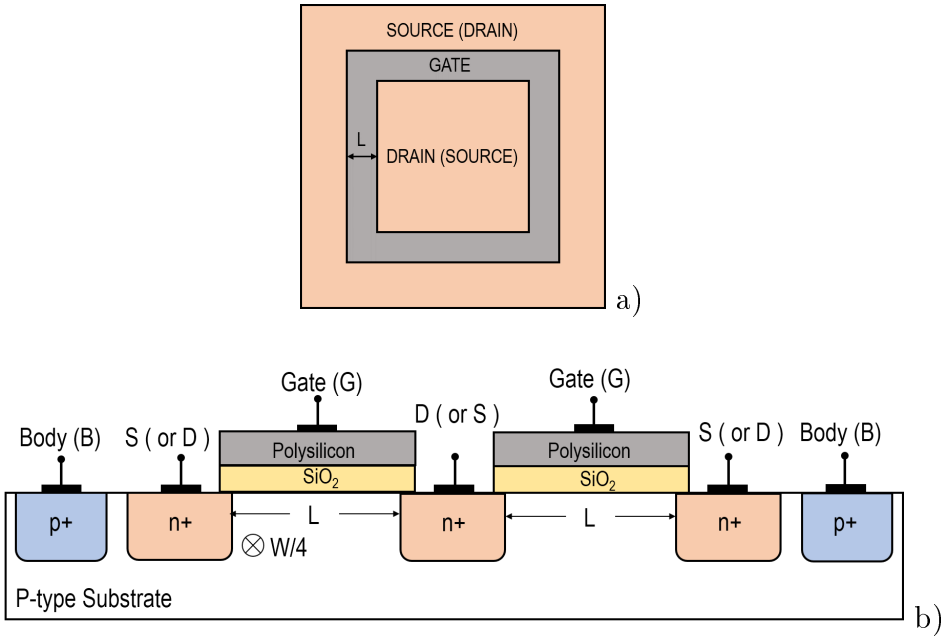


Figure 2.16: Planar view (a) and cross section (b) of an enclosed gate nMOSFET

In enclosed gate MOSFETs the drain (or source) diffusion is fully surrounded by the gate polysilicon and the source (or drain) diffusion. The choice of the inner electrode as drain or source is defined by the bias voltage although as reported at [14] and [15], by selecting the outer electrode as the drain an annular structure device exhibits lower drain electric fields and improved reliability when compared to a transistor with a standard layout. Conversely, if the inner electrode is selected as the drain, the substrate contact will be closer to the source diffusion reducing drain resistance; thus, the value of the output conductance will be increased [15, 16]. Enclosed gate transistors come in a variety of different shapes. In Figure 2.17 some of the most widely used layouts are shown [14, 17]. In quarter sub-micron processes design rules prevent the manufacture of circular and 45^o gate corners layouts, thus structures with 45^o corner cuts are used [14].

In standard (ST) MOSFETs thick field oxides, STI or LOCOS, are used in order to provide better isolation between different devices and define the active silicon area. As it will discussed in detail in Section 3, in radiation environments, due to the positive charge trapping at the edges of the field oxides, an induced inversion layer will give rise to a transistor leakage current path from drain to source diffusions. EG MOSFETs without STI (or LOCOS), can eliminate the edge leakage preventing leakage currents between components. This is possible because any current between source and drain has to flow underneath the gate oxide and there is no possible current path along the edge of the active area [17].

Additionally, RTS noise, which is related to trapping sites within the Si/SiO_2 interface due to structural defects, can be affected by the presence of STI field oxide. During the STI process, the device can be damaged at the STI boundary resulting to the generation of extra traps at the edge of the channel under the gate region [18]. As the device dimensions scales down the ratio of device gate edge-to-area increases and the STI edge effect dominates the overall RTS performance [19]. Since low frequency noise is strongly related to RTS noise, devices without STI are expected to exhibit greatly improved $1/f$ noise characteristics like lower drain current noise spectra and relative current variations.

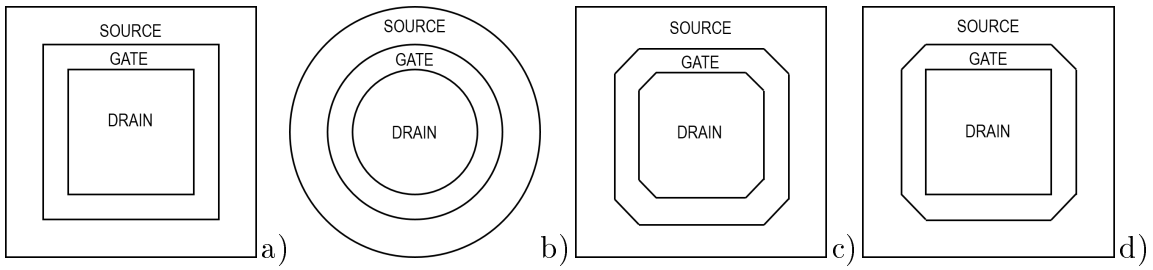


Figure 2.17: Typical EG MOSFETs shapes: square (a), circular (b), octagonal (c) and square with 45^o outer poly-edge cut (d)

2.13 W/L ratio modeling in enclosed gate MOSFETs

Unlike conventional MOSFETs in transistors with enclosed gate layouts the definition of the aspect ratio W/L, is not trivial. For rectangular and square layouts, due to the distribution of the electric field in the corners of the gate, the transistor must be divided into smaller parts with the use of conformal mapping technique [14, 16]. These parts can be considered as smaller transistors contributing accordingly to the drain current of the device. Figure 2.18 shows the decomposition of a broken corner square and a square MOSFET into smaller transistors with 3 different basic shapes. Trapezium 1 is the approximation of the edge transistor, trapezium 2 corresponds to the corner

transistor and rectangle 3 is used to model the 45^o edge cuts in the case of broken square corner MOSFET.

Following [14] and [20] ,the effective $\frac{W}{L}$ ratio of a broken corner square MOSFET can be calculated from

$$\left(\frac{W}{L}\right)_{eff} = 4\frac{2a}{ln\left(\frac{d'}{d'-2aL_{eff}}\right)} + 2K\frac{1-a}{0.5ln\left(\frac{1}{a}\right)\sqrt{a^2+2a+5}} + 3\frac{\frac{d-d'}{2}}{L_{eff}}, \tag{2.70}$$

where $d' = d - c\sqrt{2}$ and a is a fitting parameter which is needed to identify the borders between transistors 1 and 2. For different CMOS technologies scaling from $2.5um$ to $0.25um$, parameter a has been found to be almost technology independent with a value of 0.05. Parameter K is geometry dependent with a value of 7/2 for devices with $L \leq 0.5um$ and 4 for longer devices.

Under the same approach, the aspect ratio of the square layout is given by

$$\left(\frac{W}{L}\right)_{eff} = 4\left(\frac{2a}{ln\left(\frac{d}{d-2aL_{eff}}\right)} + \frac{2}{0.5\sqrt{a^2+2a+5}} + \frac{2\,(1-a)}{-lna}\right). \tag{2.71}$$

Again $a = 0.05$ can be chosen to assure a good $\frac{W}{L}$ predictability. It should be noticed that the only way to achieve lower aspect ratios is to increase L and keep d constant. Therefore, transistors with enclosed gate layouts, cannot have aspect ratios lower than a certain value [20].

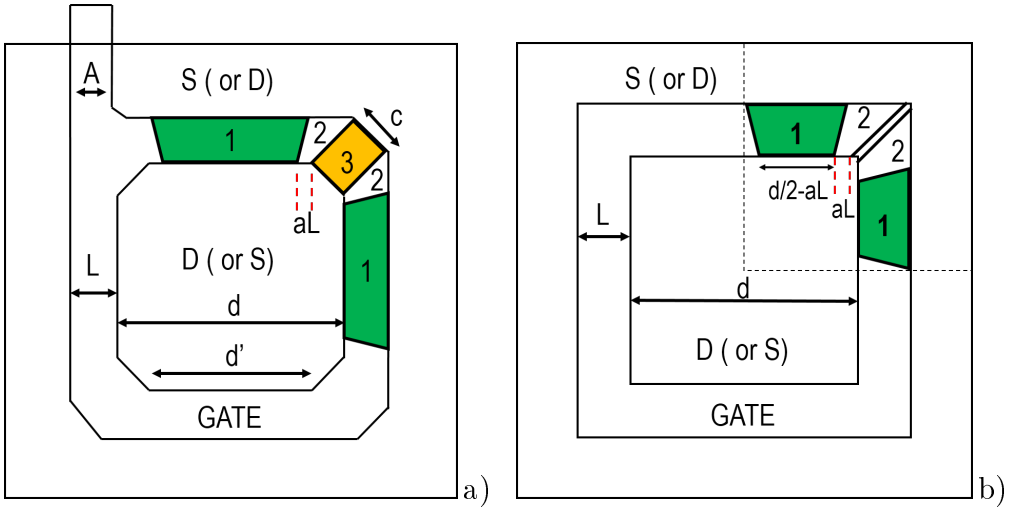


Figure 2.18: Square (a) and broken corner square (b) MOSFET formed by different types of transistors in parallel

For EG MOSFETs with circular geometry the effective $\frac{W}{L}$ ratio can be approximated by

$$\left(\frac{W}{L}\right)_{eff} = \frac{2\pi}{ln\left(\frac{R2}{R1}\right)}, \tag{2.72}$$

where $R1$ is the inner diffusion radius and $R2 = L + R1$. If the drain radius is much greater than the channel length $L \ll R1$ the above equation gives a very good approximation of the effective $\frac{W}{L}$ ratio. Conversely, for long channel devices (2.72) overestimates the result.

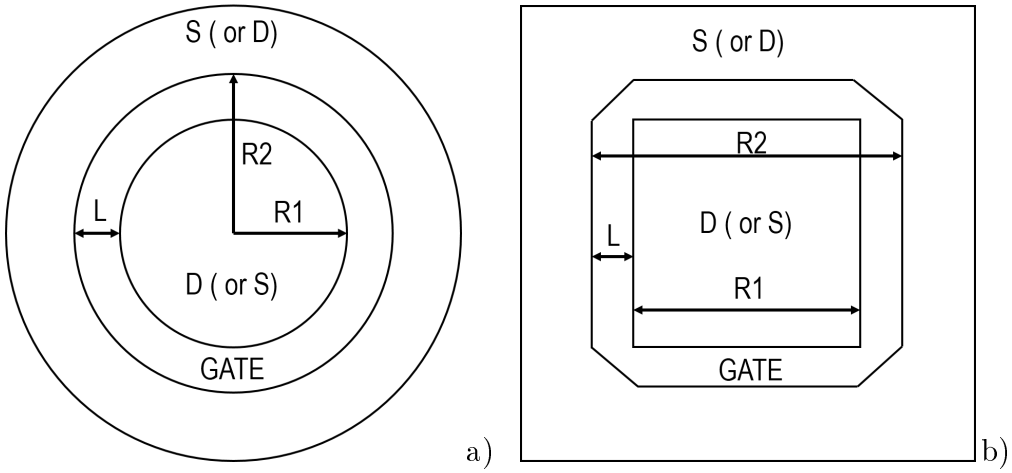


Figure 2.19: Circular (a) and square with 45^o outer poly-edge cut (b) EG MOSFETs.

For square transistors with 45^o outer poly-edge cut, a more compact approach of $\left(\frac{W}{L}\right)_{eff}$ is given by [20]

$$\left(\frac{W}{L}\right)_{eff} = \frac{8}{ln\left(\frac{R2}{R1}\right)}. \tag{2.73}$$

As mentioned above, transistors with enclosed gate layout can prevent current leakage and exhibit improved low frequency noise characteristics. However, drawbacks like, consumption of area, limited device dimensions options and difficulties in approximating accurately the $\frac{W}{L}$ ratio should be mentioned.

3 Total Ionizing Dose (TID) effect on MOS transistors

3.1 Introduction

Radiation effects on CMOS technology have been the objective of research, with recent examples for 130 nm, 65 nm [21], and 28 nm [22] bulk CMOS. Advanced bulk CMOS technologies with thinner gate oxides are considered to be more resilient to radiation exposure [23]. The High-Luminosity Large Hadron Collider (HL-LHC) project at CERN aims to increase the luminosity (number of collisions that occur in a specified time window) of the LHC by a factor of 10. Electronics in the innermost locations of the detector, close to the collision point, are expected to be exposed to a cumulative total ionizing dose (TID) of radiation up to 1 Grad(SiO_2) for 10 years of operation [24]. The 65 nm bulk CMOS node offers valuable trade-offs among performance, radiation tolerance and cost [23, 25]. MOS transistors with enclosed-gate (EG) layouts have shown increased resistance to radiation effects, but also show improved mismatch and low frequency noise properties. The impact of high TID on analog performance in 65 nm bulk CMOS requires further investigation. The benefit of EG layout should be detailed further, and modeling approaches for all the above need to be discussed.

3.2 Physical process of TID effect on MOSFETs

3.2.1 Basic Mechanisms

Ionization is the process by which electrically neutral atoms or molecules are converted to electrically charged atoms or molecules (ions). Ionization is one of the basic mechanism that radiation, such as charged particles and x-rays, interacts with electronics. In general, particles passing through electronic materials deposit a portion of their energy into ionization and the rest into displacement. Some particles, such as neutrons, primarily produce displacement of atoms from their lattice sites, whereas low energy electrons (e.g., 10keV x-rays), give up all their energy into ionization [28]. The SI unit of the total absorbed dose is the *gray* (Gy). Alternatively the *rad* (Radiation absorbed dose) unit can be used ($1gray = 1J/Kg$ and $1rad = 0.01gray$) [26]. Typically, the material in which the dose is deposited must be specified (such as rad(SiO_2)) when using this unit.

3.2.2 Charge yield

High-energy incident photons, electrons, or protons can ionize atoms creating electron-hole pairs [27]. When a MOSFET is exposed to high-energy ionizing radiation, electron-hole pairs are generated at random sites in the SiO_2 lattice. The average energy required to create an electron−hole (e-h) pair in SiO_2 is approximately 18 eV [28, 29]. Table 1 shows the electron-hole pairs concentrations created in both Si and SiO_2 lattice as a result of 1 rad dose exposure. If an electrics field is applied across the oxide, the generated electrons will rapidly drift toward the gate and holes toward the Si/SiO_2 interface. Before all electrons leave the oxide, some fraction of the electrons will recombine with holes in the oxide valence band [30]. This is referred to as initial

recombination. The fraction of electron-hole pairs that escape initial recombination is called electron-hole or charge yield. The amount of initial recombination depends on the magnitude of the electric field and the energy of the incident radiation. Weakly ionizing particles generate relatively isolated charge pairs. Consequently, recombination rate is low. On the other hand, strongly ionizing particles form dense columns of charge resulting into a relatively high recombination rate [31]. In both cases the probability that a hole will recombine with an electron decreases, as the electric field strength increases [28].

Material	Energy demand for 1 e-h pair	Number of e-h generated pairs
Silicon	3.6 eV	1 rad(Si) generates$\backsim 4\,10^{13} pairs/cm^3$
Silicon Dioxide	18 eV	1 rad(SiO_2) generates$\backsim 8.1\,10^{12} pairs/cm^3$

Table 1: Electron-hole pair generation energies for Si and SiO_2

3.2.3 Oxide and Interface traps buildup

Electrons that escape initial recombination are swept out of the oxide towards the corresponding electrodes. The remaining holes move through the SiO_2 lattice by "polaron hopping" as a result of local shallow trap sites [32]. Negative applied gate bias will direct holes to the $GATE/SiO_2$ interface while positive applied gate bias to the Si/SiO_2 interface. Close to the Si/SiO_2 interface oxygen vacancies (lattice defects) acting as trapping centers will capture a significant number of holes. Oxide trapped charges Q_{ot} are positive for both n- and p-type MOSFETs causing negative threshold-voltage shift in either case [30].

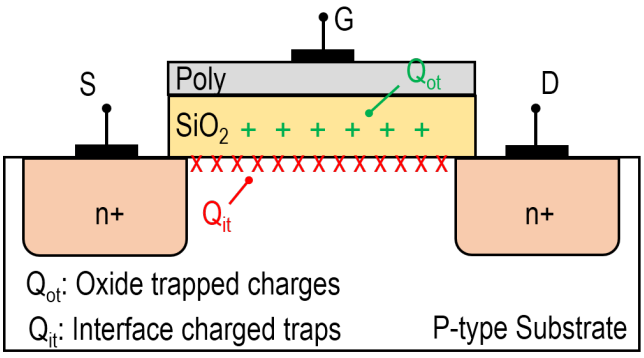


Figure 3.1: Cross section of an n-type MOSFET after irradiation. "+": Oxide trapped charges, positive for n- and p-type MOSFETs. "x": Interface charged traps, negative for n- and positive for p-type MOSFETs

Additionally, radiation introduces the formation of interface traps at the Si/SiO_2 interface [33]. Holes "hopping" through the oxide lattice and charge trapping mechanism near the interface, will release hydrogen ions (H^+) that can drift toward the Si/SiO_2 interface forming electrically active interface traps Q_{it} [27, 30]. Interface traps present energy levels within the silicon band gap and can be charged easily by applying an external bias. Traps close to the valence band act as donors and they are positively charged. On the contrary, traps at the upper level of the band gap are acceptors presenting a negative charge. In a p-channel device interface traps are predominately positive causing a negative threshold voltage shift. Conversely, an n-channel device is mainly affected by negatively charged traps and therefore threshold voltage will be positively shifted [34]. In Figure 3.1 a cross section of an nMOSFET is depicted. Positive oxide trapped charges (Q_{ot}) are labeled with "+" and interface charged traps (Q_{it}) with "x". Oxide- and interface-trap charge compensate each other for n-type and add together for p-type MOSFETs.

Following [35], the total shift of the flat-band voltage resulting from oxide and interface traps can be expressed as

$$\Delta V_{fb} = -\frac{Q_{it} + Q_{ot}}{C_{ox}}. \tag{3.1}$$

Threshold voltage shift due to the change of flat-band voltage can be expressed through (2.17)

$$V_{TB} \triangleq V'_{fb} + \Psi_s + \gamma\sqrt{\Psi_s}, \tag{3.2}$$

where

$$V'_{fb} = \Phi_{MS} + \Delta V_{fb}. \tag{3.3}$$

	Q_t sign	$\Delta V_{fb} = \Delta V_{TB}$
nMOS	+ (oxide trapped charge)	< 0
	- (interface traps)	> 0
pMOS	+ (oxide trapped charge)	< 0
	+ (interface traps)	< 0

Table 2: Oxide trapped charge Q_{ot} and interface trap charge Q_{it} impact on threshold voltage of n- and p-type MOSFETs

Incremental capacitance corresponding to interface traps with respect to surface potential Ψ_s can be expressed as [3]

$$C_{it} \equiv -\frac{d(Q_{it})}{d\Psi_s}. \tag{3.4}$$

In this case slope factor described from (2.18) can be expressed as

$$n = 1 + \frac{C_b + C_{it}}{C_{ox}}, \tag{3.5}$$

where C_b is the depletion region capacitance per unit area.

3.2.4 Parasitic field oxide transistor leakage

Ultra-thin commercial gate oxides can suppress the radiation induced charge build up. Oppositely, in advanced commercial technologies the use of thick field oxides, vulnerable to ionizing radiation, can produce sufficient charge trapping causing field-oxide induced *IC* failure [36]. Two commonly used types of field oxides are: local oxidation of silicon (LOCOS) and shallow-trench isolation (STI). In advanced sub-micron technologies, LOCOS isolation is replaced by STI. In Figure 3.2 the positive charge build up at the edges of STI field oxide is depicted. Similar charge build up can occur, in the so-called "bird's beak" regions, when LOCOS isolation is used [37].

Positive radiation-induced charge accumulation can invert the p-type surface forming an n-type region underneath the field oxide. As the surface inverts, parasitic conduction paths can be generated and therefore the leakage current is increased. Figure 3.2 shows two possible leakage paths for STI. The first (leakage path a) occurs at the edge of gate-oxide transistor between the drain and source diffusions. The second (leakage path b) occurs between the n-type source or drain region of the nMOS transistor and the n-well of the adjacent pMOS device [37]. Since radiation charge build up is primarily positive, the effects is more pronounced in nMOS transistors.

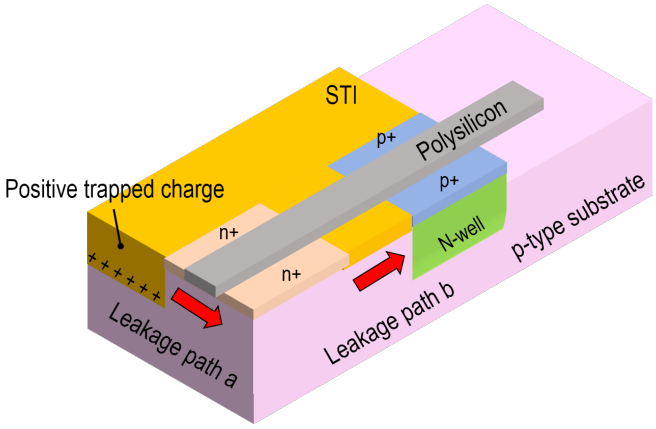


Figure 3.2: Shallow-trench isolated MOSFETs. Possible leakage paths due to positive trapped charge are marked with red arrows

The field oxide forms a parasitic transistor in parallel with the gate oxide transistor. The former consists of the gate polysilicon, a portion of the field oxide and the source

and drain of the gate transistor. Since the thickens of the field oxide is large, the parasitic transistor present a very large threshold voltage in the pre-irradiation (PreRad) state. As positive radiation-induced charge builds up in the field oxide, the threshold voltage of the parasitic transistor is negatively shifted resulting into the increment of the off-state current $I_{D,OFF}$ ($I_D = I_{D,OFF}$ when $V_{DS} = V_{GS} = 0V$), which can significantly add to the drain current of gate oxide transistor. Consequently, the field oxide leakage prevents the gate oxide transistor from being completely turned off, increasing substantially the static supply leakage current of the IC [33, 37].

3.3 Performance degradation overview

TID effects induce several types of performance degradation in MOS transistors such as threshold voltage shift, mobility reduction, subthreshold slope degradation, radiation-modified drain induced barrier lowering and off-state current increment.

Figure 3.3 shows typical effects of TID experiments on transfer characteristics of short-channel n- and p-type saturated MOSFETs, with a moderate channel width ($W = 1um$). Threshold voltage shifts leading to the corresponding on-state current evolution. $I_D = I_{D,ON}$ when $V_{DS} = V_{GS} = 1.2V$. Note that in pMOSFETs, threshold voltage becomes more negative and therefore its absolute value is increased respectively. Leakage current increment at higher TID may be observed in both n- and pMOSFETs, with the latter being less sensitive to the specific effect. Subthreshold slope degradation at increasing TID levels can also be observed.

In Figure 3.4 output characteristics for the same nMOS device are shown. Drain current degradation may exceed 50% for a total ionizing dose of 500 Mrad. The output conductance g_{ds} is also degraded; the impact of high TID is less severe in saturation as compared to conduction.

Figure 3.5 shows gate transconductance g_m versus gate voltage V_{GS} and transconductance to current ratio $\frac{g_m U_T}{I_D}$ versus drain current I_{DS} in saturation regiment ($V_{DS} = 1.2V$). The latter is degraded particular in weak inversion which corresponds to a degradation of the subthreshold slope factor n. Gate transconductance degradation at increasing TID levels is observed.

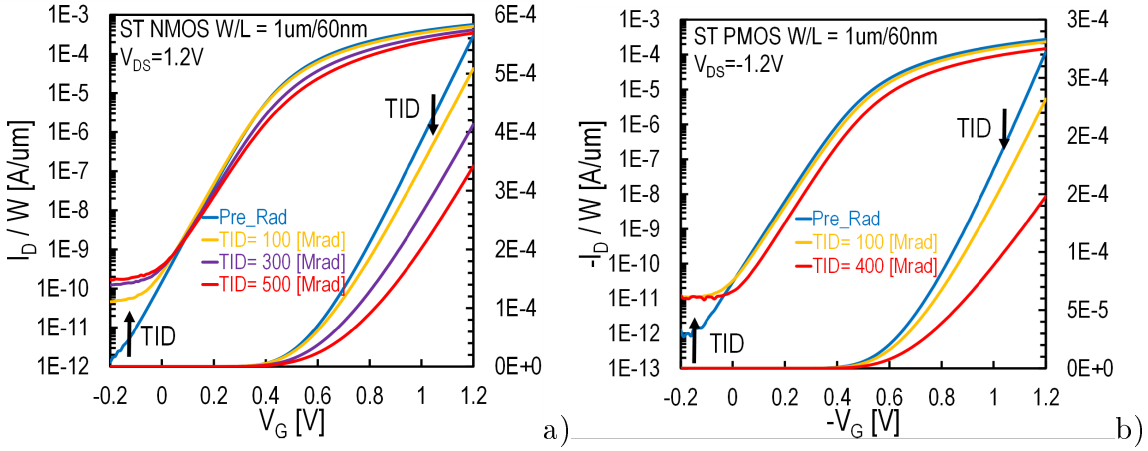


Figure 3.3: Measured transfer characteristics at varying TID for short-channel n- (a) and p - (b) type MOSFETs in saturation ($V_{DS} = |1.2V|$)

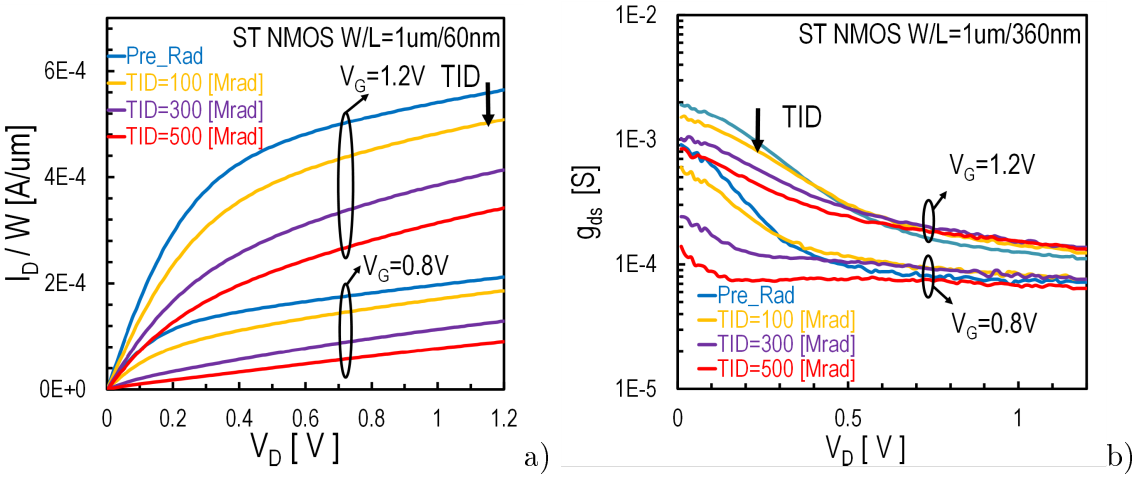


Figure 3.4: Normalized drain current I_D/W (a) and output conductance g_{ds} (b) vs. drain voltage V_{DS} at increasing TID levels for short-channel nMOSFETs in saturation ($V_{DS} = 1.2V$)

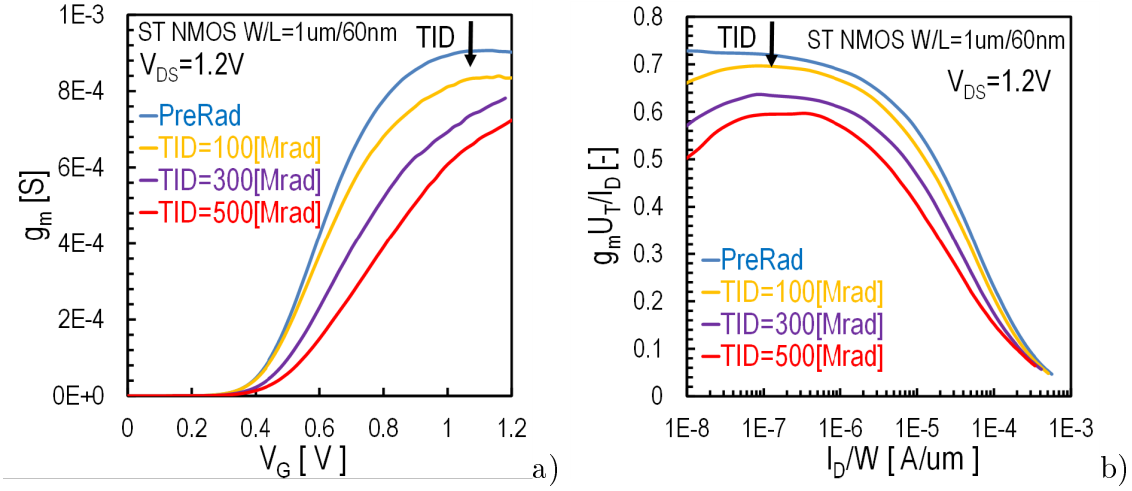


Figure 3.5: Gate transconductance g_m (a) and transconductance-to-current ratio vs. drain current (b) with respect to TID for short-channel nMOSFETs in saturation ($V_{DS} = 1.2V$)

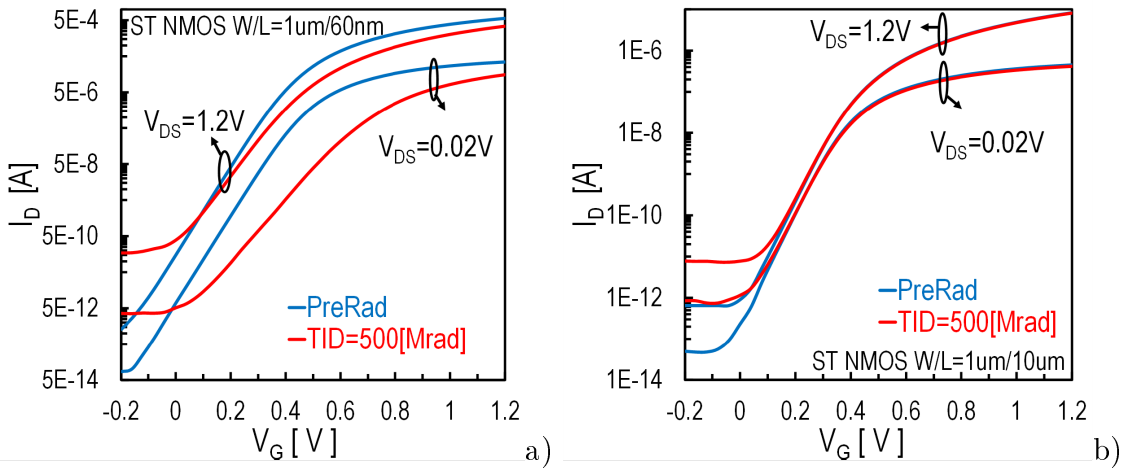


Figure 3.6: Measured transfer characteristics at PreRad state and after 500Mrad TID exposure for short- (a) and long- (b) channel nMOSFETs, in both linear ($V_{DS} = 0.02V$) and saturation ($V_{DS} = 1.2V$) regions

4 Low-Frequency Noise in MOSFETs

4.1 Noise

Noise can be described as random and uncorrelated fluctuations of a signal. Consequently, an instantaneous noise value is unpredictable even if past values are known. In time domain, noise can be described by the average noise power P_{av} while in frequency domain by the Power Spectral Density (PSD). The average power of a noise waveform $x(t)$ is given by [38, 39]

$$P_{av} = lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{T/2} x(t)^2 dt, \tag{4.1}$$

and is expressed in V^2 or $Watt$. The spectrum (PSD) shows how much power a signal carries at each frequency and can be defined as

$$S(f) = lim_{T\to\infty}\frac{|X(f)|^2}{T}. \tag{4.2}$$

$S(f)$ is expressed in V^2/Hz or $Watt/Hz$ and $X(f)$ is the Fourier transform of the noise waveform x(t).

4.2 Noise in MOSFETs

Noise is generated in all semiconductor devices and is perceived as spontaneous random fluctuations in current or in voltage. In MOSFETs, there are several noise mechanisms coming from the channel of the device, related to local random fluctuations of the carrier velocity or the carrier density and they are observed over various frequency ranges [1].

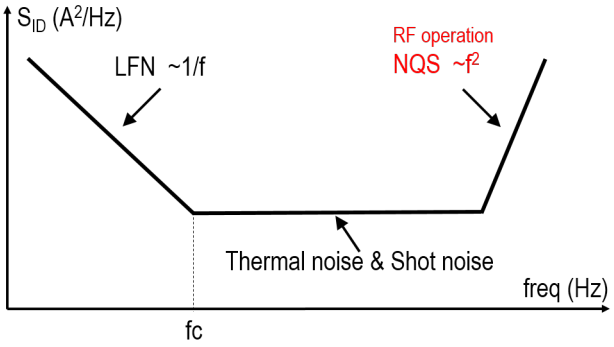


Figure 4.1: Typical drain-referred noise current PSD of a MOSFET

Specifically, noise sources are: Thermal noise, low frequency noise (LFN) or 1/f noise, generation-recombination noise (RTS) and Shot noise. The total noise is thus a superposition of all noise components. In Figure 4.1 the typical PSD of drain current noise is depicted. Thermal noise has no dependence on frequency and so is flat across the entire spectrum while low frequency noise, comes with a power spectra density inverse proportional to the frequency and is dominant in frequencies lower than the corner frequency f_c. f_c is defined as the frequency where LFN and thermal noise have equal PSDs [40]. Low frequency noise consists of 1/f noise and in smaller devices from RTS noise, whereas shot noise is flat across the spectrum. Note that for RF operation, thermal noise is capacitively coupled to the gate of the transistor leading to the so called Non-Quasi-Static (NQS) noise. NQS noise presents a PSD proportional to the square of frequency $\sim f^2$ [41].

Both thermal and low frequency noise can be represented as drain current noise sources (output referred noise) S_{ID}, or gate voltage noise sources (input referred noise) S_{VG} as shown in Figure 4.2.

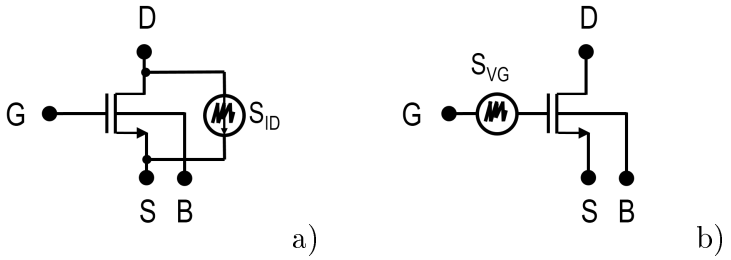


Figure 4.2: Output referred (a) and equivalent input referred (b) noise sources

Usually, output noise is measured as in this work and input noise is calculated. The expressions used for the PSD conversion between drain-referred and gate-referred noise sources are:

$$S_{ID} = S_{VG}\, g_m^2 \;\; (A^2/Hz) \tag{4.3}$$

and

$$S_{VG} = S_{ID}/g_m^2 \;\; (V^2/Hz), \tag{4.4}$$

where g_m is the gate transconductance in Siemens.

4.3 Thermal noise

Thermal noise in a resistive element is caused by random motion of carriers due to thermal excitation and introduces voltage fluctuations, in the voltage measured across the element even if the average current is zero. Thermal noise sometimes called Johnson or Nyquist noise and because of its constant PSD with frequency is also referred as "white noise". Resistor thermal noise voltage PSD is given by

$$S_{VG,R} = 4kTR \ (V^2/Hz) \tag{4.5}$$

where k is the Boltzmann's constant in J/K, T is the absolute temperature in K and R the resistance value in Ohm [38].

MOSFETs also exhibit thermal noise generated in the channel area. The PSD of the drain current fluctuations due to thermal noise can be expressed as

$$S_{ID,thermal} \triangleq 4kT\, G_{nD,} \tag{4.6}$$

where G_{nD} is the thermal noise conductance at the drain and can be approximated as

$$G_{nD} \triangleq \mu \frac{W}{L^2} \int_0^L (-Q_i(x))\, dx = \mu \frac{W}{L^2} |Q_I|. \tag{4.7}$$

Here mobility μ is assumed to be constant. The total mobile charge Q_I can be calculated from

$$Q_I \triangleq W \int_0^L Q_i(x) dx. \tag{4.8}$$

A more practical approximation of thermal noise PSD is given by

$$S_{ID,thermal} = 4kT\, \gamma\, g_m, \tag{4.9}$$

where γ is the thermal noise excess factor that is given by [1]

$$\gamma = \begin{cases} n\frac{1}{2} & WI \, and \, saturation \\ n\frac{2}{3} & SI \, and \, saturation. \end{cases} \tag{4.10}$$

4.4 Shot noise

Shot noise gives rise to white noise spectrum and results from the random arrival of discrete carriers across a pn junction. In weak inversion diffusion dominates channel current. The diffusion current injected by the source-to-substrate junction flows near the surface and is collected by the drain. The PSD of shot noise current related to the diffusion of carriers is given by [42]

$$S_{ID,sh} = 2qI_D, \tag{4.11}$$

where q is the charge of the electron. It should be mentioned that shot noise associated with gate leakage current I_G can be expressed as [43]

$$S_{IG,sh} = 2qI_G. \tag{4.12}$$

4.5 Generation-Recombination (RTS) Noise

Generation-recombination noise in MOSFETs is correlated to trapping sites either within gate oxide or gate oxide-silicon interface. Carrier traps emerge from local defects of the SiO_2 near the silicon substrate due to fabrication imperfections and introduce a trapping-detrapping (capture-emission) mechanism of free charges at or near the Si/SiO_2 interface[44, 45, 46]. Because of a trap presence in the oxide, a free carrier can be displaced from the channel for a short time period and then emitted back. This mechanism is depicted in Figure 4.3.

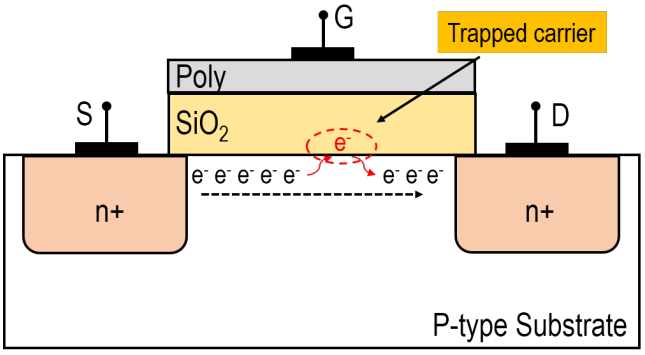


Figure 4.3: Cross section of an nMOSFET showing a trapped carrier near the Si/SiO_2 interface

Structural defects are caused by dangling bonds of silicon atoms that are not bounded to other oxygen or silicon atoms. This lattice discontinuity creates energy levels in the band-gap of the semiconductor acting as generation recombination centers or traps.

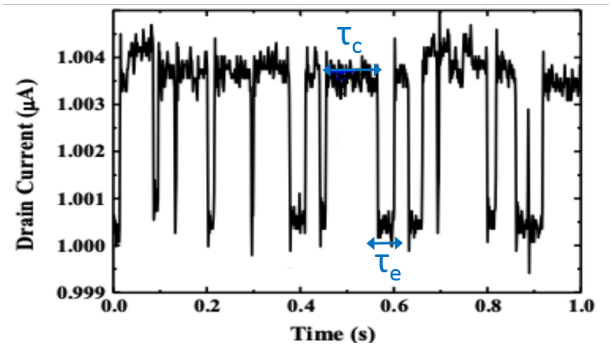


Figure 4.4: Drain current Random Telegraph Signal noise in time domain. Capture (τ_c) and emission (τ_e) time constants are shown

In time domain, each trapping-detrapping event associated with a single trap, give rise to a random telegraph signal (RTS). An RTS exhibits two discrete levels; the upper level corresponds to an empty trap, where τ_c denotes the average time it takes to capture a carrier, while the lower level to an electron occupied state, with τ_e to be the average time needed to release the carrier [47] (Figure 4.4). Each trap is characterized by a relaxation time constant τ that can be expressed as

$$\tau = \frac{1}{\frac{1}{\tau_c} + \frac{1}{\tau_e}}. \tag{4.13}$$

RTS noise is dominant in small area MOS devices where the number of traps is relatively low and therefore individual carrier trapping is enhanced [48]. An RTS is associated with a Lorentzian frequency spectrum as shown in Figure 4.5. A Lorentzian power spectrum is characterized by a constant power spectral density at low frequencies, the so called Lorentzian plateau [49], and a roll-off with f^2 at frequencies higher than f_c frequency. A Lorentzian PSD is given by

$$S_{ID} = \frac{A}{\left(1 + \frac{f}{fC}\right)^2}, \quad (V^2/Hz) \tag{4.14}$$

where A is the amplitude factor and f_c the roll-off frequency.

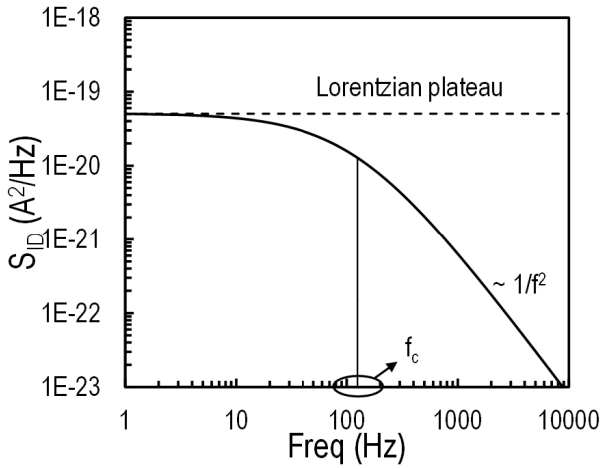


Figure 4.5: Typical Lorentzian PSD of an RTS. Corner frequency (f_c) is indicated

4.6 Flicker Noise

Flicker or $1/f$ noise is characterized by a PSD that is inversely proportional to frequency and dominates in low frequencies beyond the so called corner frequency. Because the $1/f$ noise scales inversely proportional to the gate area and varies significantly across processes and process generations, it is becoming a major issue for analog IC design in deep sub-micron technology nodes. Figure 4.6 shows the typical measured LFN spectrum of a saturated nMOSFET ($V_{DS} = 1.2V$).

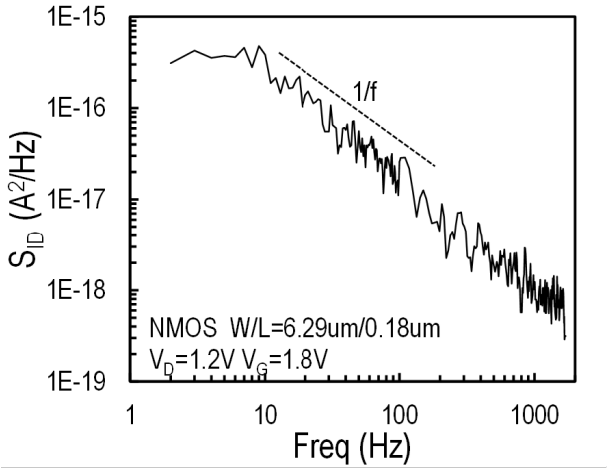


Figure 4.6: Measured low frequency noise spectrum of an nMOSFET with $W/L = 6.29um/60nm$ in strong inversion ($V_{GS} = 1.8V$) and saturation ($V_{DS} = 1.2V$).

Basic mechanisms of flicker noise are; carrier number fluctuation, carrier mobility fluctuation and series resistance fluctuation. In literature, the most common equation describing $1/f$ noise is [50]

$$S_{VG} = \frac{K_F}{C_{ox}^2 W L f^{AF}}, \tag{4.15}$$

where K_F is the flicker noise factor with units of C^2/cm^2. K_F typical values ranging from 10^{-33} to $10^{-29}\, C^2/cm^2$. AF exponent is added to consider the deviation from the ideal $1/f$ slope with values from 0.8 to 1.2 [4, 51].

4.7 Carrier number fluctuation with correlated mobility fluctuations theory

Carrier number fluctuation theory (ΔN), also known as Mc Worther theory, describes flicker noise as a result of mobile carriers trapping and detrapping near the Si/SiO_2 interface and it is strongly correlated to the generation-recombination (RTS) noise process. As mentioned above, every single trap will modulate the total drain current with a Lorentzian spectrum that is characterized by a specific roll-off frequency f_c. A trap is an energy state in the band-gap with an energy level between conduction-band energy level E_c and valence-band energy level E_V. The activity of a trap is maximum when its energy level is close to Fermi level. A generation of an RTS can be attributed to the flowing effects. Firstly, the captured electron takes no further part in the conduction process, resulting to carrier number fluctuation (ΔN) effect. Secondly, a captured elector will make the trap more negatively charged. Consequently, the position of the channel will be modulated accordingly. This is known as Coulomb scattering or $\Delta\mu$ effect, causing mobility of the carriers (μ) to fluctuate. The second mechanism causes larger drain current variation compared to that deriving from ΔN effect [47] .

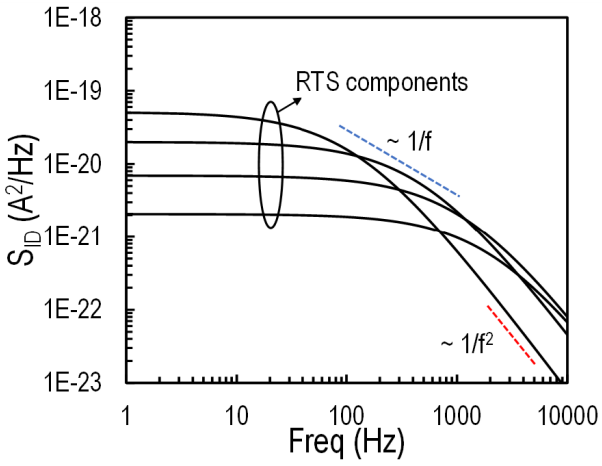


Figure 4.7: Superposition of Lorentzian components forming the $1/f$ slope of LFN

Shallower traps will lead to shorter time constants and higher roll-off frequencies while deeper traps to longer time constants and lower roll-off frequencies . A uniform spatial trap distribution, will result to uniformly distributed time constants and therefore the superposition of different Lorentzian components will create a PSD inversely proportional to the frequency, typical of 1/f noise [52]. In Figure 4.7 a simplified approach of this mechanism is represented. In literature carrier number fluctuation model is commonly expressed as (FBP approach) [40, 53, 54, 55]

$$\frac{S_{ID}}{I_D^2} = \frac{kTq^2 N_T \lambda}{C_{ox}^2 WLf} \left(\frac{g_m}{I_D}\right)^2 \left(1 + a_c \mu C_{ox} \frac{I_D}{g_m}\right)^2, \tag{4.16}$$

where N_T is the oxide volumetric trap density per unit energy in $eV^{-1}\,cm^{-3}$, f is the frequency, λ is the tunneling attenuation distance ($\approx 0.1\,nm$ for SiO_2), kT the thermal energy, a_c the Coulomb scattering coefficient and μ the carrier mobility. N_T typically ranges from 10^{14} to $10^{18}/eV^{-1}\,cm^{-3}$ and a_c 10^4 to $10^5 VsC^{-1}$.

4.8 LFN charge based modeling approach

The total PSD of $1/f$ noise at the drain can be obtained from the sum of two different LFN contributors, carrier number fluctuation (ΔN) and mobility fluctuation ($\Delta\mu$) effect, as follows

$$\frac{S_{\Delta I_{nD}^2}}{I_D^2} = \frac{S_{\Delta I_{nD}^2}}{I_D^2}|_{\Delta N} + \frac{S_{\Delta I_{nD}^2}}{I_D^2}|_{\Delta\mu}. \tag{4.17}$$

In the next sections both noise mechanisms will be expressed with respect to the charge-based modeling approach.

4.8.1 Mc Worther model

Considering an elementary channel section comprised between x and $x+\Delta x$, if a number of carriers get trapped at position x the relative current fluctuation can be expressed as

$$\frac{\delta I_D(x)}{I_D} = \frac{\delta N}{N} + \frac{\delta \mu}{\mu}. \tag{4.18}$$

Following [1] Equation (4.18) can be written as

$$\frac{\delta I_D(x)}{I_D}|_{\Delta N} = \left(\frac{1}{q_i + 1/2} + a\,\mu\right)\frac{\delta N_t}{N_{spec}}, \tag{4.19}$$

where

$$N_{spec} \triangleq -\frac{Q_{spec}}{q}, \tag{4.20}$$

$N_t \triangleq -\frac{Q_t}{q}$ is the number of total trapped carriers in position x, Q_t is the total trapped charge density and μ the carrier mobility. Coefficient a is related to Coulomb scattering coefficient a_c as follows

$$a \triangleq a_c(-Q_{spec}) = \widehat{a}N_{spec}. \tag{4.21}$$

The related PSD of the local noise current source δI_n normalized to the square of the drain current I_D can be expressed as

$$\frac{S_{\delta I_n^2}}{I_D^2}|_{\Delta N} = \left(\frac{1}{q_i + 1/2} + a\,\mu\right)^2\frac{S_{\delta N_t^2}}{N_{spec}^2}, \tag{4.22}$$

where $S_{\delta N_t^2}$ is the PSD of the the trap charge density fluctuation, depending on trapping mechanisms in the oxide and is defined by [1, 55, 56]

$$S_{\delta N_t^2} = \frac{kT\lambda N_T}{W\Delta x f} \tag{4.23}$$

and

$$N_T \triangleq \frac{N_t}{\lambda kT}. \tag{4.24}$$

The fluctuation of the drain current related to elementary section Δx given by

$$\frac{S_{\delta I_{nD}^2}}{I_D^2}|_{\Delta N} = \left(\frac{\Delta x}{L}\right)^2\frac{S_{\delta I_n^2}}{I_D^2}|_{\Delta N} \tag{4.25}$$

and by substituting (4.22) in (4.25) the following can be obtained

$$\frac{S_{\delta I^2_{nD}}}{I^2_D}|_{\Delta N} = \left(\frac{\Delta x}{L}\right)^2 \frac{S_{\delta I^2_n}}{I^2_D}|_{\Delta N} = \left(\frac{\Delta x}{L}\right)^2 \left(\frac{1}{q_i + 1/2} + a\,\mu\right)^2 \frac{S_{\delta N^2_t}}{N^2_{spec}}. \tag{4.26}$$

The PSD of the total fluctuation of the drain current due to carrier number fluctuation (ΔN) effect, can be obtained by integration along the channel as follows

$$\frac{S_{\Delta I^2_{nD}}}{I^2_D}|_{\Delta N} = \int_0^L \left(\frac{\Delta x}{L}\right)^2 \left(\frac{1}{q_i + 1/2} + a\,\mu\right)^2 \frac{S_{\delta N^2_t}}{N^2_{spec}} dx$$

$$= \frac{1}{L^2}\int_0^L \Delta x \left(\frac{1}{q_i + 1/2} + a\,\mu\right)^2 \frac{S_{\delta N^2_t}}{N^2_{spec}} dx$$

$$= \frac{1}{L^2}\frac{S_{\delta N^2_t}}{N^2_{spec}}\int_0^L \Delta x \left(\frac{1}{q_i + 1/2} + a\,\mu\right)^2 dx = S_D|_{\Delta N}\, K_D|_{\Delta N}, \tag{4.27}$$

where

$$S_D|_{\Delta N} = \frac{q^4 \lambda N_T}{kTWLn^2 C^2_{ox} f}. \tag{4.28}$$

Assuming that $S_D|_{\Delta N}$ is weakly bias dependent most of the bias dependence is accounted for by the unitless factor $K_D|_{\Delta N}$ defined by

$$K_D|_{\Delta N} \triangleq \frac{1}{4}\int_0^1 \left(\frac{1}{q_i + 1/2} + a\,\mu\right)^2 d\xi$$

$$= \frac{1}{4i_d}\int_{qd}^{qs} \left(\frac{1}{q_i + 1/2} + a\,\mu\right)^2 (2q_i + 1)\, dq_i$$

$$= \frac{1}{2i_d} ln\left(\frac{1 + 2q_s}{1 + 2q_d}\right) + \frac{a\,\mu}{1 + q_s + q_d} + \left(\frac{a\,\mu}{2}\right)^2, \tag{4.29}$$

where q_s and q_d are the normalized inversion charges at the source and drain end of the channel respectively and i_d is the normalized drain current (IC) (2.49). It should be mentioned that the position x in the channel is normalized according to $\xi = \frac{x}{L}$ and i_d can be expressed as [1]

$$i_d = (2q_i + 1)\frac{dq_i}{d\xi}. \tag{4.30}$$

Figure 4.8 shows the bias-dependent factor $K_D|_{\Delta N}$ versus IC for two different values of the product $a\,\mu$ in forward saturation ($q_d = 0$). In SI q_s, $q_d \gg 1$ and $K_D|_{\Delta N}$ is reduced to

$$K_D|_{\Delta N} \backsimeq \left(\frac{a\,\mu}{2}\right)^2, \tag{4.31}$$

whereas in WI q_s, $q_d \ll 1$ and $K_D|_{\Delta N}$ can be approximated by

$$K_D|_{\Delta N} \backsimeq \left(1 + \frac{a\,\mu}{2}\right)^2. \tag{4.32}$$

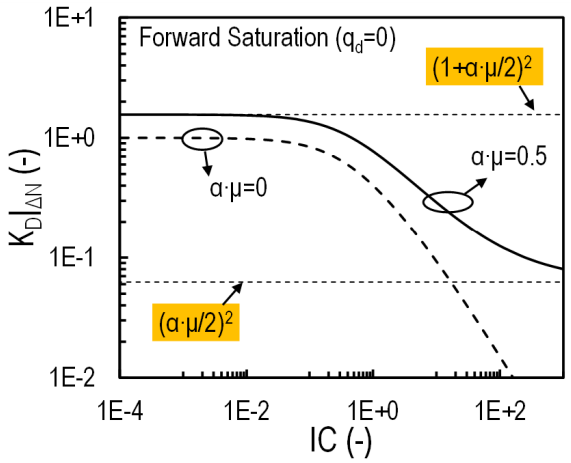


Figure 4.8: Bias-dependent factor $K_D|_{\Delta N}$ versus IC in forward saturation ($q_d = 0$). Solid line: $a\,\mu = 0.5$. Long dashed: $a\,\mu = 0$

4.8.2 Hooge model

Mobility fluctuation effect ($\Delta\mu$) first proposed by Hooge [57], relates $1/f$ noise with mobility fluctuations of the mobile carriers. $\Delta\mu$ effect on drain current related to elementary section Δx of the channel is expressed as [1, 56]

$$\frac{S_{\delta I^2_{nD}}}{I_D^2}|_{\Delta\mu} = \left(\frac{\Delta x}{L}\right)^2 \frac{S_{\delta I^2_n}}{I_D^2}|_{\Delta\mu} = \frac{\Delta x a_H q}{WL^2(-Q_i)f}, \tag{4.33}$$

where a_H is the unitless Hooge parameter typically ranges from 10^{-4} to 10^{-6}.

The PSD of the total fluctuation of the drain current due to $\Delta\mu$ effect can be obtained from

$$\frac{S_{\Delta I_{nD}^2}}{I_D^2}|_{\Delta\mu} = S_D|_{\Delta\mu}\, K_D|_{\Delta\mu}, \tag{4.34}$$

with

$$S_D|_{\Delta\mu} = \frac{a_H q^2}{kTWLnC_{ox}f}. \tag{4.35}$$

The bias-dependence factor $K_D|_{\Delta\mu}$ is defined as

$$K_D|_{\Delta\mu} \triangleq \int \frac{1}{2q_i(\xi)} d\xi = \frac{1}{i_d}\int_{qd}^{qs} \left(1 + \frac{1}{2q_i}\right) dq_i$$

$$= \frac{1}{i_d}\left[q_s - q_d + \frac{1}{2} ln\left(\frac{q_s}{q_d}\right)\right]$$

$$= \frac{1}{1 + q_s + q_d}\left[1 + \frac{ln\left(q_s/q_d\right)}{2\left(q_s - q_d\right)}\right]. \tag{4.36}$$

In Figure 4.9 the bias-dependent factor $K_D|_{\Delta\mu}$ is plotted versus IC in forward saturation assuming $q_s = 200q_d$. The WI and SI asymptotes are also depicted. Following [1] in SI $K_D|_{\Delta\mu}$is approximated by

$$K_D|_{\Delta\mu} \backsimeq \frac{1}{q_s + q_d}, \tag{4.37}$$

whereas in WI

$$K_D|_{\Delta\mu} \backsimeq \frac{ln(q_s/q_d)}{2(q_s - q_d)}. \tag{4.38}$$

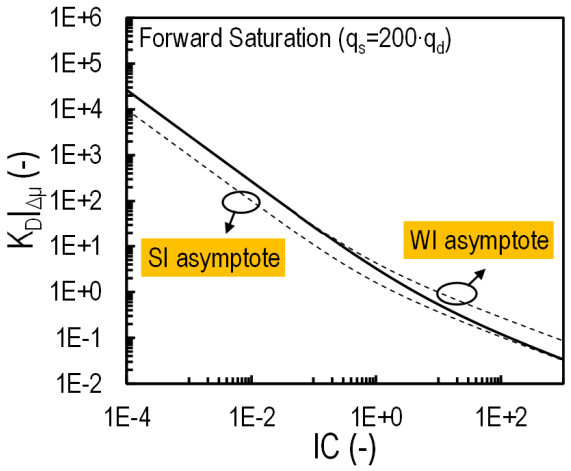


Figure 4.9: Bias-dependent factor $K_D|_{\Delta\mu}$ versus IC in forward saturation assuming $q_s = 200q_d$. Solid line: model. Dashed lines: WI, SI asymptotes

4.9 Statistical charge based $1/f$ noise model

Basic contributors to the variability of LFN are, carrier number fluctuation (ΔN) and mobility fluctuation ($\Delta\mu$) effects through the variation of trap density N_T and Hooge parameter a_H respectively. According to (4.17) the mean value of total $1/f$ noise is calculated by adding ΔN and $\Delta\mu$ effects. Consequently, the total variance of $1/f$ noise is given by [59]

$$Var\left(WLf\frac{S_{\Delta I^2_{nD}}}{I^2_D}\right) = Var\left(WLf\frac{S_{\Delta I^2_{nD}}}{I^2_D}|_{\Delta N}\right) + Var\left(WLf\frac{S_{\Delta I^2_{nD}}}{I^2_D}|_{\Delta\mu}\right). \quad (4.39)$$

4.9.1 Variance of $1/f$ noise due to ΔN effect

As mentioned above, variance of $1/f$ noise as a result of ΔN effect arises because of the statistical deviation of trap density N_T. The total number of traps N_{tr} can be expressed as

$$N_{tr} \triangleq WLN_t, \quad (4.40)$$

where N_t is related to N_T through (4.24). Number of traps follow a Poisson distribution and therefore the following can be obtained [60, 61]

$$\sigma^2_{N_{tr}} = WLN_t. \tag{4.41}$$

Following [59], the normalized PSD $WLf\frac{S_{\delta I_n^2}}{I_D^2}|_{\Delta N}$ of a local noise source due to ΔN effect, using (4.22), (4.23) and (4.40), is defined as

$$\frac{S_{\delta I_n^2}}{I_D^2}|_{\Delta N} = \left(\frac{1}{q_i + 1/2} + a\,\mu\right)^2 \frac{N_{tr}}{W\Delta x N_{spec}^2}. \tag{4.42}$$

Local noise sources are considered uncorrelated [1, 58, 59]; thus, the statistical sum-up of the variability of each noise source leads to the total $1/f$ variance. The total LFN variance due to carrier number fluctuation, in terms of the inversion charge densities q_s and q_d, is given by [59]

$$Var\left(WLf\frac{S_{\Delta I_{nD}^2}}{I_D^2}|_{\Delta N}\right) = \frac{N_t}{WLN_{spec}^4}\Lambda_D|_{\Delta N}, \tag{4.43}$$

where

$$\Lambda|_{\Delta N} = \left[\begin{array}{c} \frac{1}{(q_S+0.5)^2(q_d+0.5)^2} + (a\,\mu)^4 + \frac{8(a\,\mu)^3}{1+q_s+q_d} \quad + \\ \frac{12(a\,\mu)^2}{i_d} ln\left(\frac{q_s+0.5}{q_d+0.5}\right) + \frac{8(a\,\mu)}{(q_S+0.5)(q_d+0.5)(1+q_s+q_d)} \end{array}\right] \tag{4.44}$$

and i_d is the normalized drain current described by (2.49).

4.9.2 Variance of $1/f$ noise due to $\Delta\mu$ effect

Hooge parameter a_H is related to the number of traps N_{tr} as [62, 63]

$$a_H = \frac{2qN_{tr}}{WLQ_{spec}v_p}, \tag{4.45}$$

where v_p is the pinch off voltage. Equation (4.33) in terms of normalized mobile charge q_i can be expressed as [62]

$$WLf\frac{S_{\delta I_{nD}^2}}{I_D^2}|_{\Delta\mu} = \frac{a_H qWL}{q_i W\Delta x N_{spec}}, \tag{4.46}$$

where $WLf\frac{S_{\delta I_n^2}}{I_D^2}|_{\Delta\mu}$ is the normalized PSD of a local noise source due to $\Delta\mu$ effect. The total $1/f$ variance due to mobility fluctuation, can be expressed as [59]

$$Var\left(WLf\frac{S_{\Delta I_{nD}^2}}{I_D^2}|_{\Delta\mu}\right) = \frac{a_H}{q_i WLN_{spec}^3}\frac{1}{i_d}\left(2ln\left(\frac{q_s}{q_d}\right)+\frac{q_s-q_d}{q_s q_d}\right) \tag{4.47}$$

where q_s and q_d are the normalized inversion charges at the source and drain end of channel respectively and i_d is the normalized drain current described from (2.49).

4.9.3 Standard deviation of $\sigma\left(ln\left(WLS_{ID}f/I_D^2\right)\right)$ of $1/f$ noise

Considering the log normal distribution of LFN amplitude [64, 65], the standard deviation of the logarithm of LFN can be related to its variance $Var\left(WLfS_{ID}/I_D^2\right)$ and mean value $E\left(WLfS_{ID}/I_D^2\right)$, according to [62, 64]

$$\sigma\left(ln\left(WLS_{ID}f/I_D^2\right)\right) = \sqrt{ln\left[1+\frac{Var\left(WLfS_{ID}/I_D^2\right)}{E\left(WLfS_{ID}/I_D^2\right)}\right]}, \tag{4.48}$$

where variance is given by (4.39) and mean value from (4.17).

Equations (4.39), (4.44), (4.47) and (4.48) describe a statistical charged based $1/f$ noise model. The statistical model uses parameters N_T, a_C and a_H of the physical model, but provides additional flexibility by using adjusted values

$$N_{TS} \equiv E_{NT}N_{T,} \tag{4.49}$$

$$a_{CS} \equiv E_{aC}a_{c,} \tag{4.50}$$

$$a_{HS} \equiv E_{aH}a_{H,} \tag{4.51}$$

which are required to adjust noise statistics [59, 62].

5 Experimental procedures and results

5.1 TID experimental setup on $65nm$ CMOS

A set of transistors in arrays covering different width and length ranges, of $65nm$ bulk CMOS process with nominal supply voltage of $1.2V$ were fabricated. Devices comprise standard threshold voltage transistors of both kind (n- and p-type MOSFETs) standard and enclosed gate layout. Irradiation with an X-ray source ($10keV$) and measurements were carried out at CERN. Devices were exposed to radiation levels up to $500\,Mrad(SiO2)$ at a very high dose rate of $9\,Mrad/h$. During irradiation, drain and gate terminals are biased under worst degradation conditions ($|V_{GS}| = |V_{DS}| = |V_{DD}| = 1.2V$) for TID experiments [21, 36]. Devices are first measured at pre-irradiation (PreRad) conditions, irradiated up to $100Mrad$, measured again, irradiated up to $200Mrad$, measured newly etc. up to $500Mrad$. At each targeted TID, irradiation is stopped, and identical DC characterization is performed, keeping the samples at the same temperature (25^oC). Possible annealing effects are not accounted for in the present study. Figure 5.2 shows the experimental setup at CERN, composed of a temperature controlled wafer prober, a probe card, the X-ray source, a switching matrix, and a semiconductor parameter analyzer.

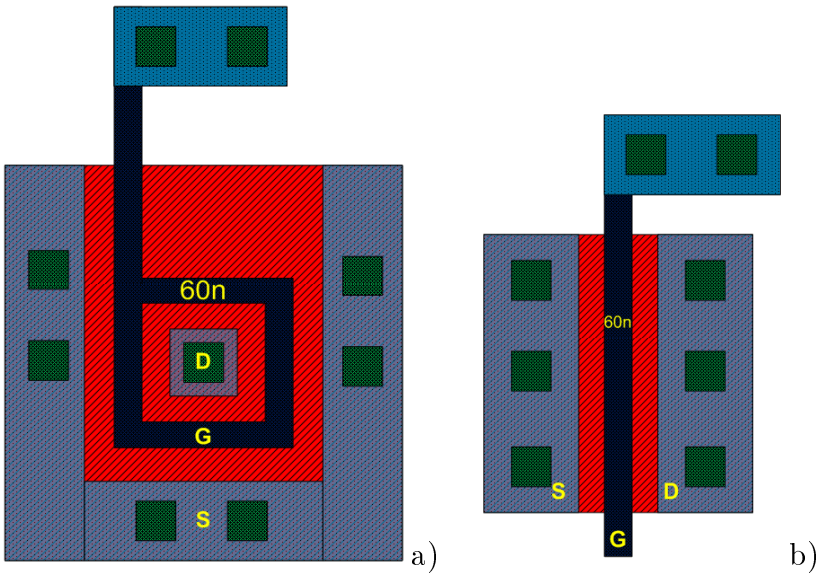


Figure 5.1: Layout of MOS transistors with enclosed (a) and standard (b) gate of an experimental $65nm$ bulk CMOS process

EG transistors with a tetragonal layout, operated with drain at the center as shown in Figure 5.1, have their widths varying according to their channel length, ranging from L = 60nm to several um. Standard (ST) transistors considered here have a fixed width

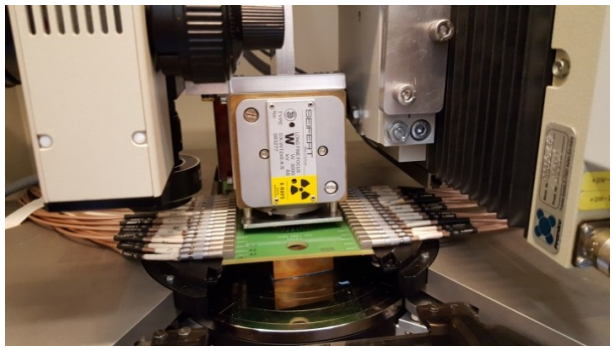
of W=1um and variable length. The incidence of channel width and temperature effects will be considered elsewhere. Measured IV characteristics comprise transfer characteristics in linear ($|V_{DS}| = 20mV$) and saturation ($|V_{DS}| = 1.2V$) regimes, and output characteristics.

ST MOSTs	$W\,(um)$	1	1	1	1	1	1	1	1
	$L\,(um)$	0.06	0.12	0.24	0.36	0.48	0.6	1	10

Table 3: Tested ST MOSFETs list. Fixed $W = 1um$

EG MOSTs	$W\,(um)$	1.32	1.42	1.63	1.84	2.43	3.42	8.95
	$L\,(um)$	0.06	0.12	0.24	0.36	0.6	1	4

Table 4: Tested EG MOSFETs list. Widths varying according to channel length


a)


b)

Figure 5.2: (a)$10keV$ X-ray source and 32-channel probe card mounted on a temperature- controlled prober at CERN. (b) Complete setup with the cabinet for irradiation experiments in the center, Keithley SCS 4200 semiconductor characterization system and switching matrix with temperate controller to right

5.2 Geometrical scaling of basic electrical parameters

The main electrical parameters under examination are threshold voltage V_{TH}, drain induced barrier lowering $DIBL \equiv -dV_{TH}/dV_{DS}$, subthreshold slope factor n, and mobility. For the extraction of threshold voltage V_{TH}, the "Adjusted Constant Current" (ACC) method is used [9]. This method provides an adaptation of the current criterion depending on V_{DS} conditions, an important aspect in correctly estimating DIBL, a key parameter for analog performance. Quantities such as intrinsic gain $A_V = g_m/g_{ds}$, are governed mostly by DIBL. In the following, examples are provided for selected individual transistors. Length-scaling effects are then examined in detail. Comparisons among standard and enclosed-gate layout transistors are provided.

Figure 5.3 shows typical effects of TID experiments on transfer characteristics of saturated ($|V_{DS}| = 1.2V$) short-channel n- and p-type MOSFETs with a moderate channel width. Well-known decrease of mobility, threshold voltage shift, degradation of subthreshold slope (particularly ST nMOS transistors), and increase in leakage current with increasing TID can be observed. While pMOSTs typically show a reduced sensitivity, EG transistors show overall significantly reduced effects with TID.

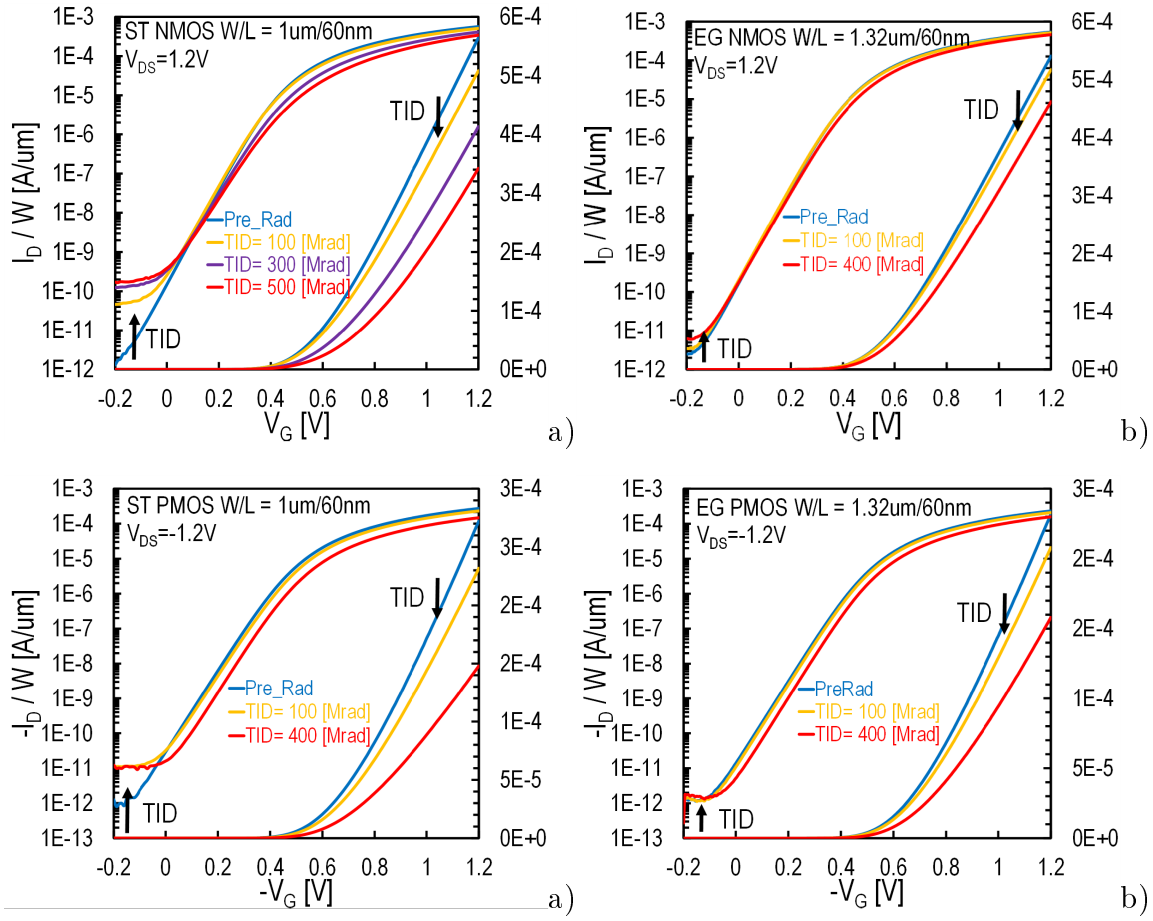


Figure 5.3: Measured transfer characteristics at varying TID for short-channel ST and EG n- and p-MOSFETs in saturation ($V_{DS} = |1.2V|$)

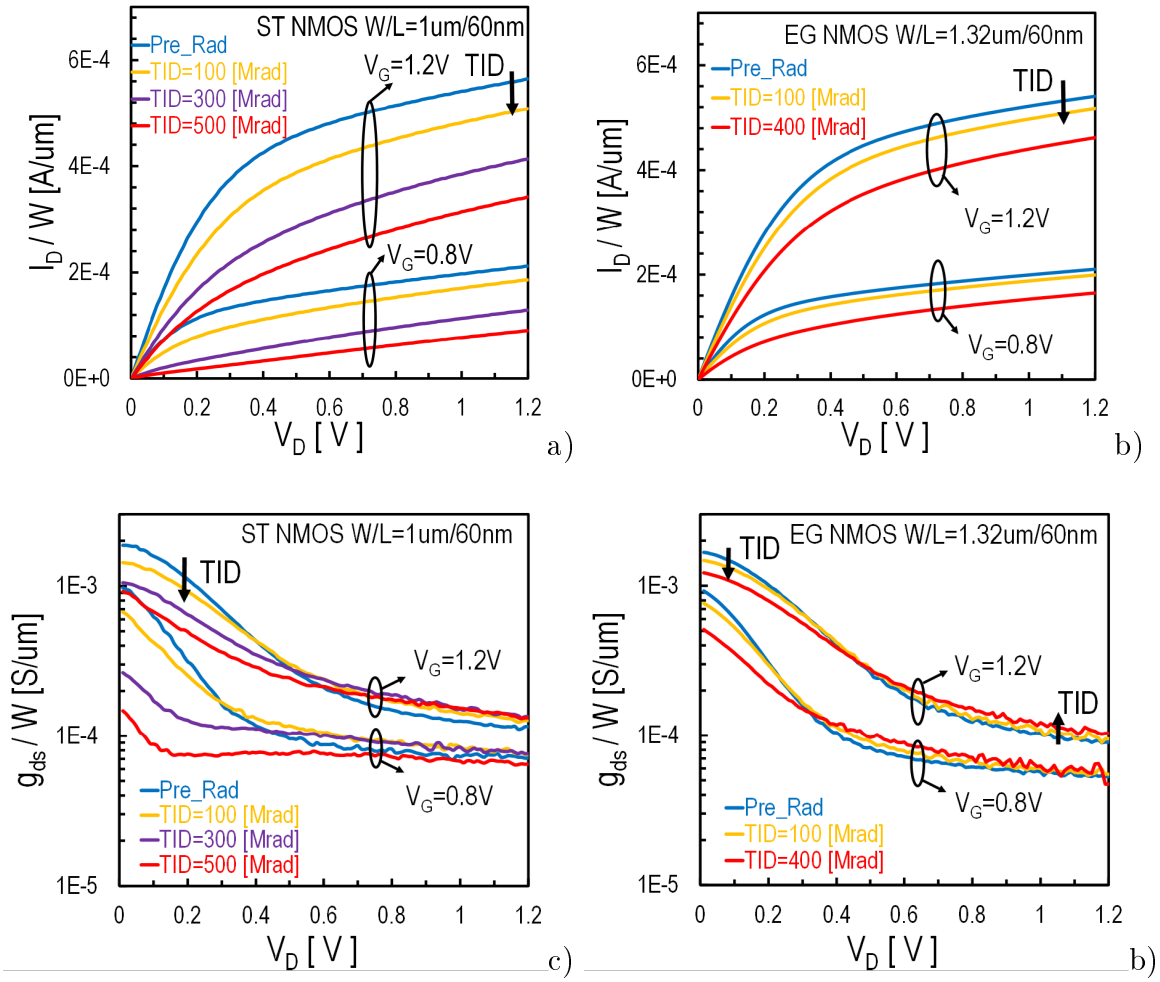


Figure 5.4: Normalized drain current I_D/W and output conductance g_{ds} vs. drain voltage V_{DS} at increasing TID levels for short-channel nMOSFETs with ST (a, c) and EG (b, d) layouts, in saturation ($V_{DS} = 1.2V$)

Figure 5.4 shows that drain current degradation of ST nMOSFETs may reach 50% for a TID of $500Mrad$, while EG transistors show reduced losses on the order of 20% . Output conductance is also degraded.

In Figure 5.5 the normalized transconductance-to-current ratio $g_m U_T/I_D$ versus drain current is depicted. The former is degraded, particular in weak inversion, which corresponds to a degradation of the subthreshold slope factor n.

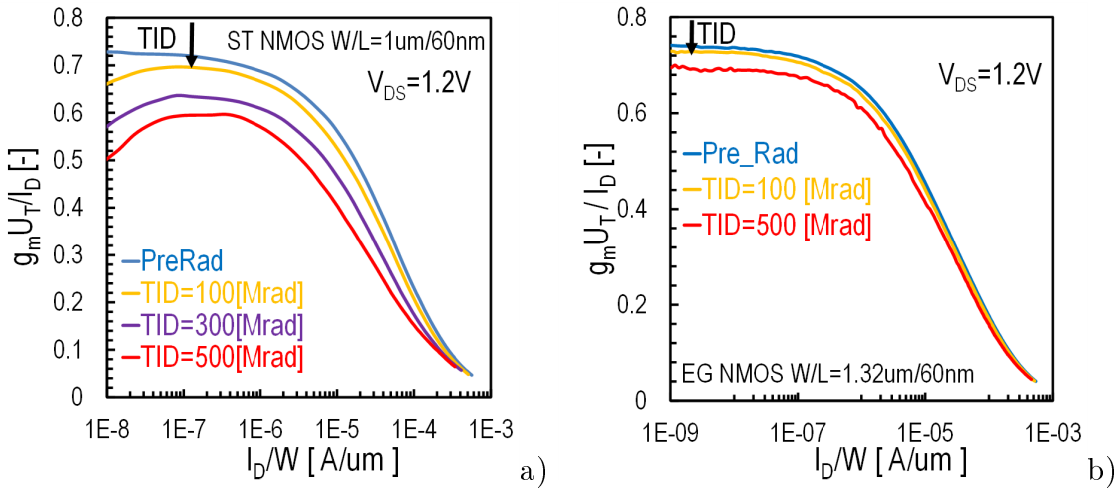


Figure 5.5: Transconductance-to-current ratio $g_m U_T/I_D$ vs. normalized drain current I_D/W with respect to TID for short-channel nMOSFETs with ST (a) and EG (b) layouts, in saturation ($V_{DS} = 1.2V$)

Figure 5.7 shows threshold voltage V_T in saturation and linear modes versus channel length L, and the impact of TID according to the type and layout of transistors. Clearly, the linear mode threshold voltage exhibits a strongly increased RISCE [21] with TID in nMOSFETs, while saturated transistors are much less affected.

In Fig 5.8, the resulting DIBL effect derived from the data in Figure 5.7 is presented. DIBL effect is most sensitive to TID in ST nMOSFETs. Significantly lower DIBL is observed in EG vs. ST layout devices. For short channel nMOSTs, DIBL worsens with TID, and shows a $1/L$ dependence. EG pMOSFETs are insensitive to TID at all channel lengths.

In Figure 5.9, the subthreshold slope n is examined. The degradation of slope factor n for ST nMOSFETs with increasing TID is prominent at all channel lengths. The same phenomenon is significantly less pronounced for ST pMOSTs. For both channel types, the EG layout transistors show definitely better slope factor, at pre-rad as well as at high TID conditions.

The combination of lower DIBL (and better slope factor) should lead to improved intrinsic gain $A_V = g_m/g_{ds}$, as is indeed confirmed in Figure 5.10. Note that here, the intrinsic gain is evaluated around-threshold, with an inversion coefficient of about unity. ST nMOSFETs show a clear sensitivity to high TID. EG n-MOSTs show an improved intrinsic gain, combined with reduced sensitivity to TID. The scaling of $A_V \backsimeq L^{3/2}$ can be observed. Overall, the intrinsic gain is mainly dictated by the behavior of DIBL. Improvement of A_V is observed at shorter channel length according to $\sim L$, while Av scaling levels off at longer channel lengths due to so-called drain-induced threshold shift (DITS).

Figures 5.11 and 5.12 provide an evaluation of on-state ($|V_G| = |V_D| = 1.2V$) and off-state ($|V_G| = 0V$, $|V_D| = 1.2V$) currents versus channel length. The observed I_{off} scaling is expected and coherent with the behavior of threshold voltage. On-state

current degradation at shorter channel length is also impacted by mobility and velocity saturation effects, which are more pronounced for nMOSTs as compared to pMOSTs.

5.2.1 Threshold voltage

Threshold voltage extraction from measured data is determined by using the "Adjusted Constant-Current Method" (ACC) [9]. This method provides an adaptation of the current criterion depending on V_{DS} bias conditions. As described in Section 2.5, drain current in all operating regions can be expressed as $I_D = I_{spec}\,(q_s^2 + q_s - q_d^2 - q_d)$. Additionally, following (2.48), the normalized inversion charge at any point of the channel q_{ch} can be expressed as

$$2q_{ch} + lnq_{ch} = v_{ch} - v_{ch} \Longleftrightarrow$$

$$e^{(2q_{ch}+lnq_{ch})} = e^{(v_p - v_{ch})} \Longleftrightarrow$$

$$q_{ch}e^{2q_{ch}} = e^{(v_p - v_{ch})} \Longleftrightarrow$$

$$2q_{ch}e^{2q_{ch}} = 2e^{(v_p - v_{ch})} \Longleftrightarrow$$

$$2q_{ch} = LambertW\left[2e^{(v_p - v_{ch})}\right] \Longleftrightarrow$$

$$q_{ch} = \frac{1}{2} LambertW\left[2e^{(v_p - v_{ch})}\right]. \tag{5.1}$$

Thus, inversion charges at source and drain end of the channel can be evaluated as

$$q_s = \frac{1}{2} LambertW\left[2e^{\left(\frac{V_P - V_S}{U_T}\right)}\right],\ q_d = \frac{1}{2} LambertW\left[2e^{\left(\frac{V_P - V_D}{U_T}\right)}\right]. \tag{5.2}$$

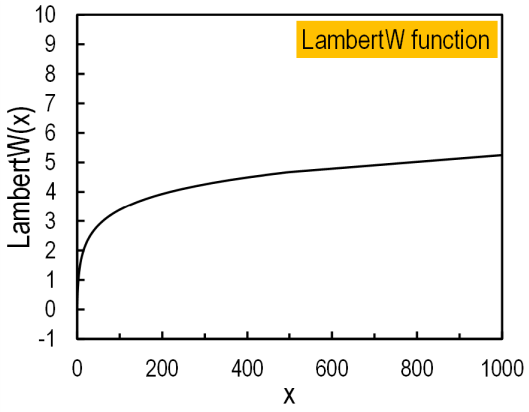


Figure 5.6: Lambert W or omega function along the real axes

The threshold voltage is defined as the lowest gate bias for which the potential across the channel is equal or higher to/than the pinch-off voltage V_P. Since the region near source terminal is considered to be at the lowest channel potential ($V_S = 0V$), V_S will determine the threshold voltage. Consequently, threshold voltage V_{TH} is given by

$$V_{TH} \equiv V_G|_{V_P=V_S.} \tag{5.3}$$

It should be noticed that $V_G = V_G - V_B$ and $V_S = V_S - V_B$ where $V_B = 0V$. Equation (5.3) is valid for both linear and saturation region.

In forward saturation, the inversion charge at the drain end of the channel is approximately zero ($q_d \backsimeq 0$). Therefore, from (2.49) the drain current value I_{th-sat} which corresponds to $V_P = V_S$ is given by

$$I_{TH-sat} = I_{spec}\left(q_s^2|_{V_P=V_S} + q_s|_{V_P=V_S}\right) \tag{5.4}$$

and by using (5.2) the following can be obtained

$$\begin{aligned} I_{TH-sat} &= I_{spec}\left(\left(\frac{1}{2}LambertW\left[2e^{\left(\frac{V_S-V_S}{U_T}\right)}\right]\right)^2 + \left(\frac{1}{2}LambertW\left[2e^{\left(\frac{V_S-V_S}{U_T}\right)}\right]\right)\right) \\ &= I_{spec}\left(\left(\frac{1}{2}LambertW\left[2e^{0}\right]\right)^2 + \left(\frac{1}{2}LambertW\left[2e^{0}\right]\right)\right) \\ &= I_{spec}\left(\left(\frac{1}{2}0.852\right)^2 + \left(\frac{1}{2}0.852\right)\right) \\ &= 0.608\, I_{spec}. \end{aligned} \tag{5.5}$$

Then, the threshold voltage in saturation V_{TH-sat} is determined as the value of gate voltage V_G for which the drain current is approximately $0.608\, I_{spec}$.

In linear mode, the inversion charge at the drain end of the channel cannot be considered as zero ($q_d \neq 0$). Therefore, by using (5.4), the drain current which defines linear mode threshold voltage V_{TH-lin} can be approximated by

$$I_{TH-lin} = I_{spec}\left(\underbrace{q_s^2|_{V_P=V_S} + q_s|_{V_P=V_S}}_{0.608} - q_d^2|_{V_P=V_S} - q_d|_{V_P=V_S}\right), \tag{5.6}$$

where $q_s^2|_{V_P=V_S} + q_s|_{V_P=V_S} = 0.608$. Following (5.2) the inversion charge q_d for $V_P = V_S$ can be expressed as

$$q_d|_{V_P=V_S} = \frac{1}{2}LambertW\left[2e^{\left(\frac{-V_{DS}}{U_T}\right)}\right] \overset{V_{DS}=0.02V}{=} 0.265 \tag{5.7}$$

and by combining (5.6) and (5.7) the following can be obtained

$$I_{TH-lin} = 0.273\, I_{spec}. \tag{5.8}$$

Similarly to V_{TH-sat}, the linear mode threshold voltage V_{TH-lin} (for $V_{DS} = 0.02V$) is determined as the value of gate voltage V_G for which $I_D = 0.273\, I_{spec}$. Note that the specific extraction method is applicable for any V_{DS} value and at any temperature.

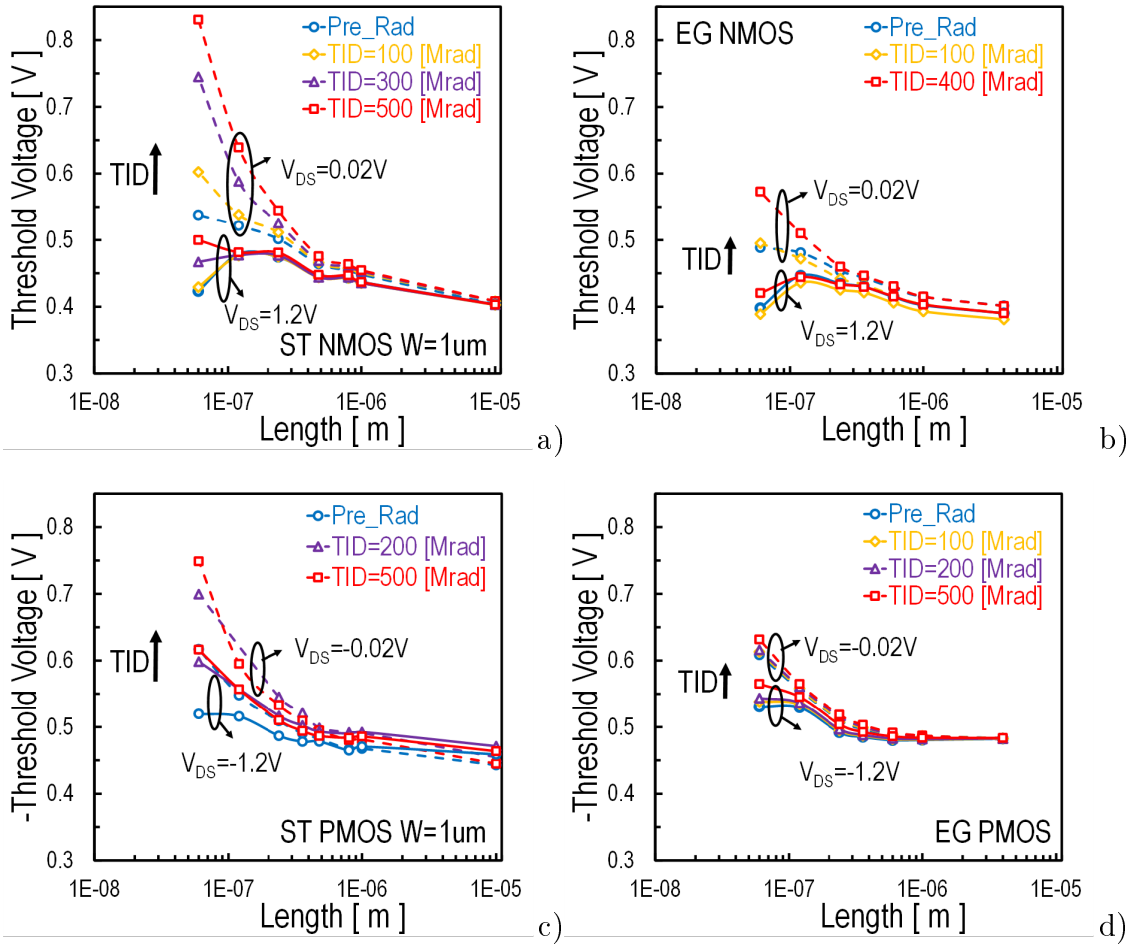


Figure 5.7: Threshold voltage vs. channel length at increasing TID levels for ST and EG n- and p-MOSFETs in linear ($|V_{DS}| = 0.02V$) and saturation ($|V_{DS}| = 1.2V$) modes. Linear mode threshold voltage exhibits a strongly increased RISCE with TID

5.2.2 DIBL

Drain induced barrier lowering (DIBL) for both n- and p-type MOSFETs can be extracted from the following equation

$$DIBL \equiv \frac{|V_{TH-lin}| - |V_{TH-sat}|}{|V_{DS-lin} - V_{DS-sat}|}, \tag{5.9}$$

where V_{TH-lin} and V_{TH-sat} are the linear and saturation threshold voltage values correspond to $|V_{DS}| = 0.02\, and\, 1.2V$ respectively.

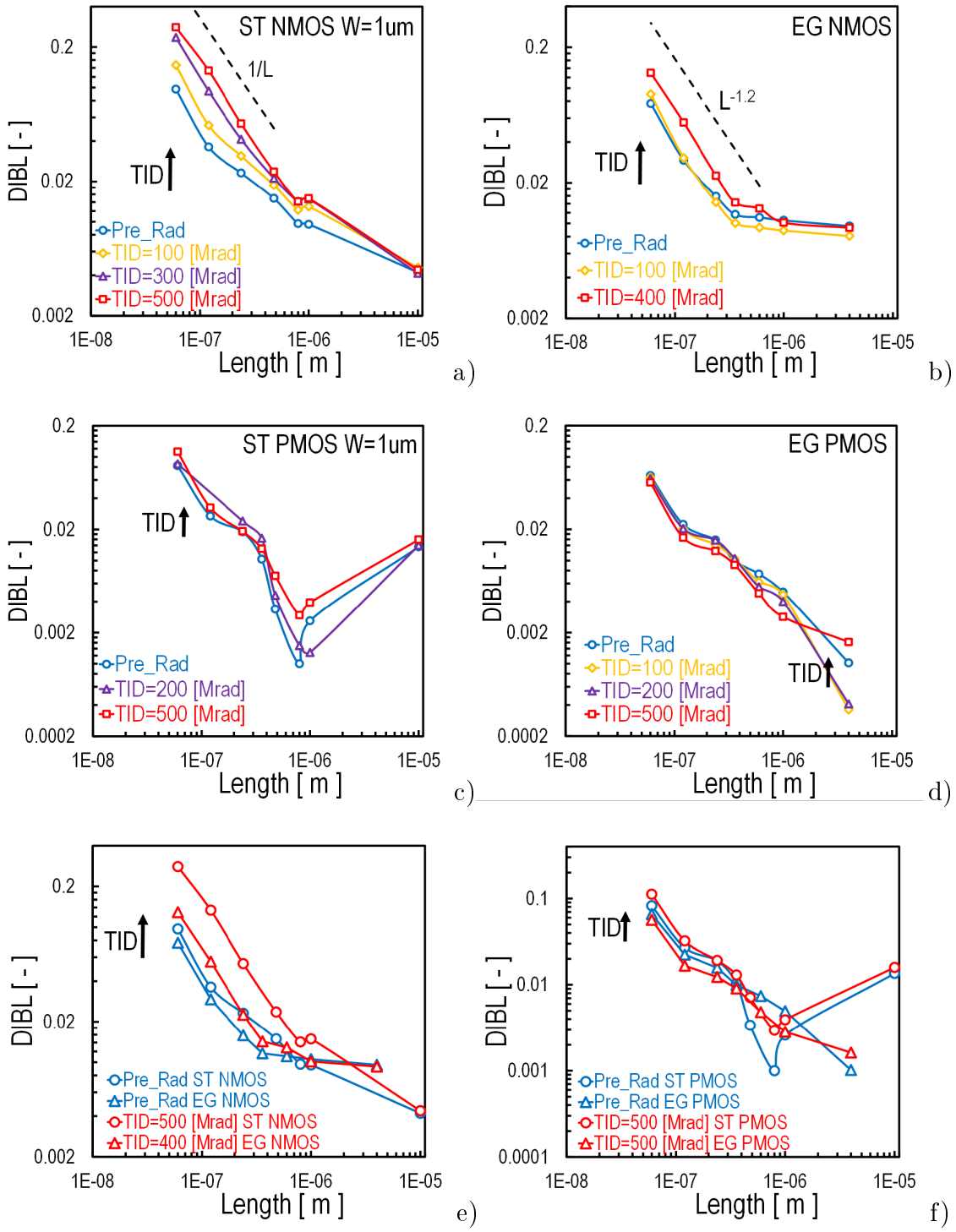


Figure 5.8: Drain Induced Barrier Lowering (DIBL) vs. channel length for varying TID for ST and EG n- and pMOSFETs. DIBL effect is most sensitive to TID in ST nMOSFETs

5.2.3 Slope factor

As described in (2.69) slope factor n is extracted in weak inversion from the maximum $g_m U_T / I_D$ vs. I_D plateau according to

$$n = \frac{1}{\left(\frac{g_m U_T}{I_{D-sat}} \mid_{max} \right)}, \tag{5.10}$$

where $I_{D-sat} = I_D$ for $|V_{DS}| = 1.2V$.

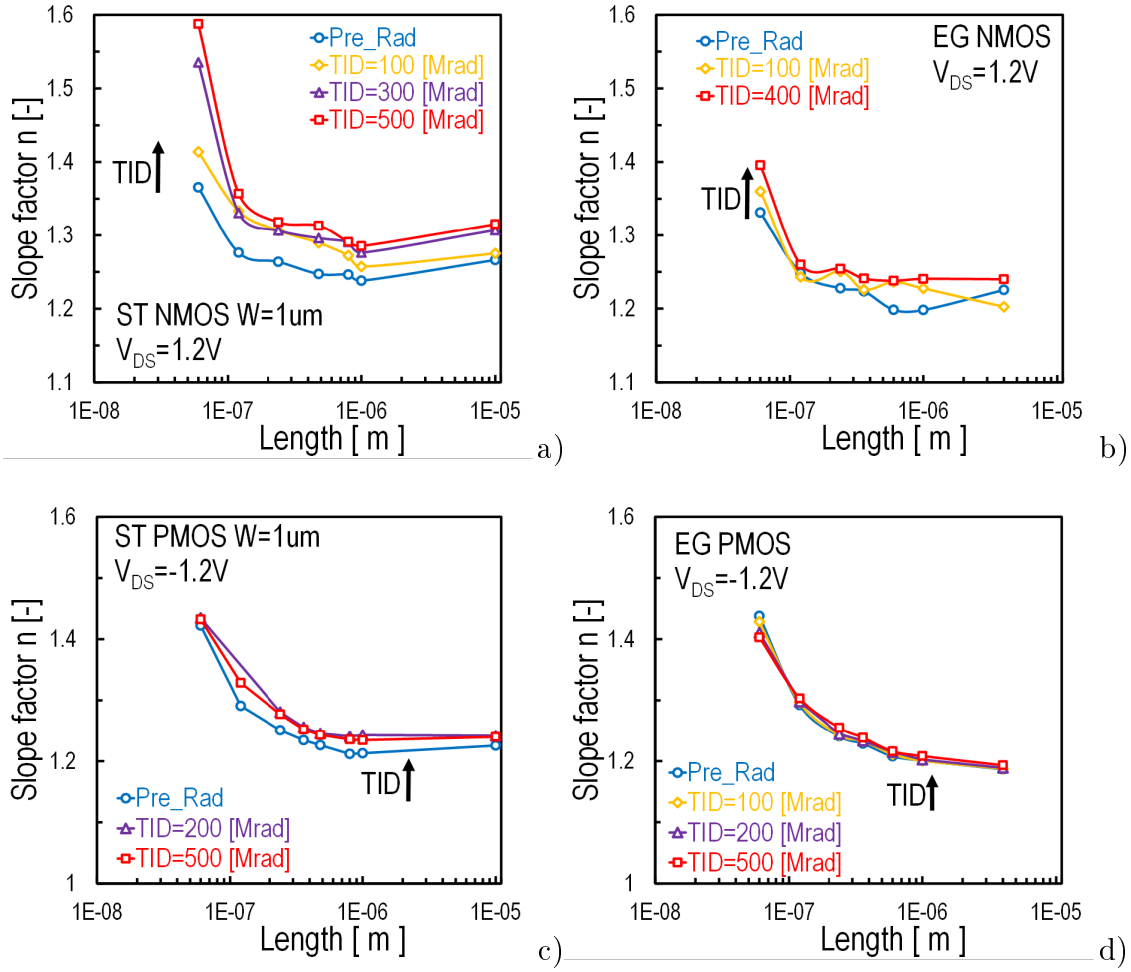


Figure 5.9: Slope factor vs. channel length at increasing TID levels for saturated ST and EG n- and pMOSFETs. Degradation of slope factor n at higher TID levels is most pronounced at ST nMOSFETs

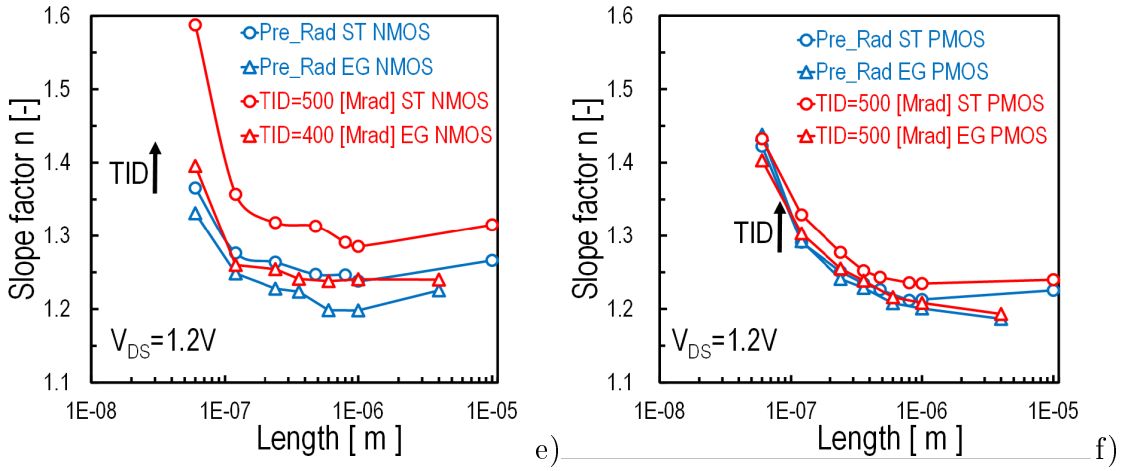


Figure 5.10: Slope factor vs. channel length for saturated ST and EG n- and pMOSFETs prior irradiation and after 500 $Mrad$ exposure. Degradation of slope factor n at higher TID levels is most pronounced at ST nMOSFETs

5.2.4 Intrinsic gain

Intrinsic gain A_V is defined as

$$A_V \triangleq \frac{g_m}{g_{ds}}, \tag{5.11}$$

where g_m and g_{ds} are the gate and drain transconductances respectively. Rearranging (2.60) g_m can be expressed in terms of IC as

$$g_m = \frac{I_D}{U_T}\frac{G(IC)}{n}, \tag{5.12}$$

where $G(IC)$is given by (2.59). Furthermore, g_{ds} in weak-moderate inversion can be expressed as a function of DIBL effect as [66]

$$g_{ds} \backsimeq n_{DIBL}\frac{I_D}{U_T}\frac{G(IC)}{n}, \tag{5.13}$$

where $n_{DIBL} = -\frac{dV_{TH}}{dV_{DS}}$. By introducing (5.12) and (5.13) into (5.11) the following can be obtained

$$A_V \backsimeq \frac{1}{n_{DIBL}}. \tag{5.14}$$

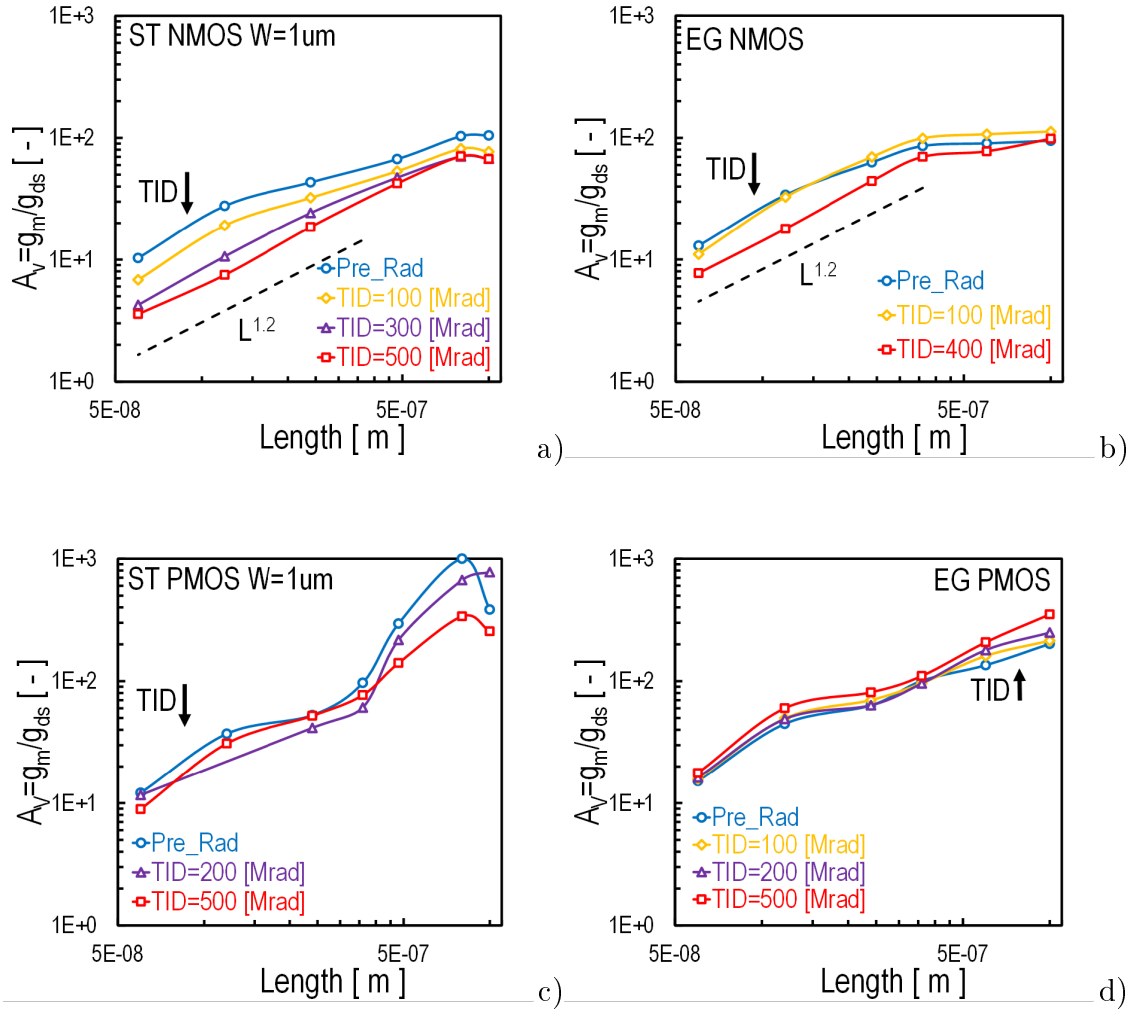


Figure 5.11: Intrinsic gain g_m/g_{ds} at $V_G \approx V_{TH}$ vs. channel length at increasing TID levels ST and EG n- and pMOSFETs

5.2.5 On-state current

On-state current is evaluated at maximum gate voltage in saturation and is defined as $|I_D| = |I_{D,ON}|$ when $|V_{DS}| = |V_{GS}| = |1.2V|$.

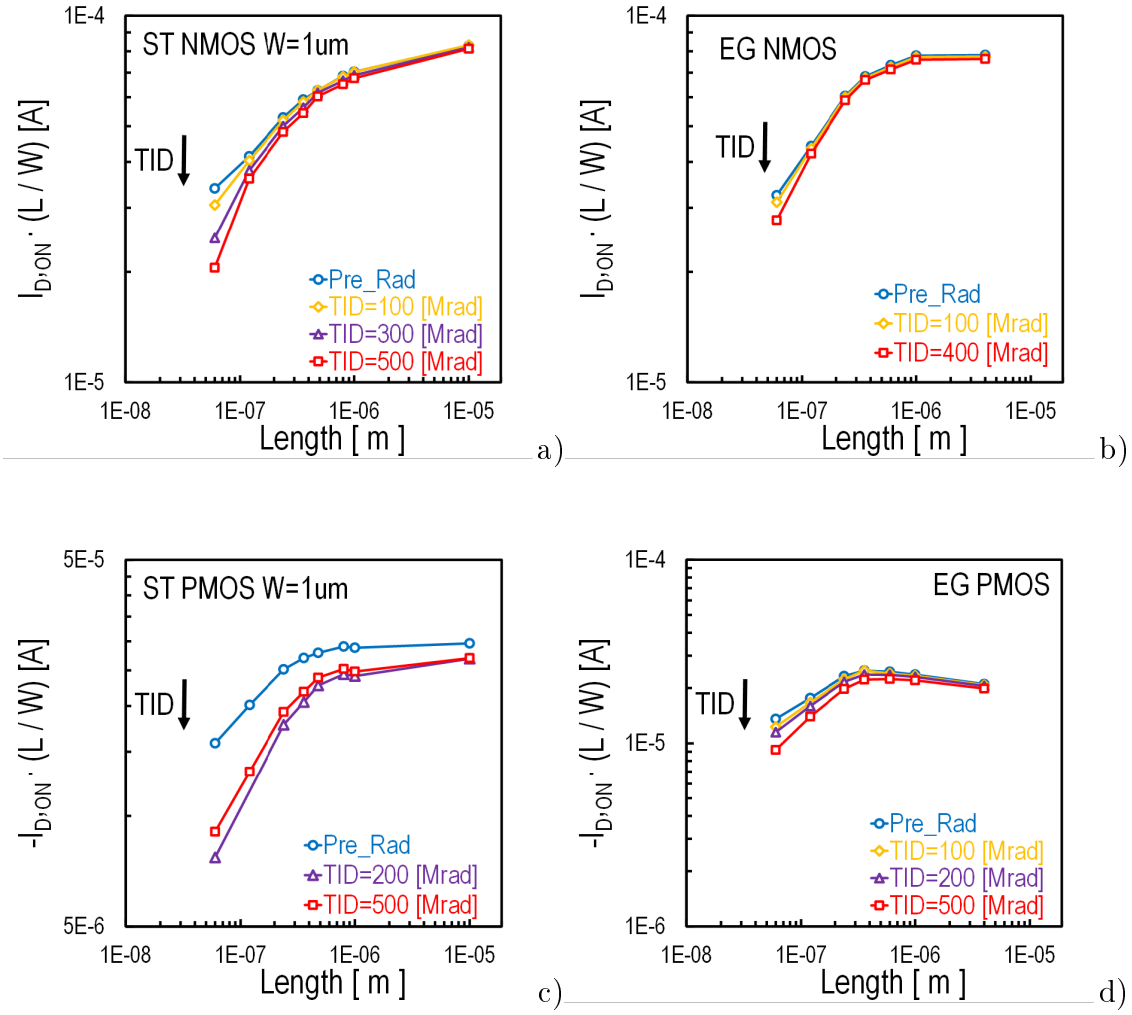


Figure 5.12: Normalized on-state current $|I_{D,ON}|\,(L/W)$ vs. channel length at increasing TID levels for n- and p-type transistors with standard and enclosed gate layout. $|I_D| = |I_{D,ON}|$ when $|V_{DS}| = |V_{GS}| = |1.2V|$

5.2.6 Off-state current

Off-state current is defined as $|I_D| = |I_{D,OFF}|$ when $|V_{DS}| = |V_{GS}| = 0V$.

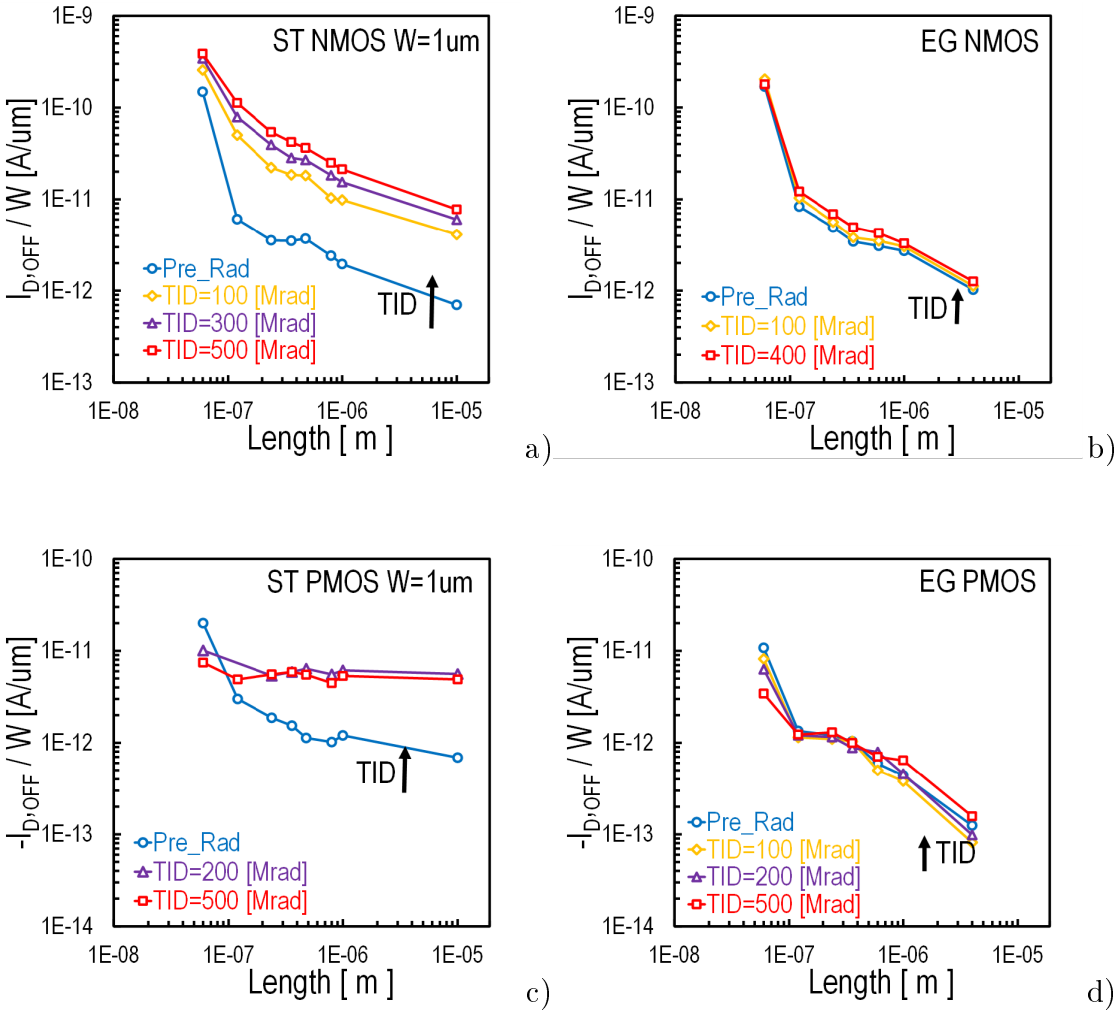


Figure 5.13: Normalized on-state current $|I_{D,OFF}|/W$ vs. channel length at increasing TID levels for n- and p-type transistors with standard and enclosed gate layout. $|I_D| = |I_{D,OFF}|$ when $|V_{DS}| = |V_{GS}| = 0V$

5.3 Velocity saturation analytical model

In the current section, the analytical model presented in Section 2.11 (Equations (2.21), (2.40), (2.41), (2.48) and (2.65)) will be used to capture the effects of increasing TID in both ST and EG n- and p-type MOSFETs. A set of parameters (I_0, V_{TO}, n, λ_c) is extracted for every device and TID exposure. The followed extraction procedure is the same as described in Section 2.11. Note that I_0 is extracted from the longest- and widest-channel device available and it is different for every TID level. In Figure 5.12, the above model is adapted to the transfer characteristics of saturated short-channel ST and EG MOSFETs of both type (n- and p-type MOSFETs).

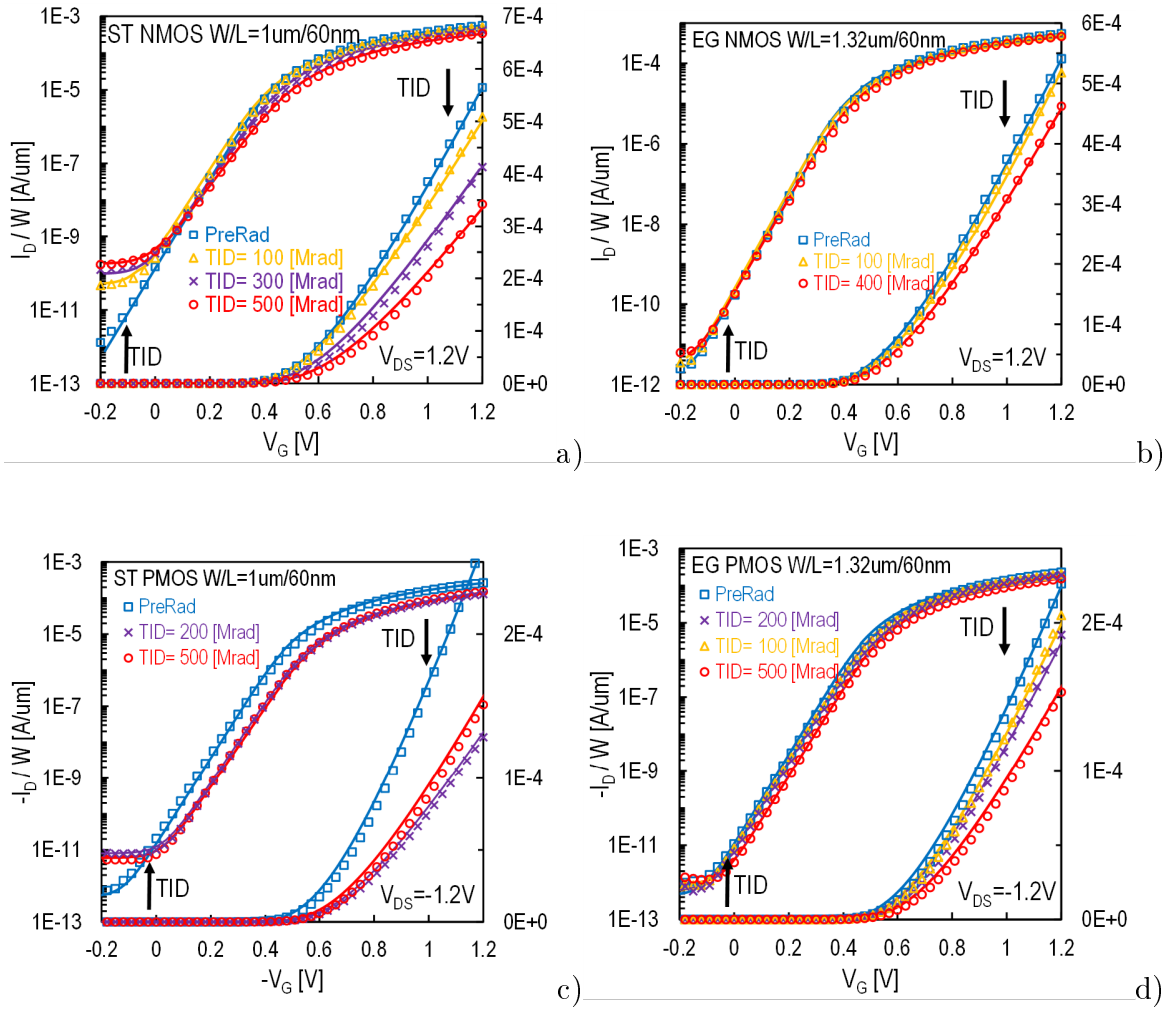


Figure 5.14: Transfer characteristics for different TID levels, for short-channel ST and EG MOSFETs in saturation. Markers: measurements, lines: model.

Figures 5.14 and 5.16 show the normalized drain current I_D/W versus gate voltage V_G for ST and EG n- and p-type MOSFETs, prior irradiation and for maximum

TID exposure. In all cases it the model (lines) is adapted to the experimental results (markers) for all the available channel lengths. Figures 5.15 and 5.17 show the adaption of the model to the transconductance-to-current ratio $g_m U_T/I_D$ vs. normalized drain current I_D/W characteristics for the same TID conditions and geometries.

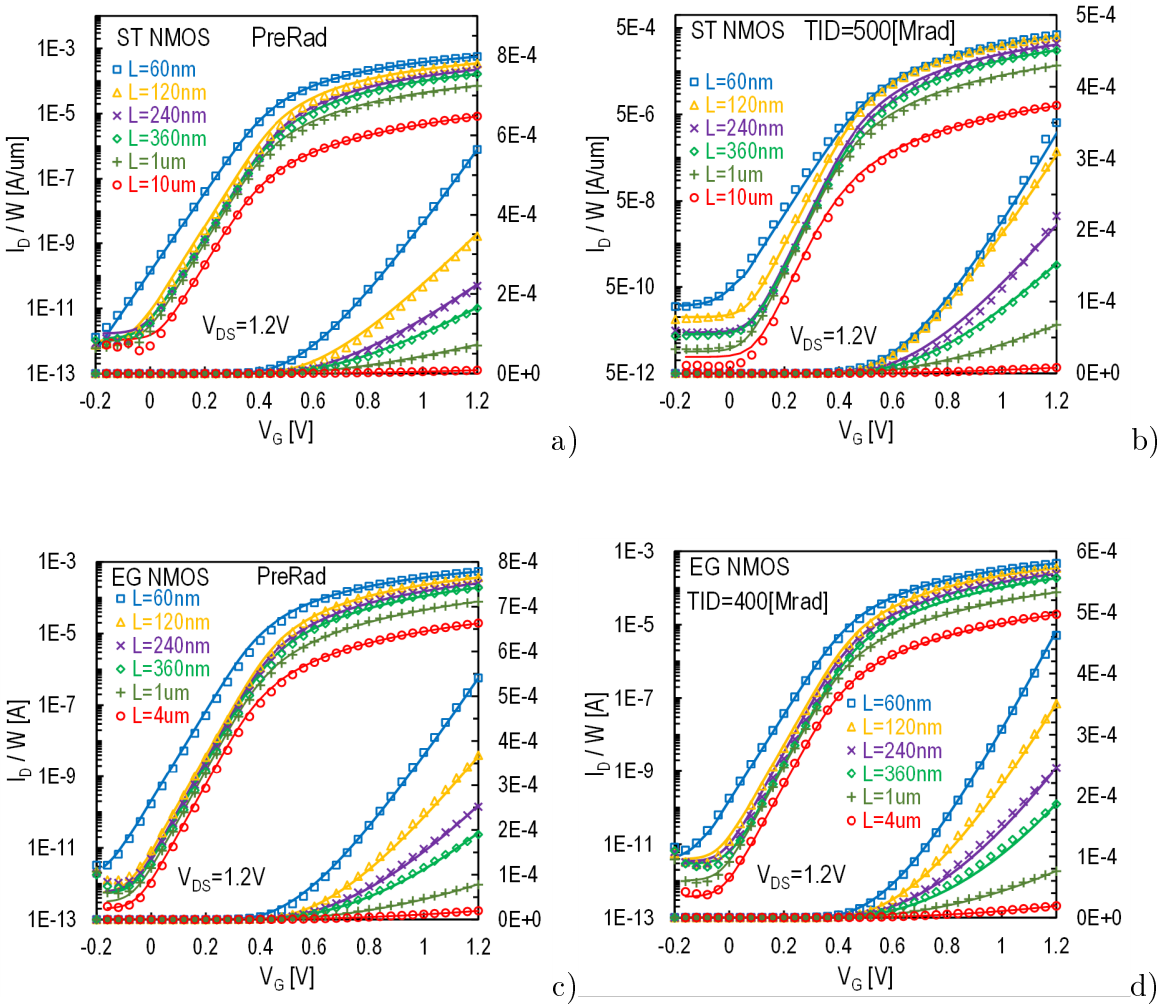


Figure 5.15: Normalized drain current I_D/W versus gate voltage V_G for ST and EG n-type MOSFETs, prior irradiation (a, c) and for maximum TID exposure (b, d), for different channel lengths. In all cases transistors are operating in saturation ($V_{DS} = 1.2V$). Markers: measurements, solid lines: model

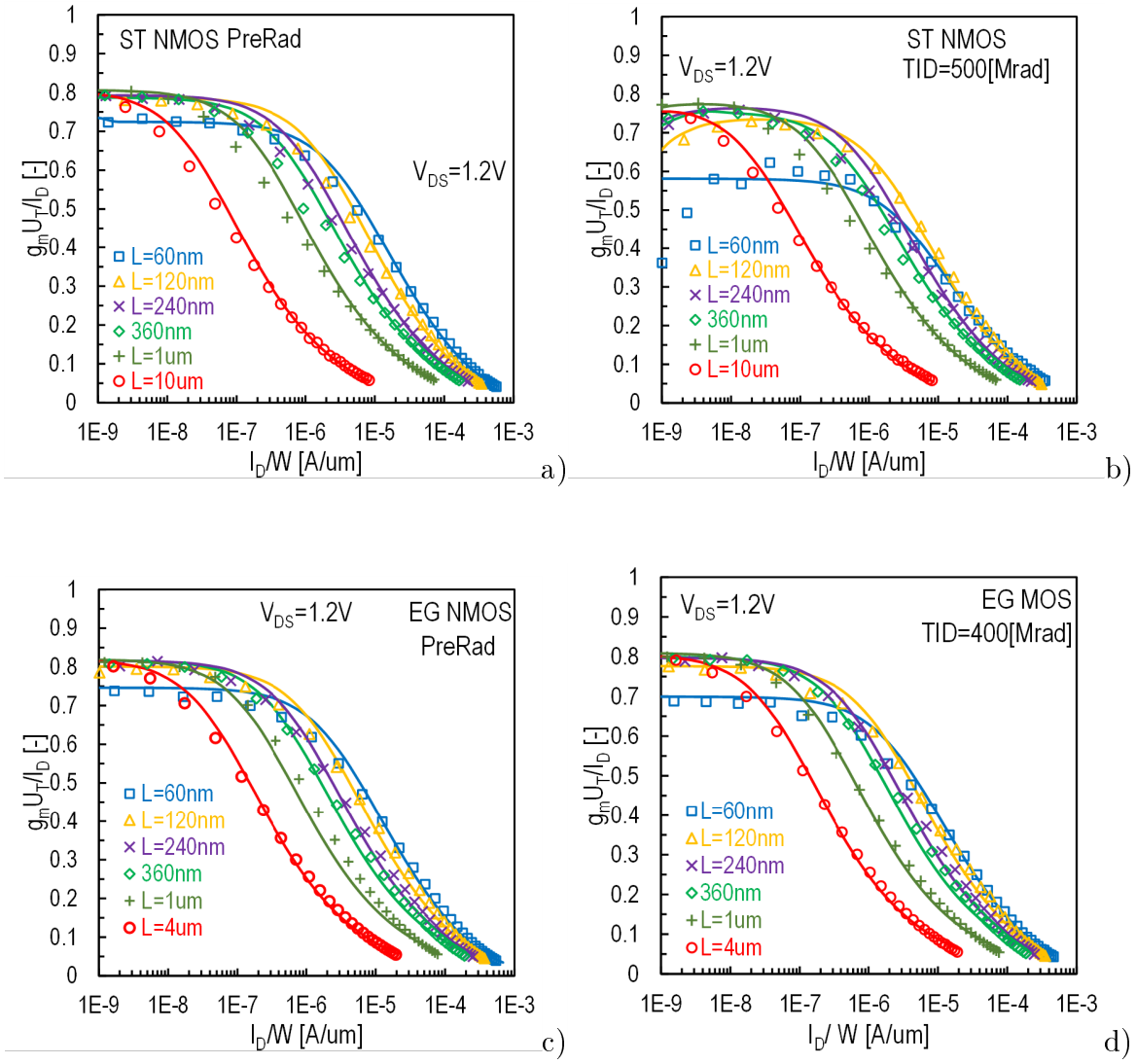


Figure 5.16: Transconductance-to-current ratio $g_m U_T/I_D$ vs. normalized drain current I_D/W for ST and EG p-type MOSFETs prior irradiation (a, c) and for maximum TID exposure (b, d), for different channel lengths. In all cases transistors are operating in saturation ($V_{DS} = 1.2V$). Markers: measurements, solid lines: model

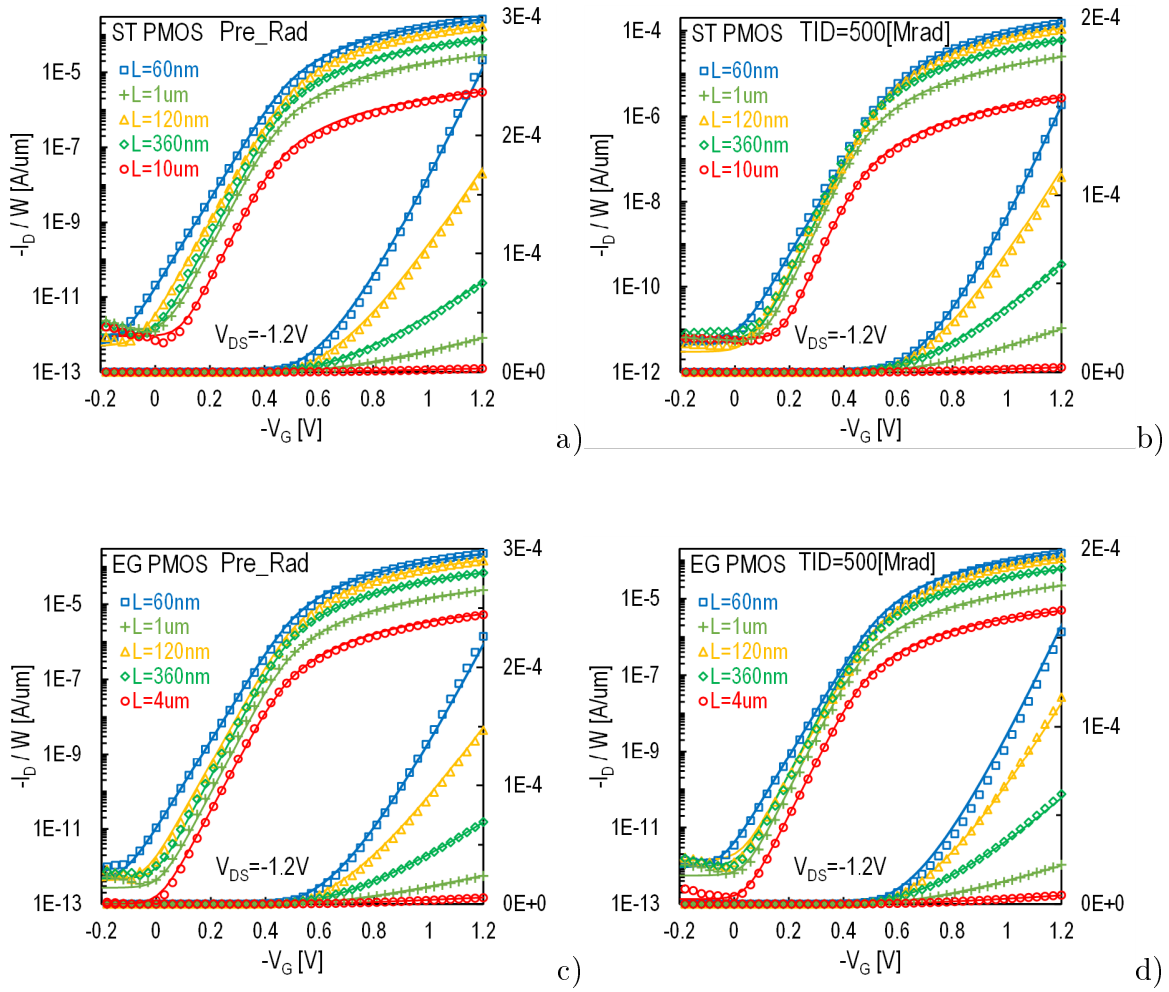


Figure 5.17: Normalized drain current I_D/W versus gate voltage V_G for ST and EG p-type MOSFETs prior irradiation (a, c) and for maximum TID exposure (b, d), for different channel lengths. In all cases transistors are operating in saturation ($V_{DS} = -1.2V$). Markers: measurements, solid lines: model

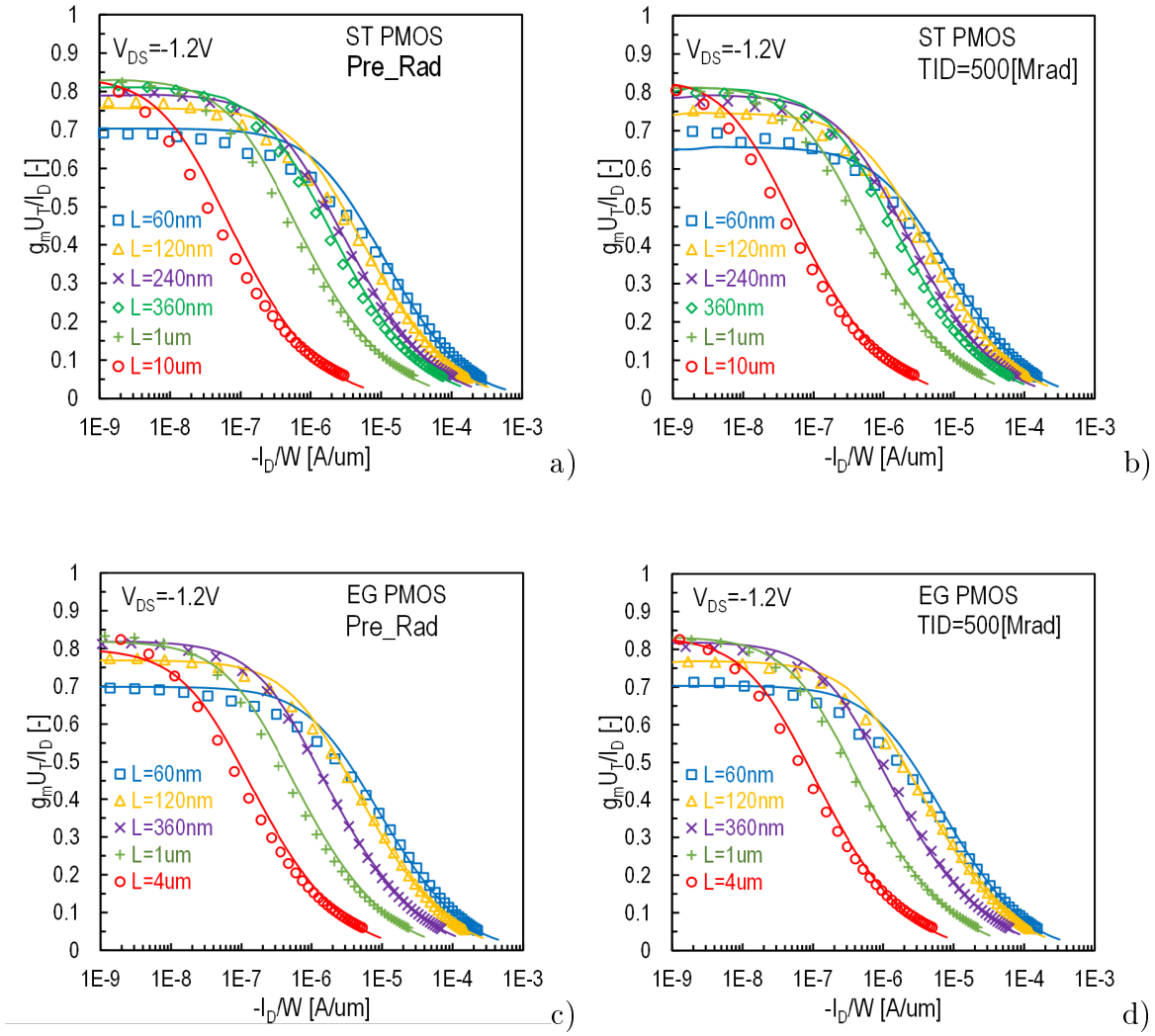


Figure 5.18: Transconductance-to-current ratio $g_m U_T/I_D$ vs. normalized drain current I_D/W for ST and EG p-type MOSFETs prior irradiation (a, c) and for maximum TID exposure (b, d), for different channel lengths. In all cases transistors are operating in saturation ($V_{DS} = -1.2V$). Markers: measurements, solid lines: model

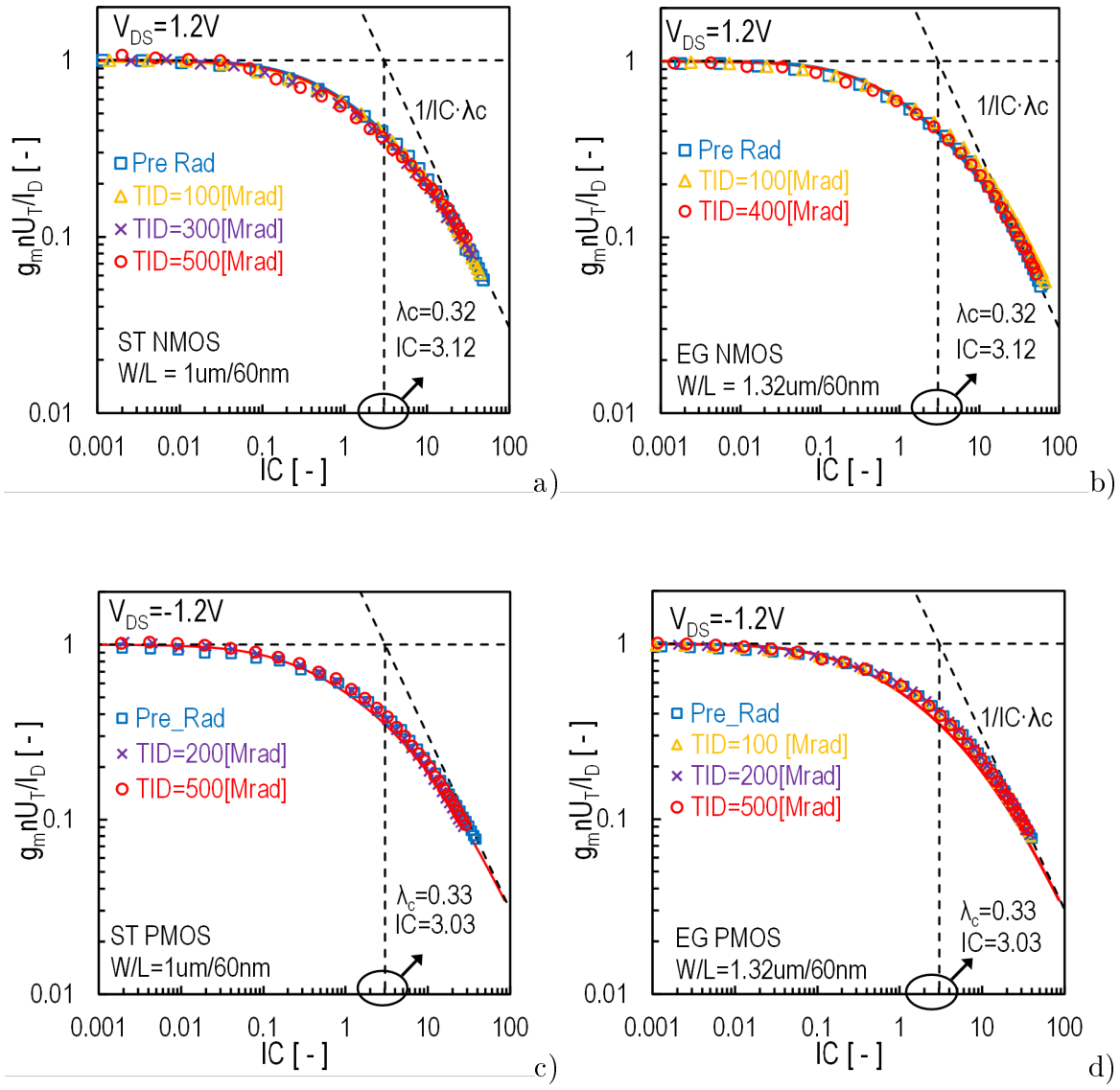


Figure 5.19: Normalized transconductance efficiency vs. inversion coefficient IC for different TID levels, for short-channel ST and EG nMOSTs in saturation ($V_{DS} = -1.2V$). Markers: measurements, solid lines: model. Asymptotes (dashed) and extracted parameter λ_c are shown.

5.4 Proposed model for λ_c parameter

In this section a new model describing λ_c parameter dependence on channel length is presented. The current model is differentiated from typical $\lambda_c = L_{sat}/L$ approach and it is valid for both n- and p-type MOSFETs. Additionally, it will be evaluated from prior irradiation state to maximum TID exposure in all cases.

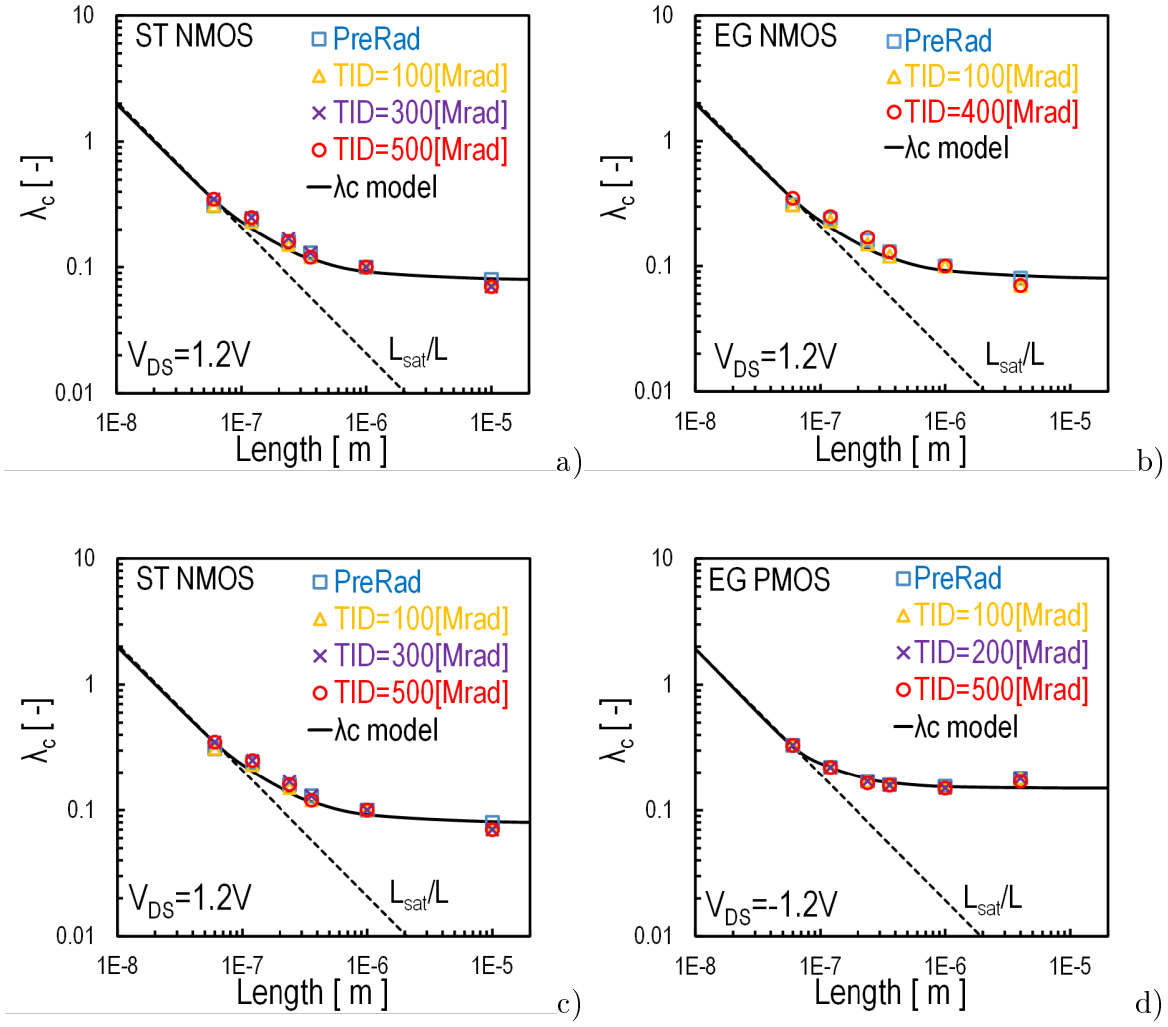


Figure 5.20: Parameter λ_c vs. channel length at various TID for ST and EG n- and pMOSFETs. Markers: λ_c values extracted from measurements, solid line: proposed model (5.15), dashed line: L_{sat}/L

The proposed model is given by

$$\lambda_c(L) = \lambda_0 + \left[\frac{L_b}{L}\right]^a, \tag{5.15}$$

where λ_0, $L_b \, and \, a$ are fitting parameters.

Figure 5.19 shows parameter λ_c versus channel length at various TID for ST and EG n- and pMOSFETs. Interestingly, velocity saturation effect is basically unaffected by TID in both n- and pMOSFETs. Additionally, λ_c parameter present the same length-dependence in both ST and EG transistors. The L_{sat}/L dependence of λ_c can be observed towards shorter channel lengths. Values of λ_0, $L_b \, and \, a$ parameters are listed in Table 3. The same model parameters apply for both ST and EG MOSFETs of both types (n and p).

Parameter	Units	ST & EG nMOS	ST & EG pMOS
λ_0	-	0.08	0.15
L_b	m	$18n$	$13n$
a	-	1.1	1.55
L_{sat}	m	$19.9n$	$19.2n$

Table 5: List of λ_c model parameters

5.5 Compact modeling with BSIM4

Compact MOSFET models such as BSIM and EKV do not specifically account for TID effects. Incorporation of radiation induced effects in such models is currently under investigation [22]. Two approaches may be envisaged: (i) incorporating the physical effects of radiation, such as near-interface charge trapping in the oxide, by modifying the equations of the compact models ; (ii) adjusting only parameter sets of compact models, without further modifications to the compact model equations. In the present section, the second of the above approaches will be followed. Scalable BSIM4 models, extracted for different doses of radiation on a $65nm$ bulk CMOS technology will be demonstrated. The procedure followed to establish a PDK where the designer could choose appropriate models according to particular TID level will be outlined.

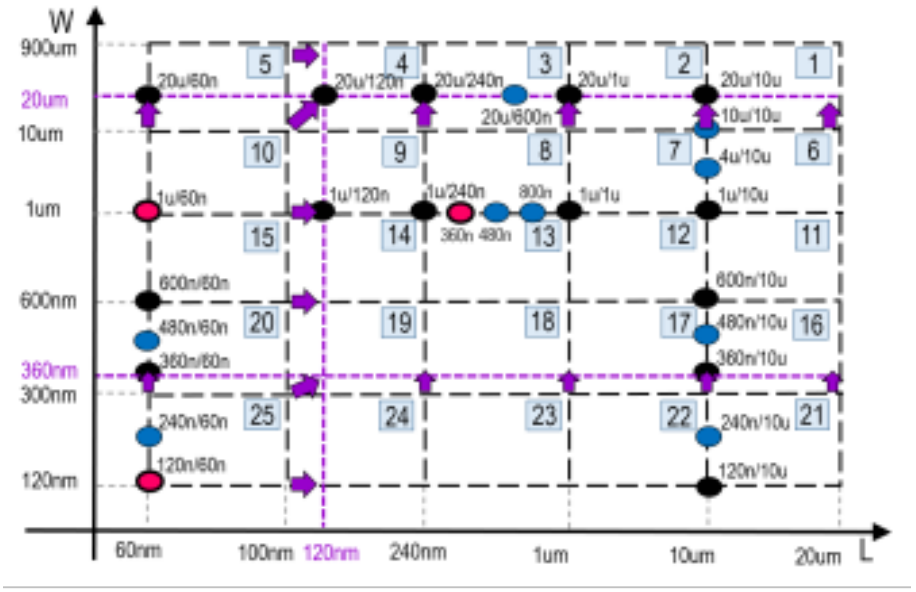


Figure 5.21: Matrix of fabricated devices vs. geometry (width, length) of the test chip for TID experiment. Each fabricated device is shown with an oval marker. The foundry process design kit provides BSIM4 models covering the 25 geometrical bins #1 – #25. Some bin boundaries are slightly modified (initial: dashed, adapted: short dashed) according to fabricated device geometries.

The models provided in the foundry PDK are based on geometrical binning, using 25 bin regions as shown in Fig. 1. Since the foundry-provided PDK is the basis, the choice was to maintain as much of its initial functionalities as possible, such as setups for "worst case" and statistical effects. BSIM4 model parameters can be extracted by using either a global – fully scalable – or binning methodologies, or even a mixture of both [68]. The binning approach distributes devices into different bins according to device geometry and provides different model parameter sets for one scalable model. Binned parameters in each bin follow the equation,

$$P_{eff} = P + \frac{lP}{L_{eff}} + \frac{wP}{W_{eff}} + \frac{pP}{W_{eff}L_{eff}} \tag{5.16}$$

Devices at the four corners of each of the bins are used to determine parameters for one bin, allowing to preserve continuity of the model at a given bin boundary. P_{eff} is the effective parameter value at a given W and L inside a bin and P is the basic model parameter. lP, wP and $pP$are length-, width- and area-dependent parameters, respectively. Effective gate length (L_{eff}) and width (W_{eff}) are used. For a given bin and binned parameter set, binning parameters lP, wP and pP are initialized to zero. Then, for every corner device, and using only basic model parameters, a different BSIM4 model is formed by following the model extraction methodology as described in [69]. Finally, by using four different sets of parameters and (5.16), basic parameters and binning parameters are determined anew. In Table 6, an indicative list of the BSIM4 parameters that are binned are shown. Other parameters are treated as global parameters, which are geometry independent and have the same value for all bins. Ideally, a test chip for binned modeling would comprise devices at the four edges of each bin. Binning boundaries had to be slightly adjusted as indicated in Fig. 1. For bins 1 to 5 and 16 to 25, minimum width was changed from $10um$ to $20um$ and from $300nm$ to $360nm$, respectively. Maximum length for bins 5, 10, 15, 20 and 25 was changed from $100nm$ to $120nm$. Adjacent bin boundaries were affected accordingly. Note that for a number of bin corners, experimental devices are missing. For these, a scalable model approach – based here on EKV3 model [70] – was used as a basis for producing approximate BSIM4 binned models.

NAME	DESCRIPTION	UNITS
$VTHO$	Long-channel threshold voltage	V
$VOFF$	Offset voltage in subthreshold region	V
$NFACTOR$	Subthreshold swing factor	-
$K2$	Second-order body bias coefficient	-
$U0$	Low-field mobility	$m^2/(Vs)$
UA	First-order mobility degradation coefficient	m/V
UB	Second-order mobility degradation coefficient	m^2/V^2
$VSAT$	Velocity saturation	m/s
$A0$	Channel length dependence of bulk charge effect	-
AGS	V_{GS} dependence of bulk charge effect	V^{-1}
$PCLM$	Channel length modulation parameter	-
$ETA0$	DIBL coefficient	-
$KETA$	Body-bias coefficient of bulk charge effect	V^{-1}
$PDIBLC2$	DIBL effect on Rout	-

Table 6: List of Binned BSIM4 Model Parameters

Following the outlined procedure, compact models for TID at different TID levels have been established. Device characteristics of devices with selected geometries exposed to radiation levels up to 500 $Mrad(SiO2)$ will be illustrated.

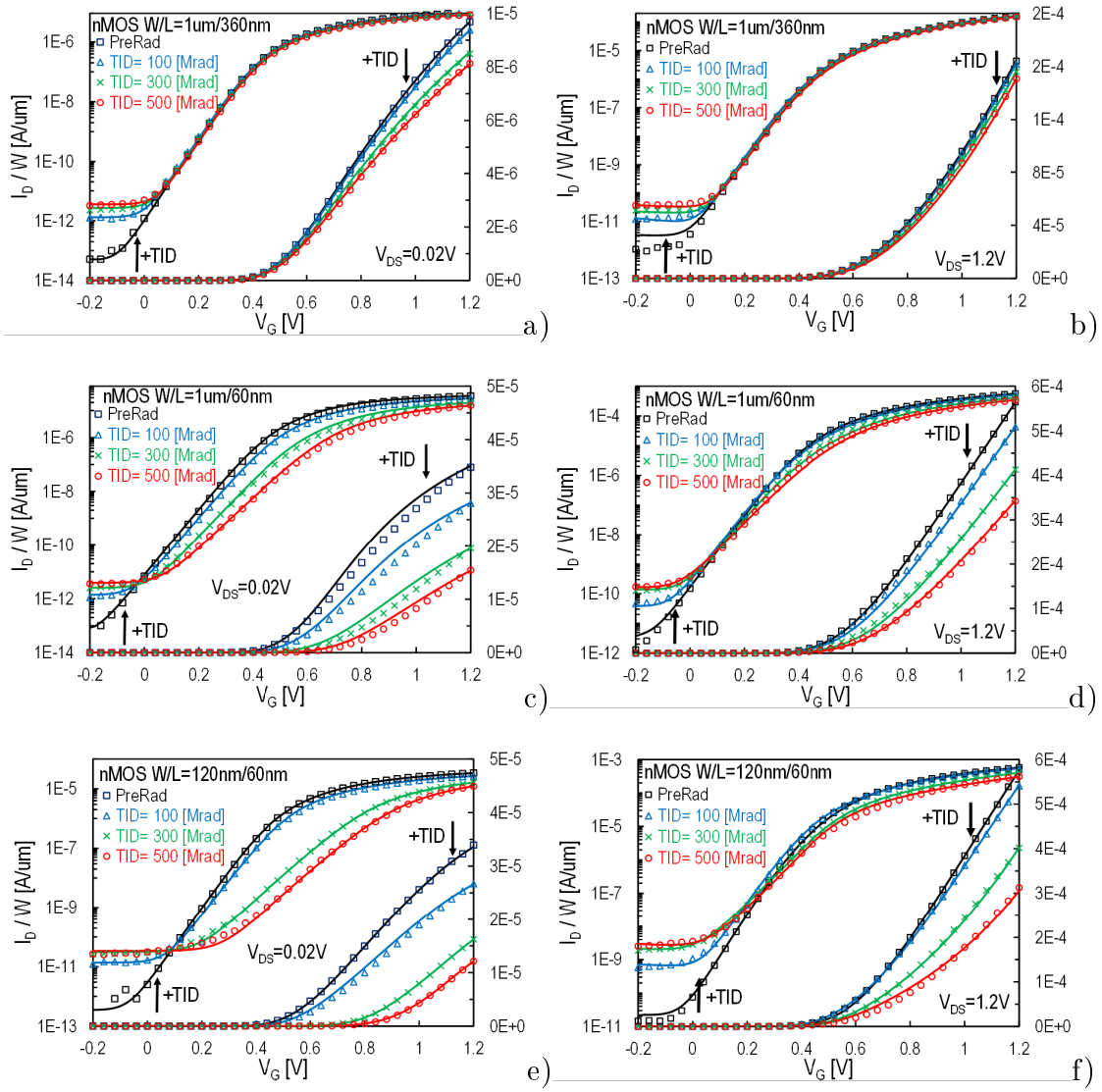


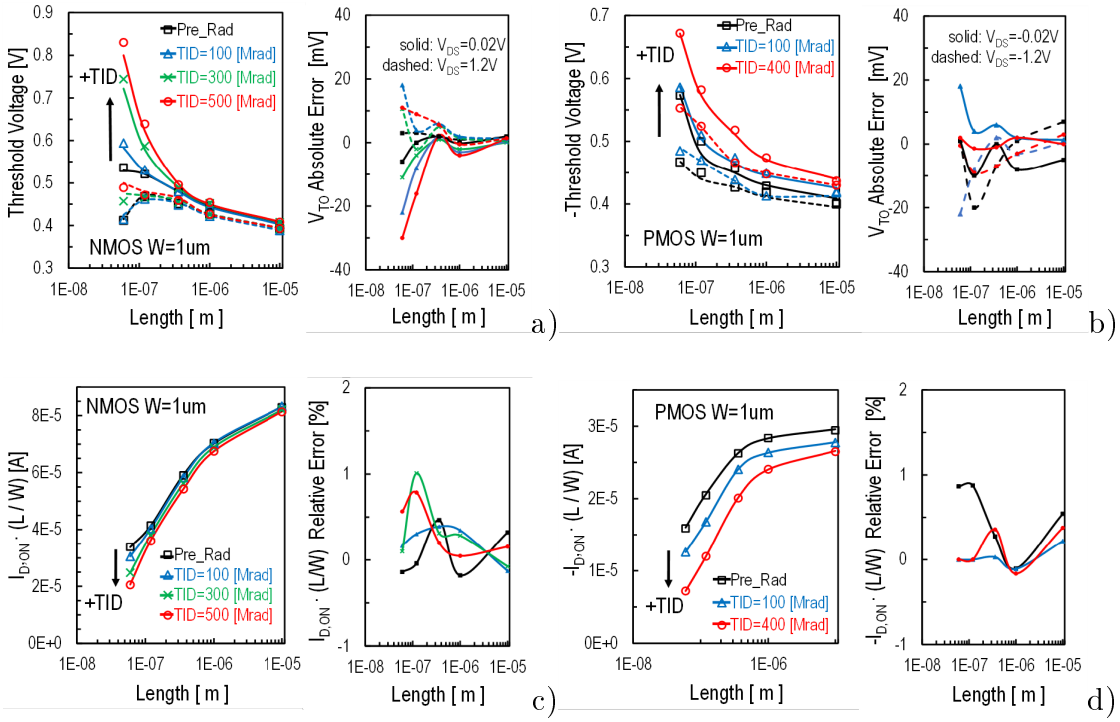
Figure 5.22: Transfer characteristics of nMOSTs in linear (a), (c), (e) ($V_{DS} = 20mV$) and saturation (b), (d), (f) ($V_{DS} = 1.2V$) modes for pre-rad and TID of 100, 300 and 500 $Mrad(SiO_2)$, at 25^oC. Threshold voltage is dramatically increased at higher TID levels and particularly in short- and short-narrow channel devices in linear mode. Mobility is reduced at higher TID. Drain leakage current increment and subthreshold slope degradation are observed. Markers: measured data, lines: BSIM4 model

Emphasis will be on moderate-short and narrow-channel MOSTs where the impact of radiation exposure is expected to be highest. The selected geometries correspond to red markers in Figure 5.20. Furthermore, scaling plots over channel length will be also

shown. In Figure 5.21(a, c, e) the impact of increased TID on transfer characteristics of nMOSTs in linear mode ($V_{DS} = 20mV$) is shown. Drain current normalized to channel width, is shown on both logarithmic and linear axes. A device with moderate channel width and length ($W/L = 1um/360nm$) mainly shows degraded mobility in strong inversion and increased leakage current. At the same width, a short-channel device ($W/L = 1um/60nm$) shows an important increase of threshold voltage with increasing TID, while weak inversion slope is significantly worsened. Mobility degradation is further enhanced. Finally, for a minimum-sized transistor ($W/L = 120nm/60nm$), the same phenomena are further exacerbated.

In Figure 5.21(b, d, f), transfer characteristics are presented in saturation regime ($V_{DS} = 1.2V$) for the same devices. Moderate threshold voltage shift, as well as increased mobility degradation in strong inversion can be observed at higher TID levels for smaller devices. Drain current leakage degradation with increased TID is present in all cases.

In Fig. 3, TID effects on output characteristics of the same nMOSTs are shown. Drain current suppression can reach about 50% at maximum dose. Interestingly, to first order, the output conductance in saturation even of shortest transistors is not strongly degraded with increased TID.



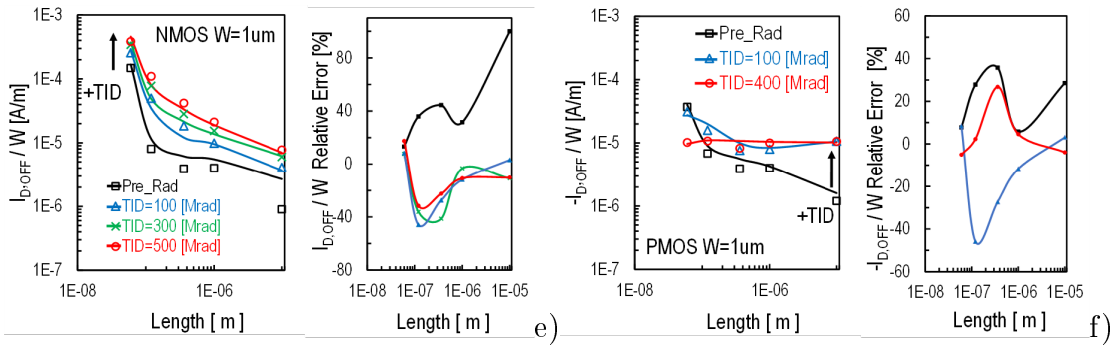


Figure 5.23: Threshold voltage in linear ($|V_{DS}| = 1.2V$) and saturation ($|V_{DS}| = 0.02V$) modes (a, b) and normalized on- (c, d) and off-state currents (e, f) vs. channel length, for n- and p-MOSTs with $W = 1um$, for pre-rad and increased TID, at 25^oC. Absolute (for V_{TO}) and relative (for $I_{D,ON}$ and $I_{D,OFF}$) errors are shown in all cases. Markers: measured data, lines: BSIM4 model. The model shows adequate coverage of TID effects for both types of channels

Figure 5.22(a) shows TID effect on threshold voltage V_T, in linear and saturation modes versus channel length, for nMOSTs with fixed $W = 1um$. V_T values were extracted using the "adjusted constant current" (ACC) method described in Section 5.2.1 [9]. Linear mode threshold voltage presents a significantly increased radiation induced short channel effect (RISCE) towards minimum channel length. In saturation, the impact of radiation versus channel length is minor causing maximum V_T shift of almost $10mV$ for the shortest channel length ($L = 60nm$).

In Figure 5.22(c, e) the result of TID effect for on-state ($V_{DS} = 1.2V$, $V_{GS} = 1.2V$) and off-state ($V_{DS} = 1.2V$, $V_{GS} = 0V$) currents of nMOSTs with respect to channel length is examined. For this purpose, currents are normalized with the aspect ratio (W/L) and width (W) respectively. On-state current $I_{on}/(W/L)$ degradation worsens at higher TID levels and shorter channel devices. Threshold voltage shift, mobility reduction and velocity saturation influence $I_{on}/(W/L)$ degradation. Scaling of off-state current I_{off}/W is dominated by subthreshold characteristics, except at shortest channel lengths, where junction leakage dominates. In Figure 5.22(b, d, f) , analogous characteristics are presented for pMOSTs. Similarly to the nMOSTs, linear mode threshold voltage in short-channel pMOSTs exhibits an increased sensitivity to TID. On-state current degradation at higher TID levels can also be observed, but is less pronounced when compared to that of the NMOS counterpart. TID impact on pMOS off-state current is maximum for moderate-longer channel transistors. In all cases, both measured data (markers) and simulation (lines) are presented.

The BSIM4.5 model represents qualitatively well the measured results for all shown quantities, in both n- and p-type MOSTs, for a wide range of device geometries. The corresponding error plots show that threshold voltage is roughly modeled within $\pm 20mV$. While this may seem somewhat imprecise, one has to keep in mind that the (binned/scalable) model is compared here to single device measurements. On the other hand, the vastly increased DIBL effect at high TID as observed in small devices is

difficult to be reproduced by the BSIM4.5 model. While on-current and its dependence on TID is well represented by the model (to within a couple percent), large errors may occur in off-state leakage, a parameter which is not generally well-controlled.

Threshold voltage shifts, subthreshold slope degradation, mobility reduction, and degradation of leakage current are significant at extreme levels of TID as observed in 65nm bulk CMOS. These effects are seen to be relatively moderate in devices of widths/lengths larger than roughly $W/L = 1um/360nm$, but increase drastically with reduced device dimensions. The present paper has shown the adaptation of a foundry-provided process design kit based on the BSIM4 model, to successfully include TID effects up to $500\,Mrad(SiO_2)$. The binning approach underlying the foundry PDK has been conserved, and appears to be a viable approach for incorporating extreme TID effects. Hence the high-energy physics design community is given the perspective of using a compact model library adjusted to various levels of TID. This should prove to be highly useful in designing new electronics for the ongoing HL-LHC update, as well as for similar work in other radiation environments. Future extensions of the TID-PDK include temperature dependence of TID exposure, covering high- and low-VT devices available in the same 65 nm bulk CMOS process, as well as establishing compact models for enclosed-gate (EG) transistors.

5.6 $1/f$ noise measurement set up

On-wafer low frequency noise measurements were performed on nMOS transistors with standard and enclosed gate layout as shown on Figure 5.1, using an experimental $180nm$ process flow. The EG layout device is a square nMOSFET with outer polysilicon-edge cut, a fixed drain size of $1.4*1.4um^2$ and no shallow trench isolation. LFN spectra of 50 dies of short-channel transistors were measured over one wafer, in linear and saturation regions with $V_{DS} = 0.05$ and $1.2V$, respectively, over all the range from weak to strong inversion. Gate voltage values are V_{GS} =0.3, 0.35, 0.4, 0.45, 0.5, 0.55, 0.6, 0.7, 0.8, 1, 1.2, 1.5 and 1.8V. The measured frequency range spans $2Hz$ to $1.7KHz$. The exact dimensions of the EG devices is $W/L = 6.29um/180nm$ whereas for standard layout MOSFETs $W/L = 10um/180nm$.

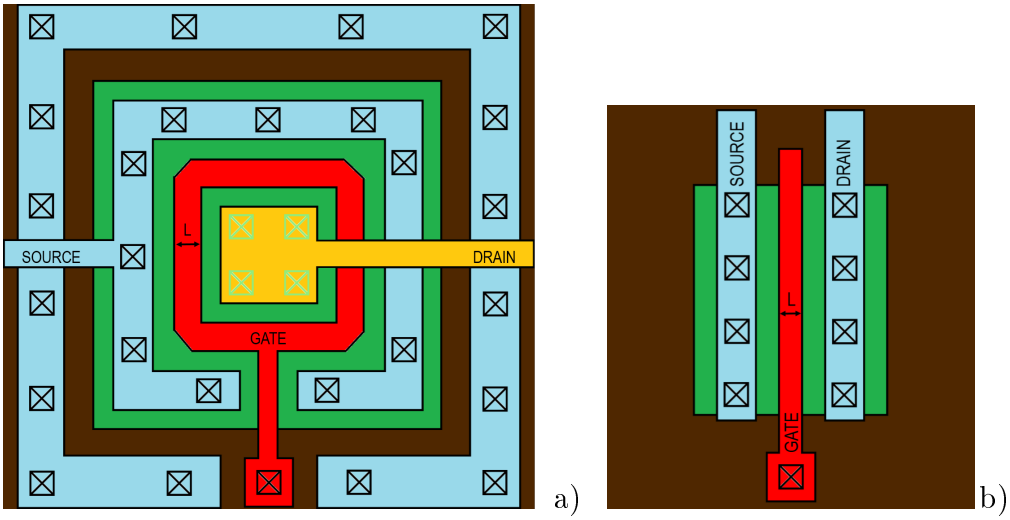


Figure 5.24: Enclosed gate (EG) nMOSFET with outer polysilicon - edge cut, p+ guard rings, without STI and fixed $1.4*1.4um^2$ drain size (a) and standard (ST) nMOSFET (b) of an experimental $180nm$ process flow

The noise measurement setup consists of the following instruments:

- Cascade Microtech 10600 summit probe station
- Standford Research SR570 Low Noise Amplifier
- Agilent 35670 Dynamic Signal Analyzer
- HP4542A DC Analyzer
- Low Pass Filter at $1Hz$
- GPIB-USB interface

- NI CV232A RS232-GPIB interface

The experimental procedure for every device started with I/V measurements in order to export the basic output and transfer characteristics. Then, through AdMOS noise measurement software interface, the drain referred PSD for every device was extracted, at a frequency range from $2Hz$ to $1.7KHz$, for all the gate and drain voltage values mentioned above. The software used to make the measurements was Agilent ICCAP.

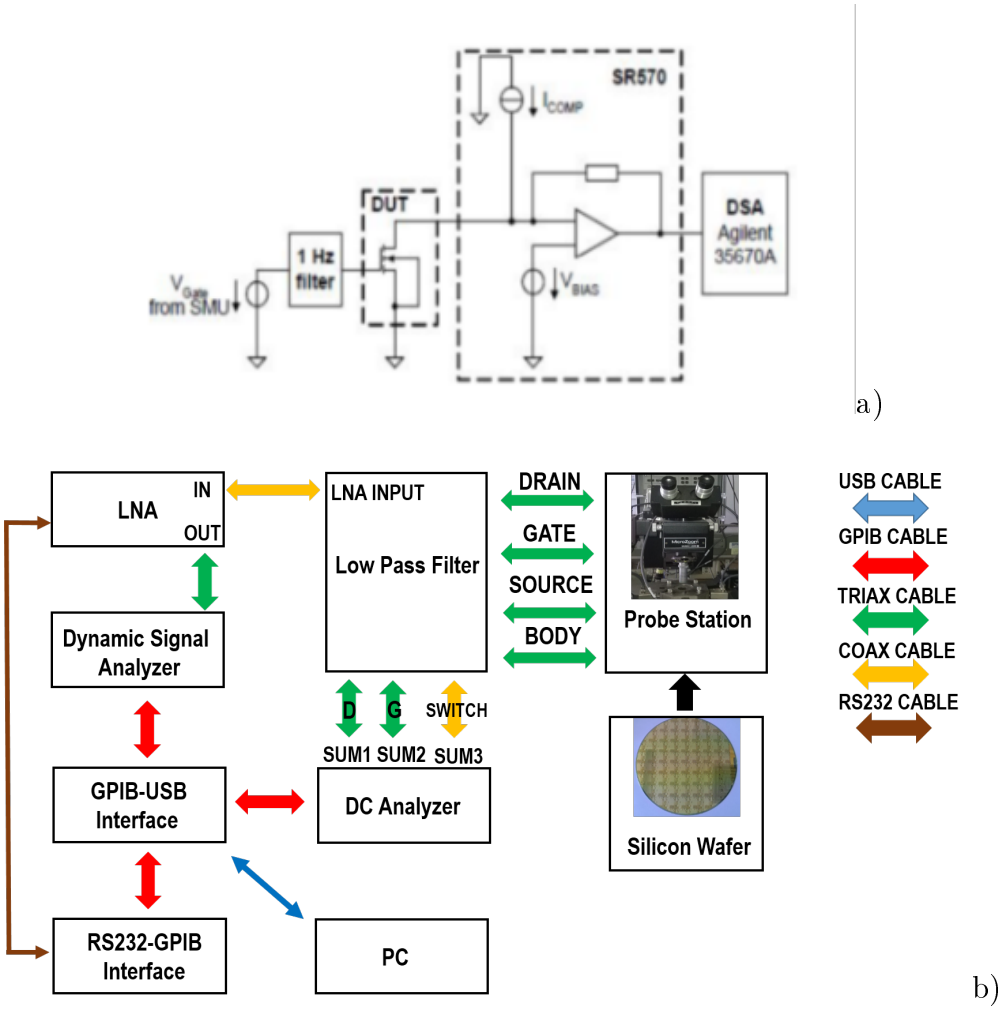


Figure 5.25: Low-Frequency noise set-up: (a) circuit diagram and (b) block diagram with cable connections

5.7 LFN data processing typical procedure

In this section, the measured data processing standard procedure will be described. For both ST and EG MOS devices, statistical analysis of low frequency noise, is typically

presented in the form of $E[WLS_{ID}f/I_D^2]$ and $E[WLS_{VG}f]$ versus I_D, $E[S_{ID}f]$ and $E[S_{VG}f]$ versus I_D and $\sigma(ln(WLS_{ID}f/I_D^2))$ versus I_D plots. Typical data processing procedure is described next. The first step is to multiply every S_{ID} measured value with the matching frequency value f. Then, the average $S_{ID}f$ value is extracted from the frequency range between 10 and 100Hz, where the clear $1/f$ behavior can be observed for almost every bias condition and device. Next, the ln-mean value of noise, $E[S_{ID}f]$, is calculated over the number of the different samples as follows:

$$E[S_{ID}f] = exp\left\{\frac{\sum S_{n=1}^{n=x} ln(S_{IDx}f)}{x}\right\} \ (A^2), \tag{5.17}$$

where x is the number of samples. The geometric standard deviation $\sigma(ln(WLS_{ID}f/I_D^2))$ is calculated from

$$\sigma(ln(WLS_{ID}f/I_D^2)) = exp\left\{\sqrt{\frac{\sum S_{n=1}^{n=x}\left(ln\left(WLS_{IDx}f/I_D^2\right) - E\left[WLS_{ID}f/I_D^2\right]\right)^2}{x-1}}\right\}. \tag{5.18}$$

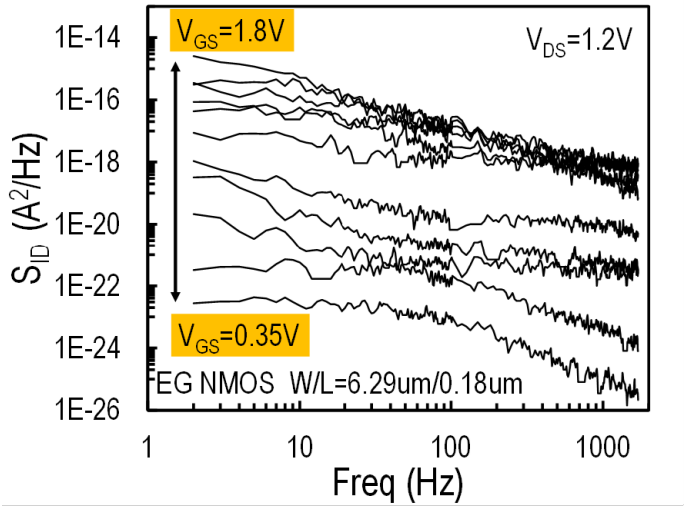


Figure 5.26: Measured S_{ID} vs. frequency for an EG nMOSFET device with $W/L = 6.29um/180nm$ in saturation ($V_{DS} = 1.2V$) for several gate voltage values (V_{GS} =0.35, 0.4, 0.45, 0.5, 0.55, 0.6, 0.7, 0.8, 1, 1.2, 1.5 and 1.8V)

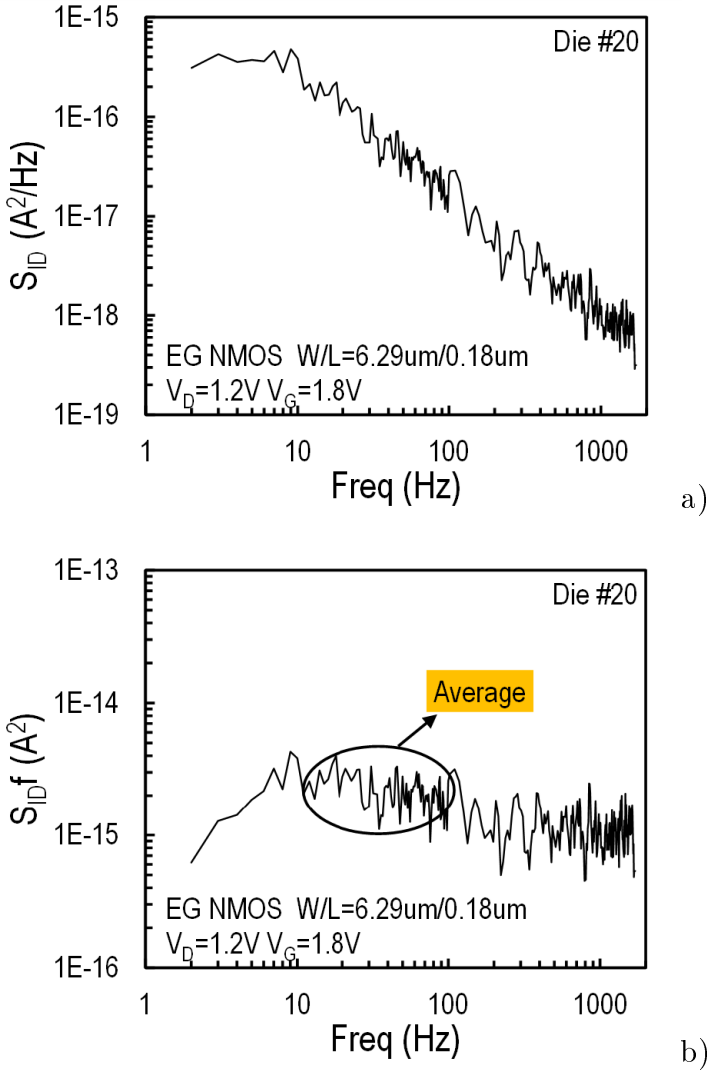


Figure 5.27: Measured S_{ID} (a) and normalized $S_{ID}f$ (b) vs. frequency for one sample device with $W/L = 6.29um/180nm$. The average $1/f$ noise at 1 Hz is extracted over the frequency range between 10 and 100Hz.

Mean value of gate input referred LFN is given by

$$E[S_{VG}] = E[S_{ID}]/E[g_m]^2 \ \ (V^2/Hz), \tag{5.19}$$

where $E[g_m]$ is the mean value of the gate transconductance for a specific gate bias voltage value. The rest of the quantities are extracted by following similar methodology.

5.8 Measured LFN spectra

In this section several LFN measured spectra are shown. Results of both standard and enclosed gate layout nMOSTs in linear ($V_{DS} = 0.05V$) and saturation ($V_{DS} = 1.2V$) modes, for $V_{GS} = 0.4$, 0.45, $0.6\,and\,1.8V$, are presented. The highlighted (red) spectra is the result of LFN measurement over the same device for different bias condition. In all cases the measured PSDs are mostly dominated by flicker noise with a slope close to $1/f$. At lower gate voltages Lorentzian-like spectral components appear. The spread of noise clearly increases towards moderate-weak inversion.

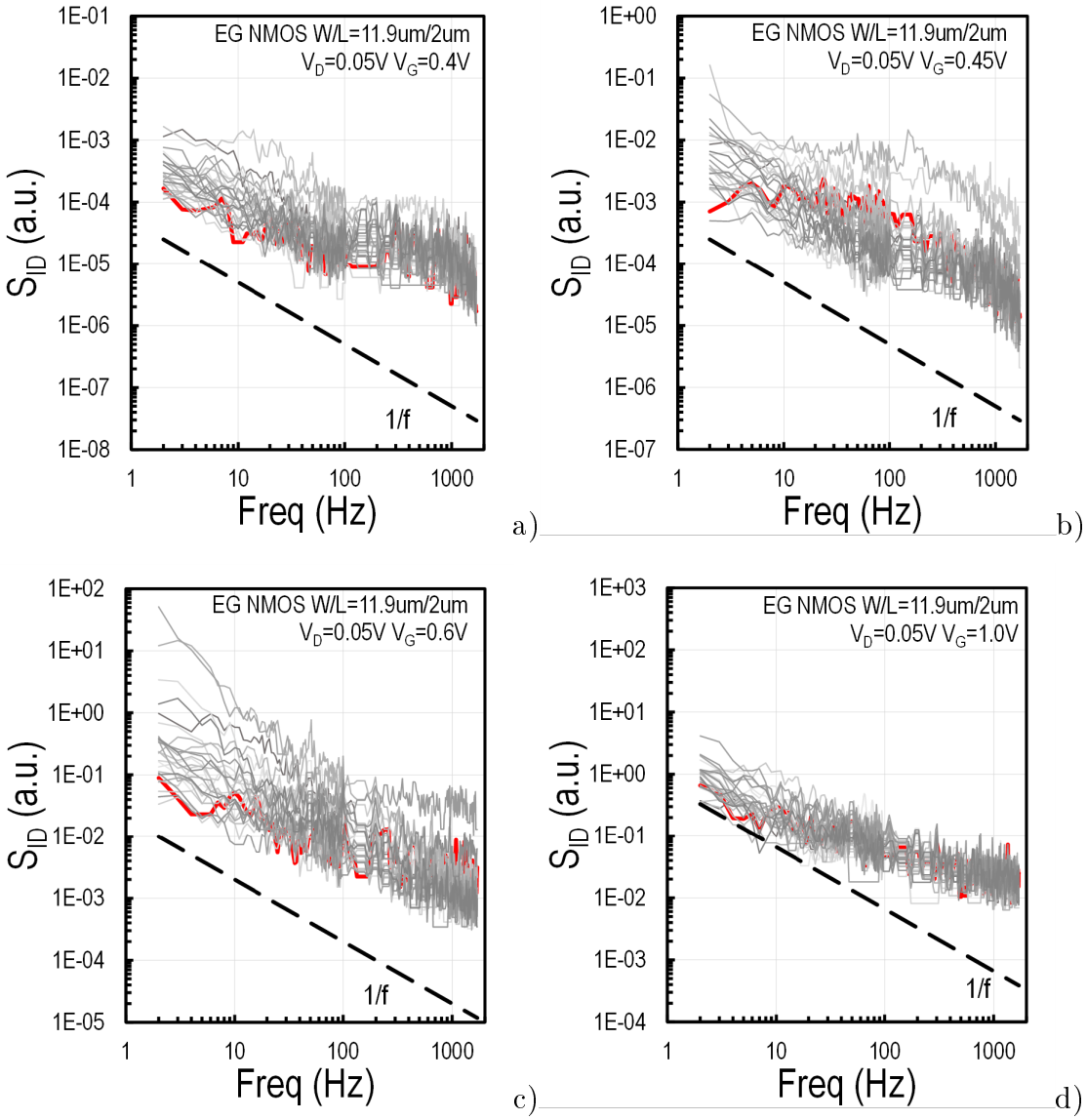


Figure 5.28: Low frequency noise spectra (S_{ID} vs. frequency) of 50 long channel ($W/L = 11.9um/2um$) enclosed gate NMOS transistors at $V_{GS} = 0.4$, 0.45, $0.6\,and\,1.0V$, with $V_{DS} = 0.05V$ (linear mode). The highlighted (red) spectra are individual characteristics of the same transistor. $1/f$ slope is depicted

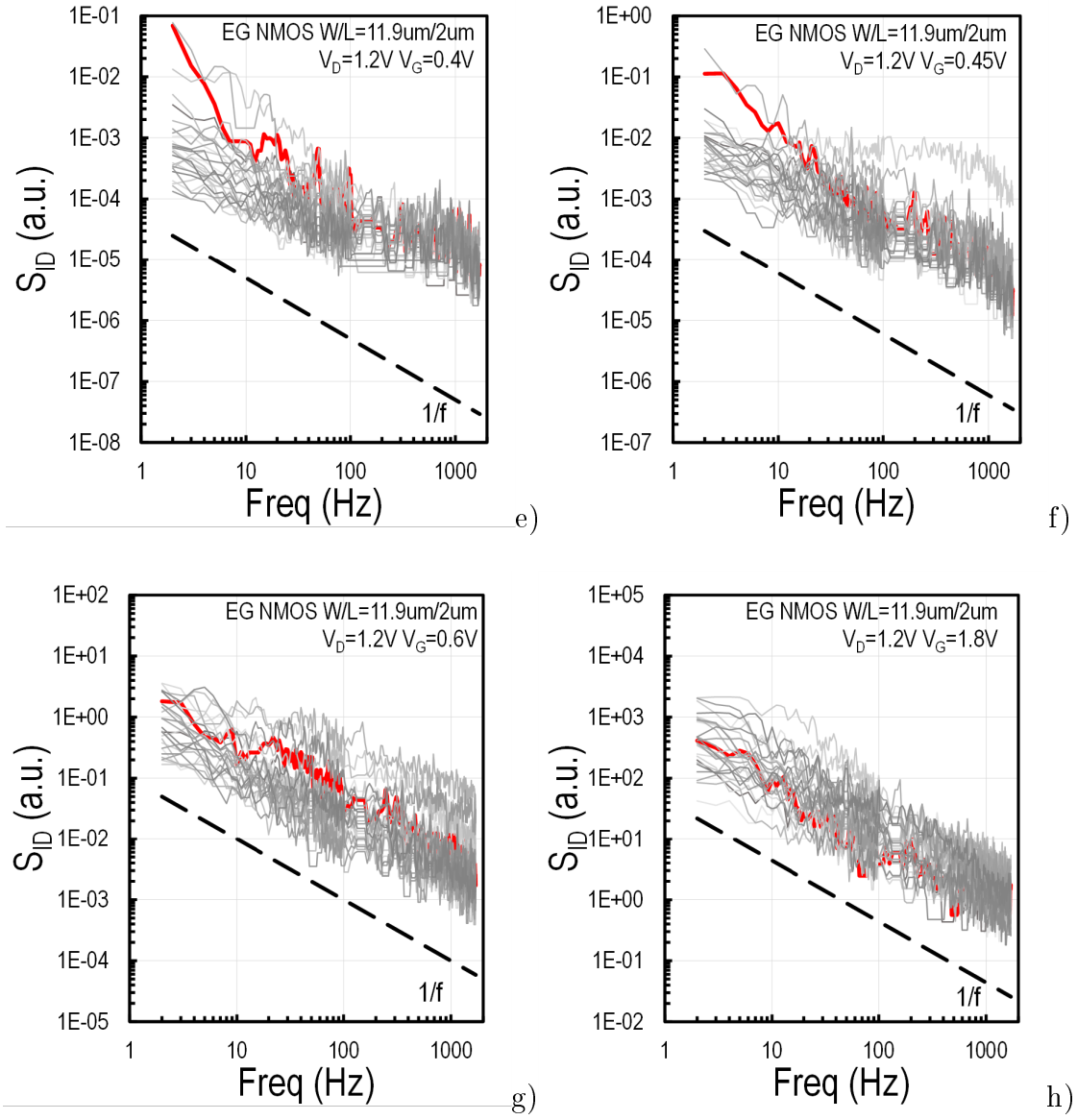


Figure 5.29: Low frequency noise spectra (S_{ID} vs. frequency) of 50 long channel ($W/L = 11.9um/2um$) enclosed gate NMOS transistors at $V_{GS} = 0.4, 0.45, 0.6\,and\,1.8V$, with $V_{DS} = 1.2V$ (saturation mode). The highlighted (red) spectra are individual characteristics of the same transistor. $1/f$ slope is depicted

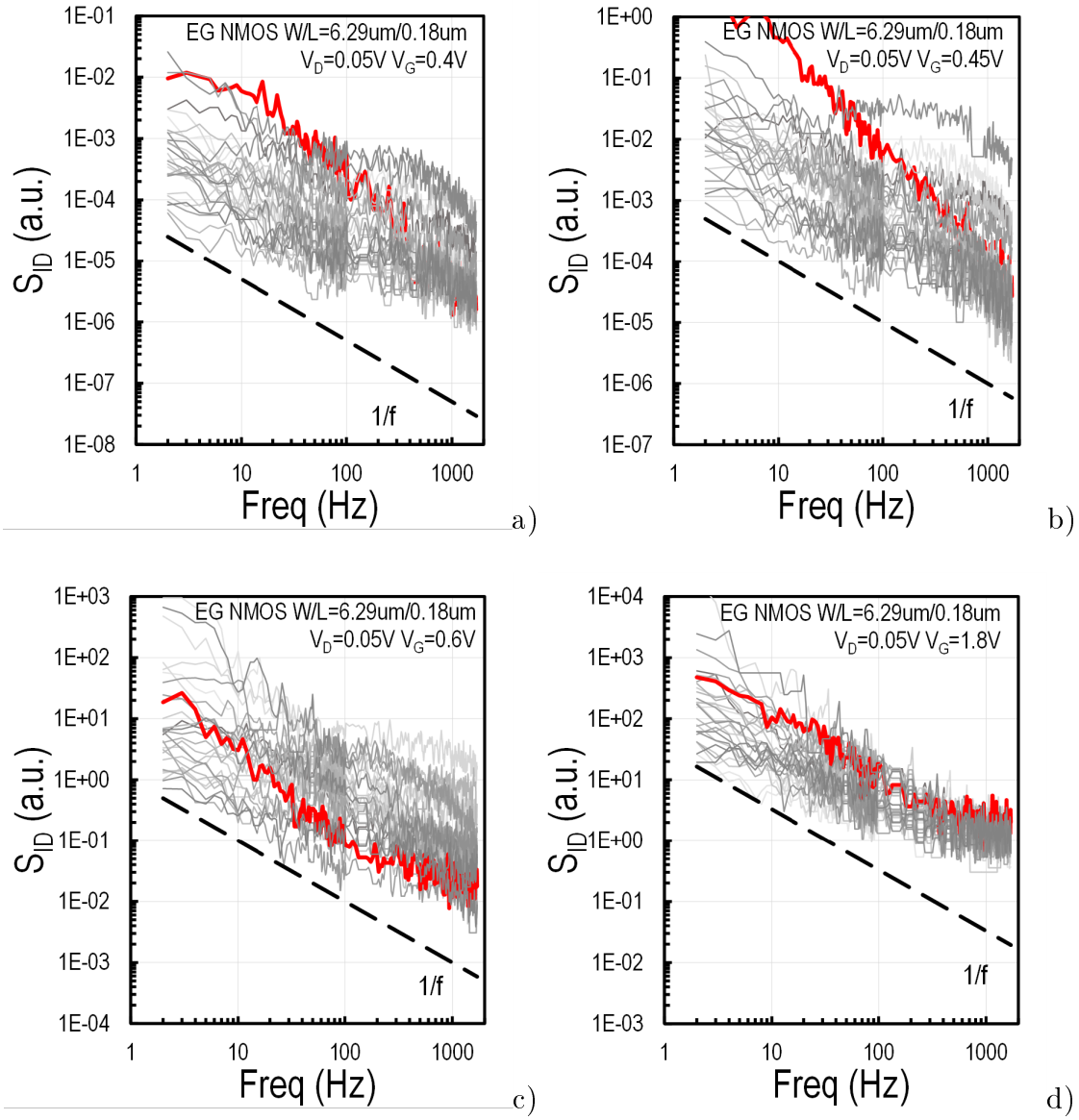


Figure 5.30: Low frequency noise spectra (S_{ID} vs. frequency) of 50 short channel ($W/L = 6.29um/180nm$) enclosed gate NMOS transistors at $V_{GS} = 0.4, 0.45, 0.6\,and\,1.8V$, with $V_{DS} = 0.05V$ (linear mode). The highlighted (red) spectra are individual characteristics of the same transistor. $1/f$ slope is depicted

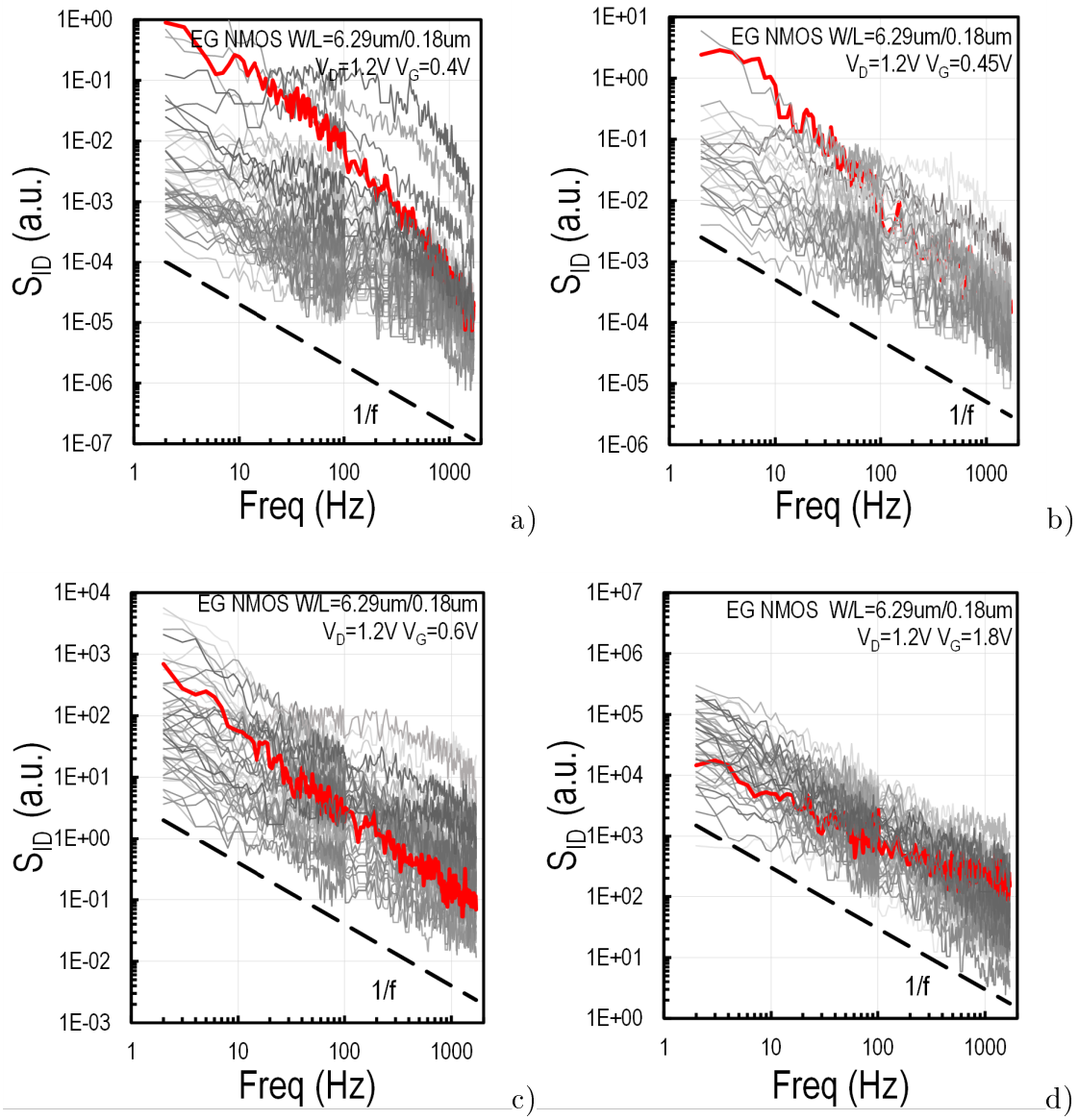


Figure 5.31: Low frequency noise spectra (S_{ID} vs. frequency) of 50 short channel ($W/L = 6.29um/180nm$) enclosed gate NMOS transistors at $V_{GS} = 0.4, 0.45, 0.6 and 1.8V$, with $V_{DS} = 1.2V$ (saturation mode). The highlighted (red) spectra are individual characteristics of the same transistor. $1/f$ slope is depicted

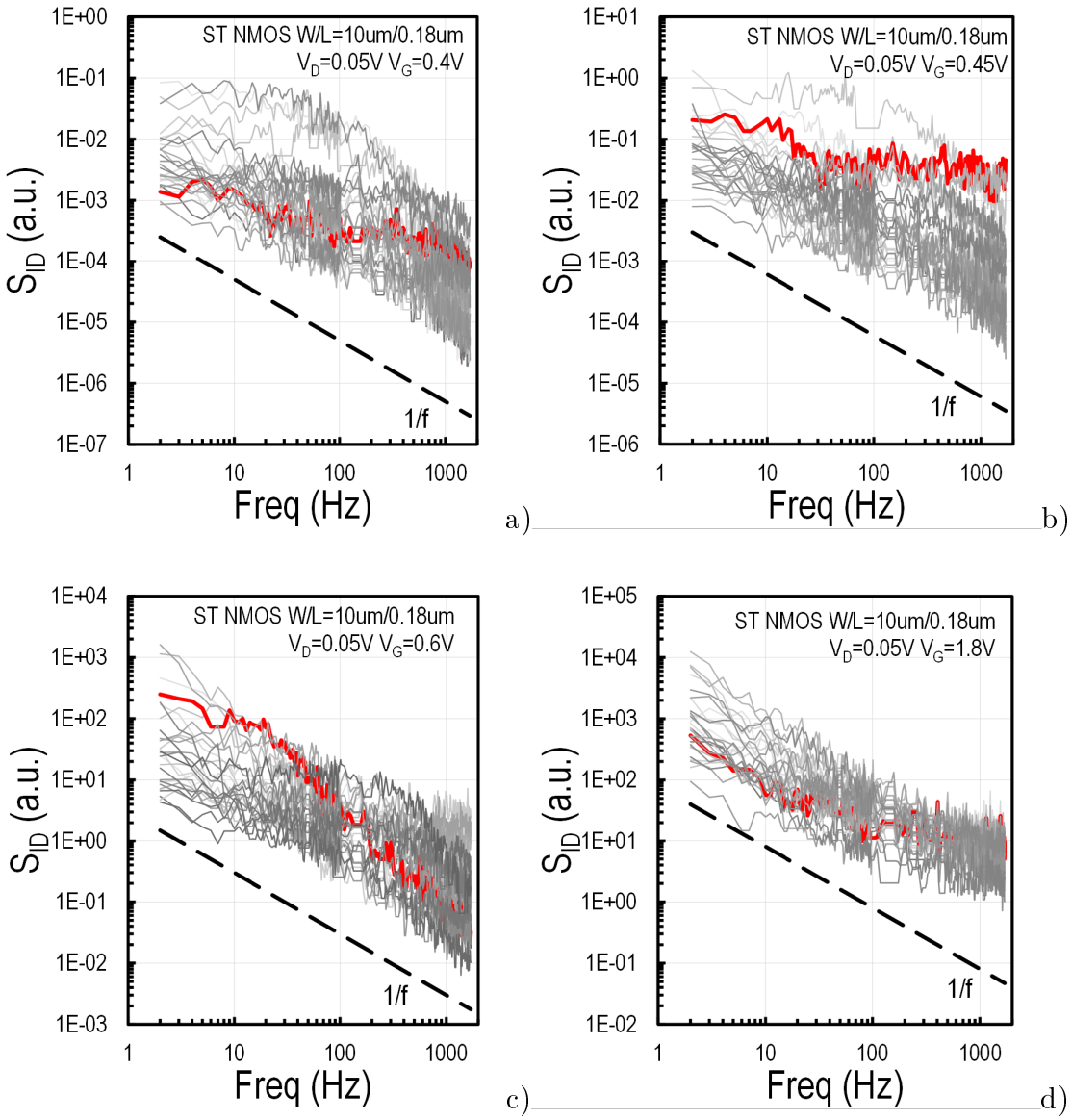


Figure 5.32: Low frequency noise spectra (S_{ID} vs. frequency) of 30 short channel ($W/L = 10um/180nm$) standard (ST) NMOS transistors at $V_{GS} = 0.4, 0.45, 0.6\,and\,1.8V$, with $V_{DS} = 0.05V$ (linear mode). The highlighted (red) spectra are individual characteristics of the same transistor. $1/f$ slope is depicted

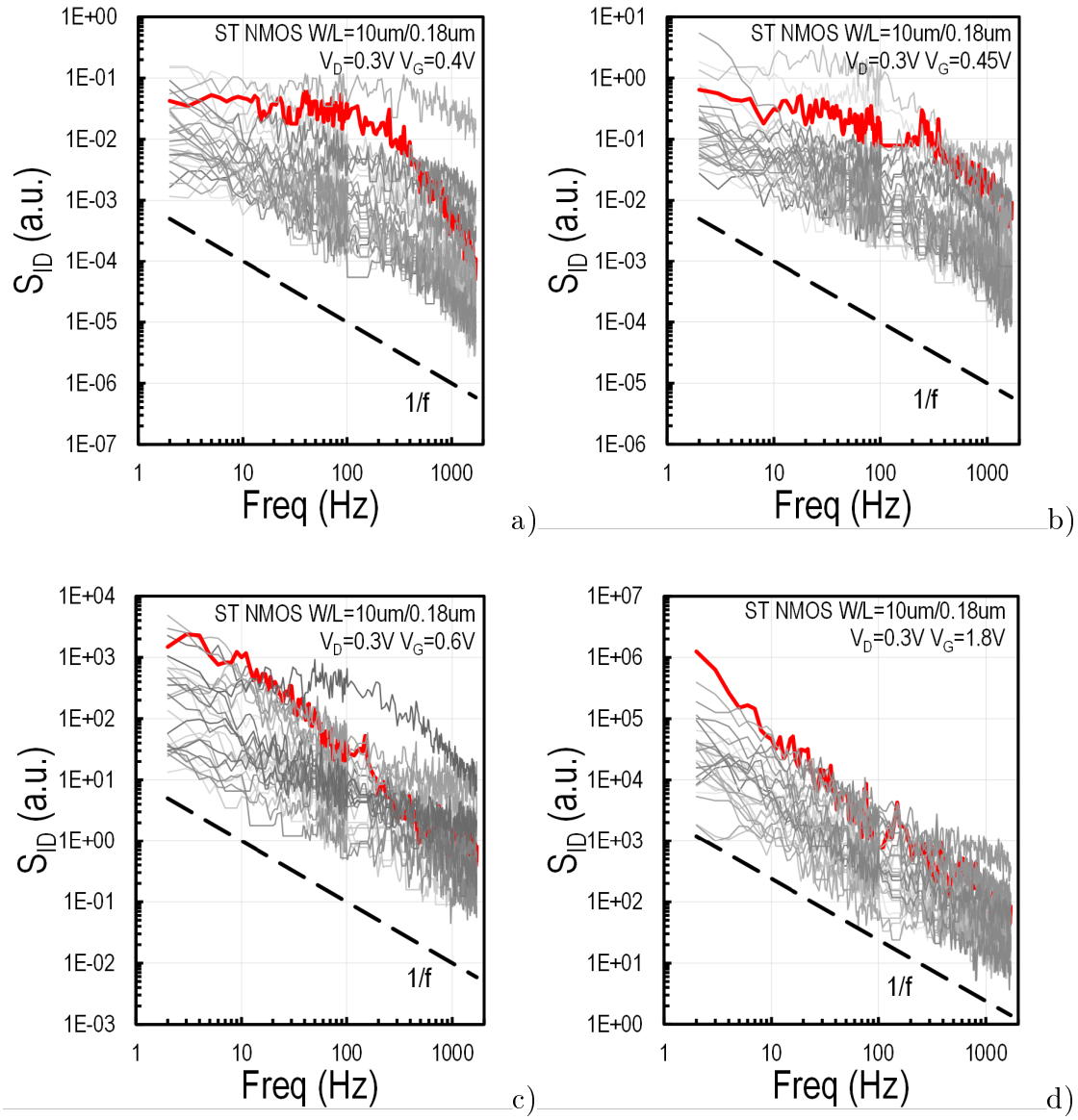


Figure 5.33: Low frequency noise spectra (S_{ID} vs. frequency) of 30 short channel ($W/L = 10um/180nm$) standard (ST) NMOS transistors at $V_{GS} = 0.4, 0.45, 0.6\,and\,1.8V$, with $V_{DS} = 0.3V$. The highlighted (red) spectra are individual characteristics of the same transistor. $1/f$ slope is depicted

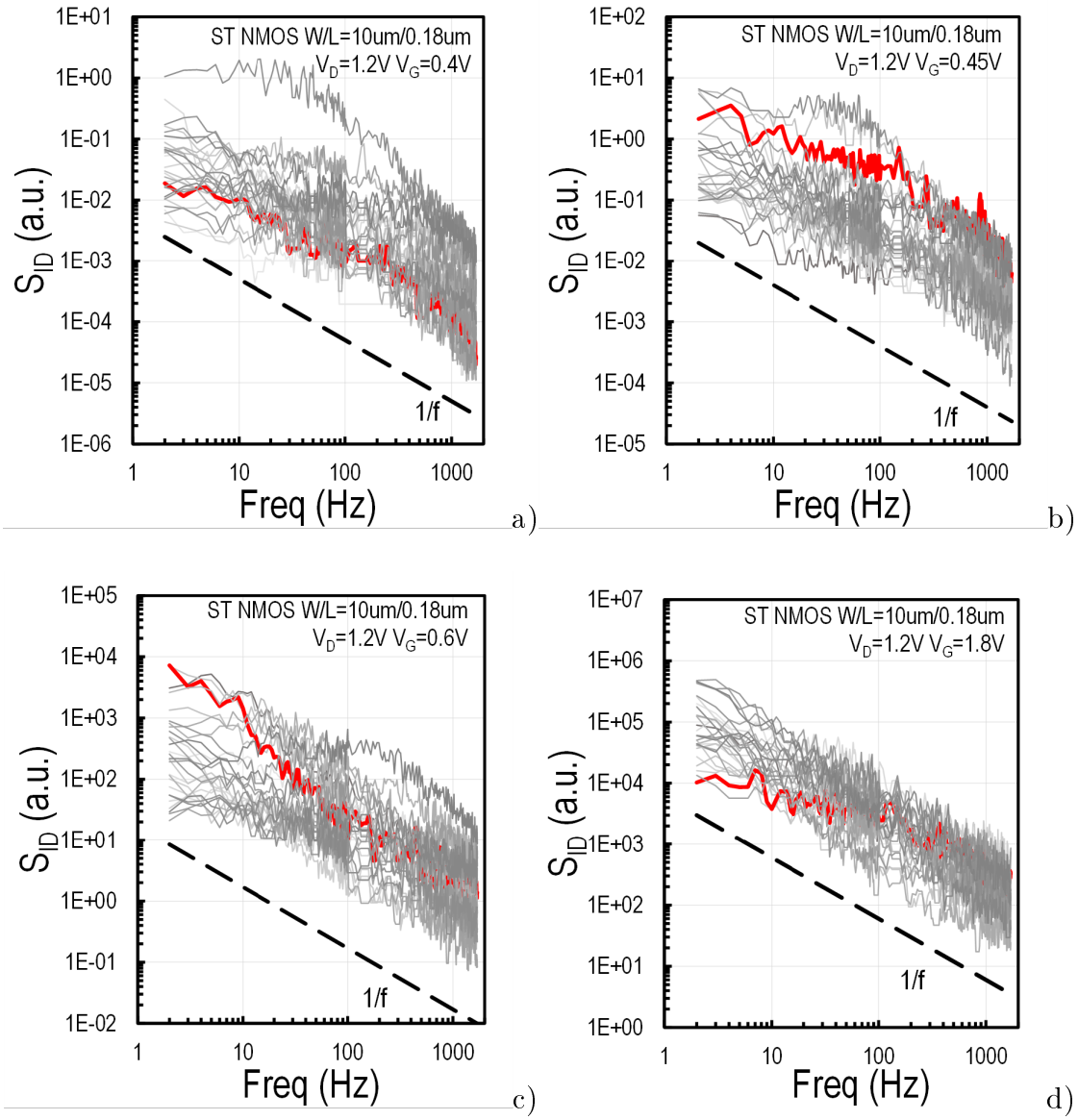


Figure 5.34: Low frequency noise spectra (S_{ID} vs. frequency) of 30 short channel ($W/L = 10um/180nm$) standard (ST) NMOS transistors at $V_{GS} = 0.4, 0.45, 0.6\,and\,1.8V$, with $V_{DS} = 1.2V$ (saturation mode). The highlighted (red) spectra are individual characteristics of the same transistor. $1/f$ slope is depicted

5.9 Extracted LFN Model

In this section the LFN charge based model described in Sections 4.8 and 4.9 is applied to nMOS transistors with enclosed and standard layouts. In Figure 5.31(a) the LFN power spectral density (PSD) $WLS_{ID}f/I_D^2$ versus drain current of long channel ($L = 2um$) enclosed gate nMOSFETs, from weak to strong inversion in both linear ($V_D = 0.05V$) and saturation ($V_D = 1.2V$) regions, is depicted. Figure 5.31(b) shows the normalized standard deviation $\sigma(ln(S_{ID}/I_D^2))$ (b) vs. normalized drain current $I_D/(W/L)$ at $1Hz$ for the same transistors and bias conditions. In Figure 5.32 LFN PSDs are shown in the form of output (drain current noise) $S_{ID}f$ and input (gate referred noise) $S_{VG}f$ noise versus normalized drain current $I_D/(W/L)$. In all cases Markers represent the measured data and lines correspond to the charge based model.

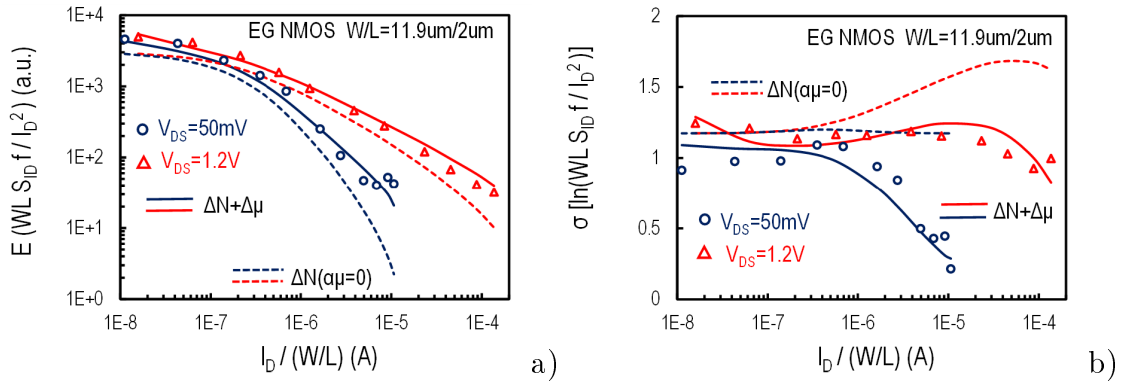


Figure 5.35: Normalized PSD S_{ID}/I_D^2 (a) and standard deviation $\sigma(ln(S_{ID}/I_D^2))$ (b) vs. normalized drain current $I_D/(W/L)$ at $1Hz$, at $V_D = 0.05, 1.2V$, for EG nMOSFETs with $L = 2um$. Markers: measured data, lines: model

From Figure 5.33 to 5.36 identical characteristics as in Figures 5.31 and 5.32 are shown for short channel ($L = 180nm$) EG and ST nMOSFETs. For the latter, 30 devices where measured including also at an intermediate drain voltage of $V_D = 0.3V$. Note that LFN statistical data are sensitive especially in weak inversion. LFN in all case is clearly dominated by the carrier number fluctuation (ΔN) effect while mobility fluctuation ($\Delta\mu$) effect is not apparent. When neglecting the correlated number and mobility fluctuation effect ($a\,\mu = 0$) the standard deviation $\sigma(ln(S_{ID}/I_D^2))$ takes a very different shape than observed from measurement. Overall, the model (lines) fits the measured data (markers) for either device qualitatively well.

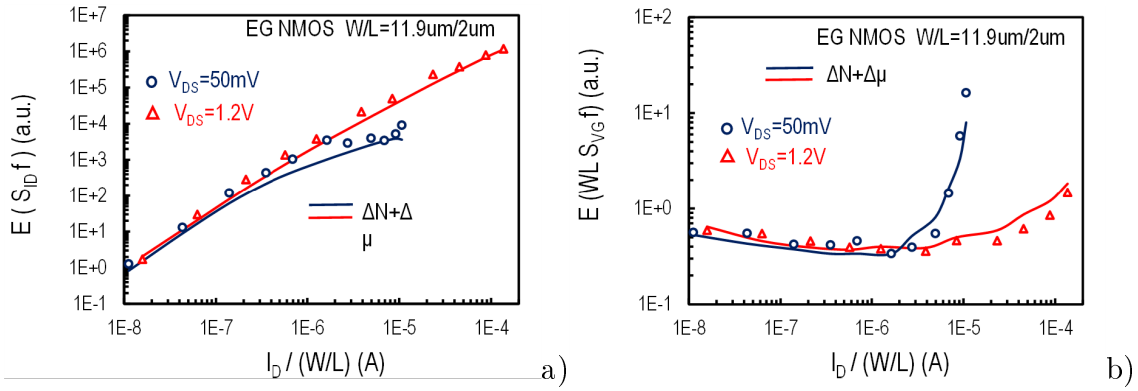


Figure 5.36: Output $S_{ID}f$ (a) and normalized gate referred $S_{VG}f$ (b) noise PSD, at $V_D = 0.05, 1.2V$, for EG nMOSFETs with $L = 2um$. Markers: measured data, lines: model

PARAMETER	UNITS	EG nMOS $L = 2um$
N_T	$eV^{-1}cm^{-3}$	$1.5\,10^{17}$
a_c	VsC^{-1}	$5.5\,10^{3}$
a_H	-	$7\,10^{-7}$
E_{NT}	-	20
E_{aC}	-	0.1
E_{aH}	-	0.2

Table 7: Extracted parameters of LFN model for enclosed gate MOSFETs with $W/L = 11.9um/2um$

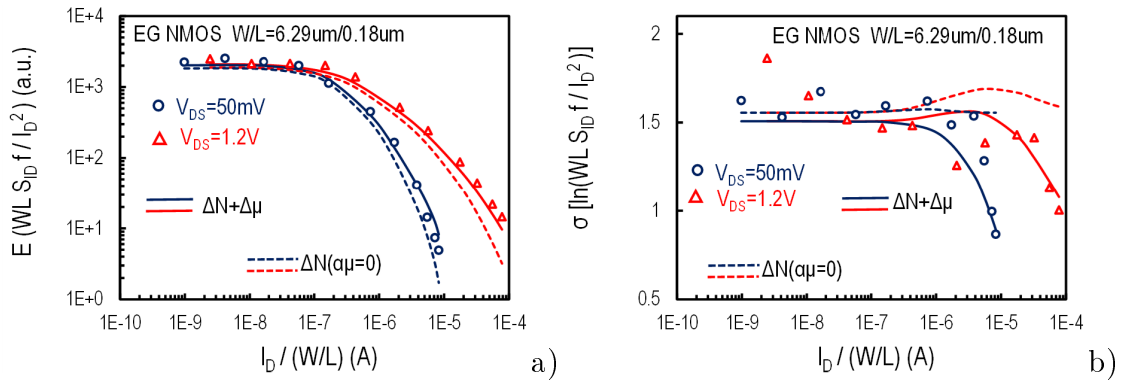


Figure 5.37: Normalized PSD S_{ID}/I_D^2 (a) and standard deviation $\sigma(ln(S_{ID}/I_D^2))$ (b) vs. normalized drain current $I_D/(W/L)$ at $1Hz$, at $V_D = 0.05$, $1.2V$, for enclosed gate nMOSFETs with $W/L = 6.29um/0.18um$. Markers: measured data, lines: model

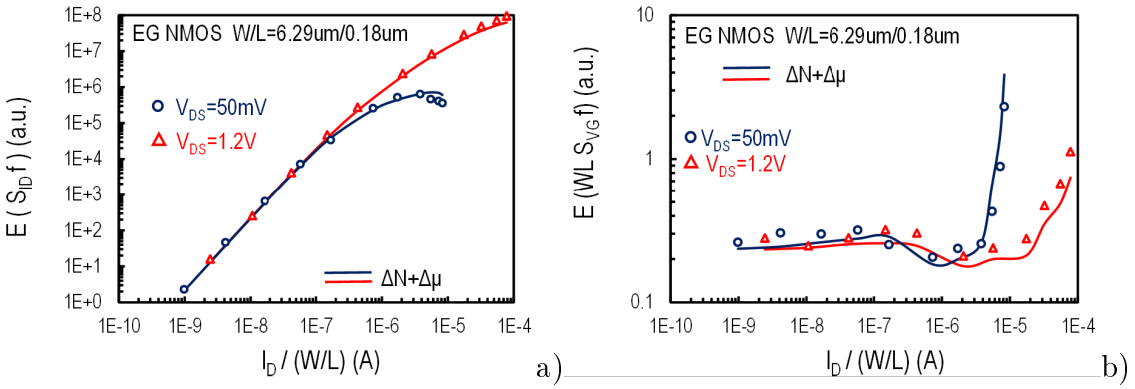


Figure 5.38: Output S_{ID} (a) and normalized gate referred S_{VG} (b) noise PSD at $1Hz$, at $V_D = 0.05$, $1.2V$, for enclosed gate nMOSFETs with $W/L = 6.29um/0.18um$. Markers: measured data, lines: model

PARAMETER	UNITS	EG nMOS $L = 0.18m$
N_T	$eV^{-1}cm^{-3}$	$6\,10^{16}$
a_c	VsC^{-1}	$3\,10^{3}$
a_H	-	0
E_{NT}	-	1.8
E_{aC}	-	2
E_{aH}	-	1

Table 8: Extracted parameters of LFN model for enclosed gate MOSFETs with $W/L = 6.29um/0.18um$

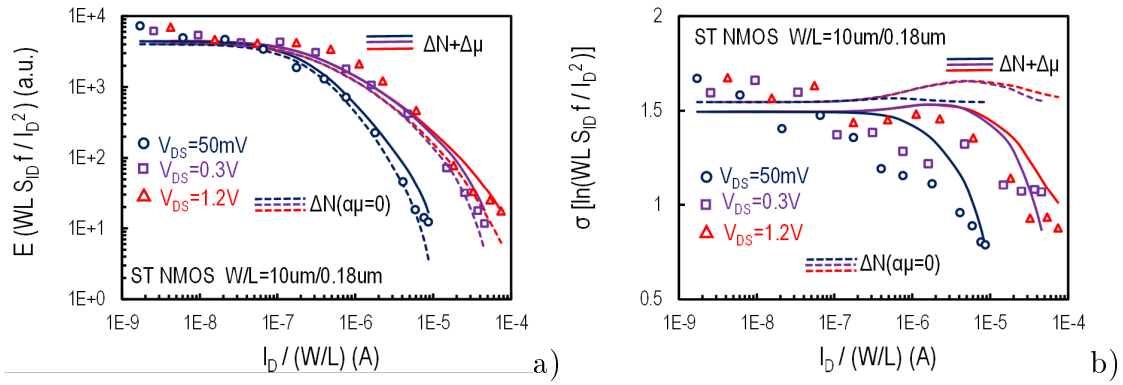


Figure 5.39: Normalized PSD S_{ID}/I_D^2 (a) and standard deviation $\sigma(ln(S_{ID}/I_D^2))$ (b) vs. normalized drain current $I_D/(W/L)$ at $1Hz$, at $V_D = 0.05,\ 0.3,\ 1.2V$, for standard nMOSFETs with $W/L = 10um/0.18um$. Markers: measured data, lines: model

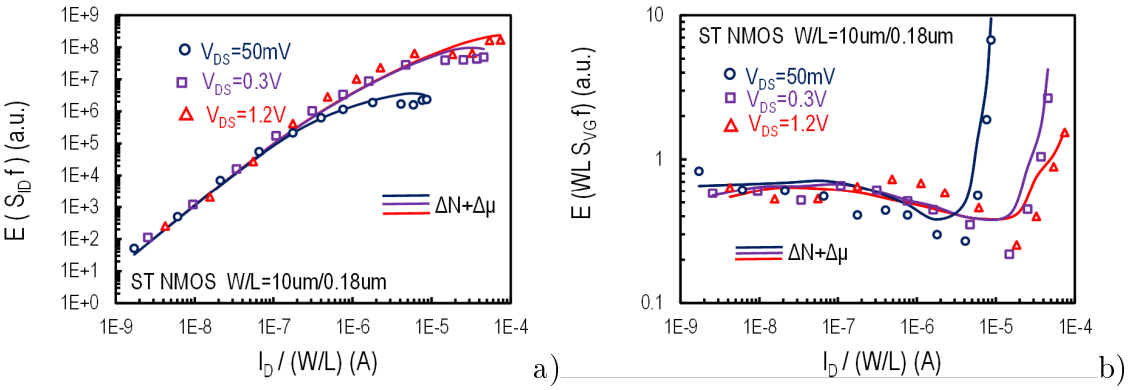
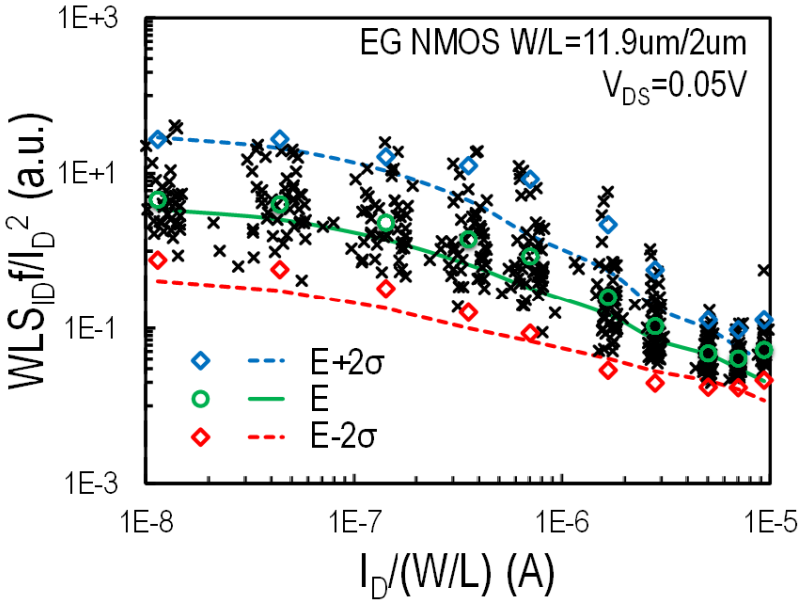


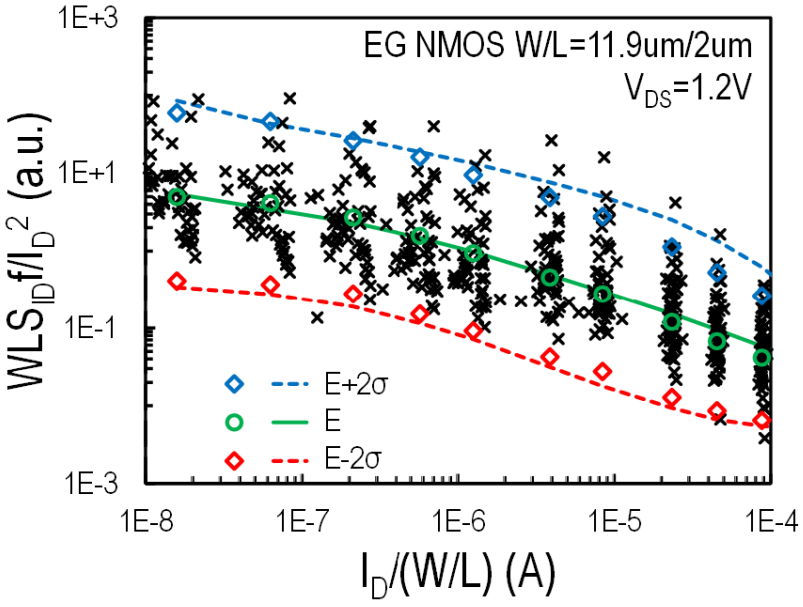
Figure 5.40: Output S_{ID} (a) and normalized gate referred S_{VG} (b) noise PSD at $1Hz$, at $V_D = 0.05,\ 0.3,\ 1.2V$, for standard nMOSFETs with $W/L = 10um/0.18um$. Markers: measured data, lines: model

PARAMETER	UNITS	ST nMOS $L = 0.18m$
N_T	$eV^{-1}cm^{-3}$	$1.3\,10^{17}$
a_c	VsC^{-1}	$2.75\,10^{3}$
a_H	-	0
E_{NT}	-	5
E_{aC}	-	0.1
E_{aH}	-	1

Table 9: Extracted parameters of LFN model for standard nMOSFETs with $W/L = 10um/0.18um$

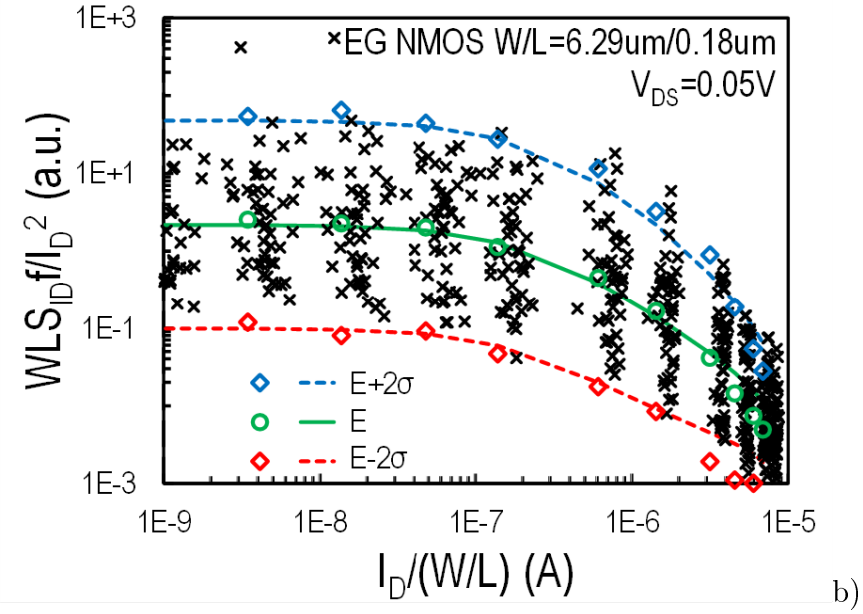


b)

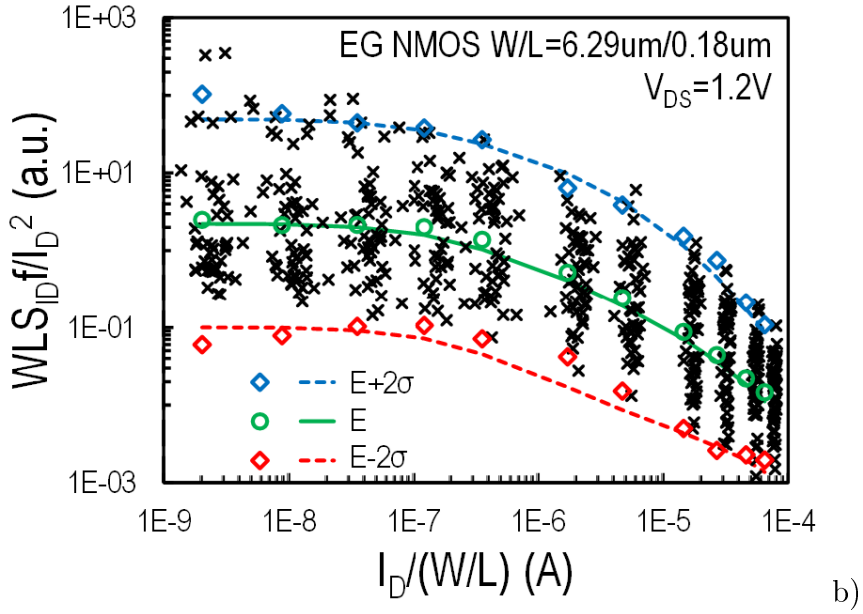


b)

Figure 5.41: Output noise WLS_{ID}/I_D^2, referred to at $1Hz$, measured in linear ($V_D = 0.05V$) (a) and saturation ($V_D = 1.2V$) (b) regions, for enclosed gate nMOSFETs with $W/L = 11.9um/2um$ vs. normalized drain current $I_D/(W/L)$. Measured noise: crosses. Measured average noise, $\pm 2\sigma$-deviation: open markers. Model: average noise (lines), $\pm 2\sigma$-deviation (dashed lines)

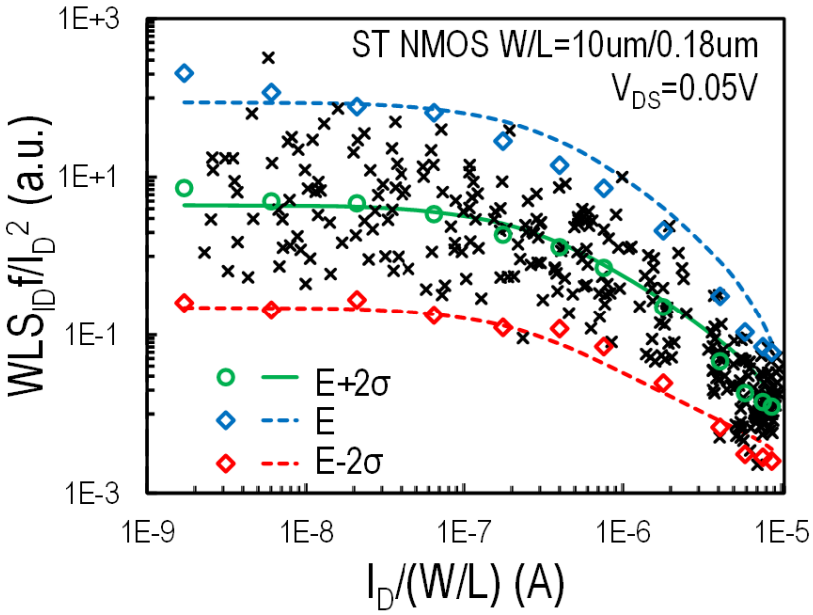


b)

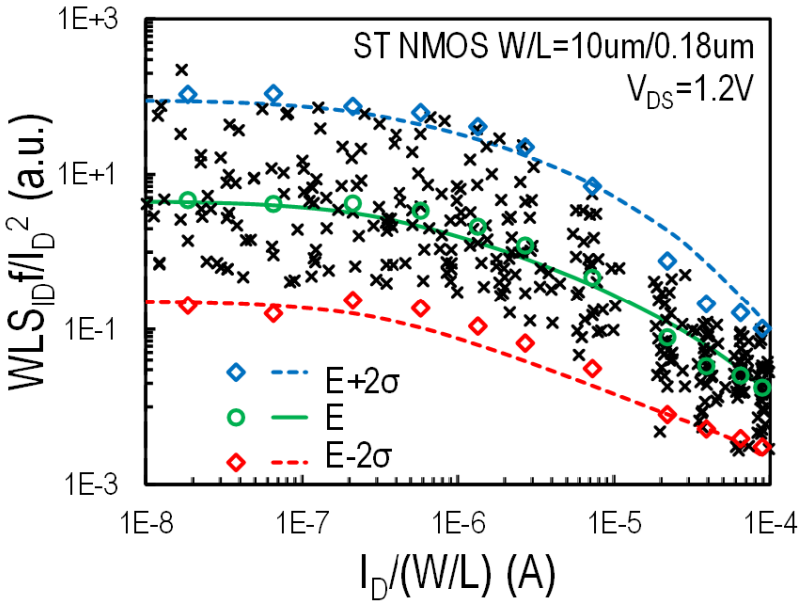


b)

Figure 5.42: Output noise WLS_{ID}/I_D^2, referred to at $1Hz$, measured in linear ($V_D = 0.05V$) (a) and saturation ($V_D = 1.2V$) (b) regions, for enclosed gate nMOSFETs with $W/L = 6.29um/180nm$ vs. normalized drain current $I_D/(W/L)$. Measured noise: crosses. Measured average noise, $\pm 2\sigma$-deviation: open markers. Model: average noise (lines), $\pm 2\sigma$-deviation (dashed lines)



b)



b)

Figure 5.43: Output noise WLS_{ID}/I_D^2, referred to at $1Hz$, measured in linear ($V_D = 0.05V$) (a) and saturation ($V_D = 1.2V$) (b) regions, for standard nMOSFETs with $W/L = 10um/180nm$ vs. normalized drain current $I_D/(W/L)$. Measured noise: crosses. Measured average noise, $\pm 2\sigma$-deviation: open markers. Model: average noise (lines), $\pm 2\sigma$-deviation (dashed lines)

5.10 LFN impact on ST and EG nMOSFETs:Direct comparison

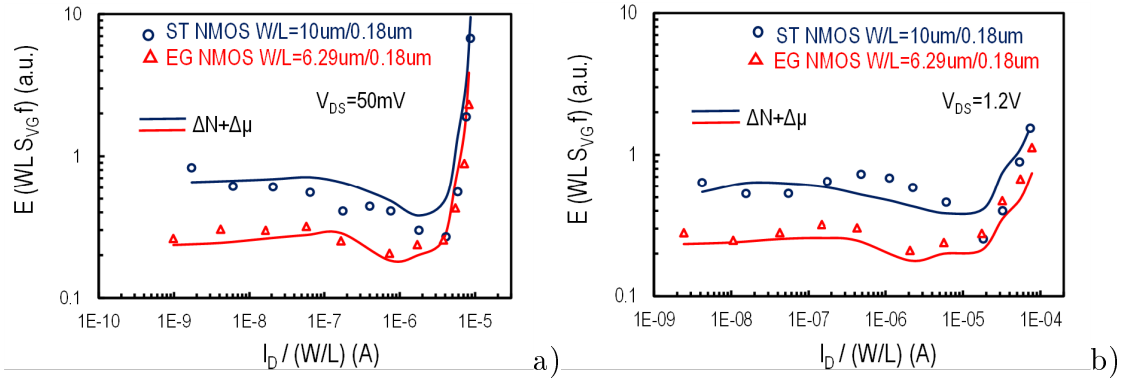


Figure 5.44: Comparison of gate referred noise PSD WLS_{VG} vs. $I_D/(W/L)$ at $1Hz$, in standard and enclosed gate nMOSFETs operating in linear ($V_D = 0.05V$) (a) and saturation ($V_D = 1.2V$) (b) mode. Markers: measured data, lines: model

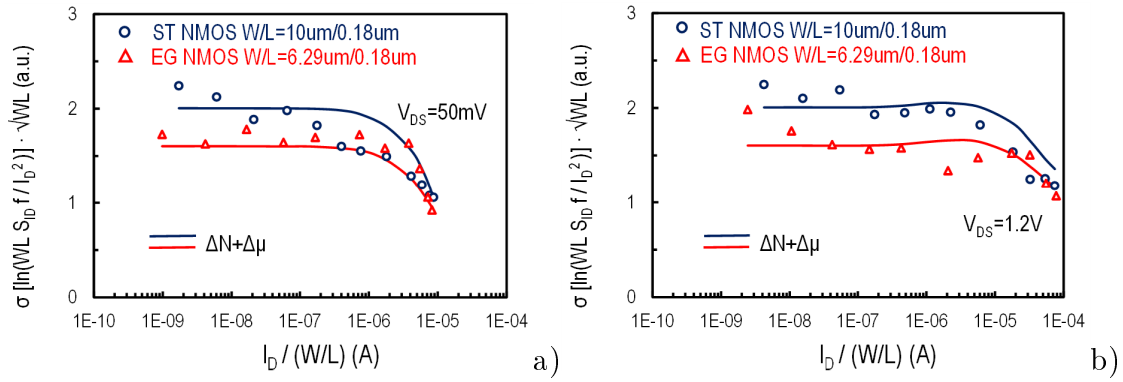


Figure 5.45: Comparison of standard deviation $\sigma(WLln(S_{ID}/I_D^2))$ vs. normalized drain current $I_D/(W/L)$ at $1Hz$, in standard and enclosed gate nMOSFETs, operating in linear ($V_D = 0.05V$) (a) and saturation ($V_D = 1.2V$) (b) mode. Markers: measured data, lines: model

5.11 Charge based model vs. LFN measured spectra

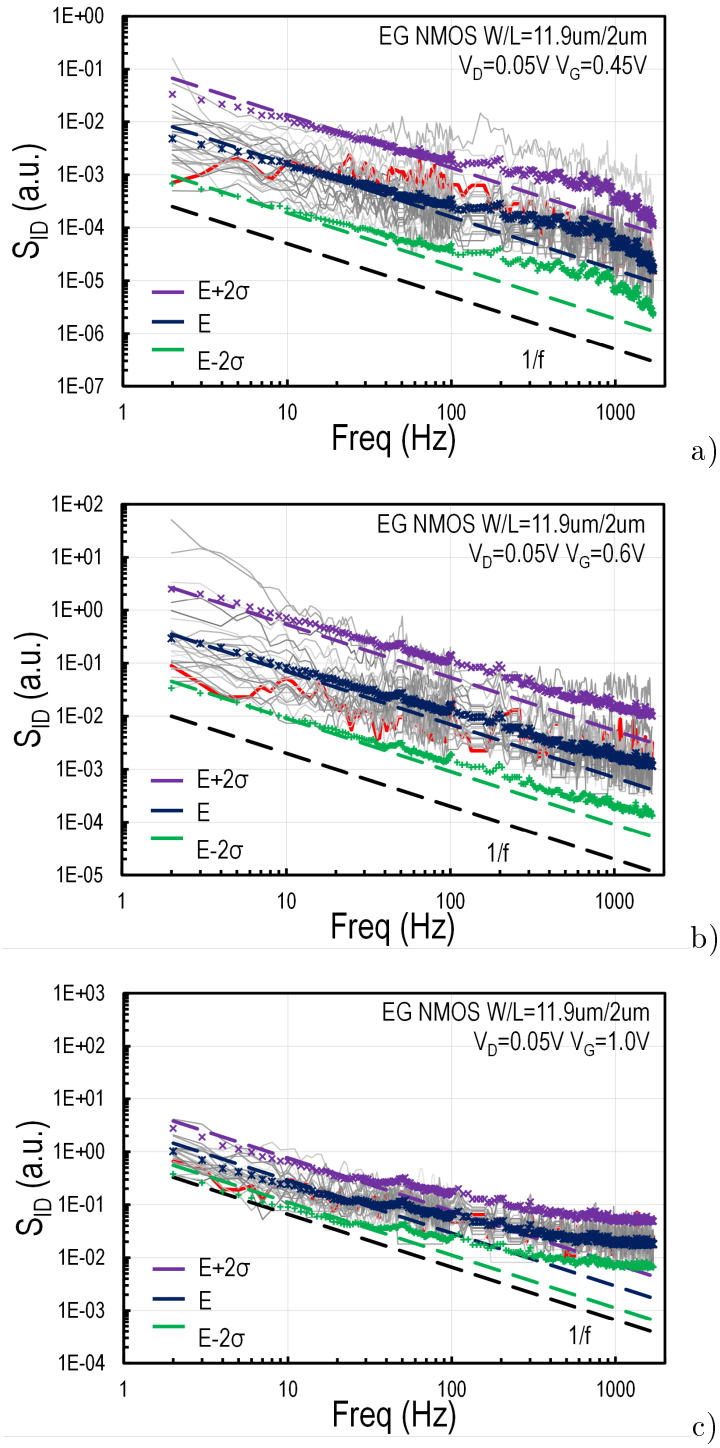


Figure 5.46: Low frequency noise spectra (S_{ID} vs. frequency) of 30 short channel ($W/L = 10um/180nm$) standard (ST) NMOS transistors at $V_{GS} = 0.4, 0.45, 0.6 and 1.8V$, with $V_{DS} = 1.2V$ (saturation mode). The highlighted (red) spectra are individual characteristics of the same transistor. $1/f$ slope is depicted

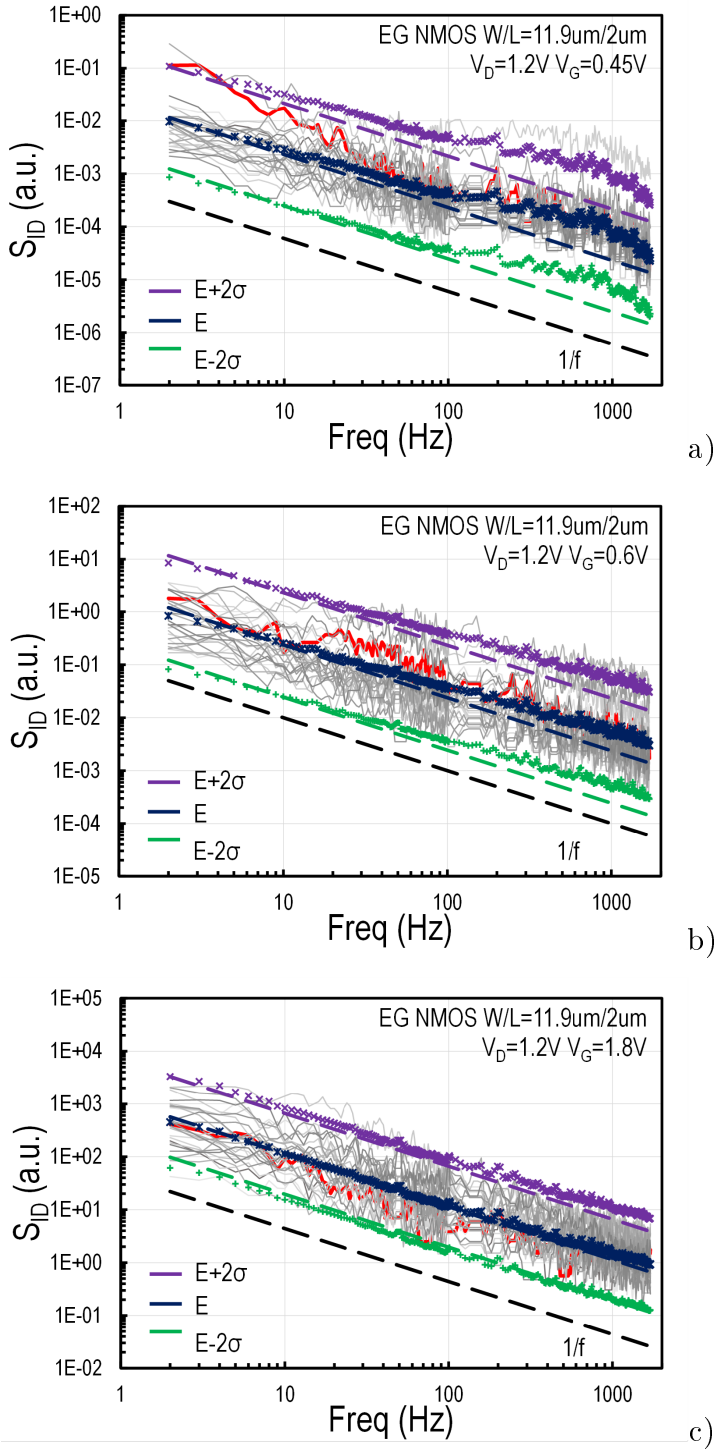
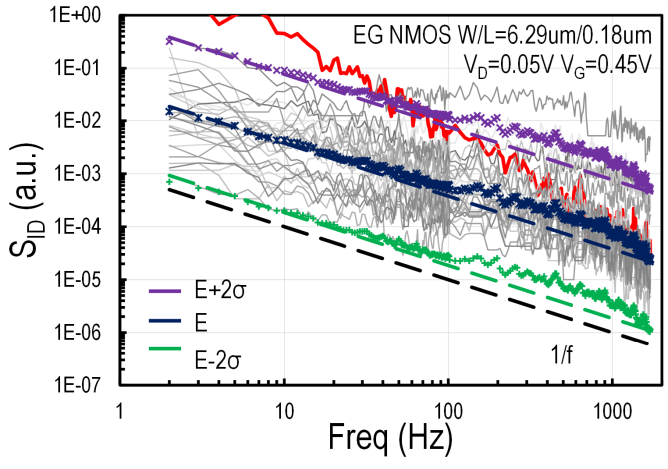
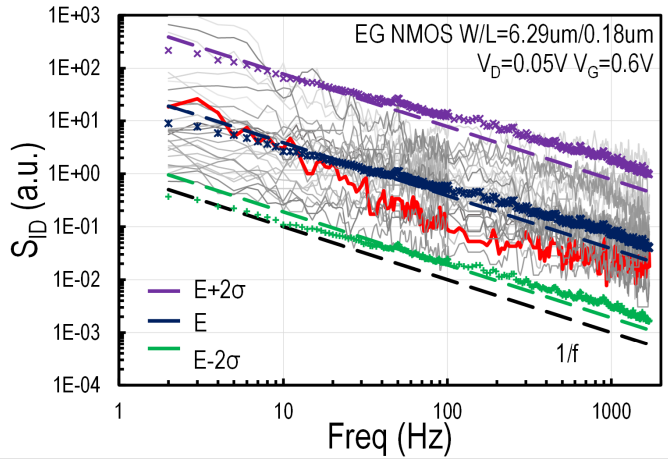


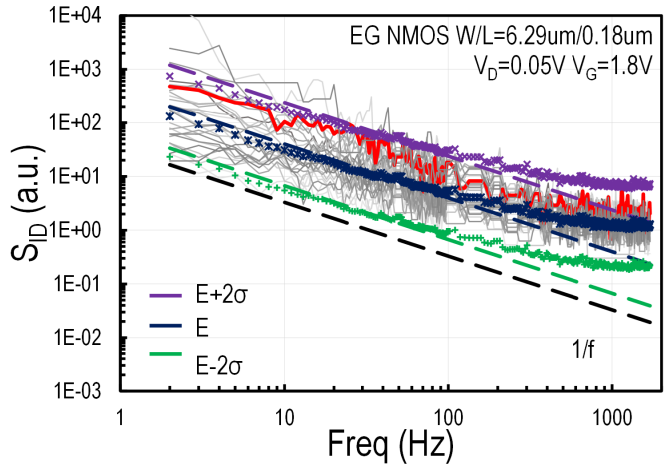
Figure 5.47: Low frequency noise spectra (S_{ID} vs. frequency) of 30 short channel ($W/L = 10um/180nm$) standard (ST) NMOS transistors at $V_{GS} = 0.4, 0.45, 0.6 and 1.8V$, with $V_{DS} = 1.2V$ (saturation mode). The highlighted (red) spectra are individual characteristics of the same transistor. $1/f$ slope is depicted



a)

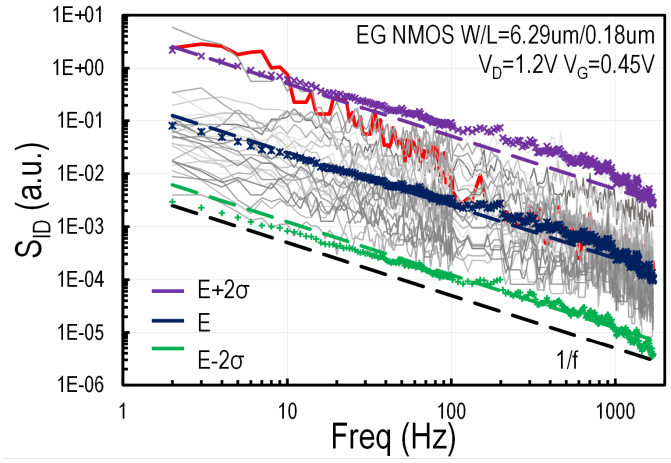


b)

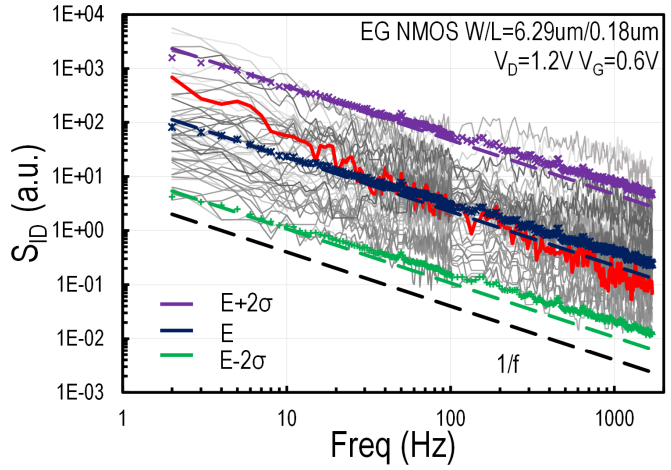


c)

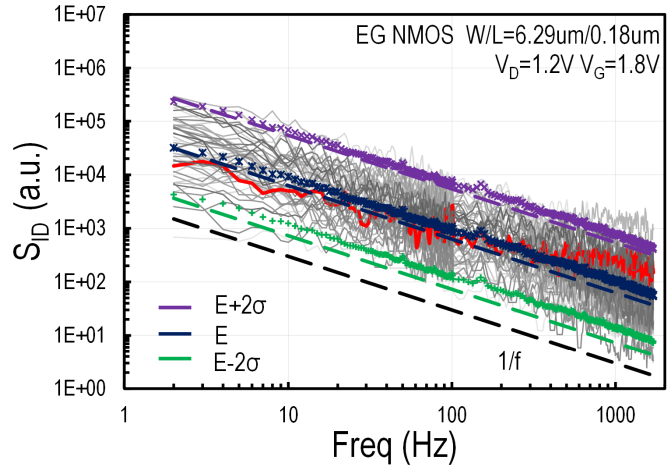
Figure 5.48: Low frequency noise spectra (S_{ID} vs. frequency) of 30 short channel ($W/L = 10um/180nm$) standard (ST) NMOS transistors at $V_{GS} = 0.4, 0.45, 0.6 and 1.8V$, with $V_{DS} = 1.2V$ (saturation mode). The highlighted (red) spectra are individual characteristics of the same transistor. $1/f$ slope is depicted



a)



b)



c)

Figure 5.49: Low frequency noise spectra (S_{ID} vs. frequency) of 30 short channel ($W/L = 10um/180nm$) standard (ST) NMOS transistors at $V_{GS} = 0.4, 0.45, 0.6 and 1.8V$, with $V_{DS} = 1.2V$ (saturation mode). The highlighted (red) spectra are individual characteristics of the same transistor. $1/f$ slope is depicted

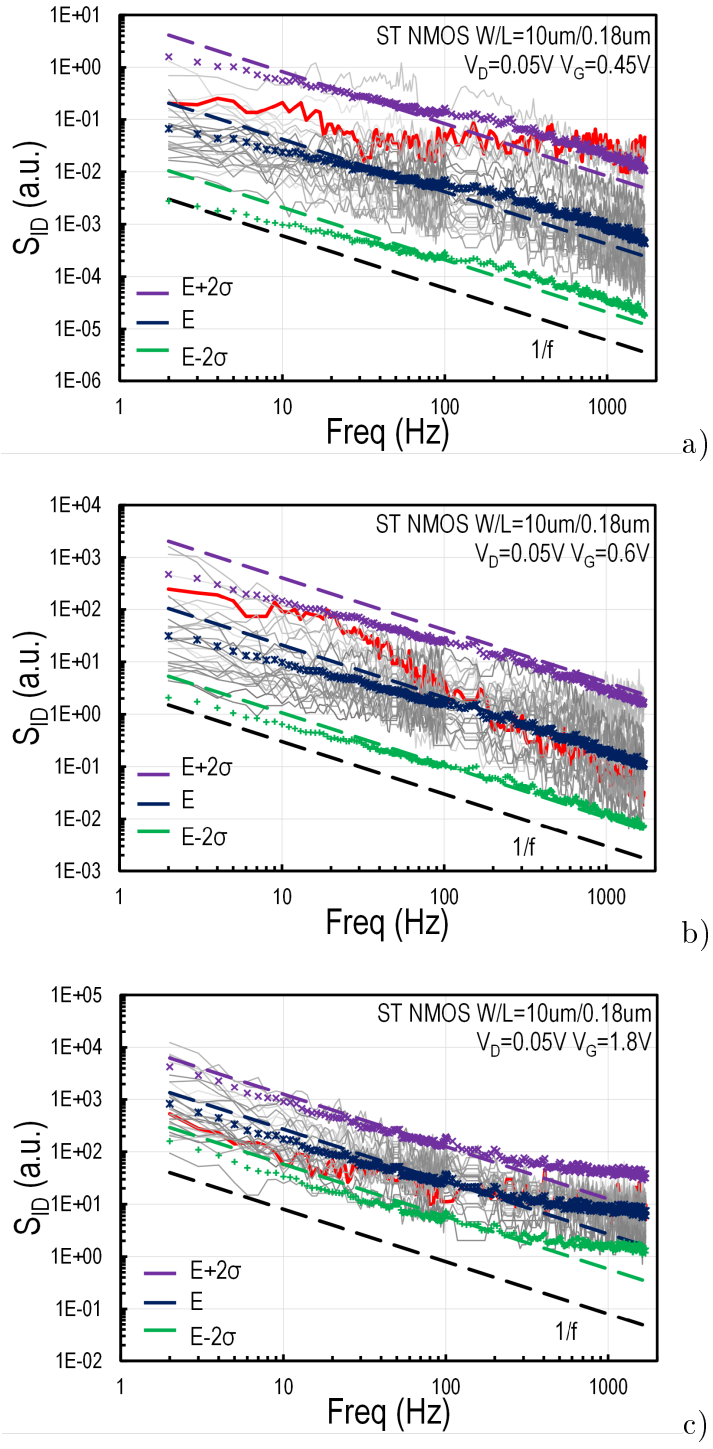
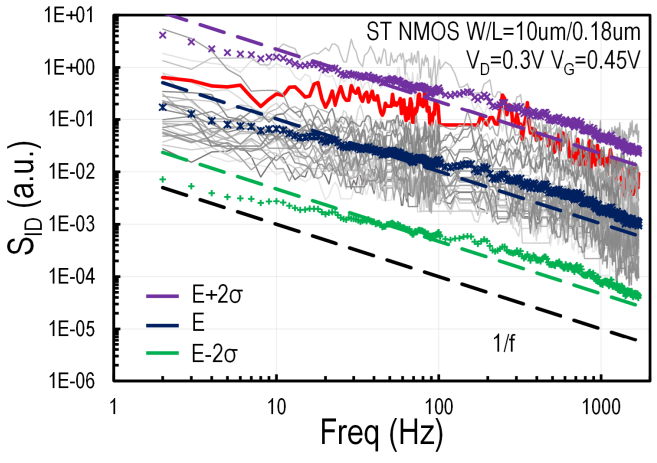
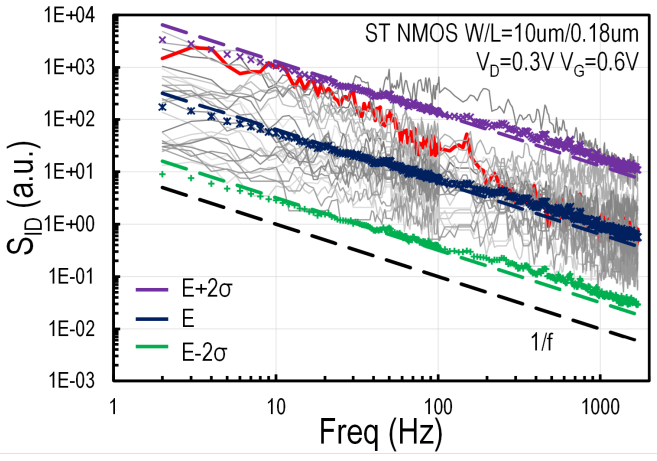


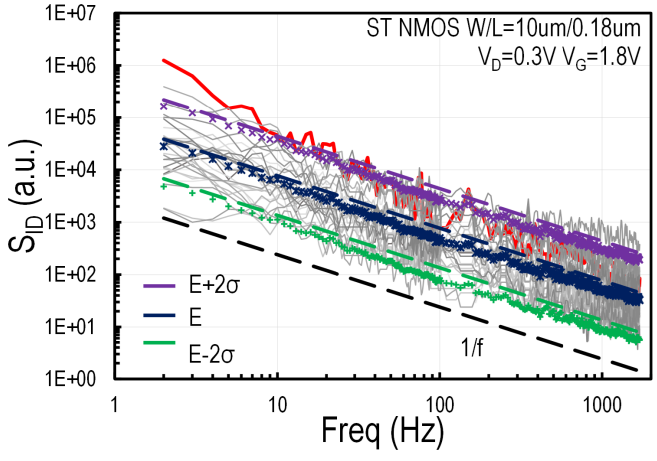
Figure 5.50: Low frequency noise spectra of 30 short channel standard NMOS transistors at $V_{GS} = 0.45, 0.6\,and\,1.8V$ in linear mode ($V_{DS} = 0.05V$). The highlighted (red) spectra are individual characteristics of the same transistor. Markers: measured ln-mean value E and $E \pm 2\sigma$. Lines: model.$1/f$ slope is depicted



a)

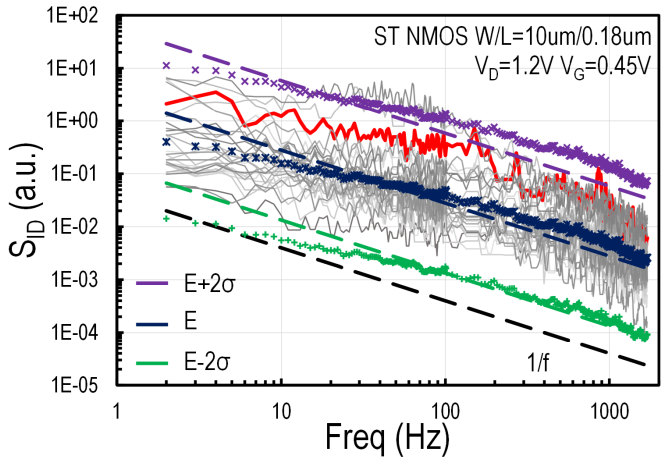


b)

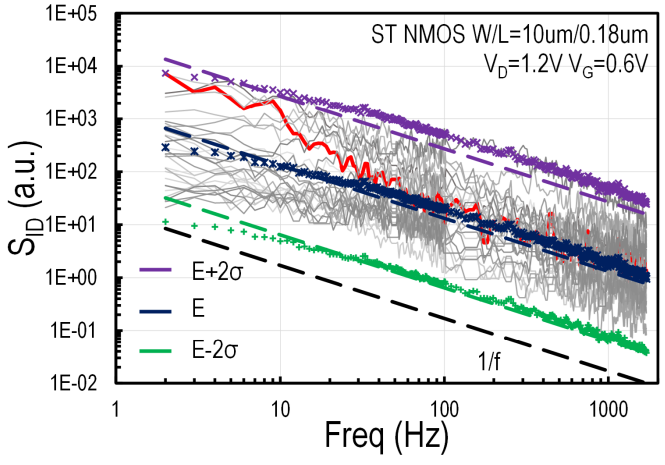


c)

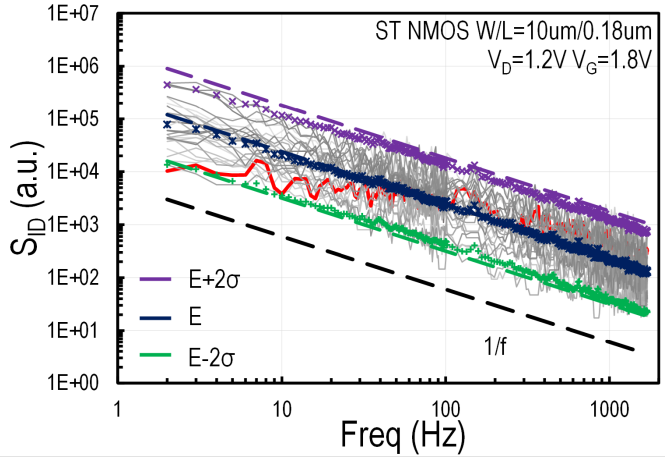
Figure 5.51: Low frequency noise spectra of 30 short channel standard NMOS transistors at $V_{GS} = 0.45, 0.6\,and\,1.8V$ at $V_{DS} = 0.3V$. The highlighted (red) spectra are individual characteristics of the same transistor. Markers: measured ln-mean value E and $E \pm 2\sigma$. Lines: model.$1/f$ slope is depicted



a)



b)



c)

Figure 5.52: Low frequency noise spectra of 30 short channel standard NMOS transistors at $V_{GS} = 0.45,\ 0.6\,and\,1.8V$ in saturation ($V_{DS} = 1.2V$). The highlighted (red) spectra are individual characteristics of the same transistor. Markers: measured ln-mean value E and $E \pm 2\sigma$. Lines: model.$1/f$ slope is depicted

5.12 Impact of TID on LFN

In current Section the basic effects of high TID on low frequency noise will be discussed. As reported in [71], when a MOSFET is exposed on high doses of ionizing radiation, up to $600\,Mrad(SiO_2)$, a $10\% - 20\%$ increment of LFN mean value can be observed. TID impact on LFN is mostly pronounced in WI. Furthermore, at higher frequencies, beyond corner frequency f_c, thermal noise is practically unaffected by TID exposure. At lower doses, up to $10\,Mrad(SiO_2)$, the major degradation mechanism can be attributed to the positive charge build-up (Q_{ot}) at the STI field oxides. Regarding LFN annealing effects, those depend on the type of the substrate and as reported in [72], Ge pMOS devices anneal more quickly than Si pMOS devices. Moreover, an increase halo implant dose can increase leakage current, enhance interface trap build up (Q_{it}) and decrease LFN performance in radiated MOSFETs [72].

6 Conclusions

In conclusion, a 65 nm bulk CMOS process has been investigated for analog performance with TID experiments up to $500 Mrad(SiO_2)$. The present work provides detailed insight into TID sensitivity of key analog performance parameters of devices, as well as their basic length-dependent scaling. Enclosed gate layout offers significant advantages over standard layout, and is particularly effective for EG nMOSFETs in suppressing effects related to high TID. EG layout devices are shown to have better DIBL, slope factor, and intrinsic gain, even for pre-radiation conditions, as compared to devices with standard layout. An EKV-type modeling approach has been shown to be highly effective in describing saturated drain current and transconductance throughout all inversion conditions. The model is based on four TID- and length- dependent parameters, namely threshold voltage V_{TO}, slope factor n, technology current I_0, and leakage current. Velocity saturation related parameterλ_c is shown to be rather insensitive to TID, for both enclosed gate and standard layout devices. Velocity saturation behavior is only marginally affected by TID and layout.

Enclosed gate nMOS transistors show reduced low frequency noise levels compared to standard the same technology, reduced by a factor of 2 to 3 in weak moderate inversion. Furthermore, the EG nMOS devices show also a reduced standard deviation of LFN. These improvements are all attributed to the absence of the STI-edge effect in the enclosed structures. The 50 measured devices show a behavior at higher gate voltages, while RTN components appear at gate voltages around moderate and weak inversion. The statistical LFN model can cover accurately both gate drain-voltage bias-dependence of average noise and its standard deviation, similarly for enclosed-gate as well as standard-layout transistors.

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Author's Publications

1. L. Chevas, **A. Nikolaou**, M. Bucher, N. Makris, A. Papadopoulou, A. Zografos, G. Borghello, H.D. Koch, F. Faccio, "Investigation of scaling and temperature effects in total ionizing dose (TID) experiments in 65nm CMOS", 25th Int. Conf. Mixed Design of Integrated Circuits and Systems (MIXDES), Gdansk, Poland, June 21-23, 2018. (ieeexplore)

2. **A. Nikolaou**, M. Bucher, N. Makris, A. Papadopoulou, L. Chevas, G. Borghello, H. D. Koch, K. Kloukinas, T. S. Poikela, F. Faccio, "Extending a 65 nm CMOS Process Design Kit for High Total Ionizing Dose Effects", IEEE Int. Conf. on Modern Circuits and Systems Technologies (MOCAST), pp. 1-4, Thessaloniki, Greece, May 7-9, 2018. DOI:10.1109/MOCAST.2018.8376561.

3. M. Bucher, **A. Nikolaou**, A. Papadopoulou, N. Makris, L. Chevas, G. Borghello, H. D. Koch, F. Faccio, "Total Ionizing Dose Effects on Analog Performance of 65 nm Bulk CMOS with Enclosed-Gate and Standard Layout", 31st IEEE Int. Conf. on Microelectronic Test Structures (ICMTS), pp. 1-6, Austin, Texas, Mar. 19-22, 2018. DOI:10.1109/ICMTS.2018.8383790.

4. **A. Nikolaou**, N. Mavredakis, P. Habas, A. Acovic, R. Meyer, M. Bucher, "Statistical Analysis of 1/f Noise in Enclosed-Gate N- and PMOS Transistors", 24th Int. Conf. on Noise and Fluctuations (ICNF), pp. 1-4, Vilnius, Lithuania, June 20-23, 2017. DOI:10.1109/ICNF.2017.7986018.

5. M. Bucher, **A. Nikolaou**, N. Mavredakis, N. Makris, M. Coustans, J. Lolivier, P. Habas, A. Acovic, R. Meyer, "Variability of Low Frequency Noise and Mismatch in Enclosed-Gate and Standard nMOSFETs", 30th IEEE Int. Conf. on Microelectronic Test Structures (ICMTS), pp. 177-180, Grenoble, France, March 27-30, 2017. DOI:10.1109/ICMTS.2017.7954285.