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Study of Enclosed Gate P-Type MOS Field Effect Transistors – Characterization and Variability

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Abstract

A MOSFET (metal oxide semiconductor field effect transistor) is by far the most common transistor in digital circuits, as hundreds of thousands or millions of them may be included in a memory chip or microprocessor. Since they can be made with either p-type or n-type doped semiconductors, complementary pairs of MOS transistors can be used to make switching circuits with very low power consumption, in the form of CMOS (complementary metal oxide semiconductor) logic. The same transistors are used to implement analog circuitry, co-integrated with the digital circuits, to form systems-on-chip (SoCs).

Nowadays, many integrated circuits are designed to operate in radiation environments such as aircraft, medical, space, nuclear applications and high energy physical experiments. Radiation total ionizing dose effects (TID) degrade the performance and reliability of MOSFETs, giving rise to positive charge trapping at the edges of shallow trench isolation (STI) corners, resulting to the formation of leakage current paths from drain to source diffusions.

The use of transistors with enclosed gate layouts is the proposed solution for applications in radiation environments since due to their geometry and the absence of STI corners, leakage current paths along the edge of the active area are suppressed. However, enclosed gate MOS devices present drawbacks like: increased area and limitations in the choice of the W/L ratio that should be taken into consideration.

In this thesis we study enclosed gate (circular) P-type MOSFETs. Specifically, we present a statistical analysis to the results of the electrical parameters (threshold voltage, electron mobility, slope factor, transconductance, voltage-current dependence) for seven different geometries of those specific MOSFETs in linear mode as well as saturation mode. Also, a detailed study of the three basic parameters (threshold voltage, mobility, slope factor) is implemented, leading to useful conclusions regarding their variability.

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INTRODUCTION

1.1 MOSFETs

Recently, layout techniques for the safe operation of microelectronic devices in radiation harsh environments, such as in space or nuclear applications, have been proposed utilizing new commercial sub-micron CMOS technologies. Ultra -thin gate oxides are naturally radiation hard, thanks to the modest net charge trapping and negligible threshold voltage shift even after high dose irradiation. Nevertheless, other failure mechanisms related to gate oxide damage could be activated, such as the increase of the low-field leakage across the oxide itself.

On the other hand, thick oxides are still present in the isolation regions of CMOS components and can be quite sensitive to radiation damage. In fact, due to positive charge trapping, ionizing radiation may induce the formation of an inversion layer at the bird's beak or shallow trench corner or underneath the field oxide around NMOS, giving rise to various leakage current paths. MOSFETs with gate-enclosed layouts (GE-MOSFET) are used in traditional rich environments, radiation rich environments, as they can effectively survive such failure mechanisms as the increase of drain-to-source leakage current due to turn-on of parasitic transistors. The main drawbacks of these devices are represented by slow switching times, due to a larger input capacitance than in standard layouts, and large area consumption. These defects can be partially compensated by using aggressive CMOS technologies, such as quarter- and sub-quarter-micron technologies.

GE-MOSFETs were already proposed for logic applications 20 years ago. At that time, no analysis of the electrical characteristics of these devices was supplied. Nowadays, treatments of this problem can be found for particular shapes: circular, square or hexagonal.

In this contribution, we treat at length the circular GE-MOSFETs. Experimental measurements have been made and compared in various technologies starting from 0.18 μm to 10 μm minimum size.

1.2 Thesis structure

The structure of the thesis divided into 5 chapters:

1. Introduction on MOSFETS.
2. Basic MOSFETs structure and operation along with the special characteristics of MOSFETs with enclosed gate layout and especially that with circular gate.
3. The theory of MOSFET characteristics which later are going to be studied in the experimental process.
4. Complete experimental process and its results are presented and analyzed.
5. Conclusions

2.Device Structure & Physical Operation

2.1 Basic MOSFET structure

The MOS transistor is a field effect device, where the current flow in the longitudinal direction, from drain to source terminal in the region labeled as “channel region”, is modulated by the voltage applied at the gate [2, 4]. In Figure 2.1 the simplified structure of an NMOSFET is depicted. The four terminals of a MOSFET are: Gate (G), Source (S), Drain (D) and Body or Bulk (B). The transistor is fabricated in a p-type substrate silicon wafer, which provides physical support for the device, and consists of two heavily doped n-type diffusion regions, indicated in the figure as n+ drain and n+ source. The dimension of the gate along the source-drain path is called length L, whereas W is the width.

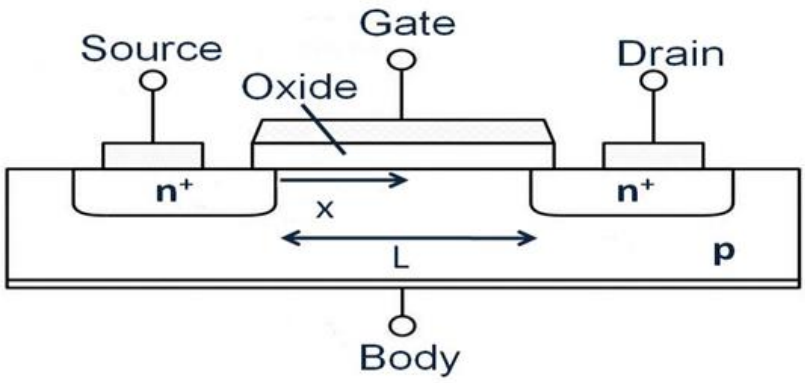


Figure 2. 1 *Cross-Section of an n-type MOS Transistor*

The surface between drain and source regions is covered with a thin layer of silicon dioxide (SiO2), which is an excellent electrical insulator, while a layer of polycrystalline silicon (or aluminum in older technologies) is deposited on top of the dielectric of the gate. The transistor structure is completely symmetrical with respect to source and drain. The role is defined by terminal voltages which establish the direction of carrier’s flow [1,2].

The PMOS transistor is a complementary structure to the NMOS transistor, it has a similar structure with n-type MOSFETs and they are fabricated in the same substrate. They have opposite doping types, with p+ drain and p+ source diffusions placed in a local substrate called n-type. In a PMOSFET the minority carriers are the positive holes whereas in an NMOSFET the negative electrons [2].

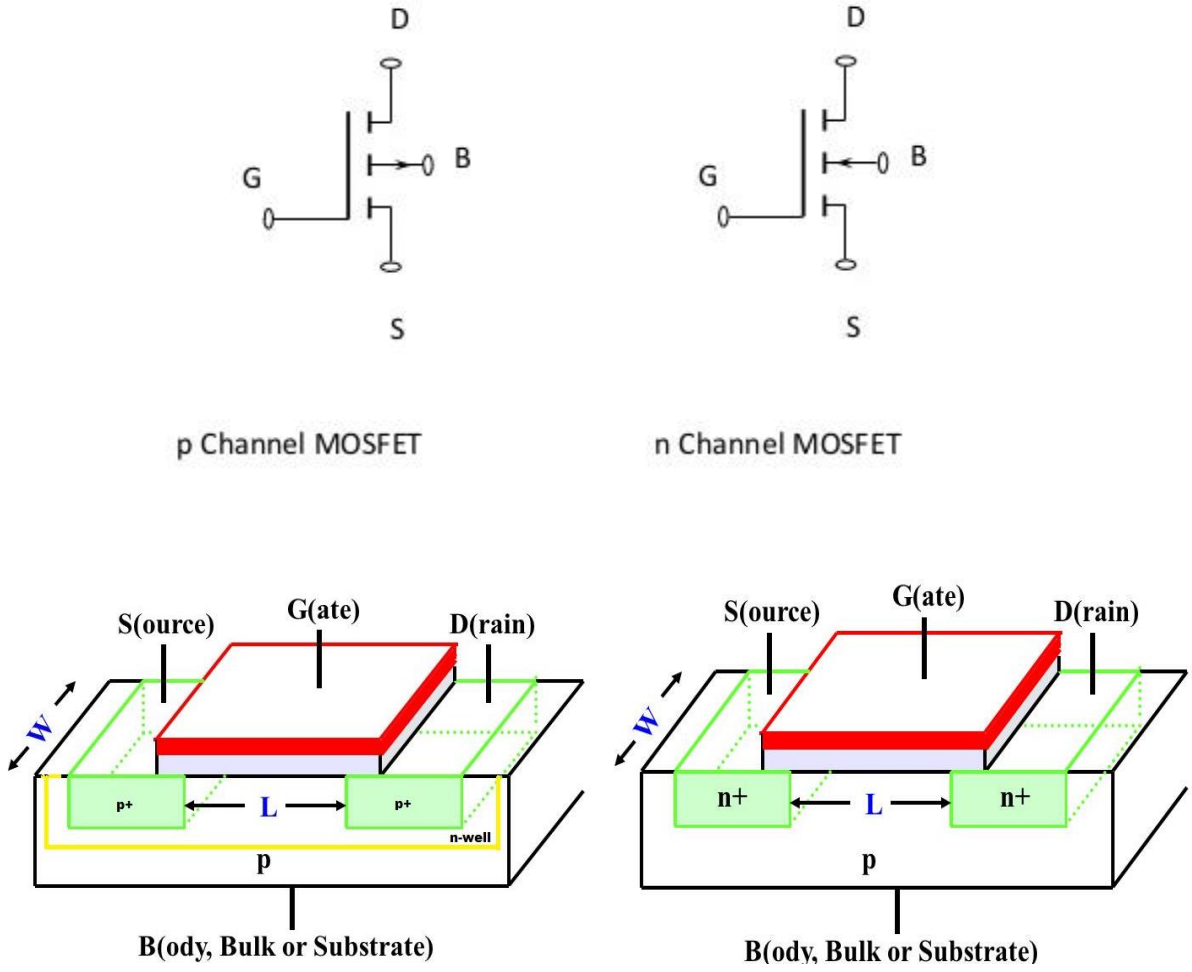


Figure 2. 2 *a) Circuit symbols, b) (left) Cross-Section of an NMOS device and (right) Cross-Section of a PMOS device.*

The potential of the substrate that the device is fabricated influences the device characteristics. In an NMOSFET the substrate is usually connected to the most negative supply of the system, usually the ground, and the actual connection is implemented through a p+ diffusion region, as illustrated in Figure 2.3 a). The n-type local substrate of a PMOSFET is tied to the most positive supply voltage through an n+ diffusion region (Figure 2.3 b) [1].

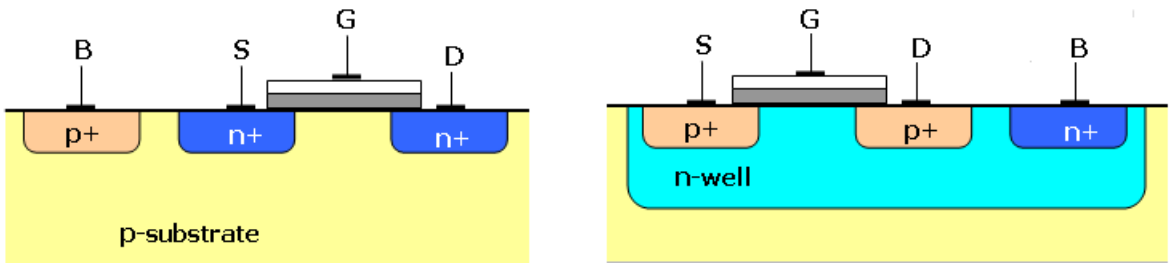


Figure 2. 3 *Substrate connection of a) an NMOSFET and b) a PMOSFET*

2.2 MOSFET Operation

2.2.1 Operation with gate Voltage

- With zero voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the *pn* junction between the *n*+ drain region and the *p*-type substrate, and the other diode is formed by the *pn* junction between the *p*-type substrate and the *n*+ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage *Vds* is applied.

- When gate voltage increases from zero (VGS>0), since gate and substrate form a capacitor (dielectric is SiO2), free holes are repelled from the substrate region under the gate leaving negative ions behind, and thus a depletion region is formed (Figure 2.4 a).

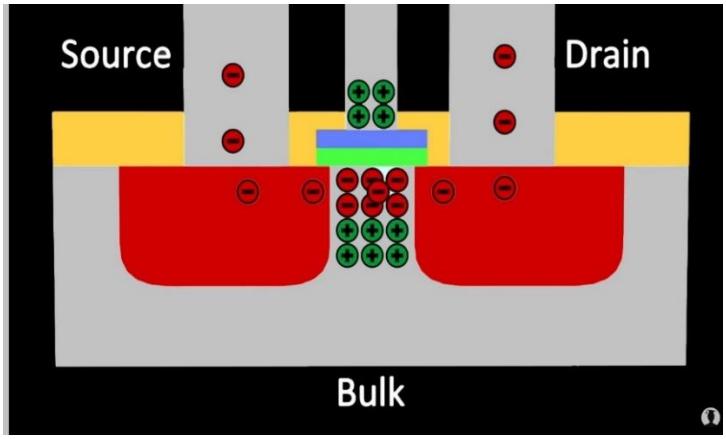


Figure 2. 4 a)

- As the gate voltage increases more, the width of the depletion region expands further and electrons are attracted from n+ drain and source areas, near the surface of the substrate under the gate oxide. When the gate voltage approaches a sufficiently positive value called the threshold voltage (VGS≈VTH), an n-type channel of charge carriers, or inversion layer, is formed connecting drain and source regions (figure2.4 b).

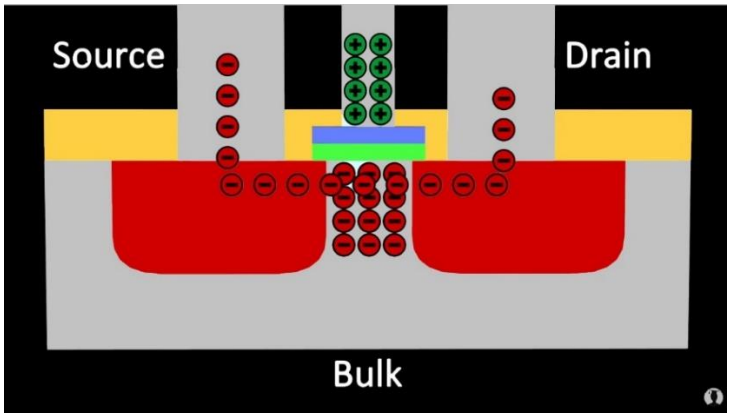


Figure 2.4 b)

2.2.2 The p-Channel MOSFET

Figure 2.5(a) shows a cross-sectional view of a *p*-channel enhancement-type MOSFET. The structure is similar to that of the NMOS device except that here the substrate is *n* type and the source and the drain regions are *p*+ type; that is, all semiconductor regions are reversed in polarity relative to their counterparts in the NMOS case. The PMOS and NMOS transistors are said to be *complementary* devices [2].

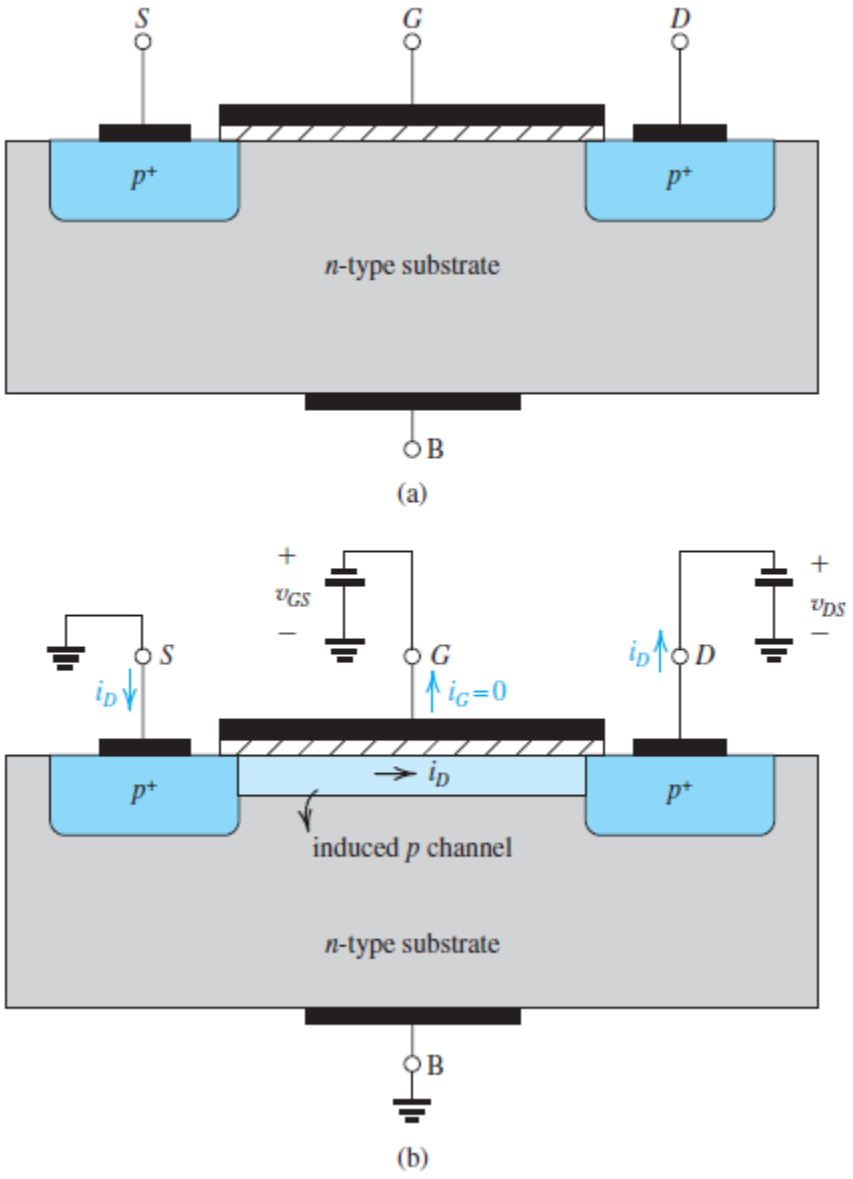


Figure 2. 5*(a)* ***Physical structure of the PMOS transistor. Note that it is similar to the NMOS transistor except that all semiconductor regions are reversed in polarity***

(b) ***A negative voltage V_{GS} of magnitude greater than $|V_{Tp}|$ induces a P channel, and a negative V_{DS} causes a current I_D to flow from source to drain.***

To induce a channel for current flow between source and drain, a negative voltage is applied to the gate, that is, between gate and source, as indicated in Fig. 2.5(b). By increasing the magnitude of the negative *Vgs* beyond the magnitude of the threshold voltage *Vtp*, which by convention is negative, a *p* channel is established as shown in Fig. 2.5(b). This condition can be described as $Vgs \leq Vtp$ or, to avoid dealing with negative signs, $|Vgs| \geq |Vtp|$

Now, to cause a current *iD* to flow in the *p* channel, a negative voltage *vDS* is applied to the drain.7 The current *iD* is carried by holes and flows through the channel from source to drain.

As we have done for the NMOS transistor, we define the process transconductance parameter for the PMOS device as

$$kp' = \mu pCox$$

where μp is the mobility of the holes in the induced *p* channel. Typically, $\mu p = 0.25\mu n$ *to* $0.5\mu n$ *and* is process-technology dependent. The transistor transconductance parameter *kp* is obtained by multiplying *kp'* by the aspect ratio *W*/*L*,

$$kp = kp'(W/L)$$

The remainder of the description of the physical operation of the *p*-channel MOSFET follows that for the NMOS device, except of course for the sign reversals of all voltages. PMOS technology originally dominated MOS integrated-circuit manufacturing, and the original microprocessors utilized PMOS transistors. As the technological difficulties of fabricating NMOS transistors were solved, NMOS completely supplanted PMOS. The main reason for this change is that electron mobility μn is higher by a factor of 2 to 4 than the hole mobility μp, resulting in NMOS transistors having greater gains and speeds of operation than PMOS devices. Subsequently, a technology was developed that permits the fabrication of both NMOS and PMOS transistors on the same chip. Appropriately called **complementary MOS**, or **CMOS**, this technology is currently the dominant electronics technology [2].

2.2.3 Complementary MOS or CMOS

As the name implies, complementary MOS technology employs MOS transistors of both polarities. Although CMOS circuits are somewhat more difficult to fabricate than NMOS, the availability of complementary devices makes possible many powerful circuit configurations. Indeed, at the present time CMOS is the most widely used of all the IC technologies. This statement applies to both analog and digital circuits. CMOS technology has virtually replaced designs based on NMOS transistors alone. Furthermore, by 2014 CMOS technology had taken over many applications that just a few years earlier were possible only with bipolar devices. Throughout this book, we will study many CMOS circuit techniques.

Figure 2.6 shows a cross section of a CMOS chip illustrating how the PMOS and NMOS transistors are fabricated. Observe that while the NMOS transistor is implemented directly in the *p*-type substrate, the PMOS transistor is fabricated in a specially created *n* region, known as an ***n* well**. [2] The two devices are isolated from each other by a thick region of oxide that functions as an insulator. Not shown on the diagram are the connections made to the *p*-type body and to the *n* well. The latter connection serves as the body terminal for the PMOS transistor.

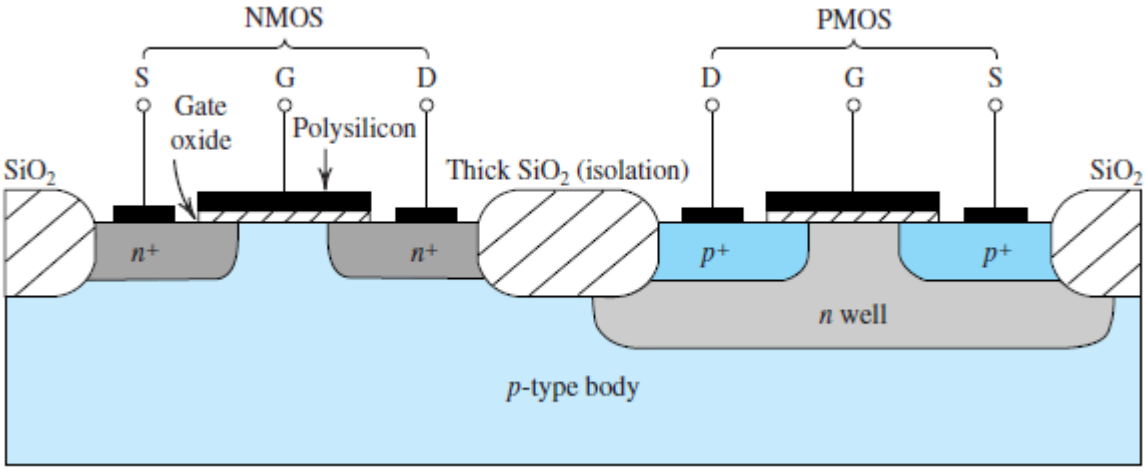


Figure 2. 6 Cross section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n*-type region, known as an *n* well. Another arrangement is also possible in which an *n*-type substrate(body) is used and the *n* device is formed in a *p* well. Not shown are the connections made to the *p*-type body and to the *n* well; the latter functions as the body terminal for the *p*-channel device.

2.3 Regions of inversion

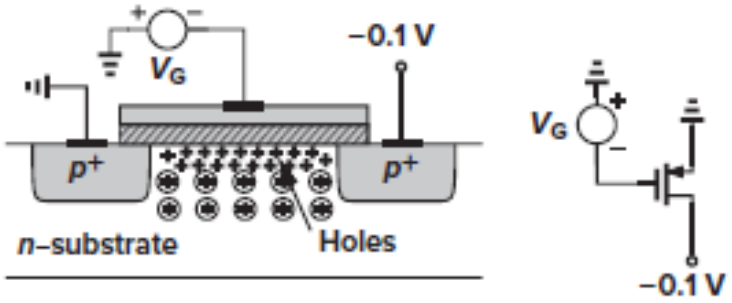


Figure 2. 7 Formation of inversion layer in a PFET.

As described in the previous section gate voltage is responsible of forming the inversion layer, or channel, under the gate oxide, whereas the value of drain voltage defines two regions of operation linear and saturation. Additionally, depending on the value of the gate-source voltage, the MOSFET has two distinct physical regions of operation: weak (WI) and strong (SI) inversion. Between them there is a transition region known as moderate inversion (MI)[3].
In weak inversion the channel is weakly inverted and drain diffusion current dominates. This occurs when the device is operating at sufficiently low effective gate-source voltage (VEFF=VGS-VTH≈-72mV) where the gate-source voltage is below the threshold voltage (sub-threshold region) by at least 72 mV. MOS weak inversion drain current in saturation is approximated by:

$$ID(WI,SAT) = 2n\mu Cox' UT^2 (W/L) e^{(VG-nVS-VTH/nUT)} \quad (2.1)$$

where, n (n ≈1.4) is the substrate factor, μ is the channel carrier mobility, COX' is the gate-oxide capacitance per unit area:

$$Cox' = eSiO2/Tox \quad (2.2)$$

and UT the thermal voltage:

$$U_T = kT/q \quad (2.3)$$

where εSiO2 = 3.45 · 10-11 F/m is the permittivity of silicon dioxide, q = 1.602 · 10-19 C is the magnitude of electron charge, Tox is the oxide thickness which is determined by the process technology used to fabricate the MOSFETs (Tox = 3.3 nm for 0.18 um CMOS technology), k = 1.3086 · 10-23 J/K is the Boltzmann's constant and UT = 25.8 mV at room temperature (T=300 K).

When the gate-source voltage exceeds the threshold voltage by at least 225 mV, the channel is strongly inverted and drift current dominates [3]. At this point the device is operating in strong inversion. Drain current for strong inversion and saturation is defined as:

$$ID(SI,SAT) = 1/2\mathrm{n}\,(\mu Cox')(W/L)(VG - nVS - VTH)^2 \quad (2.4)$$

For the two different regions of inversion, weak inversion (WI) and strong (SI) inversion, the drain-source saturation voltage, VD, SAT, can be calculated from the following equations:

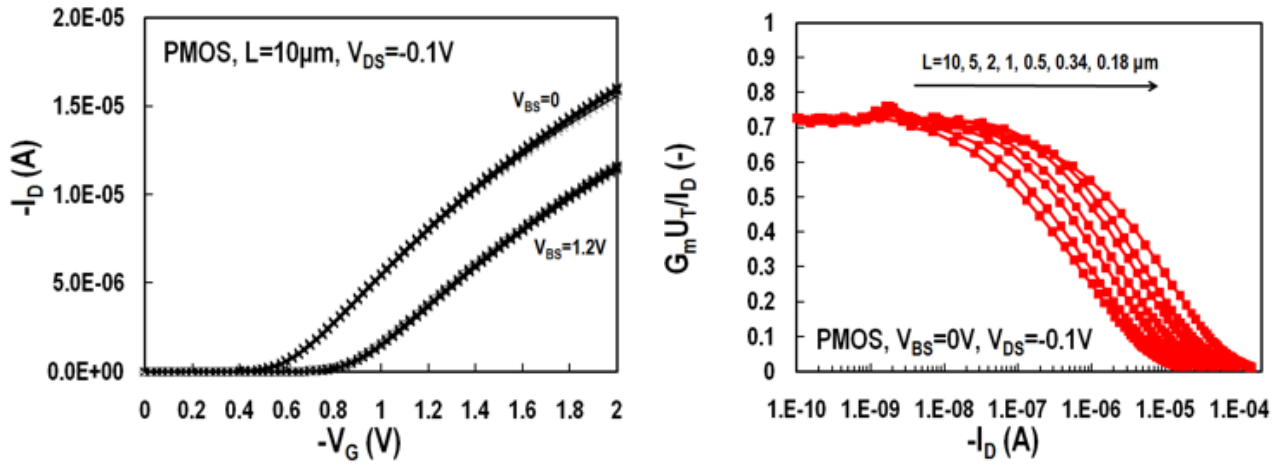
$V_{D,\,SAT}(WI) = 4U_T$ (2.5)

$V_{D,\,SAT}(SI) = V_G\text{-}nV_S\text{-}V_{TH}$ (2.6)

The drain current for both weak and strong inversion, in linear region of operation can be approximated from the following equation:

ID, LIN ≈ (µCOX') (WL) [VG-VTH-n 2(VD+VS)] ·(VD-VS) (2.7)

The typical I_D versus V_G plot of a MOS device, also called transfer characteristic along with G_mU_T/I_D versus I_D plot, are presented in Figure 2.8. In weak inversion I_D presents an exponential behavior.



a) b)

Figure 2. 8 a) I_D vs.V_G transfer and b) G_mU_T/I_D vs. I_D, of an PMOS transistor from weak to strong inversion.

2.4 Enclosed gate layout MOSFETS

2.4.1 Structure & Operation

Recently, layout techniques for the safe operation of microelectronic devices in radiation harsh environments, such as in space or nuclear applications, have been proposed utilizing new commercial sub-micron CMOS technologies

Ultra-thin gate oxides are naturally radiation hard, thanks to the modest net charge trapping and negligible threshold voltage shift even after high dose irradiation. Nevertheless, other failure mechanisms related to gate oxide damage could be activated, such as the increase of the low-field leakage across the oxide itself. On the other hand, thick oxides are still present in the isolation regions of CMOS components and can be quite sensitive to radiation damage. In fact, due to positive charge trapping, ionizing radiation may induce the formation of an inversion layer at the bird's beak or shallow trench corner or underneath the field oxide around NMOS, giving rise to various leakage current paths

MOSFETs with gate-enclosed layouts (GE-MOSFET) are used in traditional rich environments, radiation rich environments, as they can effectively survive such failure mechanisms as the increase of drain-to-source leakage current due to turn-on of parasitic transistors. The main drawbacks of these devices are represented by slow switching times, due to a larger input capacitance than in standard layouts, and large area consumption. These defects can be partially compensated by using aggressive CMOS technologies, such as quarter- and sub-quarter-micron technologies.

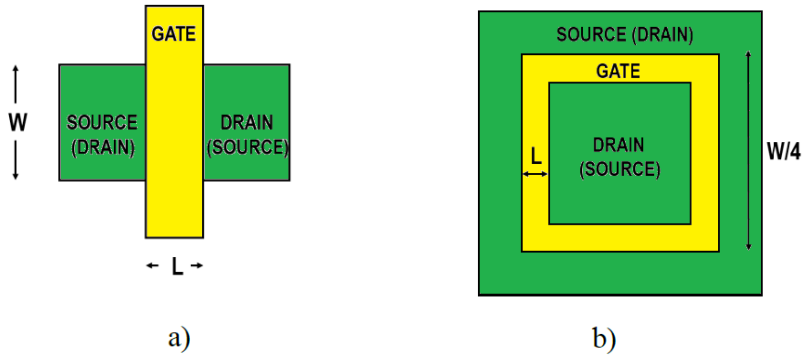


Figure 2. 9 a) Planar view of a standard MOSFET and b) an enclosed gate MOSFET.

In MOSFETs with enclosed gate layout the drain (or source) diffusion is fully surrounded by the gate polysilicon and the source (or drain) diffusion. The choice of the inner electrode as drain or source is defined by the bias voltage although as reported at [4] and [5] with the selection of the outer electrode as the drain, a device with an annular structure will exhibit lower drain electric fields and better reliability than a conventional one. On the other hand, if the inner electrode is selected as the drain, the substrate contact will be closer to the source and the drain resistance will be reduced resulting to higher output conductance [4]. In Figure 2.10 a cross section of an enclosed gate n-type MOSFET is depicted [6].

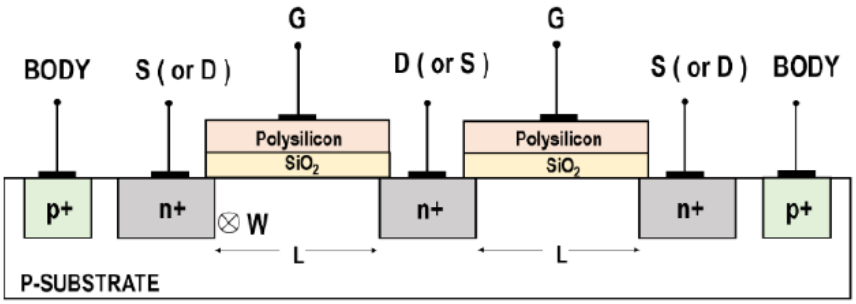


Figure 2. 10 Cross section of an enclosed gate NMOSFET with a p+ diffusion bulk connection.

GE-MOSFETs were already proposed for logic applications 20 years ago. At that time, no analysis of the electrical characteristics of these devices was supplied. Nowadays, treatments of this problem can be found for particular shapes: circular, square or hexagonal.

2.4.2 GE-Transistor shapes

The standard MOSFET layout consists of a source and a drain separated by a channel of width W and length L. The GE-MOSFET (or annular MOSFET) is a transistor with the drain (or source) diffusion in the middle, encircled by the channel and the source (or drain) diffusion. Placing the drain in the middle brings the substrate contact closer to the source and reduces the drain resistance. As a consequence, this configuration gives a higher output conductance.

When comparing the standard and GE transistors, different potential distributions can be observed along the transistor channel. In a circular NMOS when a drain voltage +VDS is applied, the 1/r dependence leads to a higher electric field close to the inner drain diffusion. In the GE shape narrow gate effects, typically due to the fringing electrical field that causes a sideways spreading of the depletion region, are not present.

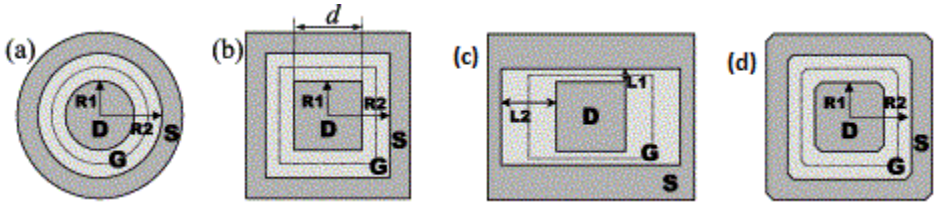


Figure 2. 11. Gate-enclosed transistor shapes: (a) circular, (b) square, (c) rectangular with stressed edges, and (d) square with the corner cut at 45° (broken corners). Drain (D), gate (G) and source (S) are indicated, as well as the gate-channel dimension [4].

In conventional MOSFETs, techniques like STI (Shallow Trench Isolation) and LOCOS (Local Oxidation of Silicon) are used in order to provide better isolation between different devices and define the active silicon area. In radiation environments, due to positive charge trapping at the edges of STI corners, or Bird's Beak region [8], an induced inversion layer will give rise to a transistor leakage current path from drain to source. Enclosed gate MOSFETs without STI along with guard rings, can eliminate the edge leakage and prevent leakage current between components. This can be realized because any current between source and drain has to flow underneath the gate oxide and there is no possible current path along the edge of the active area [7]. Additionally, RTS noise which is related to trapping sites within the gate oxide-silicon interface due to structural defects, can be affected by the presence of shallow trench isolation. During the STI process, the device can be damaged at the STI boundary resulting to the generation of extra traps at the edge of the channel under the gate region. As the device dimensions scales down the ratio of device gate edge to area increases and the STI edge effect dominates the overall RTS performance [9]. Since low frequency noise is strongly related to RTS noise, devices without STI, like enclosed gate transistors, are expected to exhibit greatly improved 1/f noise characteristics like lower drain current PSDs and lower relative current variations ($\Delta I_D/I_D$) [10].

2.5 Modeling the W/L ratio

2.5.1 Modeling the W/L ratio in enclosed gate MOSFETs

Considering the GE-MOSFETs, the initial problem is the definition of the aspect ratio W/L, which is not as trivial as in standard devices. In the first intuitive approach, the minimum gate length is L. The definition of the width W is less straightforward. For instance, W can be taken as the length of the curve lying at mid-channel, named hereafter as mid-channel width ($W_{1/2}$). Alternatively, W could be chosen as the drain or source diffusion perimeter. Posteriori, these last definitions appear however, unsatisfactory upon a comparison with experimental measurements, and will not be considered in this communication [4,11].

The extraction of the experimental (or simulated) W/L values comes from the comparison of the I_D -V_{GS} characteristics between a GE and a standard device with the same L. Assuming the SPICE level 1 model, W/L can be extracted from the ratio of transconductances g_m as follows:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \left(\frac{W}{L}\right)_{eff} \mu C_{ox} V_{DS}(1 + \lambda V_{DS}), \qquad (1)$$

$$\left(\frac{W}{L}\right)_{eff}^{enc} = \left(\frac{W}{L}\right)_{eff}^{std} \frac{g_m^{enc}}{g_m^{std}}, \qquad (2)$$

where superscript ‘enc’ and ‘std’ refer to the GE and standard geometries, respectively. As the effective aspect ratio of the standard transistor is known, the aspect ratio of the GE transistor can be determined. In this procedure, we assumed that the GE and standard transistors have the same electrical properties μC_{ox} and λ. Even in the case of different λ values, the effect of such a difference on the aspect ratio values has been minimized by always operating the transistor at a low drain voltage V_{DS} = 50 mV. In this way, our description of the GE-MOSFET is congruent with SPICE level 1 approximations. Even in the short channel devices, where SPICE level 1 fails, the aspect ratio of GE-MOSFETs can be extracted from the comparison with standard transistors. In this case, we must assume the same functional dependence of I_D on the drain and gate voltages for both standard and GE devices [4,11].

In the long channel model, the ID expression is calculated by integrating the resistance of the infinitesimal element along the channel in the hypothesis of current continuity (no generation or recombination inside the channel)

$$\int_{channel} I_D \, dR = \int_{channel} dV. \qquad (3)$$

In GE transistors, integration has to take into account the non-standard gate geometry. In first order approximation, we assume that W/L is the single parameter depending on the device geometry.

2.5.2 Circular MOSFET

The model for a circular MOSFET can be easily developed starting from the basic long channel equations in cylindrical coordinates. In this device, the electric field is circularly symmetric:

$$E_r(r,\theta) = E_r(r) = \frac{dV}{dr} = \frac{V_D - V_S}{\ln(R_2/R_1)}\frac{1}{r}. \qquad (4)$$

Hence, the carrier drift velocity $V_D = \mu E$ depends only on the radial position r and not on θ, as well as the charge density of the free carriers in the MOS inversion layer Q'i.

Starting with the integration of Eq. (3), the expression of the current through the cylindrical ring with radii r and r+ dr and height z is reported in the first part of Eq. (5). The vertical gate-to-channel coordinate z does not appear, as μ is taken as a constant and Q'i (V) is obtained after integration in z. The second step is the integration along the whole channel, between the source and drain radii R2 and R1 (Fig. 2.11).

$$I_D = 2\pi r\mu\frac{dV}{dr}|Q_i'(V)| \rightarrow \int_{R_1}^{R_2}\frac{I_D\,dr}{2\pi r\mu}$$
$$= \int_{V_S}^{V_D}|Q_i'(V)|dV, \qquad (5)$$

$$I_D = \frac{2\pi}{\ln(R_2/R_1)}\mu\int_{V_S}^{V_D}|Q_i'(V)|dV. \qquad (6)$$

The integration gives an aspect ratio equal to 2π/ln(R2/R1). In standard gate geometry, this integration step leads to the SPICE level 1-3 models.

The same result is also obtained if l is considered dependent on z. For instance, assuming a relation for μ with dependence also on the charge density of the fixed ionized ions Q'B, the integration of the left-hand side of Eq. (5) leads to Eq. (7) after a change of variable according to Eq. (4). In Eq. (7), the quantity in square brackets is the effective mobility [4].

$$I_D = \frac{2\pi}{\ln(R_2/R_1)}\left[\int_{V_S}^{V_D}\frac{dV}{\mu(Q_i,Q_B)(V_D - V_S)}\right]^{-1}$$
$$\times\int_{V_S}^{V_D}|Q_i'(V)|dV. \qquad (7)$$

The aspect ratio obtained from Eq. (6) can be rewritten by using the results relative to the mid-channel approximation previously introduced, where L=R2-R1

and $W_{1/2} = \pi(R1+R2)$:

$$\left(\frac{W}{L}\right)_{eff}^{circ} = \frac{2\pi}{\ln(R_2/R_1)}$$
$$= \left[\left(\frac{1}{2}+\frac{R_1}{L}\right)\ln\left(1+\frac{L}{R_1}\right)\right]^{-1}\frac{W_{1/2}}{L}. \qquad (8)$$

If the drain radius is greater than the gate length, i.e., L << R1, the mid-channel approximation is satisfactory. Instead, for the long channel devices, the mid-channel calculation overestimates the effective aspect ratio. This result is well illustrated in Fig. 2.12, which compares numerical simulations, experimental measurements, and results from our model and the mid-channel approximation, for different circular NMOS devices in the 2.5-µm technology. A good agreement is always found between the experimental (or numerically simulated) W values and the results of our model.

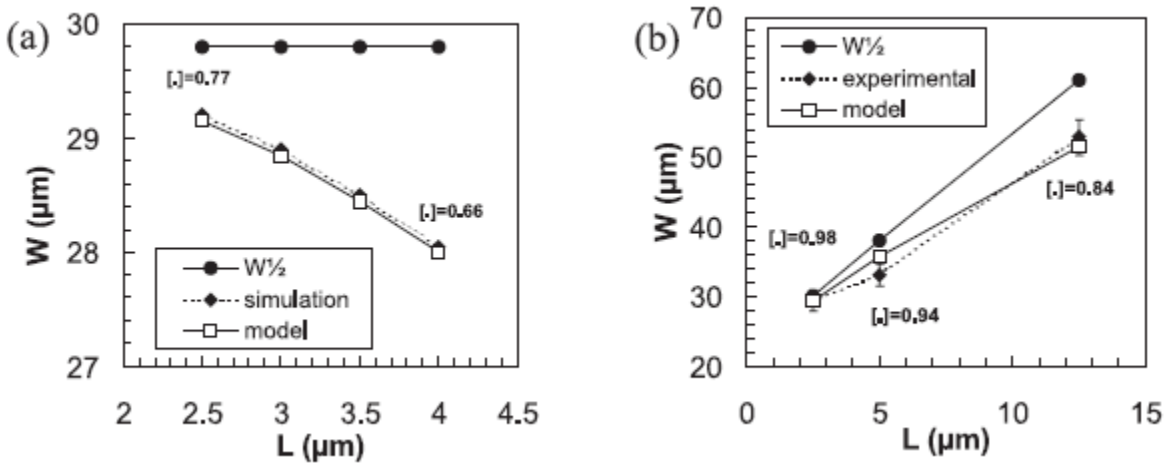


Figure 2. 12 Effective W in circular transistors for different L from mid-channel approximation (W1/2), our model and (a) numerical simulations or (b) experimental data. In figure, [.] is the quantity in square bracket in Eq. (8). Simulations and experimental data are referring to transistors with different drain sizes d.

3.MOSFET electrical characteristics

In this chapter, we are going to study MOSFET characteristics that were not mentioned in the "Device Structure & Physical Operation" chapter and are going to be examined in the experimental process.

3.1 Transconductance

Transconductance (for transfer conductance), also infrequently called mutual conductance, is the electrical characteristic relating the current through the output of a device to the voltage across the input of a device. Conductance is the reciprocal of resistance [12].

Since a MOSFET operating in saturation produces a current in response to its gate-source overdrive voltage, we may define a figure of merit that indicates how well a device converts a voltage to a current. More specifically, since in processing signals, we deal with the *changes* in voltages and currents, we define the figure of merit as the change in the drain current divided by the change in the gate-source voltage [1]. Called the “transconductance” (and usually defined in the saturation region) and denoted by *gm*, this quantity is expressed as

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VDS\ const.} \qquad (2.17)$$

$$= \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) \qquad (2.18)$$

In a sense, gm represents the sensitivity of the device: for a high gm, a small change in VGS results in a large change in ID. We express gm in 1/_ or in siemens (S); e.g., gm = 1/ (100 _) = 0.01 S. In analog design, we sometimes say a MOSFET operates as a “transconductor” or a “V/I converter” to indicate that it converts a voltage change to a current change. Interestingly, gm in the saturation region is equal to the inverse of Ron in the deep triode region.
The reader can prove that gm can also be expressed as

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \qquad (2.19)$$

$$= \frac{2I_D}{V_{GS} - V_{TH}} \qquad (2.20)$$

Plotted in Fig. 3.1, each of the above expressions proves useful in studying the behavior of gm as a function of one parameter while other parameters remain constant. For example, (2.18) suggests that gm increases with the overdrive if W/L is constant, whereas (2.20) implies that gm decreases with the overdrive if I_D is constant.
The I_D and $V_{GS} - V_{TH}$ terms in the above gm equations are bias values. For example, a transistor with W/L = 5 µm/0.1 µm and biased at I_D = 0.5 mA may exhibit a transconductance of (1/200 _). If a signal is applied to the device, then I_D and $V_{GS} - V_{TH}$ and hence gm varies, but in small-signal analysis, we assume that the signal amplitude is small enough that this variation is negligible.

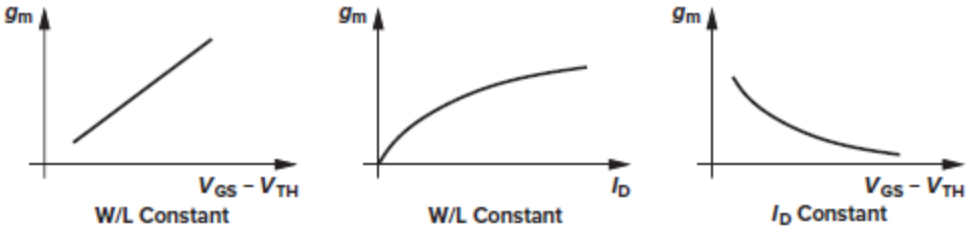


Figure 3. 1 Approximate MOS transconductance as a function of overdrive and drain current.

3.2 Mobility

In solid-state physics, the electron mobility characterizes how quickly an electron can move through a metal or semiconductor, when pulled by an electric field. There is an analogous quantity for holes, called hole mobility. The term carrier mobility refers in general to both electron and hole mobility [12].

Electron and hole mobility are special cases of electrical mobility of charged particles in a fluid under an applied electric field.

When an electric field *E* is applied across a piece of material, the electrons respond by moving with an average drift velocity, u_d. Then the electron mobility μ is defined as: $u_d=\mu E$

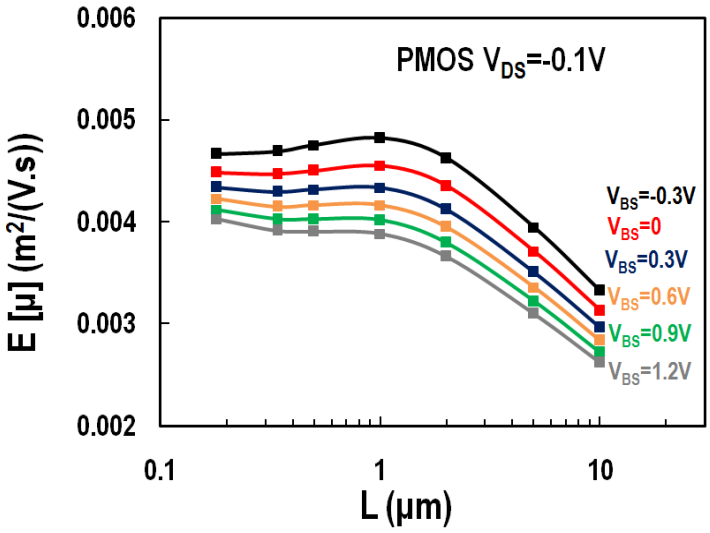


Figure 3. 2 Example of μ vs L graph

3.3 Matching-Mismatching

3.3.1 Matching

MOS transistor matching is an important design parameter in many CMOS applications. MOS transistor matching in analog CMOS applications deals with statistical device differences between pairs of identically designed and identically used transistors [14].

3.3.2 Threshold matching

The difference ΔVT between the threshold voltages of a pair of MOS transistors (mismatch) is usually described by its standard deviation [14]:

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}} = \frac{qt_{ox}\sqrt{2Nt_{depl}}}{\epsilon_0 \epsilon_{ox}\sqrt{WL}} \qquad (1)$$

This description is based on the assumptions that mismatch is caused by independent random disturbances of physical properties and that the correlation distance of the statistical disturbance is small compared to the active device area. These assumptions lead to a proportionality of the standard deviation with the inverse square root of the area, see Figure 3.3. The most important contribution to the proportionality constant AVT is the uncertainty in the number of active doping atoms in the depletion layer (N). The statistical variation in N = (N_a + N_d) determines the matching (while control of the net value (N_a - N_d) determines the threshold voltage V_T). As indicated in formula 1, the matching coefficient for different processes reduces with decreasing gate oxide thickness (t_{ox}). Examples of other statistical disturbances that contribute to MOS matching are: dimensional variations, interface states, etc.

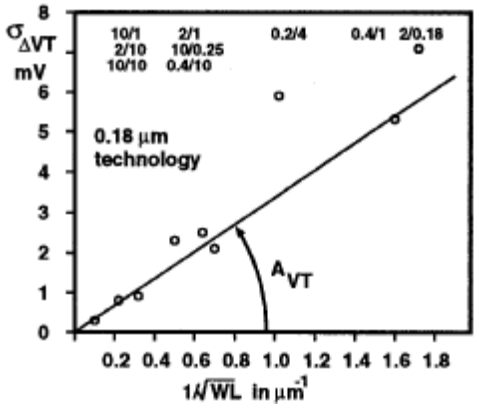


Figure 3. 3 The standard deviation of the NMOST threshold versus the inverse square root of the area, for a 0.18 µm (3.3-nm gate oxide) process.

Optimum circuit performance can only be achieved when the matched circuit elements are designed identical with respect to geometry, rotation, biasing and temperature. Moreover, various environmental effects play a role for matching: distance, topography (resist crowding), metal coverage implantation striping, packaging and mechanical strain.

8 standards for best matching	
1. structure	**5. temperature**
2.geometry	**6.proximity**
3.environment	**7.orientation**
4. non-minimum geometry	**8.symmetrical center**

Matching values for 0.35µm,0.18µm CMOS technologies

0.35µm CMOS			NMOS			PMOS	
Parameter	Symbol	Unit	3.3V	5V		3.3V	5V
Oxide capacitance	C'_{ox}	F/m^2	4.5m	2.3m		4.5m	2.3m
Threshold voltage mismatch	A_{VT}	mV.µm	10	17		15	18
Current factor mismatch	A_{BETA}	%.µm	2	2.4		2.5	2.2

0.18µm CMOS			NMOS			PMOS	
Parameter	Symbol	Unit	1.8V	3.3V	native	1.8V	3.3V
Oxide capacitance	C'_{ox}	F/m^2	8.5m	5m	8.5m	8.5m	5m
Threshold voltage mismatch	A_{VT}	mV.µm	5	9	5	5.5	6.4
Current factor mismatch	A_{BETA}	%.µm	1	0.72	0.18	1.2	0.64

3.3.3 Mismatching

Two identical designed devices on an integrated circuit have random differences in their behavior and show a certain level of random mismatch in the parameters which model their behavior. This mismatch is due to the stochastic nature of physical processes that are used to fabricate the device [16].

Mismatch is the process that causes time-independent random variations in physical quantities of identically designed devices.

Other techniques can be used to calculate the VT0 matching and β matching. In the transistors are measured in the linear region and for each individual transistor the threshold voltage VT0 and the current factor β, are extracted using classical parameter extraction algorithms. The parameter mismatch is then calculated by subtracting the parameters of the individual transistors. Also, a direct extraction technique can be derived from a more complex drain current model which includes a mobility reduction parameter θ. The extra mismatch parameter Δθ is however highly correlated to the (Δβ/β) and the overall modeling of the current mismatch becomes more complicated without improvements in accuracy [16].

3.4 Slope Factor

One important parameter for the characterization of MOS transistors is the slope factor. The “ideal” slope factor is equal to one [13]. The slope can be derived by the following rule:

$$n \equiv \left[\frac{\partial \Psi_{SP}}{\partial V_G}\right]^{-1} = 1 + \frac{\gamma}{2\sqrt{\Psi_{SP}}} \cong 1 + \frac{\gamma}{2\sqrt{\Psi_0 + V_P}}$$

The following graph shows an example of the behavior of the slope factor for different V_{BS} and channel length.

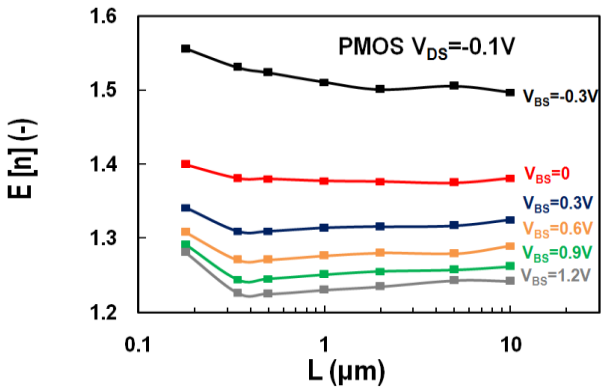


Figure 3. 4 n vs L example for various V_{BS}

4. Experimental process

In the experimental process, we used the following tools:

- Silicon Wafer
- Cascade Microtech Probe Station
- HP4142B DC Analyzer
- GPIB-USB interface
- Agilent ICCAP
- Microsoft Office Excel 2013
-

data was gathered from a total of 672 circular PMOS transistors. For each of the 48 dies measured on the wafer, there were seven pairs of PMOS Circular transistors (10um, 5um, 2um, 1um, 0.5um, 0.34um and 0.18um pairs).

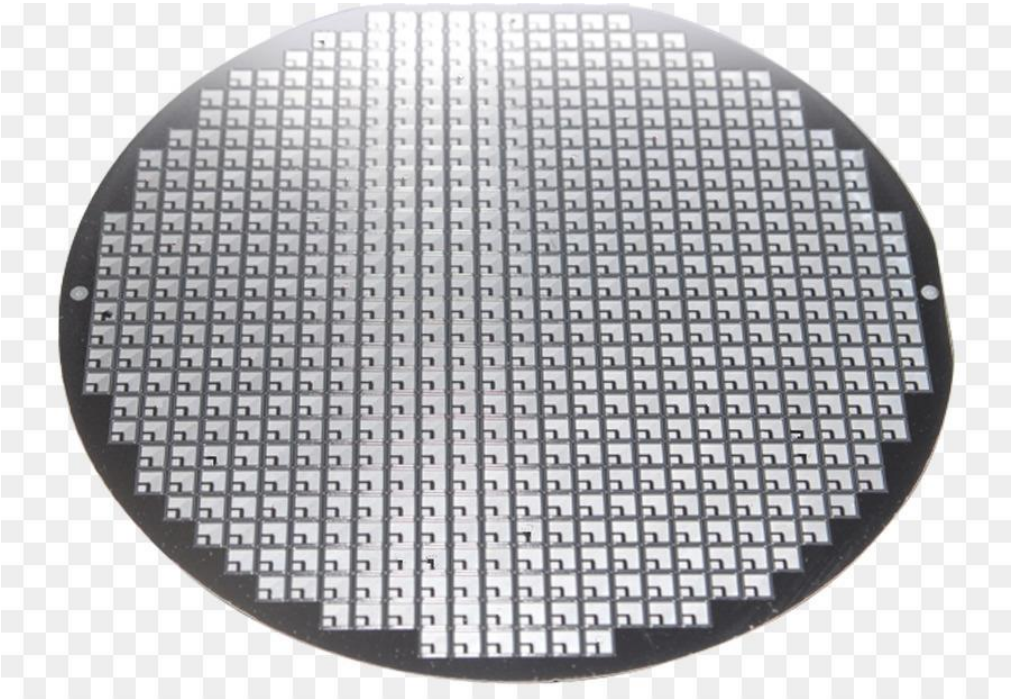


Figure 4. 1waffle-die semiconductor wafer

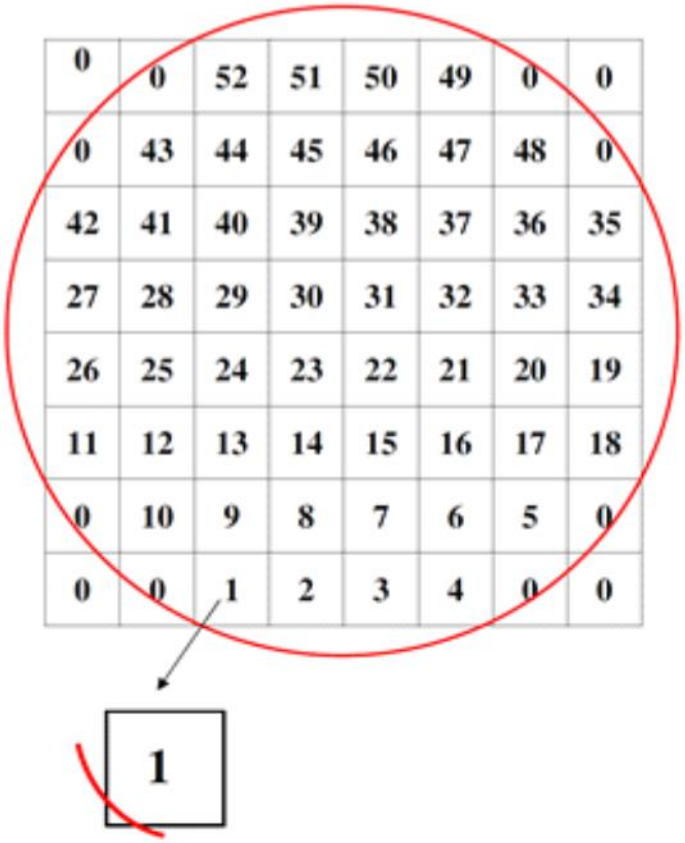
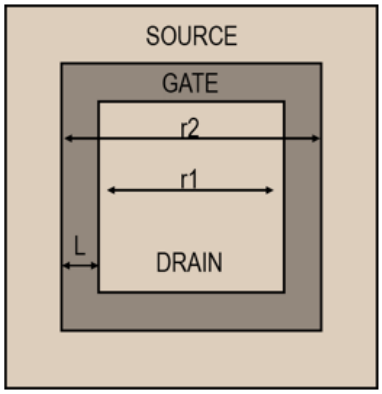


Figure 4. 2 Representation of the silicon wafer's dies

Figure 4. 3 The MOSFETs included in each die ("SPECIAL" MOSFETS were not included in the experimental process)



W(L)=8*L / ln(r2/r1)
r2=1.4um + (2*L)
r1=1.4um

L(um)	W(um)
10	29.33714
5	19.07359
2	11.8525
1	9.016084
0.5	7.421198
0.34	6.870497
0.18	6.292563

Figure 4. 4 W and L and their dependence, for every type of the measured transistors

4.1 Measurements for V_{DS}= -0.1 V (linear)

In this part of the thesis we will see the graphic representation of the MOSFET characteristics, while the drain-source voltage equals -0.1V.

4.1.1 Measured I/V characteristics

In this section the measured I_D vs. V_G plots will be presented. The |ID| for every gate voltage value, represents the mean value of the measured drain current ($|I_D|$), on a number of 96 P MOSFETs on the same gate voltage. The unitless quantity G_mU_T/I_D is also calculated from the average Gm value that was extracted from measurements.

Measurements – V_{DS}=0.1V (Lin axis)

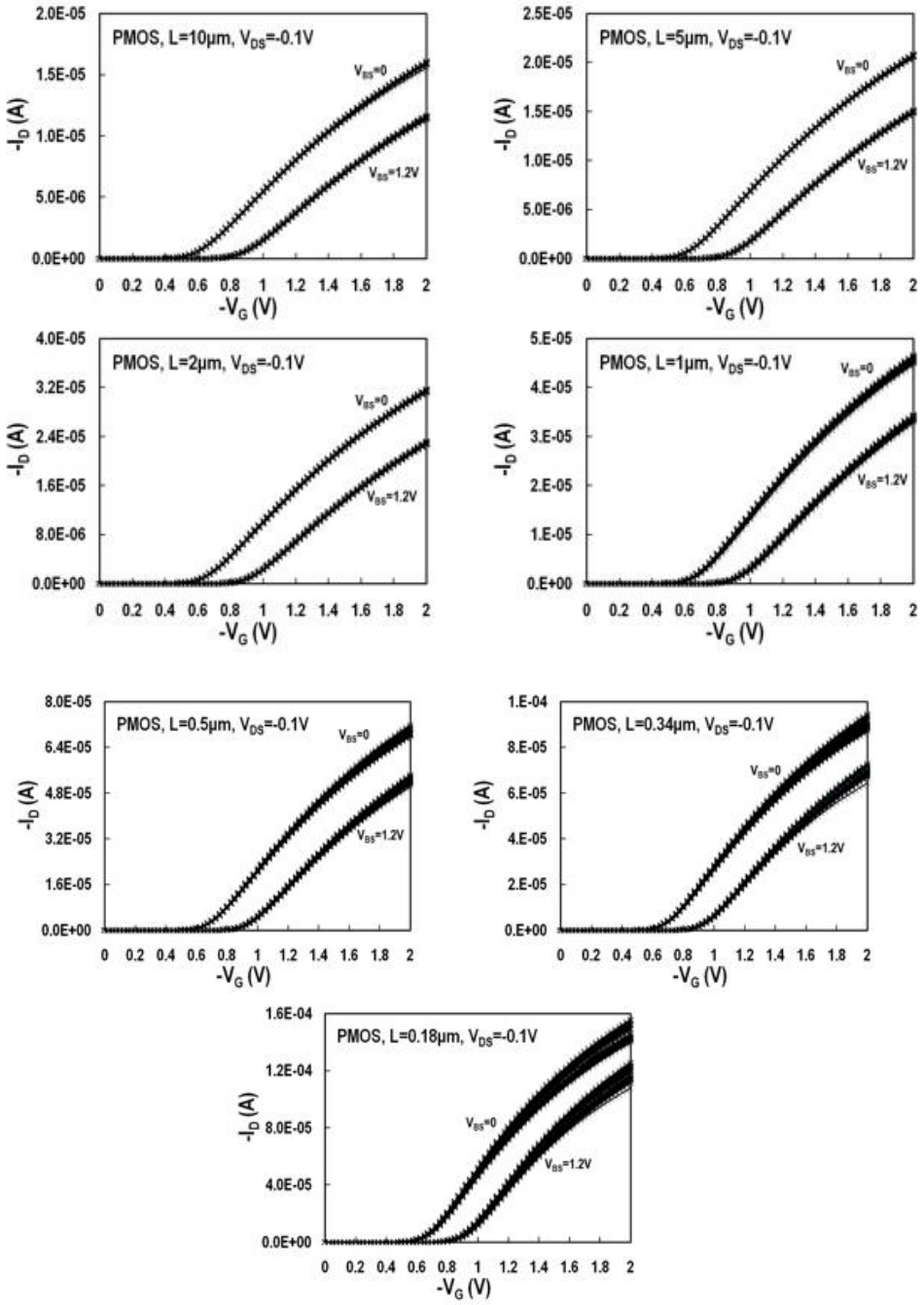


Figure 4. 5 The I_D vs VG graphs for V_{BS}=0, 1.2 V. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um)

In the figure above we see that I_D increases when we increase the gate Voltage (as expected). Also, I_D is higher for V_{BS} = 0V than it is for V_{BS} = 1.2V. This behavior is normal and similar to standard transistors.

Measurements – V_{DS}= -0.1V (Log axis)

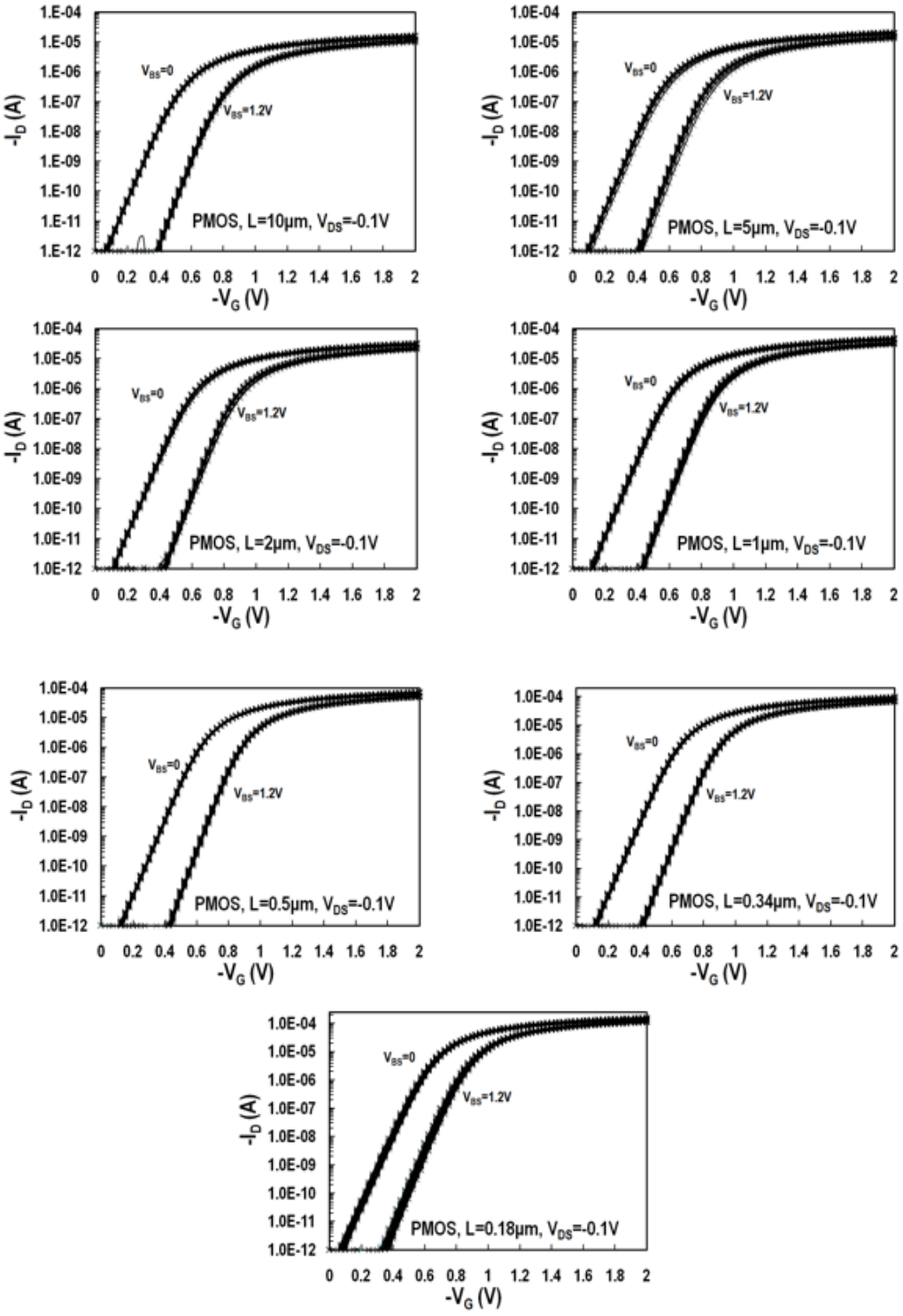


Figure 4. 6 The I_D vs V_G graphs for V_{BS}=0, 1.2 V in a logarithmic axis. Each graph shows the results for different channel lengths (L=10um5um, 5um, 2um, 1um 0., 0.34um and 0.18um)

g_m (V_{DS}=-0.1V) – Mean Value

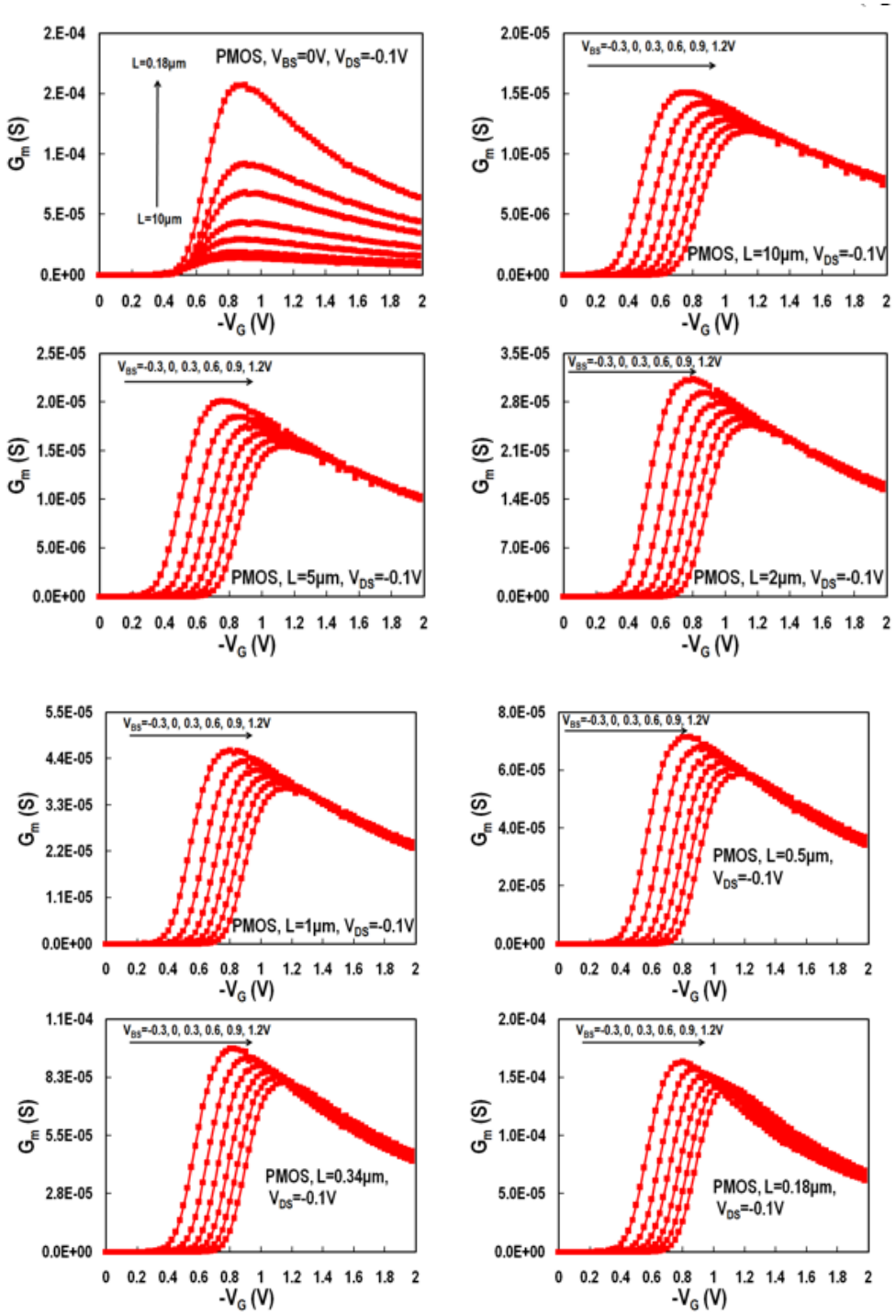


Figure 4. 7 G_m vs V_g graphs for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V are presented. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um) except for the top left graph which presents the result of all the different channel lengths when V_{BS} equals 0.

In the graphs above, we can clearly see that as the channel length gets smaller, the transconductance increases. Another observation is that G_m's peak decreases with higher V_{BS}. This is the expected result which is similar to the result of the standard version of these transistors.

g_mU_T/I_D (V_{DS}=-0.1V) – Mean Value

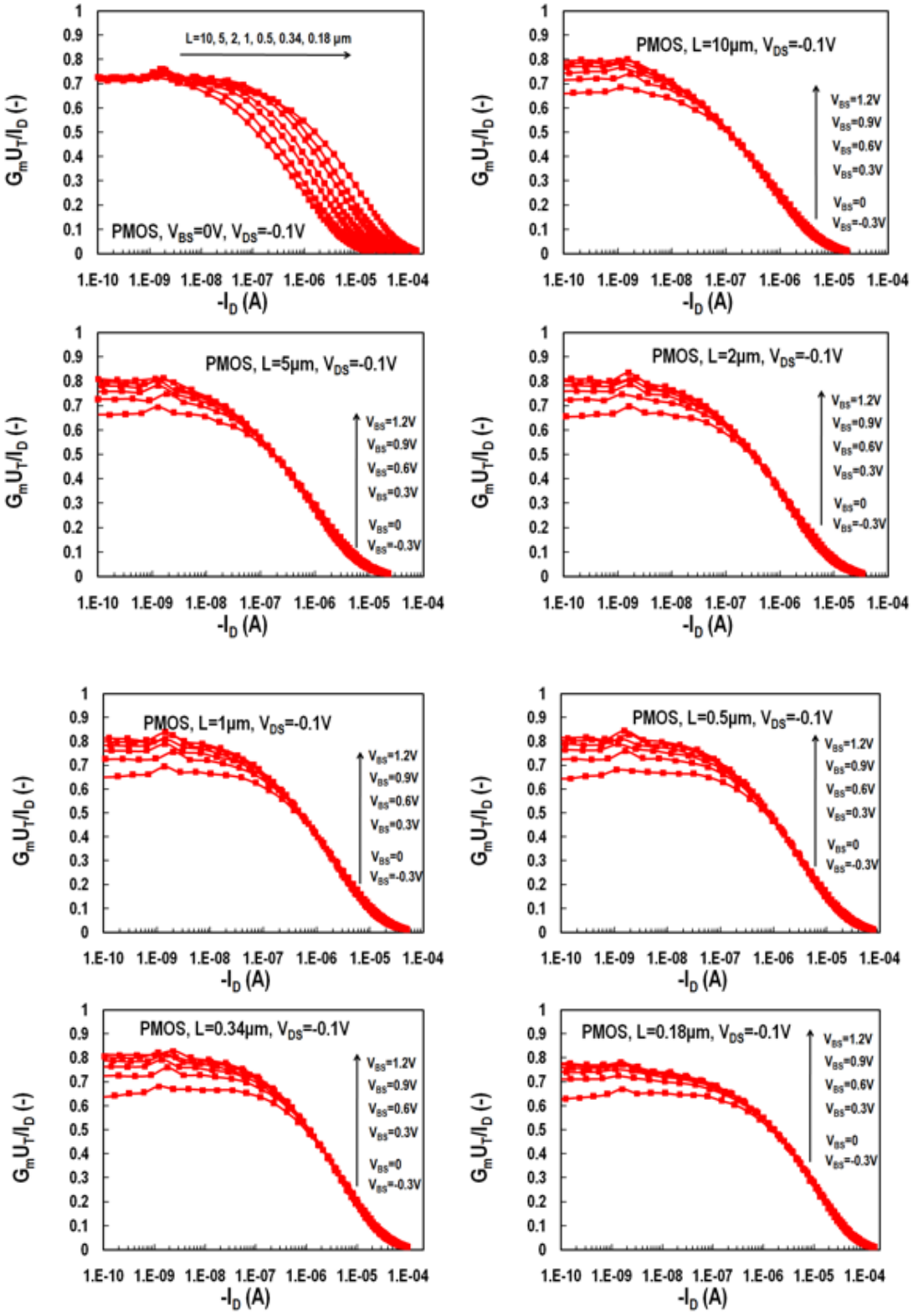


Figure 4. 8 The G_mU_T/I_D graphs for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V are presented. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um) except for the top left graph which presents the results of all the different channel lengths for V_{BS} = 0.

The unitless quantity G_mU_T/I_D is clearly higher for lower current I_D. It also appears to be higher for higher V_{BS}.

4.1.2 Threshold Voltage

In this section the threshold voltage graphs will be presented. The mean value of the threshold voltage, the threshold voltage in specific cases and its standard deviation will be the subject of this chapter.

V_{TH} – Mean Value, Sigma (V_{DS}=-0.1V)

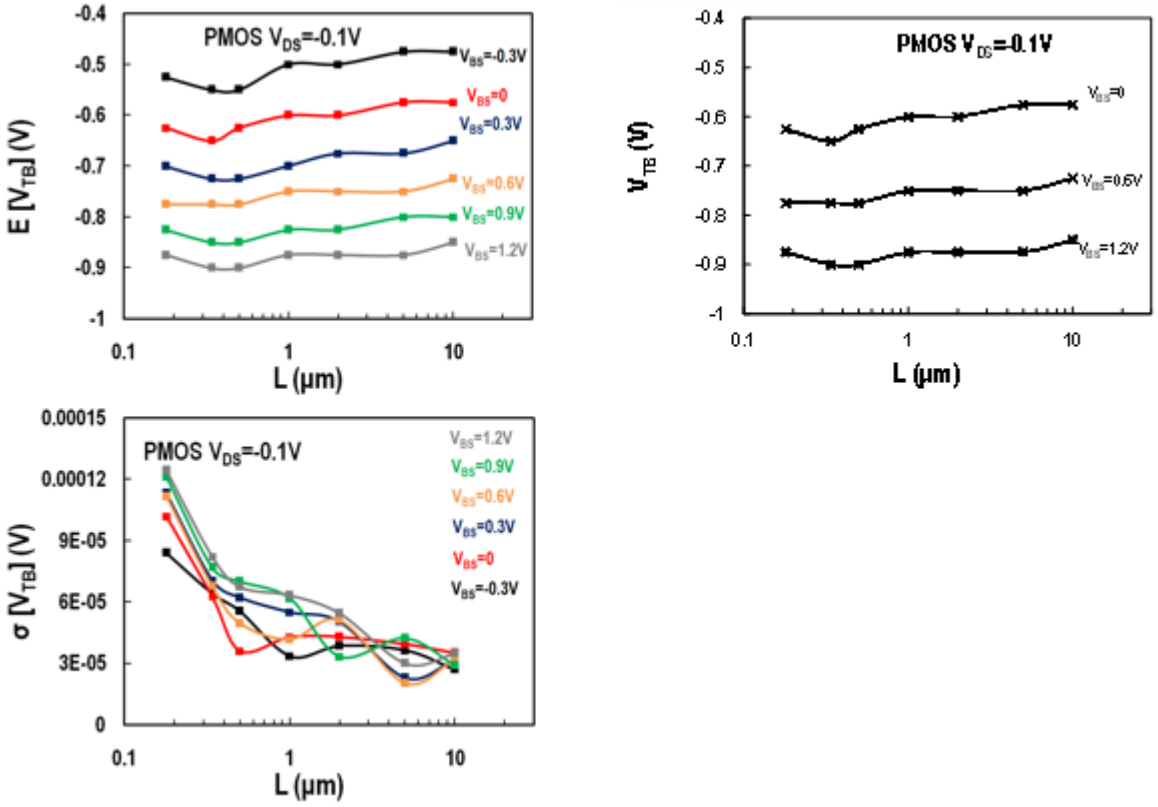


Figure 4. 9 (upper left) The E[V_{TB}] vs L graph for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2 V is presented above.

(upper right) V_{TB} vs L graph is presented. V_{DS} is -0.1 Volts and V_{BS} = 0, 0.6, 1.2

(lower left) σ[V_{TB}] vs L graph is presented for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V

E[V_{TB}] slightly increases as the channel length L increases. When V_{BS}= -0.3 V and L=10um we see the peak of the E[V_{TB}]. On the other hand, we notice the lowest value when V_{BS}= 1,2 V and L=340 nm. When L=340nm we can see the lowest values of E[V_{TB}] for any V_{BS} value.

The standard deviation of V_{TB} is significantly bigger for 180nm. While the channel length gets bigger, the V_{TB} standard deviation gets smaller. Another conclusion made after examining the graph above, is that σ[V_{TB}] is higher for higher V_{BS}.

4.1.3 Threshold Voltage Matching

The Threshold Voltage matching will be examined in this chapter. Results from 48 pairs of PMOS transistors for each channel length, will be presented in the graphs below.

ΔV_{TH} – Matching (V_{DS}=-0.1V)

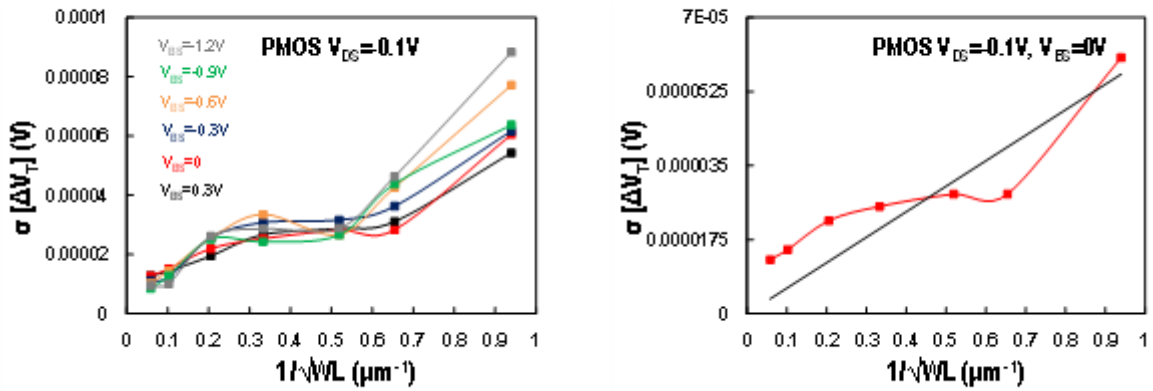


Figure 4. 10The σ[ΔV_T] vs 1/ $\sqrt{WL}$ graph for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V is presented in a). In b) we examine V_{BS} =0 exclusively.

Examining the figure above we can conclude that σ[ΔV_T] increases with 1/ $\sqrt{WL}$. This makes sense because as the product of the width and the length decreases, the unitless quantity 1/ $\sqrt{WL}$ increases and for smaller dimensions where the distance between the different semiconductors is smaller, we expect increased deviation between the measurements.

4.1.4 Mobility

The mean value of the mobility for every channel length, the mobility for specific V_{BS} and its standard deviation will be our focus in this subchapter. Representative graphs and their results will be presented below.

μ – Mean Value, Sigma (V_{DS}=-0.1V)

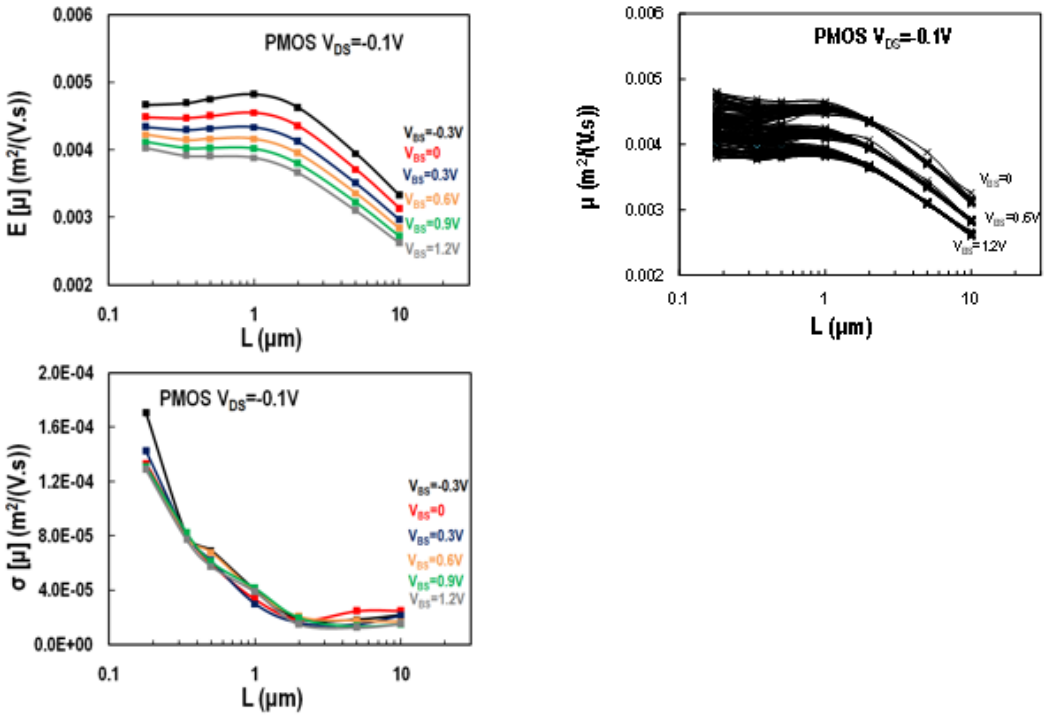


Figure 4. 11 (upper left) E[μ] vs L graph for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V

(upper right) μ vs L graph for V_{BS} = 0, 0.6, 1.2V

(lower left) σ[μ] vs L graph for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V

- The mean value of the mobility decreases with bigger channel length and higher V_{BS} following typical behavior.
- Mobility decreases for bigger channel length. It also decreases for higher V_{BS}. Furthermore, mobility becomes bigger for smaller channel length devices, following typical behavior.
- The standard deviation of μ, is higher for smaller channel lengths. This is something we expect since, as we already know, the electron mobility is inversely proportional to the channel length.

4.1.5 Slope Factor

In this part of the thesis we are going to focus on the slope factor and its behavior for transistors with different channel length and for different base-source voltages in each of them.

n – Mean Value, Sigma (V_{DS}=-0.1V)

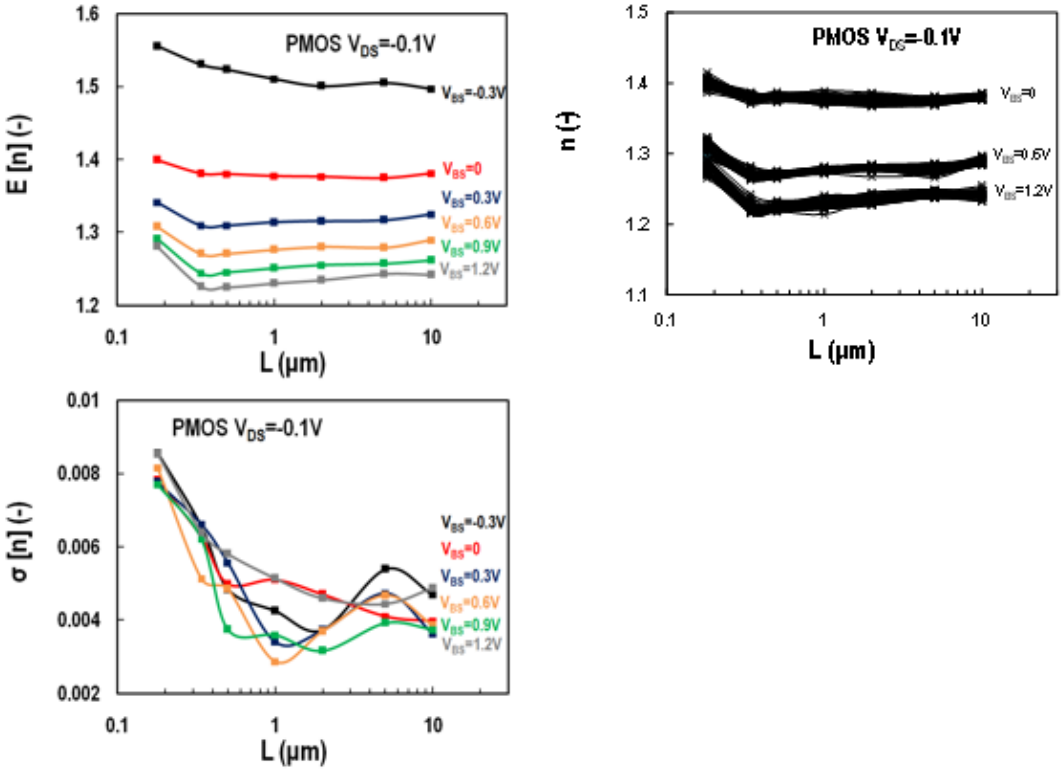


Figure 4. 12 (upper left) E[n] vs L graph for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V

(upper right) n vs L graph for V_{BS} = 0, 0.6, 1.2V

(lower left) σ vs L graph for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V

- In the figure above we can examine the mean value of the slope factor. As we can see, it increases with lower V_{BS}.
- The graph above presents how the slope factor behaves for V_{BS}=0, 0.6, 1.2V. The slope factor decreases with higher V_{BS}. Furthermore, slope factor versus channel length is almost constant with a slight increment towards smaller channel lengths as expected.
- Standard deviation of n, increases with lower V_{BS}. Similar results are extracted from respective standard transistors.

$\sigma(\Delta I_D/I_D)$ – Matching (V_{DS}=-0.1V)

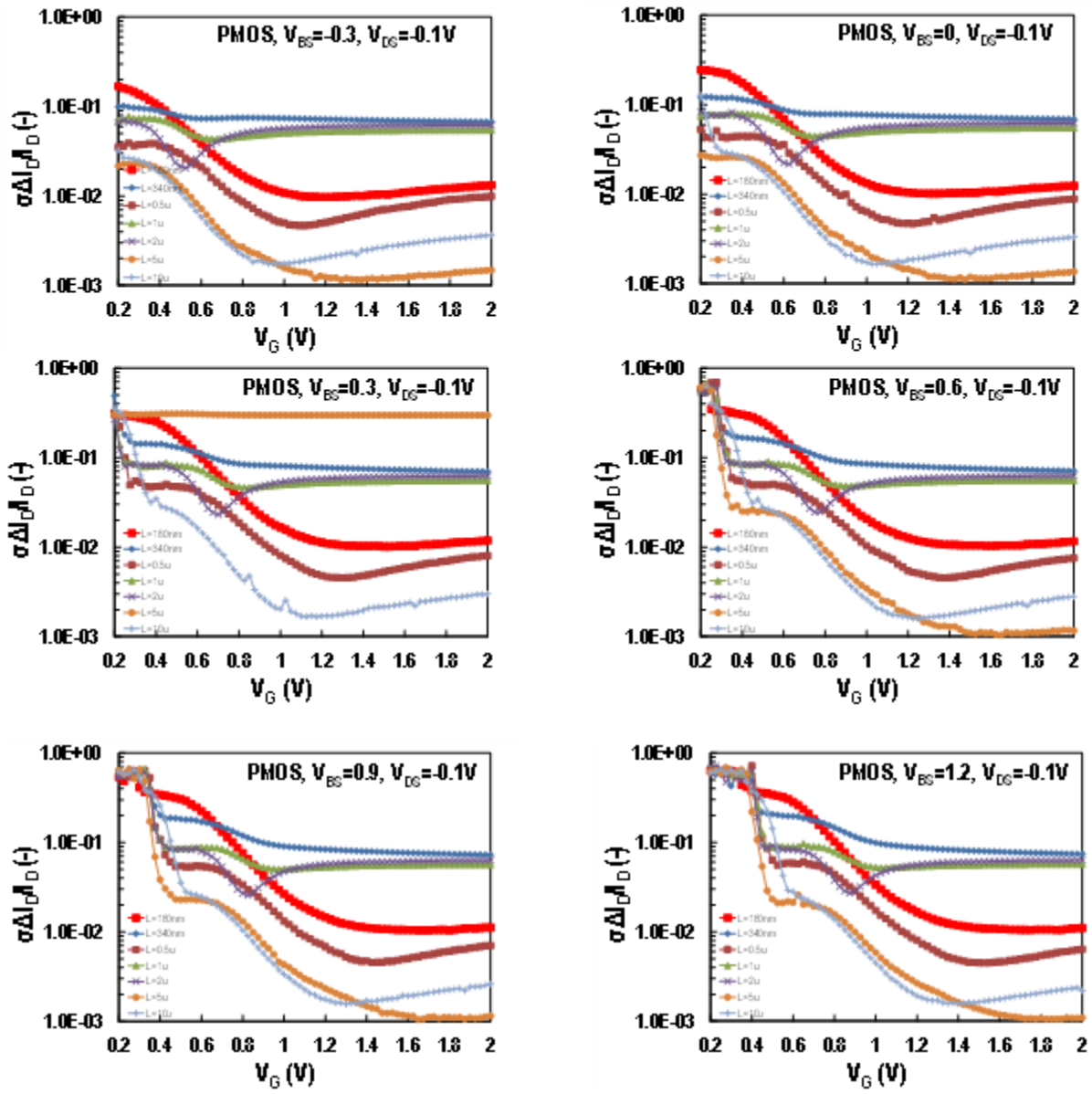


Figure 4. 13 $\sigma(\Delta I_D/I_D)$ vs V_G graphs for L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um. Each graph shows the results for different V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V.

Drain current mismatch $\sigma(\Delta_{ID}/I_D)$ decreases for bigger channel length L and becomes higher towards weak inversion. This is an expected behavior, since current mismatch is expected to follow the gm/I_D behavior versus inversion coefficient.

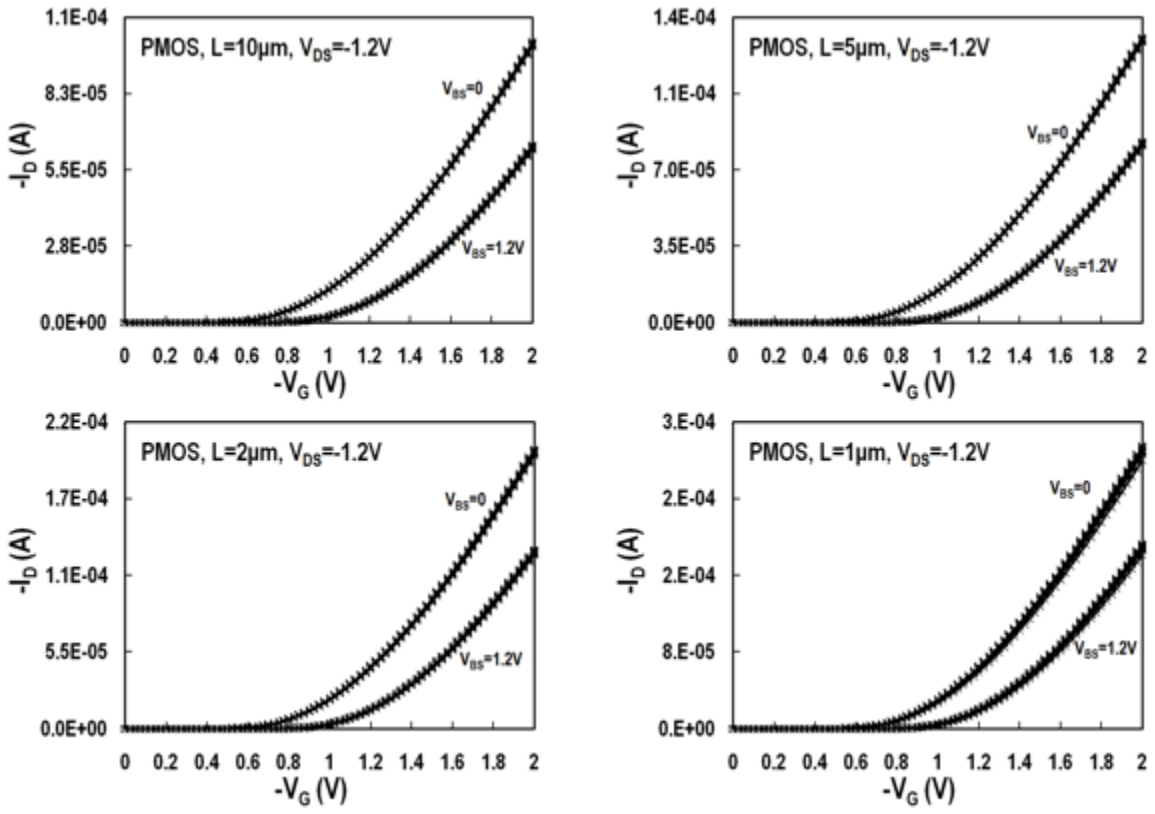
4.2 Measurements for V_{DS}= -1.2 V (saturation region)

In this part of the thesis we will examine the graphic representation of the MOSFET characteristics, while the drain-source voltage equals -1.2V.

4.2.1 Measured I/V characteristics

In this section the measured I_D vs. V_G plots will be presented. The $|I_D|$ for every gate voltage value, represents the mean value of the measured drain current ($|I_D|$), on a number of 96 P MOSFETs on the same gate voltage. The unitless quantity G_mU_T/I_D is also calculated from the average G_m value that was extracted from measurements.

Measurements – V_{DS}=-1.2V (Lin axis)



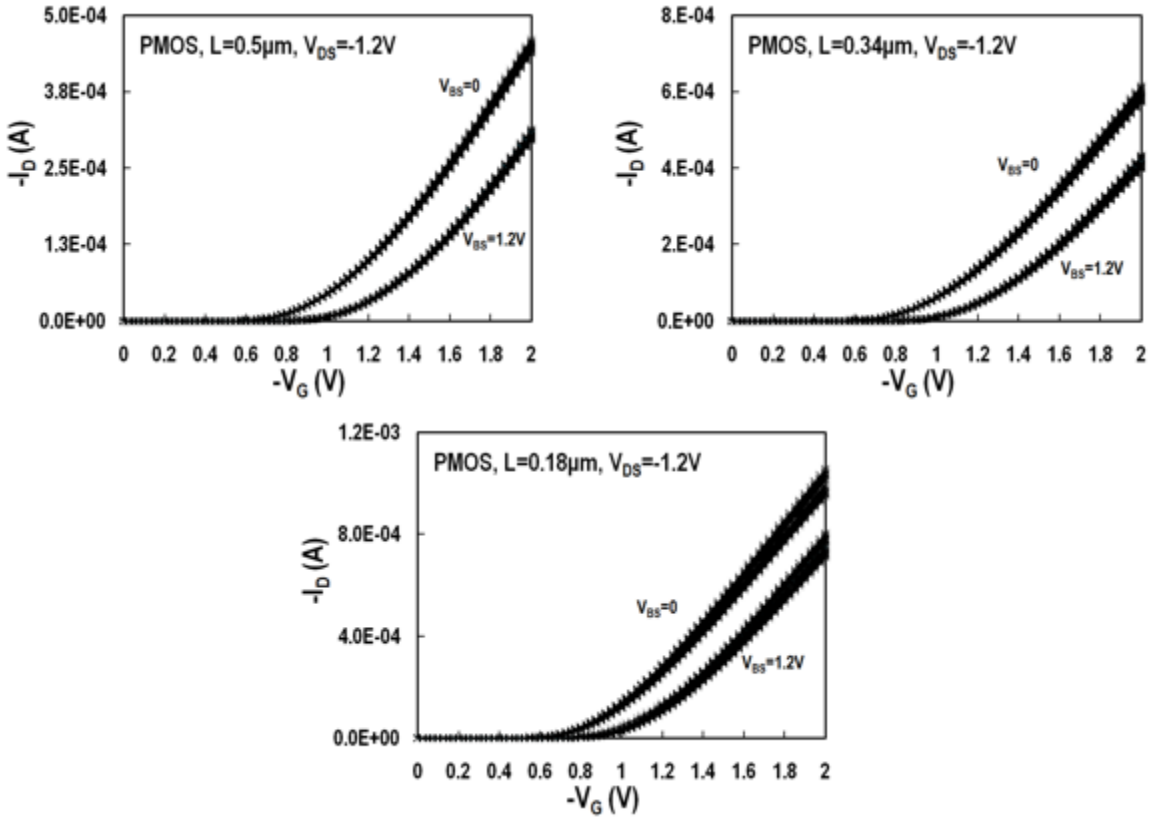


Figure 4. 14 I_D vs V_G graphs for V_{BS}=0, 1.2 V. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um)

In the figure above we see that I_D increases when we increase the gate Voltage (as expected). Also, I_D is higher for V_{BS} = 0 V than it is for V_{BS} = 1.2 V. This behavior is normal and similar to standard transistors.

Measurements – V_{DS}=-1.2V (Log axis)

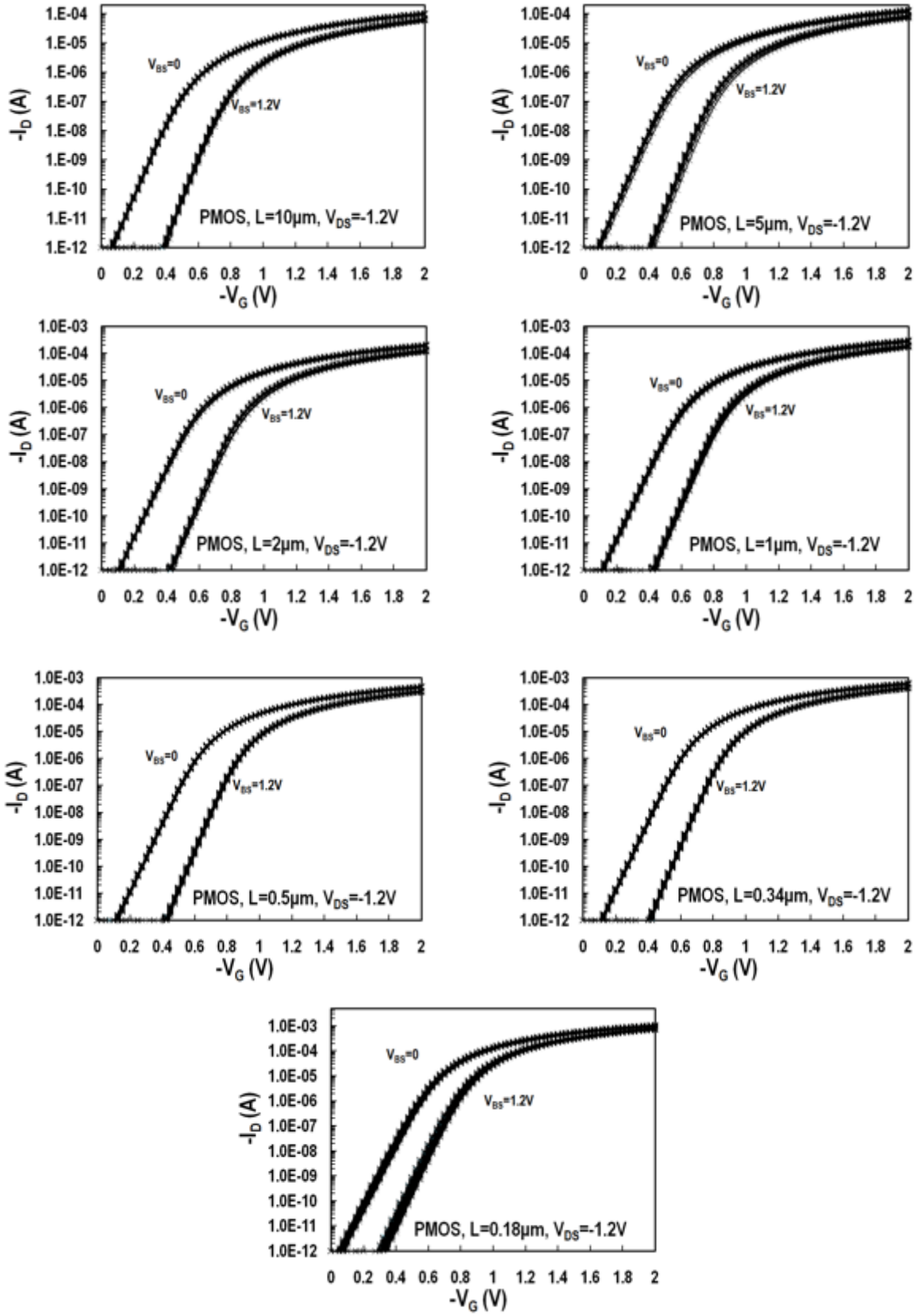


Figure 4. 15 I_D vs V_G graphs for V_{BS}=0, 1.2 V in a logarithmic axis. Each graph shows the results for different channel lengths. (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um)

g_m (V_{DS}=-1.2V) – Mean Value

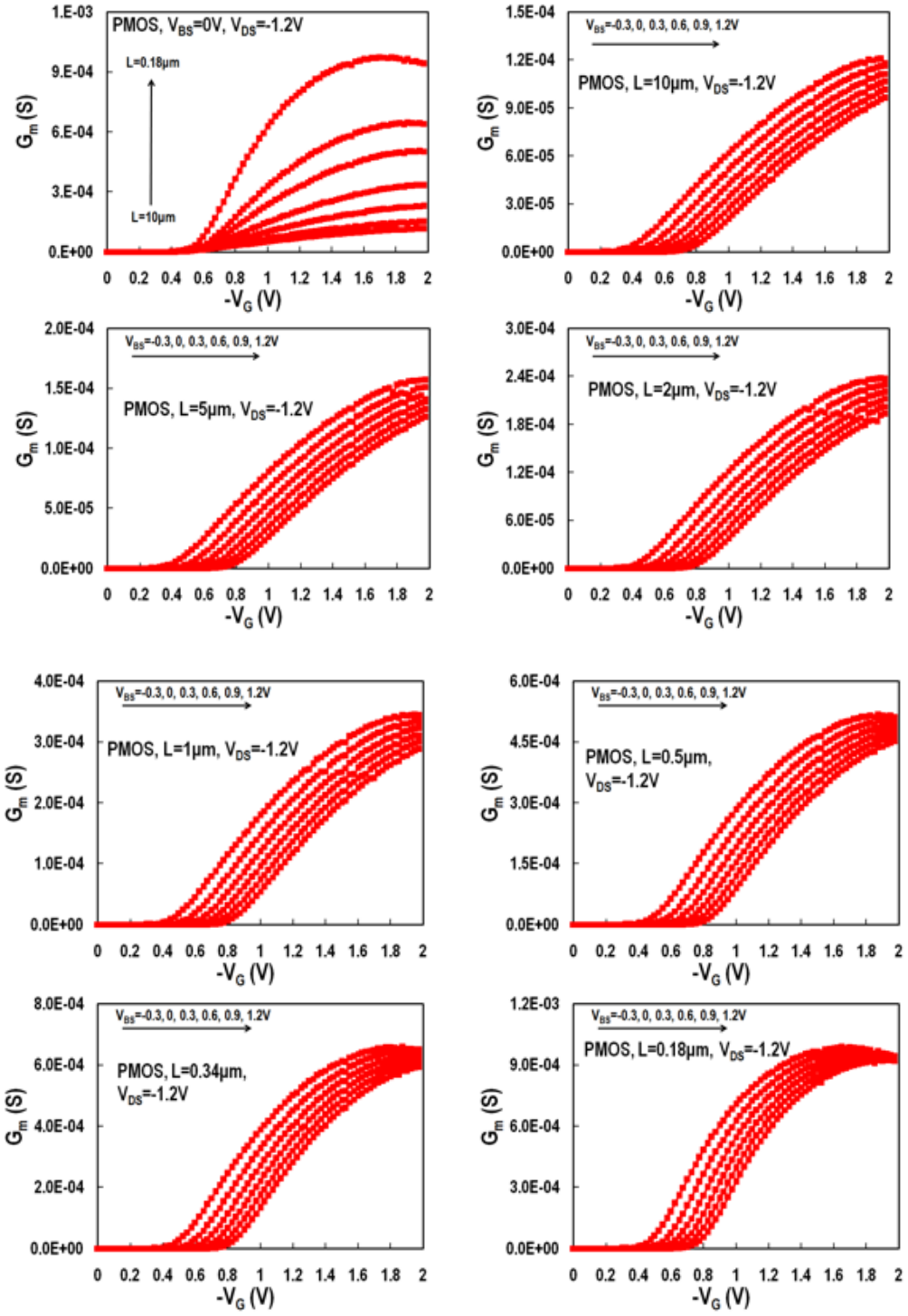


Figure 4. 16 G_m vs V_g graphs for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V are presented. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um) except for the top left graph which presents the result of all the different channel lengths when V_{BS} equals 0.

In the graphs above, we can clearly see that as the channel length gets smaller, the transconductance increases. Another observation is that Gm's peak increases with higher V_{BS}. This is the expected result which is similar to the result of the standard version of these transistors.

g_mU_T/I_D (V_{DS}=-1.2V) – Mean Value

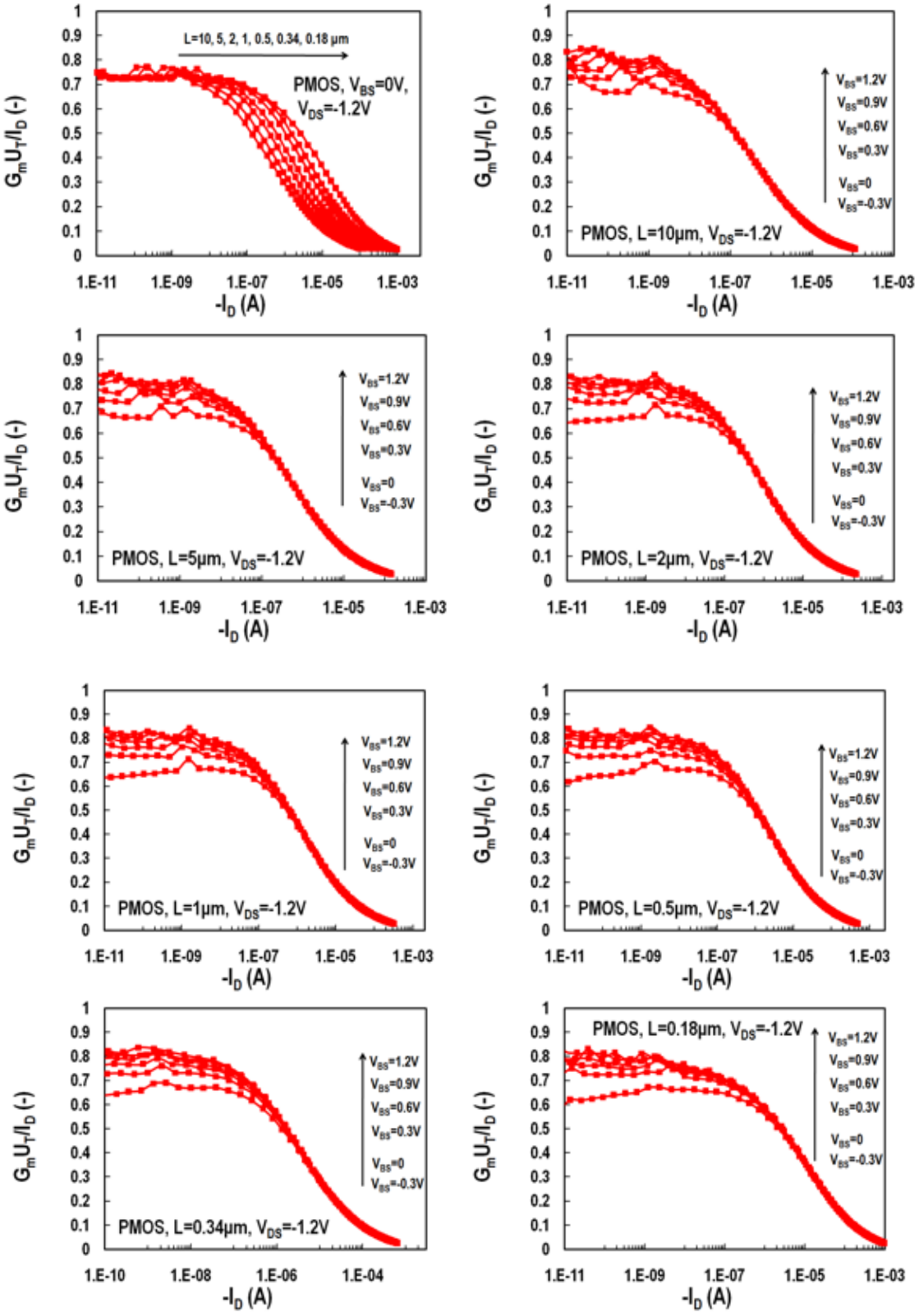


Figure 4. 17 The GmU_T/I_D graphs for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V are presented. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um) except for the top left graph which presents the result of all the different channel lengths when V_{BS} = 0.

The unitless quantity G_mU_T/I_D is higher for lower current I_D. It also appears to be higher for higher V_{BS}.

4.2.2 $(\delta\sqrt{I_D})/(\delta V_G)$

$(\delta\sqrt{I_D})/(\delta V_G)$ (V_{DS}=-1.2V) – Mean Value

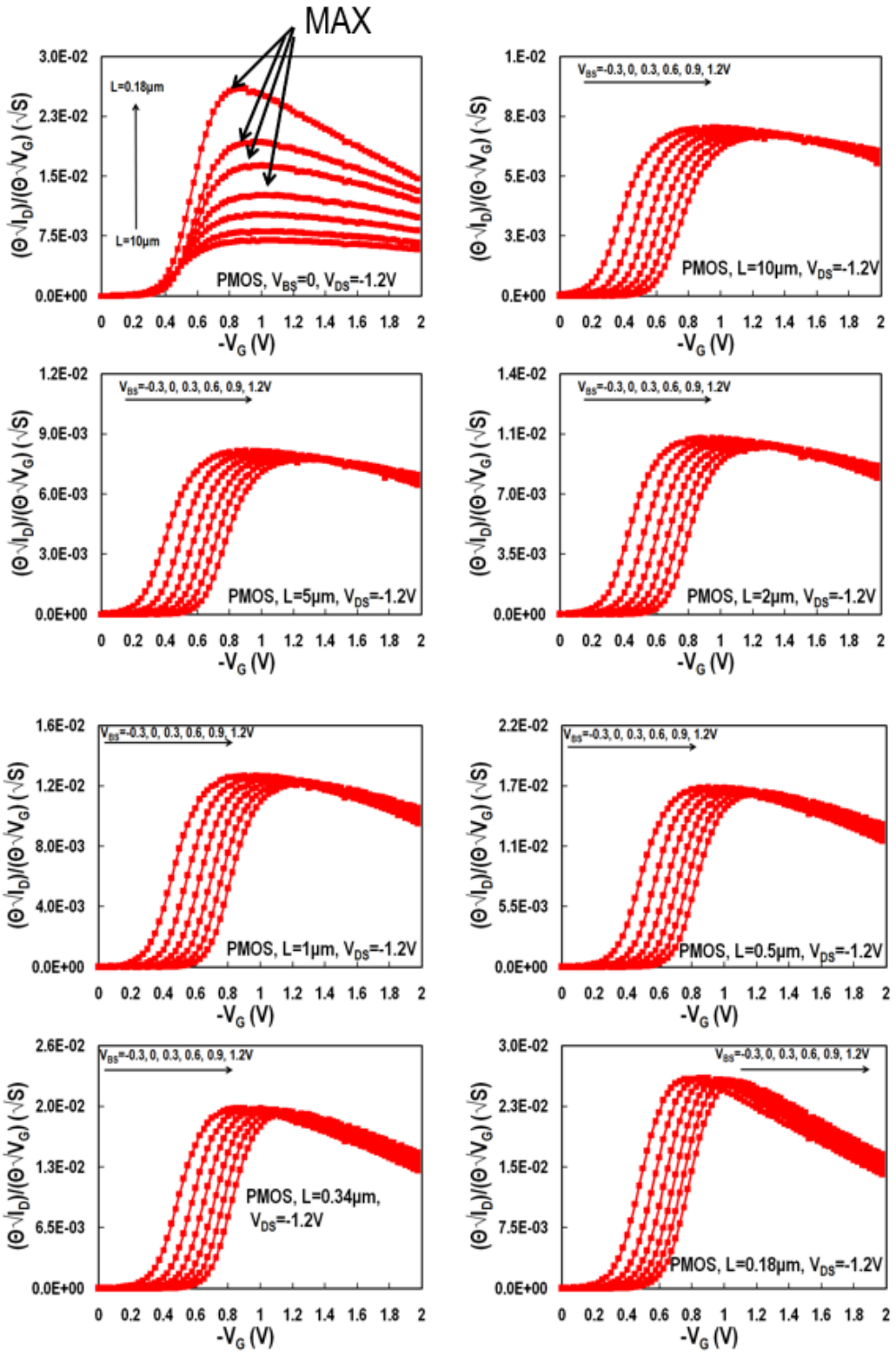


Figure 4. 18 (ΘVID)/(ΘVVG) vs VG graphs for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V are presented. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um) except for the top left graph which presents the result of all the different channel lengths for V_{BS} = 0.

4.2.3 Threshold Voltage

V_{TH} – Mean Value, Sigma (V_{DS}=-1.2V)

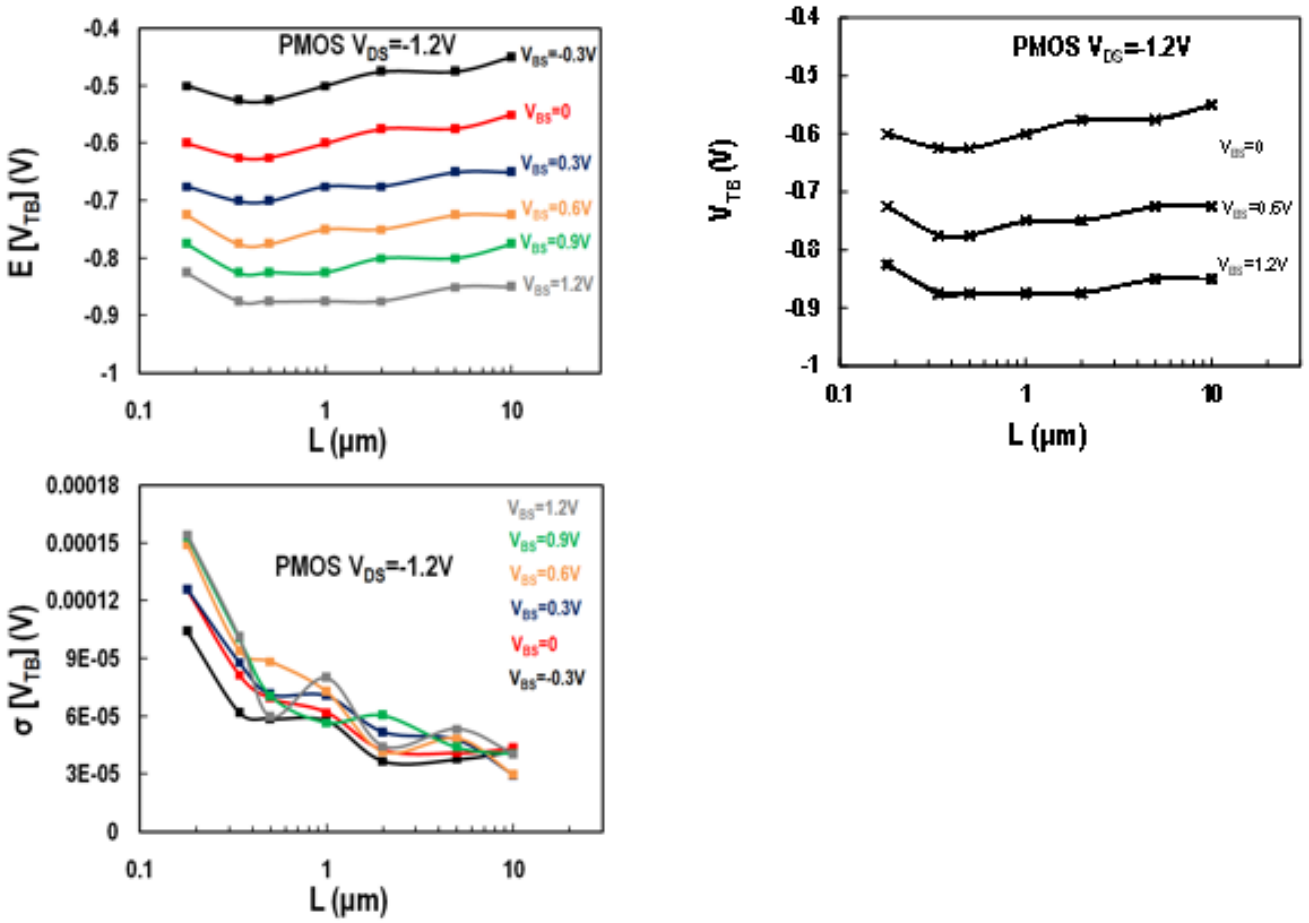


Figure 4. 19 (upper left) The E[V_{TB}] vs L graph for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V is presented above.

(upper right) V_{TB} vs L graph is presented. V_{DS} is -1.2 Volts and V_{BS}= 1.2, 0.6 and 0.

(lower left) σ[V_{TB}] vs L graph is presented for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V

- The mean value of the threshold voltage (E[V_{TB}]) dips for 340nm (the second lowest channel length) and then starts to raise while the channel lengths get bigger.
- V_{TB} dips for 340nm (the second lowest channel length) and then starts to increase while the channel lengths get bigger.
- The standard deviation of V_{TB} is significantly higher for 180nm. While the channel length gets bigger, the V_{TB} standard deviation decreases. Another conclusion made after examining the graph above, is that σ[V_{TB}] is higher for higher V_{BS}.

4.2.4 Threshold Voltage Matching

ΔV_{TH} – Matching (V_{DS}=-1.2V)

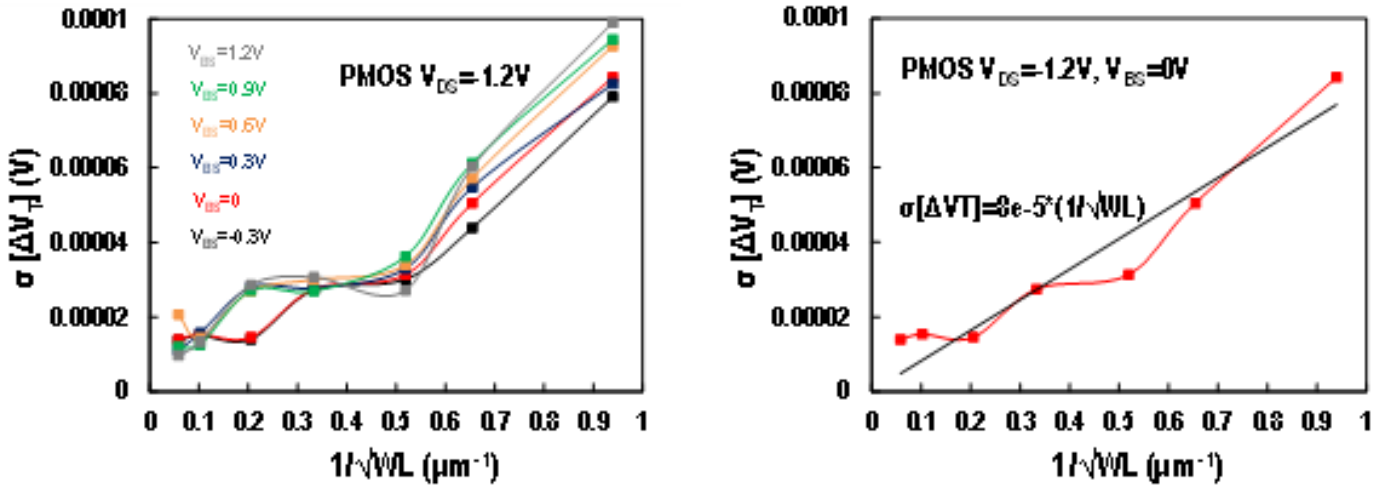


Figure 4. 20 The σ[ΔV_T] vs 1/ $\sqrt{WL}$ graph for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V is presented in a). In b) we examine V_{BS} =0 exclusively.

Examining the figure above we can conclude that the matching gets better for bigger 1/ $\sqrt{WL}$. This makes sense because as the product of the width and the length decreases, the unitless quantity 1/ $\sqrt{WL}$ increases and for smaller dimensions where the distance between the different semiconductors is smaller, we expect increased deviation between the measurements.

4.2.5 Mobility

The mean value of the mobility for every channel length, the mobility for specific V_{BS} and its standard deviation will be our focus in this subchapter. Representative graphs and their results will be presented below.

μ – Mean Value, Sigma (V_{DS}=-1.2V)

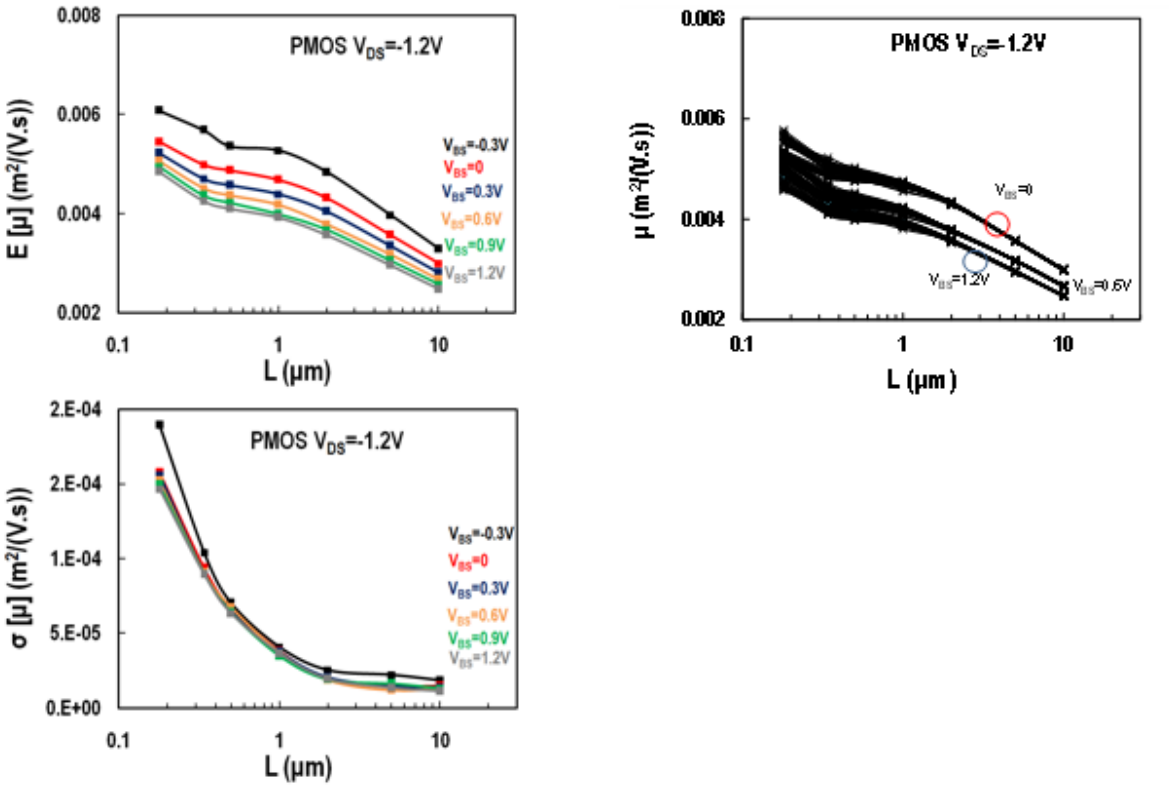


Figure 4. 21 (upper left) E[μ] vs L graph for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V

(upper right) μ vs L graph for V_{BS} = 0, 0.6, 1.2V

(lower left) σ[μ] vs L graph for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V

- The mean value of the mobility decreases for bigger channel length and higher V_{BS}. Furthermore, mobility becomes bigger for smaller channel length devices, following typical behavior.
- Mobility decreases for bigger channel length. It also decreases for lower V_{BS}. Furthermore, mobility becomes bigger for smaller channel length devices, following typical behavior.
- The standard deviation of μ, is higher for smaller channel lengths. This is something we expect since, as we already know, the electron mobility is inversely proportional to the channel length

4.2.6 Mobility Matching

In this part of the thesis our focus will be on the matching of the mobility. Results of 48 pairs of PMOS transistors for each channel length, will be presented in the graphs below.

Δμ/μ – Matching (V_{DS}=-1.2V)

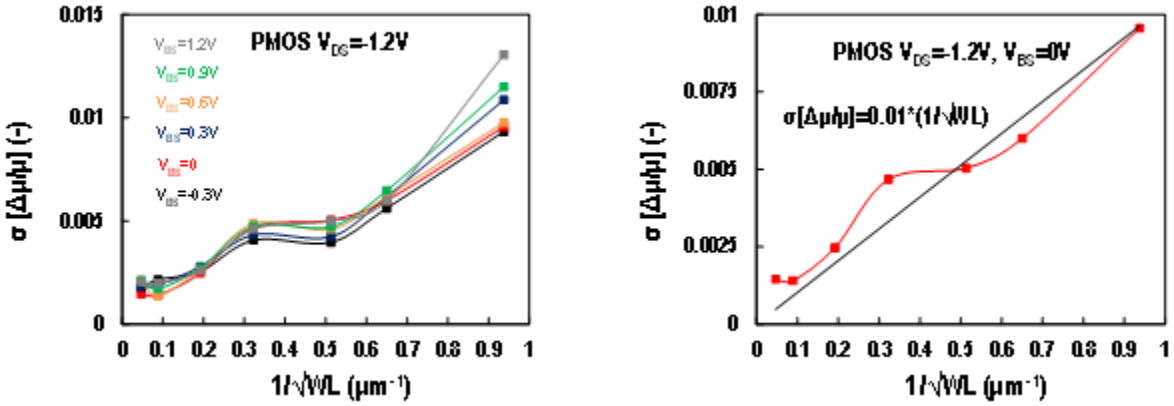


Figure 4. 22 a) σ[Δμ/μ] vs 1/ $\sqrt{WL}$ for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V. b) σ[Δμ/μ] vs 1/ $\sqrt{WL}$ for V_{BS} = 0V

In figure 4.22 we see that σ(Δμ/μ) increases with 1/ $\sqrt{WL}$ and is independent to V_{GB}, as expected and similar to the respective standard transistors.

4.2.7 Slope factor

In this part of the thesis we are going to focus on the slope factor and its behavior for transistors with different channel length and for different base-source voltages in each of them.

n – Mean Value, Sigma (V_{DS}=-1.2V)

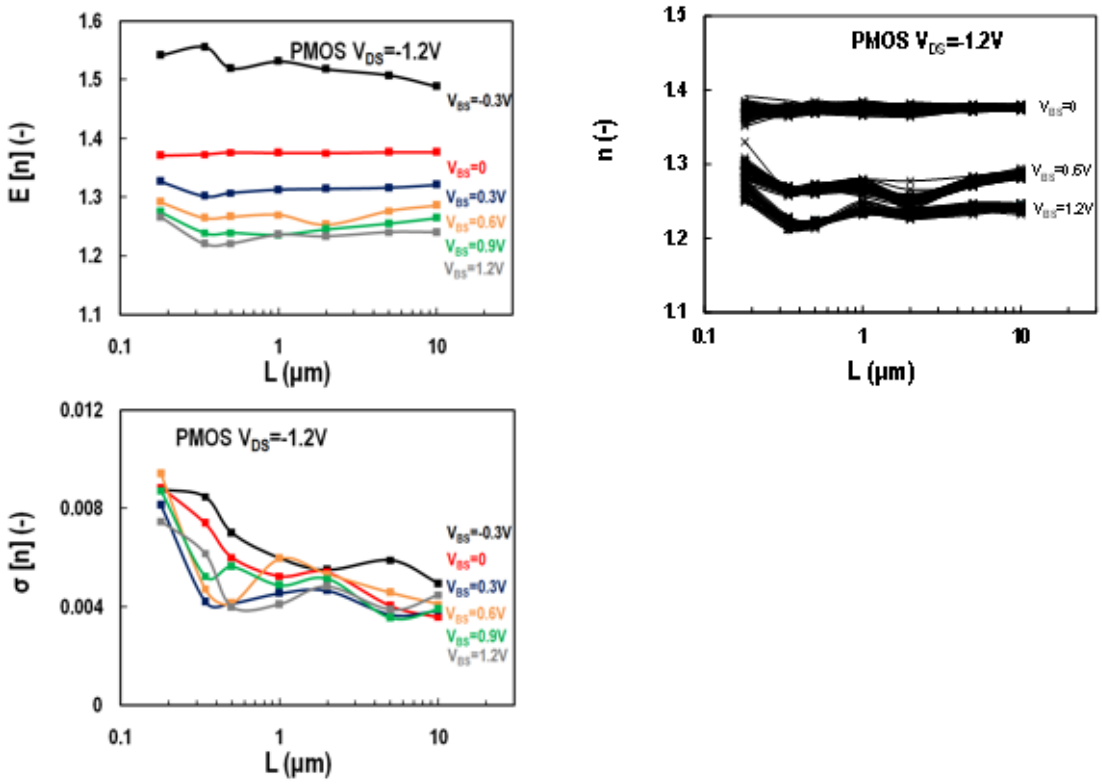


Figure 4. 23 (upper left) E[n] vs L graph for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V

(upper right) n vs L graph for V_{BS} = 0, 0.6, 1.2V

(lower left) σ vs L graph for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V

- In the figure above we can examine the mean value of the slope factor. It decreases with higher V_{BS}.
- Slope factor decreases with higher V_{BS}. It can be noticed that slope factor decreases at higher VBS. Furthermore, slope factor versus channel length is almost constant with a slight increment towards smaller channel lengths as expected.
- Standard deviation of n, decreases with higher $V_{BS.}$ Similar results are extracted from respective standard transistors.

Δn/n – Matching (V_{DS}=-1.2V)

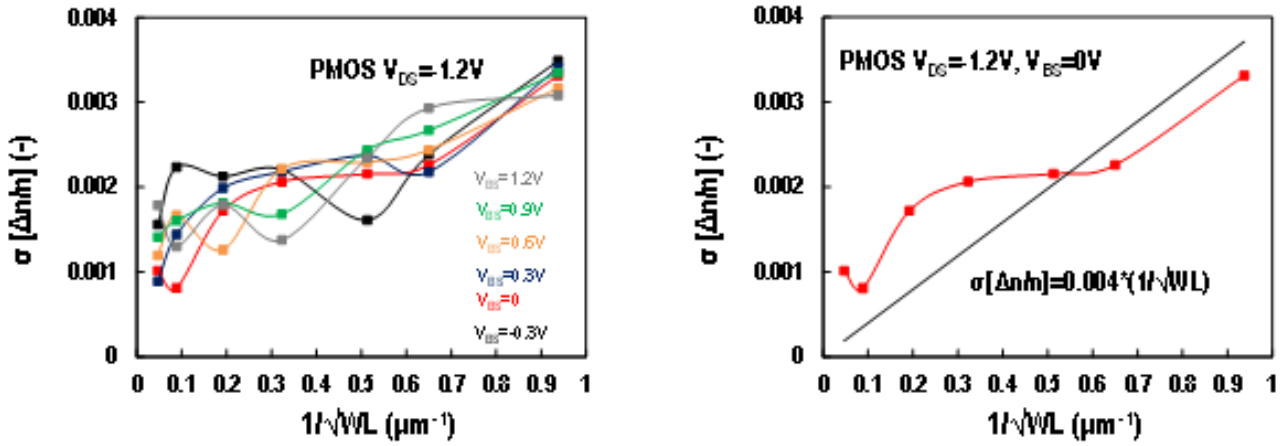


Figure 4. 24 a) σ[Δn/n] vs 1/ $\sqrt{WL}$ for V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V. b) σ[Δn/n] vs 1/ $\sqrt{WL}$ for V_{BS} = 0V

As we can see in the graphs above, σ[Δn/n] increases with 1/ $\sqrt{WL}$. This behavior of the graphs is normal.

$\sigma(\Delta I_D/I_D)$ – Matching (V_{DS}=-1.2V)

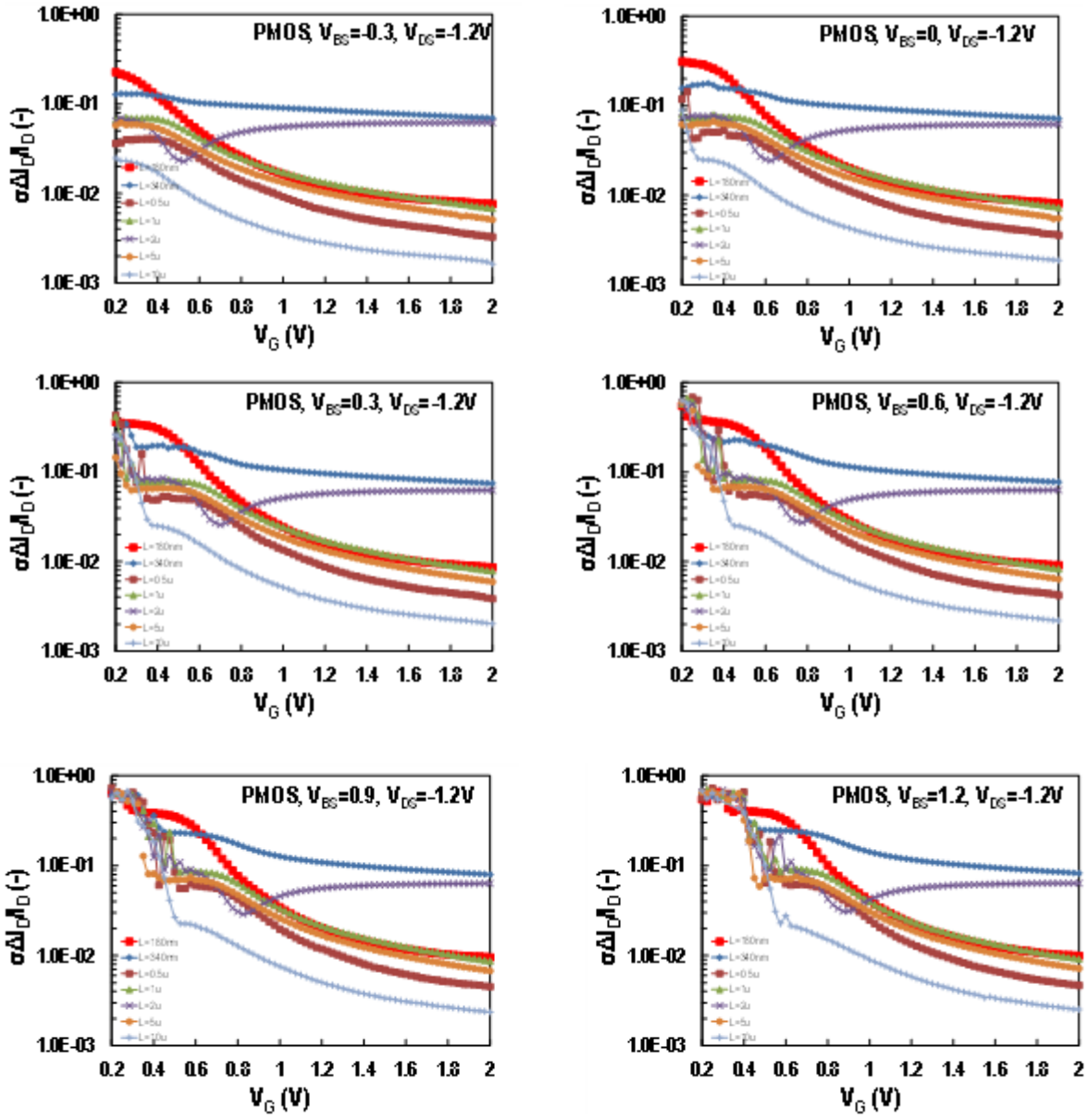


Figure 4. 25 $\sigma(\Delta I_D/I_D)$ vs V_G graphs for L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um. Each graph shows the results for different V_{BS} = -0.3, 0, 0.3, 0.6, 0.9, 1.2V.

Drain current mismatch $\sigma(\Delta_{ID}/I_D)$ decreases for bigger channel length L and becomes higher towards weak inversion. This is an expected behavior, since current mismatch is expected to follow the gm/I_D behavior versus inversion coefficient.

5.Conclusions

5.1 Summary

This thesis offers interesting results of enclosed gate PMOS transistors. The range of the channel length (0.18μm, 0.34μm, 0.5μm, 1μm, 2μm, 5μm, 10μm), as well as the total numbers of the MOSFETs (672) measured gives as a valid picture of the operation of this type of MOSFETs. Results of all regions of inversion for both linear and saturation region of operation were extracted. This thesis also includes a study of Mismatching between MOSFET pairs on same die.

The most important result of this thesis is that the statistical analysis shows that Enclosed transistors scale well from L=180nm to 1μm (choice of optimal devices).

EG MOSFETs present identical behavior with that of the standard layout MOSFET transistors as expected. Basic parameters, such as: weak inversion slope, threshold voltage, mobility, and mismatch, where extracted based on the typical extraction methods used in the ST layout MOSFETs. The statistical behavior of the extracted parameters follows that of the standard MOSFETs in all cases.

5.2 Future work

The results of the thesis give potential for future work: Comparison with NMOS transistors of the same type, comparison with standard MOSFETs and the respective channel length, studying of the result of each die separately and examining how the position of the die on the wafer affects the results (if it does), etc. Extracted parameters A_{VT}, Aμ, An can be directly used in Integrated Circuit design.

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