TECHNICAL UNIVERSITY OF CRETE
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

Design of a low-power 10 GHz LC Voltage Controlled Oscillator (LC-VCO) for wireless communications in FDSOI technology

By Nikolaos Dimosthenis Agiorgousis

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THESIS COMMITTEE
Professor Matthias Bucher, Thesis Supervisor
Professor Aggelos Bletsas
Dr. Georgios Kamoulakos

Dedicated to my family. . .

1 Abstract

The present thesis aimed to study, design, and simulate a voltage-controlled oscillator (VCO) for wireless communications at 10GHz.

Almost the entire work was conducted at weasic Microelectronics S.A, which provided access to simulation tools and the process design kit.

The proposed oscillator adopts an NMOS cross-coupled pair LC-VCO circuit which is implemented in a 22nm FD-SOI process known for its fully depleted silicon layer. This technology ensures superior power efficiency, mitigates short-channel effects and offers enhanced control over transistor electrostatics. Investigations revealed that the reduced temperature sensitivity of FD-SOI contributes to stable performance, critical for a high-performance LC-VCO. The initial specifications for implementing this specific VCO were to operate in a frequency range from 9.5GHz to 10.125GHz. Indeed, in this thesis, the operating frequencies range from 9.44GHz to 10.17GHz with a step of 4.8MHz. The phase noise at the operating frequency of 10GHz is quantified at -125.138dBc/Hz at a 1MHz offset with a tuned control voltage from 0.1V to 1.1V. The oscillator consumes 12.9mW with a 10.448mA DC current at a 1.24V supply voltage. The overall performance of the LC-VCO is compared to that of other published oscillators using quality indicators (Figures of Merit, FoM).

In this thesis, after extensive investigations, such as parametric explorations and studies of cases, the significance of the quality factor became evident, both for the individual passive elements of the circuit and the overall system. It was revealed how this factor influences the performance of the overall design, determining it as the 'bottleneck' of the system by influencing phase noise.

Keywords— VCO, LC oscillator, Cross-coupled differential oscillator, Quality factor , PN-Phase noise

2 Περίληψη

Η παρούσα διπλωματική εργασία είχε ως στόχο τη μελέτη, τον σχεδιασμό και την προσομοίωση ενός ταλαντωτή ελεγχόμενου από τάση (VCO) για ασύρματες επικοινωνίες στα 10GHz.

Το μεγαλύτερο μέρος της εργασίας πραγματοποιήθηκε στην εταιρεία weasic Microelectronics S.A:, η οποία παρείχε πρόσβαση στα πακέτα σχεδίασης και τεχνολογίας.

Ο ταλαντωτής που σχεδιάστηκε υιοθετεί ένα κύκλωμα LC-VCO διασταυρούμενου ζεύγους NMOS και υλοποιείται σε τεχνολογία FD-SOI 22nm, γνωστή για το fully depleted στρώμα στο πυρίτιο. Αυτή η τεχνολογία διασφαλίζει υψηλή απόδοση ισχύος, αντιμετωπίζει αποτελεσματικά τα short-channel effects και προσφέρει ενισχυμένο έλεγχο επί της ηλεκτροστατικής των τρανζίστορ. Οι έρευνες αποκάλυψαν ότι η μειωμένη ευαισθησία στη θερμοκρασία της τεχνολογίας FD-SOI συμβάλλει στη σταθερή απόδοση, κρίσιμη για ένα LC-VCO υψηλής απόδοσης. Οι αρχικές προδιαγραφές για την υλοποίηση του συγκεκριμένου VCO ήταν να μπορεί να κυμαίνεται σε ένα εύρος συχνοτήτων από 9.5GHz έως 10.125GHz. Πράγματι, στην συγκεκριμένη διπλωματική εργασία, οι συχνότητες λειτουργίας κυμαίνονται στο φάσμα 9.44GHz εως 10.17GHz με βήμα 4.8MHz. Ο θόρυβος φάσης σε συχνότητα λειτουργίας τα 10GHz ποσοτικοποιείται στα -125.138dBc/Hz σε 1MHz απόκλιση, με μεταβλητή τάση ελέγχου από 0.1V έως 1.1V. Ο ταλαντωτής καταναλώνει 12.9mW με 10.448mA dc ρεύμα, σε τροφοδοσία 1.24V. Η συνολική απόδοση του LC-VCO συγκρίνεται με αυτή άλλων δημοσιευμένων ταλαντωτών, με την χρήση δεικτών ποιότητας (Figures of Merit, FoM).

Σε αυτήν τη εργασία, μετά από εκτενείς έρευνες, όπως παραμετρικές προσομοιώσεις και μελέτες περιπτώσεων, έγινε εμφανές το πόσο σημαντικός είναι ο παράγοντας ποιότητας τόσο των επιμέρους παθητικών στοιχείων του κυκλώματος όσο και ολόκληρου του συστήματος. Αποκαλύφθηκε πώς αυτός ο παράγοντας επηρεάζει την απόδοση του συνολικού σχεδιασμού, χαρακτηρίζοντάς τον ως το 'bottleneck' του συστήματος, λόγω της επίδρασής του στον θόρυβο φάσης.

Keywords— VCO, LC oscillator, Cross-coupled differential oscillator, Quality factor , PN-Phase noise

3 Acknowledgements

First and foremost, I express my sincere gratitude to Prof. Matthias Bucher, my supervisor, for providing me with the opportunity to undertake this thesis and for the trust he placed in me. The chance to work on my thesis at Weasic Microelectronics allowed me to engage with the professional field and acquire knowledge that will undoubtedly benefit me in all future steps in my career and life. I am also thankful to Dr. Emmanouil Metaxakis for granting me the opportunity to join this esteemed company. Special appreciation goes to Prof. Aggelos Bletsas and Dr. George Kamoulakos for their roles as members of the thesis committee and for their valuable evaluation of my work.

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VCO	Voltage controlled oscillator
PN	Phase noise
LC	Inductor-capacitor
CMOS	Complementary metal-oxide-semiconductor
dBc	Decibel relative to the carrier
PVT	Process voltage temperature
LTV	Linear time-variant
MOS	Metal-oxide-semiconductor
Q	Quality factor
AM	Amplitude modulation
FM	Frequency modulation
PDC	Power dissipation consumption
FoM	Figure of merit
PLL	Phase locked loop
PFD	Phase/frequency detector
PSD	Power spectral density
SNR	Signal to noise ratio
ISF	Impulse sensitivity function
CP	Charge pump
LPF	Low pass filter
RF	Radio frequency
rms	Root mean square
IC	Integrated circuit
RO	Ring oscillator
CAD	Computer aided design
VDD	Positive supply voltage
VSS	Ground
EMI	Electromagnetic interference
RFI	Radio frequency interference

4 Voltage-controlled oscillator basics

Oscillators are a crucial building block of virtually every electronic system. Oscillators have been so far common and inevitable signal sources since radio technologies, such as communication, radar, broadcasting, navigation and radiometry, were invented. In most practical applications, the frequency of the signal generated by the oscillator must be controllable over some range, this is commonly achieved using a reactance element in the oscillator circuit that responds to changes in voltage. As a result, it is referred to as a voltage-controlled oscillator, often abbreviated as VCO. Several oscillator topologies were developed in past, where each one has its advantage and disadvantage. A topology may be appropriate for an application, if its fulfills the requirements to the oscillator for the given system. VCOs are in fact the most suitable among the other RF blocks to be integrated in CMOS, where the transistors are usually not the performance limiting components. The most widely used topology of VCO is LC-tank based VCO which is termed as LC-VCO due to its simple structure and good performance. In that case, the passive components such as the variable capacitors and the inductors are usually the limiting components. Although the variable capacitors have advantages when the CMOS process is scaled down, this leads to other more serious problems such us the tuning linearity.

4.1 Fundamentals of oscillator operation

Oscillators represent a foundational concept in electronics, providing a means to generate continuous periodic waveforms without an external signal source. The operation of oscillators relies on the interplay between reactive components, amplification, and feedback mechanisms. An oscillator generates a periodic output. As such, the circuit must involve a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal.

Feedback in Electronic Circuits: An Overview

Feedback is a fundamental concept in electronic circuits that involves the redirection of a portion of the output signal back to the input of a circuit. It plays a crucial role in shaping the behavior of circuits, influencing their stability, gain, bandwidth, and other performance characteristics.

The oscillator behavior can be explained by either an amplifier with positive and selective feedback model or as a negative resistance single-port connected in parallel with a resonant tank, as illustrated in Figure 1 (a) and (b) respectively. The feedback model treats the oscillator as a linear feedback system, while the negative resistance model separates the oscillator into two networks (resonator and active circuit) connected to each other. Depending on the oscillator configuration and characteristic, one model may be preferred over the other. Although the negative resistance approach is commonly used for microwave oscillator design [1].

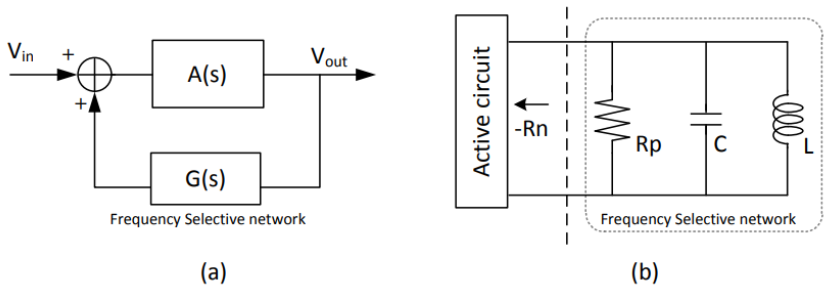

Figure 1: Oscillator model as: (a) linear feedback system and (b) as a linear negative resistance generator in parallel with a resonant tank load

Considering the simple linear feedback system in Figure 1(a), the overall transfer function can be written as:

$$\frac{Vout(s)}{Vin(s)} = \frac{A(s)G(s)}{1 - A(s)G(s)} \quad (4.1)$$

The linear behavior of a feedback circuit is typically studied using the loop-gain quantity, defined as the product of the forward and feedback transfer function A(s) and G(s) respectively. The expression 1-A(s)G(s) gives the characteristic equation of the circuit from which the poles are found. For ease of reference, we use the term feedback oscillator to denote an oscillator circuit that has a well-defined feedback loop and can be analyzed using the feedback model [2]. In order for steady oscillation to occur, the loop gain and phase shift must satisfy the Barkhausen criteria:

1. The loop gain, $|A(s)G(s)| \geq 1$

2. The total phase shift around the loop, $\angle A(s) + \angle G(s) = 0°or360°$.

Upon solving the aforementioned criteria for oscillation, one can derive both the oscillation frequency and the necessary gain. In the majority of RF oscillators, the feedback loop's G(s) can take the form of a frequency selective network, often referred to as a "resonator". It's important to highlight that Barkhausen's criteria [15] are necessary, but alone are not adequate for ensuring oscillation. For instance, the circuit might experience latch-up instead of oscillation, occurring when the loop's phase shift reaches 360° and the loop gain remains substantial.

On the other hand, if the oscillator circuit can be separated into a one-port, active circuit and a one-port, resonator. The negative resistance model can be depicted as in Figure 1 (b). The resonator is symbolized as parallel resonant LC-tank consisting of an inductor L and a capacitor C. Generally, the LC-tank determines the frequency of oscillation, while the active circuit provides a negative resistance –Rn to compensate the loss of the resonator (Rp in Figure 1 (b)) and sustain the oscillation. When the energy supplied by the active circuit matches the loss of the resonator, a stable oscillation can be maintained.

As it seems in figure 2(a), if a unit impulse applied in an LC tank with a parallel resistance the oscillation frequency decreases. In figure 2(b) the additive negative resistance has the same absolute value with the parallel resistance of LC tank. So the addition of the two resistances values eliminates the LC tank losses.

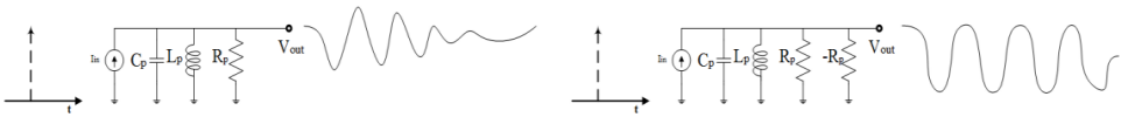

Figure 2: An LC-tank without negative resistance (a), An LC-tank with negative resistance (b).

The startup condition of the oscillation and the oscillation frequency can be given by:

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (4.2)$$

$$|R_n| < R_p \quad (4.3)$$

In practice, Rp is usually designed as three times the value of Rn to ensure a robust oscillation against process, voltage and temperature (PVT) variations.

4.2 Ring oscillators

A Ring oscillator is a type of electronic oscillator that generates a continuous periodic waveform, typically a square wave, by cascading an odd number of inverting stages in a closed-loop configuration. This arrangement creates a self-sustaining feedback loop where the output of the last stage feeds back to the input of the first stage, leading to continuous oscillation [3]. Ring oscillators find applications in various fields, including digital systems, clock generation and frequency synthesis. Ring oscillators are the simplest oscillators for integrated systems. They are easy to design and can reach very high frequencies, while having a low to moderate power consumption. The phase noise of ring oscillators suffers from the low open loop Q and the noisy active devices in the signal path, but if carefully designed, they can even have acceptable phase noise performance for transceiver systems. RC ring oscillators are a well-known type of resonator-less oscillators. As shown in Figure 3, the ring oscillator is always made up of three or more stages (of odd prime number) of inverters or delay cells with the output feedbacked to the input.

The operation of a ring oscillator can be understood by considering each inverting stage's role in introducing a phase shift [4]. The number of stages determines the cumulative phase shift and the frequency of oscillation. More stages lead to lower frequencies, but there's a trade-off with power consumption and delay. RO consume power with each cycle, and power consumption increases with higher oscillation frequencies. Each stage introduces a 180-degree phase shift due to its inverting nature. As a result, an odd number of stages (such as 3, 5, 7, etc.) creates a cumulative phase shift of an odd multiple of 360 degrees (or 2π radians), satisfying the Barkhausen criterion for oscillation. This cumulative phase shift, combined with the inherent gain of each stage, leads to self-sustaining oscillation.

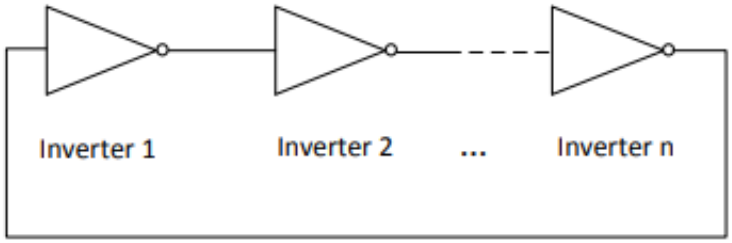

Figure 3: Topology of typical RC-ring oscillator

4.3 LC oscillators

LC oscillators play a very important role in the frequency generation of modern wireless transceiver systems, which are working usually above 800MHz. Above this frequency, LC-oscillators are much more often used than ring oscillators, since they are more efficient in terms of FOM, where the power consumption and the phase noise performance are superior to those of ring oscillators.

The operation of the LC-VCO can be easily understood by using the negative resistance model [Figure 1(b)]. The topology of an LC-VCO with a cross-coupled pair is shown in Figure 4 . The cross-coupled NMOS transistors provide a negative resistance and add energy into the circuit to sustain the oscillation. The oscillation frequency is determined by the product of the tank inductance and of the tank capacitors (eq.4.4).

$$F_{osc} = \frac{1}{2\pi\sqrt{L_{TANK} * C_{TANK}}} \quad (4.4)$$

When the added energy is larger than the energy dissipated in the LC-tank, the oscillation can be excited. The start-up condition of an oscillator can be written as :

$$g_m \geq \frac{2}{R_p} \quad (4.5)$$

where gm is the transconductance of the cross-coupled transistors, and Rp represents the parallel resistive loss of the LC-tank. To ensure robust oscillation against process, voltage and temperature (PVT) variations, g_m is usually designed as three times the value of $2/R_p$. Likewise, the cross-coupled set can be implemented employing PMOS transistors. PMOS-only LC-VCOs might exhibit

reduced phase noise due to their diminished flicker noise. Nonetheless, when contrasted with NMOS transistors, PMOS counterparts operate at roughly half the speed and necessitate nearly twice the size to attain equivalent transconductance.

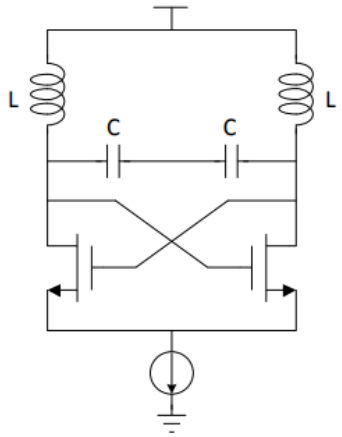

Figure 4: Topology of typical cross-coupled pair LC oscillator

Featuring an uncomplicated and balanced arrangement, LC-VCOs offer numerous benefits for high-speed and differential designs, exhibiting low power consumption and a practical tuning range. This renders them an appealing choice for designing mm-wave VCOs.

4.4 Specifications of LC-VCO's

4.4.1 Quality factor Q

The quality factor, often denoted as Q, is a crucial parameter in LC oscillators that characterizes the performance of resonant circuits. LC oscillators are electronic circuits that generate sinusoidal output signals at a specific frequency determined by the values of the inductor (L) and capacitor (C) components within the circuit. A higher-Q resonant circuit exhibits a narrower bandwidth around its central frequency. This characteristic implies that the circuit is more selective in terms of the frequencies it can resonate with. Consequently, the tuning frequency is more stable in high-Q circuits because it is less susceptible to variations in component values and external factors. However, while a higher-Q circuit indeed provides enhanced frequency stability, it can simultaneously limit the tuning range of the oscillator. The narrower bandwidth associated with high Q signifies that the oscillator can only be tuned over a reduced frequency range before losing resonance. Thus, the better the quality factor of the tuning tank, the smaller the tuning frequency becomes.

A higher-Q resonant circuit is capable of maintaining oscillations with minimal energy loss. As a result, the circuit requires less power to sustain oscillations when compared to a lower-Q circuit. Given that power consumption and the quality factor are inversely proportional, maximizing the total Q-factor becomes highly desirable [5]. The fundamental definition of Q is from the energy view, which is given by the energy stored divided by the energy dissipated per cycle.

$$Q = 2\pi \frac{\text{energy stored}}{\text{energy loss in one oscillation cycle}} \quad (4.6)$$

Typically, a resonant circuit exhibits a bandpass transfer function. Another definition of Q is the "sharpness" of the magnitude of a resonant circuit transfer function. More specifically, as shown in Figure 5, Q is defined as the resonance frequency, ω_0 , divided by the two-sided, -3 dB bandwidth (eq. 4.7). The oscillation occurs at the frequency where the phase shift of the LC-tank is zero.

$$Q = \frac{\omega_0}{\omega_{3db}} \quad (4.7)$$

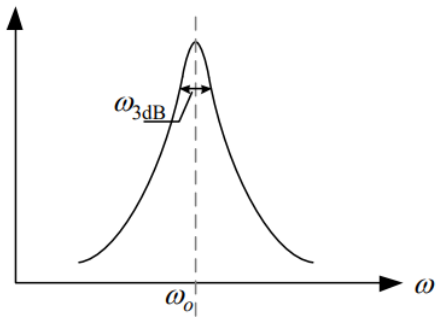

Figure 5: Magnitude of the LC tank

Another definition of Q that proves especially useful in oscillator design is illustrated in Figure 6. Here, the circuit is viewed as a feedback system and the phase of the open-loop transfer function, $\varphi(\omega)$, is examined at the resonance frequency, ω_0 [15]. The "open-loop" Q is defined as:

$$Q = \frac{\omega_0}{2} * \frac{|d_\varphi|}{|d_\omega|} \quad (4.8)$$

Referred to as "open-loop Q", this definition has an interesting interpretation. To generate steady oscillation, the total phase shift around the oscillator loop must be 360° (or zero). Assuming that the noise introduced by the components attempts to alter the frequency away from ω_0, according to Figure 6, such a deviation results in a modification of the overall phase shift within the loop, thus violating the condition of steady oscillation and forcing the frequency to return to ω_0. In other words, the open-loop Q is a measure of the opposition of the closed-loop system to variations in the frequency of oscillation.

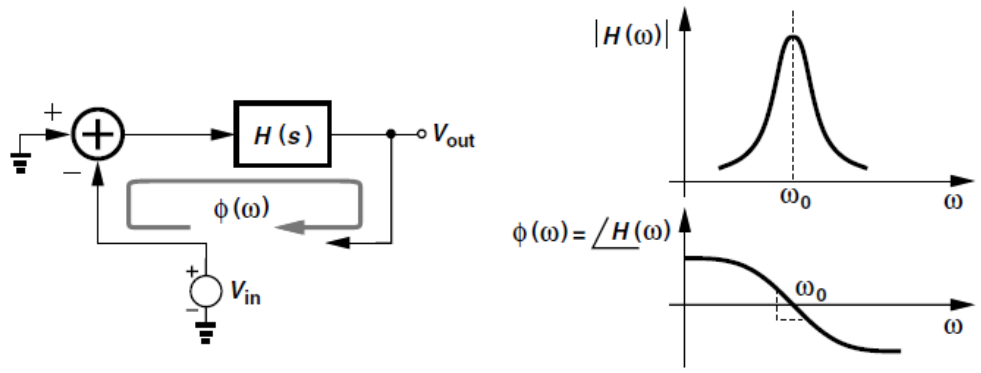

Figure 6: Definition of open-loop Q.

4.4.2 Integrated spiral inductors

IC technologies have historically grappled with the challenge of producing high-quality inductors. This is primarily because inductor coils, essential for generating magnetic flux, are constructed on a small scale and employ relatively lossy conductive materials. Small loops and the use of typical metallization, which serves well for most chip interconnections, introduce significant resistive losses when creating long wires required to achieve sufficient inductance. On-chip inductors also exhibit poor area efficiency when compared to capacitors and resistors due to the need for large loops. Nonetheless, the ongoing pressure to eliminate off-chip components has made on-chip inductors commonplace in RF transceivers. Consequently, research into integrated inductors, including analysis, design, modeling, and optimization, has been highly active over the past 15 years [6]-[10]. This section provides an overview of some of the design trade offs and modeling approaches.

In typical on-chip spiral inductor structures, as illustrated in Figure 7, multiple square, octagonal, or circular spiraling turns form their coils. The top metal layer is favored for its lower parasitic capacitance to the substrate, resulting in a higher self-resonance frequency, which indicates the frequency above which the inductor ceases to be effective. The top metal layer also benefits from a larger thickness than lower metal layers, reducing resistive losses. The choice of geometry is mainly based on loss and area efficiency considerations. Square spirals offer the densest inductance per area, while octagonal or circular spirals are considered when foundry design rules or CAD tools do not support circular shapes. In practice, "area" refers to the

smallest rectangular area encompassing the structure, as corner areas enclosing a spiral represent wasted space.

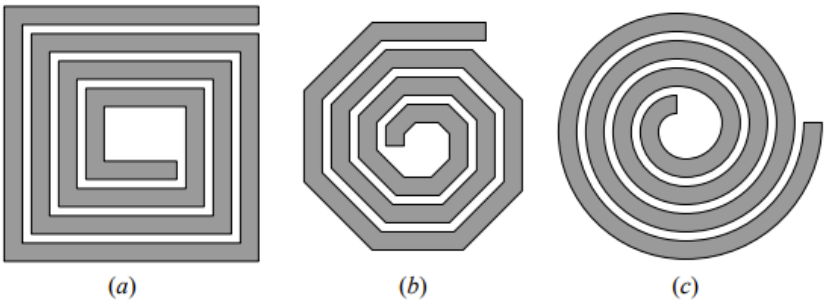

Figure 7: Typical integrated inductors: (a) square, (b) octagonal, and (c) circular spirals.

Circular spirals provide a higher quality factor Q [11]. When circular shapes are not supported, octagonal spirals become the next best alternative. To increase inductance within a given area, one could add more turns until the space is completely filled. However, loss constraints usually limit this approach, as inner turns contribute little to inductance and introduce significant loss. As a result, spiral inductors are seldom filled to their maximum number of turns, and increasing inductance is typically achieved by expanding the coil's radius. To boost inductance without sacrificing area efficiency, an approach is to connect additional turns (of similar dimensions) on other metal layers in series. An alternative to enhance the quality factor Q is to connect multiple metal layers in parallel, thereby reducing the series resistance of the coil. However, this method brings the coil closer to the substrate, lowering its self-resonance. In most cases, this tradeoff is considered acceptable.

Another technique widely used is a differential structure, as depicted in Figure 8. In differential circuits that would otherwise require two single-ended inductors, using a single differential inductor with twice the inductance results in a more compact layout. Additionally, the differential structure suppresses common- or even-mode capacitive parasitics and their associated losses [12]. These benefits can improve the self-resonance frequency and quality factor Q, making this configuration a popular choice.

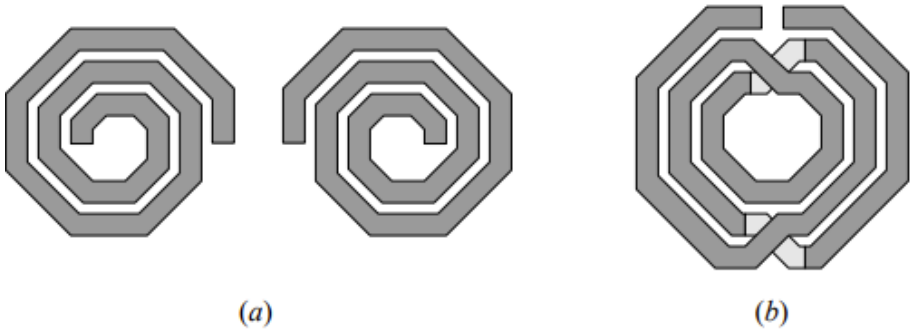

Figure 8: A pair of single-ended inductors (a) and a differential inductor (b) with similar total inductance.

4.4.3 MOS varactors

Varactors serve as voltage-controlled capacitors and find common application in voltage-controlled oscillators (VCOs), parametric amplifiers, and frequency multipliers. These devices are operated in a reverse-biased state, ensuring that no DC current flows through them.

There are three types of varactors that control the capacitance of the tank: analog varactors (Cvar), switch capacitor arrays (Cswitch), and programmable varactors (Cprog). The analog varactor, Cvar, is directly tuned by an analog tuning voltage, VCOn, with a voltage range typically between 0.1V and 0.8V. It plays a crucial role in generating a single frequency curve within the tuning range. Switch capacitor arrays, or digitally tuned varactors (Cswitch), offer two distinct states —maximum and minimum capacitance— individually controlled by digital inputs. These inputs can either be set to 0V for minimum capacitance or VDD for maximum capacitance. By modifying the control voltage applied to any of these varactors, the Voltage-Controlled Oscillator (VCO) shifts to the corresponding tuning curve. The final type of varactor is the programmable varactor (Cprog). To adjust the tuning voltage for each unit of Cprog, a 2:1 multiplexer is utilized, featuring two inputs: VDD and VCOn. The outputs of these multiplexers are determined by select signals, which are supplied by the control circuit [17].

During the last decade, due to the proliferation of nanoscale CMOS technologies, the AMOS varactor has become the most popular variable capacitance device.

AMOS varactors also operate in a reverse-biased state to prevent DC current flow. The cross-section through the device of an AMOS varactor is illustrated in Figure 9 [21]. These varactors leverage the MOS transistor's structure, where connecting drain (D), source (S), and bulk (B) together creates an MOS capacitor with a capacitance value dependent on the voltage between bulk (B) and gate (G) V_{GB} [18]. This form the ratio of C_{max} and C_{min}, capacitance always present in the circuit whether the channel is on or off. Due to the limitations of achieving a high capacitance ratio in deep submicron technology of diode varactor, MOS varactors are commonly used as tuning element in LC VCOs. MOS varactors can be constructed using either NMOS or PMOS technology, operating in three modes:

- accumulation mode
- depletion mode
- inversion mode

When the gate electrode operates with a positive voltage, the varactor is in accumulation mode. Conversely, a negative gate voltage places the varactor in depletion mode. This variety is known as an AMOS varactor, offering a higher quality factor but limited tuning range. The inversion mode of a varactor is achieved by connecting the source and drain terminals to create a unified capacitor terminal. In the case of the IMOS (Inversion MOS) type, the bulk terminal is connected to the supply voltage VDD for PMOS and to ground for NMOS [19].

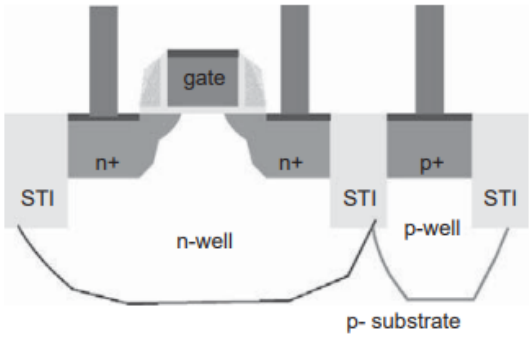

Figure 9: AMOS n-type varactor.

4.4.4 Tuning range

The frequency tuning range is an important specification for LC-VCOs. Monolithic LC-tank VCOs require the integration of high-quality passive devices, such as inductors and varactors, in inherently lossy CMOS technology. Designing them becomes more challenging when a wide tuning range is necessary to cover the required frequency band across process tolerances. Combining a wide tuning range with a low power supply voltage (i.e., a low tuning voltage range) necessitates a high VCO gain (in MHz/V), which makes the oscillator more sensitive to voltage-induced phase noise.

KVCO, or VCO gain, is a critical parameter in VCO design that quantifies the sensitivity of the VCO's output frequency to variations in the control voltage (eq 4.10). There is an interplay between KVCO and varactors; a higher KVCO will result in a wider tuning range because the VCO is more responsive to changes in voltage. Conversely, a larger tuning range can be achieved by using varactors with a high capacitance range or voltage swing. This interaction highlights the delicate balance in designing VCOs to achieve the desired frequency agility while maintaining stability and performance in various applications.

$$KVCO = \frac{df}{dVtune} \quad (4.9)$$

It is well known that an important tradeoff in VCOs is the one between phase noise and the tuning range, which is the ratio between the frequency range covered by the VCO and the average value of this range. In several applications, the required tuning range can easily exceed 20%. A large tuning range has an indirect, detrimental impact on phase noise. One reason is that, in a varactor, a large capacitance variation is often traded with the quality factor and thus with phase noise.

To achieve a wide tuning range while maintaining a low VCO tuning gain, designers often use a large number of digitally controlled switched capacitors to divide the tuning range into multiple low-gain frequency bands. In the technology used, Accumulation Mode NMOS varactors (AMOS) are the only choice available for implementing the switched tank capacitors.

The oscillation frequency of VCO is determined by the tank inductor and capacitor, thus changing either of them could change the oscillation frequency. However, in practical, inductor is difficult to be varied continuously. The tuning range of a VCO is defined as:

$$TR(\%) = \frac{\Delta f}{f_{center}} * 100 \quad (4.10)$$

where Δf = f_{max} - f_{min} , f_{center} = (f_{max} + f_{min})/2. If the inductor is fixed, f_{max} and f_{min} are determined by the minimum and maximum capacitance's of varactor. It should be noted that the parasitic capacitance of transistors will contribute to the capacitance of LC-tank and degrade the tuning range. This situation will become even worse at mm-wave frequency, because the increasing transistors size to sustain oscillation at such a high frequency will inevitably increase the transistors parasitic capacitance, which will further limit the frequency tuning range. In Figure 10, Cmax refers to the maximum capacitance, which occurs when the varactor is in accumulation mode. In this mode, the varactor exhibits its highest capacitance, often close to the gate oxide capacitance. Cmin represents the minimum capacitance, which is achieved when the varactor is in deep inversion mode. This state corresponds to the lowest capacitance, typically associated with the depletion capacitance (Cdep) when it reaches its minimum value.

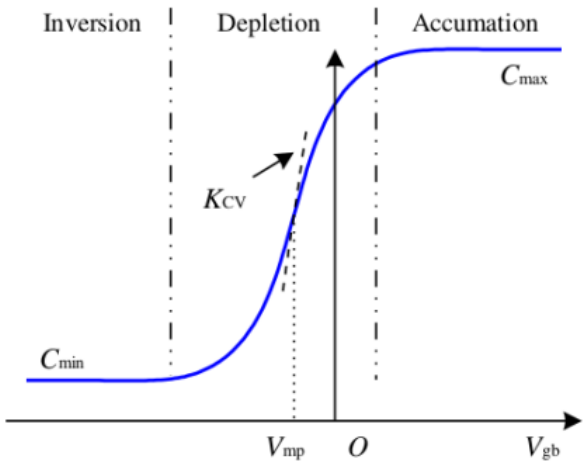

Figure 10: CV dependency of a nfet in n-well.

5 Noise in oscillators

5.1 Noise definition

Noise in oscillators refers to the unwanted and random fluctuations in the output signal's amplitude, frequency, and phase. It introduces variations in the output waveform that deviate from the ideal sinusoidal waveform, and it can impact the stability, accuracy, and quality of the oscillator's performance. Noise can originate from various sources within the oscillator's components, circuitry, and environment, thus noise can be internal or external. As internal noise can be considered thermal noise, flicker noise and phase noise etc. while a few types of external noise are electromagnetic interference (EMI), radio frequency interference (RFI), power supply noise, cross-talk noise etc.

5.2 Phase noise

Phase noise is a critical parameter in oscillators and plays a significant role in determining the stability and spectral purity of the output signal, thus it's probably the most important specification of a VCO. It is a measure of the short-term random fluctuations in frequency f and phase φ, typically expressed in decibels relative to the carrier signal's power at a specific frequency offset from the carrier. In a wireless system, the presence of phase noise in the oscillator can lead to the unwanted mixing of signals from nearby communication channels during the downconversion process [21]. This can result in a reduction in receiver sensitivity, impairing the system's ability to distinguish and decode signals effectively. Furthermore, it sets a constraint on how closely the communication channels can be allocated in terms of frequency spacing. Even in the realm of digital technology, we must recognize the significance of phase noise, which often manifests as jitter. Jitter in a clock signal has a direct impact on timing margins, ultimately influencing the overall performance of a system. It plays a crucial role in determining how efficiently a system operates [22].

The output of an ideal oscillator is an ideal sinusoidal signal and is given by the following form:

$$V_{out}(t) = V_0 cos[2\pi f_0 t + \varphi] \quad (5.1)$$

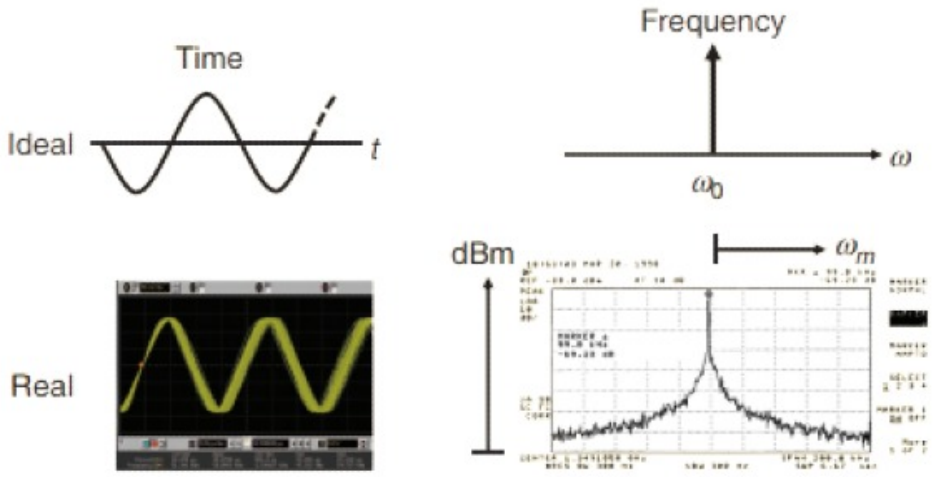

Figure 11: The impact of noise: ideal versus real in time domain (jitter) (a) and frequency domain (phase noise) (b)

with constant amplitude V_0, center frequency f_0, and a fixed phase φ. In the time domain, when multiple waveforms that were initially synchronized overlap, a phenomenon occurs at the zero-crossing point. This phenomenon is known as time jitter, which can be likened to a phase error [23]. Over time, the variability of this phase error increases proportionally, as illustrated in the Figure 11(a). In the frequency domain, it should be a single impulse, but when we analyze the spectrum, we observe symmetrical tails that decrease as we move away from the central angular frequency, denoted as ω_0 as illustrated in the figure 11 (b). These tails are commonly referred to as the phase noise of the oscillator. Thus, a real oscillator signal is given by :

$$V_{out}(t) = V_0(t)cos[2\pi f_0 t + \varphi(t)] \quad (5.2)$$

The phase noise is the signal sideband noise spectral density in a unit bandwidth at an offset of Δ_f from the center frequency f_0 divided by the carrier signal

power. It is defined as:

$$L_{total}(\Delta_f) = 10log[\frac{P_{sideband}(f_0 + \Delta_f, 1Hz)}{P_{carrier}}](dBc/Hz) \quad (5.3)$$

The above definition includes the effect of both amplitude and phase fluctuations, $V_0(t)$ and $\varphi(t)$.Its disadvantage of this definition above is that it shows the sum of both amplitude and phase variations; it does not show them separately. One limitation of this approach is that it combines both amplitude and phase variations, making it challenging to differentiate between them. However, it's crucial to distinguish between amplitude and phase noise because they have distinct effects within the circuit. For example, amplitude noise can be mitigated by implementing amplitude limiting mechanisms and practically eliminated by using a limiter on the output signal. In contrast, phase noise cannot be addressed in the same straightforward manner [24]. Therefore, in most applications, $L_{total}(\Delta_f)$ is dominated by its phase portion $L_{phase}(\Delta_f)$, known as phase noise, which we will simply denote as $L_{total}(\Delta_f)$.

In the past decade, numerous simulation techniques have emerged for precisely modeling oscillator phase noise. However, there's a pressing need for an analytical model that establishes a connection between the phase noise of a Voltage-Controlled Oscillator (VCO) and crucial factors like transistor bias current, transistor size, and the values of resonator components. This analytical description of oscillator phase noise is essential for guiding the design process. It's worth noting that accurately characterizing phase noise analytically remains one of the most formidable challenges in the realm of electronic circuit analysis and design.

The semi-empirical model introduced in references [25], also known as Leeson's phase noise model, was the first simple and intuitive VCO phase model that was developed. It relies on the assumption of linearity and time-invariance (LTI), specifically tailored for tuned tank oscillators (eq 4.4).

$$L(\Delta_f) = 10\ log\ [\frac{2FKT}{P_s}\ [1 + (\frac{f_0}{2Q\Delta_f})^2]\ (1 + \frac{\Delta f_{\frac{1}{f^3}}}{|\Delta f|})\ ] \quad (5.4)$$

where K is the Boltzmann constant, F is an empirical parameter (often called the "device excess noise number"), T is the temperature, f_0 is the oscillation frequency, Δf is frequency offset, $\Delta f_{\frac{1}{f^3}}$ is the corner frequency between $1/f^3$ and

$1/f^2$ phase noise regions as illustrated in Figure 12, P_s is the power of carrier signal, and Q is the Quality factor of the LC-tank. Figure 12 plots a general phase noise based on Leeson's phase noise model. There are three regions: $1/f^3$ region, $1/f^2$ region, and flat noise floor region. The phase noise in $1/f^3$ region is declined in a slope of -30 dB/decade, and is mainly contributed by amplitude modulation (AM) – phase modulation (PM) noise and flicker noise. The $1/f^2$ region is between the $1/f^3$ region and noise floor, and roles off with -20 dB/decade. The flat noise floor at large frequency offset is mainly contributed by thermal noise.

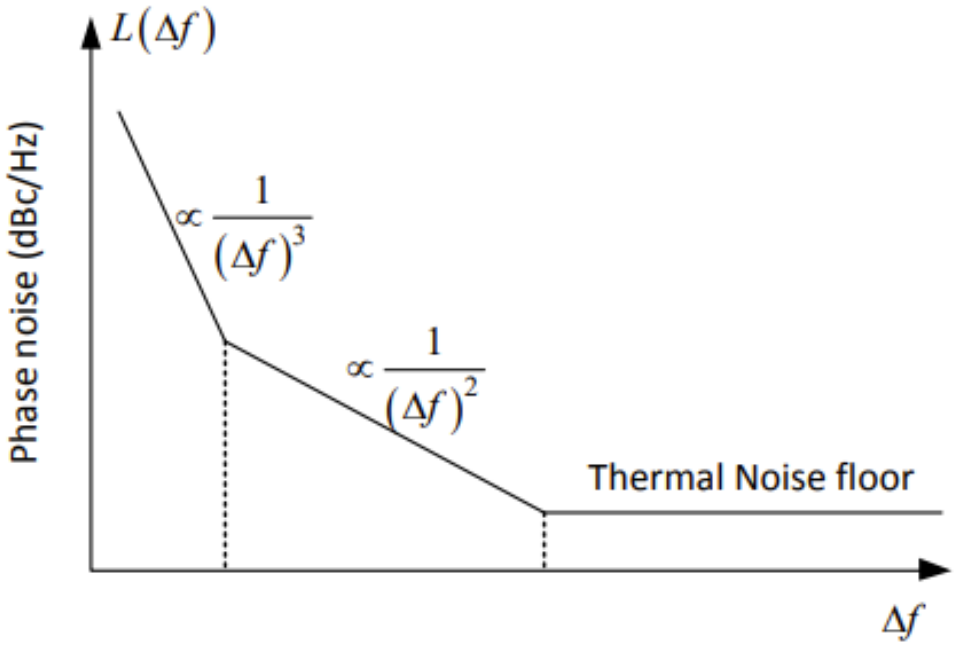

Figure 12: Typical phase noise vs. offset frequency.

5.3 Thermal noise

The most significant type of noise encountered in electronics is thermal noise, commonly known as Johnson-Nyquist noise. Thermal noise arises from the random motion of charges in various components, including resistors, transmission

lines, diodes, transistors and also can arise from inductors and capacitors due to their resistive (parasitical) parts. It is characterized as white noise because its power spectral density (PSD) remains relatively uniform across the frequency spectrum. When considered within a finite bandwidth, thermal noise exhibits an almost Gaussian amplitude distribution [26]. Mitigating thermal noise can be challenging due to its inherently random nature, making it difficult to precisely predict the noise levels in a system. However, it is essential to note that cancellation and filtering processes, such as employing low-noise amplifiers and filters, are effective in reducing its impact. To mitigate thermal noise in a circuit, it's crucial to carefully choose the right components and pay close attention to their sizing, biasing, and board layout. Factors like grounding, component placement, power supply management, decoupling, and impedance matching all play essential roles in reducing the impact of thermal noise.

The power of thermal noise primarily depends on temperature and bandwidth, with higher temperatures and wider bandwidths leading to increased thermal noise levels. Designers and engineers carefully consider these factors when designing electronic systems, as thermal noise can limit sensitivity and performance, especially in applications where a high signal-to-noise ratio (SNR) is critical, such as communication systems, medical devices, and scientific instruments.

It's also worth mentioning that in addition to thermal noise, electronic systems can experience other forms of noise, such as shot noise and flicker noise, which may require specialized mitigation techniques. While impedance matching plays a valuable role in minimizing signal reflections and optimizing power transfer, it does not directly influence the level of thermal noise. Instead, thermal noise combines with other sources of noise within the circuit, contributing to the overall noise in the system. The frequency independent value of thermal noise is [28]:

$$S_v = 4\ K_B\ T\ R \quad (5.5)$$

where K_B is the Boltzmann constant equal to $1.38 * 10^{-23}$ JK^{-1}, T is the absolute temperature and R is the resistance. The thermal noise unit of S_v is V^2/Hz.

5.4 Flicker noise

The quality and reliability of information transfer are significantly influenced by the phase noise of Voltage-Controlled Oscillators, making it a critical parameter. To meet stringent low-phase-noise requirements, integrated passive LC-VCOs often emerge as the preferred choice, as suggested in [20].

Within the phase-noise spectrum, the $1/f^2$-shaped component primarily arises from upconverted white noise generated by the parasitic resistance in the VCO's tank circuit. Furthermore, flicker noise, commonly known as 1/f noise, earns its name from its distinctive spectral density curve, where noise power decreases inversely with frequency, setting it apart from other noise forms like white noise. The comprehensive understanding of flicker noise only materialized with the introduction of the Impulse Sensitivity Function (ISF) by Hajimiri and Lee in 1998 [28]. Flicker noise originates from various sources within electronic components, encompassing semiconductor devices, transistors, and occasionally resistors. Typically, MOSFET transistors exhibit lower flicker noise levels than bipolar transistors, with PMOS transistors typically demonstrating superior noise characteristics to NMOS transistors, offering a rationale for considering PMOS transistors in VCO topologies. Notably, flicker noise's significance is pronounced at lower frequencies, typically below 1 MHz (Voinigescu). However, even at higher frequencies, the effect of flicker noise cannot be ignored and remains substantial, as nonlinearity and time variance in circuits, such as mixers and oscillators, result in the upconversion of flicker noise to a $1/f^3$-shaped phase noise, near the carrier frequency. Flicker noise sources will be up-converted to AM noise, and then go into phase noise by amplitude-modulation-to-phase-modulation (AM-PM) conversion of varactors and capacitors dependent on voltage [29]. Consequently, this upconversion process leads to phase noise components beyond the fundamental oscillator frequency, detrimentally affecting the oscillator's spectral purity and frequency stability.

The mechanism behind flicker-noise upconversion can be elucidated as follows: Flicker noise originating from the tail current source, when introduced to the LC-tank, undergoes upconversion due to the mixing actions within the VCO circuit. Furthermore, in an unbalanced single differential oscillator circuit, the common-mode node of the current source oscillates at twice the oscillator center frequency, $2\omega_0$, resulting from the switching of NMOS transistors. Through channel length modulation, the noise from the tail current source is upconverted to $2\omega_0$, subsequently entering the LC-tank and engaging in spectral mixing with the fundamental oscillator frequency. This results in phase-noise sidebands emerging above the oscillator frequency.

To mitigate flicker noise's upconversion from the tail current source, it is imperative to suppress all even harmonics, necessitating a circuit design that maximizes symmetry [30]. Recent trends have seen the replacement of the tail current source with a digitally controlled tail resistor, effectively eliminating the 1/f noise contribution while ensuring PVT robustness. This category of voltage-biased oscillators not only achieves noise reduction but also facilitates low-supply operation by obviating the need for a tail resistor [31].

5.5 Spot noise

Another common way of representing phase noise measurement results is referred to as 'spot noise'. Spot noise refers to the measurement of phase noise at specific frequency offsets. By default, these offsets are usually decade values, which are powers of 10, such as 1 kHz, 10 kHz, 100 kHz, etc. It is also possible to measure spot noise at arbitrary user-defined offsets. Spot noise data is often presented in tabular form and is frequently used to confirm that the phase noise at a particular offset is below a specified threshold.

6 LC-VCO topologies

There are several topologies aimed at realizing the active pair that generates a negative resistance which is required to sustain oscillation in a VCO. The selection of an active pair topology usually depends on the specifications of a particular VCO design, and may also depend on process technology. In other words, the designer must evaluate given restrictions on phase noise, power consumption, tuning range and other VCO parameters, and choose the topology that best accommodates the most vital specifications.

6.1 Cross-coupled LC VCO

A succinct explanation of the LC tank VCO follows, emphasizing its superior performance regarding normalized phase noise when compared to other fully integrated structures such as ring oscillators, relaxation oscillators, multivibrators, and gm-C oscillators. In most RF oscillators, an LC tank, serving as a resonator, is an integral part of the VCO's feedback loop, ensuring frequency stability. The quality of an LC tank VCO is inherently tied to the LC tank itself, a factor directly influencing the oscillator's quality factor. Ideally, an optimal VCO would feature an infinite-Q LC tank, yet, in practical CMOS standard processes, inductors tend to exhibit lower Q values. To address this, the introduction of negative resistance becomes necessary to maintain energy replenishment and sustain oscillations. In a basic RLC circuit, current consumption is inversely proportional to inductance value, underscoring the importance of achieving the highest possible Q for the inductor to achieve superior VCO phase noise performance while minimizing power dissipation. The Q value is process-dependent, with inductance value influenced by node capacitance and the required oscillation frequency. This balance effectively addresses phase noise and power dissipation for a given frequency in a specific process.

CMOS technology, recognized for its low power consumption, comes at the trade-off of reduced noise immunity and performance. For more than three decades, CMOS devices were scaled; later, this approach was replaced by single NMOS or PMOS transistors, offering improved noise immunity, reduced power consumption, and enhanced circuit robustness [32]. NMOS transistors are celebrated for their high-speed switching capabilities and excellence in logic gates, making them indispensable for energy-efficient digital systems. In contrast, PMOS transistors, although typically slower, are preferred in applications where minimizing phase noise is paramount, particularly in RF and wireless communication systems. These

transistors exhibit varying carrier mobility in the channel, a fundamental parameter influencing MOSFET operation, determining current drive, transconductance, and transistor speed [33]. The first topology utilizes PMOS transistors instead of NMOS transistors as cross-coupled pair to provide negative resistance (Figure 13 (a)).

Within VCOs, NMOS and PMOS transistors operate in cross-coupled pairs, fostering a dynamic interplay. NMOS transistors oversee the charging of the resonating tank circuit, while PMOS transistors manage the discharging process. This push-pull arrangement plays a crucial role in generating the oscillatory behavior necessary for frequency synthesis in VCOs. For Nmos device, when a voltage is applied to the gate (usually VDD), it creates an electric field, depleting the channel of electrons and forming a conductive path between the source and drain, It is in the "on" state, allowing current to flow. PMOS transistors are typically "on" when a negative voltage (usually VSS) is applied to the gate terminal. Applying voltage causes "holes" to flow from the source to the drain. Understanding the intricacies of NMOS and PMOS transistor interaction in VCOs is essential for optimizing phase noise performance and power consumption, making them pivotal components in modern semiconductor technology, particularly in wireless and RF applications where phase-locked loops and frequency synthesis are essential for system functionality.

In an alternative topology as illustrated in Figure 13 (b), both NMOS and PMOS transistors are utilized in cross-coupled pairs to generate negative resistance. This configuration offers a reduction in power consumption when the need for negative resistance remains consistent. However, it's essential to note that the voltage swing is confined to the supply voltage range. While PMOS-only cross-coupled LC-VCOs and complementary LC-VCOs deliver favorable phase noise and improved power performance, an increase in the width of PMOS transistors leads to elevated parasitic capacitance, introducing design challenges in mm-wave VCOs. Noise originating from the bias current source can disrupt the voltage at the common source node of the cross-coupled pair and modulate with the oscillation frequency of the nonlinear VCO, resulting in a degradation of close-in phase noise. One potential modification involves eliminating the bias current source, as depicted in the Figure 14 . This topology omits the use of a current source, allowing for a larger signal swing and eliminating noise associated with the current source. However, it's vital to be aware that the absence of a current source can heighten the oscillator's sensitivity to power supply variations.

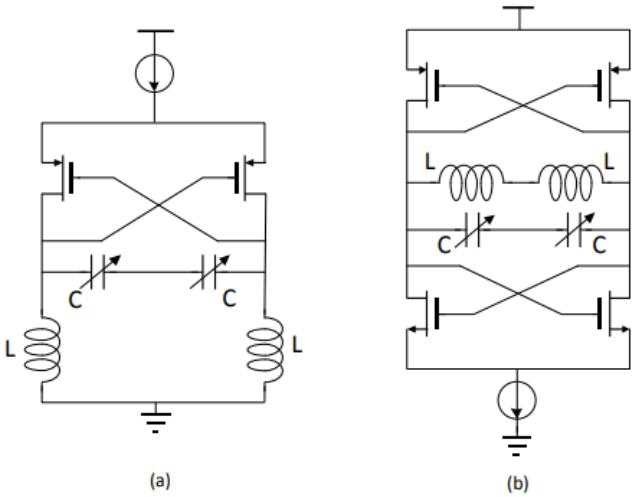

Figure 13: A pmos cross-coupled LC-VCO (a),a complementary LC-VCO with current source to ground (b).

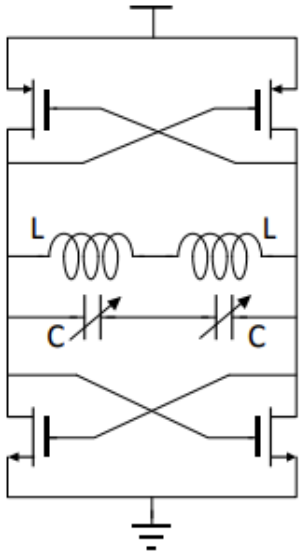

Figure 14: A modification of complementary LC-VCO which omits the use of a bias current source.

6.1.1 Transformer techniques

Transformer-based feedback technique can be applied to cross-coupled LC-VCO to enhance the voltage swing of oscillator and improve the phase noise. Figure 15 (a) shows an LC-VCO with transformer-based drain-to-source feedback [34]. This topology allows for the drain voltage to be higher than VDD and the source voltage to be lower than GND. Since the drain voltage is in phase with source voltage, the oscillation amplitude can be enhanced. Consequently, the phase noise would be reduced. In Figure 15 (b), we observe an alternative topology of an LC-VCO employing transformer-based feedback. In this configuration, the NMOS transistors are cross-coupled via the transformer-based drain-to-gate feedback. It will bring an advantage that the gate and drain of transistors can be separately biased in DC. By properly design the turn ratio of transformer, the voltage swing at the gate of transistor can be much smaller than that at the drain. Hence, the voltage swing of VCO output could be increased for same bias current, resulting in an improvement of phase noise.

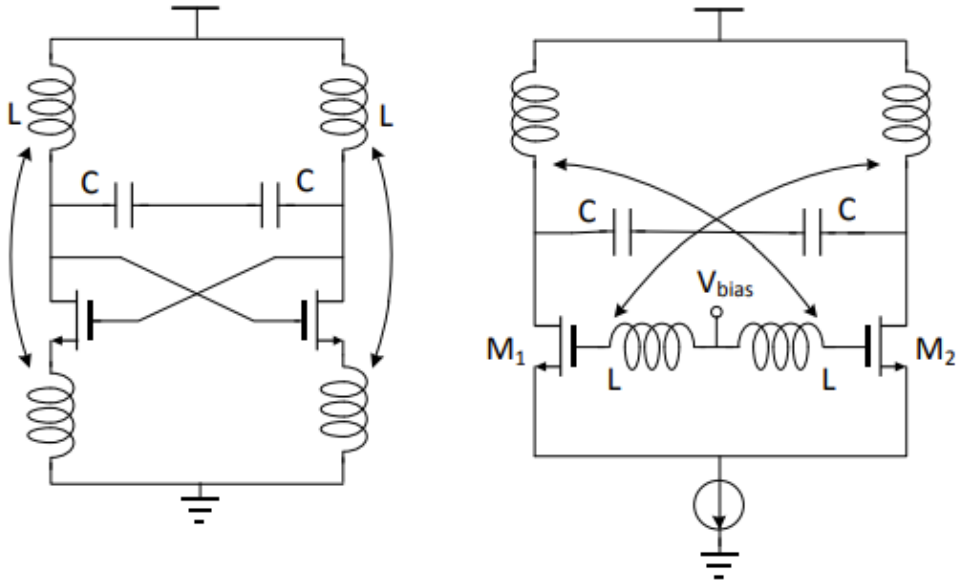

Figure 15: LC-VCOs with transformer-based feedback (a) drain-to-source feedback, and (b) drain to-gate feedback.

6.2 Quadrature LC VCO

Quadrature oscillators are valuable components in communication systems, particularly in modulation schemes that rely on both in-phase and quadrature components for easy demodulation. These oscillators are engineered to produce outputs with a 90° phase difference, facilitating seamless signal processing.

The fundamental principle behind creating quadrature oscillators involves coupling two identical oscillators in such a way that they operate with a 90° phase shift. The underlying concept is that by introducing a signal with the same frequency into an oscillator, we can precisely alter the phase of the oscillator's output. However, the goal is to inject only a fraction of each oscillator's output into the other. As discussed in [35], by ensuring that the transconductance of the injection mechanisms is both equal and opposite, effectively creating anti-phase coupling, we can achieve the desired outcome of having the outputs of the two VCOs precisely 90° out of phase.

In Figure 16, the injection mechanism consists of a DC-biased NFET current source and an NFET device, with its drain connected to one of the outputs of the other VCO. This injection mechanism is applied to each of the VCOs' outputs. This single-ended design offers improved isolation between the VCO outputs when compared to a differential injection mechanism, albeit with a slightly higher power consumption. The outputs of the injection mechanism, denoted as Vout1 and Vout2, are then connected to the tank outputs of the second VCO, as illustrated in Figure .

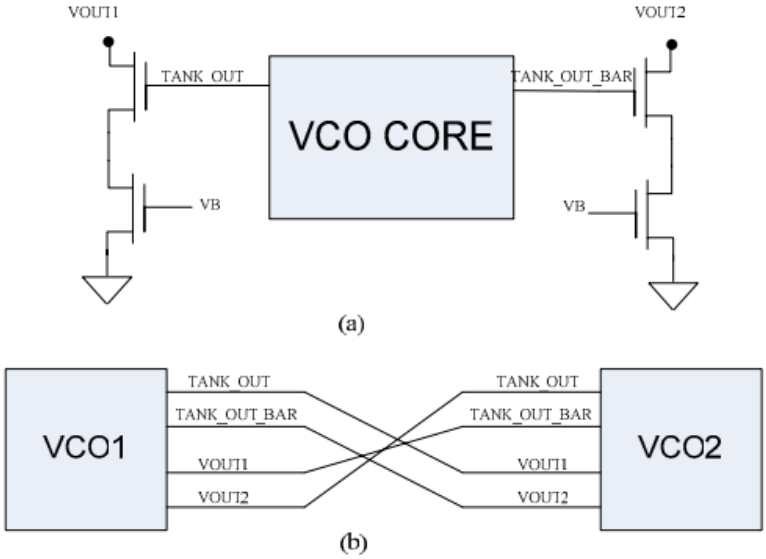

Figure 16: Quadrature VCO injection mechanism (a), quadrature VCO injection topology (b)

6.3 Selective feedback oscillators

Selective feedback oscillators are a class of electronic oscillators designed to generate stable and precise frequencies for various applications. They utilize selective feedback components to achieve precise frequency control and improved spectral purity compared to simple LC tank oscillators. One key distinction among selective feedback oscillators is the specific feedback network used, which can include resonators, crystal filters, or surface acoustic wave (SAW) devices. Crystal oscillators, for instance, rely on the high Q-factor and temperature stability of crystal resonators, offering exceptional frequency accuracy. SAW oscillators utilize surface acoustic wave devices as a feedback element, providing good phase noise performance.

Armstrong, Hartley, Colpitts, Clapp, and Pierce oscillators represent distinct oscillator architectures that fall under the category of selective feedback oscillators, typically realized using transformers, inductors, and capacitors [21]. Each of these designs employs unique feedback networks to achieve precise frequency control and improved spectral purity when compared to basic LC tank oscillators.

Armstrong oscillators utilize a super-regenerative feedback mechanism to generate high-frequency signals with minimal components, making them suitable for early radio communication applications. The Hartley oscillator employs an inductive-capacitive feedback network, providing good frequency stability and simplicity, which is ideal for low-frequency applications.

Colpitts oscillators incorporate a capacitive voltage divider in their feedback network, offering a wide frequency tuning range and are commonly used in RF and audio frequency generation. An extended version, the Clapp oscillator, adds an additional capacitor in series with the inductor for improved frequency stability, making it a popular choice for crystal oscillators. Lastly, the Pierce oscillator utilizes a quartz crystal as a frequency-determining element, ensuring exceptional frequency accuracy and stability, often used in applications demanding precise timekeeping.

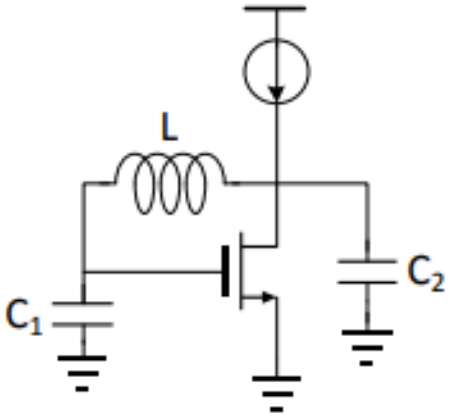

Figure 17: A traditional Colpitts oscillator.

The most common topology among these designs is the one invented by Canadian-born Edwin Colpitts as illustated in Figure 17. Due to their non-differential structure, single-ended Colpitts VCOs were rarely adopted as integrated circuits. In contrast, the differential common gate and common drain Colpitts oscillator topologies are shown in Figure 18 and 19 [36]. The differential Colpitts oscillator exhibits good close-in phase noise. However, it is worth noting that the poor start-up characteristics may require higher power dissipation. The Colpitts LC-VCO

is particularly promising for high-frequency applications due to its superior phase noise performance and tuning range at a given bias current [37].

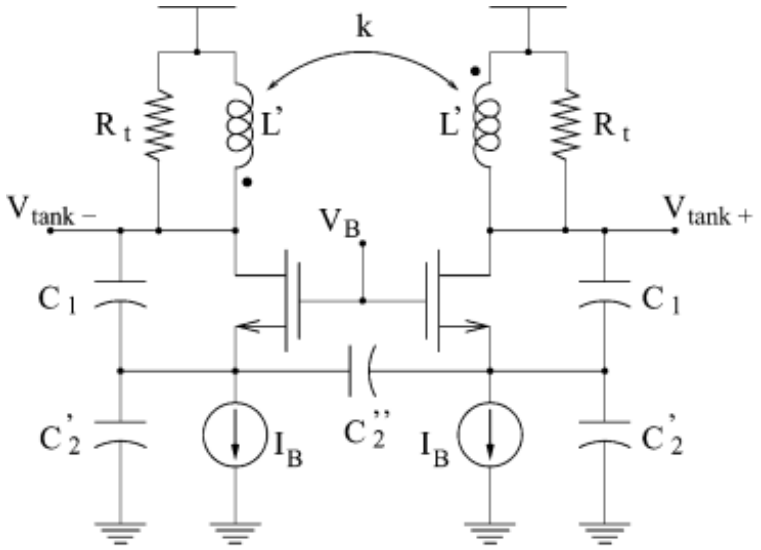

Figure 18: Differential common gate Colpitts oscillator.

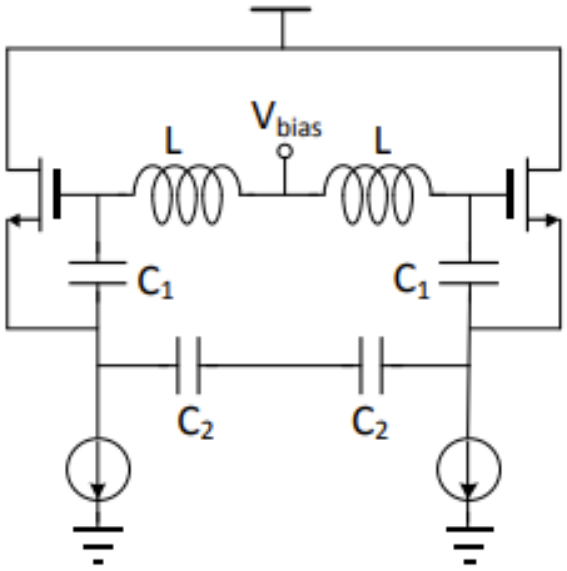

Figure 19: Differential common drain Colpitts oscillator.

7 VCO design

Voltage-Controlled Oscillators (VCOs) stand as crucial components in RF communication systems, with their significance underscored by the demand for achieving good phase noise, wide tuning range and low power consumption. Meeting the stringent requirements for spectral purity in oscillators has prompted numerous endeavors to enhance the phase noise performance of integrated LC VCOs, leading to a wealth of research papers [40], [41], [42]. The reported methods for achieving low phase noise can be summarized as follows: maximizing the Quality factor of the LC-tank and maximizing oscillation amplitudes. For the first one, it has been mentioned in a previous chapter, and it will also be mentioned in subsequent ones that follow. Regarding the second one, we know that phase noise is equal to the ratio between Pnoise and Psignal, as illustrated in the eq. 7.1. Thus, maximizing the oscillation amplitude can decrease the phase noise at all offsets. This can be achieved by either increasing the biasing current or raising the tank inductance (assuming a constant tank quality factor). However, these approaches come with trade-offs; for example, augmenting biasing current results in higher power consumption. Despite these efforts, the design and optimization of integrated LC VCOs continue to pose challenges for circuit designers, as it necessitates the simultaneous optimization of multiple variables.

$$PN(db) = log(Pnoise) - log(Psignal) \quad (7.1)$$

While numerous phase noise models have been developed for various oscillator types, each is built on assumptions that are only applicable to specific classes of oscillators. Most of these models are grounded in the assumption of a linear time-invariant (LTI) system, but they often fall short by not fully considering the mechanism through which electrical noise sources, such as device noise, translate into phase noise. Consequently, these models struggle to make accurate predictions about phase noise in oscillators, given that any oscillator is inherently a periodically time-varying system. So considering everything mentioned above, limitations arise due to the fact that the VCO is a large signal non-linear circuit.

The VCO core in this work, is based on a standard LC -tuned cross-coupled NMOS topology, chosen primarily for its ability to achieve low phase noise combined with a wide tuning range. The design features a transformer with differing values between the primary and secondary coils, with the maximum value as-

signed to the drain. In addition, a constant capacitor was linked to the drain, PCAP varactors at the gate, and the design was finalized by incorporating a capacitor bank at the gate. To refine these connections, corresponding adjustments were implemented, leading to the selection of the most effective options for the final implementation. Figure 20 shows a simplified schematic of the VCO core.

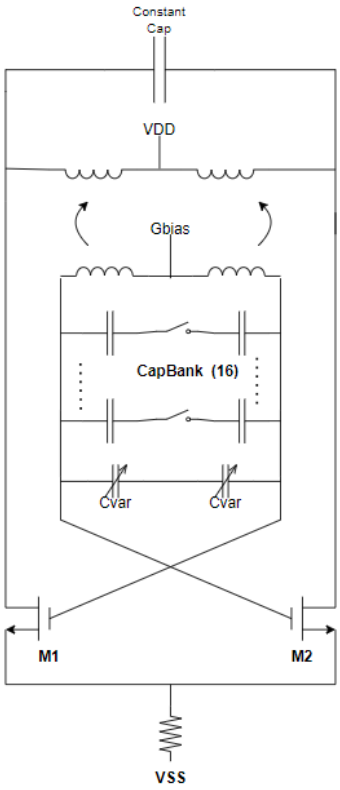

Figure 20: Simplified schematic of the VCO core.

The primary and crucial aspect of the design concerns the biasing of the devices. In this work, NMOS transistors, specifically the egulvtnfet-mmw-6t, were chosen. Given the VCO's significant voltage swings at the output, these particular devices were selected for their capability to withstand such swings while at the same time delivering optimal phase noise. These devices, characterized by their small size with a length reaching 70nm, permit a supply voltage of 1.2V with a $\pm 10\%$ difference. Additionally, they feature low Vthreshold and generally exhibit higher transconductance (gm) compared to other transistors, contributing to improved loop gain in the design. However, the primary criterion for device selection was the minimization of noise in the circuit.

The total width of each NMOS device in the design reach the value of 234.1 um. To circumvent an excessively large width and manage the resultant internal resistance, nine parallel transistors were incorporated, using the multiplier capability provided by Cadence. Generally, Vgate is determined by the optimal biasing for noise. However, in this work, the varactor played a crucial role in determining the final value of Vgate. Therefore, a biasing scheme in the circuit had to be implemented that works effectively with the varactor, which, as we will see later, is connected to the gate. This configuration needed to achieve a very good gain, KVCO. To ensure that the KVCO falls within the range of Vtune values in the circuit and achieves the optimal pick in its waveform, the ideal value following parametric simulations was approximately 0.3V, Vgate = 0.3V. However, applying 0.3V to the gate voltage resulted in a negative loop gain, resulting in no oscillation. So, the next value identified as the most effective for achieving good performance in the design was Vgate = 0.5V.

For the Vgate value, a voltage divider was implemented, as illustrated in Figure 21. Initially, the voltage divider employed very small resistances, specifically R1=405Ω and R2=600Ω. However, it was observed that thermal noise was not adequately filtered through the RC filter. As a result, the final values for resistances R1 and R2, to achieve a 500mV value at Gbias (eq 7.2), were determined as 405.4KΩ and 600KΩ, respectively. Both capacitors in this configuration have a value of 180pF. In general, capacitor values above 200pF can sometimes cause layout issues where there might not be sufficient space for placement. Therefore, it is advisable to use a relatively smaller value, less than 200pF.

$$Gbias = \frac{R1}{R1 + R2} * VDD \quad (7.2)$$

	Length(m)	Total Width(um)	Multipliers
egulvtnfet mmw6t(M1—M2)	70n	26	9
Constant Cap	2u	9.6	5

Table 1: Size realization.

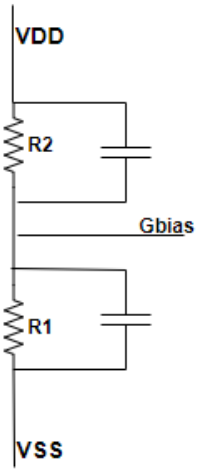

Figure 21: Voltage divider for Gbias.

Note: The choice for the length of the devices was made as follows. The value of 70nm represents the minimum possible length for this specific device. The goal in implementing this VCO was to achieve the best possible loop gain. Therefore, the length had to remain constant because if the length value is increased, the Ron resistance increases, and therefore the transconductance decreases. The gm is proportional to the loop gain, so as gm decreases, the loop gain also decreases. This particular transistor is a millimeter-wave device. In general, there are three types of transistors: basic transistors, RF transistors, and millimeter-wave (mmW) transistors. As the oscillation frequency increases, in addition to the standard parasitic capacitance's (e.g., Cgs, Cds, etc.) of the transistor, the parasitic capacitances between the metals become significant. For this reason, we employ mmW transistors, as they are designed with these extra parasitic capacitances of metals, making the circuit more realistic. Finally, the 6t of the devices symbolizes six terminals, which are as follows: source, drain, gate, bulk, sub and nwell.

7.1 Design steps

After selecting the devices, the next step was to determine a size for them. Since the length remained constant, along with the power supply voltage at 1.24 V, the only variable for the device was the width. According to theory, while a larger total width generally leads to increased power consumption, higher Idc, contribute to improved loop gain. However, larger transistor size implies the creation of additional parasitic capacitance's, which in turn, affect the overall capacitance of the tank and thereby affecting the output frequency. Therefore, choosing the final size involved numerous simulations, taking into consideration all the influencing factors. Next, the LC tank needed to be created. Initially, a model transformer was introduced in parallel with a capacitor to allow the circuit to reach a frequency close to 10GHz, with values chosen from equation 3.2. At this point, simulations provided by Cadence Virtuoso were initiated, and these simulations continued throughout the design process, including DC, stability (STB), harmonic balance (HB), and HB noise simulations.

Among these, the most crucial is the DC analysis. Regardless of how any circuit is designed, it must undergo a DC analysis. DC analysis assumes no excitation, meaning everything remains steady from the past to the future. It deals with biases and allows the calculation of all voltages and currents in the design. The inductor behaves as a short circuit, while the capacitor acts as an open circuit during DC analysis.

After the verification of the DC analysis, the next step is the STB (stability) analysis. The STB analysis is essentially an AC analysis running on top of a DC analysis in a circuit with feedback. Through the STB analysis, the exact feedback, whether positive or negative, can be determined. Finally, it reveals how stable a circuit is over a range of frequencies. Therefore, the STB analysis allows the calculation of the loop gain at a specific frequency.

Numerous parametric simulations were conducted by varying the values of the transformer and capacitor to achieve optimum performance at the oscillation frequency of 10GHz. However, in a real implementation and on the layout, inductor values below 65pH are generally impractical. It's merely under certain assumptions. Further discussion on the transformer will follow later.

Following the STB analysis, the next step is the HB analysis, which constitutes the cornerstone of the VCO. In the STB analysis, we essentially perform a steady DC analysis with small variations. However, the VCO operates at ex-

tremes, transitioning suddenly from 0 to a large Vgs and then to a large Vds, etc. Thus, the STB analysis doesn't provide the most accurate values for the oscillation frequency of the VCO. Consequently, we generally consider the VCO as a circuit that operates in a large signal regime, and for this reason, we use the HB analysis. This analysis goes to each point and calculates the corresponding values using the necessary equations. For example, at some point, there might be a significant Vgs compared to Vds, which could be 0, causing the VCO to transition from saturation to triode region. Different equations are used in this case compared to the saturation region. Additionally, in such instances, certain parasitic capacitances are added or removed (in extreme cases) to calculate the average parasitic capacitance, which is greater than what an STB analysis would present.

In summary, if an STB analysis is run on the VCO, it might yield a resonant frequency of 11GHz, while an HB analysis on the same circuit can go to any point, calculate the respective values, and ultimately present a resonant frequency lower than the 11GHz from the STB analysis. This result is logical since, with the HB analysis, an average of parasitic capacitances is obtained from extreme conditions, resulting in a reduced Fosc. Generally, when a system has positive feedback, an HB analysis is imperative as it operates in a large signal regime. In contrast, in an LNA (low-noise amplifier), which can be single-ended, an STB analysis makes sense as it operates in a small signal regime. Finally, the HB noise analysis calculates all noises at all offsets.

7.2 Transformer

In this section, we will focus on the transformer, which constitutes one of the most significant and integral components of the final circuit of the VCO presented in this thesis.

Following parametric simulations of an transformer model to optimize the design for excellent performance, striving for the best possible coupling close to unity, the values obtained for the primary and secondary coils were Lp=97.2pH and Ls=85.1pH at 10GHz.

The goal of a design method for an on-chip transformer is to be implemented with the lowest possible losses in the desired bandwidth and optimal coupling between the regions it occupies on the chip. Therefore, knowledge of critical parameters characterizing a transformer (xfmr) is deemed essential. The term "coupling" refers to how well-matched the primary and secondary windings of the

transformer are. It is represented by the factor "k". The closer this factor is to unity, the better coupling is achieved, resulting in a broader frequency bandwidth. The equation describing the coupling coefficient, "k" between the primary and secondary is given by Eq. 7.3, where "M" is the mutual inductance between the primary and secondary coils, and "Lp" and "Ls" are the self-inductance values of the individual windings.

$$K = \frac{M}{\sqrt{Lp * Ls}} \quad (7.3)$$

So in this thesis a strongly coupled transformer with large coupling coefficient (k) is utilized to increase the oscillation stability at the desired resonant frequency. The large k transformer also facilitates the enhancement of tank Q at the lower resonant frequency. Usually, on chip inductors or transformers are often designed using the top metal layers in order to keep the inductors far away from the substrate, so that the capacitive couplings from substrate can be reduced. Moreover, in a commercial RFIC process, the top metal layers are usually much thicker than the bottom metal layers, thus the resistive loss can be much smaller. Therefore, the top metal layers are preferred to design the required two-coil transformer.

As the example of transformers shown in Figure 22, generally, there are two ways to realize a transformer: stacked and concentric [38], [39]. To obtain large coupling coefficients, the stacked transformer structure which involves conductors on different planes is preferred. Our target process has only three thick metal layers, which is enough for stacked two-coil transformer.

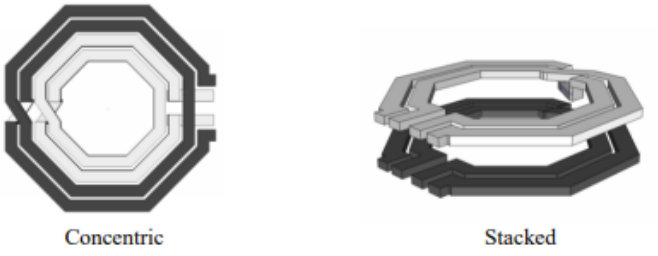

Figure 22: Examples of transformer realization with concentric and stacked coupling method.

As shown in Figure 23, the proposed transformer is designed using the top three metal layers named LB, QA, and QB with the thickness of 1.325 μm, 2.95 μm, and 2.95μm. The LB exhibits a resistance equal to 11mΩ/sq, while QA and QB have resistances of 6mΩ/sq each. In general, these three metals have the lowest resistance per square, and for this reason, they are often chosen to achieve the best performance in the circuit.

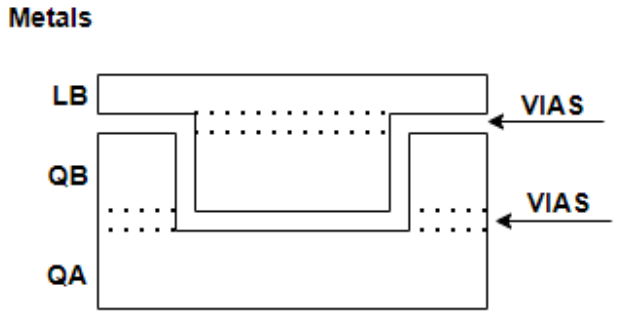

Figure 23: Transformer structure.

The primary objective from the outset was to achieve excellent coupling in the transformer (xfmr), as explained earlier. For this reason, a technique was employed to connect the primary and secondary coils. The larger coil value, specifically 97.24pH, is located in the LB metal, while the smaller value, 85.14pH, is situated in the QA metal. Between these two metals, there is another metal, QB, which shares the same characteristics as QA but is more distant from the substrate, resulting in lower parasitics. As depicted in Figure 23, QB was utilized as a 'step' to connect these two metals, and the distance between each metal was covered with the respective VIAS.

It is noteworthy that at the beginning of the design, Lp and Ls were initially planned in LB and QB, respectively, without any intermediate metal and VIAS. However, this approach proved to result in poor coupling, leading to the adoption of the aforementioned technique.

In Figure 24, the layout of the designed transformer is illustrated, with each metal represented by a specific color and the small squares are the vias. For the

layout design is important to note that, as the diameter increases, the value of each coil also increases. Additionally, as the width increases, the inductor value decreases, although not as significantly as the diameter. So there is a slower change in the inductor value when the width changes. Furthermore, all the edges of the transformer are positioned on the same side, allowing for future connection of devices in the actual implementation. In Figure 24, the transformer is observed from a top view.

The coil presented in Figure 25 has an internal diameter of 75μm, while the coil in Figure 26 has 62μm. As explained earlier, a larger internal diameter corresponds to a higher inductor value. Moreover, one can be observed that the coil with the green color appears thicker, with a greater width, compared to the other coil in blue. Specifically, the width of the coil with the value of 97.2p is 31μm, whereas the coil with the value of 85.1p has a width of 40μm. One might wonder why the decision was made to increase the width in order to decrease the inductor value, rather than decreasing the internal diameter to achieve the desired value; If hypothetically, we kept the width the same for both coils, then to achieve the value of 85.1p, it would be needed to reduce the internal diameter of the 'green' coil more. However, this would result in very poor coupling coefficient between the two coils, as they would not match at all.

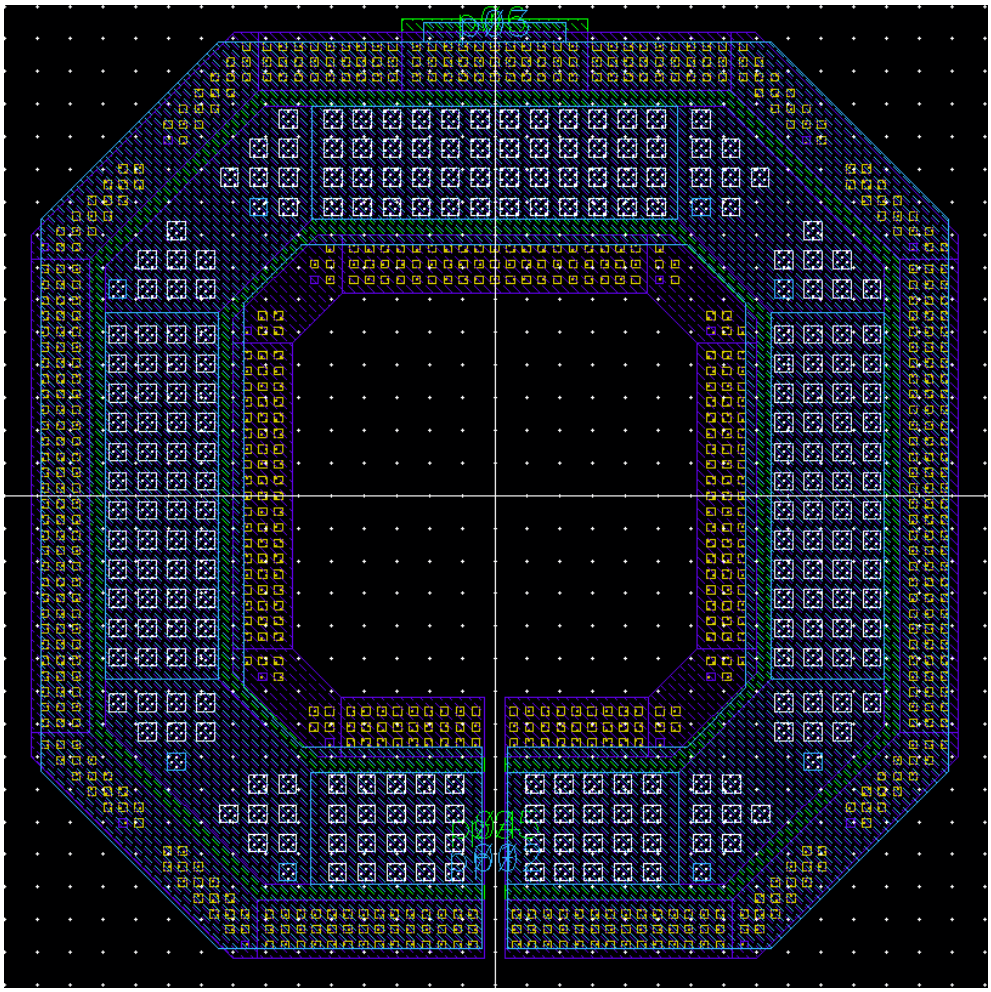

Figure 24: Transformer in layout design.

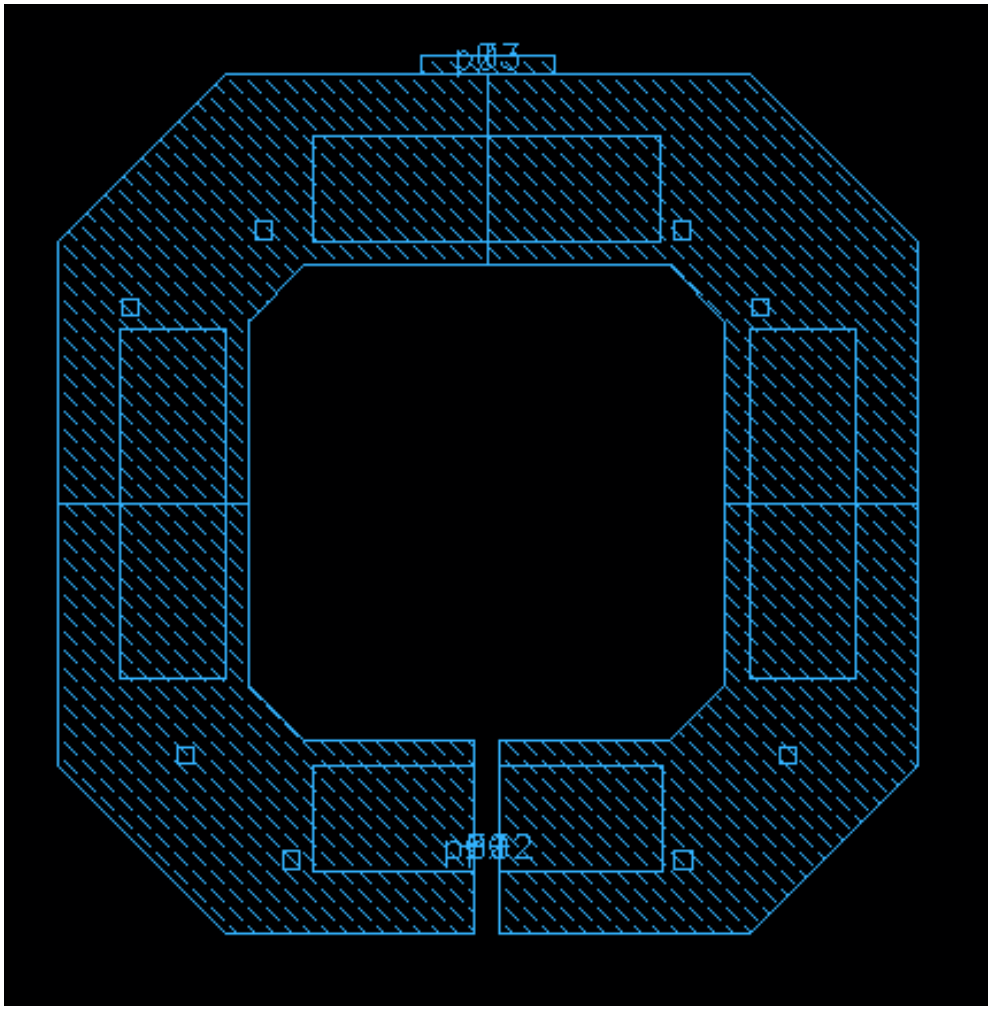

Figure 25: Layout design for the inductance value of 97.2pH.

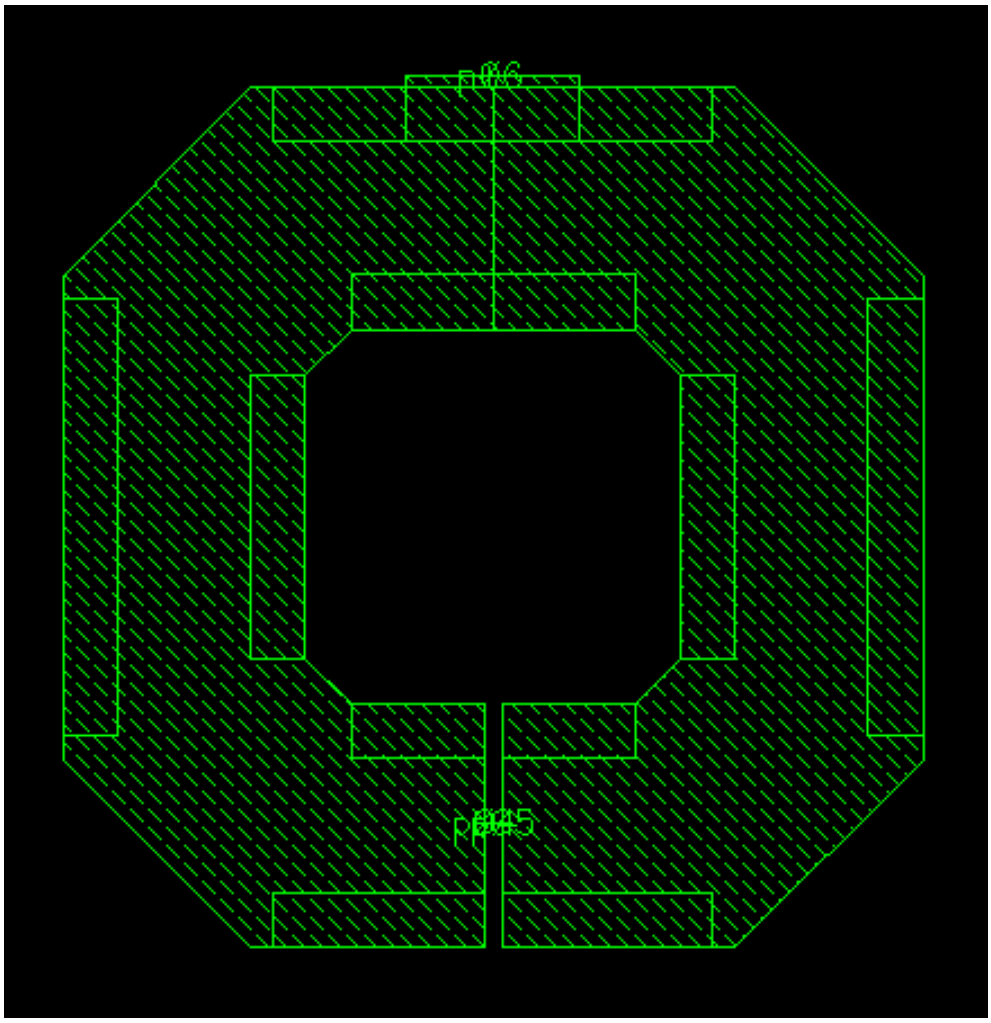

Figure 26: Layout design for the inductance value of 85.1pH.

7.2.1 Transformer simulation results.

A comprehensive model for a center-tapped transformer with two independent ports, as illustrated in Figure 27, is utilized in the Cadence environment to calculate the performance metrics of the transformer. It is worth noting that the presented schematic is a component of the library with six ports, representing the simulated EMX transformer. Specifically:

- The ports p1 and p2 correspond to the terminals of the primary coil.
- The ports p4 and p5 correspond to the terminals of the secondary coil.
- The ports p3 and p6 are grounded.

In this specific case, two ports were used, so the equation for calculating the coupling coefficient between the primary and secondary coils is appropriately formulated. Initially, the self-inductance value of each coil is calculated using Z-parameters:

$$L1 = \frac{1}{\sqrt{2\pi f}} * Im(Z11) \quad (7.4)$$

$$L2 = \frac{1}{\sqrt{2\pi f}} * Im(Z22) \quad (7.5)$$

Where Z11 and Z22 represent the complex impedance's of ports 1 and 2, respectively.

The mutual inductance between the primary and secondary windings is:

$$M = \frac{1}{\sqrt{2\pi f}} * Im(Z12) \quad (7.6)$$

Where Z21 is the transfer impedance seen at port 1 with port 2 open. It is also referred to as the complex open-circuit transfer impedance.

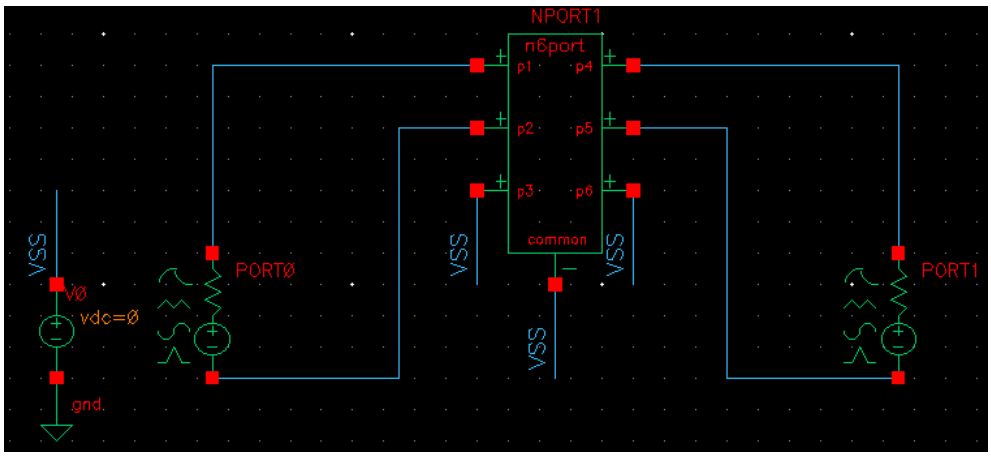

Figure 27: Configuration of the transformer for conducting measurements.

By substituting the above relationships into equation 7.3, the expression for the coupling coefficient is modified as follows:

$$K = \frac{M}{\sqrt{L1 * L2}} = \frac{Im(Z12)}{\sqrt{Im(Z11) * Im(Z22)}} \quad (7.7)$$

Upon defining the aforementioned equations in the Cadence Analog Design Environment, the analysis of S-parameter simulation (Sp simulation) is chosen, with frequency as the sweeping variable, specifically ranging from 1 GHz to 20 GHz. It is observed that the value of K is very close to unity, specifically normalized to 0.86 at 10 GHz. Consequently, the initial design goal of achieving excellent coupling in the transformer has been accomplished. Furthermore, the Quality Factor of each coil was calculated. In the table there are all the values that calculated from this testbench.

Parameters	Normalized at 10GHz
L1	97.2pH
L2	85.1pH
Q1	12
Q2	23.6
K	865m

Table 2: Transformer layout results.

7.3 Varactor selection

Following the STB analysis and defining the desired oscillation frequency for the VCO, the next step involved incorporating the varactor into the circuit, to convert the oscillator to a voltage controlled oscillator and to achieve a bandwidth between fmin and fmax and thereby obtain a broader tuning range. The primary aim of this thesis was to design a VCO with an extensive tuning range. The tuning range is directly linked to the varactor as mentioned in a previous chapter. There were two options for varactor connection: either at the drain or at the gate, each associated with a different voltage. There are two types of varactors: PCAP and NCAP, resulting in four possible ways to connect them to the circuit—either connecting PCAP to the drain or gate, or NCAP to the gate or drain. Each of these connection options has a direct impact on the VCO's parameters. PCAP stands for PFET in p-well variable capacitor, while NCAP stands for NFET in the n-well variable capacitor. Their principal of operation relies on the intrinsic capacitance in a MOS transistor. The structure of these varactor types is essentially a modification of a standard MOS transistor, connecting together the drain and Source terminals. The change in intrinsic capacitance is caused by the voltage between the two terminals (gate - drain/source). Consequently, great care was taken in the selection of the varactor and the determination of the voltage to be applied to its gate.

Eventually, a dedicated testbench 28 was created specifically for the varactor, implementing the four chosen connection options for varactor technology. To facilitate a more logical and informed choice of the varactor, initial simulations were performed with the varactors connected to drain using a 1.2V gate voltage. The Figure 30 reveals that when connected to the drain, NCAP dominates, as the capacitance of PCAP changes only minimally with Vtune. However, when both varactors are connected to the gate as illustrated in Figure 31, with a 0.5V gate voltage, a careful examination revealed that PCAP performs better. It can be observed that over the entire operating range of Vtune from 0.1 to 1.1V, the PCAP exhibits greater ΔC and will contribute a larger tuning range to the VCO implementation. This can be explained as the NCAP exhibits a slow variation of ΔC for Vtune from 0.6V to 1.1V, while the slow variation observed in PCAP ranges from 0.1V to 0.4V.

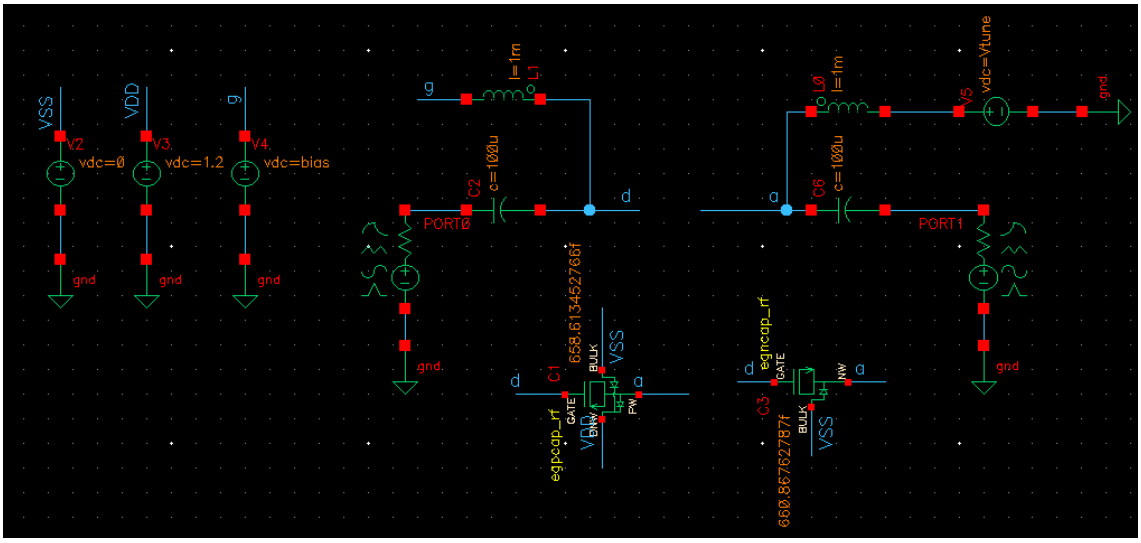

Figure 28: Varactor testbench showing NCAP (egncap rf) and PCAP (egpcap rf) and the respected biasing of gate and drain terminals.

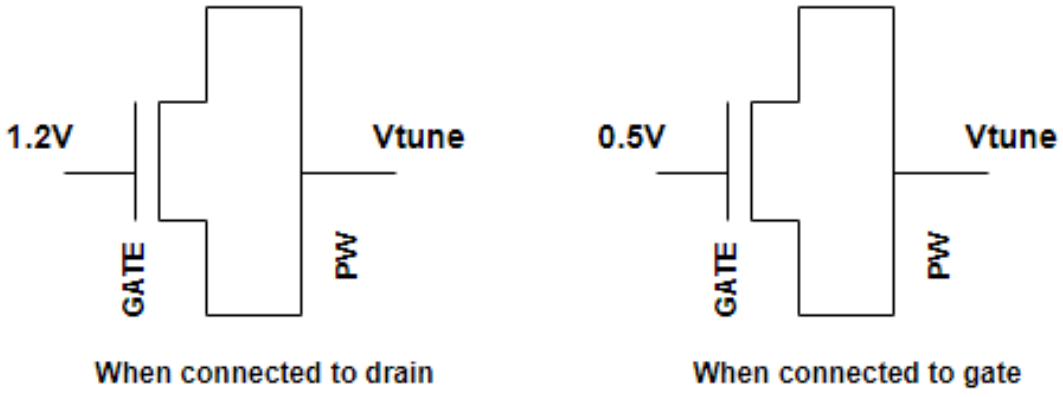

Figure 29: Theoretical representation and biasing of the PCAP varactor when connected to the drain and when connected to the gate.

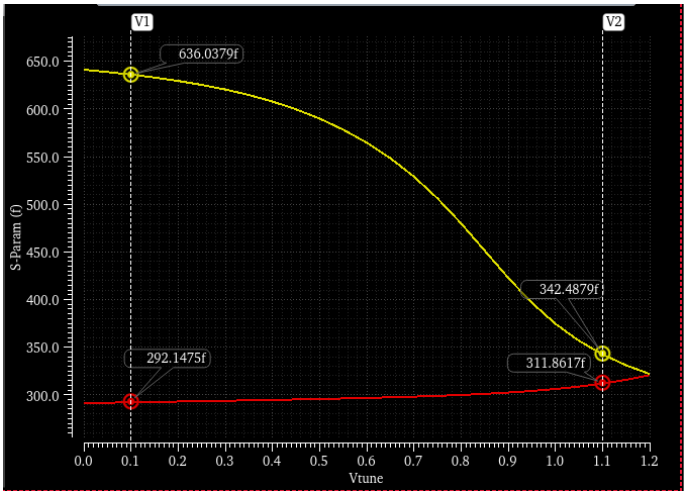

Figure 30: Comparing ΔC vs. ΔVtune characteristics of PCAP and NCAP connected to drain.

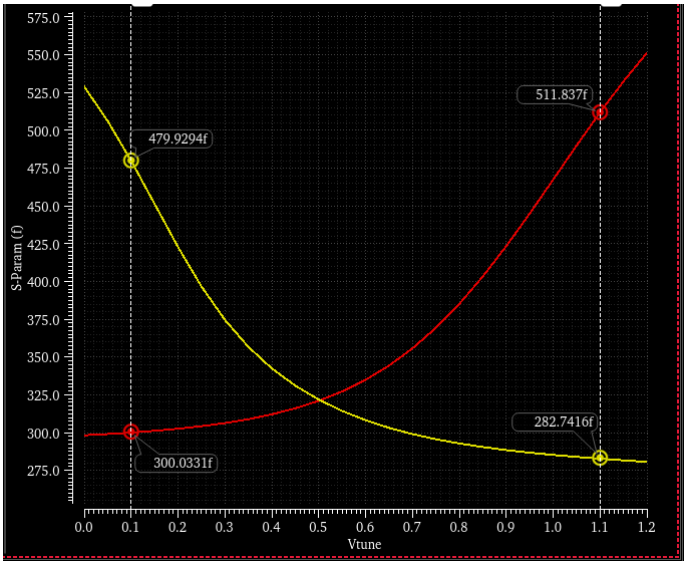

Figure 31: Comparing ΔC vs. ΔVtune characteristics of PCAP and NCAP connected to gate.

It is desirable to have a wide span of Fmax and Fmin. For the circuit to achieve optimal performance under the light of tuning range, in the varactor simulation, it is preferable to have a linear response of the C-Vtune characteristics (NCAP or PCAP), where a significant shift in the capacitance (ΔC) of the varactor occurs in response to Vtune. This significant change in capacitance allows for a broader tuning range. However, in practice, due to parasitic elements, biases, and other factors, this often becomes quite challenging.

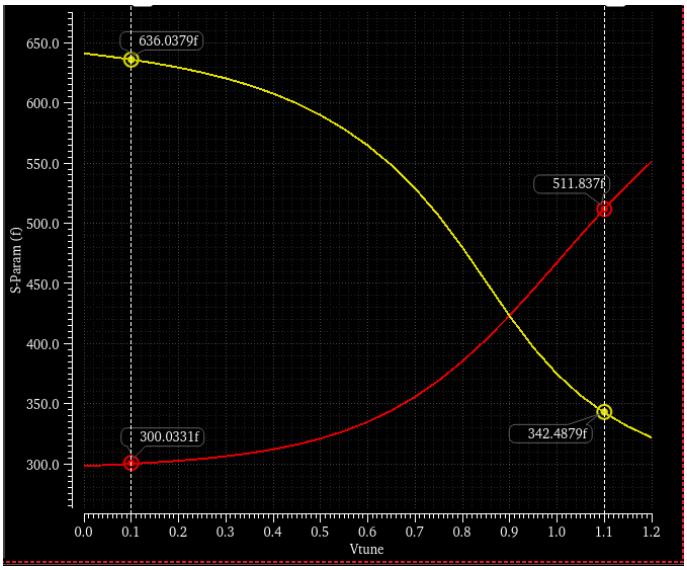

Figure 32: Comparing ΔC vs. ΔVtune characteristics of PCAP and NCAP connected to gate and drain, respectively.

To further evaluate performance, considering PCAP's dominance when connected to the gate and NCAP's dominance when connected to the drain, an additional testbench was set up to ascertain which of these connection methods would yield superior results for the circuit. As seen in the figure 32 , it is initially challenging to discern which varactor will perform better in regards of tuning range, as the two graphs are quite similar. In order to choose among the two possible solutions, it will also be needed to examine the quality factor of each varactor which is also one of the most significant metric for a VCO design. As previously mentioned, theoretical understanding suggests that the NCAP varactor should theoretically outperform the PCAP varactor. To confirm this, the quality factor of each varactor was measured using the testbench depicted in Figure 28. The results indicated a quality factor of 50 for NCAP and 38 for PCAP, establishing that, as a component, NCAP outperforms PCAP. It's crucial to recognize the analogy between quality factor and phase noise. Generally, the lower the overall quality factor of the tank, the worse the phase noise at all offsets. So before choosing the final NCAP implementation, a validation of Quality factor of the LC-tank is required.

To provide a logical and practical answer, another testbench was constructed based on the theoretical RLC circuit shown in Figure 33 . This testbench aimed to calculate the quality factor of the LC-tank, utilizing a theoretical 1A current source and the tank voltage equation V=I*Z, simplified to V=Z at I=1A. The overall quality factor was assessed using equation 7.8. In this testbench, 16 different cases were implemented involving NCAP in the gate or drain and a constant capacitor in the gate or drain, each with a model xfmr of the final values. The procedure was repeated similarly for PCAP. In this simulation, both NCAP and PCAP were modeled with a capacitor in series with a resistor, with the Qseries identical to the Q of the NCAP and PCAP equivalent. For NCAP, Q was set to 50, while for PCAP, it was 38. The same experiment was then conducted with the xfmr connected inversely to ensure all possible combinations exist. The table below illustrates the 16 options, including the calculation of the quality factor and resonance frequency for each case. 'Q50' denotes the NCAP model with a capacitor and a resistor in series with Q=50. Q38 denotes the PCAP model respectively. The table shows all the possibles connections.

Xfmr with L=97(Q=12) at drain and L=85(Q=22) at gate			
Metrics	Q	fc(GHz)	Q(10GHz)
1) Q50-gate with Con-Cap drain	22	10.1	21.7
2) Q50-gate with Con-Cap gate	19.7	10.57	18.63
3) Q50-drain with Con-Cap drain	10.3	9.89	10.4
4) Q50-drain with Con-Cap gate	24.1	10.2	23.6
5) Q38-gate with Con-Cap drain	21.2	9.2	23.04
6) Q38-gate with Con-Cap gate	17	9.5	17.89
7) Q38-drain with Con-Cap drain	9.14	9	10.15
8) Q38-drain with Con-Cap gate	18.3	9.1	20.10
Xfmr with L=85(Q=22) at drain and L=97(Q=12) at gate			
Metrics	Q	fc(GHz)	Q(10GHz)
9) Q50-gate with Con-Cap drain	24	10.2	23.5
10) Q50-gate with Con-Cap gate	10.3	9.8	10.5
11)Q50-drainwith Con-Cap drain	19.7	10.5	18.76
12) Q50-drain with Con-Cap gate	22	10.1	21.78
13) Q38-gate with Con-Cap drain	18.3	9.1	20.1
14) Q38-gate with Con-Cap gate	9.14	8.9	20.26
15) Q38-drainwith Con-Cap drain	17	9.5	17.89
16) Q38-drain with Con-Cap gate	21.2	9.2	23.04

Table 3: All the possible ways of connection.

From the above 16 options, an effort will be done to determine the best topology. Choices 1, 2, 7, 8, 9, 10, 15, and 16 are excluded because of the small tuning range that can be achieved. These correspond to 8 cases that exhibit very small ΔC for a ΔVtune shift based on the C-Vtune characteristics presented earlier. This implies a poor tuning range, deviating substantially from the specifications of this design. Consequently, out of the initial 16 options, only 8 remained. From these 8, the two with the highest Q were chosen, one for NCAP and one for PCAP. Therefore, option (4) with Q=24.1 and option (5) with Q=21.2 were selected. Subsequently, two different VCO designs were created, namely D2 and D3. D2 represents the choice with PCAP at the gate, while D3 involves NCAP at the drain, as illustrated in Table 4. To conduct a fair comparison between the two circuits, both were adjusted to ensure equal (a maximum of 2% deviation) power consumption, tuning range, frequency, and device size. By achieving these uniform settings, the selection of the optimal varactor can primarily be assessed based on phase noise.

NCAP-PCAP differences		
Metrics	NCAP	PCAP
Total width(u M)	234	234
Ids (mA)	10.4	10.4
$IH0_{VDD}$ (mA)	43.4	40.2
Vg_{bias} (mA)	500	500
Fosc(Ghz)	10.123	10.145
PN 10K (dbc)	-54.42	-62.46
PN 100K (dbc)	-84.21	-98.84
PN 1M (dbc)	-112.6	-125.6
PN 10M (dbc)	-138.1	-146.8
Tuning range (MHz)	683.1	685.3
Loop gain	6.66	7.89
$Vout_{H1}$ (V^2/Hz)	1.85	2.65
Quality factor	11.2	19.06

Table 4: Performance comparison of NCAP (connected to gate) and PCAP (connected to drain) varactors.

We have thus concluded with two designs, and it can be observed that design D3, with the implementation of NCAP, exhibits worse phase noise at all offsets. In contrast to the initial results presented in Table 3, indicating that D2 and D3 choices should have approximately equivalent results since they have an equivalent Q, in contrast to NCAP, which seems to have Q=50 compared to PCAP's Q=38, suggesting that NCAP would be the superior solution. It is observed that the better solution is, in fact, PCAP.

It is important to note that the simulations presented in Table 1 have been conducted with the xfmr model. Therefore, PCAP likely prevails because the parasitics and the entire network introduced by a real emx transformer slightly alter the picture, favoring PCAP. As mentioned earlier, there is a correlation between the quality factor and the phase noise, so we suspect that the PCAP implementation has an overall better quality factor. Using Cadence Virtuoso, the noise summary highlighted that 80% of the noise, particularly flicker noise at a 1MHz offset, originated from the two transistors. Additionally, all other noise contributions in the NCAP implementation are increased at all offsets, for example, thermal noise with the NCAP implementation was observed to be three times larger than with PCAP implementation. This indicates a generally worse quality factor with the NCAP implementation and that means that less noise is filtered, resulting in more noise

presence at the output.

Finally, for the valid confirmation of this phenomenon, an experimental implementation was carried out to measure the Q value for D2, D3, and as shown in Table 4, indeed, in the real implementation, the Q of PCAP appears better than the Q of NCAP.

$$QualityFactor = \frac{Fosc}{Bandwidth} \quad (7.8)$$

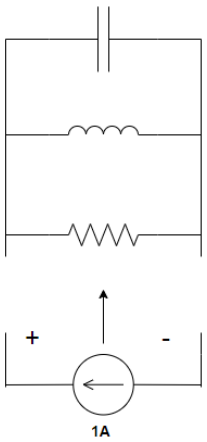

Figure 33: RLC circuit with theoretical 1A current source to determine the quality factor of the LC tank.

7.4 Capacitor bank

A frequency synthesizer is a crucial component in wireless transceivers, generating the local oscillation (LO) signal for both up-conversion in a transmitter and down-conversion in a receiver. Employing negative feedback, a phase-locked loop PLL-based frequency synthesizer acts as a control system to synchronize the phase of the output signal with that of the input reference signal. This synchronization allows for a constant phase difference in the locked status, ensuring the frequency synchronization of the output and reference signals. The block diagram in Figure 34 illustrates a simple PLL-based frequency synthesizer, comprising a phase/frequency detector (PFD), a charge pump (CP), a low pass filter (LPF), a voltage-controlled oscillator (VCO), and a divide-by-N frequency divider chain. This chain consists of a high-speed first-stage divider and subsequent low-speed dividers. The VCO's output frequency is divided, applied to the PFD, and compared with a reference signal. During the locking procedure, the PFD initially functions as a frequency detector (FD), aligning the VCO frequency with the reference signal. Subsequently, it operates as a phase detector (PD), generating an output proportional to the phase difference between the two inputs.

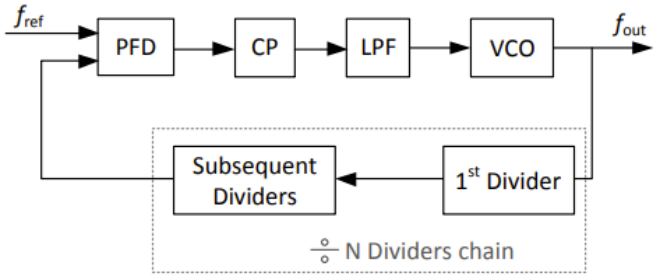

Figure 34: The topology of a typical PLL based frequency synthesizer.

In VCO design, specific frequency range specifications are crucial. In this project, the VCO was designed to operate at the range of 9.5GHz to 10.125GHz. The choice of capacitors in the LC parallel configuration directly influences the frequency. Increasing capacitance leading to a decrease in the resonant frequency. To meet these specifications, the initial objective is to achieve the higher frequency (in this design is 10.125GHz) using only the constant capacitor in the LC parallel configuration. Subsequently, a switch capacitor is inserted to enable oscillation

at the lower frequency of 9.5GHz. The capacitance of this capacitor is then divided according to the desired number of steps, determining the transition from 10.125GHz to 9.5GHz. VCO specifications guide the determination of the number of steps or specific values at which this transition should occur. In this design, a capacitor bank was implemented, comprising 16 thermo capacitors and three binary capacitors. The three binary capacitors create eight steps between each thermo, enhancing the precision of the oscillation frequency. Subsequent sections will delve into the details of both implementations.

Each passive element has a quality factor that describes it. It is crucial how the capacitor is designed to achieve the best possible quality factor. In this specific design, the constant capacitor has a value of 611.5 fF. Initially, it was implemented as a simple capacitor with a total value of 611.5 fF, with a large length and width. However, it was observed that the resistance created along the length, as theoretically known that the longer the length, the higher the internal resistance created, significantly affected all the metrics of the VCO. For this reason, the main constant capacitor of the circuit was implemented with five parallel capacitors using the multiplier in Cadence, with a length of 2um and a width of 9.6um. However, a testbench was created to calculate the quality factor of the capacitor, and parametric simulations were performed, varying the W, L, and multiplier to find the best possible solution with the highest Q, which turned out to be the above configuration. The same methodology was applied to the capacitors within the capacitor bank.

All capacitors are placed in parallel and are connected to the gate of the VCO, as shown in Figure 35. However, because the VCO must be symmetrical, the connection scheme is as follows: capacitor-switch-capacitor, so that both gates of the VCO can see the same interface. The switch is implemented with an NMOS device, as presented in Figure 36. In this specific implementation, the source and drain of the device have the same value, while the Vgate differs. The value received by each terminal comes from the digital part, where, when a signal, for example, 0.8V, is given, it passes through an inverter that makes the signal low (0V), and then directly through another inverter to make the signal high (VDD). The Vgate of the switch device takes the high value of the second inverter, i.e., VDD, so Vgs=VDD. In this specific design, Vgs=1.24V, while the source/drain terminals take the low value of the first inverter, and thus have a value of Vds=0. Thus, the NMOS is activated, opens, but because $Vds \ll Vgs$, the transistor is in the triode region and operates as a small resistance, i.e., a short circuit, activating the capacitor in the circuit. The value of each capacitor is 68.78 fF. However, we know from theory that when two equal capacitors C are connected

in series, the total capacitance they exhibit is calculated as C series with Cseries = C/2. Therefore, the total capacitance of each thermo inside the bank is 34.39 fF.

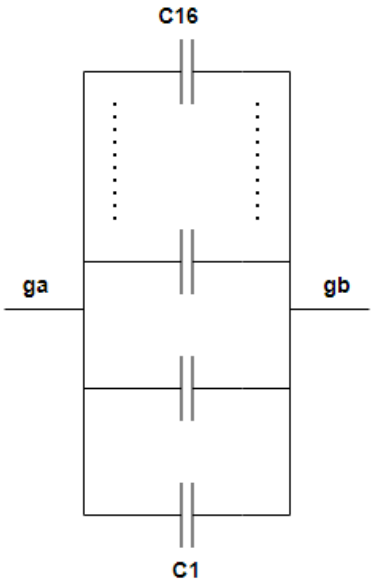

Figure 35: Capacitor bank.

The thermo capacitors differ significantly from the binary ones. In this specific design, as mentioned earlier, there are 16 thermo capacitors and 3 binary capacitors, where the 3 binary capacitors have 8 different combinations. When the design needs to activate, for example, 10 thermo capacitors within the bank, all capacitors up to the tenth one will be activated. However, if a more specific frequency is required, which cannot be achieved solely with the capacitance provided by the thermo capacitors, and a binary capacitor needs to be activated, only the one selected in binary will be activated, not all the previous capacitors. These three binary capacitors have different capacitance values from each other. The first binary capacitor has half the capacitance of the thermo capacitor, the second has one-fourth of the thermo capacitor, and the third has one-eighth, representing powers of 2. Therefore, each different combination with these 3 binary capacitors will result in different total capacitance and, consequently, different oscillation frequencies. Thus, within a range of the VCO from 10.125GHz to 9.5GHz, nearly

all intermediate frequencies are covered with a very high level of precision. It is crucial to note a significant aspect of the design process. The design begins by creating the thermo components and defining a total width for the switch. As mentioned earlier, when the switch is activated, it functions as a small resistance. Therefore, by keeping the capacitance value of the capacitors constant and adjusting only the width (W) of the device, the Quality factor of this implementation changes. As the W of the switch device increases, the resistance value decreases. Thus, when creating the binary, great care is required. As mentioned earlier, in the first binary, the capacitance of the capacitors will be half that of the thermo. In this case, the size of the switch device should also be reduced by half to increase the resistance value proportionally and keep the Quality factor at the same value. At this point, one might wonder why I am halving the size of the transistor when, if left the same, I would have a better Quality factor (if C decreases and R remains the same, Q increases). It is crucial to understand here that generally, the VCO across its entire operating range (i.e., all operating frequencies) is desired to exhibit constant performance.

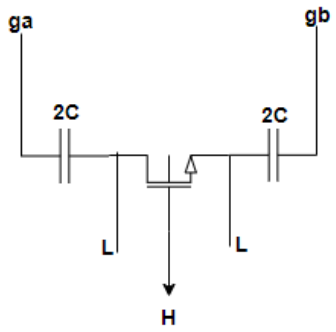

Figure 36: The switched capacitor in the design.

The final implementation, featuring inverters and the capacitor-switch-capacitor as explained earlier, is illustrated in Figure 37. The specific implementation varies based on the digital signal received at selCap. As mentioned earlier, a scenario was discussed where the digital signal is at 0.8V. In the event the signal is at 0V, the first inverter will drive it high. With 0V, as detailed in a preceding section, the PMOS device will open. Consequently, at the first inverter's output, the value VDD will transmit, serving as an input for the second inverter. Subsequently, the

NMOS (with PMOS closed) will open, and the output will yield the value VSS, resulting in a low signal. The gate of the switch device will thus receive the value 0, and the drain/source will receive the value VDD. As a result, the NMOS switch will remain inactive, functioning as an open circuit and leading to the closure of the specific thermo.

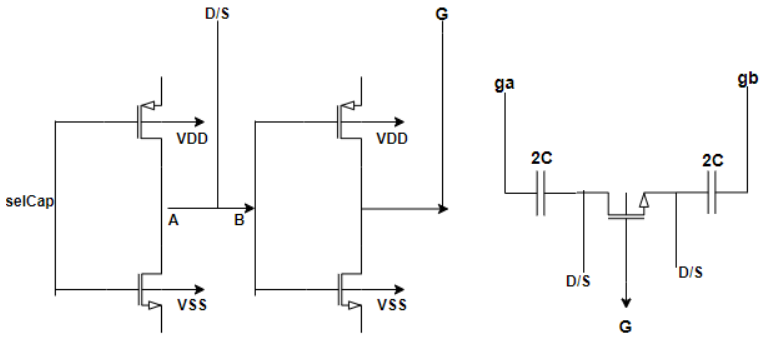

Figure 37: Capacitor bank topology.

Figure 38 illustrates 17 cases. In the specific case highlighted in red, neither a thermo nor a binary has been activated by the capacitor bank, resulting in no additional capacitance added to the design. Therefore, the oscillation frequency remains unchanged. After presenting the characteristic that describes the Fosc-Vtune without adding any capacitors, the features of each thermo for capBank values ranging from 1 to 16 are presented sequentially from top to bottom. Each case is associated with its unique tuning range, and it is important for the tuning range value to remain close to the value when the capacitor bank is closed.

In Figure 39, the characteristic Fosc-Vtune curves are presented when the first thermo is open, along with all possible combinations of the binary capacitors (8 in total). As observed, the entire gap range between each thermo is covered, as shown in Figure 38.

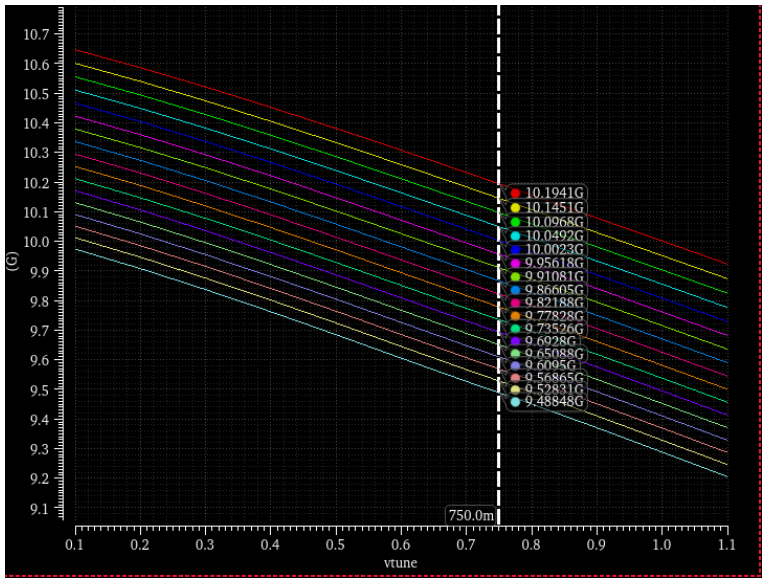

Figure 38: Oscillation frequency Fosc vs. Vtune, for each thermo capacitor.

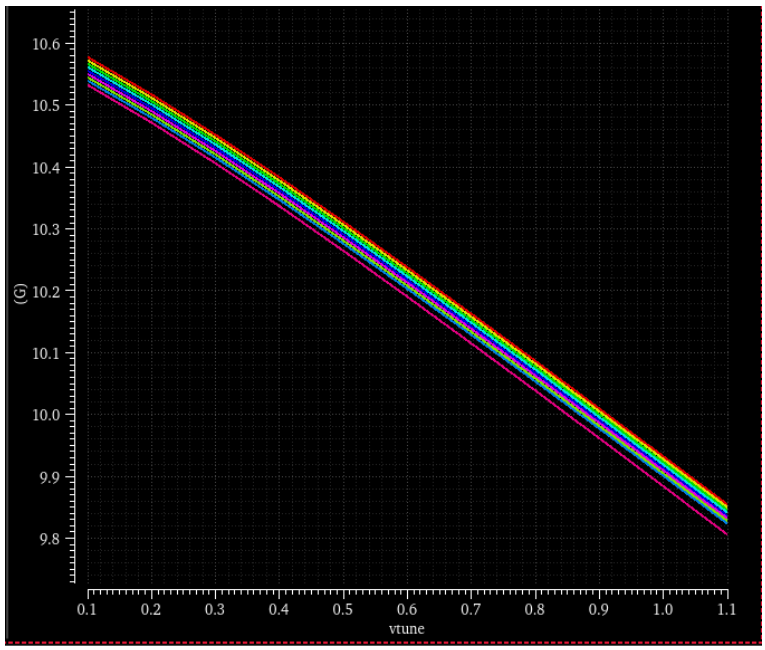

Figure 39: Oscillation frequency Fosc vs. tuning votage Vtune for all the binary combinations.

7.4.1 Thermometer and binary coding

In the design of the capacitor bank, both thermometer and binary coding methods are employed, leveraging their respective advantages. The thermometer code emphasizes the utilization of capacitance values during continuous adjustment, contributing to a smoother frequency step. Operating on a unary coding principle, it displays a range where the quantity of '1's corresponds to a smooth frequency step. Graphically resembling a thermometer reading, each code value represents a number 'N,' with the lowermost 'N' bits as '1' and the rest as '0'. Conversely, binary code offers a straight forward representation, with the capacitance value equal to the weight of the corresponding control code, allowing for flexible adjustments. The combined use of high-bit thermometer coding and low-bit binary coding optimally balances precision and flexibility in the capacitor bank for effective continuous adjustments in VCO design. Additionally, for an n-bit binary code, the corresponding thermometer code necessitates 2n – 1 symbols, requiring as many bits to represent the thermometer code.

decimal	thermo	binary
0	00000000	000
1	0000001	001
2	0000011	010
3	0000111	011
4	0001111	100
5	0011111	101
6	0111111	110
7	1111111	111

Table 5: Thermo and binary coding.

7.5 VCO simulation results

After placing all the essential structural elements of the circuit, adjustments were made to the values of the passive components of the VCO to ensure its operation specified frequency range from the outset. As mentioned earlier, the operational limits of this VCO are designed to cover a frequency range from 9.5 GHz to 10.125 GHz. In this work, it operates in the range of 10.17 GHz to 9.44 GHz. However, references will be made to the values of all metrics at the operational frequency limits rather than the extreme values. In Table 6 , the values of the parameters are presented at three different frequencies: the upper, the lower and the intermediate frequency of the frequency limits.

VCO results			
Central frequency (GHz)	f=10.125	f=9.816	f= 9.5
Idc (mA)	20.8	20.8	20.8
Vg_{bias} (V)	0.5	0.5	0.5
Vd_{dc} (V)	1.23	1.23	1.23
Vs_{dc} (mV)	10.44	10.44	10.44
Vth (mV)	374	374	374
gm (mS)	63.56	63.56	63.56
$IH0_{VDD}$ (mA)	41.5	42.5	43.7
Loop Gain	8.85	8.61	8.24
PN 10K (dbc)	-60.63	-60.99	-61.18
PN 100K (dbc)	-97.1	-97.93	-98.7
PN 1M (dbc)	-124.7	-125.7	-126.7
PN 10M (dbc)	-146.4	-147.3	-148.1
Tuning Range (MHz)	723.1	735.8	759.7

Table 6: Final simulations results.

As previously mentioned, the gain of the VCO, or KVCO, is an extremely crucial factor and is determined by KVCO = (Δf/ΔVtune). KVCO played a pivotal role in determining the value of VGbias in this work. Figure 40, 41 present two graphical representations of KVCO with different Vgate values. The first one, in red, represents the characteristic for Vgate = 0.3V, while the yellow one is for Vgate = 0.5V. Ideally, we would want the peak of KVCO to fall within the Vtune range (from 0.1V to 1.1V). However, in practice, it was observed that with VGbias set at 0.3V, there was no oscillation, indicating a negative loop gain ($Vgs < Vth$). Therefore, after experimental simulations, the value of 0.5V was determined as the

most optimal.

The KVCO in the final circuit is illustrated in Figure 42. Here, one can perceive the relative peak that KVCO reaches.

Figure 40: Representation of KVCO vs. Vtune, with 0.3V Vgate (ΔC/ΔVtune).

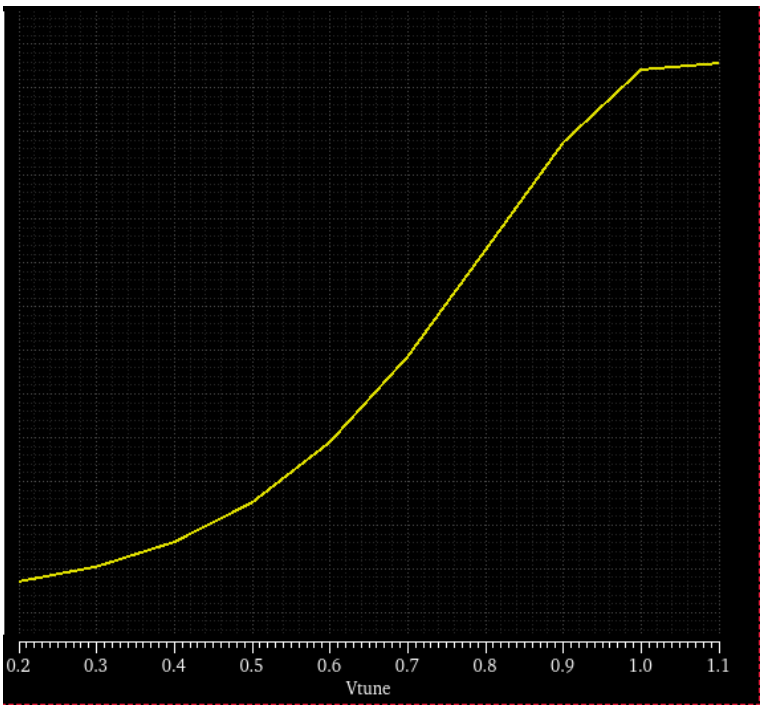

Figure 41: Representation of KVCO with 0.5V Vgates(ΔC/ΔVtune).

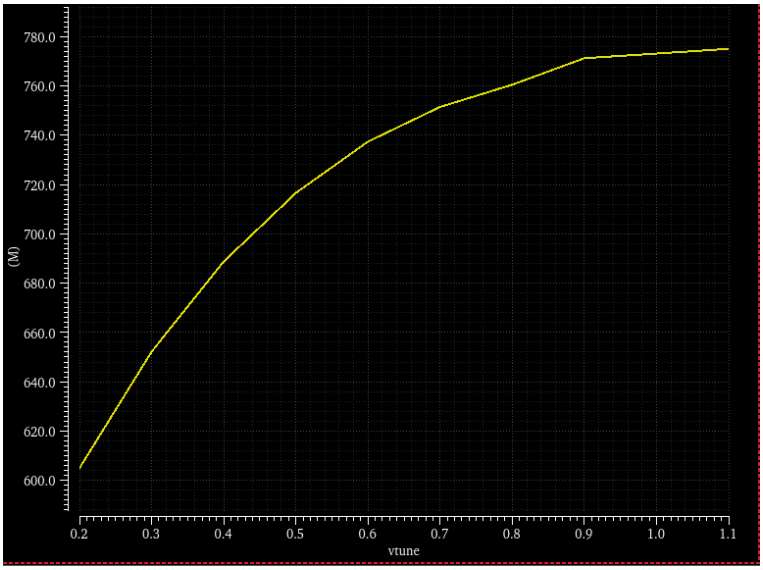

Figure 42: Representation of KVCO of the final design(ΔF/ΔVtune).

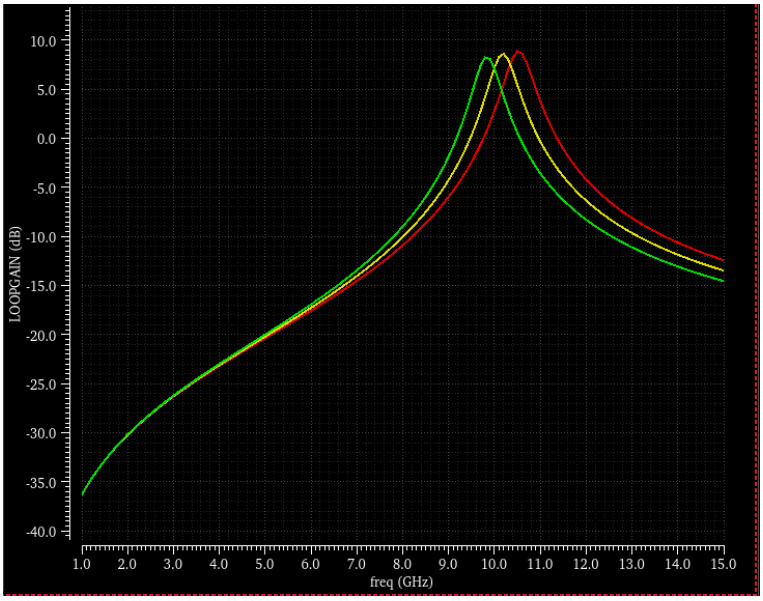

Figure 43: Loop gain for the three cases of frequency.

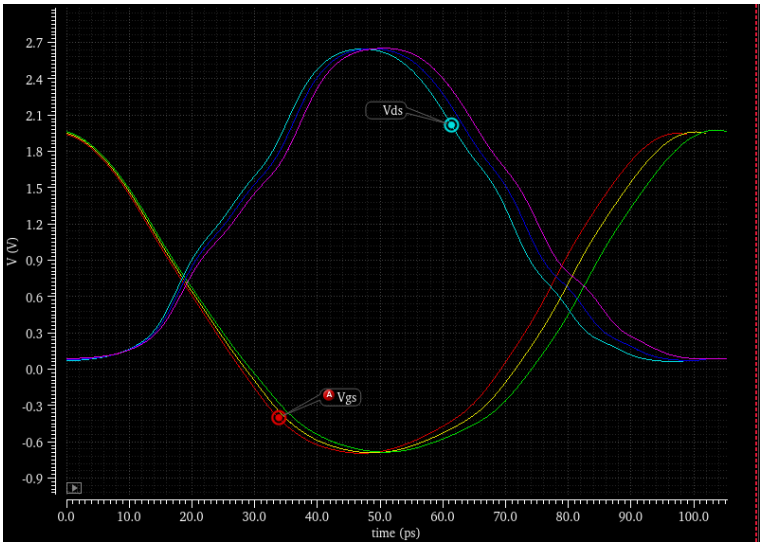

Figure 44: Voltages across the devices Vgs and Vds.

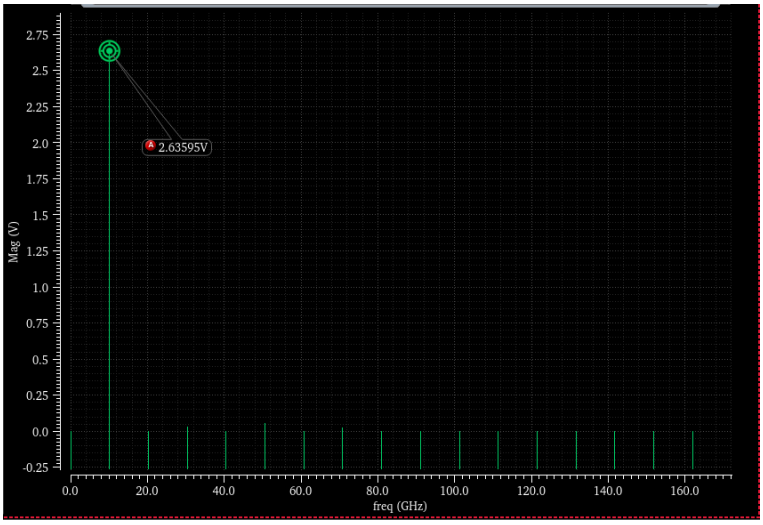

Figure 45: Differential output voltage (first harmonic).

Results Display Window

Window Expressions Info Help cadence

Active

Device	Param	Noise Contribution	% Of Total
/N4	flicker	9.81783e-14	17.00
/N6	flicker	9.80678e-14	16.98
/N4	therm_sid	6.77766e-14	11.74
/N6	therm_sid	6.775e-14	11.73
/NPORT1	rn3	5.08612e-14	8.81
/R10	rn	3.44774e-14	5.97
/N4	therm_Rs	1.46209e-14	2.53
/N6	therm_Rs	1.46132e-14	2.53
/R1	rn	8.30633e-15	1.44
/N4/egulvtnfet_mmw_6t/rgres	rn	7.82694e-15	1.36
/N6/egulvtnfet_mmw_6t/rgres	rn	7.82396e-15	1.35
/N4	therm_Rd	5.78238e-15	1.00
/N6	therm_Rd	5.77911e-15	1.00
/R0	rn	5.61231e-15	0.97
/NPORT1	rn5	5.59701e-15	0.97

Spot Noise Summary (in V^2/Hz) at 1M Hz Sorted By Noise Contributors
Total Summarized Noise = 5.77445e-13
No input referred noise available
The above noise summary info is for hbnoise_pm data

Figure 46: Spot noise summary (in V^2/Hz) at 1MHz offset.

From the noise summary provided by Cadence (Figure 47), the noise sources which translate into phase noise may be identified. The most significant impact is from the flicker noise of the MOS pair (/N6, /N4), which determines the phase noise in the $1/f^3$ region. This noise decreases only with an increase in the size of the transistor. Nevertheless, the size of the existing transistors is already sufficiently large to achieve the best possible phase noise. If the size of the transistors becomes too large, layout issues may arise. In a practical implementation, the space required for very large devices would be extensive, making their implementation impractical. Moreover, generally, large sizing implies the addition of other parasitic elements, something that is generally undesired in the circuit. The next phase contributor is the thermal noise of the MOS pair, which determines the phase noise in the $1/f^2$ region. This noise decreases only with a reduction in the bias current. However, the latter has been optimally adjusted, providing the highest possible ratio: 'output voltage/thermal noise of MOS,' and remains unchanged. The /R10 noise contributor in the circuit originates from the resistance in the Itail of the circuit. The resistance in the tail introduces parasitic resistance. An estimation of the parasitic resistance from the common source of the devices to the ground net is approximately 1Ω. It is evident from the noise summary that this resistance contributes about 6% to the total phase noise. Therefore, during the layout phase, careful attention is required to minimize this resistance as much as possible. Finally, the phase contribution /NPORT1, originates from the transformer. The integration of the transformer in silicon is one of the most undesirable processes in integrated circuits. It takes up a very large surface area and has a very small Q. Numerous efforts were made to model the transformer, leading to the attempt that was incorporated into the final circuit, yielding the best results achieved so far. In conclusion, altering various design parameters does not significantly enhance the results. The sole indirect method for improving phase noise is the quality factor Q. Unconstrained, a higher Q in the topology results in superior phase noise, establishing the quality factor Q as the bottleneck of the system.

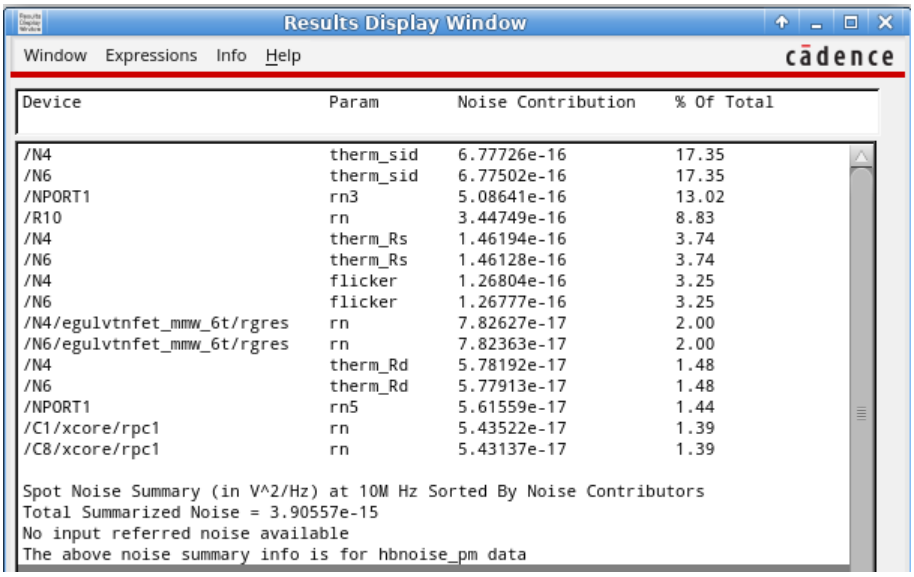

Figure 47: Spot noise summary (in V^2/Hz) at 10MHz offset.

Applying the noise summary once again, this time for a 10MHz offset, it can be observed that thermal noise is the dominant phase contributor. This is logical, as explained earlier and in accordance with the theory. Flicker noise is associated with the up-conversion that occurs at high frequencies, hence closer offsets from Fosc, whereas thermal noise dominates at lower frequencies, hence larger offsets.

According to Figure 48, two distinct regions, $1/f^2$ and $1/f^3$, are easily identified, as anticipated by the theory (Figure 12). The $1/f^3$ region exhibits a slope of -36.46 dB/decade between 10kHz and 100kHz, and -27.69 dB/decade between 100kHz and 1MHz, concluding at approximately 1MHz. On the other hand, the $1/f^2$ region has a slope of -21.69 dB/decade. This aligns well with the theoretical expectations, confirming the presence of the predicted frequency-dependent characteristics.

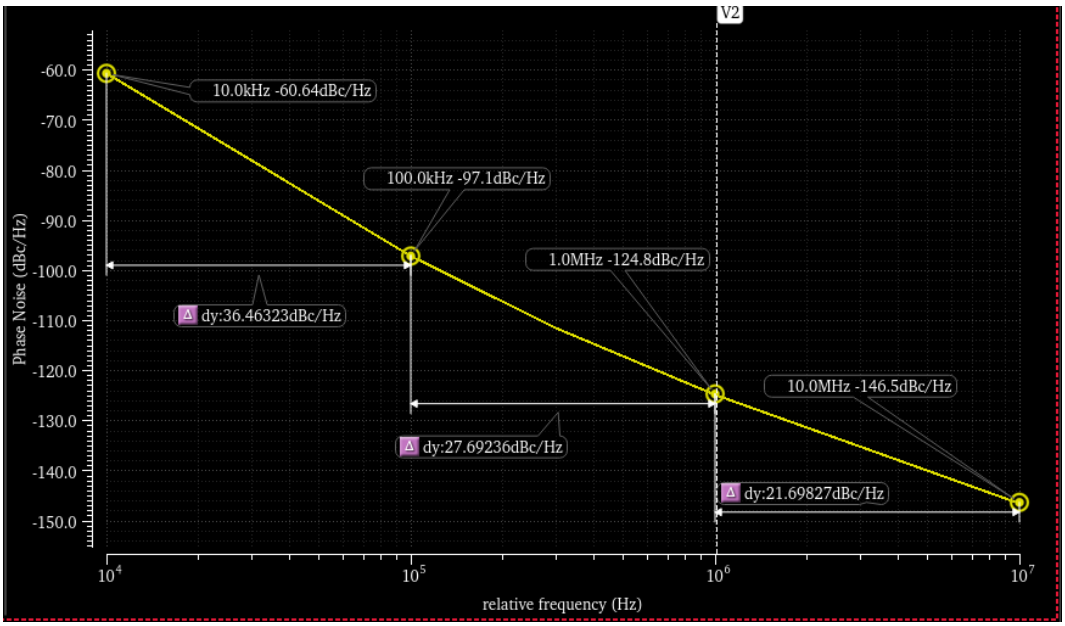

Figure 48: Phase noise vs. frequency offset for the optimum design of the LC-VCO.

7.6 Figure of merit and state of the art

Recently, there has been an increased focus on the performance of VCOs because of their critical role in determining the overall performance of key circuit components such as RF front-ends and clock generators. In literature on VCO design, several Figures of Merit (FoM) are employed to assess VCO performance. FoM is a quantity to measure the performance of a device relative to its alternatives. The performance of VCOs is difficult to compare as they feature different center frequencies, power consumption and phase noise over different offset frequencies. A standard formula for Figure of Merit is referenced here:

$$FoM = L(Fm) - 20 * log(\frac{Fosc}{Fm}) + 10 * log(\frac{Pdc}{1mW}) \quad (7.9)$$

where L(Fm) is the phase noise from the oscillator frequency (Fosc) at a frequency offset of fm, and Pdc is the DC power consumption of VCO in milliwatt.

Ref.	Proc.	Freq(GHz)	VDD(V)	PDC(mW)	PN@1MHz	TR	FOM(dBc/Hz)	FOMT(dB)
[43]	65nm	39.9	1.2	14.4	-98.1	15.1	-178.5	-182.1
[44]	22nm	23	0.65	11.5	-106	27	-182.6	-191
[45]	90nm	2.42	1.8	0.51	-119.7	10.53	-190.2	-190.7
[46]	180nm	11.2	1.8	6.8	-109.4	2.6	-181.8	-170
[47]	90nm	12.72	1.2	3	-105.2	1.6	-182.7	-166.8
This.	22nm	10.17	1.24	73	-124.6	7	-186.1	-183.3

Table 7: Performance and comparison with state of the art.

A commonly used figure of merit FoMT which additionally takes into account the tuning range is also included in the comparison. The FoMT is defined as:

$$FoMT = L(Fm) - 20 * log(\frac{Fosc}{Fm}) + 10 * log(\frac{Pdc}{1mW}) - 20 * log(\frac{TR}{10}) \quad (7.10)$$

This work, as shown in the above table, exhibits a -124.6 PN at a 1M offset, a 7% tuning range, and demonstrates higher power consumption compared to other designs (73mW). To calculate the Power Dissipation Consumption (Pdc), the rms value of the harmonics in the equation Pdc = VDD * Irms was utilized, rather than Idc, to ensure a more accurate and correct result. This choice was made because the value of Irms was almost six times greater than Idc (58.89mW compared to 10.44mW). The Tuning Range (TR) was calculated using the equation 7.11, where Fmax=10.62GHz, Fmin=9.903GHz, and Fcenter=10.27GHz.

$$TR = \frac{Fmax - Fmin}{Fcenter} \quad (7.11)$$

$$Fcenter = \frac{Fmax + Fmin}{2} \quad (7.12)$$

As observed from Table 7, the specific design exhibits a very good performance. In comparison to the other implementations presented above, the Figure of Merit appears superior, except one case [45]. The superior performance of this design, as indicated in Table 7, can be mainly credited to a focused initiative to minimize phase noise. The process commenced with careful selection and biasing

of transistors, followed by endeavors to optimize the quality factor throughout the LC-TANK. Consequently, the VCO in this work achieve the most effective reduction in phase noise.

8 Conclusion

In this work, a voltage-controlled oscillator (VCO) was designed and simulated in a 22nm FD-SOI technology. The implemented work achieved a tuning range of 723 MHz (7%) within the range of 9.5-10.125 GHz, with a step of 4.8MHz and a phase noise of -124.8 dB/Hz, with a 1 MHz offset. Through this work, the crucial importance of the quality factor Q, for LC oscillators, became clear, determining it as the 'bottleneck' of the system by influencing phase noise. The overall Q of the design is 18.4, constrained by the quality factor of the transformer.

The present design of an RF/mmW VCO shows the drastic importance that the active (transistors) but maybe even more so passive elements (varactors, inductors, transformers, transmission lines) have on the performance that may be achieved with a certain available technology. The present work is based on extensive practical knowledge available in a design team, but furthermore employs extensive investigations, such as parametric explorations and studies of cases. In the final design of the LC-VCO, the phase noise at 1MHz offset is dominated by about 34% stemming from flicker noise and about 23.5% from the thermal noise of the MOS differential pair, while the remainder 42.5% of phase noise stem from the accumulated noise of all other noise contributors (mainly parasitic resistances) in the circuit, which have very small impact when considered individually.

In this design, the primary emphasis was on the selection of the varactor, where the significance of the Quality Factor and its impact on the circuit's performance became evident. For every VCO design, certain specifications are always present, with tuning range being the most critical, followed by phase noise, power consumption, etc. Depending on these specifications, the VCO design changes each time, always demanding to meet the specific requirements.

Finally, at the conclusion of the work, the importance of a thorough understanding of Electronic Design Automation (EDA) tools and the constraints of the respective technology were recognized. Without these, designing practical and realistic applications is not feasible.

9 Future work

As a future task, efforts will be directed towards improving the transformer to achieve a higher Quality Factor, thereby enhancing the overall quality factor of the system. Since the current design has progressed only to the layout stage for the transformer, the immediate next step is to extend the layout design to encompass all individual components of the VCO. Furthermore, an investigation of PVT variations should be carried out, namely exploring process variability, and performance over a large temperature range. Additionally, it is essential to familiarize ourselves with the individual circuits that directly interface with the VCO, such as LDO and Output buffers. This effort aims to gain a more comprehensive understanding of any factors that may influence the performance of the VCO.

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