Design of a mm-Wave Low Noise Amplifier (LNA) in FDSOI CMOS Technology

Σχεδίαση Ενισχυτή Χαμηλού Θορύβου (LNA) για χιλιοστομετρικές συχνότητες με τεχνολογία FDSOI CMOS

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Abstract

In today's data-driven world, where efficient data transmission is paramount, there's an increasing adoption of 5G technology in both mobile and satellite communications. 5G offers a cost-effective, energy-efficient solution with broad global coverage. Operating in the Ka-band high-frequency spectrum, enables high-speed data transfer with minimal latency. Meeting these demands necessitates advancements in high-performance RF components. Low Noise Amplifiers (LNAs) serve as crucial components in the receiver chain, amplifying signals while minimizing added noise. Hence, designing high-performance LNAs that are cost-effective and offer integration advantages is essential to support technological advancements. This thesis focuses on designing a Low Noise Amplifier using 22nm FD-SOI Technology. The design is based on a Single Stage Common Source Amplifier circuit with Inductive Degeneration, operating at a frequency of 28 GHz. Throughout the process, Schematic design, Optimization, Layout design, and Simulation are conducted to provide a comprehensive design approach. During the design process, Cadence's Virtuoso software was utilized as the primary tool. The work resulted in notable outcomes, for a power consumption of 16.29 mW from a 0.8 V supply, the LNA achieves a NF of 1.88 dB, provides peak gain at 10.62 dB , area 0.15 mm^2 and linearity I1dB of -3.6 dBm, reflecting the efficacy of the implemented design strategies. The Simplified EKV Model and the design method based on Inversion Coefficient, were applied in this work to extract parameters and explore trade-offs, comparing them to the design simulation results illustrating the efficacy of employing Inversion Coefficient in estimating the optimal bias when designing analog FD SOI circuits.

Περίληψη

Σε έναν κόσμο όπου η αποδοτική μετάδοση δεδομένων είναι ύψιστης σημασίας, παρουσιάζεται μια όλο ένα και ανερχόμενη τάση για την εξάπλωση της τεχνολογίας 5G, τόσο στις κινητές όσο και στις δορυφορικές επικοινωνίες. Το 5G προσφέρει μια οικονομική, ενεργειακά αποδοτική λύση με ευρεία, παγκόσμια κάλυψη. Η λειτουργία του στο φάσμα υψηλής συχνότητας Ka προσφέρει μεταφορά δεδομένων υψηλής ταχύτητας με χαμηλή απόκριση. Για την ικανοποίηση αυτών των αναγκών, η προηγμένη σχεδίαση RF-στοιχείων υψηλής απόδοσης καθίσταται απαραίτητη. Οι Ενισχυτές Χαμηλού Θορύβου (LNAs) αποτελούν βασικά δομικά στοιχεία στην αλυσίδα του δέκτη, ενισχύοντας σήματα ενώ ταυτόχρονα ελαχιστοποιώντας προστιθέμενο θόρυβο. Επομένως, η σχεδίαση LNA υψηλης απόδοσης που είναι οικονομικοί και προσφέρουν πλεονεκτήματα ολοκλήρωσης συνιστούν στοιχεία ζωτικής σημασίας για την υποστήριξη των τεχνολογικών εξελίξεων. Αυτή η διπλωματική εργασία, επικεντρώνεται στον σχεδιασμό ενός Ενισχυτή Χαμηλού Θορύβου χρησιμοποιώντας την τεχνολογία 22nm FD-SOI. Η σχεδίαση έχει ως βάση έναν Single Stage Common Source LNA, με Inductive Degeneration, σε συχνότητα λειτουργίας 28GHz. Κατά τη διάρκεια της διαδικασίας, πραγματοποιήθηκε σχεδιασμός του Σχηματικού, Βελτιστοποίηση, σχεδιασμός της Διάταξης και Προσομοίωση για την παρουσίαση μιας ολοκληρωμένης σχεδιαστικής διαδικασίας. Καθ'ολη τη διαδικασία σχεδίασης, το λογισμικό της Cadence, Virtuoso αποτέλεσε το βασικό εργαλείο. Η εργασία παρουσίασε σημαντικά αποτελέσματα. Για μια κατανάλωση ισχύος 16.29 mW από μια τροφοδοσία 0.8 V, ο LNA επιτυγχάνει NF 1.88 dB, παρέχει peak Gain στα 10.62 dB, επιφάνεια $0.15mm^2$ και γραμμικότητα -3.6 dBm, ανταγακλώντας την αποτελεσματικότητα των σχεδιαστικών στρατηγικών που υοθετήθηκαν. Το Απλοποιημένο Μοντέλο EKV και η σχεδιαστική μέθοδος βασιζόμενη στον Συντελεστή Αναστροφής εφαρμόστηκαν σε αυτή την εργασία με σκοπό την εξαγωγή παραμέτρων και διερεύνηση των trade-offs συγκριτικά με τα αποτελέσματα του προσομοιωτή που προκύπτουν από το σχεδιαστίκό κομμάτι της εργασίας που προηγήθηκε, επισημαίνοντας την αποδοτικότητα της χρήσης του Συντελεστή Αναστροφής για την εύρεση του βέλτιστου σημείου πόλωσης όταν σχεδιάζουμε αναλογικα κυκλώματα σε τεχνολογία FD-SOI.

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I am deeply thankful to my friends, whose companionship made my time in Chania truly unforgettable, and to my partner Damianos, whose support has been constant throughout these years.

Lastly, I wish to express my profound appreciation to my parents, Evi and Manolis, and sister Marianthi to whom I dedicate this work. My father's encouragement and expertise in Microelectronics inspired me to pursue this path, my mother and sister have consistently been there to support and believe in me, during my five-year study. Without them, this journey would have seemed much more difficult or even impossible.

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Abbreviations

Abbreviation	Meaning
5G	Fifth Generation Mobile Network
22-FDX	22nm Fully Depleted Silicon on Insulator
AWGN	Additive White Gaussian Noise
BOX	Buried OXide
CG	Common Gate
CH	Carrier Heating
CLM	Channel Length Modulation
CMOS	Complementary Metal Oxide Semiconductor
CS	Common Source
EKV	Enz-Krummenacher-Vittoz
FDSOI	Fully Depleted Silicon on Insulator
FEM	Front End Module
FinFET	Fin Field Effect Transistor
FoM	Figure of Merit
GaAs	Gallium Arsenide
IC	Inversion Coefficient, Integrated Circuit
IP3	Third Order Intercept Point
LEO	Low Earth Orbit
LNA	Low Noise Amplifier
MI	Moderate Inversion
mm-Wave	Millimeter Wave
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NF	Noise Figure
NFET (PFET)	N (P)-Channel Field Effect Transistor
NMOS (PMOS)	N (P)-Channel Metal Oxide Semiconductor
P1dB	1dB Compression Point
PD	Partially Depleted
RF	Radio Frequency
SATCOM	Satellite Communications
SI	Strong Inversion
Si	Silicon
SLVT	Super Low V_T
SNR	Signal to Noise Ratio
SOI	Silicon On Insulator
SP	S-Parameter
T/R, TX/RX	Transmit/Receive
TID	Total Ionizing Dose
TNEF	Thermal Noise Excess Factor
VGA	Variable Gain Amplifier
VS	Velocity Saturation
WI	Weak Inversion

Chapter 1

Introduction

1.1 Understanding 5G: Challenges and Solutions

The contemporary lifestyle and work dynamics are greatly dependent on high performance mobile communications. For instance, in the growing popularity of the digital nomad lifestyle, where individuals travel to various locations while working remotely, a reliable high-speed internet connection is paramount. This example extends to remote workers fulfilling their job duties from home, online entrepreneurs managing their online businesses, and students who are increasingly attending virtual classes and conducting research as online education gains popularity. The reliance on high-speed internet becomes especially critical in remote rural areas, crowded urban environments, and underdeveloped countries, where internet access may be unreliable. The need for high speed connectivity lies in the widespread adoption of 5G technology.

5G networks operate through cellular structures, dividing service areas into small cells. Within each cell, 5G devices communicate with a cellular base station using radio waves and fixed antennas, utilizing frequencies allocated by the base station. These base stations, referred to as nodes, connect to telephone network switching centers and Internet routers through high-bandwidth optical fiber or wireless backhaul links. Similar to traditional cellular networks, mobile devices seamlessly transition between cells as they move, ensuring continuous connectivity. In this work, the 5G frequency band of interest is the High-band, also known as millimeter-wave (mmWave). This frequency band with a range of 24-47 GHz, provides high spectral efficiency, average data speed of 1.6 Gbps (peak up to 20 Gbps), offers up to 2 GHz channel bandwidth, around 1 millisecond latency, and susceptibility to obstacles while being less affected by disruptions from other devices.

Operating in mm-Wave frequencies, 5G devices present some technical constraints that pose challenges to their widespread adoption, despite their numerous advantages. For instance, the shorter wavelengths of mm-Wave signals restrict their coverage, making them prone to obstruction by structures like buildings and trees. Consequently, deploying more base stations and access points becomes necessary, leading to increased costs due to the current utilization of expensive technologies like GaAs. Moreover, atmospheric conditions such as rain, fog, and electromagnetic radiation sources can interfere more significantly with 5G high bands. Lastly, the elevated power consumption of high bands may reduce mobile device battery life and escalate infrastructure energy usage. Therefore, the advancement and design of high-performance RF components have the potential to mitigate the mentioned issues concerning cost-effectiveness, power consumption, and resilience, assisting this technology in enabling reliable and efficient communication networks. One crucial building block in the receiver chain is the Low Noise Amplifier (LNA). Though small in size, this component holds significant importance in amplifying the received sig-

nal while minimizing any accompanying noise and rejecting unwanted interference from other signals. Thus, it is crucial to develop silicon-based technologies that enable the creation of high-performance LNAs, which are cost-effective and provide integration benefits, in order to facilitate technological progress. These aspects will be further explored and discussed within the scope of this thesis.

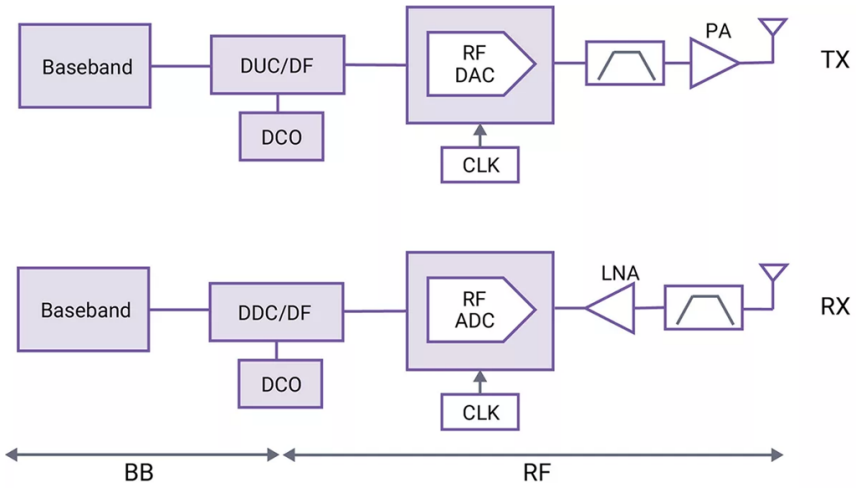


Figure 1.1: 5G mmWave front-end signal chain architecture uses direct RF sampling [31]

1.2 Outline

- **Chapter 2: mm-Wave Design and LNAs -** This chapter will give an understanding of significant concepts in mm-Wave design, including LNA Design for Satellite applications and the various types of noise, a crucial concept in LNA Design theory.
- **Chapter 3: Low Noise Amplifier Design Considerations -** This chapter will delve into the essential design parameters and present significant LNA topologies applicable to this study.
- **Chapter 4: SOI Technology -** This chapter provides an overview of SOI technology, including its benefits, drawbacks, a comparison with alternative technology, a design methodology based on Inversion Coefficient, and an evaluation of the figure of merit.
- **Chapter 5: Low Noise Amplifier Design -** This chapter will serve as a crucial section detailing the design methodology for schematic creation, layout extraction, and the comparison of the final LNA with other researches.
- **Chapter 6: Conclusion -** This final chapter will provide summaries, remarks, and suggestions for future research to be explored.

Chapter 2

mm-Wave Design and LNAs

2.1 Introduction to Low Noise Amplifiers

What exactly is a low-noise amplifier?

A low-noise amplifier, commonly known as an LNA, plays a crucial role in digital processing setups by establishing connections to analog components. Situated as the initial amplification phase in a receiver, the LNA's primary objective is to boost the input signal to a level that ensures subsequent signal processing remains unaffected by noise. Given that the LNA circuit kick-starts the receiver chain, its design significantly influences overall noise levels. Hence, effective LNA design targets minimal noise figure (NF) and substantial gain [22]. Consequently, an effective LNA design should aim to minimize noise influence in subsequent stages and amplify the weakened signal received by the antenna, thus facilitating efficient processing by subsequent stages (like the mixer and VGA)[24].

2.2 LNAs for Satellite Applications

One of the main focuses of a mass production of miniaturised satellites such as LEO (Low Earth Orbit) Satellites and CubeSats, is to choose a suitable silicon implementation process that meets the requirements of low cost and maximum integration.

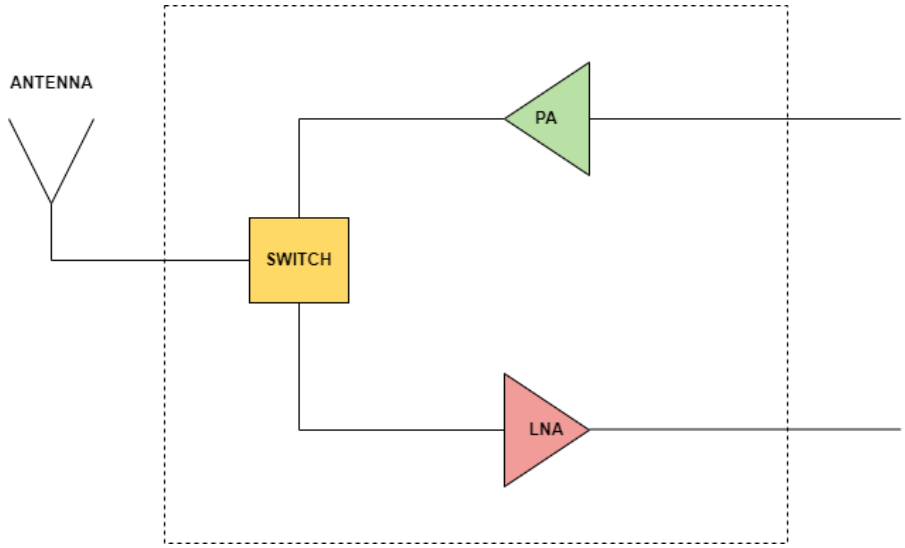


Figure 2.1: Front End Module

The Front End Module or FEM in SATCOM is an integrated single chip, consists of an LNA, PA, and switch that processes signals at the antenna or receiver end, as shown in **Figure 2.1**. In an application like the ones described here, the F_t/F_{max} specs should reach over 300GHz in order to support the amplification requirements and enable the design of high quality T/R switches and low loss passive components assisting. The most promising process currently for that purpose seems to be a fully depleted SOI silicon process, such as the 28/22mm FDSOI one, which is one of the most appropriate semiconductor processes for the integration of such wireless transceivers and can be provided by well-known European-based foundries (such as ST Microelectronics and Global Foundries). The "Radiation Hardening Fully-Depleted Silicon-On-Insulator process" makes the RF IC elements resistant to damage or malfunction caused by high levels of ionizing radiation, with a superior radiation immunity, combines good RF characteristics, high self-gain devices for good analog baseband circuits, fast digital cells, as well as programmable performance,dissipation and leakage [1]

The buried insulating layer (buried oxide – BOX) is also known to introduce problematic considerations for total ionizing dose (TID) radiation effects, particularly for fully-depleted (FD) SOI. Recent work in characterization of TID effects in partially depleted (PD) SOI indicates that the inherently high doping levels of the body region result in insensitivity to TID. The RF IC elements designed and manufactured in the Radiation Hardening Fully-Depleted Silicon-On-Insulator process that deliver cost effective performance for connected and low power applications, with a superior radiation immunity >30x/1000x lower SCU/MCU SER. FD-SOI very small sensitive volume and very low bipolar gain offers maximum protection against neutrons, alphas, heavy ions, protons, muons, thermal and low energy protons. The reduced pitch size provides tolerance to total ionization dose. This makes this process the best candidate for Satellite Communication in the space environment[2]. (the advantages and more about SOI technology will be elaborated in Chapter 4)

(a) CUBE Satellite [3]

(b) LEO Satellite [4]

2.3 Noise in Electronic Systems

The term noise in the broadest sense can be defined as any unwanted disturbance that obscures or interferes with a desired signal, remarkably altering its quality and generally the performance of the electronic system [5].

The problems caused by electrical noise are apparent in the output device of an electric system, but the sources of noise are unique to the low-level portions of the system. For

example, the snow that may be observed on a television receiver display is the result of internally generated noise in the first stages of signal amplification. Noise is a totally random signal, consisting of frequency components that are random in both amplitude and phase. Although the long-term rms value can be measured, the exact amplitude at any instant in time cannot be predicted. If the instantaneous amplitude of noise could be predicted, noise would not be a problem. It is possible to predict the randomness of noise. Much noise has a Gaussian or normal distribution of instantaneous amplitudes with time. The Gaussian distribution predicts the probability of the measured noise signal having a specific value at a specific point in time.

$$p(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}}$$

where $p(x)$ is a probability density function, μ is mean value, σ is standard deviation σ^2 standard deviation of variable x.
The area under the curve in **Figure 2.3** represents the probability that a particular event will occur

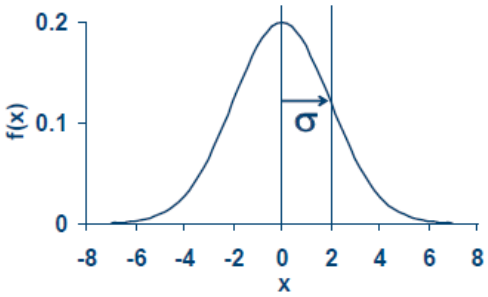


Figure 2.3: Gaussian Distribution of Noise [6]

A noise signal with a Fundamental or true noise cannot be predicted exactly nor it can be totally eliminated but it can be manipulated and its effects minimised.

Noise is an extremely important parameter in analog design. It should be noted that the mentioned shifts in the value of voltage or current do not carry any useful information but only create problems in interpreting the signal. The sources that introduce noise in the system vary as presented below:

2.3.1 Thermal Noise

Firstly, thermal noise, also known as Johnson-Nyquist noise, originates from the random movement of charge carriers inside an electrical conductor caused by thermal energy.

This type of noise is the most often encountered and considered first. It increases with temperature and poses a difficult obstacle when designing low-noise electronics. It is present in all of the electronic components, including resistors, diodes, and transmission lines. and transistors. Thermal noise is nearly white, which means that its power spectral density is almost equal throughout the frequency spectrum. The term "white" suggests that the Noise consists of numerous frequency components, similar to how white light is composed of all colors in the spectrum. The name colored noise is used in situations where the power spectrum is not white. Examples of colored noise spectra are low-pass, high-pass, and band-pass processes [7]. The amplitude of the signal follows closely a Gaussian

probability density function. A communication system affected by thermal noise is often modeled as an additive white Gaussian noise (AWGN) channel.

The strength of thermal noise depends mainly on temperature bandwidth and bias. Higher temperatures and wider bandwidths increase thermal noise levels. Designers should carefully consider these factors to prevent limitations in sensitivity and performance, especially in critical applications like communication systems, medical devices, and scientific instruments where a high signal-to-noise ratio (SNR) is crucial.

The following formula describes the frequency dependence of thermal noise:

$$S_v = 4 \cdot K_B \cdot T \cdot R \qquad (V^2/Hz) \qquad v_n^2 = 4 \cdot K_B \cdot T \cdot R \cdot \Delta f (V^2)$$

where K_B is the Boltzmann constant, T is the absolute temperature and R is the resistance [6].

A more detailed approach on Thermal Noise in MOS Transistors is presented in 4.5.

2.3.2 Flicker Noise

Another important type of noise is flicker noise or $\frac{1}{f}$ noise which is more usually observed in low frequencies and mostly appears in semiconductor devices. When first observed in vacuum tubes, this noise was called "flicker effect," probably because of the flickering observed in the plate current. 1/f noise not only is observed in vacuum tubes, transistors, diodes, and resistors, but it is also present in thermistors, carbon microphones, thin films, and light sources. The fluctuations of a membrane potential in a biological system have been reported to have flicker noise. No electronic amplifier has been found to be free of flicker noise at the lowest frequencies. The reason flicker noise occurs is due to a variety of mechanisms such as mobility fluctuations, traps associated by contamination and crystal defects, making it a crucial aspect in electronic system design. However, this form of noise does not affect the performance of LNAs.

$$S_{\frac{1}{f}}(f) = K \cdot \frac{I^b}{f^a} \qquad (A^2/Hz), \qquad i_n^2 = K \frac{I^b}{f^a} \Delta f \qquad (A^2)$$

Where $a = 1$, $0.5 \leq b \leq 2$ Note that the power spectral density of $\frac{1}{f}$ depends on frequency[8].

2.3.3 Shot Noise

Lastly, shot noise, named after Schottky, is a notable noise current mechanism found within transistors, diodes, and vacuum tubes. This phenomenon arises from the discrete nature of electric charge when the current flow comprises discrete packets, or quanta. In the case of devices like forward-biased silicon diodes, the pulsing flow of current occurs as Electrons and holes cross the potential barrier, with each carrying a charge represented by q. This granular effect results in variations known as shot noise. Essentially, the current flowing in these devices is not smooth and continuous; rather, it is the sum of the pulses caused. by the flow of carriers, each carrying one electronic charge. Shot noise becomes particularly evident in low current or weak signal conditions, impacting the stability and reliability of electronic components. It introduces random fluctuations in current as electrons arrive at a detector in a statistically variable manner, adding an element of unpredictability to the performance of diodes and transistors. Understanding and managing shot noise are crucial aspects of optimizing the behavior of these electronic devices:

$$S_i(f) = 2ql, f \geq 0 \qquad (A^2/Hz) \qquad i_g^2 = 2qI_r\Delta_f \qquad (A)$$

where q is the electronic charge $1.6 \cdot 10^{-19} C$, I_r is the reverse current and Δ_f is the noise bandwidth in Hz [9].

It is important to realize the influence of noise on a signal's quality. Certainly, noise introduces interference and challenges in separating the actual signal from the unwanted disturbances. It is worth mentioning that noise affects the signal-to-noise ratio by degrading the system's ability to transmit and receive information with accuracy.

Taming noise for optimal system performance, low-noise components, different filtering techniques, or even signal processing algorithms are introduced in the design. Many communication applications aim for reliable signal reception and accurate data transmission, so maintaining a high SNR is of utmost importance. Therefore, a careful balance between signal amplification and noise reduction should be pursued.

Chapter 3

Low Noise Amplifier Design Considerations

3.1 Key Parameters in LNA Design

As mentioned before, LNAs consist the first stage of receivers and thus play a critical role in the overall performance, and their design is governed by the following parameters: presented in [10]:

3.1.1 Noise Figure

The noise figure (NF) of a low-noise amplifier (LNA) is a critical parameter directly impacting the overall noise of a receiver system. LNAs, designed to receive and amplify weak signals, encounter an attenuated input signal comprising both the transmitted signal and antenna-generated noise. Minimizing the noise introduced by the amplifier is essential for achieving high signal power with a favorable signal-to-noise ratio (SNR). This is encapsulated by the noise factor (F):

$$F = \frac{SNR_{in}}{SNR_{out}} \qquad (dB)$$

The Noise Figure, expressed in decibels serves as a metric for the amplifier's noise performance.

$$NF = 10 \cdot log(F) \qquad (dB)$$

In an ideal scenario, the noise factor of a noiseless LNA equals unity.

Beyond individual component considerations, the importance of low noise in LNAs influences total system performance. Pursuing low noise imposes constraints on circuit topology choices, particularly in cases with strict noise specifications, rendering some existing LNA topologies unsuitable and imposing limitations on the number of amplifying stages.

$$NF = 10 \cdot log(F) = 10 \cdot log(\frac{SNR_{in}}{SNR_{out}}) \qquad (dB)$$

3.1.2 Gain

The gain of the LNA is also an important aspect when designing since it should be large enough to eliminate the noise contribution of the following stages as presented with the Friis formula. However, the pursuit of high gain introduces a compromise between noise figure and receiver linearity. Increased gain highlights the non-linearity of subsequent stages, presenting a design challenge to strike a balance between optimal noise performance

and receiver linearity. In modern RF design, the LNA directly drives the down-conversion mixer without impedance matching, making it more meaningful and simpler to perform chain calculations in terms of voltage gain rather than power gain. Nevertheless, with a 50 Ω input and output impedance-matched LNA, voltage and power gain coincide.

Various power gain types are often employed in LNA design. For instance, Transducer power gain (G_T) signifies the ratio of power delivered to the load to power available from the source. Operating power gain (G_P) represents the ratio of power delivered to the load to power absorbed at the input. Available power gain (G_AV) indicates the ratio of available output power to available power from the source.Simplified expressions for these power gains, using S-parameters, can be found in the following equations. Typically, LNA power gain is simplified to transducer power gain, specifically equal to S_{21}^2. [2]

$$G_T = |S_{21}^2| \qquad G_P = \frac{1}{1-|S_{11}^2|}|S_{21}^2|, \qquad G_{AV} = |S_{21}^2|\frac{1}{1-S_{22}^2}$$

3.1.3 Bandwidth Considerations

The LNA should deliver a fairly consistent response across the frequency range of interest, ideally with a gain variation of less than 1 dB. To ensure this, the LNA's 23-dB bandwidth must significantly exceed the actual band, preventing gain variations beyond 1 dB at the edges. Quantifying the challenge in achieving the required bandwidth, we often reference the "fractional bandwidth," calculated by dividing the total 23-dB bandwidth by the center frequency of the band.

3.1.4 Input and Output Impedance Matching

The input impedance, meaning the impedance at the input port of the amplifier, serves a determining purpose in the design. The main reason for performing the so-called input Impedance matching is a step necessary for maximizing power transfer from the source to the amplifier, improving the overall performance. Moreover, proper impedance matching can help optimize the noise figure of the LNA and contribute to the stability of the LNA.

The band-select filter placed between the antenna and the LNA is usually designed and evaluated as a high-frequency device with a standard termination impedance of 50 Ω. If the load impedance experienced by the filter corresponds to the LNA input impedance deviates significantly from 50 Ω, which can result in adverse effects on the pass-band and stop-band characteristics of the filter, leading to increased loss and ripple.

In the absence of a filter, the antenna directly delivers the incoming signal to the LNA, and it is typically designed for a specific real load impedance, commonly 50 Ω. Therefore, to attain input matching, the LNA should have an input impedance of 50 Ω (corresponding to $\Gamma = 0$). It's important to note that in this scenario, power matching is equivalent to impedance matching. Inadequate matching at the receiver input can result in reflections, signal loss, and potential voltage attenuation. The input match quality is indicated by the input "return loss," which is the relationship between reflected power and incident power, specifically for a source impedance of R_S:

$$\Gamma = |\frac{Z_{in} - R_S}{Z_{in} + R_S}|^2$$

It is important to mention that achieving correct input (conjugate) matching for LNAs involves employing specific circuit techniques to obtain a real part of 50Ω in the input impedance without the introduction of noise from a 50Ω resistor. Similarly, achieving output impedance matching is crucial when considering the LNA as a standalone circuit. Often, for measurement convenience, the output impedance is also set to 50Ω. Alternatively, the input impedance of the LNA should align with that of the mixer.

3.1.5 Power Consumption

The LNA inherently involves a trade-off between noise, linearity, and power dissipation. Despite this, in most receiver designs, the LNA's power consumption constitutes only a small portion of the overall power. In practical terms, the circuit's noise figure tends to be more critical than its power dissipation. As technology scales, the demand for lower-power circuits intensifies. However, diminishing supply voltage poses a challenge, potentially limiting the design of circuits with adequate signal integrity at reasonable power consumption. While the LNA typically consumes a small fraction of the overall receiver power, in scenarios where power is a primary concern, such as portable devices, careful consideration of power dissipation becomes imperative during the design process. LNA designers need to efficiently balance figures of merit, including noise, linearity, and gain, considering trade-offs among them.

3.1.6 Linearity and Distortion

In the majority of applications, the linearity of the receiver is not constrained by the LNA. The cumulative gain across the receive chain typically shifts the limitation of the overall input third-order intercept point (IP3) or 1 dB compression point (P1dB) to later stages, such as base-band amplifiers or filters. Consequently, when designing and optimizing LNAs, concerns about their linearity are often minimal. However, an exception to this general rule emerges in "full-duplex" systems, where simultaneous transmission and reception occur. In such scenarios, the linearity of the LNA becomes crucial. Additionally, in wide-band receivers that may encounter numerous strong interferers, the linearity of the LNA plays a significant role. It's noteworthy that, in the context of LNAs, attention to distortion characteristics, like inter-modulation distortion, is essential to ensuring optimal performance in various operational scenarios.

3.1.7 Stability

Unlike other components in a receiver, the LNA interacts with the external environment, facing unpredictable source impedance variations. For instance, if a cell phone user grips the antenna, it alters the antenna impedance. Consequently, the LNA must maintain stability across all source impedances and frequencies. While one might assume the LNA only needs to operate within the desired frequency band, any tendency to oscillate at other frequencies leads to highly nonlinear behavior and severely compressed gain.

Circuits' stability is often assessed using the "Stern stability factor" (K), defined as

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}| \cdot |S_{12}|)}$$

.Where Δ is defined by: $\Delta = S_{11}S_{22} - S_{12}S_{21}$.

If $K > 1, \Delta < 1$, the circuit is unconditionally stable, indicating it won't oscillate with any source or load impedance combination. In modern RF design, the well-controlled load impedance of the LNA makes K a conservative stability measure. Moreover, the mismatch between the LNA output and the mixer input renders S_{22} irrelevant in this context.

LNAs may encounter instability due to parasitic inductances from the ground and supply, especially in packaging and on-chip line inductances at higher frequencies. For instance, a significant series inductance at the gate terminal of a common-gate transistor can induce substantial feedback, leading to instability. Thus, careful design, layout considerations and accurate package modeling are imperative precautions.

3.2 LNA Topologies for mmWave Frequencies

Several circuit topologies exist to meet the primary objectives of LNA design. In this section, the most important points of amplifier topologies will be briefly presented, including classical common gate, common source, and cascode stages, along with a discussion of their advantages, challenges, and adjustments necessary to meet specific specifications based on the theory discussed in [10] and [11]

3.2.1 Common-Source LNA with Inductive Load

Typically, the compromise between voltage gain and supply voltage in the common source (CS) stage with a resistive load proves insufficient due to inadequate matching and limitations on operation at high frequencies caused by the output node time constant. The trade-off between voltage gain and supply voltage in this setup becomes less favorable as technology scales down. For example, at low frequencies:

$$|A_v| = g_m R_D = \frac{2I_D}{V_{GS} - VTH} \cdot \frac{V_{RD}}{I_D} = \frac{2V_{RD}}{V_{GS} - V_{TH}}$$

To address this issue and enable operation at higher frequencies, an inductive load can be integrated into the CS stage, as depicted in **Figure 3.1(a)**. This topology allows operation with very low supply voltages because the inductor sustains a smaller DC voltage drop compared to a resistor. Additionally, L_1resonates with the total capacitance at the output node, enabling much higher operational frequencies than the resistively loaded counterpart.

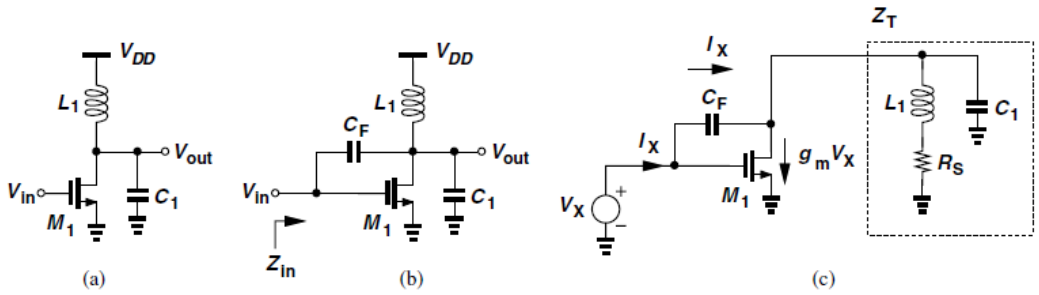


Figure 3.1: Common Source LNA Topology with Inductive Load [10]
(a) Inductively loaded CS stage, (b) Input Impedance in presence of C_F, (c) Equivalent Circuit

The circuit in **Figure 3.1.b** is thought to be more comprehensive, where C_F represents the gate-drain overlap capacitance. Temporarily disregarding the gate-source capacitance of M1, the objective is to calculate Z_{in}. The circuit is modified in **Figure 3.1.c** and observe that the current passing through the output parallel tank equals $I_X - g_m V_X$. Here, we account for inductor loss using a series resistance, R_S, as it exhibits significantly less variation with frequency compared to the equivalent parallel resistance.

The circuit equations suggest that it's feasible to choose suitable values to achieve $ReZ_{in} = 50\Omega$ and attain the desired input matching.

Although offering the potential for $ReZ_{in} = 50\Omega$ at the desired frequency, the feedback capacitance in (b) may introduce negative input resistance at different frequencies, which could lead to instability. In order to counteract the impact of C_F within a certain frequency range, parallel resonance can be employed. However, this approach will introduce notable parasitic capacitances at both the input and output, leading to performance degradation.

3.2.2 Cascode CS Stage with Inductive Degeneration

The examination of the CS stage depicted in **Figure 3.1(a)** suggests that utilizing feedback via the gate-drain capacitance could potentially generate the necessary real part. However, this approach also results in negative resistance at lower frequencies. Therefore, a topology where the input is "isolated" from the inductive load and the input resistance is established by means other than and C_{GD} needs to be found.

Active devices need to be utilized to achieve a 50Ω input resistance without introducing the noise associated with a 50Ω resistor. One method to accomplish this involves employing a CS stage with inductive degeneration, as depicted in **Figure 3.2**.

The computation of the input impedance of the circuit contains a frequency-independent real part, thus, it can be chosen to be equal to 50Ω.

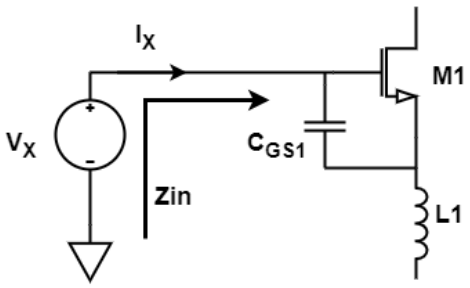


Figure 3.2: Input impedance of inductively-degenerated Common Source stage [1]

In practical implementations, the degeneration inductor is commonly implemented using a bond wire. This choice is driven by the fact that bond wires are inherent in packaging and thus need to be integrated into the design.

Besides C_{GD}, the input pad capacitance of the circuit also contributes to reducing the input resistance. The application of this effect in an equivalent circuit, 2 observations are made:

- The gate-drain and pad capacitance effects imply that reducing the transistor f_T excessively to achieve $R_1 = 50\Omega$ may not be necessary.
- Since the degeneration inductance required for $\mathrm{Re}\{Z_{\mathrm{in}}\} = 50\Omega$ is inadequate to resonate with $C_{\mathrm{GS}} + C_{\mathrm{pad}}$, an additional inductor must be placed in series with the gate, as illustrated in Fig. 5.34, with L_G assumed to be off-chip.

How to choose between CS and CG Cascode LNA

The choice between CG and CS LNA topologies depends on the balance between input match robustness and the noise figure lower limit. CG offers accurate input resistance that is relatively unaffected by package parasitics, while CS provides a lower noise figure. CG is preferred for an LNA noise figure around 4 dB, while CS is suitable for lower values. A notable difference between CG and CS LNAs lies in the contribution of the load resistor, $R1$, to the noise figure. In CG, this contribution $(4RS/R1)$ equals 4 divided by the voltage gain from input to output, reaching 0.4 for a typical gain of 10. Conversely, for the inductively-degenerated CS stage, the contribution $(4RS/R1)$ multiplied by $(\omega 0/\omega T)^2$ renders the noise contribution of $R1$ negligible at operation frequencies well below the transistor's f_T.

3.2.3 Common Gate LNA with Inductive Load

The attractiveness of the common-gate (CG) stage for LNA design is attributed to its low input impedance. Due to the shared gain-headroom trade-off experienced by its CS counterpart, consideration is limited to a CG circuit with inductive loading **Figure 3.3 (a)**. In this configuration, resonance with the total capacitance at the output node, including the input capacitance of the subsequent stage, is achieved by L_1, while R_1 represents the loss of L_1. If channel-length modulation and body effect are neglected, R_{in} is determined to be $\frac{1}{g_m}$. Consequently, the dimensions and bias current of M1 are adjusted to ensure $g_m = \frac{1}{R_S} = 50\Omega^{-1}$.

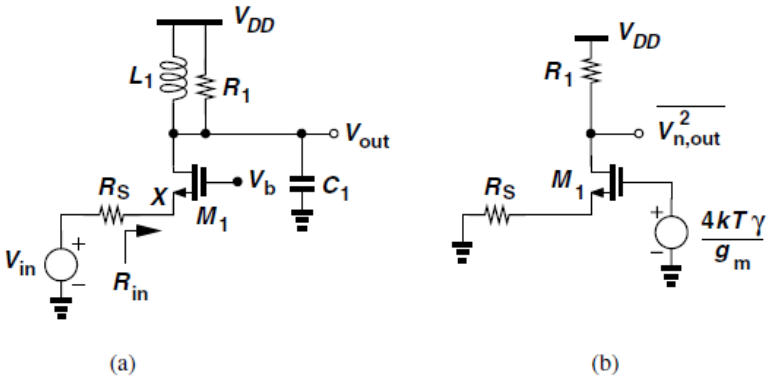


Figure 3.3: Common Gate LNA Topology with Inductive Load from [10]
(a) Inductively loaded CG tage, (b) Effect of Noise of M1

Under the condition where $g_m = \frac{1}{R_S}$ and at the resonance frequency, the noise figure of the circuit is determined. By modeling the thermal noise of $M1$ as a voltage source in series with its gate, and subsequently multiplying it by the gain from the gate of $M1$ to the output, the output noise due to $R1$ can be simply calculated as equal to $4kTR1$. In order to obtain the noise figure, the output noise due to $M1$ and $R1$ is divided by the gain and $4kTRS$, with unity added to the result.

Even when $\frac{4R_S}{R_1} \leq (1 + \gamma$, the noise figure still reaches 3 dB (with γ approximately equal to 1), which is a consequence of the condition $g_m = \frac{1}{R_S}$. In simpler terms, achieving a higher g_m leads to a lower noise figure but also results in a decreased input resistance.

Chapter 4

SOI Technology

4.1 Introduction to SOI Technology

Silicon-on-insulator (SOI) technology has become essential in modern electronic devices, including laptops, mobile phones, and smartphones, forming the basis of complementary metal-oxide-Semiconductor (CMOS) integrated circuits (ICs). Initially, CMOS ICs were built solely on bulk silicon substrates. However, the adoption of SOI offers significant advantages over traditional silicon wafers, such as improved reliability, radiation resistance, a wider temperature range, reduced parasitic capacitances, and enhanced overall device performance and speed. Over the last two decades, the rapid advancement of SOI CMOS technology has been driven by its ability to address fundamental challenges encountered by bulk Si CMOS, especially in downsizing MOSFETs to nanometer scales. Furthermore, SOI enables a decrease in device operation voltage and power consumption, making it highly desirable for modern computing and communication systems.

Traditionally confined to aerospace, nuclear, and military applications due to extreme condition requirements, the widespread adoption of SOI initially faced challenges like limited availability and high costs of high-quality wafers. However, as SOI wafers became more accessible and cost-effective, their applications expanded rapidly, penetrating mainstream ultra-large-scale ICs. This surge in SOI usage can be attributed to factors such as the limitations of bulk Si CMOS technology in MOSFET miniaturization and the increasing demand for high-speed, low-voltage, and low-power operation in consumer electronic devices. Currently, SOI stands as the primary technology for IC manufacturing and crucial electronic components across various applications, from high-performance processors to RF front-end modules (FEMs), ensuring its continuous growth and dominance in the ever-changing landscape of electronic technology [12].

4.1.1 FD vs PD SOI

SOI MOSFETs are categorized into two classes with significant differences in their electrical properties, based on the thickness and doping level of the buried oxide layer: Partially Depleted (PD) and Fully Depleted (FD) SOI MOSFETs.

Partially Depleted (PD) SOI MOSFETs, also known as thick film SOI devices, have a buried oxide layer with nearly double the thickness of the maximum inversion layer in strong inversion (S.I.). Unlike fully depleted SOI devices, in PD devices, the inversion layers at the interface do not extend entirely across the buried oxide, forming a quasi-neutral

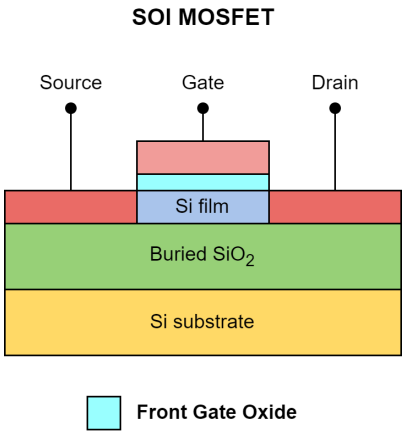


Figure 4.1: Silicon On Insulator MOSFET

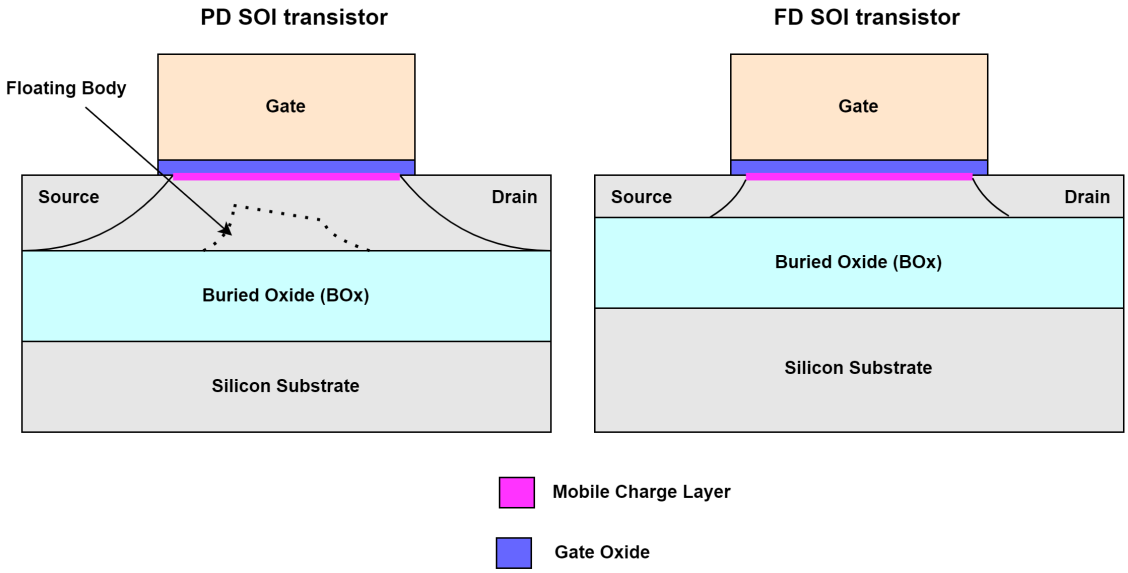


Figure 4.2: Silicon On Insulator MOSFET categories Partially and Fully Depleted

zone. If left electrically floating, this region leads to undesired phenomena called floating body effects. One characteristic effect, known as the "kink-effect," manifests as a sharp increase in drain current (ID) at high drain voltages (VD). The underlying physical process involves impact ionization near the drain, generating electron-hole pairs. In n-channel PD SOI MOSFETs, electrons flow into the drain while holes accumulate near the source, reducing the threshold voltage and causing a stepwise increase in drain current. This effect is less pronounced in p-channel transistors due to lower hole mobility. Floating body effects can lead to hysteresis, parasitic bipolar transistor effects, and dynamic threshold voltage variations. While grounding the body can mitigate these effects, it is not favored in manufacturing. Alternatively, thin-film, fully depleted SOI structures offer a solution devoid of floating-body effects.

Fully depleted (FD) SOI MOSFETs, also known as thin-film SOI MOSFETs, have a silicon film thickness (tSi) less than the maximum depletion layer width. This ensures that the silicon film is fully depleted under threshold and above threshold conditions, except for a possible thin accumulation or inversion layer at the back silicon film surface with significant bias applied to the substrate. As a result, the charge of the depletion layer re-

mains constant and does not increase with increasing gate voltage. Compared to partially depleted devices, FD SOI MOSFETs demonstrate enhanced electrical characteristics, including increased transconductance and carrier mobility due to reduced effective electric field, a sharper subthreshold slope resulting from lower effective substrate capacitance, and improved short-channel performance [13].

4.2 Comparison Between Bulk CMOS and SOI Technology

In this section the advantages of SOI CMOS are presented, while highlighting the technology's abilities in overcoming challenges commonly encountered in Bulk Si CMOS devices.

Enhanced reliability and radiation hardness of SOI CMOS to transient radiation effects

Bulk Si CMOS ICs face a significant challenge known as latch-up, wherein unintentional activation of the parasitic thyristor structure creates a low-impedance path. This can result in temporary malfunction or permanent damage and is triggered by factors like ionizing radiation and voltage spikes. In contrast, SOI CMOS devices lack the wells that contribute to this issue, making them immune to latch-up. Additionally, while SOI CMOS devices have high radiation hardness due to lower ionization currents, they still experience cumulative dose effects, which can be managed through techniques like thinning gate dielectrics and using radiation-resistant dielectrics. Furthermore, SOI CMOS devices also address the specific issue of radiation-induced positive charge accumulation in the buried S_iO_2 layer through techniques like deep ion implantation and the application of negative substrate bias during irradiation [14].

Reduced parasitic capacitances and higher operation speed

In CMOS devices, the primary parasitic capacitance of concern is the one between the source and drain regions and the substrate. In bulk devices, this arises from the capacitance of p-n junctions. With the miniaturization of MOSFETs in bulk Si technology, increasing doping concentrations around p-n junctions leads to higher parasitic capacitances. Additionally, reducing the supply voltage in bulk CMOS circuits further elevates the parasitic drain capacitance. In thin-film SOI CMOS devices, where p-n junction regions extend to the buried SiO2 layer, the parasitic capacitance of junctions represents a MOS structure formed by a highly doped region of the p-n junction, buried dielectric, and substrate. This capacitance is proportional to the dielectric constant of the buried dielectric layer, typically SiO2, which is lower than that of Si. Therefore, the drain and source junction capacitances in SOI CMOS devices are significantly lower compared to their bulk Si counterparts [12]. Furthermore, in SOI devices, using a high-resistivity Si substrate can further reduce parasitic capacitance. The presence of a thick buried oxide in SOI devices not only reduces drain/source p-n junction capacitances but also other parasitic capacitances, leading to a notable increase in operation speed compared to bulk counterparts.

Operation in high and cryogenic temperatures

Conventional bulk silicon CMOS devices are limited to moderate temperatures of $\leq 150 \ldots 200°C$ due to issues such as increased off-state leakage current, temperature-induced latch-up, and threshold voltage shifts. In contrast, thin-film SOI CMOS devices

can operate at temperatures up to 300–400 °C due to several advantages. These include the absence of temperature-induced latch-up, lower off-state leakage current at high temperatures, and weaker variation of threshold voltage and sub-threshold slope with temperature compared to bulk MOSFETs. These advantages make SOI devices suitable for high-temperature electronic applications.

The main advantages of MOS at cryogenic temperatures are associated with increased carrier mobility, better turn-on capabilities, higher saturation velocity, higher thermal and electrical conductivity, lower power consumption, reduced thermal noise, and a decrease in junction leakage currents [15]. In the study discussed [16], 28-nm FD SOI transistor behavior at cryogenic temperature is investigated, showing notable enhancements in various characteristics compared to room temperature. Low-voltage operation is emphasized to minimize heat dissipation. Results also reveal increased gate transconductance with temperature drop due to improved carrier mobility, while resistance values show minimal temperature dependence. Gate capacitances and output conductance remain largely unaffected by temperature, with transconductance primarily influencing cutoff frequencies.

Simplicity of FD SOI Integration

Scaling beyond 28nm with bulk CMOS technologies necessitates increased complexity, involving additional masks, process steps, and the adoption of new processes, materials, and tools to enhance the conformality and controllability required for FinFET 3D integration. These advancements result in escalated manufacturing costs and other non-recurring engineering expenses, encompassing design flow, design verification, and mask sets, among others. In contrast, an FD-SOI device is manufactured on a thin layer of silicon (TSi) atop a thin BOX substrate, with a ground plane formed on the handling substrate. It predominantly relies on existing CMOS manufacturing processes and tools, featuring a simpler process flow [17].

F_T and F_{max} Comparison

As studied in [18], the differences in F_T and F_{max} values in PMOS and NMOS transistors are much lower for the 45 nm RF-SOI CMOS technology compared to the 40nm bulk CMOS. Hence, it seems advantageous for applications that can benefit from truly complementary CMOS circuitry, such as high-speed digital and mixed-signal blocks, and wherever it is needed to achieve lower power consumption.

4.3 Super Low VT FD SOI Technology Performance

Examining the performance of SOI transistors holds paramount significance. The measurements of the Super Low VT (SLVT) NFET discussed in this section concern the transistor employed in the LNA design outlined in Chapter 5.

$I_D - V_G$

To begin with, in **Figures 4.3 and 4.4**, the drain current is plotted both in linear and logarithmic scale vs. the gate voltage. The curves were created directly from the measurements of the LNA. The vertical dashed lines demarcate the $V_{th} = 245.1mV$ calculated from the operating point of the transistor, and the V_{GS} at 426.3mV.

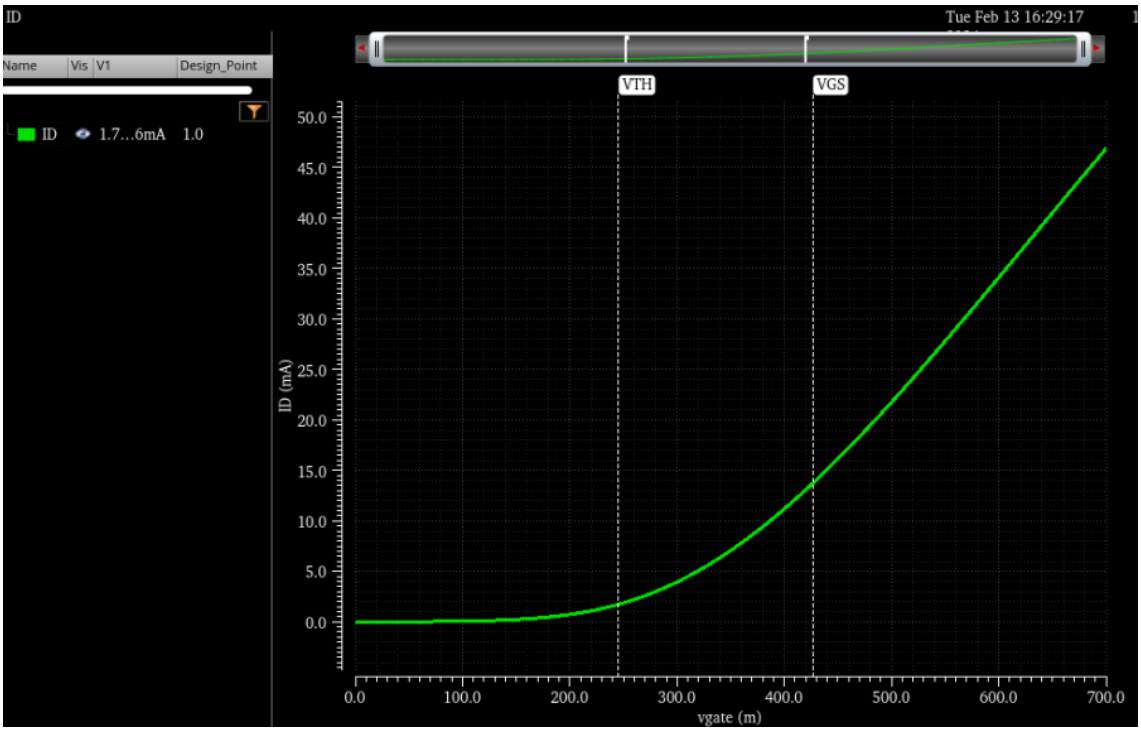


Figure 4.3: Drain Current vs. Gate Voltage Curve

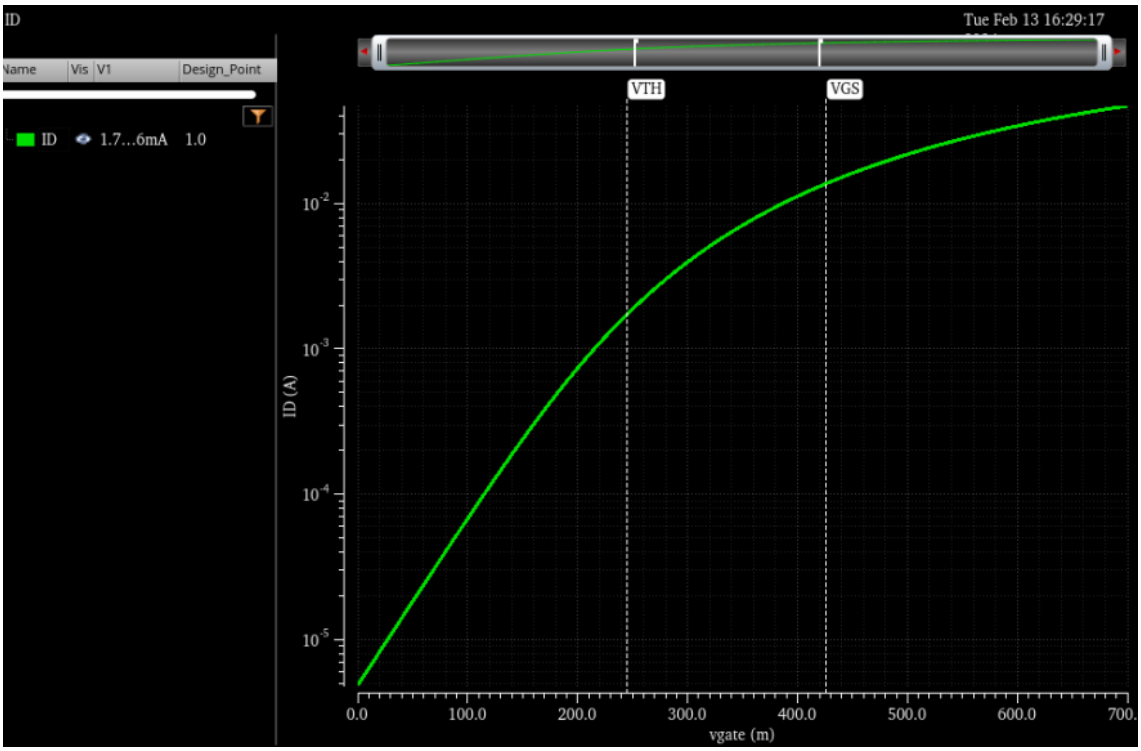


Figure 4.4: Logarithmic Scale of Drain Current vs. Gate Voltage Curve

$I_D - V_D$

In **Figure 4.5, 4.6** the drain current in linear and logarithmic scale vs. drain voltage. The $V_{DS} = 784.5m$ calculated from the operating point of the transistor.

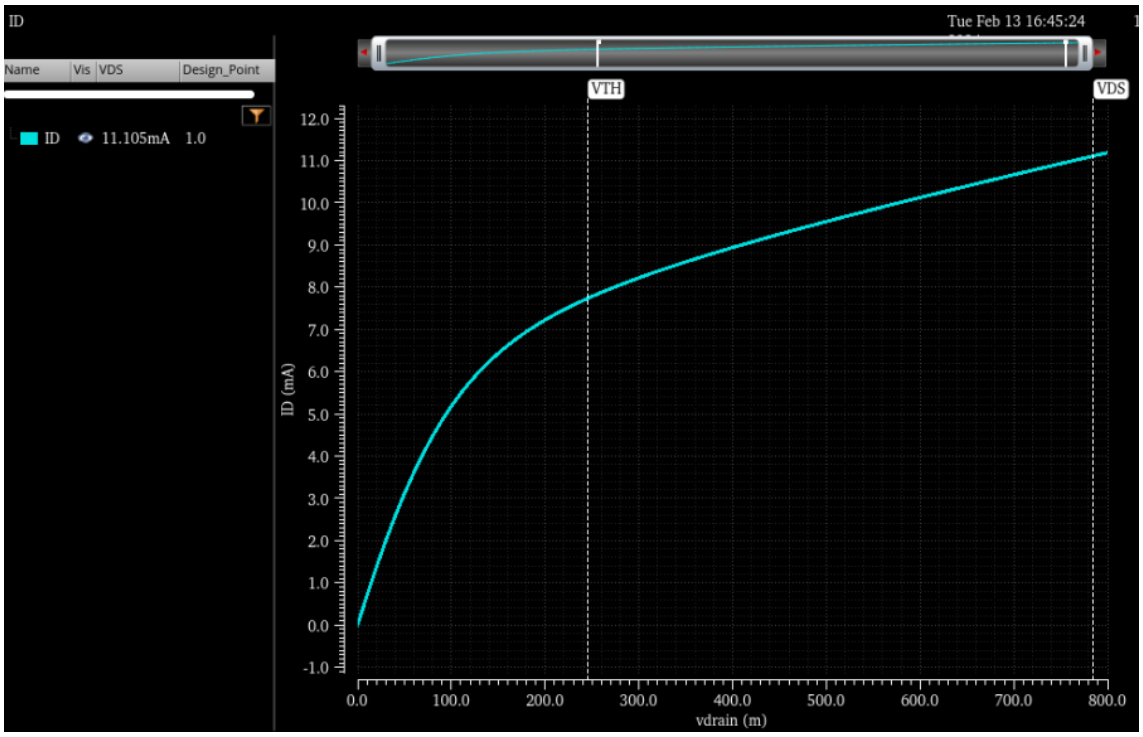


Figure 4.5: Drain Current vs. Drain Voltage Curve

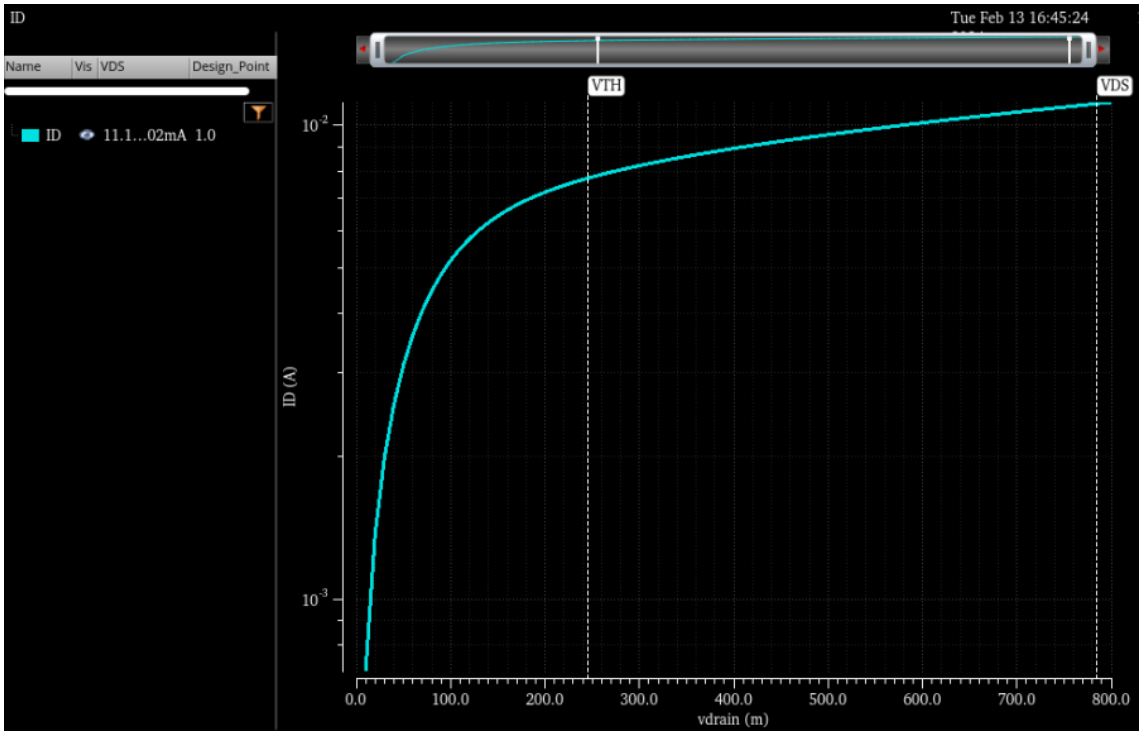


Figure 4.6: Logarithmic Scale of Drain Current vs. Drain Voltage Curve

Transconductance

As pointed out in [19] without doubt, the most important small signal parameter is the gate transcoductance G_m The curve for the transconductance was created by the

derivative of drain current vs. gate voltage **Figure 4.7**

$$\frac{D(I_D)}{D(V_G)} = Gm$$

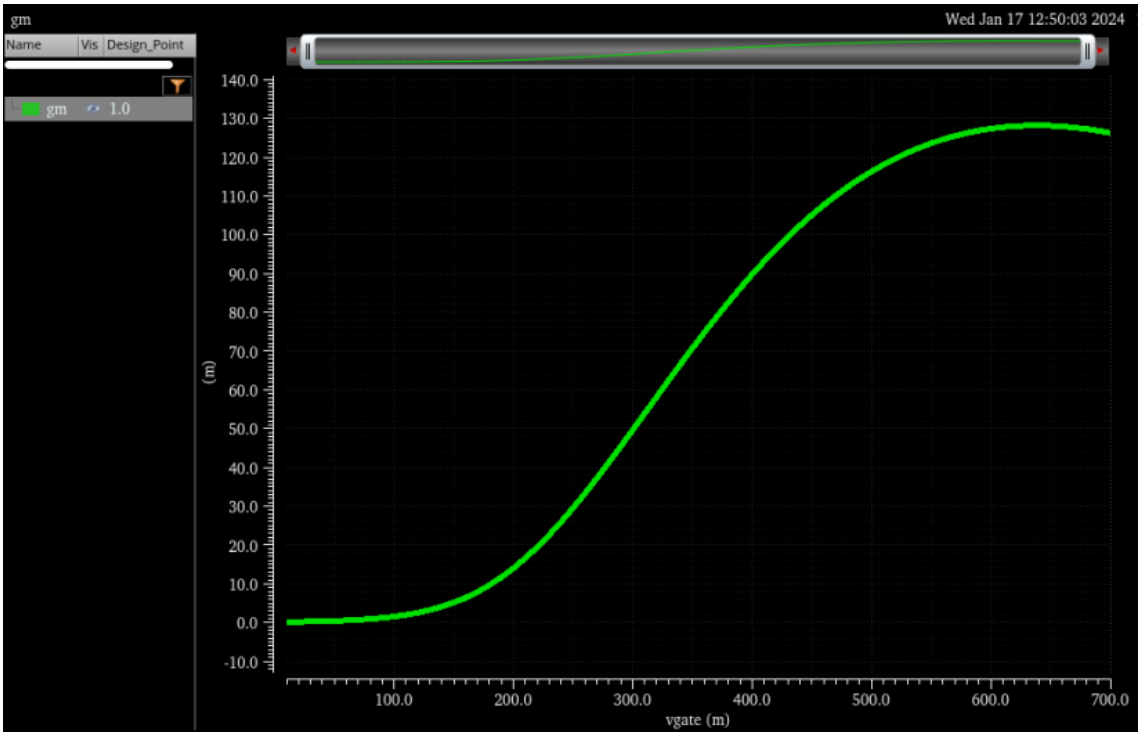


Figure 4.7: Transconductance vs. Gate Voltage Curve

4.4 Design Methodology Based on Inversion Coefficient

4.4.1 Concept of Inversion Coefficient

The continual aggressive downscaling of CMOS processes and the accompanying decrease in supply voltage, driven by the demand for low-power, highly efficient designs, have shifted the operating point away from traditional strong inversion towards moderate and weak inversion. This trend has sparked a growing interest in the inversion coefficient as a primary design parameter, even in advanced technologies, as it serves as a measure of channel inversion, normalizing drain current across diverse technological parameters.

The Inversion Coefficient (IC) functions as a measure of the level of inversion within a single MOSFET channel and is mathematically defined as

$$IC = \frac{I_D}{I_{spec}}|_{\text{saturation}}$$

The normalizing factor I_{spec}, known as the specific current, is determined by

$$I_{spec} = I_0 \frac{W}{L}, \qquad I_0 = 2n\mu_0 C_{ox} U_T^2$$

encompassing parameters such as the slope factor (n), constant low-field mobility (μ_0), gate capacitance per unit area (C_{ox}), and thermal voltage ($U_T = \frac{kT}{q}$).

Normalizing the drain current in this manner eliminates any dependence on size and technology from the standardized quantity IC. In a specific technological context, the specific currents per square (Ispec) for each transistor type (n- and p- channel) are foundational parameters for designers. Using IC, the operational regions of a MOSFET can be classified as follows:

$$\begin{aligned} I_C \leq 0.1 &: \text{ weak inversion (WI)}, \\ 0.1 < I_C \leq 10 &: \text{ moderate inversion (MI)}, \\ 10 < I_C &: \text{ strong inversion (SI)}. \end{aligned}$$

4.4.2 Parameter extraction

In this section, the successful application of the simplified EKV model in this work will be presented. The articles [19] and [20] will primarily provide guidance on extracting parameters from characteristics. Throughout the following sections, results based on the observations and notes outlined in the referenced articles will be demonstrated.

Slope Factor n and Specific Current I_{spec} Extraction

The following curves depict the $\frac{G_m \cdot U_t}{I_D} - I_D$ in logarithmic scale , $U_T = 0.0258V$ at $300K$.

The quotient $\frac{W}{L}$ was calculated as shown below:

$$\frac{W}{L} = \frac{72\mu m}{18nm} = 4000$$

where the transistor width is the product of the total transistor width with multiplier value $8\mu m \cdot 9 = 72\mu m$.

The process regarding the sizing of the active device are elaborated in detail in Chapter 5.

The slope factor is extracted from the plateau reached by $\frac{I_D}{G_m \cdot U_t}$ curve in W.I. as shown in **Figure 4.8**. The specific current is obtained by the intersection between the S.I. tangent asymptote $45.6 \cdot \sqrt{I_D}$ and the slope factors horizontal line as shown in **Figure 4.8**. The specific current per square I_0 can be derived by dividing by the aspect ratio $\frac{W}{L} = 4000$ as shown in the formula before.

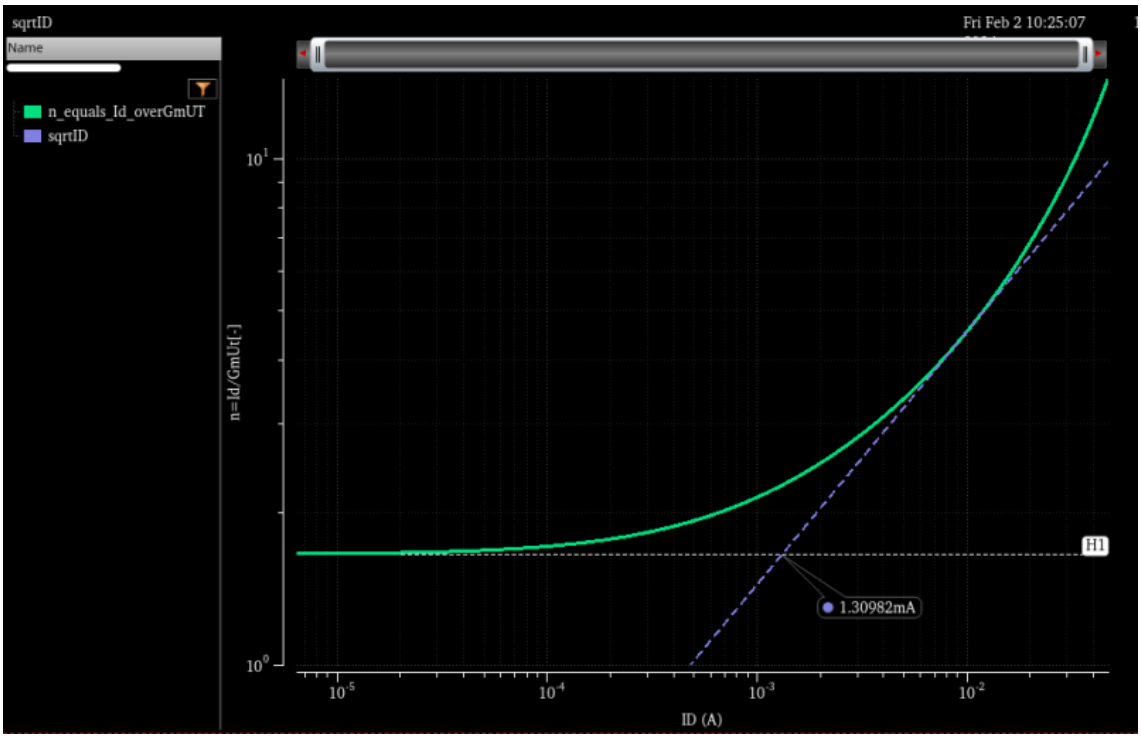


Figure 4.8: The extraction of $Ispec$ and n from $\frac{I_D}{G_m \cdot U_t} - I_D$ (log scale)

For this particular device the parameters have the following values:

Slope Factor and Specific Current Extraction Values	
n	1.65
I_{spec}	$1.13mA$
I_0	$283nA$

Table 4.1: Parameter extraction values

Velocity Saturation λ_c Parameter Extraction

The parameter λ_c is accounting for VS according to $\lambda_c = \frac{L_{sat}}{L}$ and scales inversely proportional to the transistor length. The VS parameter is extracted from the normalised characteristic $\frac{Gm \cdot n \cdot U_t}{I_D} - IC$ from the intersection between the proportional asymptote $\frac{1}{\lambda_c \cdot IC}$ and the slope factor horizontal line **Figure 4.9**

The asymptote of $\frac{Gm \cdot n \cdot U_t}{I_D}$ is found to be the $\frac{1}{0.2 \cdot IC}$ and the interception point is 5 which is verified by the given formula that the intercept equals to $\frac{1}{\lambda_c} = \frac{1}{0.2} = 5$

Also, $L_{sat} = 0.2 \cdot 18nm = 3.6nm$

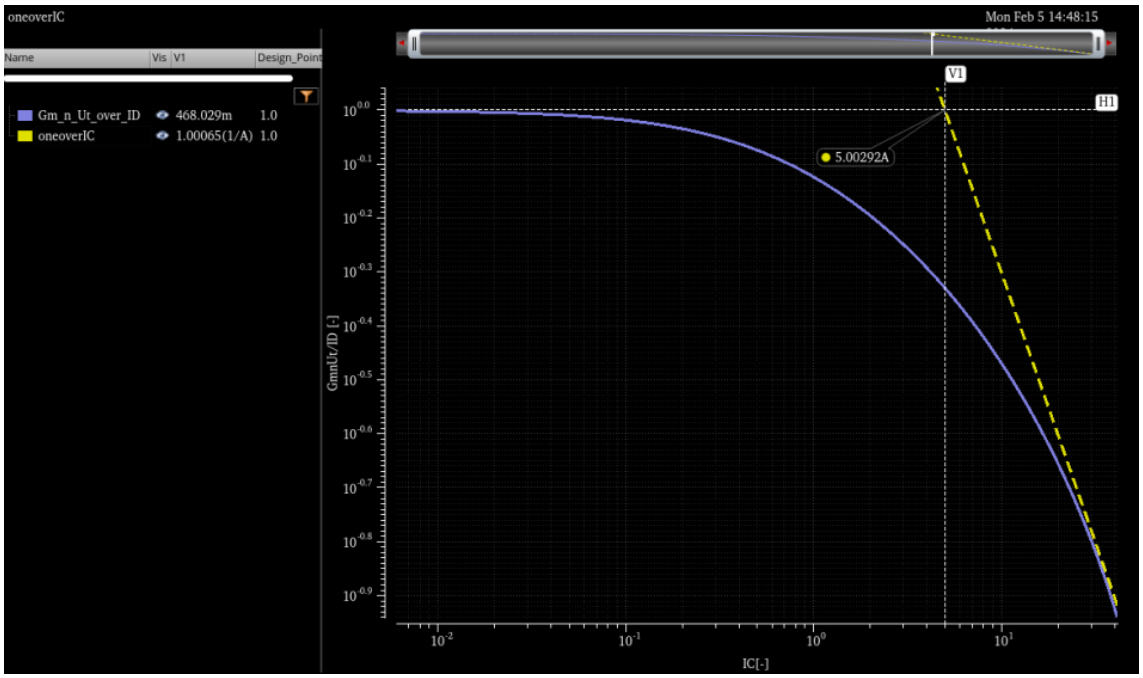


Figure 4.9: VS parameter (λ_c) extraction

The Transconductance Efficiency $\frac{G_m}{I_D}$

Transconductance Efficiency $\frac{G_m}{I_D}$, often called current efficiency, is one of the most important FoMs for low-power analog design. It is a measure of how much transcoductance is produced for a given bias current and is a function of IC, appearing in many expressions related to the power optimization of analog circuits.

$$\frac{G_m \cdot n \cdot U_t}{I_D} = \frac{\sqrt{\lambda_c^2 IC^2 + 2\lambda_c IC + 4IC + 1} - 1}{\lambda_c^2 IC^2 + \lambda_c IC + 2IC}$$

The essence of VS is to degrade the transconductance efficiency in SI, meaning that more current is required to reach the same transcoductance obtained without VS. [21]In **Figure 4.10** , the expression of transconductance efficiency is plotted, including the effect of VS, continuously from WI to SI.

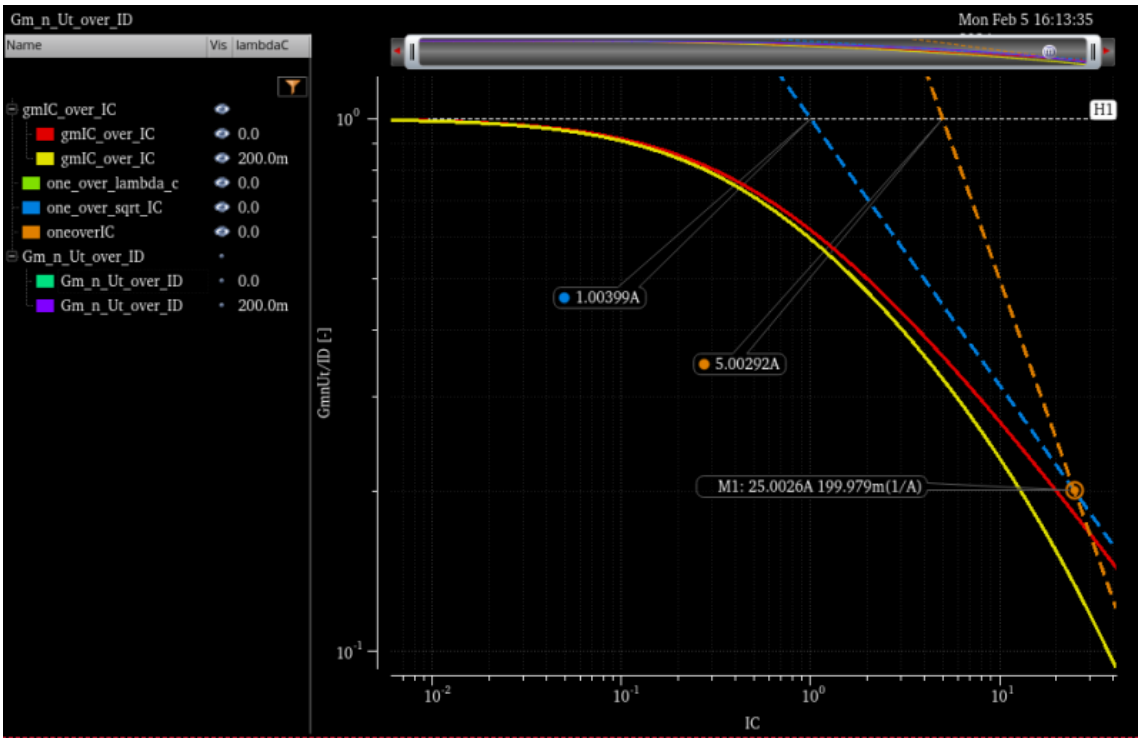


Figure 4.10: $\frac{g_m}{IC}$ presents 2 versions with VS ($\lambda_c = 0.2$) and without VS ($\lambda_c = 0$)

The characteristics plotted present favorable results that verify the theory of [21]. In detail:

- The $\frac{g_m}{IC}$ curve on which VS effect is present, scales as $\frac{1}{\lambda_c IC} = \frac{5}{IC}$
- The $\frac{g_m}{IC}$ curve on which VS is absent, scales as $\frac{1}{\sqrt{IC}}$
- The intersection between the horizontal slope line and $\frac{1}{\sqrt{IC}}$ is equal to 1, which can be interpreted as the demarcation between weak inversion and velocity saturated strong inversion region.
- The intersection between the horizontal slope line and $\frac{1}{\lambda_c \cdot IC}$ is equal to $\frac{1}{\lambda_c} = \frac{1}{0.2} = 5$
- The intersection between the two asymptotes is equal to $\frac{1}{{\lambda_c}^2} = \frac{1}{0.2^2} = 20$

The VS parameter λ_c is inversely proportional to the channel length the strong inversion asymptote of $\frac{g_m s}{IC}$ curve is no more scaling and technology invariant. Due to this dependence on λ_c the curve starts bending inwards towards moderate inversion region [22].

Parameter Fine Tuning λ_c and I_0:

In order to make the measurements and the model match, the parameters were fine tuned to achieve the desired results.

Parameter Values after fine tuning			
Transistor Length	18nm	36nm	90nm
λ_c	0.58	0.28	0.1
I_0	$1000nA$	$1200nA$	$1200nA$
n	1.65	1.39	1.33

Table 4.2: Parameter Values After Fine Tuning for Different Device Lengths

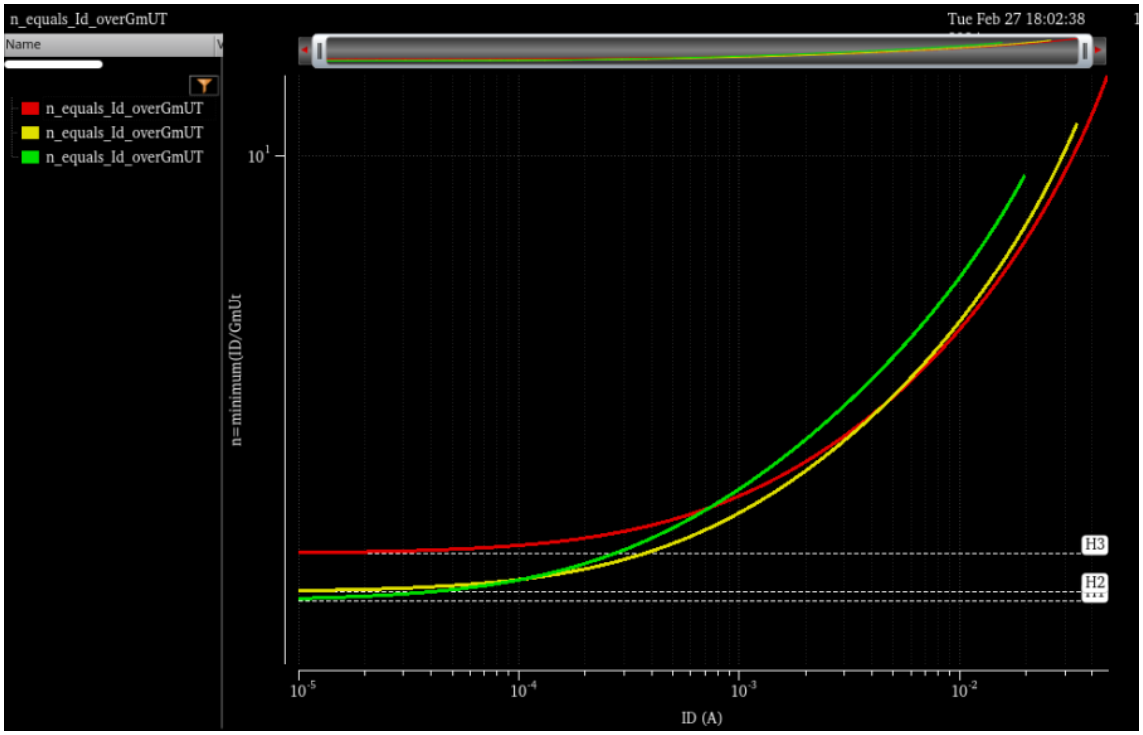


Figure 4.11: Slope factor variation after fine tuning for the different device lengths (18nm, 36nm, 90nm)

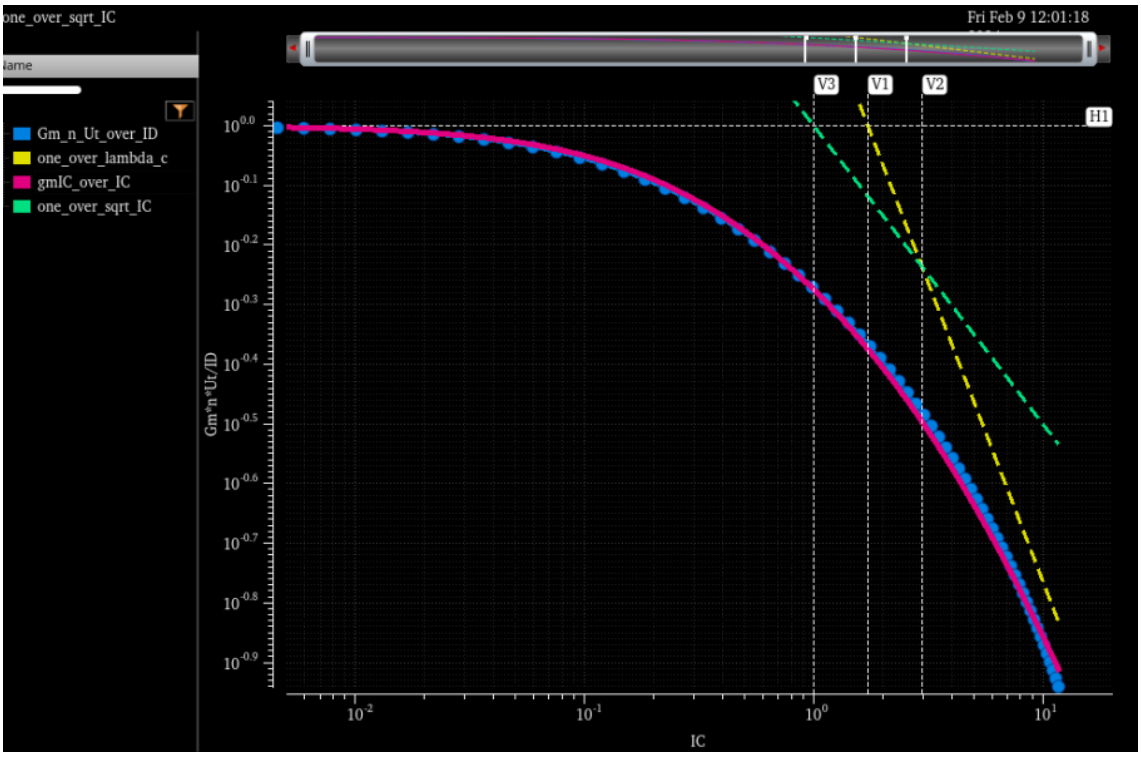


Figure 4.12: $\frac{g_m}{IC}$, $\frac{G_m \cdot n \cdot U_t}{I_D}$ after fine tuning in the original length 18nm

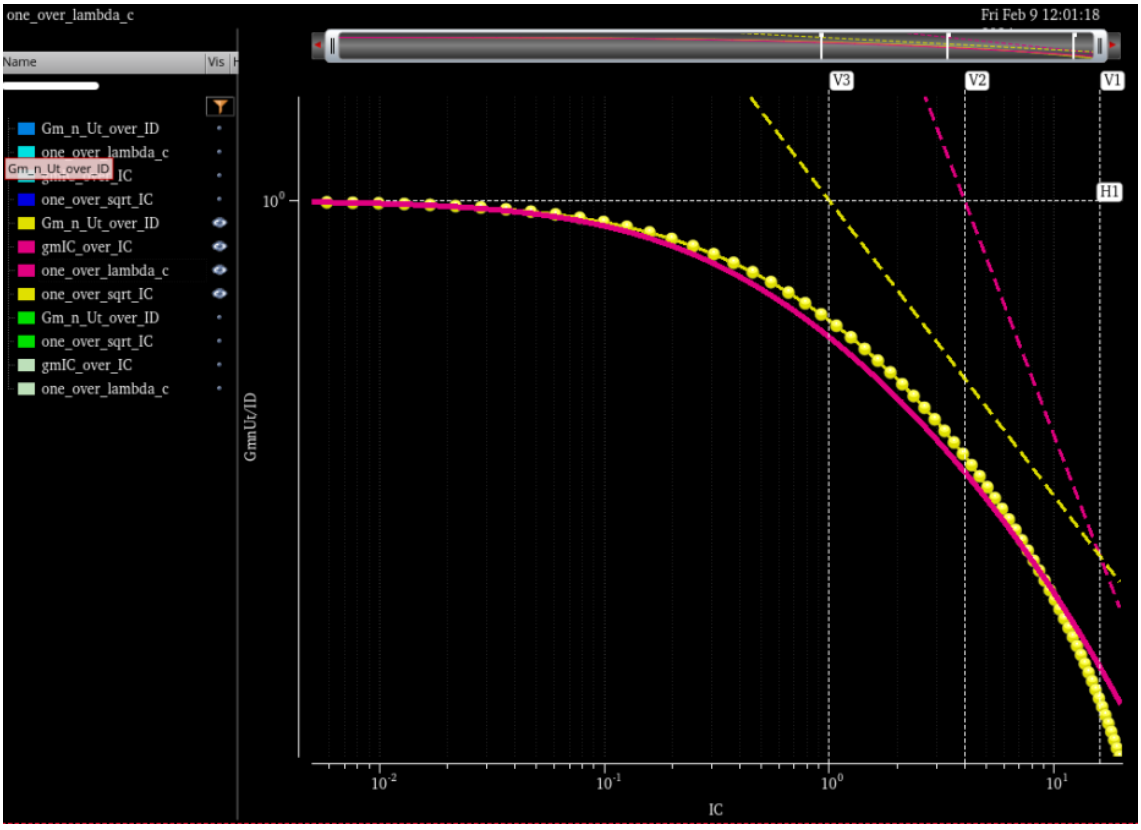


Figure 4.13: $\frac{g_m}{IC}$, $\frac{G_m \cdot n \cdot U_t}{I_D}$ after fine tuning for a device with length 36nm

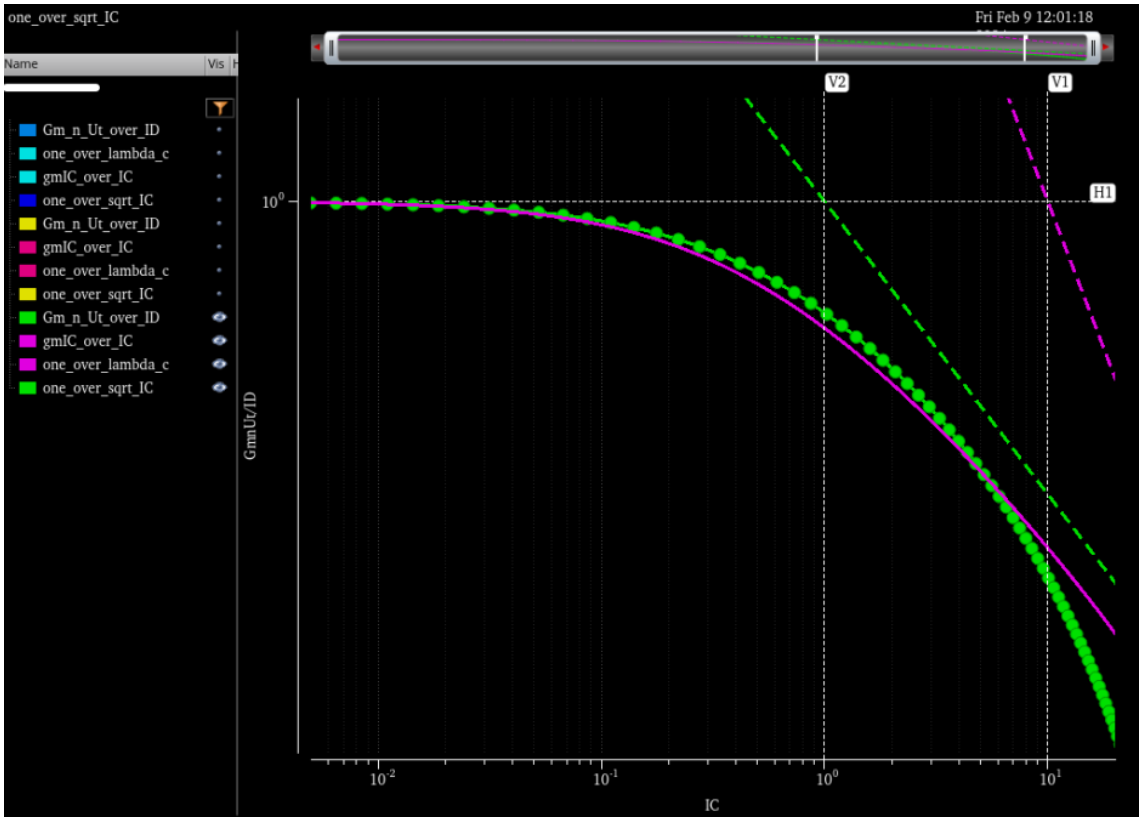


Figure 4.14: $\frac{g_m}{IC}$, $\frac{G_m \cdot n \cdot U_t}{I_D}$ after fine tuning for a device with length 90nm

The same observations made for **Figure4.10** apply and verified in the following characteristics (**Figure 4.12, Figure 4.13, Figure 4.14**)

Transit Frequency f_T

As stated in [19], the transit frequency (f_T) is defined as the frequency at which the extrapolated small-signal current gain of the transistor in CS configuration decreases to unity. f_T is commonly used to characterize the high-frequency behavior of a MOSFET because many performance metrics, such as the gain at RF and the minimum noise factor, are directly related to f_T. A good approximation of f_T is provided by the formula:

$$f_T = \frac{G_m}{2\pi C_G}$$

where $C_G = C_{Gi} + C_{Ge}$ represents the total gate capacitance, comprising the intrinsic capacitance C_{Gi} and the extrinsic capacitance C_{Ge}.

The values of C_{gg} are obtained from the operating points of the transistor through a sweep DC analysis. In **Figure 4.15**, F_{spec} can be defined as the value of f_T on the WI asymptote corresponding to $I_C = 1$.

The normalised transient frequency $f_T = \frac{F_t}{F_{spec}}$.

The $F_{tpeak} = \frac{F_{tspec}}{\lambda_c} = 393.2GHz$

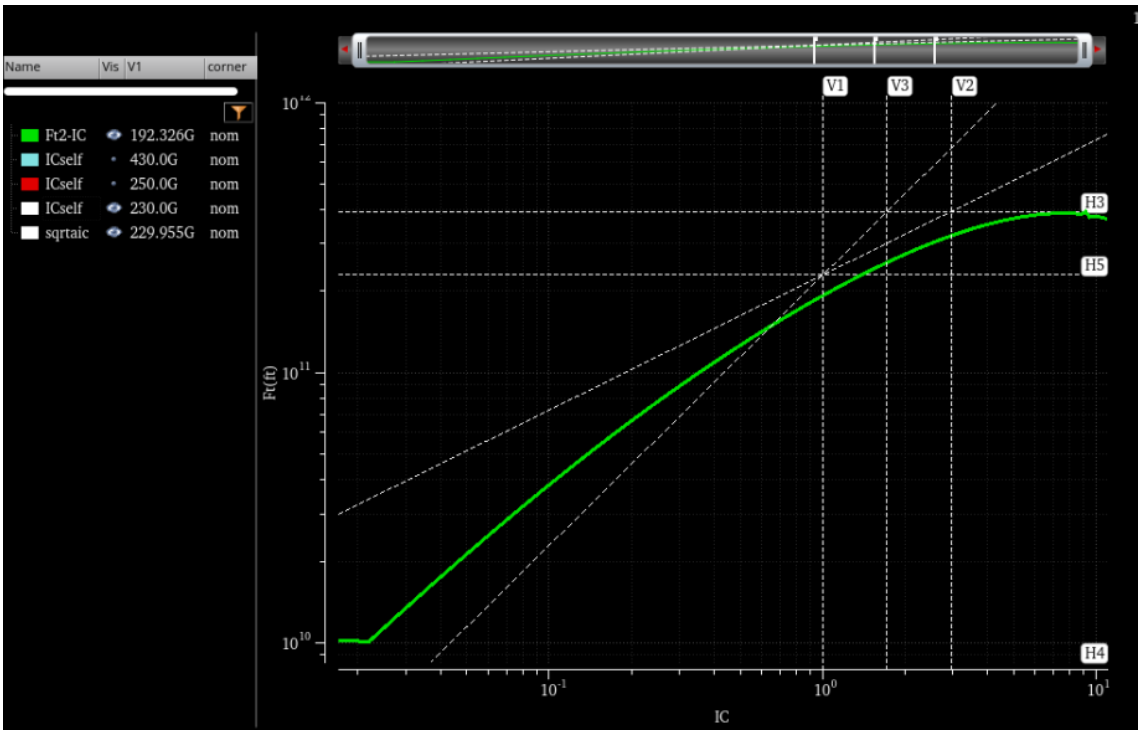


Figure 4.15: Transient Frequency F_t vs. IC - (after fine tuning parameters)

4.4.3 Figure Of Merit

Both $\frac{G_m}{I_D}$ and f_T are critical Figures of Merit (FoMs) from an analog/RF design perspective: the former characterizes the DC performance of a device, while the latter characterizes its high-frequency performance. It can be defined as:

$$FoM = \frac{g_{ms} \cdot f_T}{IC}$$

Targeting low-power operation by aiming for a high $\frac{G_m}{I_D}$ at small values of I_C invariably means compromising on speed (bandwidth). This is where the FoM defined as the product of the two previously mentioned metrics becomes relevant, offering a good trade-off among gain, noise and power consumption. Combining two quantities that have their maxima at opposite ends of the I_C axis, fom_{rf} serves as a design guide to locate the optimum I_C. The **Figure 4.16** shows the 2 FoMs vs. IC, the yellow curve corresponds to measured data and red curve to model data.

Optimal IC value for achieving higher FoM		
	measured data curve	model data curve
FoM	484	470.2
IC	1.94	1.805
v_{gate}	359mV	352mV

Table 4.3: FoM and IC Values based on model and measurement characteristics

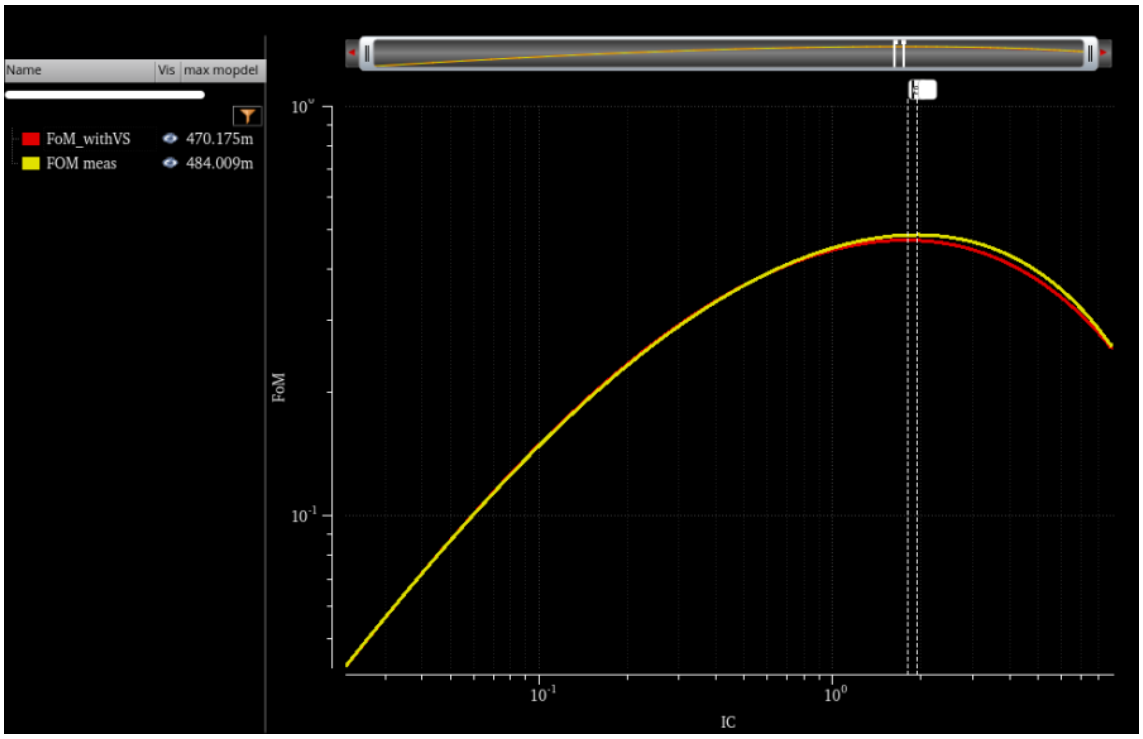


Figure 4.16: FoM normalised on a log scale

4.5 Thermal Noise of MOS Transistors

The thermal noise in MOS transistors presents a complex phenomenon that needs to count for all the short channel effects such as carrier heating, velocity saturation, and channel length modulation. These factors emerge and notably impact thermal noise and described thoroughly in [11],[32]:

Velocity Saturation an Carrier Heating effect on thermal noise

In CMOS technologies, electrons and holes exhibit characteristic electric field (E_c) and saturation drift velocity (v_{sat}). When the longitudinal field (E_x) aligns with E_c along the channel, the drift velocity (v_{drift}) begins to saturate. The critical field is determined by the ratio of saturated drift velocity to the mobility at low longitudinal field (μ_z): $Ec = \frac{v_{sat}}{\mu_z}$. In regions of high lateral electrical field, carriers gain increased energy, leading to heightened collisions with the lattice and subsequently raising carrier temperature as a function of the electric field. This elevation in carrier temperature results in increased thermal noise, emphasizing the interdependence between velocity saturation (VS) and carrier heating (CH). EKV3 accounts for the influence of VS and CH on thermal noise through the dimensionless critical field parameter λc. Higher λc values correspond to stronger short channel effects for a given technology node.

$$\lambda_c = \frac{2Ut}{L_{eff}E_c}$$

Channel Length Modulation effect on thermal noise

In strong inversion, as V_{DS} increases, the MOSFET channel pinches off, reducing the electrical channel length due to increasing electrical field—an effect known as channel

length modulation (CLM). CLM, closely tied to velocity saturation (VS), splits the channel into two regions: the non-saturated and the VS region near the drain. The effective channel length (Leff) represents the non-saturated region, while ΔL denotes the VS region, influenced by gate and drain bias voltages. EKV3 model considers CLM, where noise voltage fluctuations in the VS region do not propagate to the drain, implicating only the active region in channel thermal noise .

4.5.1 Thermal Noise Parameters

According to [33] in MOS transistor design, white noise is characterized by transconductance Gm and the thermal noise excess factor (TNEF) γ_n. Since Gm influences gain and bandwidth, selecting the appropriate Gm is vital for balancing these aspects along with noise. Engineers employ various figures-of-merit (FoMs) to navigate this trade-off effectively. The γ_n serves as a key FoM in low-noise circuit design, assessing noise production for a given transconductance and aiding in determining the necessary transconductance for achieving specified input-referred noise levels or minimum Noise Figure (NF).

In detail, the power spectral density of drain current fluctuations is denoted by

$$S_{\Delta I_D^2} = 4 \cdot K_B \cdot T \cdot G_n$$

where G_n represents the thermal noise conductance, proportional to the integral of the product of mobility and inversion charge density across the channel:

$$g_n = \frac{G_n}{G_{spec}} = \int_0^1 q_i \, d\xi$$

- q_i normalised inversion charge ($q_i = q_s = \frac{Q_i}{Q_spec}$ at the source when ξ=0)
- ξ normalisation parameter for distance $\xi = \frac{x}{L}$
- G_spec normalisation parameter for conductances $G_{spec} = \frac{I_{spec}}{U_T}$
- U_T normalisation parameter for voltages $U_T = \frac{K_B \cdot T}{q}$
- I_{spec} normalisation parameter for currents $I_{spec} = I_0 \cdot \frac{W}{L}$

Van der Ziel characterised Thermal Noise in MOSFETs introducing the following factors:

$$\delta_n = \frac{G_n}{G_{dso}} = \frac{g_n}{g_{dso}}$$

δ_n, is called the *thermal noise parameter* , quantifies the deviation of thermal noise in an active device from that in a passive resistor with conductance G_{dso}. It's primarily used for modeling rather than direct circuit design due to its comparison at a specific operating point.

$$\gamma_n = \frac{G_n}{G_m} = \frac{g_n}{g_m}$$

For circuit design, it's more practical to define the *thermal noise excess factor* (TNEF) γ_n, where *gm* denotes the normalized gate transconductance. γ_n indicates the noise generated relative to transconductance, serving as a useful figure-of-merit (FoM). Unlike δ_n, γ_n evaluates noise conductance and gate transconductance at the same operating point.

- In SI, saturation (with VS)

$$\gamma_{nsat} = \frac{n}{2} \cdot \lambda_c^2 \cdot IC = a_n \cdot IC \qquad \text{with } a_n = \frac{n}{2} \cdot \lambda_c^2$$

- In WI, saturation

$$\gamma_{nsat} = \gamma_{nwi} = \frac{n}{2} \cdot (1 + \frac{\lambda_c}{2})$$

- In WI (with VS)

$$\gamma_{nsat} = \gamma_{nwi} + a_n \cdot IC$$

When applying the model in an LNA design, it's evident that various noise specifications like input-referred noise resistance R_n or minimum noise factor F_{min} incorporate the term $\frac{\gamma_{nsat}}{G_{msat}}$.

- without VS: γ_{nsat} remains constant and G_{msat} increases with IC, hence $\frac{\gamma_{nsat}}{G_{msat}}$ decreases with respect to IC improving the noise performance
- with VS:

$$\frac{\gamma_{nsat}}{g_{msat}} = \alpha_n \cdot \lambda_c \cdot n \cdot IC = \frac{n^2}{2} \cdot \lambda_c^3 \cdot IC \qquad \text{in SI}$$

$$\frac{\gamma_{nsat}}{g_{msat}} = \frac{n \cdot \gamma_{nwi}}{IC} = \frac{n^2(1 + \frac{\lambda_c}{2})}{2IC} \qquad \text{in WI}$$

In a CS LNA the input referred noise resistance R_n is given by

$$R_n = \frac{\gamma_{nsat}}{G_{msat}} + R_G$$

R_G, the gate resistance of the transistor, is significant particularly in advanced CMOS technologies.

$NF_{min} = 10log(F_{min})$, the minimum noise figure represents the lowest achievable noise for a transistor at a specific operating point and frequency, assuming noise impedance matching at the input. An uncomplicated expression for F_{min}, which considers gate resistance noise and induced gate noise (excluding correlation to channel noise and contribution from substrate resistance), is presented.

$$F_{min} = 1 + 2\frac{\gamma_{nsat}}{G_{msat}}\omega C_{GS}\sqrt{\alpha_G + b_n}$$

Upon observation of the above formula, C_{GS} transcoductance is related to the f_T. When $\frac{C_{GS}}{G_m}$ increases, F increases while f_T decreases inversely.

Chapter 5

Low Noise Amplifier Design

The design of this LNA uses as a basis the simplest circuit, Common Source LNA **Figure 5.1**. The process begins by initially determining the basic LNA parameters according to the specifications. The chosen design specifications draw inspiration from commercial LNAs utilized in similar applications, ensuring alignment with established industry standards. The mentioned specifications are related to the NF, the gain, the linearity, and the amplifier bandwidth at a specific frequency of operation. It then advances to optimizing these parameters, substituting ideal components with real ones. The final steps involve the extraction and simulation of the layout mask design. The chapter concludes by comparing this work with other relevant studies.

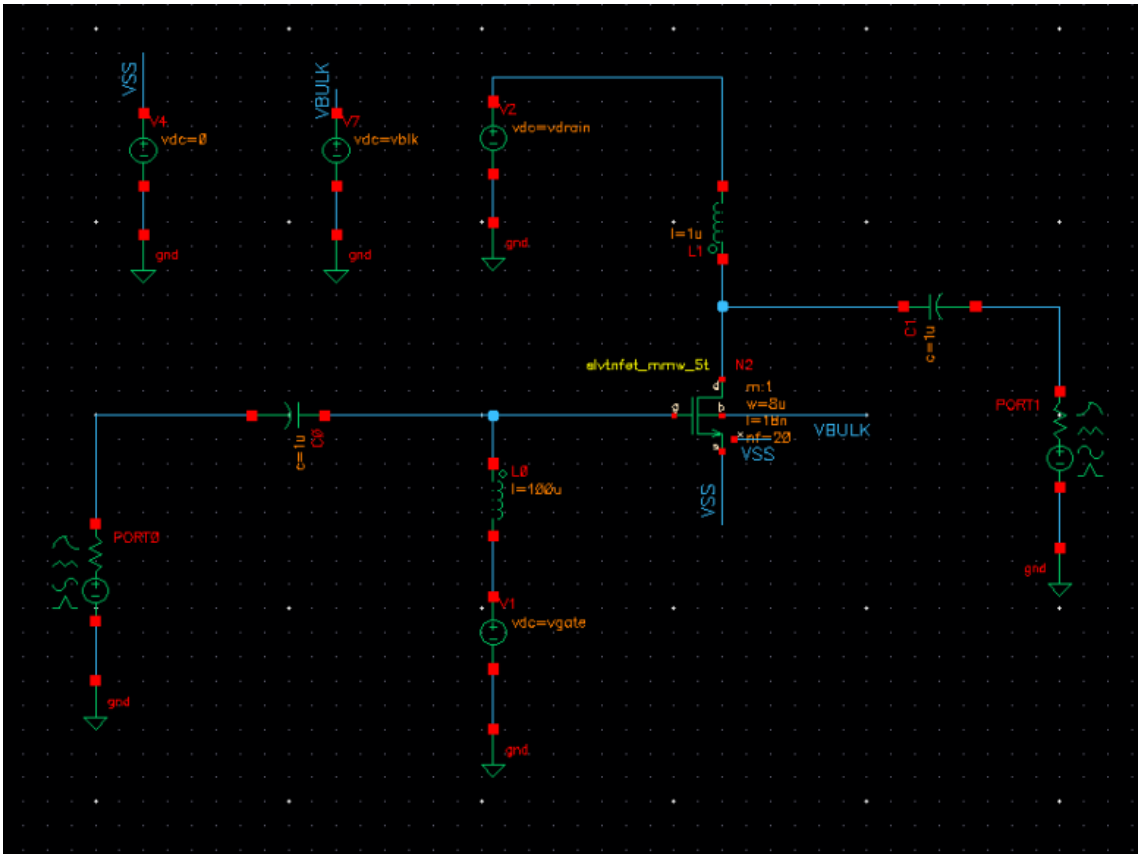


Figure 5.1: Common Source LNA Schematic - the basis for this design work

5.1 Schematic Design Methodology

The design methodology utilized in this study is based on Sorin Voinigescu's strategy for mm-wave LNAs with inductive degeneration, condensed into a sequence of five steps [22]. By adhering to this design methodology, it becomes feasible to achieve optimal noise performance within the given technology (22-FDX). The transistors used in this design are Super Low Vt NFETs with flipped well, meaning they are designed to operate with a very low threshold voltage, specifically for low-power-consuming and high-performance applications. Each step and procedure mentioned in the text refers to specific Virtuoso test benches indicated in the boxes.

5.1.1 Step 1: Biasing for Minimum Noise Figure and Maximum Gain

tb-OptBiasNFminGmax

According to the mentioned methodology, the first step involves setting the bias to the optimum current density (J_{opt}) to minimize the transistor noise figure (NF_{min}). To implement this stage in the design process, the settings for **vbulk** and **vdrain** were configured as outlined in **Table 5.1**. Concerning the vbulk value, substrate biasing with a distinct voltage is allowed by the 22-FDX FD-SOI NMOS technology, facilitating the adjustment of the threshold voltage. In the context of this mm-wave LNA, a lower vbulk value is employed, resulting in a higher threshold voltage and contributing to increased gain—consistent with our objectives. Hence, two values were assigned to vbulk to assess variations and observe the impact on the outcomes.

During this phase, the width of the device is inconsequential, as the primary concern lies in determining the optimal bias point, which is dependent on current density. Consequently, the device is configured with a minimum gate width set at $8um$,18nm length, and 20 fingers.

Bias Input Values	
v_{drain}	$0.8V$
v_{bulk}	0 $0.8V$
$NumOfFingers$	20
$Length$	$18nm$
$Width$	$8um$

Table 5.1: Starting variable values in step 1 of Schematic Design

Continuing with the analysis, an SP simulation was executed (S-Parameter) SP analysis linearizes the circuit about a periodic operating point), revealing in the **NFmin-vgate** graph (**Figure 5.2**) that the bias for attaining the minimum NFmin when $vbulk = 0V$ was $425mV$, and when $vbulk = 0.8V$, it was $365mV$.
The first vertical dashed line from the left represents the bias v_{gate} value estimated by the FoM (Chapter 4.4) found at 359mV and NFmin=0.65dB, showing the ability of the Design Method Based on Inversion Coefficient and EKV Model to predict the best bias value for acheiving the highest trade-off.

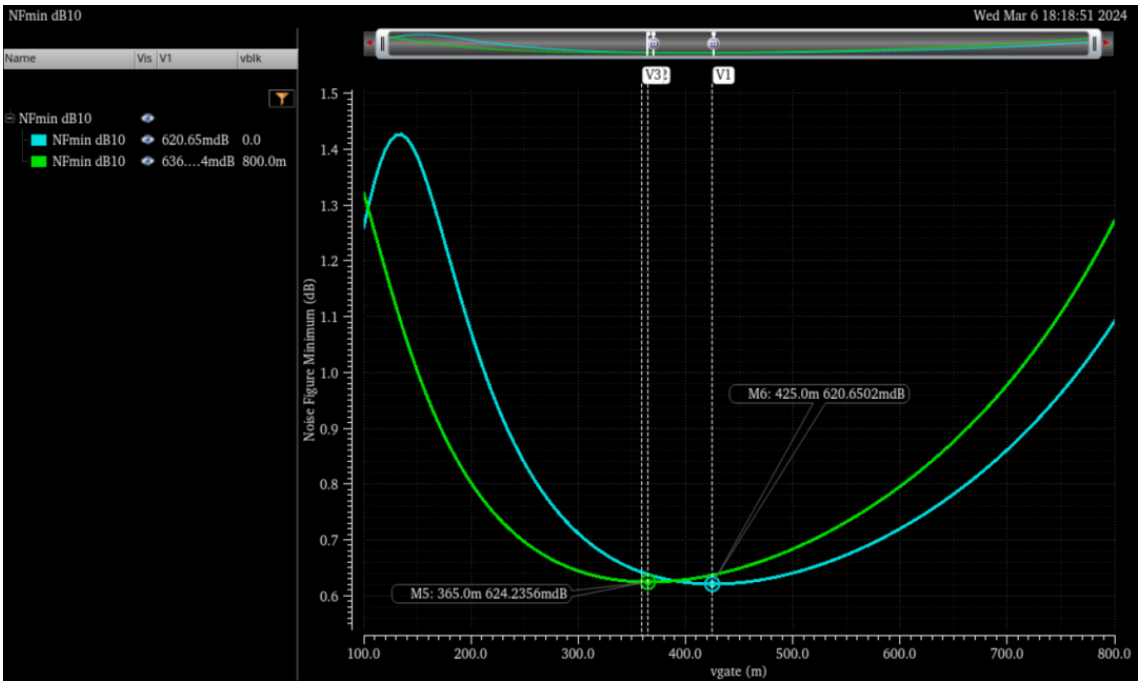


Figure 5.2: Step 1 : NF-vgate graph for determining vgate value for different values of vbulk

In the $Gmax - vgate$ graph **(Figure 5.3)**, the bias for attaining the maximum Gmax when $vbulk = 0V$ was $600mV$, and when $vbulk = 0.8V$, it was $530mV$ (**Table 5.2**).

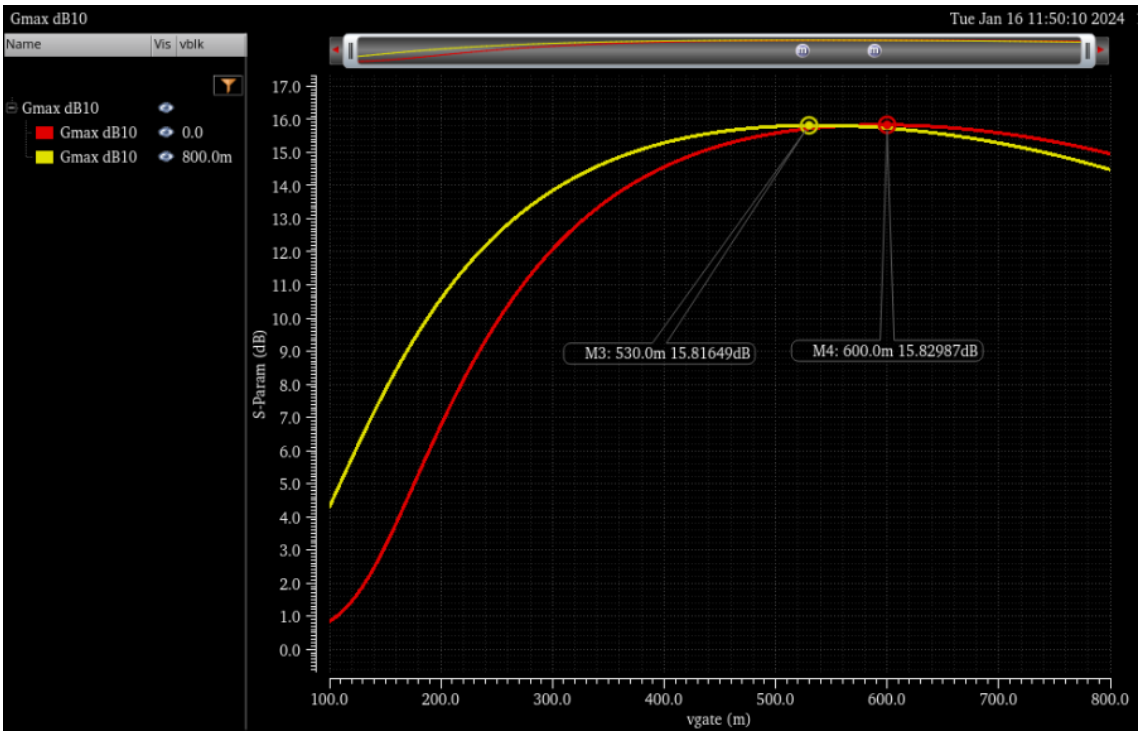


Figure 5.3: Step 1 : Gmax-vgate graph for determining Gmax value for different values of vbulk

The procedure was duplicated for different gate pinch multiplier values, including 1, 2, and 3, yielding results that were nearly indistinguishable. In applications like the one under discussion, increased current flow through the gate is facilitated by a gate pinch multiplier but introduces additional parasitic elements. Therefore, in low-noise amplifiers (LNAs), where the elimination of parasitics is crucial, opting for a value of 1 or, at most, 2 is advisable.

Optimal Bias Results		
v_{bulk}	$0V$	$0.8V$
v_{gate} value for minimum NF_{min}	$425mV$, $NF_{min} = 0.62dB$	$365mV$, $NF_{min} = 0.62dB$
v_{gate} value for maximum G_{max}	$600mV$, $G_{max} = 15.83dB$	$530mV$, $G_{max} = 15.81dB$

Table 5.2: Optimal Bias variable numbers resulted from Step 1

5.1.2 Step 2: Optimal Finger Width

tb-OptFingWidthNFminGmax

Proceeding to the subsequent step, it is imperative to determine the **optimal finger width** W_f to minimize noise figure NFmin. At first the optimal finger number will be calculated. The circuit is biased with a v_{gate} value of $425mV$, corresponding to the minimum noise figure determined in the previous step. To determine W_f, transistor specifications are adjusted by switching the Dimension mode from Finger Width to Total Width and introducing a parameter for the finger number labeled "$numOfFingers$".

Next, a new SP analysis, **Gmax - numOfFingers**, is conducted with v_{bulk} set to 0, varying numOfFingers through a sweep from 1 to 20 fingers, with a step size of 1 fingers. It is noted that within the range of 6-18 fingers, G_{max} exhibits favorable values, whereas beyond 18 fingers, G_{max} starts to slowly decrease. After careful consideration, 16 fingers are opted for as it represents a prudent and safe choice for the model. **Figure 5.4**
The finger width can be easily calculated by:

$$W_f = \frac{TotalGateWidth}{numOfFingers} = \frac{8um}{16} = 500nm$$

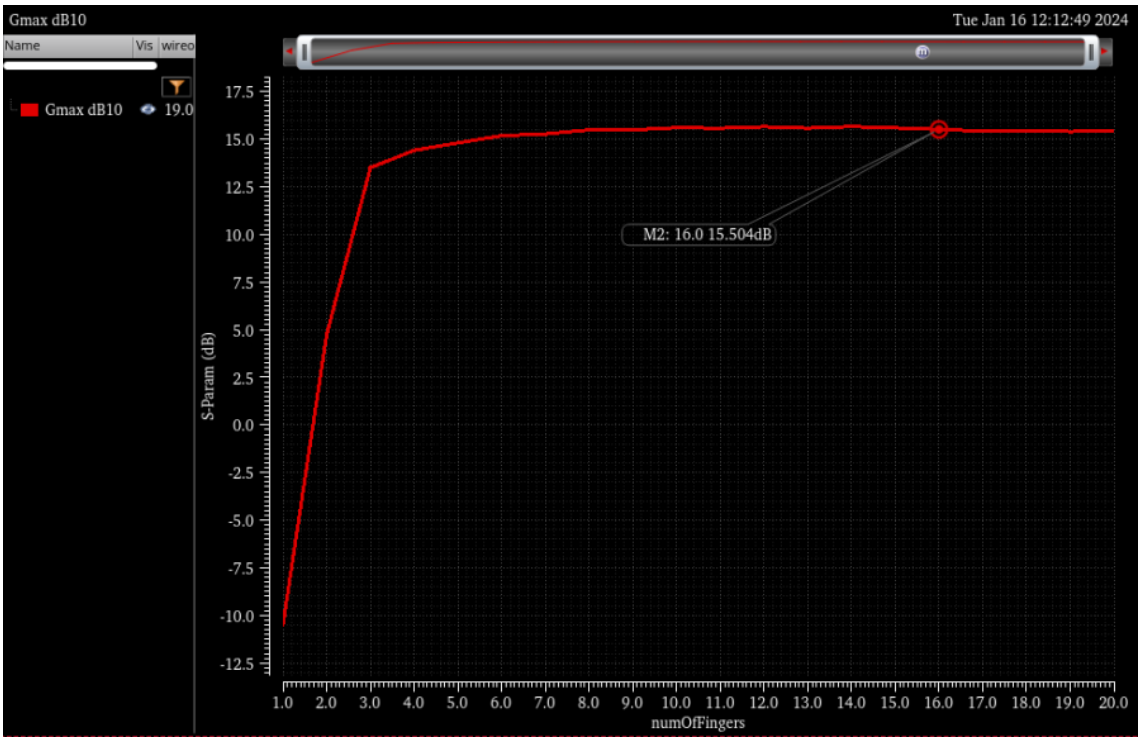


Figure 5.4: Step 2 : Gmax-numOfFingers graph for determining Number Of Fingers

5.1.3 Step 3: Scaling of the Device

Number of multipliers

tb-OptWidthScalingNFminGmax

On the third step of the design, with the device biased at $v_{gate} = 475mV$(step no1) and number of fingers set at 16 (step no2), we proceed to determine the **value of multiplier** which matches the real value of $Z_{opt} = 50\Omega$ at the frequency of operation. The complex optimal impedance Z_{opt} represents the resistance we need the transistor to see at its input to give NF equal to NF_{min}=0.62dB

During the parametric sweep analysis of the **Zopt-Number of Multiplier** graph, the parameter **mmult** is varied across the range of 1 to 20. The graph shows that in order to achieve an impedance of 50Ω, 12 multipliers are necessary.

Figure 5.5

The total transistor width W is calculated using the following formula:

$$W = mmult \cdot TotalGateWidth = 12 \cdot 8um = 96um.$$

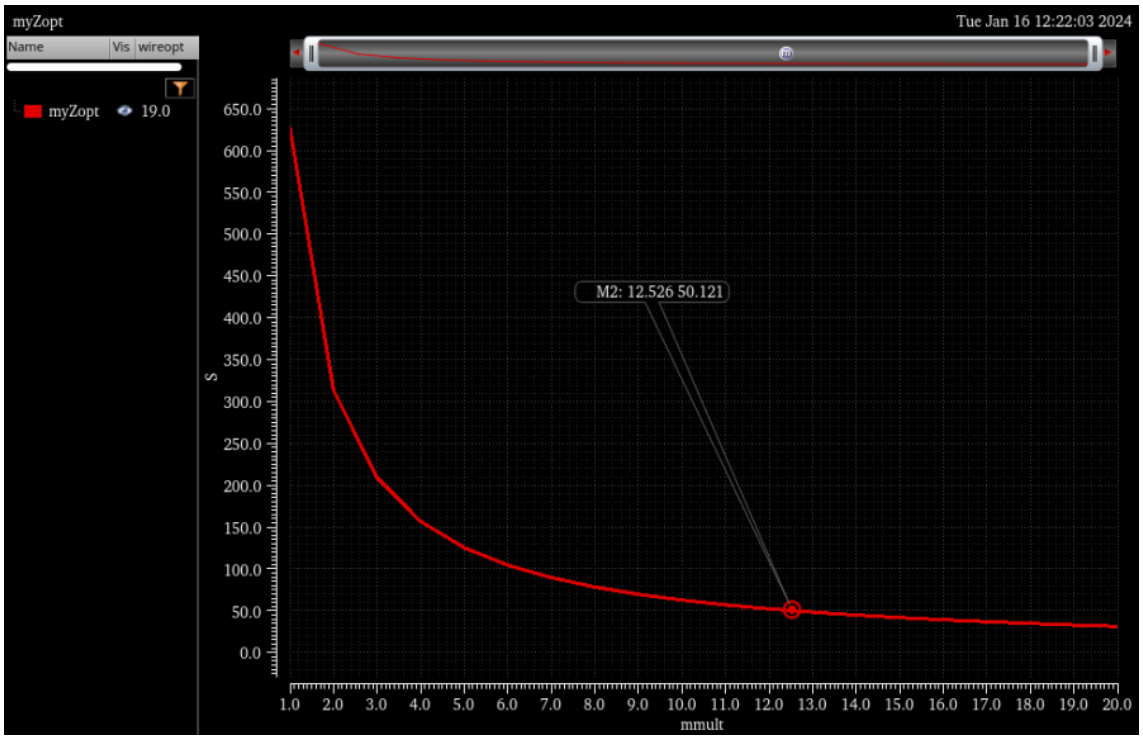


Figure 5.5: Step 3 : Zopt - Number of Multipliers graph for determining Number of Multipliers

Inductive Degeneration

tb-OptDegenZopt

When observing the parameter S_{11} (input return loss) over frequency in a Z-Smith Chart, normalised in 50Ω, it can be observed that the input impedance is unmatched.**Figure 5.6**

In order to match the real part of the input impedance, an inductor is placed in series with the transistor's source, in order to perform inductive degeneration, **Figure 5.7**. Then the Z-Smith Chart is plotted for S11 over the parametric value of the source inductor "ldegen" sweeped from 3pH-100pH and the S11 intercepts the 50Ω is at $l_{degen} = 85pH$

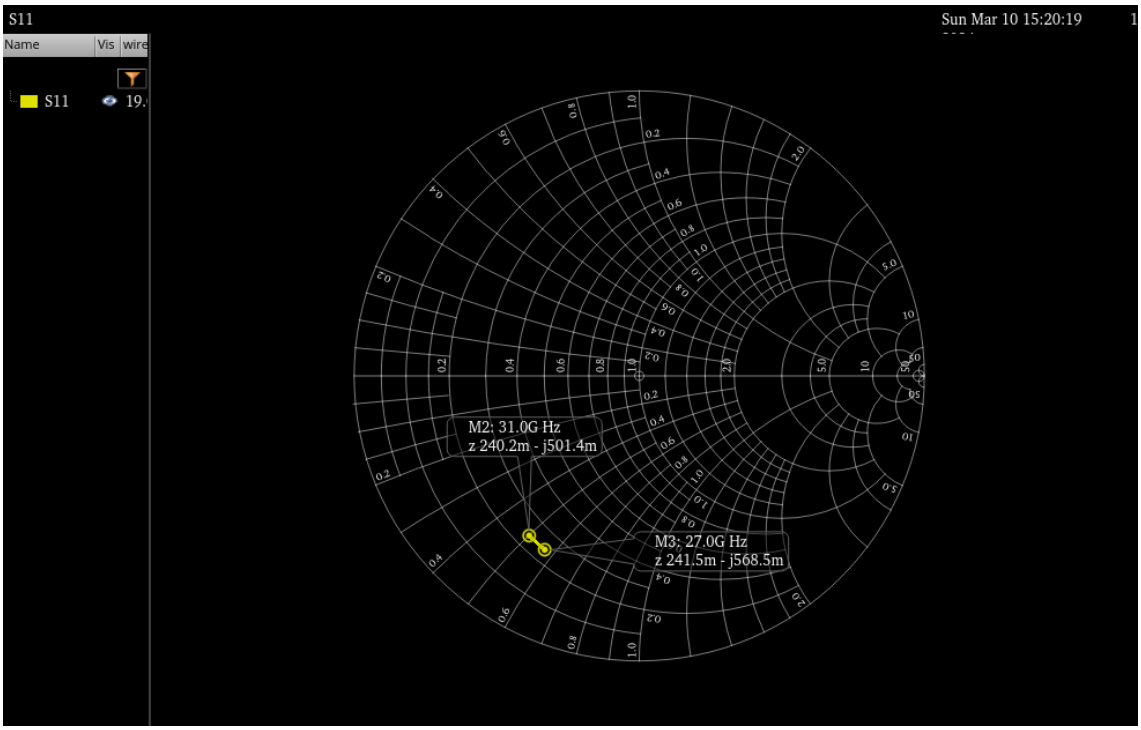


Figure 5.6: Step 3 : Z Smith Chart of S11 over Frequency (27-31GHz) - unmatched input impedance

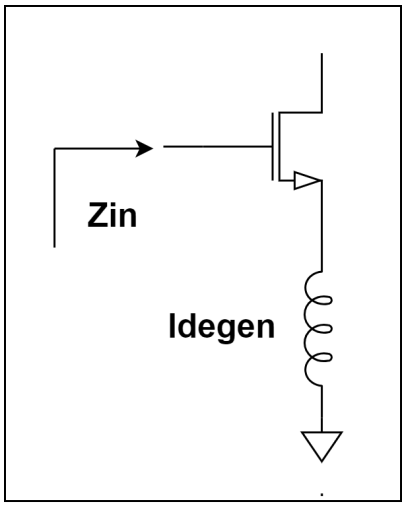


Figure 5.7: Step 3 : Implementation of inductive degeneration method

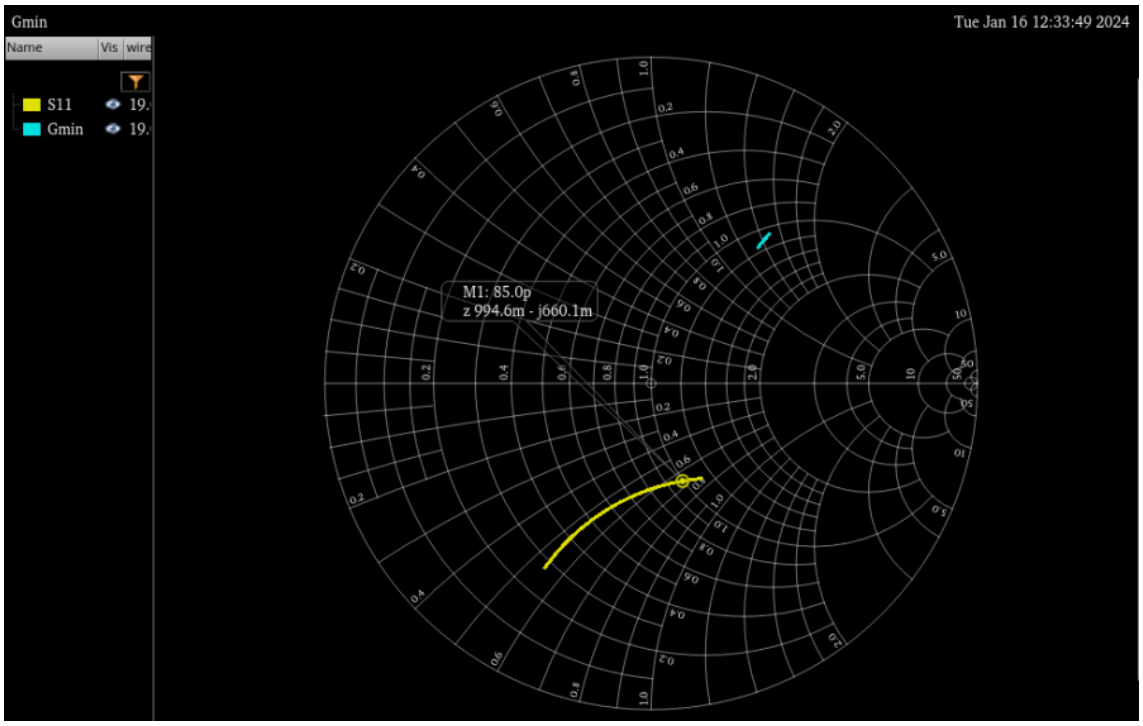


Figure 5.8: Step 3 : Z Smith chart of S11 over "ldegen" values - the value "ldegen" intercepting 50Ω matches the real part of input impedance

5.1.4 Step 4: L series

tb-LSeries

The complex impedance expression contains both the real matched term from the previous step, and the imaginary term. In order to achieve input impedance matching, the imaginary term should be equal to 0. At $28GHz$ the impedance is :

$$Z = 994.9m - j657.1m$$

the minus symbol means that the load has capacitive behavior. Hence, an inductor will be placed in series with the gate of the transistor as shown below:

$$Z = 995m - j657m + jX_L$$

By solving the formula for L_{series}:

$$j657m = X_L$$

$$\text{where: } X_L = 2 \cdot \pi \cdot f \cdot L_{series}$$

$$L = \frac{0.657 \cdot 50}{2 \cdot \pi \cdot 28G} = 186pH$$

It is observed that by raising the value of $lseries$ by additionally $2p$ the $S11$ parameter lands right on the horizontal Z-Smith Axis.

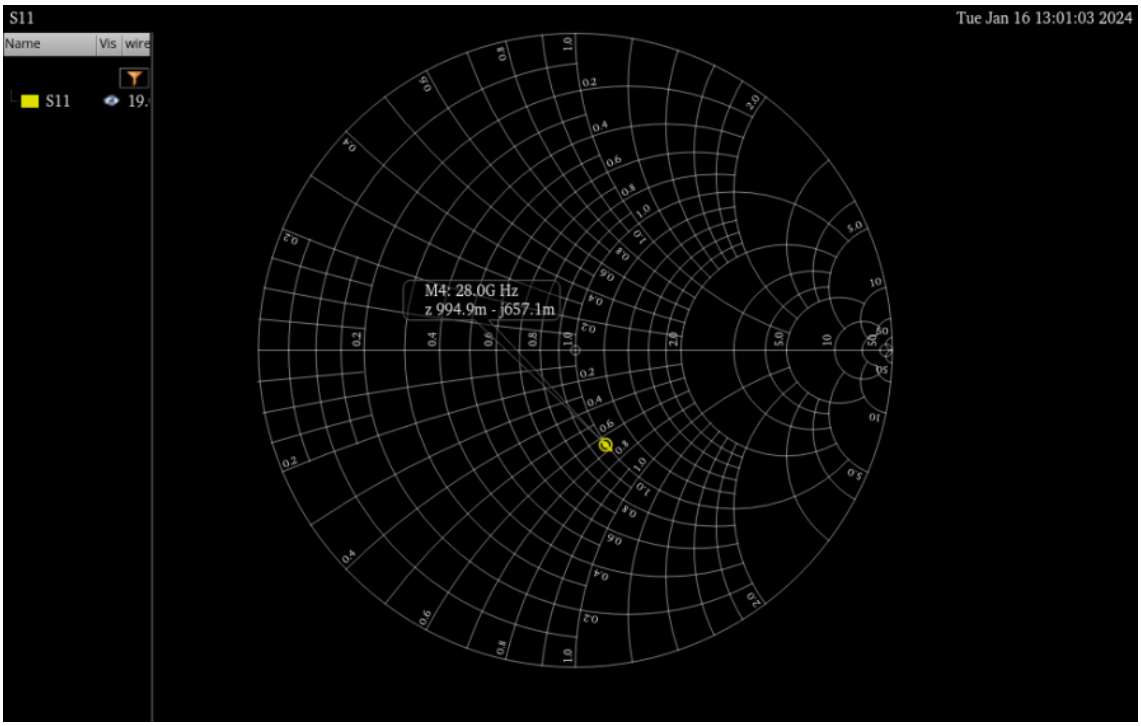


Figure 5.9: Step 4 : Z Smith Chart of S11 over Frequency (27-31GHz) with only the real part of the input impedance matched.

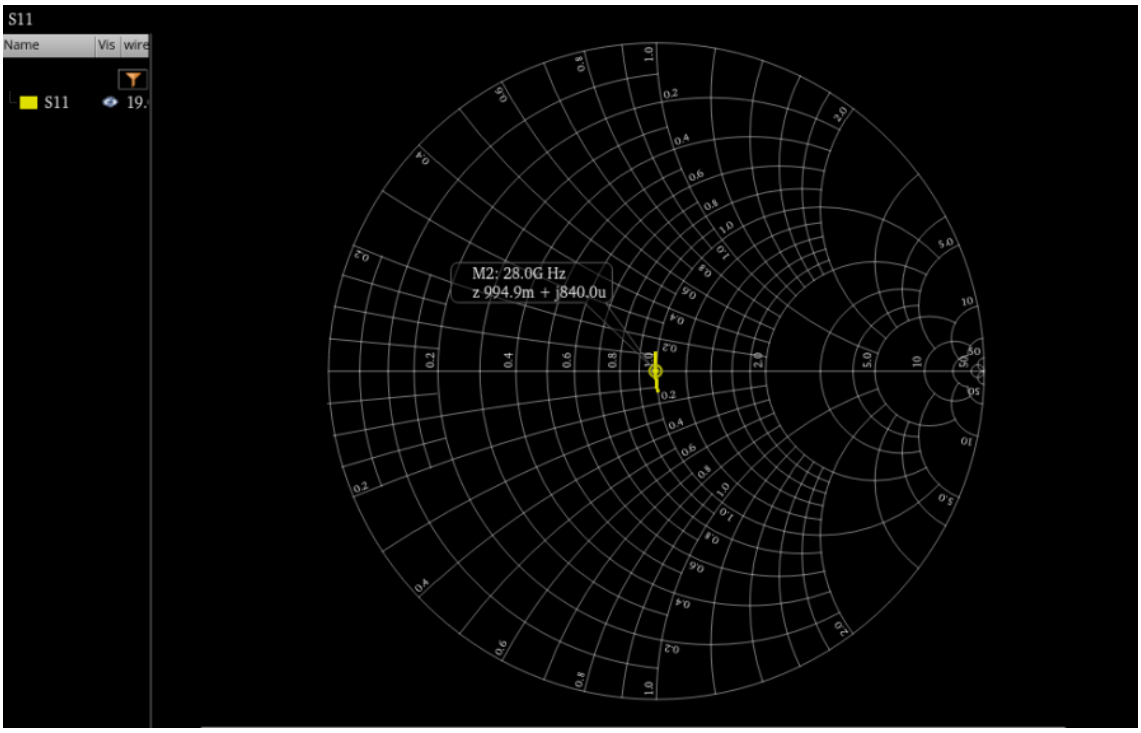


Figure 5.10: Step 4 : Z Smith Chart of S11 vs Frequency after adjusting the Lseries=188pH (matched input impedance)

5.1.5 Step 5: L drain

tb-LDrain

Now by observing the S22 parameter vs Frequency on the Y-Smith Chart normalised at $\frac{1}{50}\Omega$ the complex admittance is also unmatched. Fortunately the real part of the complex admittance is already matched so the only step needed is the elimination of the imaginary term. This time, an inductor is placed at the drain of the transistor and by repeating the same process as the previous step we result in the value of l_{drain} that matches the output admittance. At 28GHz the Y complex value is

$$Y = 960m + j549m$$

$$Y = 960m + j549m + \frac{1 = j}{X_L}$$

$$X_L = 2 \cdot \pi \cdot f \cdot L_{drain}$$

$$\text{and } j549m = \frac{j}{X_L}$$

$$L_{drain} = \frac{1}{2 \cdot \pi \cdot 28GHz \cdot 10.978} \Rightarrow L = 517pH$$

By observing again the S22 vs Frequency Y-Smith Chart, after eliminating the imaginary part, the S22 moved along the curve equal to $\frac{1}{50}\Omega$ and landed right on the horizontal axis.

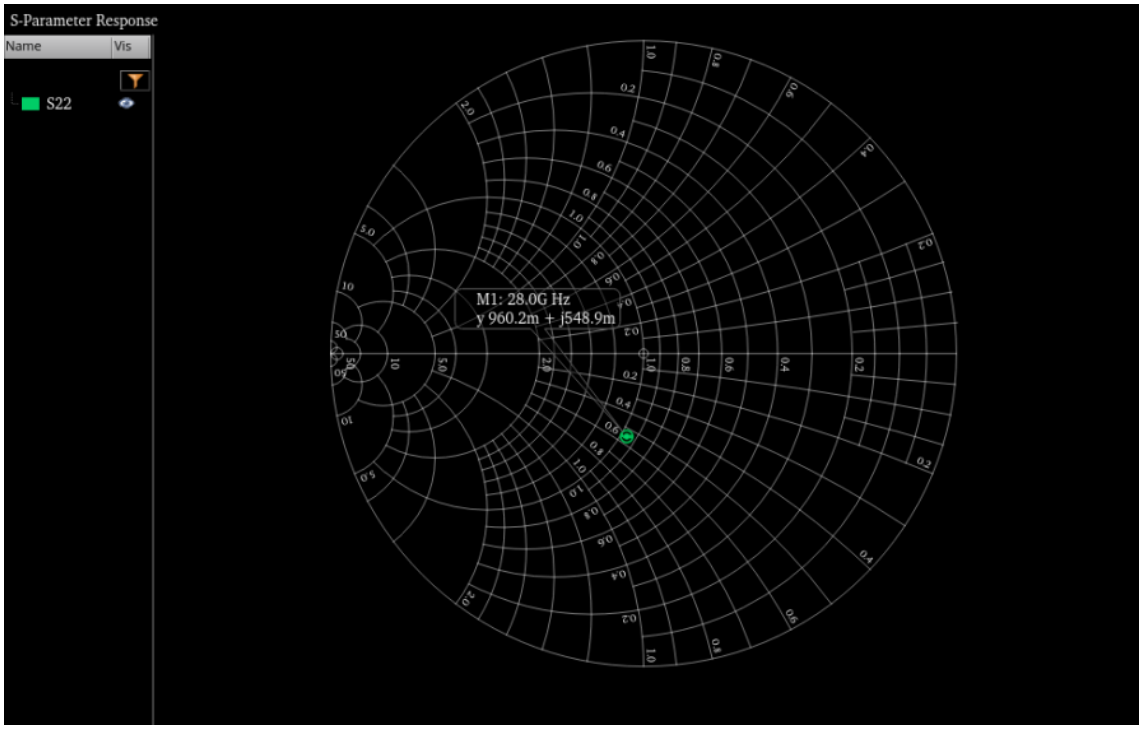


Figure 5.11: Step 5 : Y-Smith Chart of S22 vs Frequency before inserting Ldrain

5.2 Optimization

tb-Optimizer

At this point, an important tool is now introduced in the design: the **Optimizer tool**, essential for fine-tuning parameters, meeting specifications, and ensuring design precision. It's important to emphasize that the earlier steps were crucial for comprehending the inner workings, parameter relationships, and value ranges. The Optimizer tool serves to enhance the design rather than replace the preceding steps.

Parameter Values calculated during previous steps	
v_{gate}	$425mV$
$numOfFingers$	16
$mmult$	12
$ldegen$	$85pH$
$lseries$	$188pH$
$ldrain$	$517pH$

Table 5.3: Parameter values after 5.1 Design Steps

The specified ranges chosen for **NF, gain, input and output return loss** were stricter than the real specifications desired acceptable values to push the Optimizer for better results and provide room for deviation. The **specs** are presented below:

Specifications of LNA		
type	optimiser specs	real specs
NF	< 0.85	< 1.5
$Gain$	> 12	> 11
$InputReturnLoss$	> 12	> 11
$OutputReturnLoss$	> 14	> 14

Table 5.4: LNA Specifications

Initially, the simulation mode is transitioned from **"Single Run, Sweeps, Corners"** to **"Global Optimization"** in the Simulation Options. Subsequently, **Global Variables**, notably **mmult, ldegen, vgate, and lseries**, are incorporated to enable the simulation of design variables across a frequency spectrum ranging from 27 to 31GHz. The values for these variables are fine-tuned within specified ranges, determined by the preceding steps and outlined in the table below.

Global Optimization Ranges	
v_{gate}	$400m : 10m : 500mV$
$mmult$	$6 : 1 : 18$
$ldegen$	$25p : 5p : 100p$
$lseries$	$80p : 10p : 400p$

Table 5.5: Global Optimization Ranges

Optimization was pursued through three distinct configurations: exclusive utilization

of a single L series inductor, sole implementation of a parallel inductor, and a combined deployment of both. Notably, it was observed that the specifications for gain were more effectively met when employing solely the Lseries inductor.
mmult=8, ldegen=55p, lseries=330p,vgate=500m (**Figure 5.13**)

Point	Test	Output	Nominal	Spec
Filter	Filter	Filter	Filter	Filter
Parameters: mmult=8, ldegen=55p, lseries=330p, vgate=500m				
1674	tb_OptimizerLseries	NF @ 27 GHz	845.5m	< 0.85
1674	tb_OptimizerLseries	NF @ 28 GHz	828.1m	< 0.85
1674	tb_OptimizerLseries	NF @ 29 GHz	812.8m	< 0.85
1674	tb_OptimizerLseries	NF @ 30 GHz	799.8m	< 0.85
1674	tb_OptimizerLseries	NF @ 31 GHz	789.5m	< 0.85
1674	tb_OptimizerLseries	Gain @ 27 GHz	12.96	> 11
1674	tb_OptimizerLseries	Gain @ 28 GHz	12.62	> 12
1674	tb_OptimizerLseries	Gain @ 29 GHz	12.28	> 12
1674	tb_OptimizerLseries	Gain @ 30 GHz	11.93	> 12
1674	tb_OptimizerLseries	Gain @ 31 GHz	11.58	> 11
1674	tb_OptimizerLseries	Input Return Lo...	12.02	> 12
1674	tb_OptimizerLseries	Input Return Lo...	12.67	> 12
1674	tb_OptimizerLseries	Input Return Lo...	12.9	> 12
1674	tb_OptimizerLseries	Input Return Lo...	12.74	> 12
1674	tb_OptimizerLseries	Input Return Lo...	12.27	> 12
1674	tb_OptimizerLseries	Output Return L...	16.2	> 14
1674	tb_OptimizerLseries	Output Return L...	16.15	> 14
1674	tb_OptimizerLseries	Output Return L...	15.83	> 14
1674	tb_OptimizerLseries	Output Return L...	15.35	> 14
1674	tb_OptimizerLseries	Output Return L...	14.8	> 14

Figure 5.13: Optimization Results with Lseries inductor

tb-OptimizerLseries tb-OptimizerLpar tb-OptimizerLseriesLpar

5.3 From Ideal Inductors to Real Ones

tb-OptimizerLseriesRealComponents

Continuing to the next step, the design process involves replacing the ideal inductors that were used until now in the schematic, with real inductors. This transition introduces nuances such as resistance, saturation, and parasitic elements. The circuit's behavior will shift due to real-world characteristics, necessitating careful consideration of losses, tolerances, and frequency-dependent effects for accurate and reliable performance. For this reason the optimization will be repeated starting at the Ldrain Inductor, continuing with the Ldegen Inductor at the source and then replacing the Lseries Inductor at the gate.**Figure 5.14**

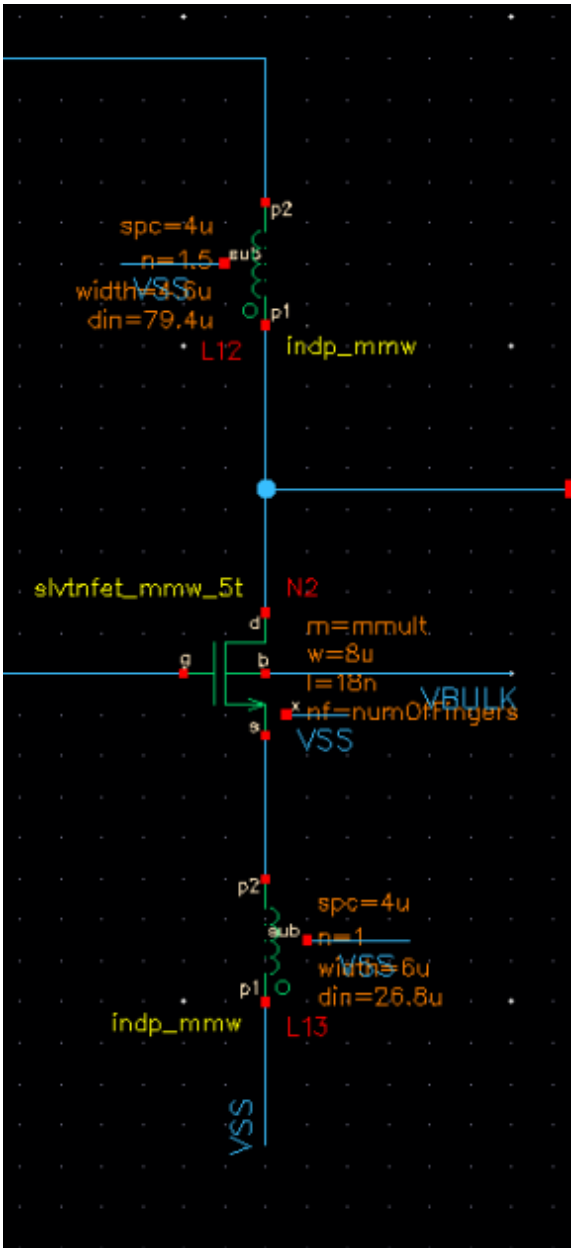


Figure 5.14: Replacement of drain and source inductors with Real Components

In detail, the tb-OptimizerLseries copy was modified by updating our parameters to match the previous Optimizer results. Ldrain was then replaced with a real inductor, maintaining the previously calculated value (419pH). Following a Single Run Sweep Simulation, it was observed that the results did not differ. Subsequently, with the real Ldrain in place, the ideal Ldgen was substituted with a real inductor, and the process was repeated. However, when attempting the same approach for the Lseries inductor, significant discrepancies emerged. The real inductor available in our technology is proved unsuitable for this specific application. As a solution, an alternative method will be employed to address this issue.

5.3.1 Customised Inductor Design

The Lseries inductor specifications did not perfectly align with the real inductor in the FDX technology library. Consequently, an attempt to design a new custom inductor from scratch was made. The process included layout design, testing and import in the original schematic as component to achieve precise specifications.

In order to ensure the accuracy of the inductor, an additional schematic featuring a 2-port network was developed. This schematic was utilized to simulate the electromagnetic behavior of the inductor. The inductor was imported as an s2p parameter file within the 2-port network. In an effort to achieve the final inductance value of 335pH, several design iterations were conducted. A notable challenge during this process was the occurrence of the Self-Resonant Frequency at low frequencies (20GHz), impacting the overall results.

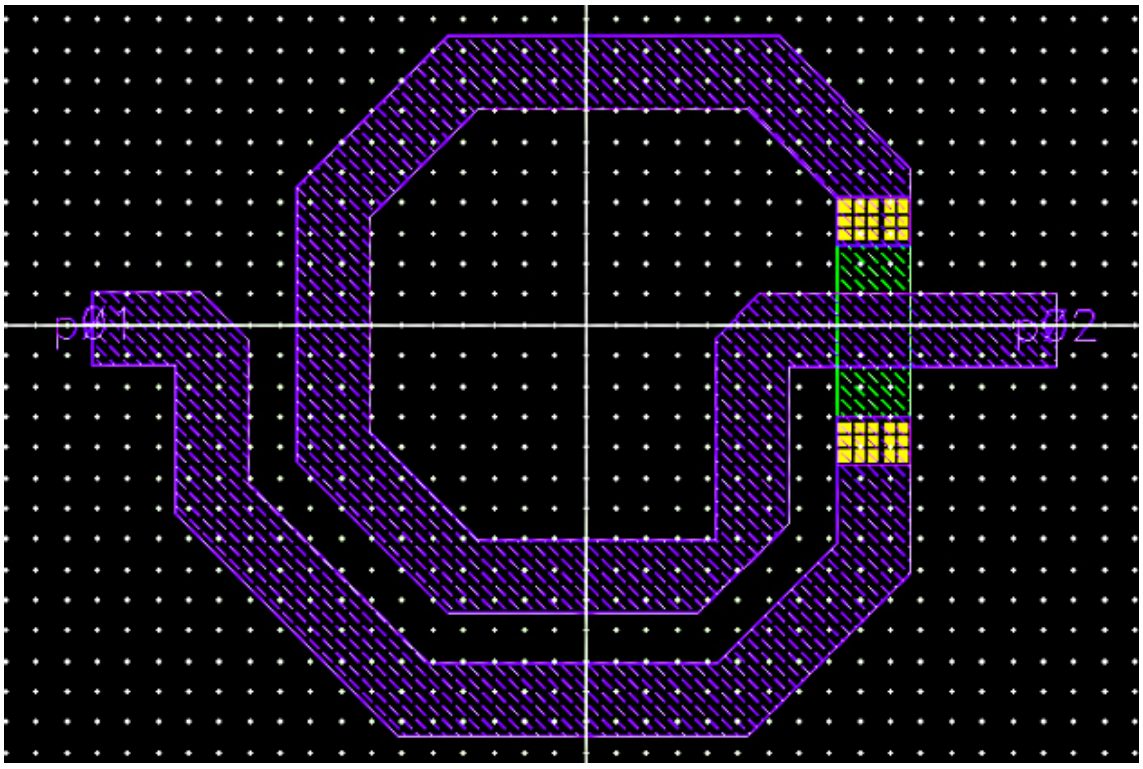


Figure 5.15: Layout Design of one of 7^{th} trial Custom Inductor

To overcome this issue, the layout design of the inductor was systematically reduced in size. This iterative process continued until the **Self-Resonant Frequency** shifted to approximately 35GHz, which was deemed acceptable despite being higher than the target

frequency of 28GHz (see Red Data Curve in Figure). The resulting inductor boasted an inductance of 335pH, and the quality factor exhibited a highly satisfactory value of 118.3. The graph below illustrates the various inductors created and highlights the frequency at which their self-resonant spikes occurred.

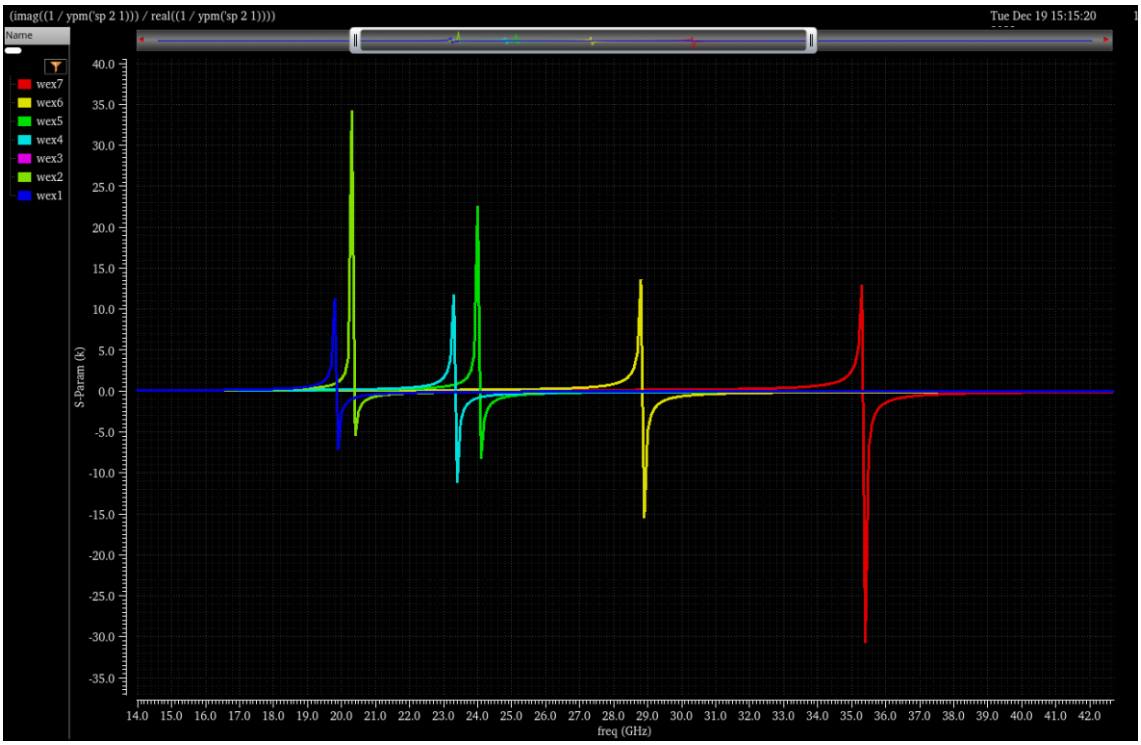


Figure 5.16: Various custom sized inductors showcasing Self-Resonant Frequency spikes

Regrettably, upon implementing the custom inductor in the realComponent Schematic, it was noticed that despite creating a component that appeared satisfactory phenomenally, it failed to yield an improved Noise Figure result compared to the technology's original inductor. Therefore, the design process and optimization continued using the provided real inductor and lead in the following results :

Test	Output	Nominal	Spec	Weight	Pass/Fail
tb_OptimizerLseriesRealComponents	NF @ 27 GHz	1.169	< 0.85		fail
tb_OptimizerLseriesRealComponents	NF @ 28 GHz	1.162	< 0.85		fail
tb_OptimizerLseriesRealComponents	NF @ 29 GHz	1.156	< 0.85		fail
tb_OptimizerLseriesRealComponents	NF @ 30 GHz	1.153	< 0.85		fail
tb_OptimizerLseriesRealComponents	NF @ 31 GHz	1.152	< 0.85		fail
tb_OptimizerLseriesRealComponents	Gain @ 27 GHz	11.49	> 11		pass
tb_OptimizerLseriesRealComponents	Gain @ 28 GHz	11.18	> 12		near
tb_OptimizerLseriesRealComponents	Gain @ 29 GHz	10.86	> 12		near
tb_OptimizerLseriesRealComponents	Gain @ 30 GHz	10.54	> 12		fail
tb_OptimizerLseriesRealComponents	Gain @ 31 GHz	10.22	> 11		near
tb_OptimizerLseriesRealComponents	Input Return Loss @ 27 GHz	11.37	> 12		near
tb_OptimizerLseriesRealComponents	Input Return Loss @ 28 GHz	11.83	> 12		near
tb_OptimizerLseriesRealComponents	Input Return Loss @ 29 GHz	12.07	> 12		pass
tb_OptimizerLseriesRealComponents	Input Return Loss @ 30 GHz	12.08	> 12		pass
tb_OptimizerLseriesRealComponents	Input Return Loss @ 31 GHz	11.9	> 12		near
tb_OptimizerLseriesRealComponents	Output Return Loss @ 27GHz	20.3	> 14		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 28GHz	19.41	> 14		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 29GHz	18.39	> 14		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 30GHz	17.39	> 14		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 31GHz	16.49	> 14		pass

Test	Output	Nominal	Spec	Weight	Pass/Fail
tb_OptimizerLseriesRealComponents	NF @ 27 GHz	1.169	< 1.3		pass
tb_OptimizerLseriesRealComponents	NF @ 28 GHz	1.162	< 1.3		pass
tb_OptimizerLseriesRealComponents	NF @ 29 GHz	1.156	< 1.3		pass
tb_OptimizerLseriesRealComponents	NF @ 30 GHz	1.153	< 1.3		pass
tb_OptimizerLseriesRealComponents	NF @ 31 GHz	1.152	< 1.3		pass
tb_OptimizerLseriesRealComponents	Gain @ 27 GHz	11.49	> 11		pass
tb_OptimizerLseriesRealComponents	Gain @ 28 GHz	11.18	> 11		pass
tb_OptimizerLseriesRealComponents	Gain @ 29 GHz	10.86	> 11		near
tb_OptimizerLseriesRealComponents	Gain @ 30 GHz	10.54	> 11		near
tb_OptimizerLseriesRealComponents	Gain @ 31 GHz	10.22	> 11		near
tb_OptimizerLseriesRealComponents	Input Return Loss @ 27 GHz	11.37	> 11		pass
tb_OptimizerLseriesRealComponents	Input Return Loss @ 28 GHz	11.83	> 11		pass
tb_OptimizerLseriesRealComponents	Input Return Loss @ 29 GHz	12.07	> 11		pass
tb_OptimizerLseriesRealComponents	Input Return Loss @ 30 GHz	12.08	> 11		pass
tb_OptimizerLseriesRealComponents	Input Return Loss @ 31 GHz	11.9	> 11		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 27GHz	20.3	> 14		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 28GHz	19.41	> 14		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 29GHz	18.39	> 14		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 30GHz	17.39	> 14		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 31GHz	16.49	> 14		pass

Figure 5.17: Simulation results with stricter specs (top) and real specs (bottom)

Parameter Values after Replacing Ideal Inductors with Real	
v_{gate}	470mV
number of multipliers	9
gate (series) inductor	170pH
source (degeneration) inductor	90pH

Table 5.6: Parameter Values after Replacing Ideal Inductors with Real

5.4 Real Bias

5.4.1 Current Mirror

At this point it is important to emphasize the concept of current mirrors, an essential building block in analog integrated circuit design.

Suppose a simple circuit in saturation, operated by a battery with drain current:

$$I_D = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_b - V_{th})^2$$

It can be observed that μ_n and V_{th} are both temperature dependent so consequently if the temperature changes, the I_D does not remain constant. Moreover, another problem of supply dependency occurs when in a battery operating device V_{DD} will start decreasing as the battery gradually drains, affecting I_D.

$$I_D = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (\frac{R_2}{R_1 + R_2} V_{DD} - V_{th})^2$$

In order to overcome such problems in the design, ensuring a constant current flow, a current mirror is used to replicate or mirror a reference current onto one or multiple branches. The key principle is to enforce the same current in the mirror transistors as flows through the reference transistor. This replication is achieved by connecting the gate of the mirror transistors to the gate of the reference transistor. As described in [23] current mirrors are indispensable for creating reliable, temperature-independent biasing solutions critical in the development of high-performance analog circuits.

5.4.2 Implementation of Current Mirror as Bias

In this step, the circuit is biased using a current mirror to create a "golden" temperature and supply-independent current source as mentioned previously. A clone transistor is added as a mirror to the existing one, and the original voltage source (v_{dc}) is replaced with a current source (i_{dc}).

Initially, before adding the current mirror, the current was calculated at $18.33mA$ with a gate voltage (v_{gate}) of $470mV$. The current in the current mirror's reference transistor is manually adjusted to $16.01mA$ to achieve the desired v_{gate} value. Subsequently, for efficient utilization of the current mirror's capabilities and to reduce the supply current, the formula

$$I_{OUT} = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \cdot I_{REF}$$

is applied. Here, the dc current I_{REF} is scaled down by a factor of 9 compared to the output current I_{OUT}, with the length $L1 = L2$ and width $W2 = 9 \cdot W1$, where W1,L1 correspond to the N5 transistor and W2,L2 correspond to the N2 transistor.

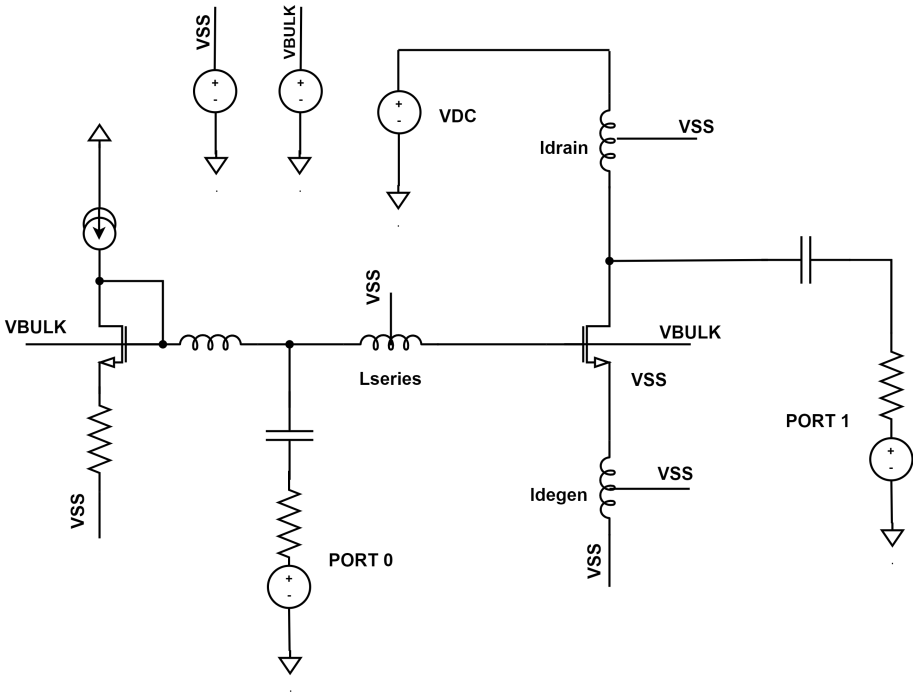


Figure 5.18: Real Bias Schematic after implementing the current mirror

Finally, in order to confirm the LNAs independence from temperature a DC analysis for a range of temperatures: -40°, 27°, 80°and 125°Celsius is performed.

The LNA is temperature independent with a small exception of NF which at lower temperatures demonstrates superior results but experiences degradation at higher temperatures, particularly at 125°Celsius. Gain reduction and increased noise figure are observed as temperature rises, with the transconductance identified as a key factor influencing these characteristics. The specification degradation of the LNA is not only related to temperature, but also to humidity, high- and low-temperature shock, and time. This insight suggests a potential avenue for enhancing LNA performance across a range of operating temperatures.

Parameter							temp_-40	temp_27	temp_80	temp_125
temperature							-40	27	80	125

25 rows

Test	Output	Spec	Weight	Pass/Fail	Min	Max	temp_-40	temp_27	temp_80	temp_125
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
tb_RealBias	NF @ 27 GHz	< 1.3		fail	640m	1.53	640m	964.5m	1.257	1.53
tb_RealBias	NF @ 28 GHz	< 1.3		fail	632.5m	1.515	632.5m	954.1m	1.245	1.515
tb_RealBias	NF @ 29 GHz	< 1.3		fail	626.5m	1.503	626.5m	945.8m	1.234	1.503
tb_RealBias	NF @ 30 GHz	< 1.3		fail	622.4m	1.495	622.4m	939.8m	1.227	1.495
tb_RealBias	NF @ 31 GHz	< 1.3		fail	620.2m	1.49	620.2m	936.5m	1.223	1.49
tb_RealBias	Gain @ 27 GHz	> 11		pass	11.43	12.09	12.09	11.85	11.63	11.43
tb_RealBias	Gain @ 28 GHz	> 11		pass	11.1	11.75	11.75	11.51	11.3	11.1
tb_RealBias	Gain @ 29 GHz	> 11		near	10.76	11.41	11.41	11.17	10.96	10.76
tb_RealBias	Gain @ 30 GHz	> 11		near	10.42	11.07	11.07	10.83	10.62	10.42
tb_RealBias	Gain @ 31 GHz	> 11		near	10.08	10.72	10.72	10.49	10.27	10.08
tb_RealBias	Input Return Loss @ 27 GHz	> 11		pass	13.85	14.51	13.85	14.24	14.42	14.51
tb_RealBias	Input Return Loss @ 28 GHz	> 11		pass	14.46	15.47	14.46	14.99	15.28	15.47
tb_RealBias	Input Return Loss @ 29 GHz	> 11		pass	14.53	15.82	14.53	15.15	15.54	15.82
tb_RealBias	Input Return Loss @ 30 GHz	> 11		pass	14.12	15.5	14.12	14.75	15.17	15.5
tb_RealBias	Input Return Loss @ 31 GHz	> 11		pass	13.4	14.7	13.4	13.98	14.38	14.7
tb_RealBias	Output Return Loss @ 27GHz	> 14		pass	15.06	16.94	16.94	16.22	15.59	15.06
tb_RealBias	Output Return Loss @ 28GHz	> 14		pass	14.6	15.87	15.87	15.41	14.97	14.6
tb_RealBias	Output Return Loss @ 29GHz	> 14		pass	14.07	14.88	14.88	14.61	14.33	14.07
tb_RealBias	Output Return Loss @ 30GHz	> 14		near	13.55	13.99	13.99	13.86	13.7	13.55
tb_RealBias	Output Return Loss @ 31GHz	> 14		near	13.04	13.22	13.22	13.18	13.11	13.04

Figure 5.19: Temperature vs Design Parameters

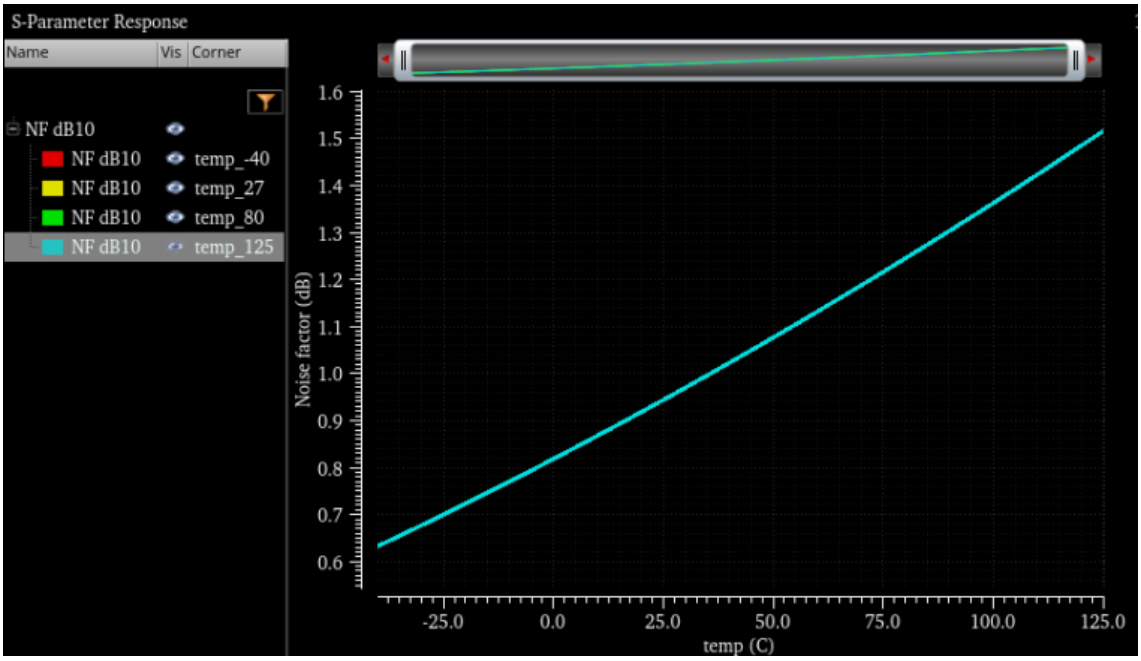


Figure 5.20: Noise Figure vs. Temperature

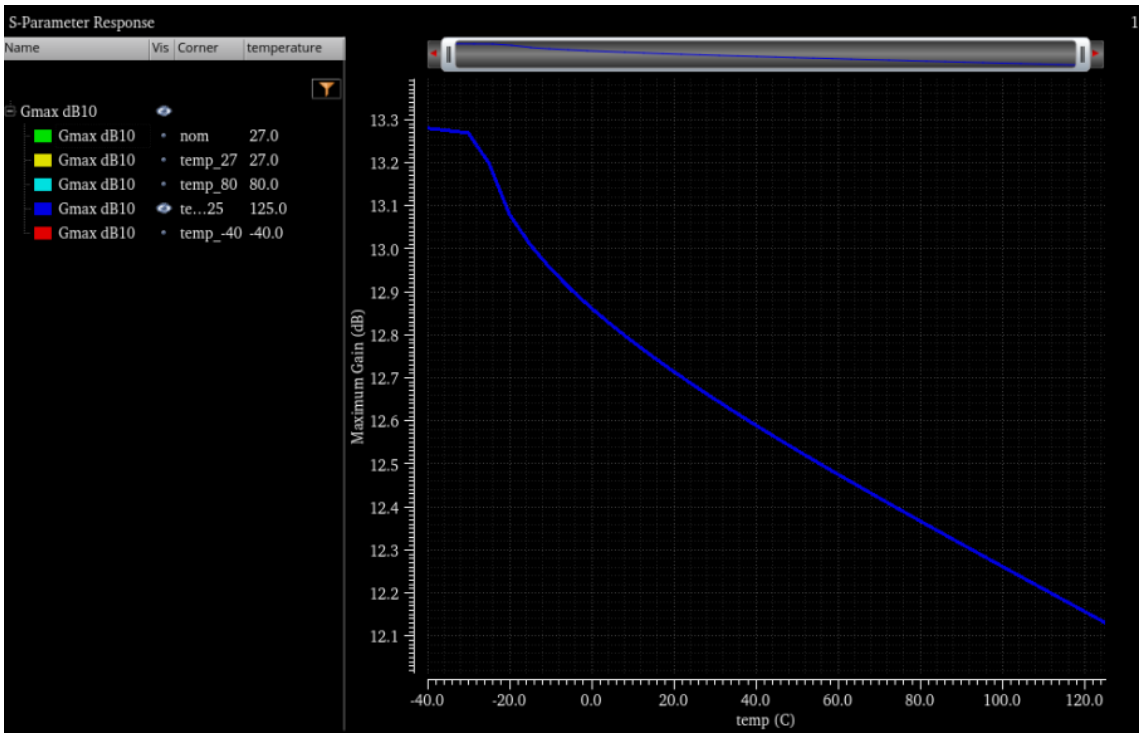


Figure 5.21: Gain vs. Temperature

5.5 Layout Design

At this point, the schematic design of the LNA is completed and now it is time to proceed to the layout design or as known as mask/IC design. In detail, the layout design creates a bridge between the schematic representation of the circuit and the physical realization with basic principles of manufacturability, performance, density, size.

5.5.1 Design

In the layout suite, the passive components of the LNA were designed in order to simulate their electromagnetic behavior **Figure 5.22**. Specifically, the components designed were the load (output) inductor at the drain of the transistor, the degeneration inductor, the series inductor (input) and finally 3 input pads.

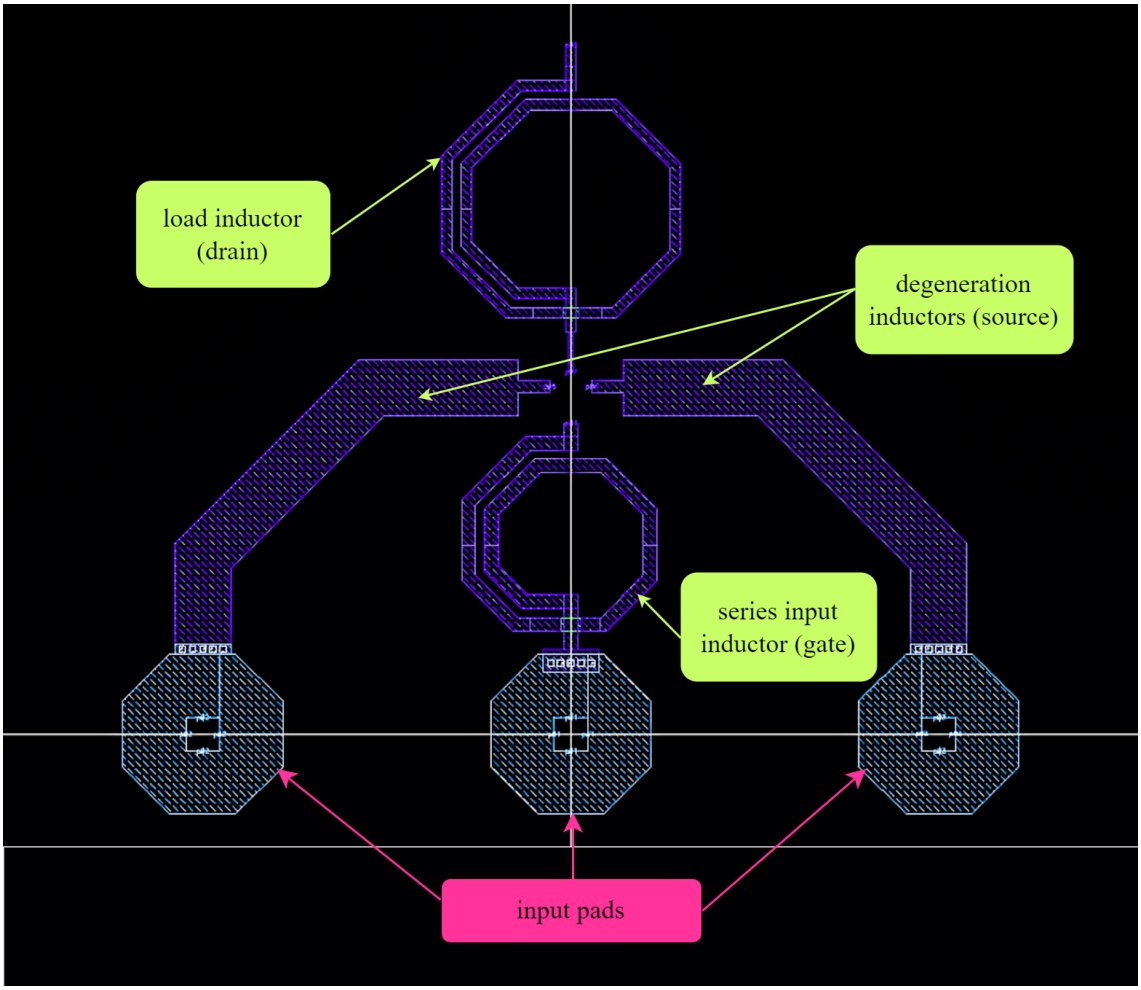


Figure 5.22: Layout of Inductors

The pads are a long distance away from the source of the transistor. For this reason a clever technique was used, instead of designing a whole inductor of 60pH, the inductors were structured at 120pH and mirrored over the horizontal axis in parallel so they would provide the same amount of inductance. In order to achieve a structure with this value of inductance, there were many trials varying in size to achieve the optimal inductor.**Figure 5.23**

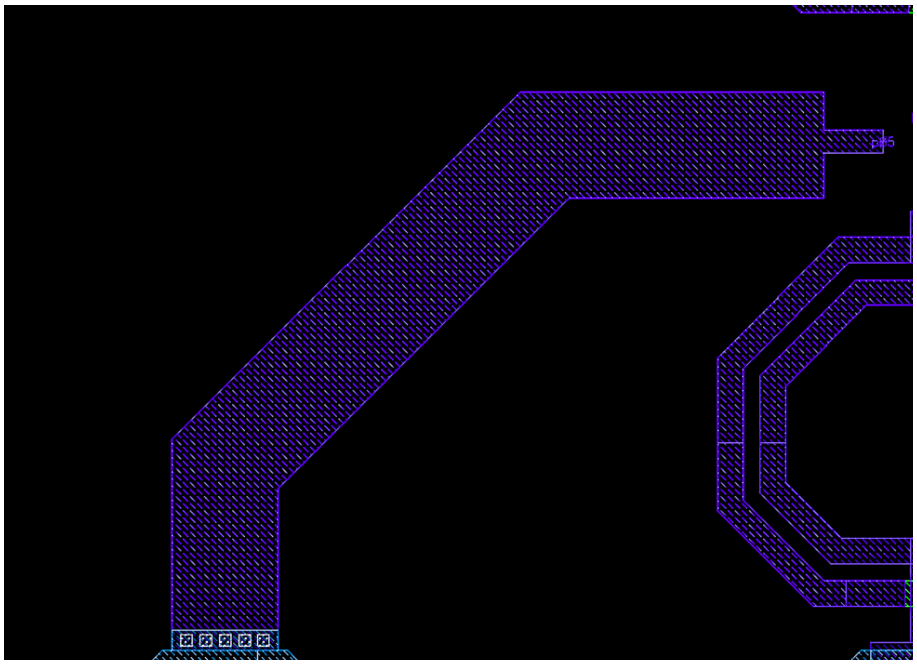


Figure 5.23: Degeneration Inductor in Layout

In the ends of each structure there have been assigned labels that stand for the port number, so after extracting the layout an 8-port will be created and added to the schematic.

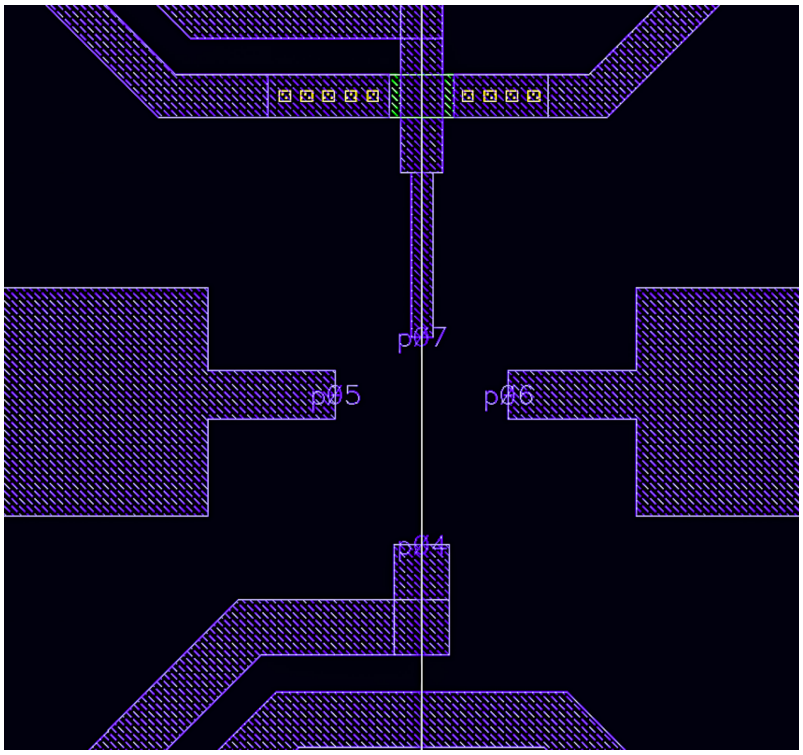
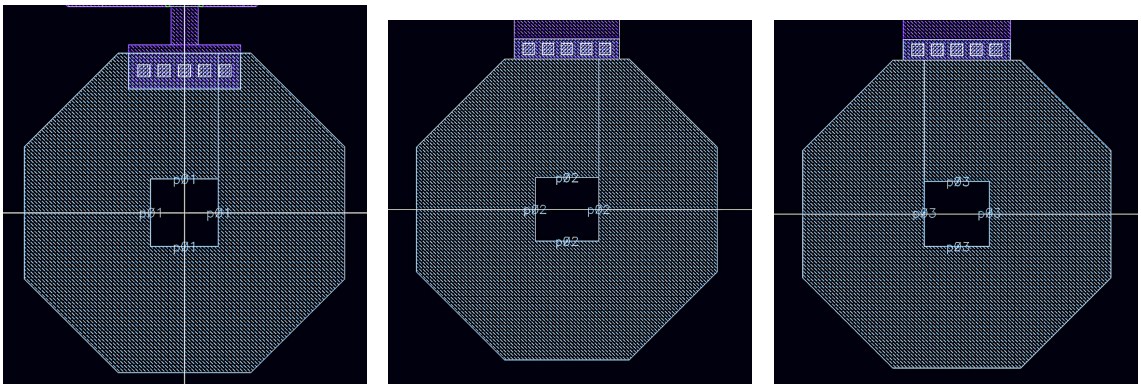


Figure 5.24: Inductor ports to be connected with the transistor



(a) input p01 (b) VSS p02 (c) VSS p02

Figure 5.25: The three Input Pads

5.5.2 Extraction and Simulation

Subsequently, after returning to the schematic and inserting the extracted 8-port, labels are inserted on every pin to assign the connections. At this point the inductors are removed and replaced with labels that map their way into the port. As shown in **Figure 5.26** and **Table 5.6** the connections between the LNA and the port are clearly visible.

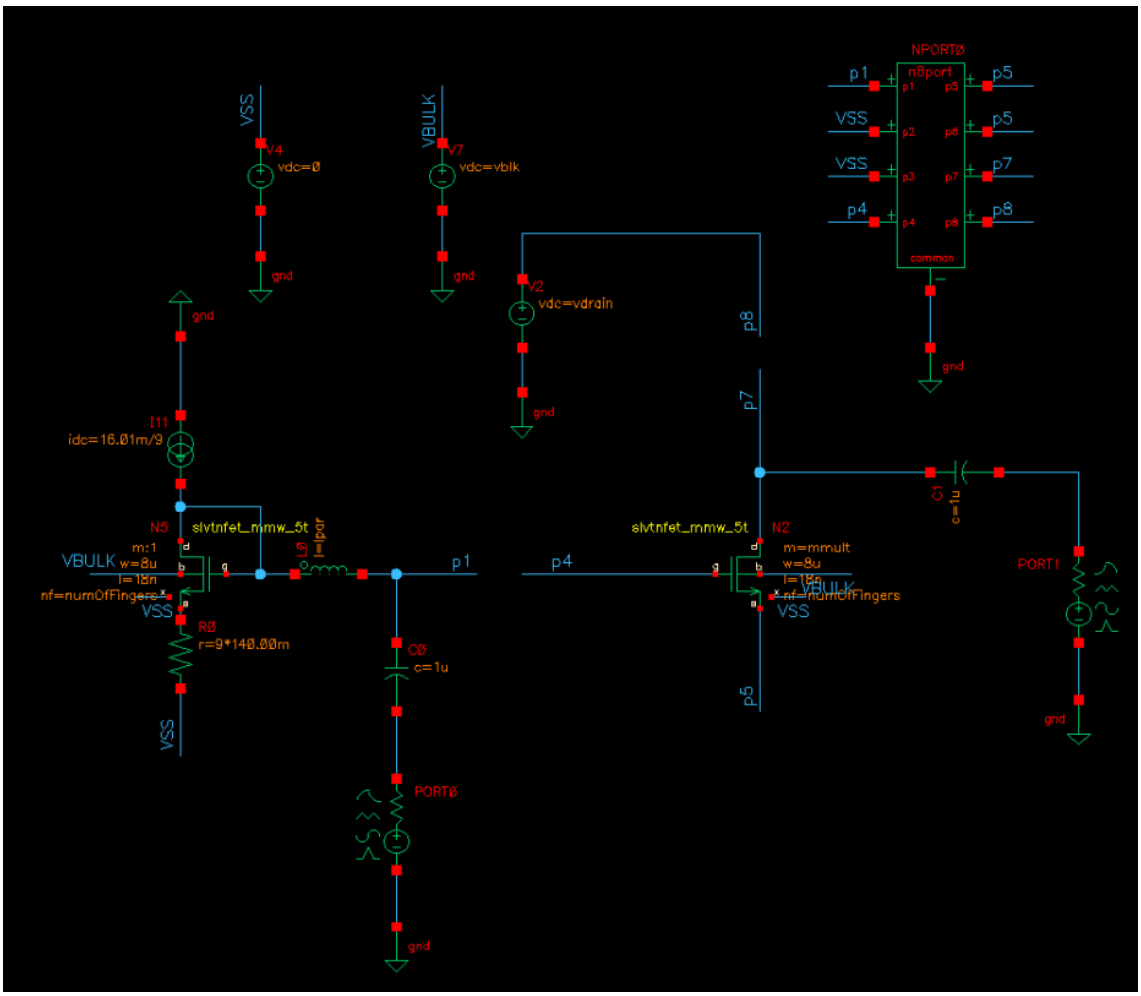


Figure 5.26: Schematic after Layout Extraction

Port assignment map	
p_{01}	left side of series input inductor
p_{02}	VSS
p_{03}	VSS
p_{04}	gate of series input inductor
p_{05}	source of degeneration inductor
p_{06}	source of degeneration inductor
p_{07}	drain of load inductor
p_{08}	output of load inductor

Table 5.7: Port placement in schematic design

5.5.3 Comparison of the Schematic with Layout Result

After running the simulation it can be noticed that the performance of the LNA did not deteriorate significantly.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
tb_8port	NF @ 27 GHz	1.883	< 1.3		fail
tb_8port	NF @ 28 GHz	1.883	< 1.3		fail
tb_8port	NF @ 29 GHz	1.883	< 1.3		fail
tb_8port	NF @ 30 GHz	1.883	< 1.3		fail
tb_8port	NF @ 31 GHz	1.883	< 1.3		fail
tb_8port	Gain @ 27 GHz	10.62	> 11		near
tb_8port	Gain @ 28 GHz	10.62	> 11		near
tb_8port	Gain @ 29 GHz	10.62	> 11		near
tb_8port	Gain @ 30 GHz	10.62	> 11		near
tb_8port	Gain @ 31 GHz	10.62	> 11		near
tb_8port	Input Return Lo...	11.31	> 11		pass
tb_8port	Input Return Lo...	11.31	> 11		pass
tb_8port	Input Return Lo...	11.31	> 11		pass
tb_8port	Input Return Lo...	11.31	> 11		pass
tb_8port	Input Return Lo...	11.31	> 11		pass
tb_8port	Output Return L...	17.83	> 14		pass
tb_8port	Output Return L...	17.83	> 14		pass
tb_8port	Output Return L...	17.83	> 14		pass
tb_8port	Output Return L...	17.83	> 14		pass
tb_8port	Output Return L...	17.83	> 14		pass

Figure 5.27: Post Layout Simulation Results

Test	Output	Nominal	Spec	Weight	Pass/Fail
tb_OptimizerLseriesRealComponents	NF @ 27 GHz	1.169	< 1.3		pass
tb_OptimizerLseriesRealComponents	NF @ 28 GHz	1.162	< 1.3		pass
tb_OptimizerLseriesRealComponents	NF @ 29 GHz	1.156	< 1.3		pass
tb_OptimizerLseriesRealComponents	NF @ 30 GHz	1.153	< 1.3		pass
tb_OptimizerLseriesRealComponents	NF @ 31 GHz	1.152	< 1.3		pass
tb_OptimizerLseriesRealComponents	Gain @ 27 GHz	11.49	> 11		pass
tb_OptimizerLseriesRealComponents	Gain @ 28 GHz	11.18	> 11		pass
tb_OptimizerLseriesRealComponents	Gain @ 29 GHz	10.86	> 11		near
tb_OptimizerLseriesRealComponents	Gain @ 30 GHz	10.54	> 11		near
tb_OptimizerLseriesRealComponents	Gain @ 31 GHz	10.22	> 11		near
tb_OptimizerLseriesRealComponents	Input Return Loss @ 27 GHz	11.37	> 11		pass
tb_OptimizerLseriesRealComponents	Input Return Loss @ 28 GHz	11.83	> 11		pass
tb_OptimizerLseriesRealComponents	Input Return Loss @ 29 GHz	12.07	> 11		pass
tb_OptimizerLseriesRealComponents	Input Return Loss @ 30 GHz	12.08	> 11		pass
tb_OptimizerLseriesRealComponents	Input Return Loss @ 31 GHz	11.9	> 11		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 27GHz	20.3	> 14		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 28GHz	19.41	> 14		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 29GHz	18.39	> 14		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 30GHz	17.39	> 14		pass
tb_OptimizerLseriesRealComponents	Output Return Loss @ 31GHz	16.49	> 14		pass

Figure 5.28: Pre Layout Simulation Results

5.5.4 Linearity Calculation

tb-linear

In Chapter 3, the Linearity was highlighted as a crucial design parameter, focusing on enhancing the power level of an input signal while maintaining the signal's original content unchanged. In this simulation, a Harmonic Balance (HB) analysis will be performed, which enables the examination of circuit behavior at high frequencies, where nonlinear effects play a substantial role.

The examination of the Power Gain - Input Power Curve depicted in **Figure 5.29** illustrates a sharp decrease in Power Gain when the Input Power increases. The input-referred 1dB compression point (P_{1db}) was determined to be at -3.604 dBm, indicating the Input Power level where the Gain is 1dB lower than its maximum value.

Figure 5.30 depicts the first harmonic for a 28 GHz frequency over time, for three different values of P_{1dB}. It is noticeable that as the value of P_{1dB} increases, the sinusoidal shape of the harmonic begins to clip and transitions towards a square wave, particularly when P_{1dB} reaches the input-referred compression point at -3.6dBm .

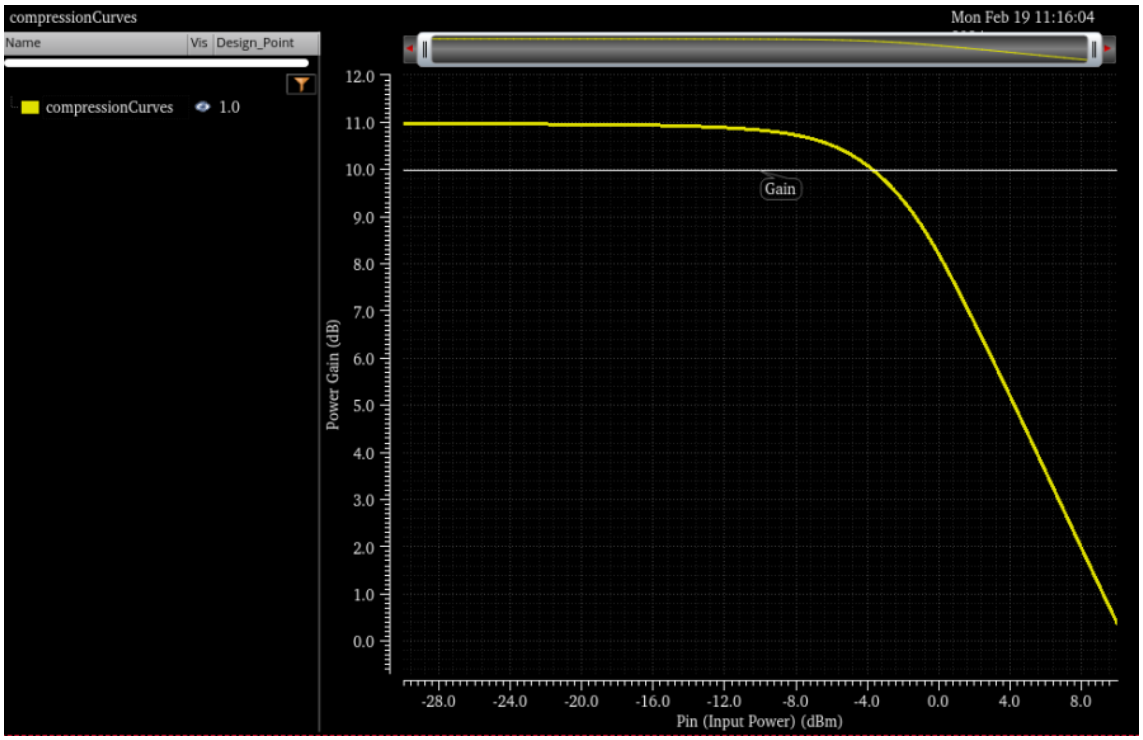


Figure 5.29: Power Gain vs. Input Power

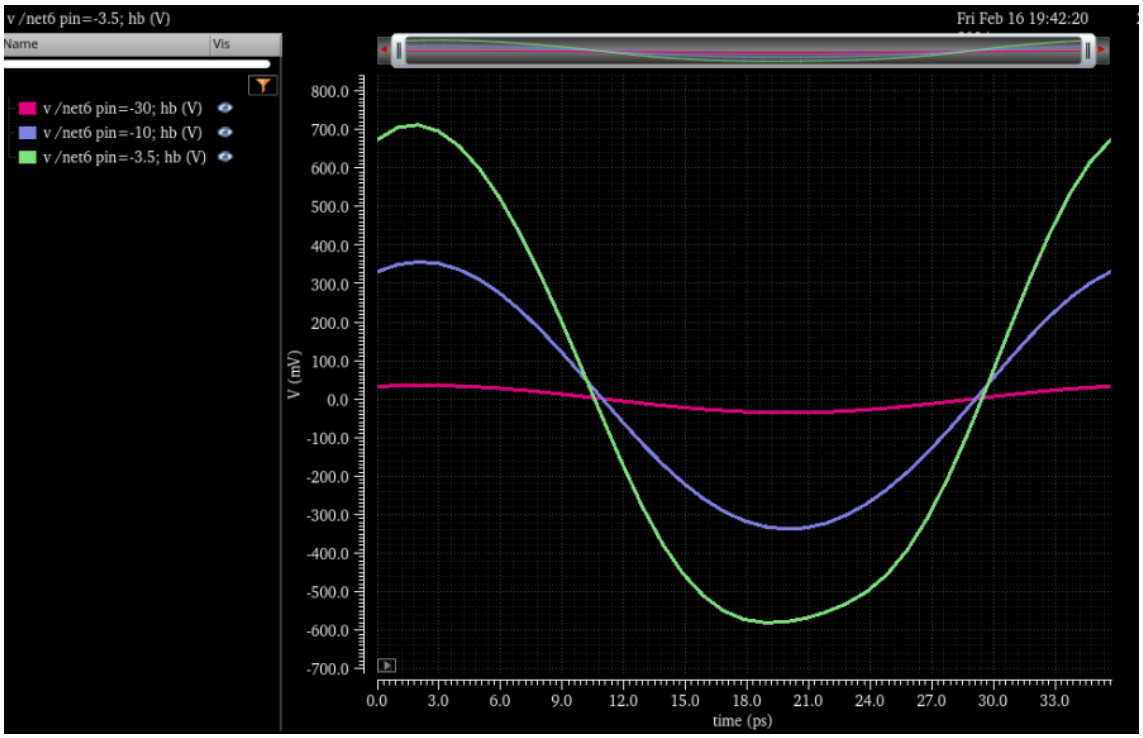


Figure 5.30: 1st Harmonic for 28GHz in different P1db values (compression points)

5.5.5 Area Calculation

The area of the device was easily calculated by measuring the size of the layout design and found that the area without including the pads is:

$233.36\mu m \cdot 354.83\mu m = 0.082mm^2$

and the area including the pads is

$400.16\mu m \cdot 380.89\mu m = 0.15mm^2$.

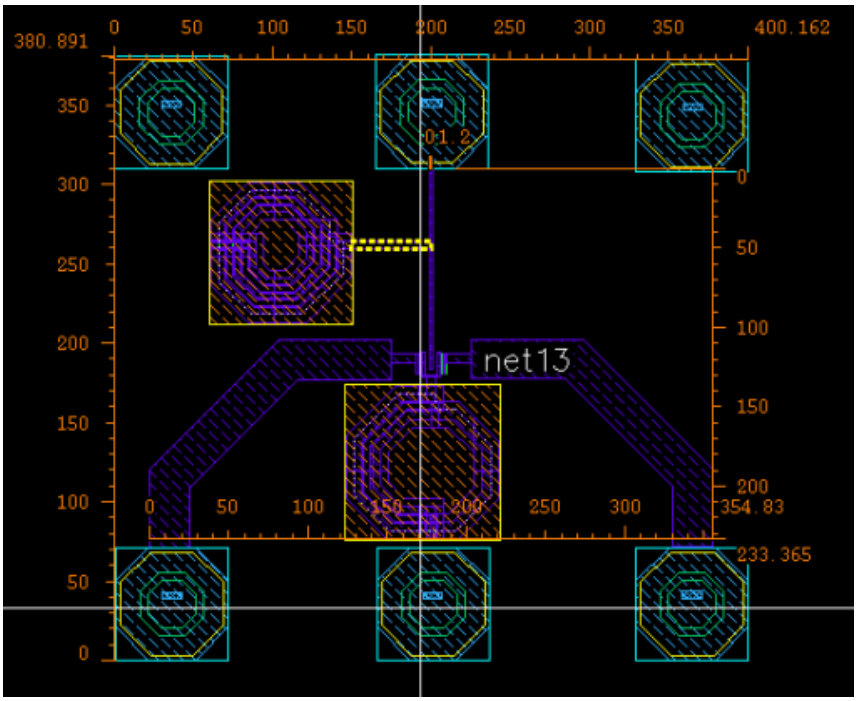


Figure 5.31: Area Calculation

5.5.6 Power Consumption Calculation

The power consumption of the LNA can be calculated by multiplying the supply voltage with the dc current. The dc current is found at the $I_D - V_G$ characteristic for the value of v_{gate} = 470mV the I_D= 18.32 mA and the supply voltage is 0.8V

$$\text{power consumption} = (I_D + I_{bias}) \cdot V_{supply} = (18.33mA + 2mA) \cdot 0.8V = 16.29mW$$

5.6 Evaluation and Comparison with other works

At first, in **5.7 Table** the final parameters and corresponding values utilized in constructing this LNA are presented :

Final Design Parameter Values	
v_{drain} (supply voltage)	0.8 V
v_{gate}	470 mV
v_{bulk}	0
Length	18 nm
Width	72 um
number of fingers	16
number of gate fingers	1
number of multipliers	9
gate (series) inductor	314 pH
drain inductor	519 pH
source (degeneration) inductor	60 pH

Table 5.8: Final Design Parameters and Transistor Sizing Values

To establish a meaningful metric of comparison, it's crucial to assess the specifications achieved in this study against those of comparable works using same and different processes. This comparison not only provides insight into our design's performance but also helps gauge its efficiency within the broader context of diverse manufacturing processes and amplifier configurations.

In **5.8 Table** it can be observed that this work presents very interesting results. The LNA showcased here demonstrates excellent linearity, low noise figure, and minimal power consumption. Given its single-stage topology, it can be replicated and utilized in a 2-stage or multiple stage configuration, connected in series to achieve higher overall gain. Each additional stage is expected to contribute an approximate gain increase of +10 dB. However, it's crucial to note that while increasing gain, there will be a notable reduction in linearity and increase of the power consumption.

The FoM created to compare this work with the others LNAs in Ka-band incorporates all the metrics :

$$FoM = Gain(dB) + IIP3(dB) + 20 \cdot log(f_c(GHz)) - NF(dB) - 10 \cdot log(P_{DC}(mW))$$

Comparison with other works							
	This work	[25]	[26]	[27]	[28]	[29]	[30]
Process	**22nm FD SOI**	22nm FD SOI	0.13um SiGe	22nm FD SOI	40nm BULK	45nm SOI	GaAs pHEMT MMIC
Frequency (GHz)	**28**	28/38	28	23-40	25-34	14-31	28
Structure	**CS**	3 Cascaded Cascode	Cascode	Cascode	1 Cascode 2 Differential Stages	Cascode	CS
NF(db)	**1.88**	4.9-4	2.8	1.8	3.4	1.4	3.84
Gain(dB)	**10.62**	24.8/ 22.4	16.2	12	18.4	12.8	10.8
Power Consumption (mW)	**16.29**	13.6	8.2	5	21.5	15	NA
P1dB(dBm)	**-3.6**	-25/ -20.3	-12	-7.9	-13.4	NA	NA
IP3(dBm)	**6.4**	-15/ -10.3	-2	2.1	-3.4	NA	NA
Area(mm^2)	**0.15***	0.31	0.1	0.21	0.26	0.3	NA
FoM	**31.97**	22.51/ 28.36	31.21	34.25	27.21	NA	NA

*area measured with pads

Table 5.9: Comparison of this work to LNAs designed in different processes

Chapter 6

Conclusion and Future Work

This thesis delves into the exploration of nano-scale Low-Noise Amplifier (LNA) design of mm-Wave frequency integrated circuits. The primary objective is to operate at low noise power while maintaining high performance levels. This work focuses mainly on presenting the detailed methodology for designing an LNA, a critical component in a receiver chain, specifically using the 22nm FD SOI process at a frequency of 28GHz. A meticulous methodology is followed to create step by step the schematic design of the LNA, by estimating the designing parameters, doing trade-offs between them, using optimizers to achieve better results, implementing real components for realistic measurements and performing layout design and extraction to ensure that the electrical and physical characteristics of the circuit meet performance specifications. Furthermore, an intriguing exploration into design utilizing the Inversion Coefficient, a method based in the Simplified EKV Model, is studied. Parameter extraction is performed and the modeled characteristics are compared against the actual measurements, verifying that the model can actually be used in this work particularly highlighting that the FoM $\frac{g_{ms} \cdot f_t}{IC}$ reaches maximum at the moderate inversion, offering a good trade-off between gain, noise and power consumption.

In conclusion, this work demonstrates the feasibility of achieving satisfactory specifications in LNA design by utilizing SOI technologies and adhering meticulously to the methodology. While it's acknowledged that parasitics present persistent challenges, there's an intriguing avenue for future exploration and advancement. Specifically, further optimization of layout design holds promise for enhancing results. Furthermore, employing Monte Carlo analysis will provide a statistical evaluation of the LNA's performance and variability under uncertain and variable conditions. This involves running multiple analyses with randomly selected parameter values to simulate environmental factors affecting circuit performance.. Additionally, a prospect for future work involves replicating and implementing the designed LNA in a two-stage amplifier topology, which could provide valuable insight into parameter variations such as linearity and power consumption, as well as potential gains compared to the single-stage common source topology.

Chapter 7

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