Technical University of Crete

Department of Electronic and Computer Engineering
Electronics Laboratory

Design of a Variable Gain Amplifier (VGA) for a RF Receiver with DC-Offset Correction in 90nm CMOS Technology

A Thesis

by

Vasileios Mylonakis

Approved by:

Bucher Matthias, Assistant Professor (Supervisor)
Kalaitzakis Konstantinos, Professor
Balas Costas, Associate Professor

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ABSTRACT

The purpose of this thesis is the design of a variable gain amplifier (VGA) for a Radio-Frequency (RF) receiver, providing simultaneously a noticeable gain range of approximately 40dB (-10.6dB~31.3dB) and achieving a 3dB bandwidth of 2.1GHz.The VGA is comprised of a 3-stage modified Cherry-Hooper amplifier while the embedded negative feedback deals with the DC-Offset Correction. One main feature of the Cherry-Hooper amplifier, which is the main building block of the circuit, is that is inductorless which helps in saving chip space. Along with that, inverse scaling technique is employed resulting in broadening the overall bandwidth if the VGA and reducing the power consumption. In the first Chapter an introduction to RF and wireless technology is made, emphasizing on the RF interface. Besides that, design issues and receiver's concepts are discussed. In the second Chapter VGA concepts are discussed, while in the third Chapter VGA design procedure is thoroughly described. Finally at fourth and final Chapter simulation results are shown with interesting conclusions respectively.

ACKNOWLEDGEMENTS

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CHAPTER 1

INTRODUCTION

The insatiable requirement for high-speed real-time computer connectivity anywhere, at any time, fuelled by the wide-spreading acceptance of the Internet Protocol, has accelerated the birth of a large number of wireless data networks. Buzzwords, such as WiFi, Bluetooth and WiMax, have already become everyday language even for people unfamiliar with their technological meaning. They all, however, refer to the same basic functionality: the transfer of high-speed data through wireless networks.

As we proceed in the twenty-first century, the variety of wireless standards is far from converging, since each one has its own peculiar advantages. Trying to figure out their evolution is very difficult. The only certain fact is that all of them will seek to enable digital communications through broadband wireless equipment, and one of the main tasks being the capability of allowing a large number of different users to coexist and operate in a crowded and often unregulated electromagnetic environment. The design of modern digital wireless modems and transceivers, capable of supporting high-speed data protocols in such wild scenarios, is very different from the traditional one. Many of the components in the wireless chain require an integration scale whose cost can be justified only for extremely large production quantities, thus, their design and production is way beyond the capability of most hi-tech industries. As a consequence, as happened with digital processors and memories, R&D engineers must now learn how to manage using off-the-shelf multi-purpose components manufactured by a few giant chipmakers.

In contrast, several of the most critical subsystems, such as voltage controlled oscillators (VCO), linear power amplifiers, fast-hopping synthesizers and so on, are so diversified and application-dependent, that in many cases there exist no suitable components from standard lines of products.

1.1 The RF Interface

Wireless transmitters and receivers can be conceptually separated into baseband and RF sections. Baseband produce their output over the range of frequencies that transmitters take their input from. The underlying rate at which data can flow through the system is determined by the bandwidth of the baseband section. The improvement of the fidelity of the data stream communicated requires a considerable amount of signal processing, as well as the reduction of the transmitter's load which is placed on the transmission medium for a particular data rate. The conversion of the processed baseband signal up to the assigned channel and the signal's injection into the medium is the prime responsibility of the RF section of the transmitter.
There are two primary design goals concerning the transmitters. Firstly, they ought to transmit a specified amount of power, while consuming as little power as possible. Secondly, they must avoid interference with transceivers operating on adjacent channels. When designing receivers on the other hand, there are three primary design goals. First, they must faithfully recover small signals. They also have to reject any possible interference outside the desired channel and finally, receivers must be frugal power consumers, like transmitters.

1.1.1 Small Desired Signals

In order to detect small input signals, receivers have to be very sensitive. It is typical for receivers to operate with as little as 1 μV at the input. It is the noise generated in the input circuitry of the receiver that limits its sensitivity. Therefore, noise and consequently the ability to detect noise by simulation are both important concerns.
As shown in Figure 1, a typical superheterodyne receiver [1] first filters and then amplifies its input with a low noise amplifier or LNA. It then translates the signal to the intermediate frequency or IF by mixing it with the first local oscillator or LO. The noise performance of the front-end is determined mainly by the LNA, the mixer, and the LO.

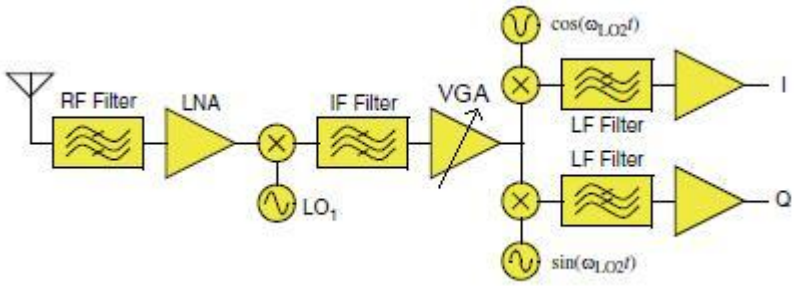


Fig.1 A superheterodyne receiver's RF interface.

The small input signal level requires a tremendous amount of amplifications by the receivers. The need of 120 dB is a common case. As a result of such a high gain, any coupling from the output back to the input can cause problems. It is important to mention at this point that the superheterodyne receiver's architecture is used not only to spread that gain over several frequencies in order to reduce the chance of coupling, but also to result in the first LO being at a different frequency than the input. As a consequence, prevents the contamination of the small input signal by the large one.
There are numerous reasons why the direct conversion or homodyne architecture is a candidate to replace the superheterodyne architecture in some wireless communication systems. In this architecture the RF input signal is directly converted to baseband in one step. Therefore most of the gain will be at baseband and the LO will be at the same frequency as the input signal. In this case, it is very important to determine the impact of small amounts of coupling. Thus careful modeling of the stray signal paths is required, such as coupling through the substrate, between package pins, bond wires and through the supply lines.

1.1.2 Large Interfering Signals

Receivers must be sensitive to small signals even in the presence of large interfering signals, often known as blockers. They are needed, when a strong transmitter broadcasting in an adjacent channel tries to receive a weak or distant signal. The interfering signal can be 60-70 dB larger than the desired signal. It can also act to block its reception by overloading the input stages of the receiver or by increasing the amount of noise generated in the input stage. Both problems result if the input stage is driven into a nonlinear region by the interferer. In order to avoid these problems, strict linearity is required from the front-end's part, which makes linearity a crucial factor in receivers. Receivers are narrowband circuits and so the nonlinearity is quantified by measuring the intermodulation distortion. This involves driving the input with two sinusoids that are in band and close to each other in frequency and then measuring the intermodulation products.

1.1.3 Adjacent Channel Interference

Another important factor in the transmitter is the distortion, since nonlinearity in the input stages can cause the transmitted signal's bandwidth to spread out into adjacent channels. The bandwidth of the signal is limited before the transmitter's power amplifier (PA, as shown in Figure 2) and the intermodulation distortion in the PA causes the bandwidth to increase again. This process is referred to as Spectral Regrowth. A large increase will prevent the transmitter from meeting the adjacent power requirements.

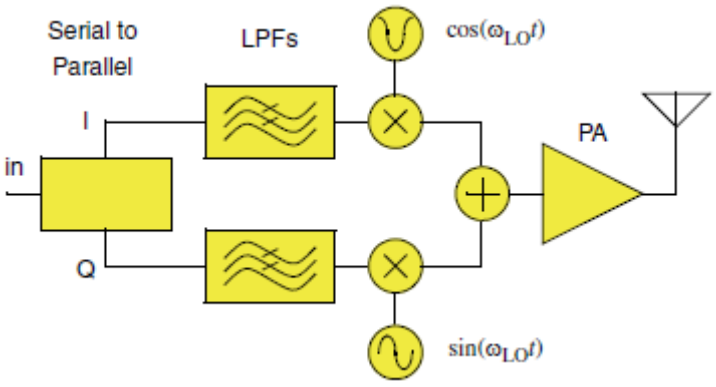


Fig.2 A digital direct conversion transmitter's RF interface.

The spectrum of a narrrowband signal is described in Figure 3. The signal is replicated at multiples of the carrier due to nonlinearity, an effect known as harmonic distortion. It also adds a skirt to the signal that increases its bandwidth, am effect referred to as intermodulation distortion. Eliminating the effect of harmonic distortion is possible with a bandpass filter; however the frequency of the frequency of the intermodulation distortion products overlaps the frequency of the desired signal. For that reason it cannot be completely removed with filtering.

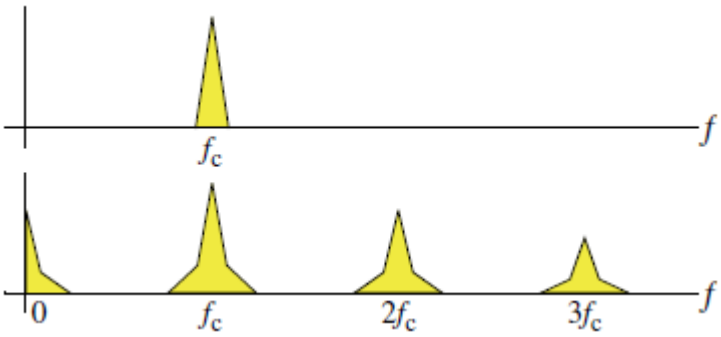


Fig.3 Spectrum of a narrowband signal passing through a nonlinear circuit.

1.2 Design Bottleneck

Nowadays mobile devices and transceivers contain more than one million transistors, however a small proportion of that operates in RF range and the rest take place in low-frequency baseband and digital signal processing, Figure 4.

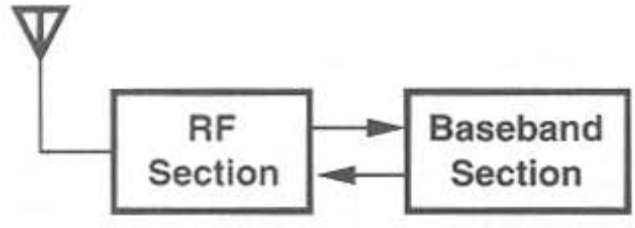


Fig.4 RF and baseband processing in a transceiver.

Nevertheless, despite the fact that transistors working in baseband frequencies are greater in number, RF transistors defines the design bottleneck for the following 3 reasons [2]:

- **Multidisciplinary Field**
  In contrast to other types of analog and mixed-signal circuits, RF systems demand a good understanding of many areas that are not directly related to integrated circuits (ICs).These areas shown in Figure 5 have been studied extensively over the last century, changing rapidly as time passes. That makes it quite difficult for an engineer to collect all the available information he needs in a small amount of time. As a result communication theory, RF system theory and analog design should be blended together in order to reach the desired outcome. This gives the RF engineer fewer options to work with since the standards of the other fields should be met. Moreover as the industry moves toward higher integration and lower cost, RF and wireless design demands increasingly more concurrent engineering, forcing IC designers to have sufficient knowledge of all sectors depicted in Figure 5.

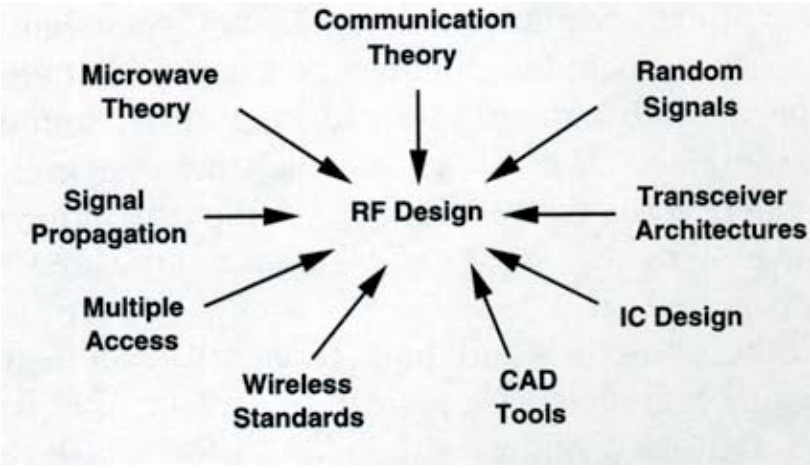


Fig.5 Disciplines required in RF design.

- **RF Design Hexagon**
  RF circuits must process analog signals with a wide dynamic range at high frequencies. It is interesting to note that the signals must be treated as analog even if the modulation is digital or the amplitude carries no information. The trade-offs involved in the design of such circuits are shown in the "RF design hexagon" shown in Figure 6.

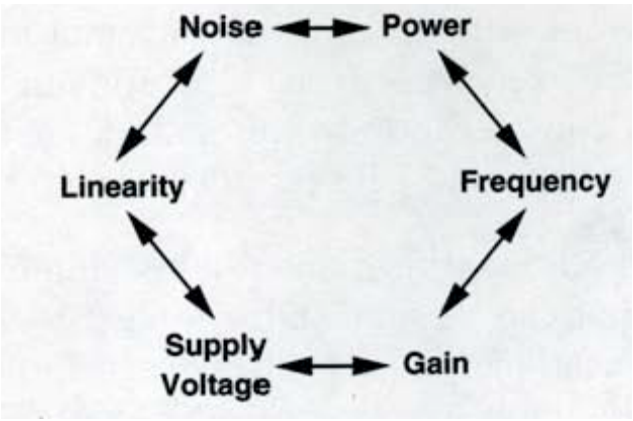


Fig.6 RF design hexagon.

What the most important is that compared to analog design of IC circuits, RF circuits do not benefit that much from technological advancements due to the fact that they require external components such as inductors which are difficult to place on the chip even in most recent IC processes.

- **Design Tools**

  Computer-aided analysis and synthesis tools for RF ICs are still in their infancy, forcing the designer to rely on experience, intuition, or inefficient simulation techniques to predict the performance. One issue is that circuits designed at a computer program are simulated in the time domain to include time-variant parameters and in order to obtain the spectrum of the frequency domain the resulting waveforms are transformed. However this procedure requires a significant amount of time, not to mention the fact that there are inaccuracies at the results since sometimes random noise is not taken into consideration. However it should be mentioned that as time passes these tools have shown dramatic evolution adding more features and accuracy at the hands of the designer. One of these tools is Cadence Virtuoso, the main design tool that this thesis was implemented.

1.3 Receiver's Concepts

1.3.1 Basics

The main purpose of the receiver is to accept the signals through the antenna from the transmitter and perform various tasks such as amplification, mixing, demodulation and then pass it on for digital signal processing. Selectivity and sensitivity are two parameters affect the performance of the receiver to a large extent. Apart from them, linearity gain and noise performance are crucial factors when designing a receiver.

1.3.2 Sensitivity

Receiver's sensitivity is specified by the minimum amount of signal that can be sensed, with noise occurrence, at a standard distance. In simple words, the distance between receiver and transmitter is determined.Sensitivity is specified in terms of dBm (decibels relative to 1 mW). Total sensitivity is affected not only from the noise figure but also from the gain of all the individual blocks. The noise Figure is defined as the ratio between the SNR at the input and the SNR at the output of the circuit.

$$F \equiv \frac{InputSNR}{OutputSNR} \qquad \textbf{(1.1)}$$

$$NF \equiv \log(F) \qquad (dB) \tag{1.2}$$

where F is the noise factor and NF is the noise figure of the system.

Noise Figure is usually estimated in relation to a specific source impedance and noise temperature. In wireless communication systems, the standard values for transmission lines resistance is Rs = 50Ω and at temperature, T=293 K. The overall noise figure at an individual block like the VGA can be expressed combining the gain and the output noise added by the system. G is the power gain of the amplifier with input signal power P_{input} and input noise power N_{input}. N_{added} is the noise added externally to the system, GP_{input} the output signal power and by adding them results in output noise power. The noise figure is given by:

:

$$F = \frac{(\frac{P_{input}}{N_{input}})}{(\frac{GP_{input}}{GN_{input} + N_{added}})} \tag{1.3}$$

$$F = 1 + (N_{added} / GN_{input}) = 1 + (N_{added,input} / N_{input}) \tag{1.4}$$

where $N_{added,input}$ is the input referred added noise from the amplifier.

1.3.3 Noise Figure

The noise figure of the overall receiver can be calculated by the noise figure of the individual cascaded blocks in the receiver chain. The noise figure of the entire cascaded chain depends on the noise figure of the individual blocks as well as the gain distribution. For a receiver chain consisting of 2 blocks cascaded with proper matching, the total output noise is given by

$$P_{noise,output} = F_1 P_{noise,input} G_1 G_2 + (F_2 - 1) P_{noise,input} G_2 \tag{1.5}$$

where G_1 and G_2 are the power gains of the individual blocks with corresponding noise figures F_1 and F_2.

The output SNR of the cascaded blocks is given by

$$SNR_{output} = \frac{S_{out}}{P_{noise,output}} = \frac{S_{input} G_1 G_2}{F_1 P_{noise,input} G_1 G_2 + (F_2 - 1) P_{noise,input} G_2} \tag{1.6}$$

Total cascaded noise figure can be calculated as

$$F = \frac{SNR_{output}}{SNR_{input}} = F_1 + \frac{(F_2 - 1)}{G_1} \qquad \textbf{(1.7)}$$

From the above equation it can be seen that the total noise figure of the cascaded blocks depends on the noise figures of the individual blocks as well as the gain of the first block. If the gain G1 is large then the noise from the succeeding blocks will have less effect on the overall noise figure. Hence the first block of the receiver, usually LNA, and VGA in this thesis, must have low noise figure and enough gain.

1.3.4 Selectivity

Selectivity is the measure of performance of the receiver to separate the wanted or required signals from those which are not required. Selectivity is significant when the receiver has to choose between a weak desired signal and a strong neighbouring interfering/undesired signal. There is no quantitative way to measure the selectivity of a receiver but usually specified as blocking masks used in filtering, nonlinearity and phase requirements in the circuit.

1.3.5 Main blocks

The receiver is divided into 3 main functional blocks:

- Front end: all the circuits whose functionality is affected by the RF frequency, such as RF front filters, low-noise amplifiers (LNA), high frequency mixers etc.

- Intermediate frequency (IF) chain: all the circuits operating at non-zero IF frequency ,which are not always met like the circuits at the front end.

- Backend: all the circuits operating at a frequency below IF and RF frequencies, such as baseband processing, detector etc.

CHAPTER 2

FUNDAMENTALS OF VGA DESIGN

2.1 Frequency Response and Stability of Amplifiers

2.1.1 Miller Effect

Nowadays in most analog circuits with high performance requirements, trade-offs between the speed and other important parameters, such as gain, power dissipation and noise, exist. In practice most of these parameters trade with each other, making the design a multi-dimensional optimization problem. The analog design octagon, illustrated in Figure 7, suggests that the design of high-performance amplifiers requires deep intuition and experience in order to achieve the specifications given [3].

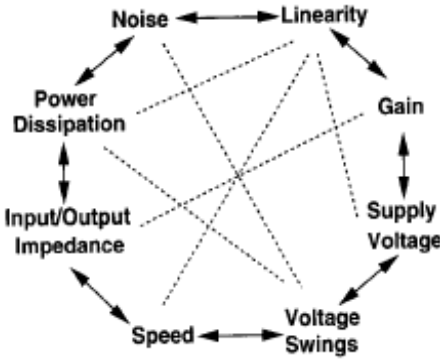


Fig.7 Analog design octagon.

Studying the frequency response of single-stage and differential amplifiers will make it easier to understand the frequency limitations of each circuit and the trade-offs set by them.

An important phenomenon that is related to frequency response, during the compensation techniques, is the **Miller Effect**. According to it, if the circuit depicted in Figure 8(a) can be converted to that of Figure 8(b) then $Z_1 = Z/(1 - A_v)$ and $Z_2 = Z/(1 - A_v^{-1})$, where $A_v = V_Y/V_X$.

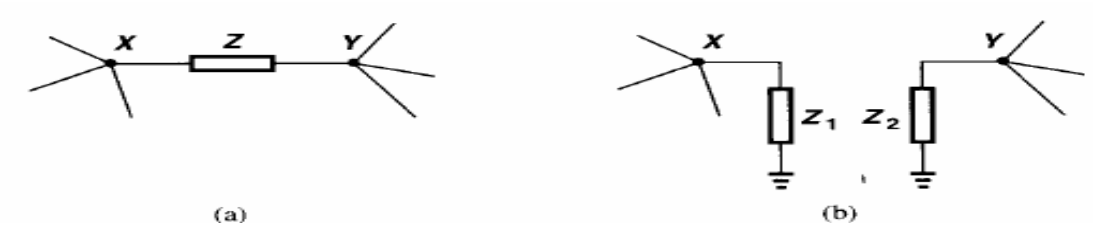


Fig.8 Miller effect on floating impedance.

This is very useful when it is needed to calculate the input and output impedance of a circuit. For example, let us consider the circuit shown in Figure 9(a), where the voltage amplifier has a negative gain equal to -A and is otherwise ideal. If it is needed to calculate the input capacitance we use the Miller Effect.

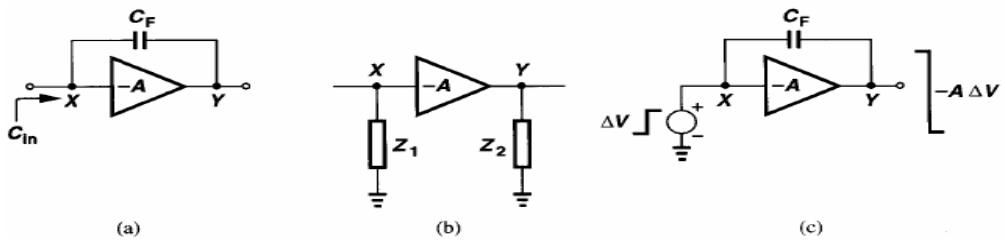


Fig.9 Voltage amplifier with negative feedback example.

First of all, according to the theorem, the initial circuit can be converted to the one depicted in Figure 9(b).If we apply a voltage step ΔV at the input ,then the voltage at the output will be -AΔV,yielding a total change of (1+A)ΔV in the voltage across C_F. Thus, the charge drawn by C_F from V_{in} is equal to (1+A)ΔVC_F and the equivalent input capacitance equal to $(1+A)C_F$.As a result,, the input capacitance is equal to $C_F(1+A)$,meaning that $Z = 1/(C_F s)$ and $Z_1 = [1/(C_F s)]/(1+A)$ Figure 9(c).

That was a simple example on how to calculate the input and output impedance of a circuit. However, Miller effect does not necessarily ensures us that we can calculate the input/output impedance of any complex circuit. It is important to know that the initial circuit can be converted to the one that Miller's theorem can be applied. If the impedance Z forms the only signal path between X and Y, then the conversion is often invalid (unique signal path). Nevertheless, Miller's theorem proves useful in cases where the impedance Z appears in parallel with the main signal Figure 10.

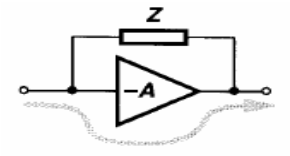


Fig. 10 Typical case for valid application of Miller's theorem

2.1.2 Association of poles with nodes

In order to understand the frequency response of a circuit we have to study the association of the poles created by the circuit, (and later the zeros) with the circuit's nodes. Considering the circuit depicted in Figure 11 it can be noticed that the circuit is consisted of two (ideal) voltage amplifiers in cascade form.

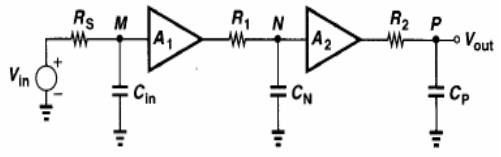


Fig. 11 Cascade of amplifiers.

C_{in} and C_N are the input capacitances of the first and the second amplifier respectively, whereas C_P stands for the load capacitance of the circuit.The overall transfer function can be written as

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_1}{1+R_S C_{in} s} \cdot \frac{A_2}{1+R_1 C_N s} \cdot \frac{1}{1+R_2 C_p s} \qquad \textbf{(2.1)}$$

According to the transfer function the circuit has three poles and more specifically $\omega_1=1/ R_sC_{in}$,$\omega_2=1/ R_1C_N$ and $\omega_3=1/ R_2C_p$,each of them determined by the total capacitance from each node to ground multiplied by the total resistance seen at the node to ground. In this simple occasion it can be said that each node generates one pole. However this is not correct because in most circuits, resistances or capacitances placed in a node parallel to the initial nodes, interact with the poles changing the transfer function and the frequency response. One example of this is the circuit depicted in Figure 12.

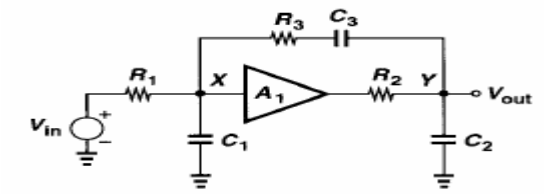


Fig.12 Example of interaction between nodes.

2.1.3 Multipole Systems

Observating the previous example, it can be easily concluded that a system with more than one pole is something common when it comes to analog design.In two-stage op amps, for example, each gain stage introduces a “dominant” pole. As it will be explained later, dominant pole is called that way because it crucially affects the system's total gain and phase margin in contrast with the other poles.

First of all it must be made clear how terms such as gain, bandwidth and phase margin are depicted on the Bode plots of a system and how can information be drawn from them. By studying the Bode plots of a feedback system at Figure 13,which depicts both gain $|\beta H|$ and phase $\angle \beta H$,firstly it should be noticed that the value of the gain of the system is the initial **20log|βH(ω)|**value, where **β** is the feedback coefficient. That value is stable for $\omega<\omega_{p1}$, where ω_{p1} is the dominant pole, and is the frequency point where gain starts to decrease. For $\omega_{p1}<\omega<\omega_{p2}$ gain drops linearly and when $\omega=\omega_{p2}$ then the gain will have been decreased by 20 dB/dec .At that point the bandwidth of the system can be found since it is the frequency of the ω_{p2} pole. By observing the phase Bode plot we can calculate the phase margin, which is the stability indicator of the system. In order to find the phase margin, we first find the pole-frequency at which the gain reaches and drops below zero, **20log|βH(ω)|=0.**Then using that specific frequency on phase plot we find the respective angle in degrees ($\angle \beta H$).By subtracting this angle from 180° the result is the phase margin (PM),$PM = 180° + \angle \beta H(\omega = \omega_1)$, where $\omega_1$is the gain crossover frequency. The bigger the value of the result the more stable the system is and this will be explained later.

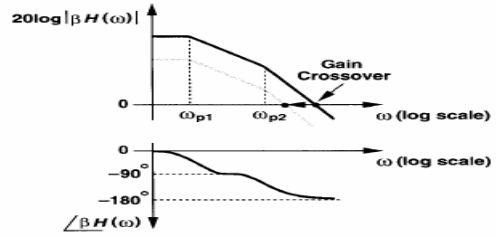


Fig.13 Bode plots of loop gain for a two-pole system.

First of all, to see theory in practice we consider that the above figure depicts the Bode plots of a loop-gain for a two-pole system. As described before, the magnitude begins to drop at 20 dB/dec at **$\omega=\omega_{p1}$** and at 40dB/dec at **$\omega=\omega_{p2}$.**On the same time phase changes at $\omega=0.1\omega_{p1}$, reaching -45° and -90° at $\omega=\omega_{p1}$ and $\omega=10\omega_{p1}$ respectively. Phase begins to drop again, because of the non-dominant pole ω_{p2} and assuming that **$0.1\ \omega_{p2}>10\ \omega_{p1}$** ,by observing the figure it can be concluded that when $\omega = \omega_{p2}$ then $\angle \beta H$=-135°.As a result the phase margin is |180°-135°|=45° declaring that the system is quite stable since the value is far from zero. However it is important to notice the system's behavior when changing the amount of the feedback, i.e. the value of β.Decreasing the β we reduce the feedback and this results in the faded gray plot of the Figure 13 .First of all it is essential the fact that the phase plot does not change, in contrast with the gain plot where the curve is shifted to the left. This in turn moves the gain crossover point to the left too, resulting in more stable system since $\angle \beta H$ is stable. All in all, the less feedback we demand the more stable the system is.

Moreover it is important to study, if additional poles or zeros affect the magnitude and the phase at the same rate. Going back to the previous example we noticed that, the phase begins to change at approximately one-tenth of the pole frequency whereas the magnitude begins to drop only near the pole frequency. For that reason the phase is much more affected by the addition of a pole or zero, than the magnitude. Studying the following plot Figure 14 will prove that.

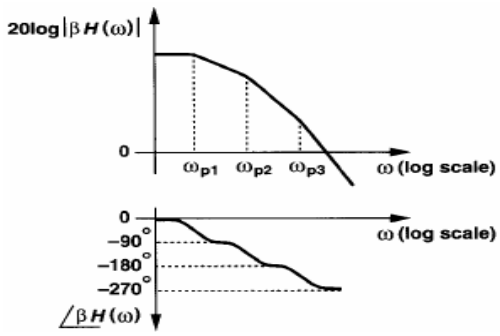


Fig.14 Bode plots of loop gain for a three-pole system.

As it can be seen the third pole ω_{p3} shifts the phase crossover point to the left (lower frequencies) and as a result $|\beta H|$ drops to below unity at a frequency for which $\angle\beta H$>-180°.This leads to a non-stable system and oscillations.

After studying the frequency response of amplifiers and multipole systems basic topologies of a simple variable gain amplifier will be studied, examining their gain and bandwidth respectively.

2.2 Gain and Bandwidth Specifications

The design of an amplifier requires an analysis of the trade-offs involved in fulfilling the specifications. For example, the higher the gain of the amplifier, the lower its bandwidth and the higher its non-linearity. It is apparent from the latter example that it is not trivial to achieve all specifications. Thus, the selection of a topology is based on fulfilling the most of the requirements, ensuring that the system operates in the desired output.

A simple differential amplifier is given in Figure 15. The gain of this amplifier is given by

$$A_v = g_m(r_{o2} \| r_{o4}) \qquad \textbf{(2.2)}$$

where g_m is the transconductance of the input transistors M1 and M2. The -3dB bandwidth of the amplifier is given by

$$\omega_{-3dB} = \frac{1}{C_L(r_{o2} \| r_{o4})} \qquad \textbf{(2.3)}$$

Equations 2.1 and 2.2 propose that that the gain of the amplifier is proportional and the -3 dB bandwidth is inversely proportional to its output resistance, leading to a trade-off between the maximum gain that can be achieved and the speed of the amplifier. Two stage amplifiers could be implemented to obtain higher gain, at the cost of additional poles and increased power consumption.

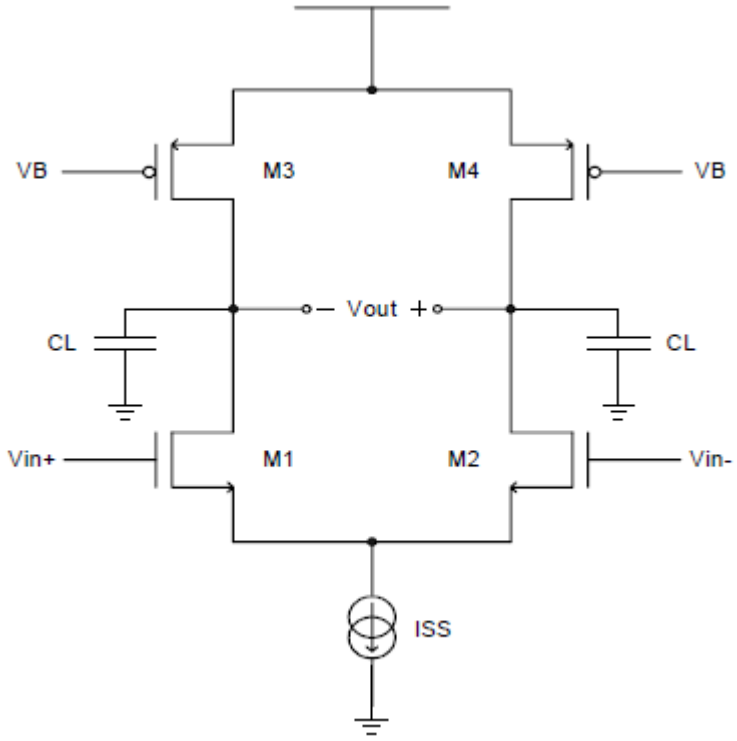


Fig.15 Differential amplifier with active load

2.2.1 Cascoding

By compromising the output voltage swing, the same gain as a two stage amplifier could be obtained by using a cascode structure with lower power dissipation [4]. The gain of the cascode stage shown in Figure 16 is given by

$$A_v = g_{m1} r_{o1} [(g_{m2} + g_{b2}) r_{o2} + 1] \quad \textbf{(2.4)}$$

$$A_v \approx g_{m1} g_{m2} r_{o1} r_{o2} \quad \textbf{(2.5)}$$

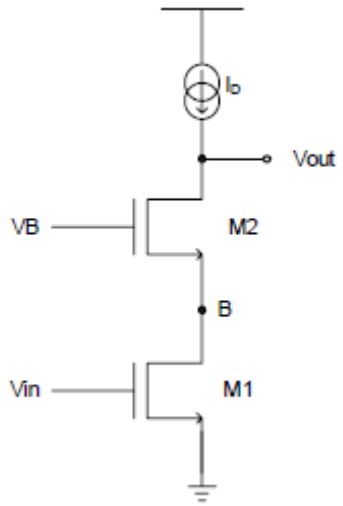


Fig.16 Cascode amplifier

A major advantage of the cascode structure over a common-source stage is the significant reduction in the Miller effect observed by the gate-drain capacitor C_{GD1} due to the low impedance seen by the capacitor, looking into node B, for small values of R_D [3]. The pole associated with the capacitors at node B is given approximately by

$$\omega_{-3dB} \approx \frac{g_{m2} + g_{mb2}}{2C_{GD1} + C_{GB1} + C_{SB2} + C_{GS2}} \quad \textbf{(2.6)}$$

This normally results in a better frequency response of the cascode structure as compared to a simple common-source amplifier. On the other hand, the cascode structure has limited output voltage swing. This prevents using broadly the cascade structure from low voltage applications. The aforementioned drawback can be avoided achieving higher output voltage swing by employing the folded cascode structure as depicted in Fig. 17. An additional major advantage of the folded cascode structure is that it supplies the transistors with more headroom, preventing the cascode transistor from stacking on the top of the input device. However, the folded amplifier provides lower gain at lower bandwidth (due to lowering of the pole at the folding point) while consuming higher power.Poles and zeros theory with frequency compensation will be better examined at the end of this chapter.

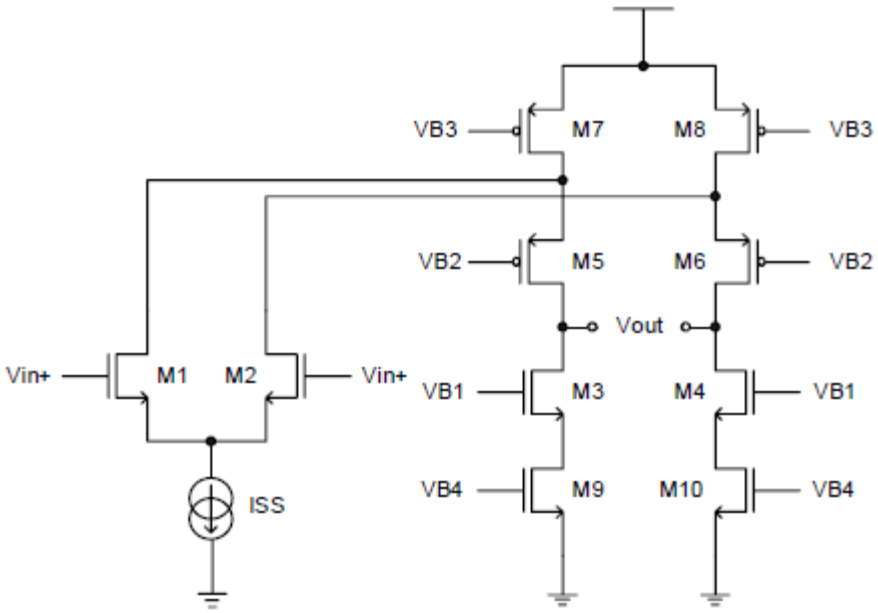


Fig.17 Folded cascode amplifier

2.2.2 Gain boosting in differential amplifiers with diode connected loads

In differential pair amplifiers with diode-connected loads, the loads consume voltage headroom, limiting the output voltage swing, gain and the input common mode range. One solution to boost the output voltage gain is to decrease the transconductance of the load transistor by reducing the W/L value of the load. However, this solution includes the drawback of increasing the overdrive voltage, and thus decreasing both the output common mode level and the voltage swing.
An alternative solution that bypasses the aforementioned disadvantage is to add PMOS current sources [4] in parallel to the load transistors, as shown in Fig. 18. The key feature of this scheme is that splits the current between the load and the current source. It leads to the advantage of reducing the W/L value of the load transistor without changing the overdrive voltage. Thus, the transconductance of the load can be decreased without compromising the output voltage swing.

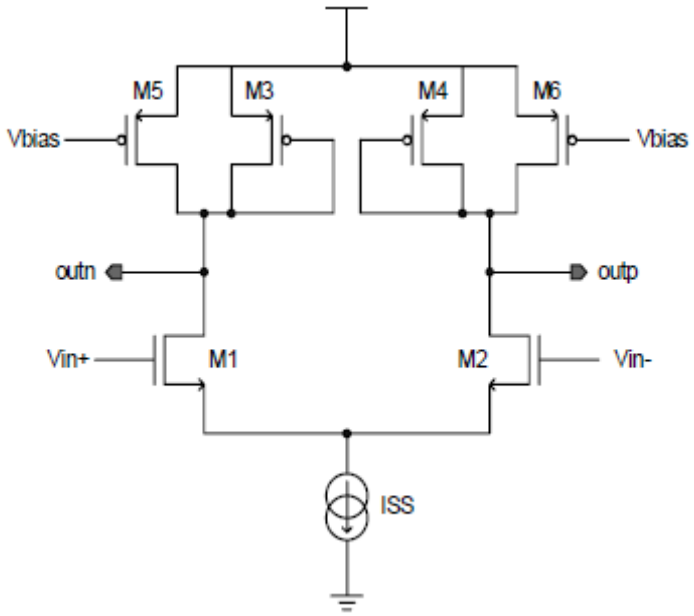


Fig.18 Addition of current sources to increase the gain of differential amplifier with diode-connected load.

In order to illustrate the function of the aforementioned scheme, we provide the following example: If transistors M5 and M6 of Figure 18 carry 40% of the drain current of M1 and M2, and the load transistors M3 and M4 carry the remaining 60%, their transconductance 10 decreases by a factor of 2/5 since the W/L ratios of M3 and M4 can also be decreased by the same amount without affecting their overdrive voltage. Thus, the differential gain increases by approximately 5/2 times that of the gain when the PMOS current sources are not included in the circuit. A disadvantage of this method of increasing the gain is that the current sources add parasitic capacitances to the output node of the circuit, slightly lowering the -3dB bandwidth.

2.3 Frequency Compensation

Nowadays, multistage amplifiers are an essential part when designing in modern technologies, as the single-stage amplifiers cannot live up to the expectations of low-voltage design. Furthermore, short-channel effect of the sub-micron CMOS transistor degrades output impedance and as a result the gain of the amplifier is reduced at a large scale. That makes frequency compensation at multistage amplifiers an essential sector and many frequency-compensation topologies have been reported based on pole-splitting and pole-zero cancelation techniques. These techniques will be explained later on having as an example a 2-stage amplifier. However, in order to reach the optimum results not only provided stability criteria but also trial and error procedure is required. At the same time, it should be noticed that the provided stability criteria find difficulties from theory to practice since any extra stage consumes more power, requires more complicated circuit structure and may reduce the bandwidth dramatically. In order to understand the more complex frequency compensation topologies, it is highly recommended to start examining the frequency response of a single-stage amplifier.

2.3.1 Single-stage amplifier review

Single-stage amplifier's frequency behavior is quite stable since the amplifier has only one left-half-plane (LHP) pole, as it can be noticed from its transfer function.

$$A_{v\sin gle}(s) = \frac{g_{mL}R_L}{1+sC_LR_L} \tag{2.7}$$

where g_{mL} is the output stage transconductance, R_L is the loading resistance and C_L the loading capacitance, which is in fact the compensation capacitor of the amplifier. The GBW of the amplifier is obtained by the equation (2.8).

$$GBW = \frac{g_{mL}}{C_L} \tag{2.8}$$

and the phase margin PM of the amplifier is 90°, because of the single pole. From () it can be deducted that GBW can be increased, by increasing the g_{mL} factor or decreasing the loading capacitance. However, the existence of many parasitic poles and zeros (p_{par} and z_{par}) should not be neglected as they affect the stability of the amplifier. The transistor's dimensions and the bias current determine the position of the parasitic poles and zeros, frequency of which, as a rule of thumb, should be at least the double of the GBW. In other words, there is a maximum g_{mL} and a minimum C_L for the single-stage amplifier at which min(p_{par} and z_{par})>2GBW. Nevertheless, the dc gain of the single-stage amplifier is relatively small and to deal with this drawback gain-boosting topologies are employed on the initial circuit. However, these topologies require a larger supply voltage, a more complicated circuit design and at the same time limit the maximum output voltage swing. It should be noticed though, that the bandwidth of the amplifier is not affected due to its independence of R_L.

2.3.2 Two-stage amplifier with Simple Miller Compensation (SMC)

As mentioned above single-stage amplifier has excellent frequency response, however cascode configuration maybe be needed in order to increase the gain. Nevertheless, cascode configuration cannot live up to the expectations of the modern demanding low-voltage design. To face this problem two-stage SMC amplifier [5] is commonly used Figure (19).

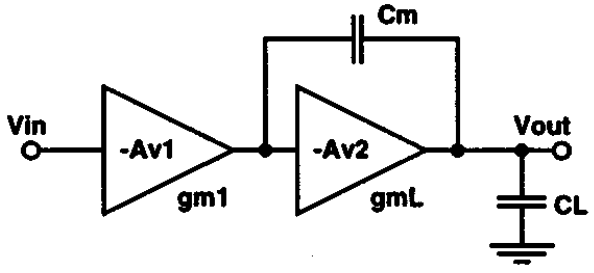


Fig.19 SMC amplifier

The transfer function of the above structure is given by:

$$A_{V(SMC)}(s) = \frac{g_{m1} g_{mL} R_{o1} R_L (1 - s\frac{C_m}{g_{mL}})}{(1 + sC_m g_{mL} R_{o1} R_L)(1 + s\frac{C_m}{g_{mL}})} \qquad \textbf{(2.9)}$$

It can be noticed that there are two LHP poles and one right-half-plane (RHP) zero. The dominant pole is $p_{-3dB}=1/C_m\ g_{mL}\ R_{o1}R_L$, the non-dominant pole is $p_2= g_{mL}\ /C_L$ while the RHP zero is $z_1=-\ g_{mL}\ /C_m$, where C_m is the compensation capacitor. It is a rule that both p_2 and z_1 should be at frequencies higher than the unity-gain frequency in order to ensure circuit's stability. How can this condition be achieved? An easy solution is to use a relatively large capacitor C_m in order to move the dominant pole to a lower frequency. However by doing this, the GBW is linearly reduced since $GBW=g_{m1}/C_m$.As a result it is suggested that GBW is set to be at the half of the frequency of p_2 in order to obtain a good phase margin and bandwidth at the same time.

$$C_L = \frac{1}{2}\frac{g_{mL}}{g_{m1}} C_m \qquad \textbf{(2.10)}$$

If $g_{m1}\ /\ g_{mL}$ has a large value then C_m is quite large compared to C_L according to (2.10).In this case, z_1 is at a frequency before or close to the one of p_2,as shown in Figure 20. On the other case where p_2 is before z_1 we receive a small gain and the amplifier shows a quite unstable behavior if there are parasitic poles and zeros. However if z_1 is after p_2 we may have low gain but the phase margin achieves quite good values. In other words the position of the RHP zero sets the tradeoff between gain and the phase margin.

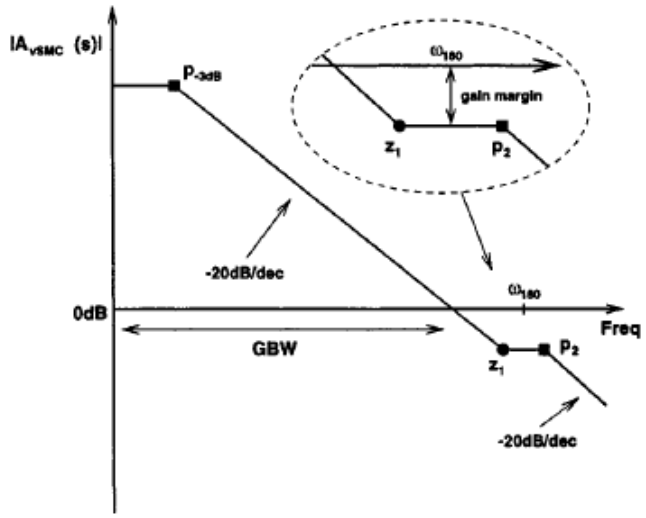


Fig.20 Frequency response of a SMC amplifier

Using (2.9) and (2.10) GBW is given by

$$GBW = \frac{g_{m1}}{C_m} = \frac{1}{2}\left(\frac{g_{mL}}{C_L}\right) \qquad \textbf{(2.11)}$$

which compared to the single-stage amplifier has the half value. The GBW of a two-stage SMC amplifier cannot be increased by increasing g_{m1}.This happens because the required C_m is increased proportionally with g_{m1} so the g_{m1}/C_m has a constant value. One way of improving GBW is increasing the output transcoductance g_{mL} and decreasing the loading capacitance C_L at the same time. Then the PM is evaluated by the following expression:

$$PM = 180° - \tan^{-1}\left(\frac{GBW}{p_{-3dB}}\right) - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{|z_1|}\right)$$

$$\approx 63° - \tan^{-1}\left(\frac{g_{m1}}{g_{mL}}\right) . \qquad \textbf{(2.12)}$$

By noticing the equation (2.12) it can be concluded that the PM is highly affected by the g_{m1}/g_{mL} ratio, which in fact reveals the RHP zero effect on the PM. The RHP zero is created by the feedforward small-signal current that flows through the compensation capacitor C_m to the output. The first way to increase the g_{m1}/g_{mL} ratio is to search for a large g_{mL} .If the g_{mL} is large, then the small-signal output current is larger than the feedforward current and the effect of the RHP zero appears at very high frequencies. At this work we care about very high frequencies so the problem

still exists. As a consequence choosing a smaller g_{m1} is preferable. However there are some limitations when choosing the g_{m1} such as the bias current, which is related to the slew rate, and the size of the input differential pair. Moreover, if the size of the differential pair is relatively small, then there is the danger of having increased offset voltage at the output. All in all, a small g_{m1} cannot be obtained easily. In conclusion, according to the previous analysis, the RHP zero creates serious concerns regarding the stability of the amplifier. To deal with this problem, several methods can be employed such as the addition of a voltage buffer or a nulling resistor to the circuit. The presence of the nulling resistor at the circuit is a technique that will be studied later at this work.

2.3.3 Two-stage amplifier with Simple Miller Compensation with Nulling Resistor (SMCNR)

As mentioned above the feedforward small-signal current creates the RHP zero. One way to eliminate this zero is to increase the impedance seen at the capacitance path, and this can be done by inserting a resistor to the circuit. The resistor, called nulling resistor, is inserted next to the compensation capacitor as shown in Figure 21.

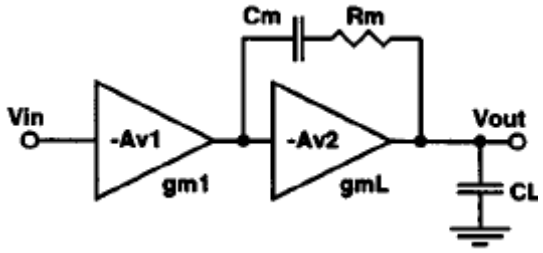


Fig.21 SMCNR amplifier

It is significant to notice that the addition of the resistor affects not only the frequency position of the RHP zero but also the position of the poles. Theoretically speaking, when the value of the nulling resistor reaches infinity, the compensation network is open-circuit and as a result no **pole-splitting** takes place. Pole-splitting will be explained afterwards in this chapter. In other words there are limits regarding both the minimum and the maximum value of the nulling resistor.

The transfer function of the SMNCR (R_m) amplifier is given by:

$$A_{v(SMCNR)}(s) = \frac{g_{m1}g_{mL}R_{o1}R_L[1+sC_m(R_m-\frac{1}{g_{mL}})]}{[1+sC_m(R_m+g_{mL}R_{o1}R_L)][1+s\frac{C_L(R_{o1}+R_m)R_L}{R_m+g_{mL}R_{o1}R_L}]} \quad \textbf{(2.13)}$$

The dominant pole is $p_{-3dB}=1/C_m$ (Rm $+g_{mL}R_{o1}R_L$), the non-dominant pole is $p_2= (R_m+g_{mL}R_{o1}R_L)/C_L$ ($R_{o1}+ R_{m)\ RL}$ and the zero is $z_1=1/C_m$ (Rm - $1/g_{mL}$).Later on, it will be proved that when $R_m=1/g_{mL}$ the RHP zero is completely eliminated. In that case, the circuit is in practice a SMC amplifier and the C_m and GBW are given by the equations (2.10) and (2.11) respectively. Moreover, as proven before, the value of the phase margin is about 63° because of the absence of the zero. However, when using a nulling resistor in design it is preferable to choose a value larger than $1/g_{mL}$ in order to transfer the zero to the left plane and in that way, increases the phase margin. Indeed, observing the transfer function (2.13), when the value of R_m is increased the position of the poles change as they move to lower frequencies. However we should be careful not to overpass the suggested value of R_m because there will be no pole-splitting effect. In other words, it is suggested that the value of R_m lies between $1/g_{mL}$ and (1/10) Ro1. The upper limit is set by the assumption that the value of R_m is negligible when determining the frequencies of p_{-3dB} and p_2 at the transfer function.

2.3.4 Pole-splitting and zero-cancellation

As mentioned before two important methods in order to utilize the frequency compensation are the pole-splitting and zero-cancellation methods. Studying an example will make it easier to understand not only the significance of the methods but also the way they work. Considering the circuit depicted in Figure 22, three poles p_x, p_E, p_A are identified at nodes X, E and A respectively.

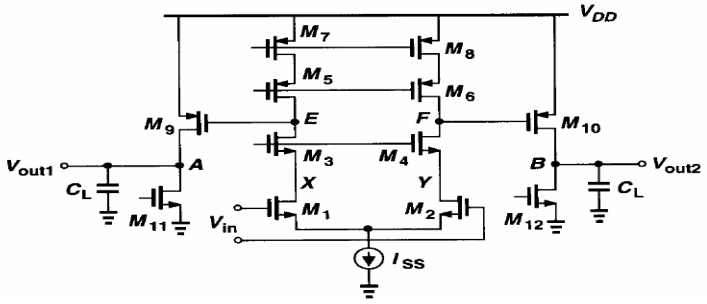


Fig.22 Two-stage opamp.

Nodes X and Y are the nodes at the sources of the differential pair transistors, so it is known [3] that their frequencies are relatively high. However, examining the rest two poles it will point out that both their frequencies lay near the origin pole. First of all, regarding the p_E this happens because the small-signal resistance seen at E is quite high, which means that M_3, M5 and M_9 are capable of creating a pole close to the origin one. On the other hand, the loading capacitance C_L is quite high at node A and this brings the same result. As a result there are two dominant poles.

Assuming that p_E is more dominant than p_A the magnitude and phase plots are constructed as shown below in Figure23.

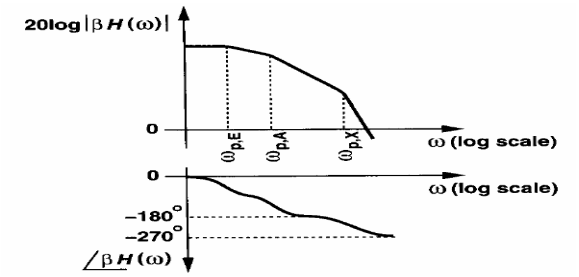


Fig.23 Bode plots of loop gain of two-stage op amp.

It can easily be observed that due to the existence of two dominant poles near the origin, the phase starts to drop quite rapidly after the second pole and before reaching the third. The question is what kind of frequency compensation should be applied to this case.

In Figure 23, one of the dominant poles must be moved toward the origin so as to place the gain crossover well below the phase crossover.However, it is a rule that, the unity-gain bandwidth cannot exceed the frequency of the second dominant pole[3].In case we decide to reduce the magnitude of p_E ,automatically we limit the bandwidth near the frequency of p_A, which is a small value, not to mention the fact that in order to achieve that we need a large capacitor, which means consuming odd space at the circuit's design.

An effective way to save a considerable amount of chip area is to use the Miller compensation technique. Shown in Figure 24 the initial circuit is a two-stage amplifier, which assumable the first stage exhibits high output impedance and the second adds a moderate gain, conditions which make the employment of the Miller theorem feasible.

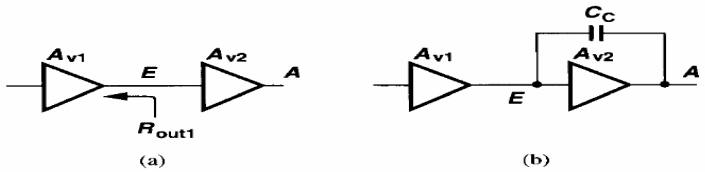


Fig.24 Miller compensation of a two-stage op amp

The goal is to create a large capacitance at node E, but using on the same time a capacitor of moderate size in order to save chip area. The capacitance that is created because of the Miller effect is $C_c(1+A_{v2})$ and the total capacitance at node E, which denotes the frequency of the respective pole, is $R_{out1}^{-1}[C_E + (1 + A_{v2})C_C]^{-1}$ where R_{out1} is the output resistance of the first stage and C_e the capacitance at node E before the addition of C_c. Besides improving the minimum chip area needed the Miller compensation moves the output pole away from the origin. This phenomenon shown in Figure 25 is called **pole-splitting.**

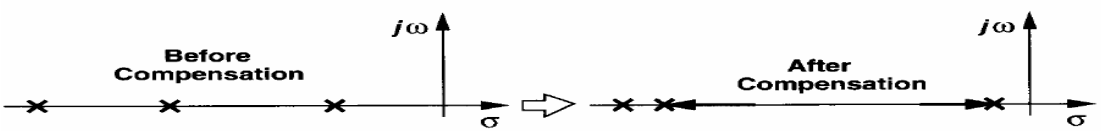


Fig.25 Pole splitting as a result of Miller compensation.

In simple words, the addition of the Miller capacitor moves the interstage pole towards the origin and the output pole in the different direction. This results in a far greater bandwidth compared to the occasion that a capacitance is interposed between a node and the ground.

However, during the previous analyses a serious fact was omitted: the presence of zeros in the transfer function. Whenever Miller compensation is applied, a RHP zero is created, as by doing that a parasitic path is formed from the input to the output. For instance, assuming that the frequency of the zero is ω_z, this is expressed at the numerator of the transfer function as $(1\text{-}s/\ \omega_z)$, producing a phase of $-\tan^{-1}(\omega/\ \omega_z)$. This is a negative value since ω_z is positive. In that way, like LHP poles, zeros increase the phase shift and move the phase crossover toward the origin. At the same time, a presence of a RHP zero slows down the magnitude curve positioning the gain crossover away from the origin. Combining the last two effects, it is easy to notice that the zero reduces the system's stability.

Figure 26 shows a simplified circuit of a two-stage opamp, and the RHP zero frequency ω_z is given by $g_m/\ (C_C + C_{GD})$ [3], where C_C is the Miller capacitance. Usually g_m has a small value so ω_z is affected at a large percent by the C_C, which occasionally has a relatively high value, in order to set the dominant pole properly.

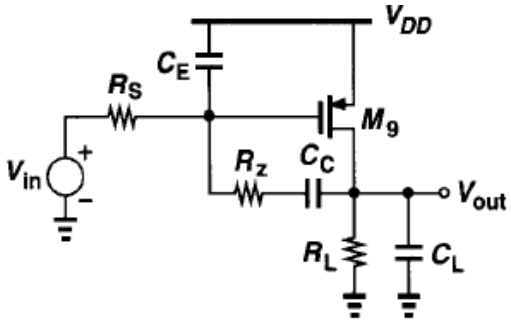


Fig.26 Simplified circuit of two-stage opamp, with the addition of R_z

In order to eliminate the zero R_z resistor is added in series with the compensation capacitor. This happens because the altered ω_z is calculated as

$$\omega_Z \approx \frac{1}{C_C(g_{m9}^{-1} - R_z)} \qquad \textbf{(2.14)}$$

One simple way to eliminate the zero would be to set $\omega_z=1/g_{m9}$. However, it is a design trend to set a R_z so that ω_z <0. A good reason to move the zero to the left half plane as a way to neutralize the first non-dominant pole, whose frequency is

$$\omega_{p2} = \frac{-g_{m9}}{C_L + C_E} \qquad \textbf{(2.15)}$$

Combining (2.14) and (2.15) and taking into consideration that C_E has typically a much smaller value than C_C, C_L:

$$R_Z \approx \frac{C_L + C_C}{g_{m9} C_C} \qquad \textbf{(2.16)}$$

Although canceling the first non-dominant pole is a quite attractive prospect, this method has two disadvantages. First of all, it is not easy to find the exact suitable value for R_z, according to 2.16 as C_L in most cases has a variable value since the output of the opamp for example may be an input to a higher level circuit. As a result the load capacitance changes. Moreover since R_z a significant value, in order to save space, is substituted by a transistor working in triode region. A random voltage swing may upset the frequency of the zero and in that way preventing it from canceling the non-dominant pole.

2.4 Gain Varying Techniques

Fundamentally, the gain of an amplifier depends on the equivalent transconductance Gm and the output impedance. In order to vary the gain, one of the two parameters needs to be varied. As a result, variable gain can be achieved by tuning bias current, emitter/source degeneration and/or loading. This section briefly introduces and compares these design techniques together with some other techniques that can be employed for variable gain amplifiers.

- **Variable Bias Current**

  The most direct way to tune the transconductance, which is highly related to the gain of the circuit, is by tuning the bias current. Although this is a simple technique, tuning the bias current lacks in versatility since noise, power, bandwidth, and linearity, which also depend heavily on it.

- **Variable Source Degeneration**

  Either using an emitter or source degeneration, another technique which enables the gain tuning is tuning the degeneration resistors, Figure 27. This is feasible if, a MOS transistor operating in its triode region as a variable resistor is employed. Its resistance is given by:

$$R = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{GS} - V_T)} \qquad \textbf{(2.17)}$$

  The differential pair performs better when given a low power supply because when is low power supplied, the degeneration does not impose penalty on voltage headroom due to bias V_{GS}-V_T. Nevertheless, the noise performance is poor.

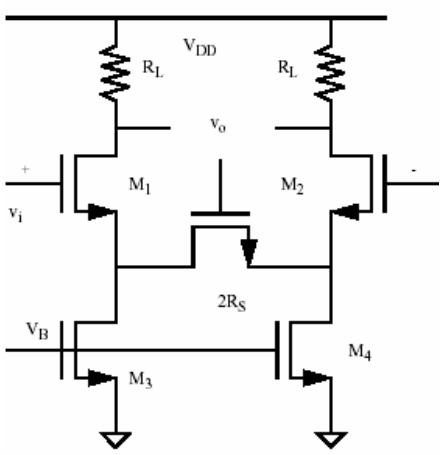


Fig.27 Variable gain amplifier with MOS as a variable degeneration resistor.

- **Variable Load**

  A technique that matches the variable bias current technique is the variable load tuning. By employing a MOS device operating in triode region, in parallel with R_D or substituting it, a variable load resistor is created. Although simple, this techniques main drawback is that it suffers from the severe trade-off of the amplifier's performance in terms of noise, linearity and bandwidth. The variable load technique is occupied in the main block of this thesis.

- **Current Steering**

Another interesting technique, referred to as current steering, can be employed to realize a variable-gain amplifier. The simplified schematic is shown in Figure 28. Transistors M1-M4 are to steer the differential drain current of M5-M6 to the output according to the control voltage VC in relation to a reference voltage Vr.

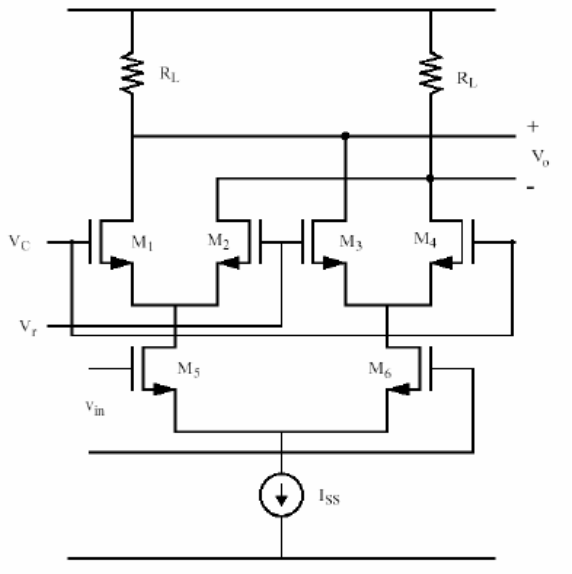


Fig.28 Variable gain amplifier based on current steering technique.

The overall gain is given by:

$$A_V = (2a-1)g_{m5}R_L \qquad \textbf{(2.18)}$$

where α is the fraction of the drain current from M5 flowing through M1 to the output[6]

$$0 < a = \frac{i_{d1}}{i_{d4}} = f(V_C, V_T) < 1 \qquad \textbf{(2.19)}$$

The key advantage of this current-steering technique is that the amplifier's parameters, including bias current, noise, bandwidth and linearity, are all independent of the control voltage and thus the gain setting. The disadvantages include more active devices and thus more noise and more voltage headroom, which may not be suitable for low-voltage and high-swing applications. It is interesting to note that the transistors M1-M4 do not need to cross couple from each other. In this case, the voltage gain becomes:

$$A_V = ag_{m5}R_L \qquad \textbf{(2.20)}$$

When having low supply voltage, it is more beneficial to steer the currents from M2 and M3 directly to the supply without cross-coupling to the load. As such, the current and the voltage drop across the load can be minimized, and the load can be maximized for maximum gain without sacrificing the dc output and the output swing. Generally, in order to make the gain less sensitive to process variation and temperature, it may prove to be significant employing resistive loads and resistive regeneration for the input devices M5 and M6.Apart from that, degeneration improves linearity at a cost of gain reduction. The range of the control voltage may be limited for a linear gain control, and a scaling network can be added right after the actual control voltage to extend it to a full supply range. Moreover, resistive degeneration can be applied to the steering devices M1-M4 as to make the gain's dependency on control voltage more linear.

2.5 Harmonic Distortion and DC Offset

2.5.1 Harmonic Distortion

In communication systems, linearity of amplifiers is normally measured by evaluating the third order input intercept point (IIP3). Due to the inherent non-linearity of amplifiers, an input signal *x(t)* results in an output as given below:

$$y(t) = k_0 + k_1 x(t) + k_2 x^2(t) + k_3 x^3(t) \qquad \textbf{(2.21).}$$

The above relation is based on the assumption that the circuit is without memory and is driven by a small signal excitation reasonably below the 1 dB compression point (1 dB compression point is the point at which the gain deviates from its ideal small signal value by 1dB). It follows from equation (2.21) that when the input signal is of the form $x(t) = x\cos(\omega_1 t) + x\cos(\omega_2 t)$, the in-band output of interest is [7]:

$$y_{in-band}(t) = k_1 x[\cos(\omega_1 t) + \cos(\omega_2 t)] + \frac{k_3}{4} x^3 \begin{Bmatrix} 9\cos(\omega_1 t) + 9\cos(\omega_2 t) + \\ 3[\cos(2\omega_2 - \omega_1)t + \cos(2\omega_1 - \omega_2)t] \end{Bmatrix} \textbf{(2.22)}$$

It can be observed from the above equation that the third order distortion components include nine new mixing products at ω_1 and ω_2 and three at frequencies $2\omega_1$-ω_2 and $2\omega_2$- ω_1. The components at $2\omega_1$-ω_2 and $2\omega_2$-ω_1 are the intermodulation distortion components.

The fundamental component in equation (2.22) increases with a slope of 1dB/dB, while the third order intermodulation component rises at a rate of 3dB/dB with respect to the input power. The third order input intercept point is defined as the input power for which the distortion power at $2\omega_1$-ω_2 (or $2\omega_2$-ω_1) is the same as the linear output

power at ω_1 (or ω_2). Normalized to a 1Ω load resistance, the IIP3 is given by:

$$X_{IIP3}^2 = \frac{4k_1}{3k_3} \qquad \textbf{(2.23)}$$

2.5.2 DC Offset

There are two types of offsets in analog circuits that affect the performance of the circuits:

1. Random offset
2. Systematic offset

Systematic offset is caused by non-idealities of the circuit, on condition that there is no transistor dimension mismatch. For instance, V_{TH} variation causes further variation to overdrive voltages resulting in mismatches difficult to predict, random mismatches, leading to DC-Offset. As a consequence, the input offset voltage is the differential input voltage that has to be applied to force the differential output to zero is called DC-Offset voltage. Furthermore in multistage amplifiers, each stage providing a significant amount of gain, the DC-Offset is often caused by the first stage [8] and this is the reason it should be optimally designed.

2.5.2.1 Systematic Offset

Systematic offset voltage is closely related to the DC power supply rejection ratio of amplifiers. Its dependence on the supply voltage is a more realistic problem in circuits in which the bias currents depend on the supply voltage. In the two stage amplifier shown in Figure 29, the two stages have been disconnected to explain the concept of input referred DC offset.

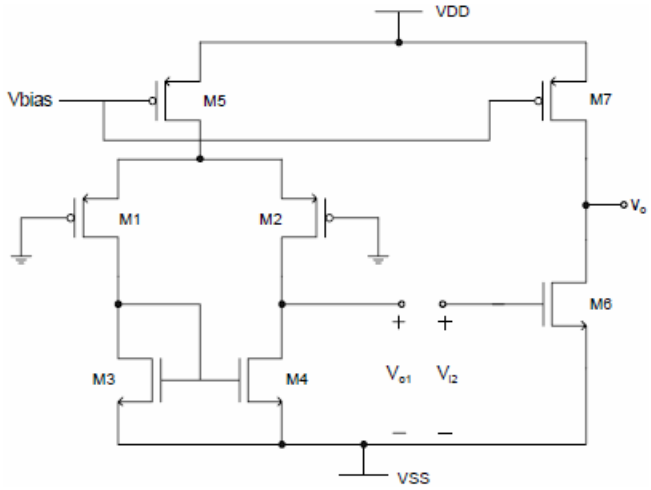


Fig.29 Input referred offset of a two stage amplifier

If the input voltages are set to zero and perfect matching is assumed, the V_{DS} of M_3 (also equal to its V_{GS}) will be equal to the V_{DS} of M_4. Then, $V_{DS1} = V_{DS2}$ and $I_1 = I_2 = I_{SS}/2$. Since M_3, M_4 and M6 are perfectly matched and $V_{GS3} = V_{DS4} = V_{GS6}$, the overdrive voltages of all three transistors are the same. Hence the ratio of their currents to W/L values should also be the same. Therefore:

$$\frac{I_{D3}}{(W/L)_3} = \frac{I_{D4}}{(W/L)_4} = \frac{I_{D6}}{(W/L)_6} \qquad \textbf{(2.24)}$$

$$\Rightarrow \frac{I_{D5}}{2(W/L)_3} = \frac{I_{D5}}{2(W/L)_4} = \frac{I_{D6}}{(W/L)_6} \qquad \textbf{(2.25)}$$

Since

$$\frac{I_{D5}}{I_{D7}} = \frac{(W/L)_5}{(W/L)_7}; \qquad I_{D6} = I_{D7}, \qquad \textbf{(2.26)}$$

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{1}{2}\frac{(W/L)_5}{(W/L)_7} \qquad \textbf{(2.27)}$$

The output DC voltage is given by:

$$V_{0,DC}=V_{DS6}-V_{ss}=V_{GS3}-V_{ss}=V_{T3}+V_{o3}-V_{ss} \qquad \textbf{(2.28)}$$

The systematic offset is obtained by calculating the difference between the value of $V_{0,DC}$ in equation (2.28) and the half value of the supply voltage. Provided that A_v is the gain of the opamp then

$$V_{OFFSET(SYS)} = \frac{V_{T3} + V_{ov3} + V_{ss} - \frac{V_{DD} - V_{ss}}{2}}{A_v} \quad \textbf{(2.29)}$$

2.5.2.2 Random offset voltage

Random offset can be met when process variations exist. This could be translated into a load mismatch, irrelevantly of active or passive amplifier channel length and width mismatches between transistors, threshold voltage mismatch and many other such variations. A constant offset component, independent of the bias current, is caused by a mismatch in the V_{TH} , which results into non-linearity and high presence of noise. At the physical design of the circuit these facts should be taken into serious consideration.

2.5.2.3 DC Offset Generation

In this section DC-Offset generation mechanism are summarized [10,11] :

1. Transistor mismatches in the signal path.

2. Self-mixing of local oscillator (LO) signals leaking into the RF port of the mixer and the input port of the LNA as shown in Figure 30.

3. Self-mixing of LO signals leaking into, radiated from, and reflected back to the antenna as shown in Figure 31.

4. Self-mixing of strong in-band interferers leaking into the LO port of the mixer from the output of the LNA as shown in Figure 32.

5. second-order intermodulation (IM2) of the components such as LNAs, mixers, and filters.

Though only the *I*-branch is shown in the above figures, the Q-branch undergoes the same phenomenon. The DC offsets generated by the mechanism 1 and 2 can be considered as systematic whereas those by the mechanism 3 and 4 as random.

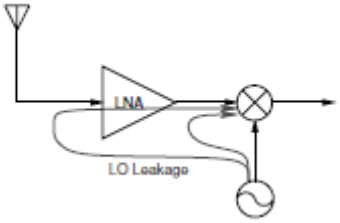


Fig.30 Self-mixing due to LO leakage

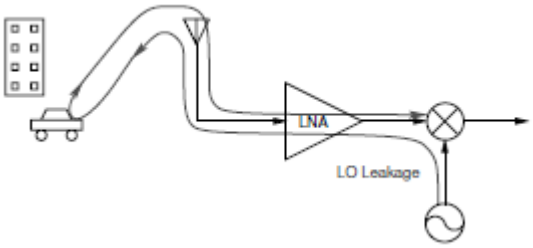


Fig.31 Self-mixing due to LO leakage radiated

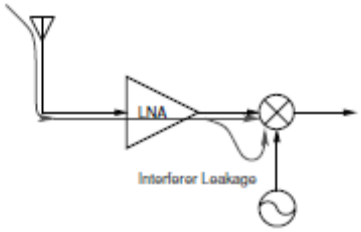


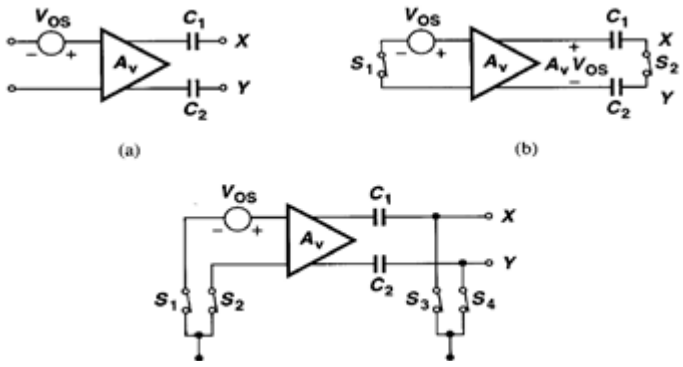
Fig.32 Self-mixing due to interferer leakage

2.5.3 DC Offset Correction

DC offset causes performance degradation in signal processing systems especially for high-speed applications. The offset cancellation method that is presented in this thesis relaxes the requirement for the offset and is based on the negative feedback topology.

2.5.3.1 Feedback Topologies

It is widely known the tradeoff between the threshold voltage mismatch and the channel capacitance. For instance, a threshold mismatch of 1 mV equals roughly to 300 fF, taking into consideration that the technology we use is 0.6 μm. There are cases, where input capacitance's value becomes quite large, and this fact causes both the decrease of the speed and higher levels of power dissipation. The most common case of the phenomenon mentioned above is the multistage topologies. Considering the fact that in practice mechanical stress may increase the offsets mentioned above, in modern systems precision is an essential factor, so we have to cut down these offsets with offset cancelation techniques that are presented below.
A common method to deal with the offset is to use capacitors in our circuit. The way we place the capacitors defines the cancellation method we deploy. First of all, we consider the case of placing the capacitors in front of our amplifier, as shown in Figure 33(a) [3].



(c)

Fig.33 (a)Simple amplifier with capacitive coupling at output, (b) circuit of (a)with its inputs and outputs shorted, (c) proper setting of the common-mode level during offset cancellation.

If the inputs of the amplifier are shorted Figure 33(b) then the output of the amplifier will be $V_{out} = A_v V_{os}$ and is stored across C_1 andC_2.We must agree that, a zero differential input results in a zero difference between V_x and V_y. Thus, after S_1 and S_2 turn off, the circuit consisting of the amplifier and C_1 and C_2 exhibits a zero offset voltage, amplifying only changes in the differential input voltage. In practice, the inputs and outputs must be shorted to proper common-mode voltages Figure 33(c) .As a result this method senses the offset by setting the differential input to zero and then stores the result to the capacitors that are placed at the front of the amplifier. However the drawback of this method is that the existence of a clock is inevitable as we need to settle the offset cancelation period Figure 34.

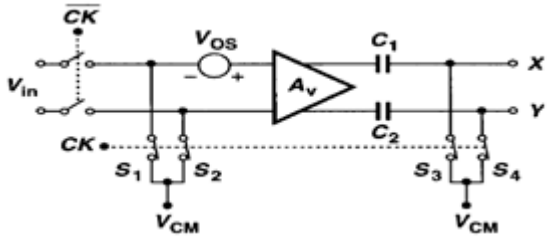


Fig.34 Control of the amplification and offset cancellation modes by a clock.

The next method is called input offset storage and as its name implies the capacitors are placed before the amplifier. Plus a unity-gain negative-feedback loop is employed Figure 35(a).

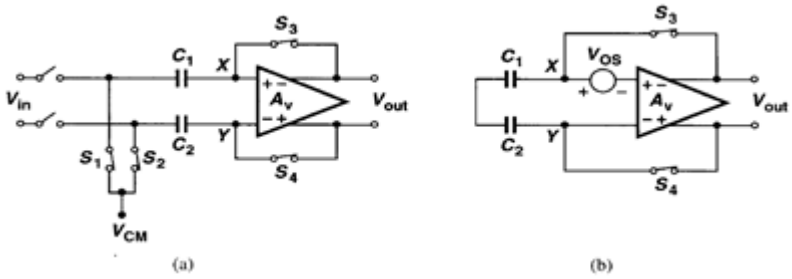


Fig35 (a) Input offset storage, (b) circuit of (a) in the offset cancellation mode.

Considering that offset exists in our circuit, the first circuit can be simplified to the one depicted in Figure 35 (b).It can be seen that V_{out}=V_{xy} and (V_{out}-V_{os}) (-A_v) =V_{out} as

$$V_{out_t} = \frac{A_v}{1+A_v} V_{OS} \approx V_{OS} \quad \textbf{(2.30)}$$

In other words, because of the negative feedback loop, the offset seen at the nodes X and Y is transferred and stored at the capacitors, where it is subtracted from the differential value of V_{out}.In case we have for a zero differential input, the differential output is equal to V_{OS}.

The disadvantage of the two previous methods is that they suggest the use of capacitors in the signal path and this affects seriously the magnitude of the circuit's poles, especially when feedback loops or opamps are used. Changing the magnitude of the poles affects the phase margin at a large extent and as a result the speed of the circuit and the power dissipation. In order to get over these problems we must protect the signal path from the capacitors used for offset cancelation and this can be achieved by using an auxiliary amplifier Figure 36.

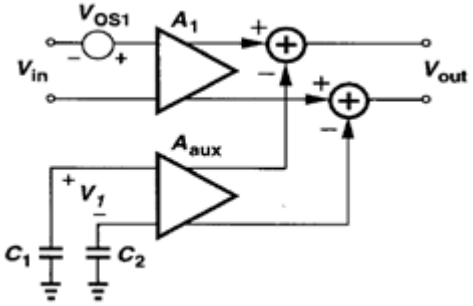


Fig.36 Additional of an auxiliary stage to remove the offset of an amplifier.

A_{aux} amplifies the differential signal V_1 and then adds it to the output of A_1 (subtraction).Supposing that $V_{OS1}A_1 = V_1 A_{aux}$ then for V_{in}=0 we receive V_{out}=0.The main question is how do we create the differential signal V_1 and this is explained by the following circuit in Figure 37.

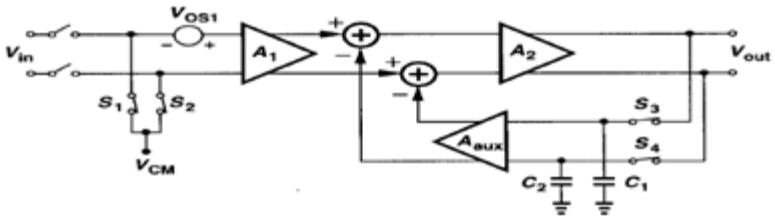


Fig.37 Auxiliary amplifier placed in a feedback loop during offset cancellation.

To cut a long story short the use of an extra stage is inevitable, as it has to serve the loop that is created by the auxiliary amplifier. In other words this method is proposed mainly for multistage amplifiers. By examining the circuit it can be noticed that S_1 and S_2 are on then $V_{out}=V_{OS1}A_1A_2$.
Turning on the S_3 and S_4 we activate the negative feedback loop and we receive

$$V_{out}' = \frac{V_{out}A_{aux}}{V_{OS1}A_1} \qquad \textbf{(2.31)}$$

and considering that ($V_{OS1}A_1/A_{aux})A_{aux} = V_{OS1}A_1$ the value kept in the capacitors is V_1.However, there are two disadvantages regarding this topology. First of all, it is obligatory to use a multistage topology, a fact that may be an obstacle in case of the design of high speed operational amplifiers. Secondly, the addition of the output voltages of A_1 and A_2 is quite difficult. To deal with the above issues at a certain extent some modifications are made to the initial circuit resulting to the one depicted in Figure 38.

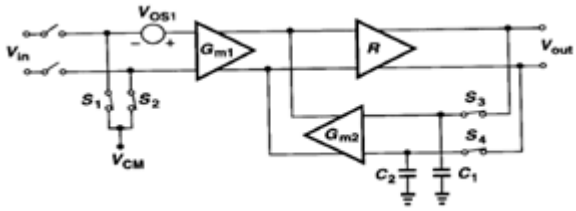


Fig.38 Previous Circuit using G_m and R stages

The new circuit is consisted of G_{m1} and G_{m2} which are stages that comprise a differential pair and R which is a transimpedance amplifier. Figure 39 shows a simple implementation of a common-gate circuit which serves as a transimpedance amplifier, which means that it converts the current source to voltage at the drain.

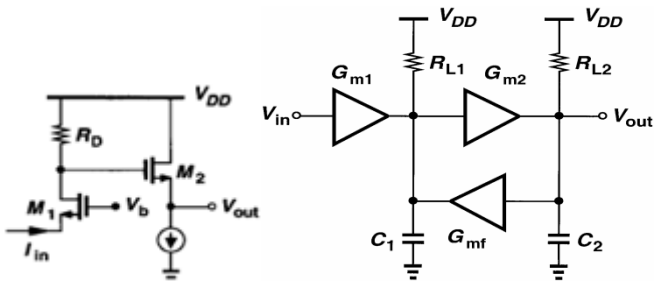


Fig.39 Transimpedance amplifier

2.5.3.2 Active Feedback Architecture

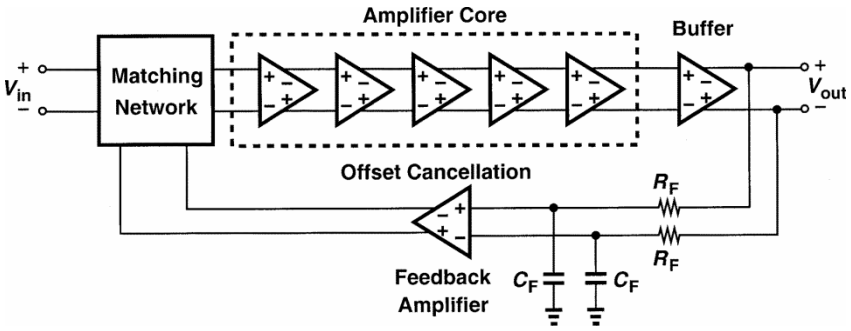


Fig.40 Active Feedback Architecture

Before studying the active feedback architecture of Figure 40 it must be noticed that the specific methodology not only helps us in DC-offset correction but also improves the gain-bandwidth of our circuit. Taking into consideration the Figure 40 which depicts the architecture employed at a multistage amplifier it must be noticed that a cascade of n identical cells, each having a BW_c, produces a total bandwidth of

$$BW_{tot} = BW_c \sqrt[m]{2^{1/n} - 1} \qquad \textbf{(2.32)}$$

Symbol m equals to 2 for first-order stages and 4 for second-order stages.[12] For example, if BW_{tot}= 10 GHz and n=5 then BW_c >26 GHz for m=2 and BW_c >16 GHz for m=4. This is a very helpful information concerning the required bandwidth of each identical cell. As far as gain is concerned,if A_{tot} is the total gain then the required cell gain-bandwidth product GBW_c can be written as [12]

$$GBW_c = \frac{GBW_{tot}}{A_{tot}^{1-1/n}\sqrt[m]{2^{1/n}-1}} \qquad \textbf{(2.33)}$$

where $GBW_{tot}= A_{tot}BW_{tot}$ and $GBW_c=A_{tot}^{1/n}BW_c$.It can be concluded that for a large n and a given GBW_{tot} the gain per stage gets lower and the existence of noise becomes more intense.

Taking into consideration the above data, it is important to study how the active negative feedback loop enhances the GBW of amplifiers. As it was mentioned before the negative feedback loop involves two stages G_{m1}- G_{m2} and a transconductance stage G_{mf} which returns a fraction of the output to the input of G_{m2}. Unlike the conventional Cherry-Hooper amplifier, actived feedback does not resistively load the transimpedance stage.

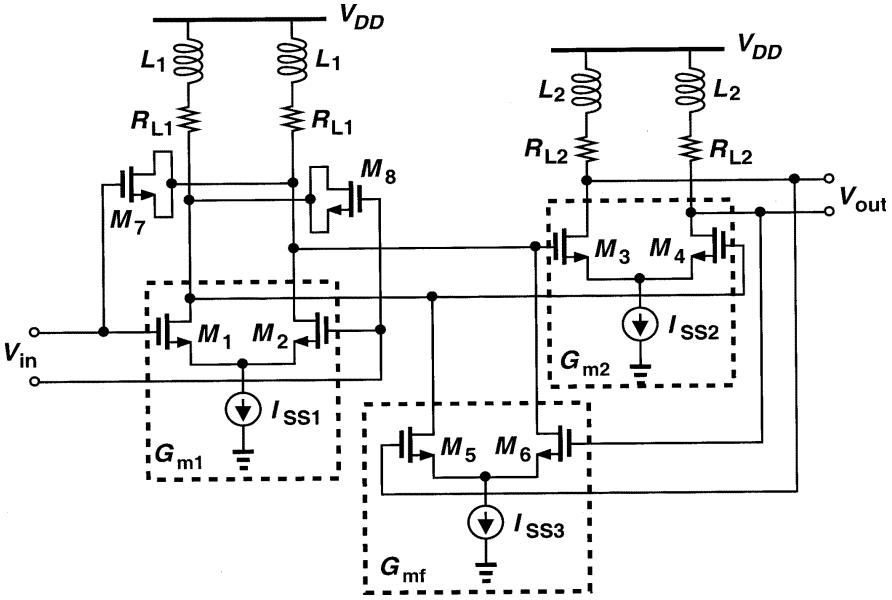


Fig.41 Active-feedback cell realization

If we study Figure 41 the transfer function of the overall amplifier is given by

$$\frac{V_{out}}{V_{in}} = \frac{A_{vo}\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \textbf{(2.34)}$$

where

$$A_{vo} = \frac{G_{m1}G_{m2}R_{L1}R_{L2}}{1+G_{mf}G_{m2}R_{L1}R_{L2}} \approx \frac{G_{m1}}{G_{mf}} \qquad \textbf{(2.35)}$$

$$\zeta = \frac{1}{2}\frac{R_{L1}C_1 + R_{L2}C_2}{2\sqrt{R_{L1}R_{L2}C_1C_2(1+G_{mf}G_{m2}R_{L1}R_{L2})}} \qquad \textbf{(2.36)}$$

$$\omega_n^2 = \frac{1 + G_{mf} G_{m2} R_{L1} R_{L2}}{R_{L1} R_{L2} C_1 C_2} \qquad \textbf{(2.37)}$$

If $\zeta=\sqrt{2}/2$ and the -3_dB bandwidth $\omega_{-3db}=2\pi f_{-3db}=\omega_n/(2\pi)$ then we receive the maximally-flat Butterworth response. If multiplied

$$A_{vo}\omega_{-3dB}^2 = \frac{G_{m1}G_{m2}}{C_1 C_2} \qquad \textbf{(2.38)}$$

or

$$A_{vo}\omega_{-3dB} = \frac{G_{m1}G_{m2}}{C_1 C_2}\frac{1}{\omega_{-3dB}} \qquad \textbf{(2.39)}$$

Assuming that $G_{m1}/C_1 \approx G_{m2}/C_2 \approx 2\pi f_T$ the equation above can be rewritten as

$$A_{vo}\omega_{-3dB} = f_T \frac{f_T}{f_{-3dB}} \quad . \qquad \textbf{(2.40)}$$

Noticing the above result it can be concluded that the active feedback increases the GBW beyond the technology f_T by a factor equal to the ratio of f_T and the cell bandwidth.

CHAPTER 3

DESIGN OF THE VARIABLE GAIN AMPLIFIER

The variable gain amplifier that will be presented in this chapter was designed, according to the demanding standards of a RF receiver, which combine not only high bandwidth but also considerable gain.Moreover, this amplifier has low power dissipation and DC offset correction. The VGA system architecture is shown in Figure 42.

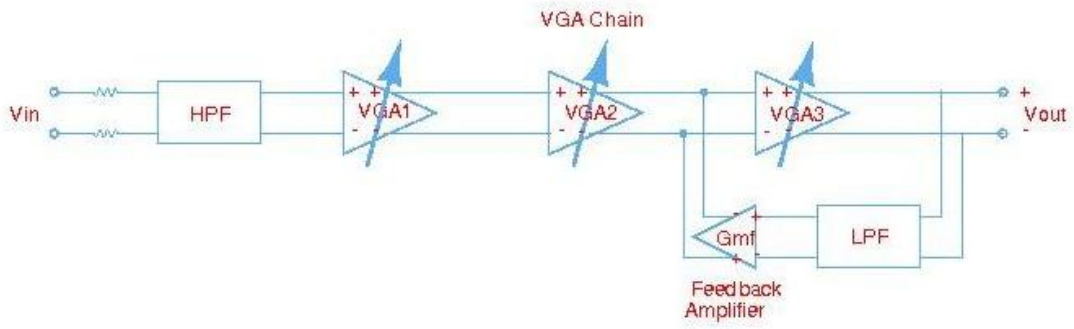


Fig.42 VGA Architecture

The VGA consists of a high pass filter, a three-stage modified Cherry Hooper amplifier gain cell and a DC-offset cancelation network, comprised by a low-pass filter and a feedback amplifier. Besides that, specific techniques are employed including the inverse scaling and the negative feedback network, as an attempt to cancel the DC-offset. Furthermore, it is important to notice that the current amplifier is inductorless, since the on-chip gain peaking inductor may extends the maximum bandwidth, it requires a large chip area though [13].Of course, using capacitors for compensation is something inevitable. As a result, in the next section each block of the VGA will be explained along its purpose.

3.1 Blocks of the VGA

3.1.1 High-pass filter

The high-pass filter is a simple first order RC filter[14], which is used in order to block the offsets from preceding stages, such as self-mixing offsets created from the LNA, Mixer and LO as shown in Figure 1.Plus it provides the desired input dc level for the input stage of the VGA gain cell. The HPF is used in feedforward in order to remove the DC-offset because the DC voltage cannot pass through a HPF, if it is placed in the signal path. However it should be decided the proportion of the input signal that will be degraded since the HPF does that. Given that the system designed has a bandwidth of around 2GHz, a filter with a cut-off frequency of 200KHz will not do much harm and the settling time will be relatively fast. As a result in order to implement that, a 1.6 MΩ resistor and 0.5pF capacitance are used, as shown in Figure 43.

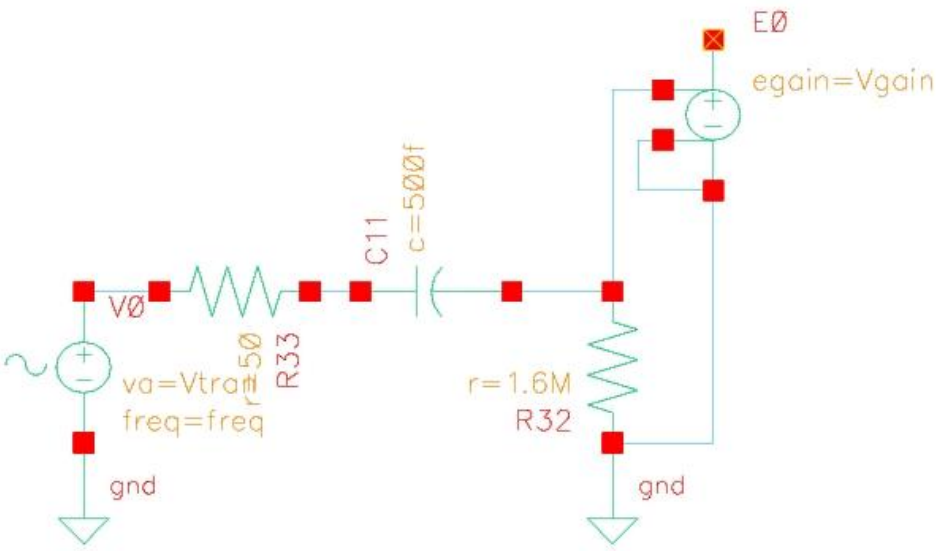


Fig.43 HPF with 50Ω resistance at transmission line and a source follower

First of all the 50Ω resistance is noticed before the filter and after the input of the system. Theoretically there is another stage that precedes the VGA and shares the same transmission line. However standing waves on transmission lines can cause gain/phase ripples. For that reason transmission lines must either be of short length or well-terminated. Since the design takes place at 90nm technology, and the transistors have small dimensions, a 50 Ω resistance would be enough to terminate the lines between two stages. Finally the use of a source follower who acts as a voltage buffer is inevitable. The gates of the differential pair theoretically have infinite input resistance and by placing the HPF we interpose a resistance with a small finite value. This results in degrading the signal and the voltage buffer is needed, with gain value 1(0dB), to keep the signal steady. The source follower was practiced using an ideal

voltage-source voltage control buffer, from the analogLib of ***Cadence Analog Design Environment***. Below lie the frequency response of the HPF, Figure 44, and the values used in the design of it, Table 1.

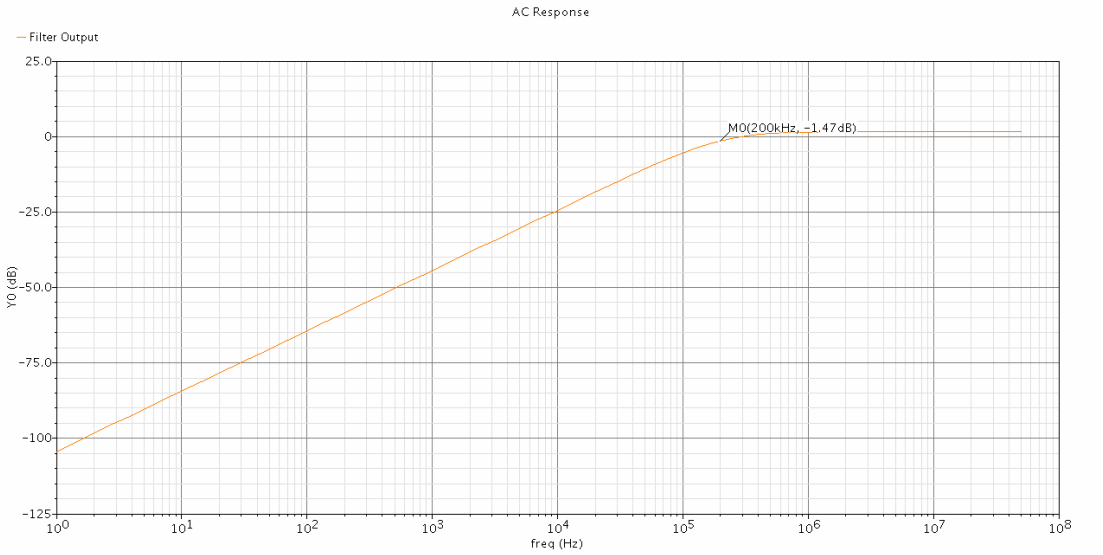


Fig.44 Frequency Response of the HPF with 200KHz cut-off frequency

Table 1. HPF design values

Block	**HPF**
Values	
R	**1.6MΩ**
C	**0.5pF**

3.1.2 VGA Chain

The three-stage VGA chain provides wide gain tuning range, having not only sufficient voltage gain for small signal inputs but also attenuation gain when strong level signals can cause saturation to the system. In that way it assures that the demodulator get an input signal that is within the input range of the demodulator. The main VGA gain cell is a modified Cherry-Hooper amplifier[15], however in order to understand its functionality, the primal Cherry Hooper amplifier should be studied first.

3.1.2.1 Cherry Hooper amplifier

One of the main purposes for using the Cherry Hooper amplifier, Figure 45, is that it provides high gain bandwidth product without the need of extra supply voltage or chip area needed for inductively peaked gain stages which use active or passive inductors. One characteristic feature of the Cherry-Hooper amplifier is that it uses local feedback at the drain network in order to improve speed. However in order to understand better its functionality it would be wise to study the cascade of common-source stages topology, as shown in Figure 46(a)[15].

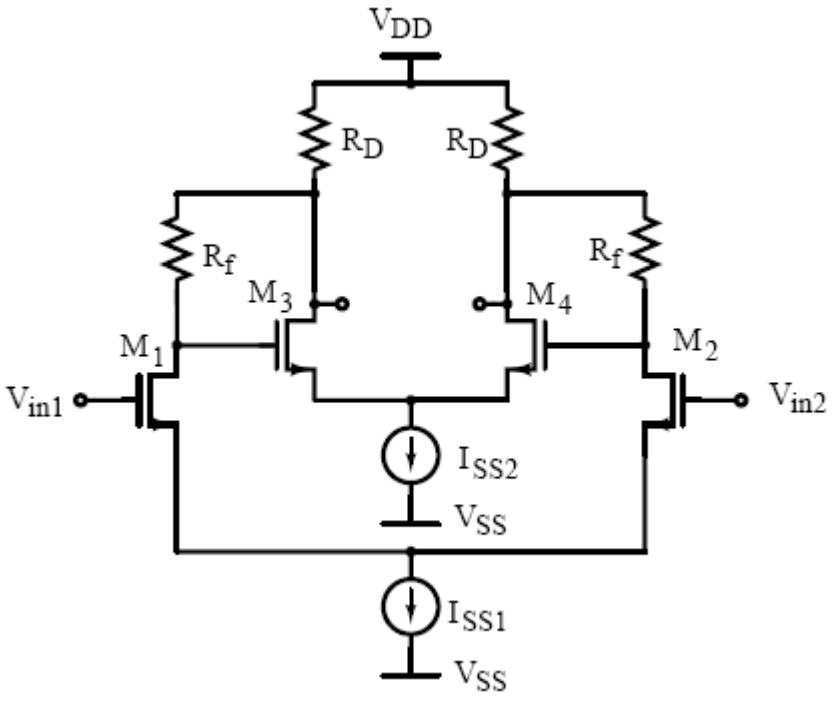


Fig.45 Cherry Hooper amplifier

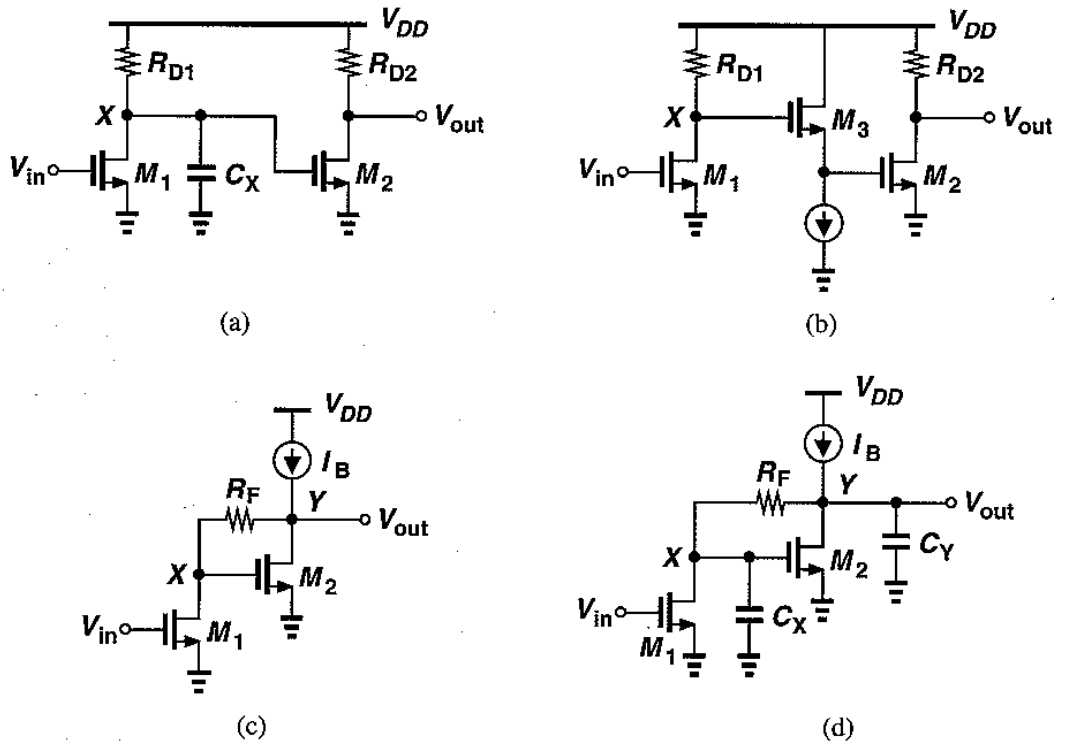


Fig.46 (a) Cascade of two CS stages,(b) Employment of a source follower voltage buffer,(c)Two CS stages with feedback resistance, (d) previous circuit with node capacitances.

C_X is the total capacitance seen from node X to ground. The trade-off between gain and bandwidth of the first stage is something easy to notice, since $A_v=g_{m1}R_D$ and $\omega_{p,X}=(R_{D1}C_x)^{-1}$.The size of transistor M_2 affects the gain of the second stage and a result the C_{GS2} and C_{GD2}(enhanced by the Miller effect)may dangerously limit the bandwidth at node X.

If a source follower, between the two stages, is interposed, as shown in Figure 46(b), diminishing the input capacitance of the second CS stage from the node X. However, in that way the voltage gain will be reduced since the source follower requires more voltage headroom, limiting the available bias voltage across the resistor R_{D1} , reducing as a result the voltage gain.Moreover, there is a chance that the signal may be attenuated, in some cases as much as a factor of 50%, if body effect and channel-length modulation are significant.

Searching an alternative solution, the topology of Figure 46(c) should be considered. At this case resistor R_F poses feedback around M_2 ,since it senses the output voltage and returns a proportional current to X. It should be noticed that the circuit provides two paths to the output, the first through M_2 and the second through R_F. The goal is to make the signal, flowing through R_F, negligible so as not to interact with the signal flowing through M_2.

At this point isolating a CS stage with resistive feedback, Figure 47, in order to examine its behavior would help. Supposing that the resistance R_G has a large value, I_D will flow through the transistor and not through the resistive path. As a result, since I_G=0 then

$$V_{GS}=V_{DS}=V_{DD}-I_DR_D \quad \textbf{(3.1)}$$

or

$$V_{DD}= V_{GS} + I_DR_D \quad \textbf{(3.2)}$$

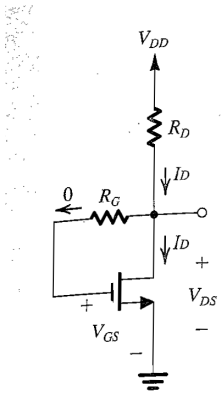


Fig.47 CS stage with resistive feedback

It can be proved that the R_G role is to keep the value of I_D constant. Assuming that the value of I_D is not fixed and is increased. According to (3.2) the value of V_{GS} should be decreased, since V_{DD} and R_D have stable value. However if there is decrease in V_{GS} ,according to the MOS device physics, I_D will decrease too. All in all the assumption was wrong and that proves that the value of I_D is stable.

Calculating the low-frequency voltage gain of the circuit in Figure 46(c)(assuming that I_B is an ideal current source and channel-length modulation is minor), the small-signal drain current of M_1 is $g_{m1}V_{in}$ .This current flows through R_F creating a voltage drop equal to $g_{m1}V_{in}R_F$. According to KVL:

$$V_{out}=V_x + g_{m1}V_{in}R_F \quad \textbf{(3.3)}$$

At the same time, the small signal current created by M_2 ,$g_{m2}V_X$, must flow through R_F resulting in:

$$g_{m2}V_{X=-}\ g_{m1}V_{in} \quad \textbf{(3.4)}$$

using (3.3) $$g_{m2}(V_{out}\text{-}g_{m1}V_{in}\,R_F)= -\ g_{m1}V_{in} \quad \textbf{(3.5)}$$

leading to $$\frac{V_{out}}{V_{in}} = g_{m1}R_F - \frac{g_{m1}}{g_{m2}} \quad \textbf{(3.6)}$$

If $R_F >> g_{m2}^{-1}$ then the gain equals to the one of a simple CS stage with a load resistance R_F. The main advantage of this circuit compared to the ones studied before, is that the small-signal resistance seen at nodes X and Y, has the value g_{m2} much smaller than R_F .Moreover comparing the pole frequencies created by the capacitances at nodes X and Y of Figure46(d) with the ones of Figures 46(a) and 46(b), we conclude that they have quite much higher values since $\omega_{p,X} \approx g_{m2}/C_X$ and $\omega_{p,Y} \approx g_{m2}/C_Y$ .For example, assuming that $C_x=C_{GS2}$ then the pole frequency would be $\omega_{p,X} \approx g_{m2}/C_{GS2}=2\pi f_{T2}$,where f_{T2} is the unity current gain frequency of transistor M_2. As a result, the final circuit not only provides a high gain of approximately $g_{m1}R_F$ but also low resistance values at nodes X,Y which in turn produce high-frequency poles as explained before. This is the basic circuit for the Cherry Hooper amplifier. At this work a modification of Cherry Hooper Initial circuit will be presented. However it would be wise to study a modification that approaches the one of this work in order to understand it better.

The previous approach was based on the assumption that $\omega_{p,X} \approx g_{m2}/C_X$ and $\omega_{p,Y} \approx g_{m2}/C_Y$,though these approximations may prove to be inaccurate. This happens, because at high frequencies, a feature of this work, C_Y *shunts* the output node. This means that a low-resistance connection is formed between 2 points in the electrical circuit, creating an alternative path for a portion of the current. In that way the impedance seen at the gate of transistor M2 increases and the loop gain is decreased. Same happens with the capacitance C_x shunting the node X. Noticing the equivalent circuit of Figure 48,

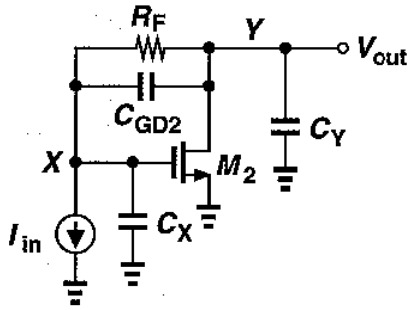


Fig.48 Equivalent circuit of the Cherry Hooper amplifier

where $I_{in}=g_{m1}V_{in}$, the current flowing through $R_f||C_{GD2}$,$I_{in}+V_XC_Xs$, produces a voltage drop equal to $(I_{in}+V_XC_Xs)R_F/(R_FC_{GD2}s+1)$.It can be seen that

$$(I_{in} + V_X C_X s)\frac{R_F}{R_F C_{GD2} s + 1} + V_X = V_{out} \quad \textbf{(3.7)}$$

On the same time summing the currents at the output:

$$-V_{out}C_Y s - g_{m2}V_X = I_{in} + V_X C_X s \quad \textbf{(3.8)},$$

leading to:

$$V_X = \frac{-V_{out}C_Y s - I_{in}}{g_{m2} + C_X s} \quad \textbf{(3.9),}$$

substituting in (3.7):

$$\frac{V_{out}}{V_{in}} = \frac{R_F^2 C_X C_{GD2} s^2 + (g_{m2}R_F C_{GD2} + C_X - C_{GD2})R_F s + g_{m2}R_F - 1}{R_F(C_X C_Y + C_{GD2}C_Y + C_{GD2}C_X)s^2 + (C_Y + g_{m2}R_F C_{GD2} + C_X)s + g_{m2}} \quad \textbf{(3.10),}$$

Supposing that the two poles are equal then, according to [5],

$$\omega_{p1} = \omega_{p2} = \frac{2g_{m2}}{C_X + C_Y + g_{m2}R_F C_{GD2}} \approx \frac{2g_{m2}}{C_X + C_Y} \quad \textbf{(3.11),}$$

simplified in case the third term in the denominator has a negligible value. What is most important is the fact that ω_{p1} and ω_{p2} have quite high values: $(R_F C_X)^{-1}$ or $(R_F C_Y)^{-1}$.

The differential version of the Cherry Hooper amplifier is depicted in Figure49(a) and in order to save the unwanted capacitance possibly added by a pnp current source, ideal current sources are replaced by resistors. The transistors M_1 and M_2 form the input pair which is also known as the transconductance stage that converts input voltage into current. The resistor R_F provides feedback between the drain and gate of the transistors M_3 and M_4 respectively. The current mode signal is then amplified and converted back to voltage by the second pair of transistors M_3 and M_4 , which form the transimpedance stage.

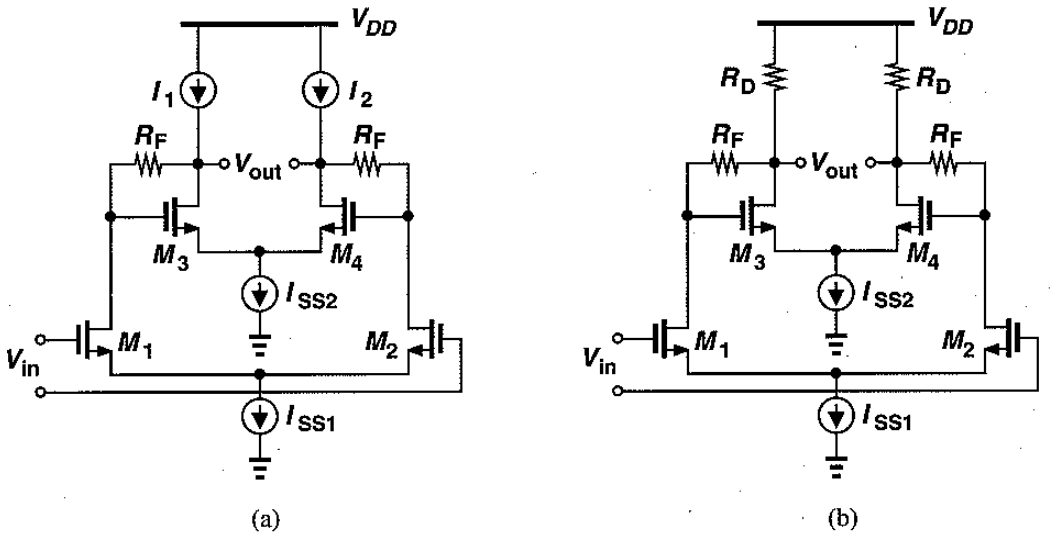


Fig.49 Cherry Hooper amplifier with differential pair with (a)current-source loads and (b)resistive loads.

However Cherry Hooper amplifier has a serious drawback, it allows limited voltage headroom since it face difficulties in working at low voltages, such as 90nm.Examining the circuit in Figure49(b) ,it can be seen that I_{ss1} forces its way to the feedback resistors while the sum $I_{ss1} + I_{ss2}$ through the load resistors. As a result the minimum supply voltage is given by

$$V_{DD,\min} = \frac{(I_{ss1} + I_{ss2})}{2} R_D + \frac{I_{ss1}}{2} R_F + V_{GS3,4} + V_{ISS2} \qquad \textbf{(3.12).}$$

V_{ISS2} is the minimum voltage required across ideal current source I_{SS2} and it can clearly be seen that it affects the maximum voltage gain of the circuit. In order to improve the voltage headroom a modification of the circuit is presented at Figure 50(a) where resistors or current sources add up to the total bias current of the input differential pair. In order to avoid reducing the total gain the value of the resistor R_H must have a greater value than the input resistance of the second stage. At this work, as it will be explained later the R_H is replaced by a PMOS transistor working in triode region in order to control the gain at the variable gain amplifier. It must be noted that the resistors are more preferable to the current sources of Figure 50(b) since current sources may introduce substantial capacitance at the drains of the transistors.

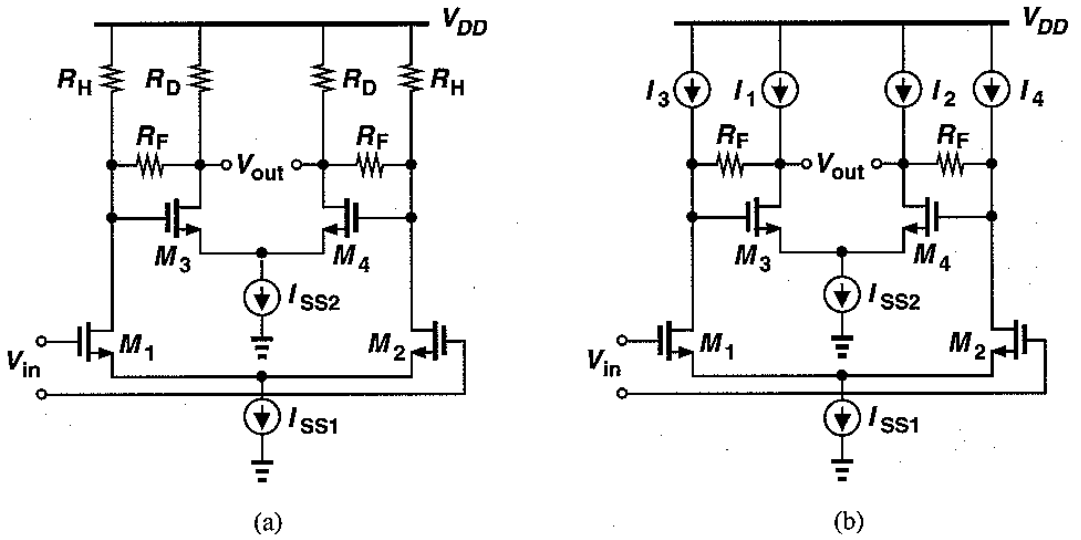


Fig.50 Modified Cherry Hooper amplifier with (a resistive loads and (b)current-source loads.

3.1.2.2 Modified Cherry Hooper amplifier

The modified Cherry Hooper amplifier cell is depicted in Figure 51.

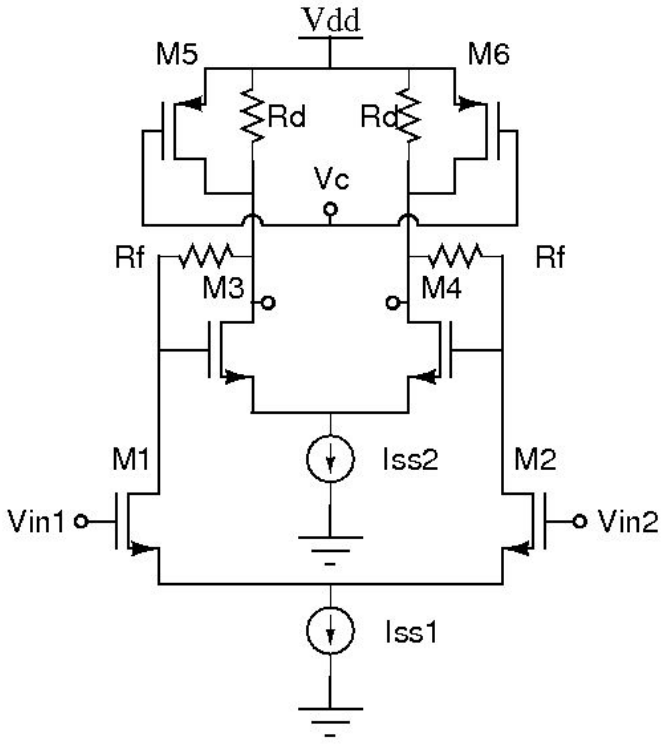


Fig.51 Modified Cherry Hooper amplifier.

In contrast with the traditional Cherry Hooper amplifier, a PMOS transistor, working in triode region, is added in parallel with the load resistance R_D .The PMOS transistor is biased with a control voltage V_C and in that way the calibration of the $M_{5,6} \parallel R_D$ is feasible. As a result the voltage drop among R_D is controlled by the value of V_C, which in turn provides the ability to control the gain of the amplifier. All in all, by having this tuneable load resistance, a wide gain range is provided since the load resistance affects the total gain at a great extent. In RF design, negative gain is also desirable since in some occasions the attenuation of the signal is necessary.

However, the Cherry Hooper amplifier has not only advantages but also drawbacks. First of all, all the transistors that comprise the differential pairs should work in saturation region and that requires large voltage headroom, making it not the optimal option when designing in small-dimension technology such as 90nm CMOS. When working under 1.2 V supply voltage, the choice of a low-threshold voltage is essential. For that reason the NMOS and PMOS transistors that were chosen from the tscm90RF library have, as it will be seen afterwards, small dimensions leading to a small value of V_{TH} . Moreover, the minimum gain of the circuit is limited by the R_D

,which in most cases has a large value. However the addition of the PMOS transistor in parallel with R_D lowers the total load resistance and in that way gain range includes negative gain.

Studying the small signal half circuit, in Figure 52, of the modified cherry Hooper amplifier the small signal gain A_V is given by:

$$A_V = A_{V0}\frac{1 - s(C_{gd2a} / g_{m2a})}{s^2 B(R_F / g_{m2a}) + sD + 1} \quad \textbf{(3.13)}$$

where $$B = C_{1T}C_{gd2a} + C_{1T}C_L + C_{gd2a}C_L \quad \textbf{(3.14)}$$

and $$D = C_{gd2a}R_F + C_{1T}\frac{R_F + R_D}{g_{m2a}R_D} + \frac{C_L}{g_{m2a}} \quad \textbf{(3.15)}$$

where A_{v0} is the DC gain of the gain cell on the condition that $g_{m2a}R_F >> 1$, $g_{m2a}R_D >> 1$ and $R_D >> R_F$[16]. C_{1T} is the total parasitic capacitance at the gates of M_3 and M_4.

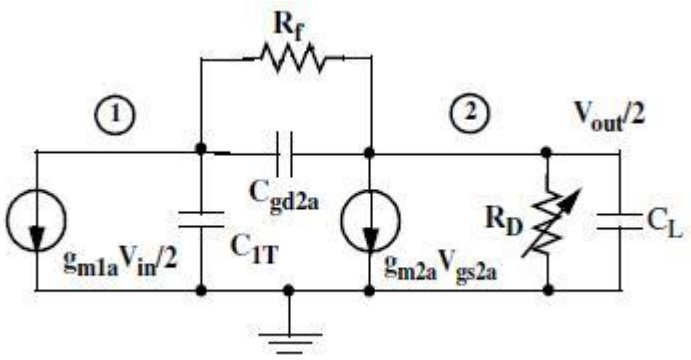


Fig.52 Simplified small-signal half circuit

3.1.2.3 VGA chain build-up

At this section, there is the description on how the VGA chain was created, starting from the first stage until the third one. In general, the first stage was designed with the maximum bandwidth which could be combined with a decent gain. Then each time an amplifier gain cell was added we had a decrease of the primal bandwidth but an increase on the overall gain of the system. On the same time always watching the phase margin in order to keep the system stable and using frequency compensation techniques to enhance the results.

- **1st stage**

At the first stage no capacitance compensation took place as according to the transfer function of (3.13) it is quite clear that the amplifier has one zero located at $\omega_z = g_{m2a}/C_{gd2a}$ and the dominant pole at $\omega_{p,\ dominant} \approx g_{m2a}/C_L$ [16].However a resistor R_{comp1} was added in order to boost the value of R_f and cause zero-pole cancelation, with the zero created. Performing zero/pole simulation analysis at Cadence Analog Design Environment the goal is to achieve pole splitting as described in Chapter 2.Knowing that the dominant pole is $\omega_p \approx g_{m2a}/C_L$, the trade-off between gain and bandwidth is declared. Increasing g_{m2a} increases the total gain of the amplifier, while increasing the load capacitance C_L increases the bandwidth. The schematic of the first stage, the frequency response graph and the result tables lie at the end of this section. The phase margin, as mentioned in Chapter 2, is calculated from $PM = 180° + \angle\beta H(\omega = \omega_1)$ where ω_1 corresponds to $2\pi f_T$.

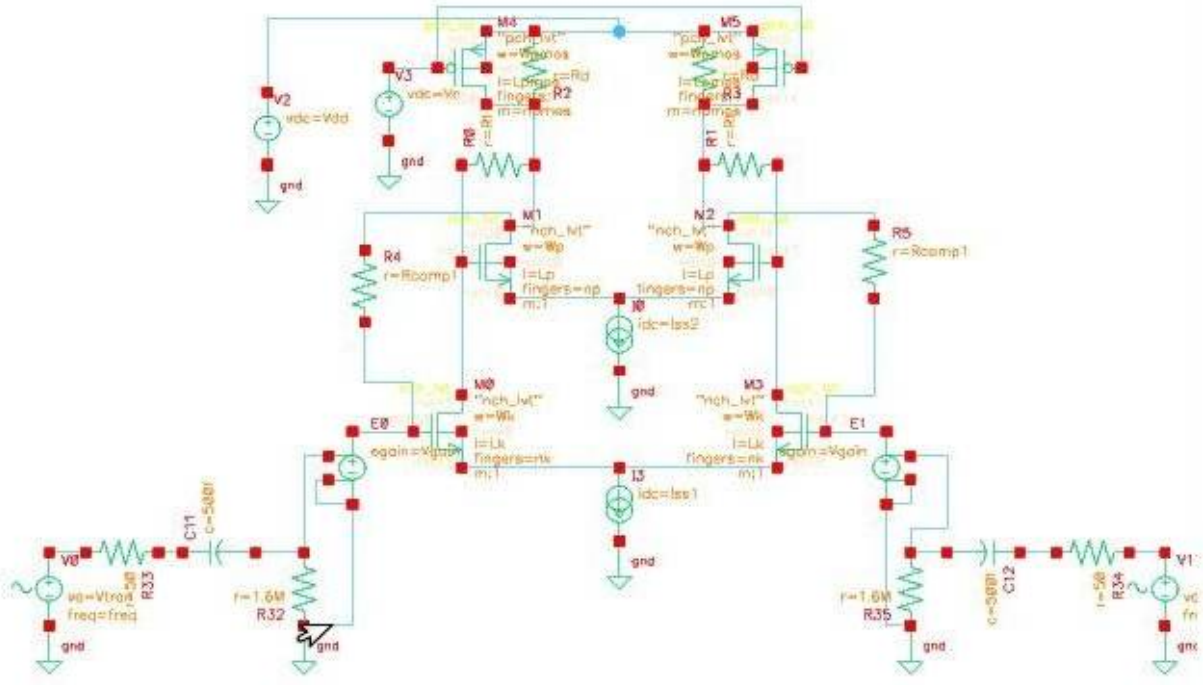


Fig.53 Amplifier's 1st stage schematic

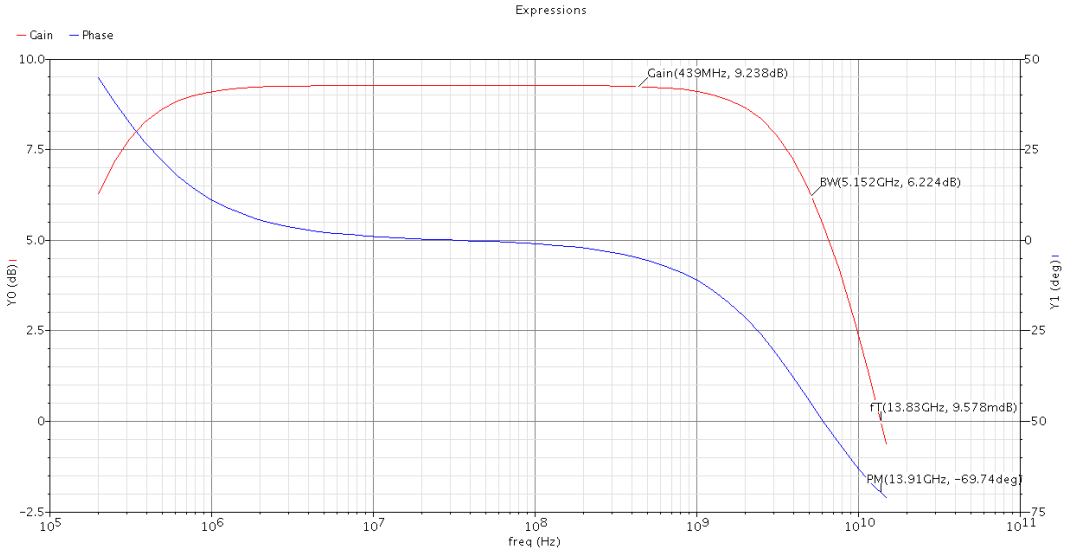


Fig.54 Frequency Response of 1st stage amplifier

Table 2.Values-dimensions of 1st stage

Block	**1st stage Cherry Hooper**
Variable	**Values/Dimensions**
$W_{1,2}$ -$L_{1,2}$	**4.356 um-140nm**
$W_{3,4}$ -$L_{3,4}$	**5um -100nm**
I_{ss1}	**77uA**
I_{ss2}	**350uA**
R_f	**9KΩ**
R_d	**5KΩ**
W_{pmos}- L_{pmos}	**20um-100nm**
R_{comp}	**634.4 Ω**
Vdd	**1.2 V**

Table 3. 1st stage efficiency

Block	**1st stage Cherry Hooper**
A	**-0.33(min)~9.23(max) dB**
f_{-3dB}	**5.15 GHz**
PM	**110^o (stable)**
f_T	**13.9 GHz**
Power Dissipation	**512.4 uW**

- **2nd stage**

When adding the second mirror stage the bandwidth of the system is expected to fall, since an increase in total gain is imminent. Connecting the output of the 1st stage with the differential pair input of the 2nd results in the presence of unwanted capacitance. As a consequence, frequency compensation proves of indispensable importance here, and more specific the simple Miller compensation with a nulling resistor (Chapter 2.3.3). A capacitor with a tiny value is used $ccap_2$=15fF, it is enough though, to cause pole splitting and keep the dominant pole as unaffected as possible. Besides that, a nulling resistor is uses,R_{comp2} =450Ω, to improve the phase margin. It must be noticed, that a new technique is employed at the second and third stage, the inverse scaling technique. It has to do with the dimension of the W of the input differential pair in correlation with the W of the first differential pair of the first stage. More specifically, the value of W at each stage is the half of the previous one, resulting in gaining extra bandwidth since unwanted input capacitance is decreased. More details will be given in the next section of this chapter, where the techniques employed on this design are described.2nd stage schematic tables and frequency response are listed below.

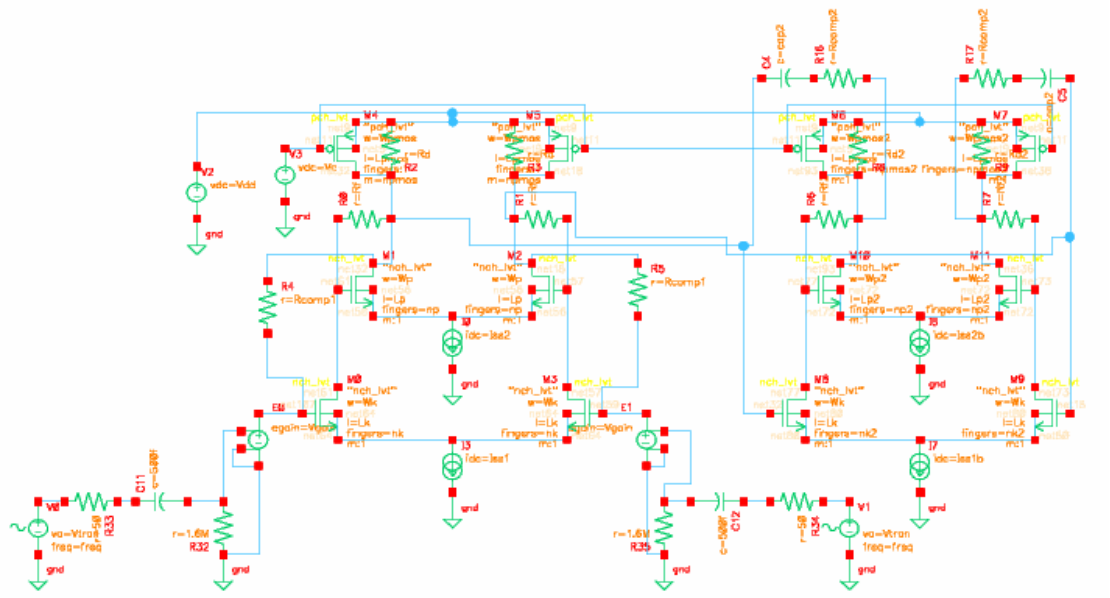


Fig.55 Amplifier's 2nd stage schematic

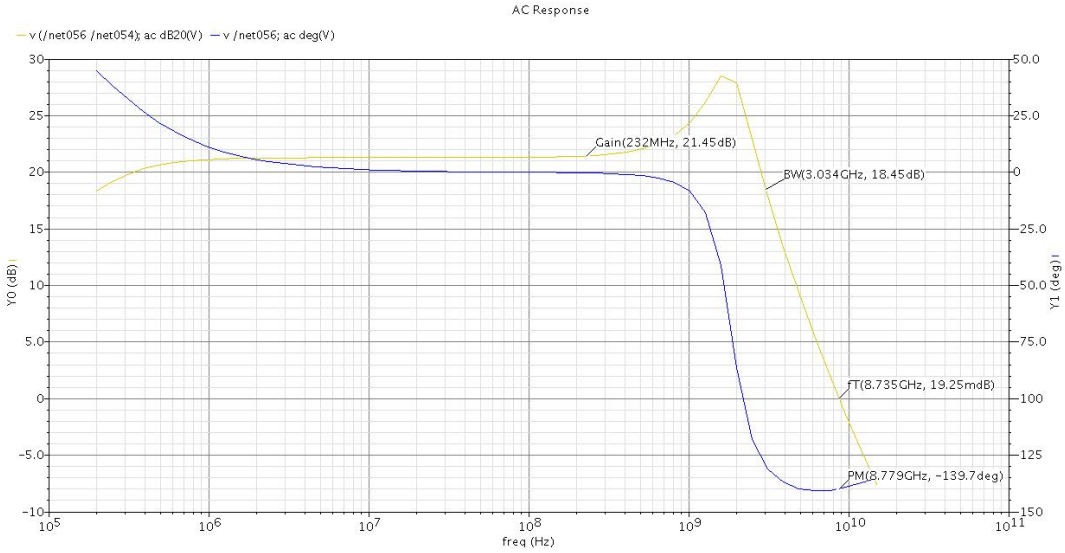


Fig.56 Frequency Response of 2nd stage amplifier

Table 4.Values-dimensions of 2nd stage

Block	**2nd stage Cherry Hooper**
Variable	**Values/Dimensions**
$W_{1,2}$ -$L_{1,2}$	**2.178 um-140nm**
$W_{3,4}$ -$L_{3,4}$	**5um -100nm**
I_{ss1}	**72uA**
I_{ss2}	**380uA**
R_{f2}	**12.75 KΩ**
R_{d2}	**5 KΩ**
W_{pmos}- L_{pmos}	**20um-100nm**
R_{comp2}	**450 Ω**
C_{cap2}	**150 fF**

Table 5. 2nd stage efficiency

Block	**2nd stage Cherry Hooper**
A	**-3.27(min)~21.45(max)dB**
f_{-3dB}	**3.03 GHz**
PM	**40^o (stable)**
f_T	**8.77 GHz**
Power Dissipation	**542.24 uW**

- **3rd stage**

The 3rd stage is the final stage of the VGA chain and it includes the DC-offset correction, comprised of a low-pass filter and a feedback amplifier. As it will be observed, the bandwidth continues to fall, however the total gain reaches its maximum value. Many would wonder why not adding a fourth stage at the VGA chain, in order to achieve a higher gain as the compensation helps to keep the bandwidth at decent levels for RF design. The answer is that the pole-zero analysis is already overloaded, since there are numerous poles and zeros at the transfer function which makes the frequency compensation quite a complicated procedure. In addition to that employing a 4th stage would increase the power dissipation since more current would be necessary.RC Miller with nulling resistor compensation is used again, exploiting the Miller effect, with compensation capacitance cap_3=25 fF and nulling resistor R_{comp3}=7 KΩ. 3rd stage VGA schematic figure, tables and frequency response are listed below.

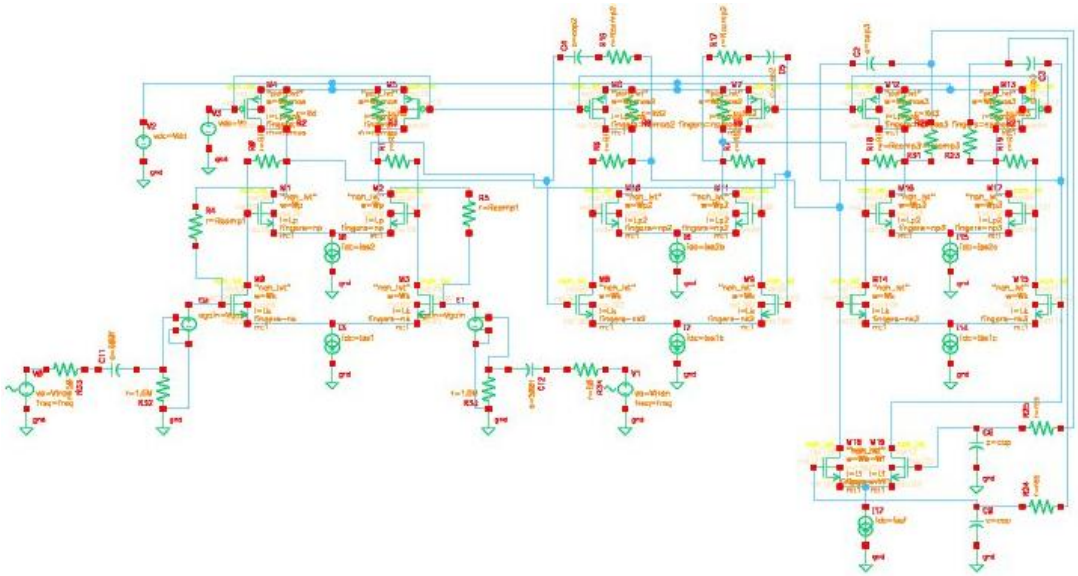


Fig.57 Amplifier's 3rd stage schematic

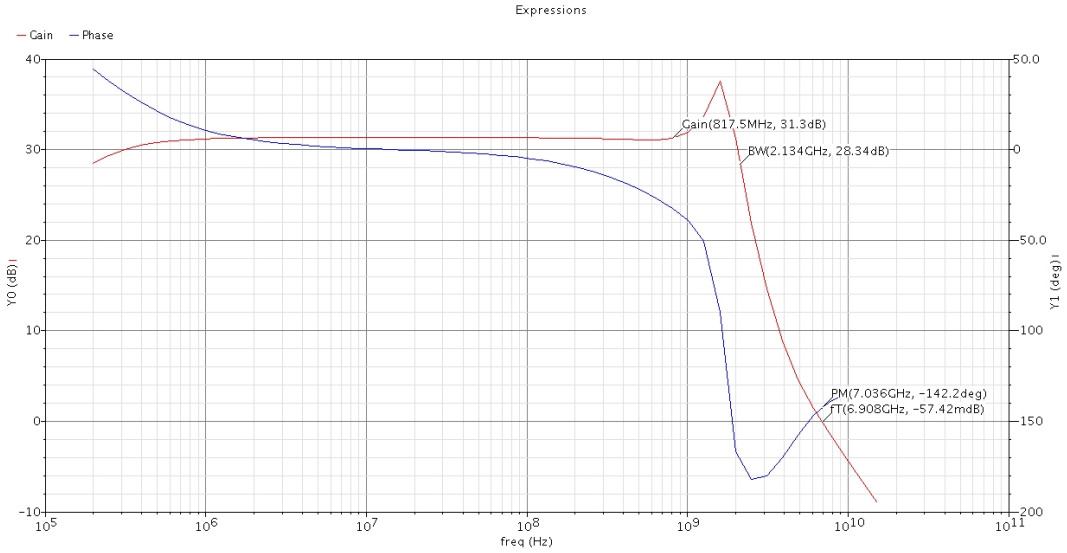


Fig.58 Frequency Response of 3rd stage amplifier

Table 6.Values-dimensions of 3rd stage

Block	**3rd stage Cherry Hooper**
Variable	**Values/Dimensions**
$W_{1,2}$ -$L_{1,2}$	**1.089um-140nm**
$W_{3,4}$ -$L_{3,4}$	**5um -100nm**
I_{ss1}	**60uA**
I_{ss2}	**380uA**
R_{f3}	**13.9 KΩ**
R_{d2}	**5 KΩ**
W_{pmos}- L_{pmos}	**20um-100nm**
R_{comp3}	**7 KΩ**
C_{cap2}	**25 fF**

Table 7. 3rd stage efficiency

Block	**3rd stage Cherry Hooper**
A	**-10.6(min)~31.3(max)dB**
f_{-3dB}	**2.13 GHz**
PM	**38^o (stable)**
f_T	**6.9 GHz**
Power Dissipation	**528 uW**

3.1.3 Low-pass filter with feedback amplifier

Both the filter and the amplifier are needed for the DC-offset correction as they form the negative feedback loop. In the next section their functionality will be explained thoroughly, even though that has been done at chapter 2.5.3.2 with a similar example. The cut-off frequency of the filter is at 500KHz.This choice was made because, in order to check for DC-Offset a fast sensing filter was needed to track the changing offsets at the output of the VGA chain. At the same time it should be ensured that there was minor degrading of the signal, since if a higher cut-off frequency was chosen the signal of interest would be removed. The low-pass filter is utilized as a first order RC filter with a capacitance of 0,102 pF and a 3.122 MΩ resistor.

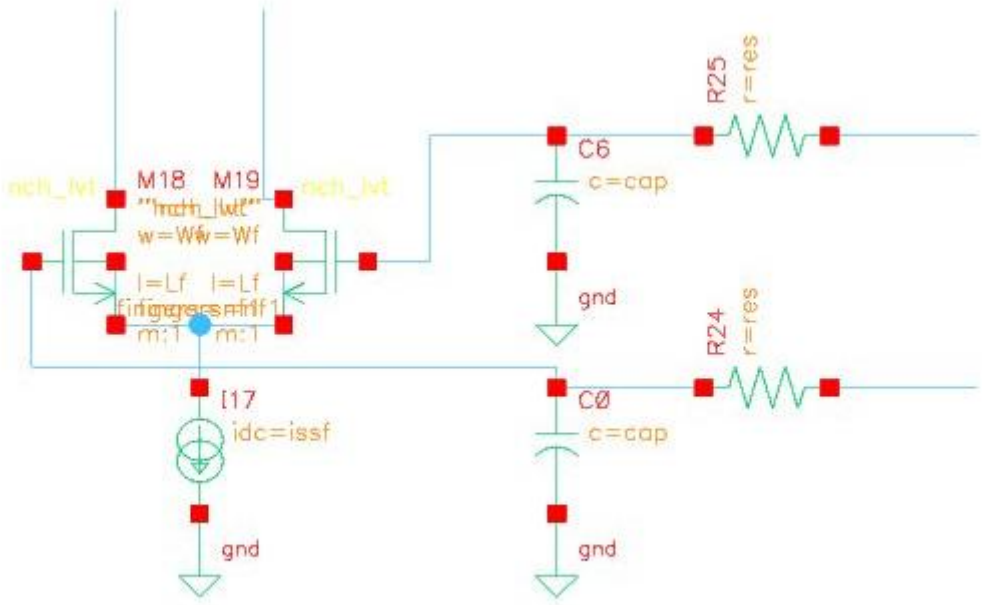


Fig.59 Feedback amplifier's and LPF schematic

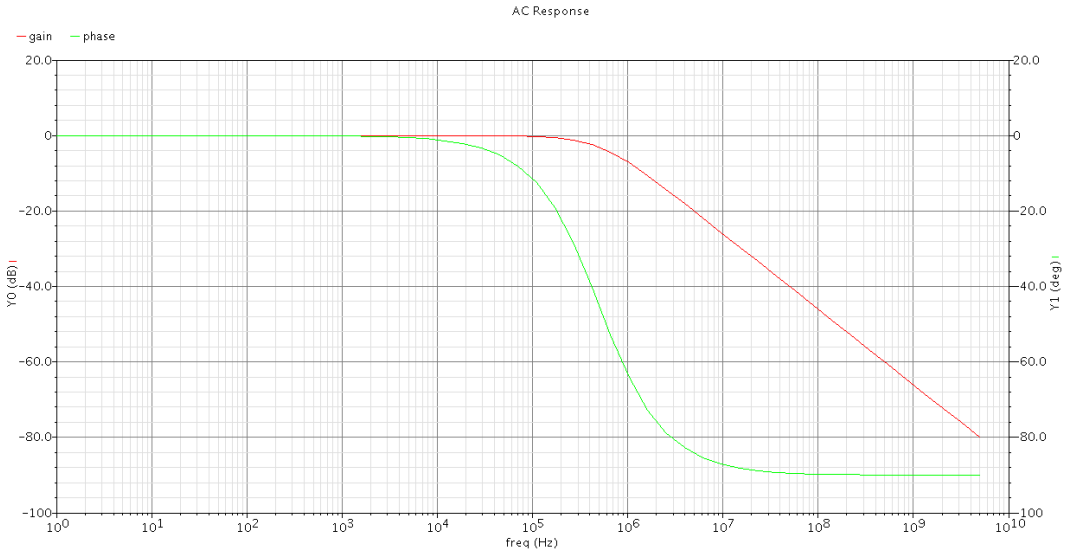


Fig.60 Frequency Response of LPF and feedback amplifier

Table 8. LPF-Feedback amplifier design values

Block	**LPF**
Values	
R	**3.122 MΩ**
C	**0.102 pF**
Block	**Feedback amplifier**
Values	
W_f	**200nm**
L_f	**100nm**
I_{ssf}	**1uA**

3.2 Techniques utilized during design

The specific VGA design employs two techniques that substantially increase the bandwidth and deal with the DC-offset correction. These two techniques are inverse scaling and active negative feedback.

3.2.1 Inverse scaling

As mentioned before inverse scaling proposes the systematic decrease by a factor of 50% the width of the transistors that form the input differential pair at the transconductance stage of the Cherry Hooper amplifier. This allows the circuit to have extra bandwidth and it will be explained why.

The GBW product of each stage, at a multistage amplifier, is g_m/C_{tot} ,where C_{tot} is the total load capacitance of the stage and includes:

- stage output capacitance C_o
- wiring capacitance C_w and
- following stage input capacitance C_i .

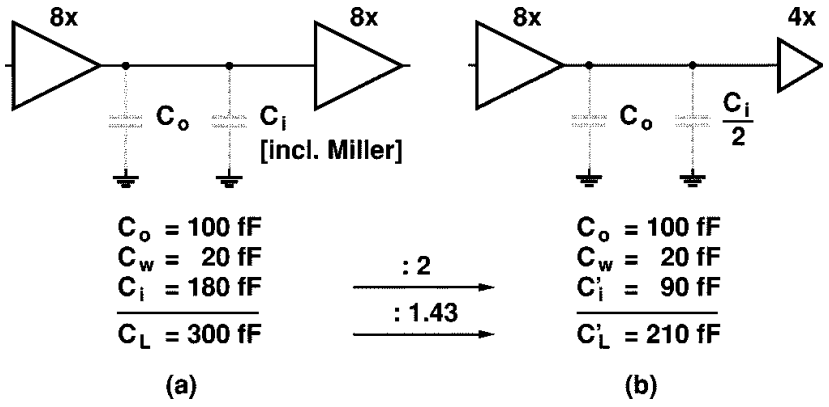


Fig.61(a)no scaling (b)inverse scaling

In case widths of the transistors and current sources scale by a steady factor then, g_m and the previously mentioned capacitances are scaled by the same factor too. As a result the GBW has a fixed value [17].Figure 61 points out an example with inverse scaling. Figure 61(a) depicts two stages without scaling and (b) the same stages with inverse scaling, as the C'_{in} of the second stage has the half value than before. As a result, total C_L is reduced by a factor of 1.43 which means that the GBW of the second case is 1.43 times more. By applying this technique to all the stages to all the stages of an amplifier chain, increases the bandwidth of all the stages giving an essential bonus to the bandwidth of the circuit. Furthermore an additional advantage

of inverse scaling is the reduction of power consumption approximately by 50%, without affecting the noise and offset, which are determined usually from the first stage which remains unscaled. As mentioned before at this work the C_i is reduced every time by a factor of two when moving to the next stage.

However, there are limits on how far the scaling can reach, as the ideal case would be to downscale by a large factor every time a stage is added, leading to a larger bandwidth value. The factors that prevent the practice of that are that a minimum value of C_L should be driven to the last stage and the maximum allowable value of input capacitance at the second in order stage.

3.2.2 Active negative feedback

The active negative feedback functionality is explained thoroughly at **chapter 2.5.3.2.**However it would be better to explain how this method adapts to the current design data, as shown in Figure 62.

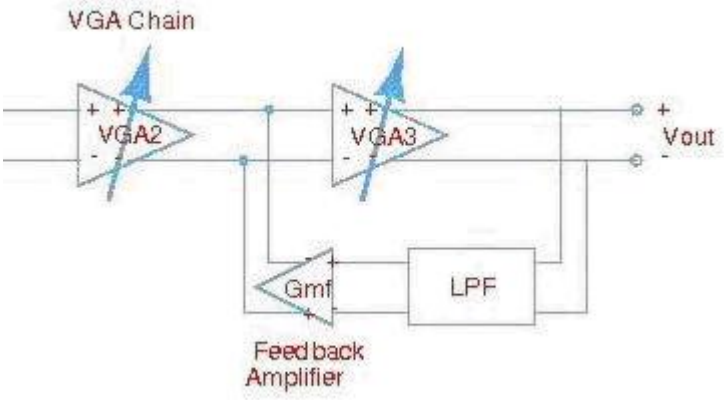


Fig.62 DC-Offset Correction network

The low-pass filter tracks the offset changes at the output of stage 3, outputs which may have been caused even by a mismatch at stage one. Since the filter is sensing at a quite rapid value, the feedback amplifier by reversing the inputs, negates any offset that appears. For example, in case DC-Offset appears, for V_{dc}=0 $VGA3_{out}(+)$=0.1mV and $VGA3_{out}(-)$=0mV.Then the output of the differential amplifier is equal to $VGA3_{out}(+)$-$VGA3_{out}(-)$=0.1mV.However, due to the feedback amplifier, the output is now the opposite input and vice versa. This results in $VGA3_{in}(+)$=$VGA3_{out}(-)$ and $VGA3_{in}(-)$=$VGA3_{out}(+)$ which leads to $VGA3'_{out}(+)$-$VGA3'_{out}(-)$=-0.1mV.The previous output was 1mV and in that way the offset is negated since the sum of the outputs is equal to zero.

3.3 Design Optimization

3.3.1 Inversion Coefficient –Performance Trade-offs

When designing at low-voltage technologies such as 90nm CMOS, design optimization is significant as the designers demands the optimal performance in order to meet the primal expectations and standards. Once the circuit is defined, the designer has to find the right tradeoffs and then size the different components, and specifically choose the bias current, width, and length of MOS transistors to achieve the desired specifications.
Inversion coefficient (IC) is the main transistor design parameter which covers all the regions of operation of the MOS transistor in a continuous way. In that way, it is possible to express all the important parameters of as single transistor, such as transconductances or capacitances, in relation with IC.Inversion coefficient is given by[18]:

$$IC = \frac{I_D}{I_{SPEC0}(\frac{W}{L})} \quad \textbf{(3.16)}$$

where I_{SPEC0} is the technology current given by:

$$I_{SPEC0} = 2n_o\mu_0 C'_{OX} U_T^2 \quad \textbf{(3.17)}$$

where n_0 is the substrate factor,μ is the mobility factor,C'_{OX} is the gate oxide capacitance per unit area and U^2_T is the thermal voltage. Selecting drain current I_D,IC and channel length L defines the transition among performance trade-offs. Figure 63 illustrates the MOSFET Operating Plane versus the selected inversion coefficient and channel length for a fixed drain current [19].

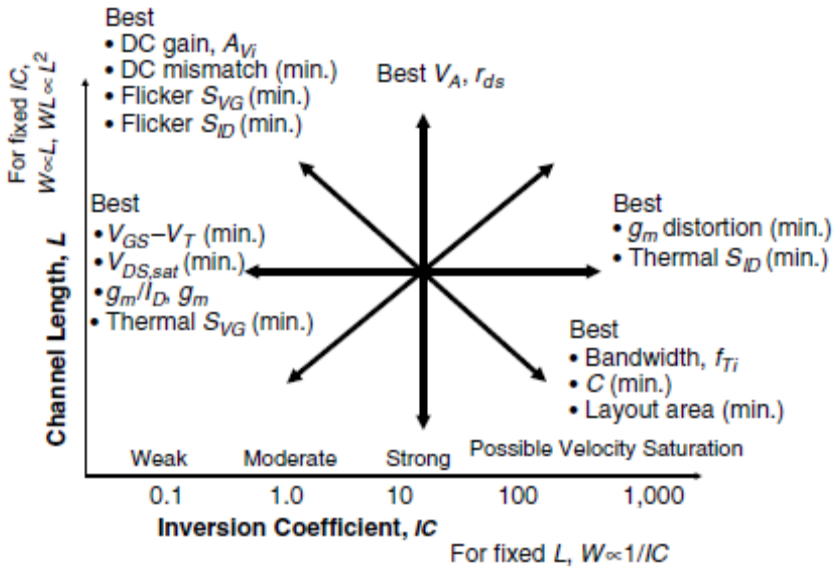


Fig.63 Trade-offs at MOSFET operating plane

By observing the plane, it can be concluded that for low values of IC, which represent weak or moderate inversion at the left half plane(IC<10), those who benefit from that are g_m and DC gain. At the same time V_{EFF} and V_{DSAT} reach their minimum possible values, similar to flicker noise. It will be proved later, using data from this design, that W/L ratio gets its highest value here.
On the other hand, moving to the right half plane, where strong inversion takes place (IC>10), bandwidth reaches high values. In addition to that, capacitances get their lowest values and so does the thermal noise.
What is important concerning this design is the selecting the values for the differential pairs of the Cherry Hooper amplifier, where DC gain and bandwidth should be combined. As a consequence, the initial idea is to choose a value of IC in moderate inversion, as it will be presented later.

3.3.2 MOSFET's Inversion Areas

At the previous section the analyses took place based on the fact that I_D had a fixed value. Now the separation of MOSFET's inversion areas is made for a given IC and channel length L, Figure 64.Observing that the inversion areas are separated into:

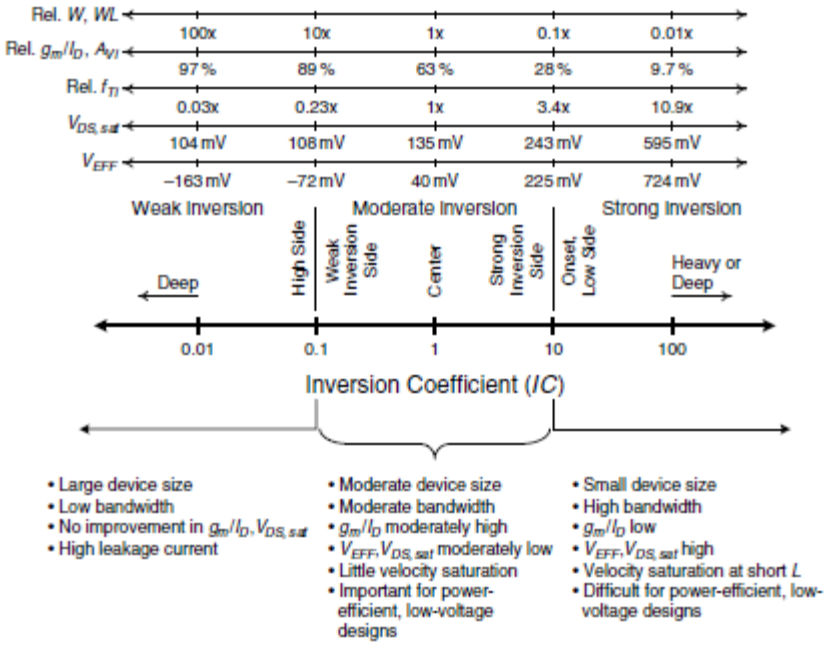


Fig.64 Trade-offs of MOSFET's inversion areas

- **Deep weak inversion** (IC < 0.1 , V_{EFF} < -163mV , V_{DSAT} <104mV).At this area V_{EFF},V_{DSAT} get their minimum values and so does bandwidth.However,large device size and high leakage current should be noticed, whereas g_m,DC gain and g_m/I_D increase by a small amount.
- **High side of weak inversion** (IC = 0.1 , V_{EFF} = -72mV , V_{DSAT} = 108mV).At this area g_m and g_m/I_D reach maximum values. DC gain, width and device size get large values in contrast with V_{EFF},V_{DSAT}. Finally, a small increase at the bandwidth should be noticed.
- **Weak-inversion side of moderate inversion** (0.1 < IC < 1 , -72mV < V_{EFF} < 40mV , 108mV <V_{DSAT} < 135mV).IC is increased and as a result width, device size area, g_m,DC gain and g_m/I_D decrease. On the other hand V_{EFF},V_{DSAT} increase.
- **Center of moderate inversion** (IC = 1 , V_{EFF} = 40mV , V_{DSAT} = 135mV).The parameters mentioned before keep increasing/decreasing at the same direction.
- **Strong-inversion side of moderate inversion** (1 < IC < 10 , 40mV < V_{EFF} < 225mV , 135mV <V_{DSAT} < 243mV).From now these areas are suitable <u>for low power dissipation and supply voltage</u>. V_{EFF},V_{DSAT}, design. Bandwidth and device size area have mediocre values, while get a remarkable increase. Due to low saturation, bandwidth may not get the highest value possible, though it is suitable for many applications.
- **Low-side of strong inversion** (10 < IC < 100 , 225mV < V_{EFF} < 724mV , 243mV < V_{DSAT} < 595mV).High bandwidth and low W describe this area. However low values of g_m and g_m/I_D ,in conjunction with the high values of V_{EFF},V_{DSAT}, do not support low voltage design.
- **Heavy or deep strong inversion** (IC > 100 , V_{EFF} > 724mV , V_{DSAT} > 595mV).As before, it is not recommended for low-voltage design. High bandwidth,V_{EFF},V_{DSAT} in contrast with quite low DC gain, device size, g_m and g_m/I_D and small device area size describe this sub-area.

All in all, while moving from weak to strong inversion and IC is increased, W, device area, DC gain, g_m and g_m/I_D decrease, whereas V_{EFF},V_{DSAT} and bandwidth get their maximum values. The trade-off between DC gain and bandwidth is easy to notice as their maximum values reside at the opposite inversion areas. Nevertheless, it should be noticed that, strong inversion area may support high bandwidth, however it is not suitable for low voltage design due to the fact of the high values of V_{EFF},V_{DSAT}.Low voltage design poses serious issues with the available voltage headroom and the high values of V_{EFF},V_{DSAT} make it almost impossible function, especially when transistors are supposed to work in saturation.

3.3.3 Optimization with design parameters

It is easy to notice that in this work the main topology is the differential pair, as it is the main part of the Cherry Hooper amplifier. What is most desirable when designing a differential pair, is the high DC gain, though at this work high bandwidth is needed too, which makes it impossible to work in wean inversion. As a result, according to the previous sections the differential pair must work at the strong side of moderate inversion area, as this area is suitable for low voltage design. The design of the first VGA cell was based on that concept and so did the following.

First of all, the calculation of the parameters is needed:

(All the useful values information needed for the calculation was taken from the tscm90RF library of *Virtuoso Analog Design at Cadence*.)

$$C'_{OX} = \frac{\varepsilon_{OX}}{T_{OX}} = \frac{3.45*10^{-11}}{2.83*10^{-9}} = 1.22*10^{-2}\,\frac{F}{m^2}$$

$K_p = \mu * C'_{OX}$ $=44.87*10^{-3}*1.22*10^{-2} = 5.474*10^{-4}$ A/V^2

Substituting at equation(3.17) :

$$I_{spec0} = 2nU_T^2 K_p\,(W/L) = 0.8109\ \mu A\,(W/L). \qquad \textbf{(3.18)}$$

For example, the W,L,I_D values for the input differential pair are W=4.356um,L=140nm and I_D=38.5uA.

Combining equations (3.16) and (3.18), we obtain IC=1.52 which is moderate inversion, very slightly above the middle of moderate inversion.

CHAPTER 4

SIMULATION RESULTS

The simulation results are divided into 3 sections. The first section is the results regarding the gain, bandwidth and other important factors of the circuit. The next section refers to DC-Offset Correction and noise figure, while the last section illustrates worst-case assumptions regarding temperature and supply voltage variations.

4.1 Gain-Phase-Slew Rate Figures

Figure 65 depicts the total gain, bandwidth of the system both of them combined with the phase margin. The utilization of the high-pass filter before the input differential pair blocks the signal for any frequency under 200 KHz. The phase margin is 38 degrees which makes the system quite stable.

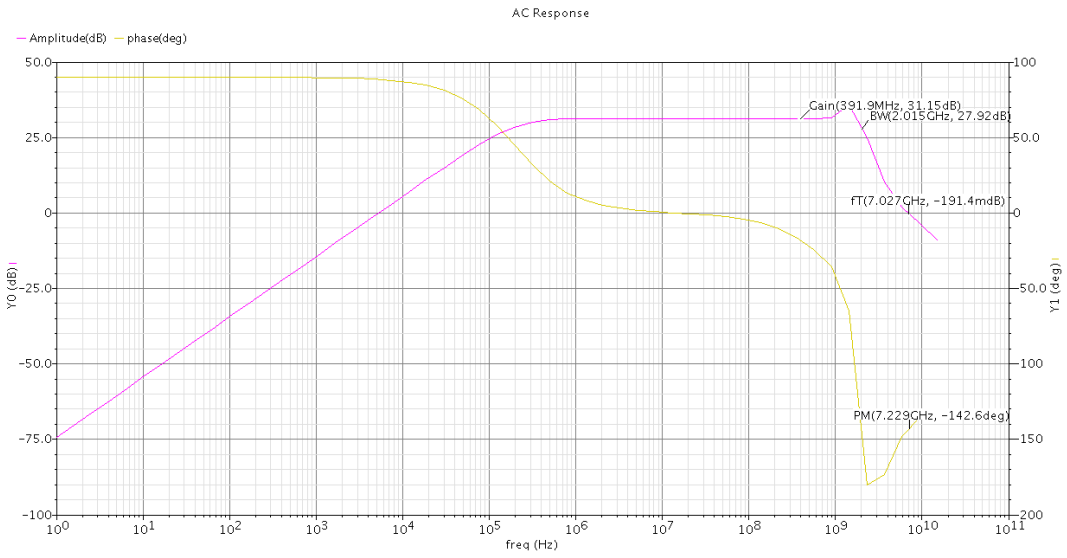


Fig.65 Gain-Bandwidth of the VGA

Figure 66 illustrates the total gain of the system for ten different V_c values, starting from 0V to 1V.The VGA shows quite linear behavior when V_c =0V to 0.65V, while gain values seem to converge at around 30dB when V_c>0.7 V. This is due to the bias of the PMOS transistor since for these values of voltage control, it escapes triode region decreasing the resistance and hence the voltage drop over R_D.

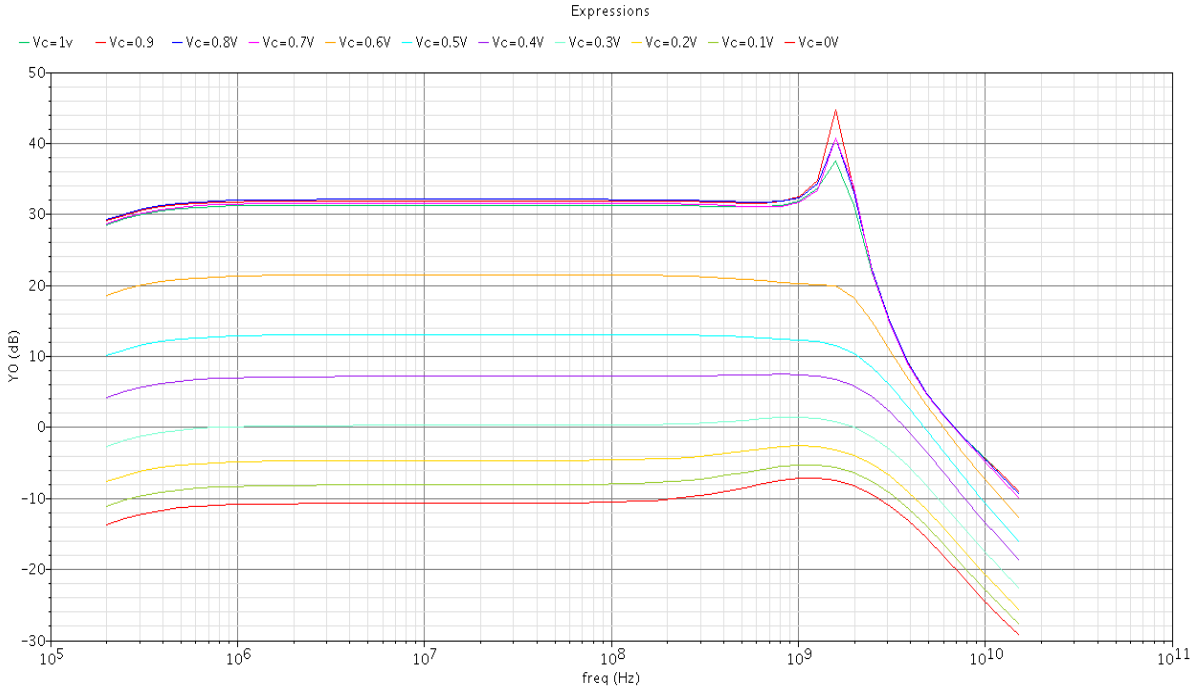


Fig.66 Gain values when sweeping V_c

At the end of this section lies the slew rate plot, Figure 67.For input V_{in}=1.5V ,in transient analysis , slew rate reaches 13.9V/nsec which is an acceptable value since slew rate ≥ Amplitude/T. T is the period of the square pulse ,which is T=2.4ns, and amplitude is A=1.5V,hence slew rate ≥ 0.625V/ns.In order to calculate slew rate, one option is to $SR = \frac{\partial \Delta V_{out}}{\partial t}$ = 13.9V/nsec

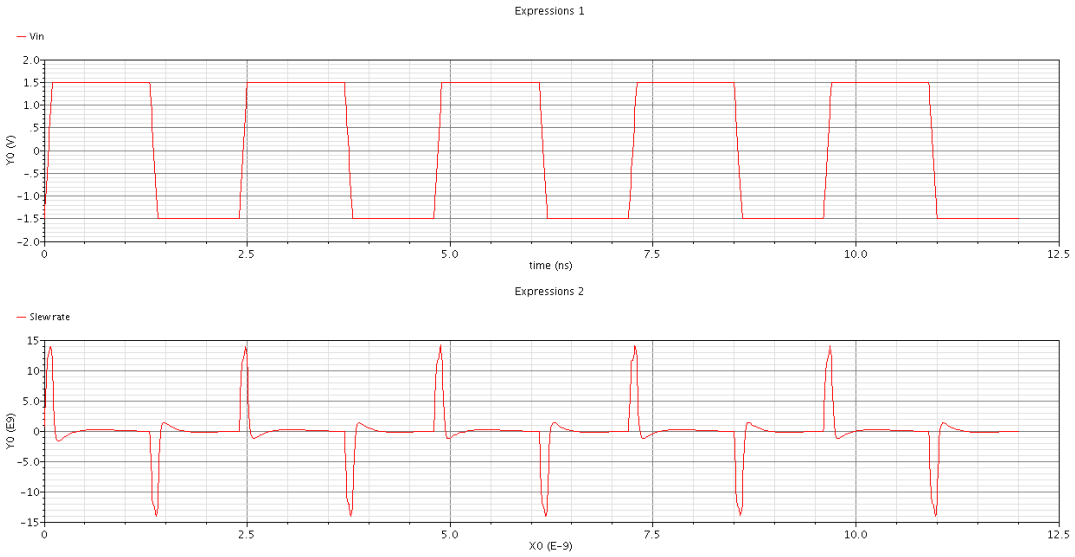


Fig.67 Slew rate of the VGA

4.2 DC-Offset, Noise Figures

In order to be more noticeable two figures regarding DC-offset correction are presented. In figure 68,Dc output is exhibited while having disconnected the negative feedback network from the main circuit. As a result a value of DC-offset is observed, and more specifically DC-offset is 12um.However when employing the feedback network the DC-offset has tiny values at the range of am and fm, Figure 69.

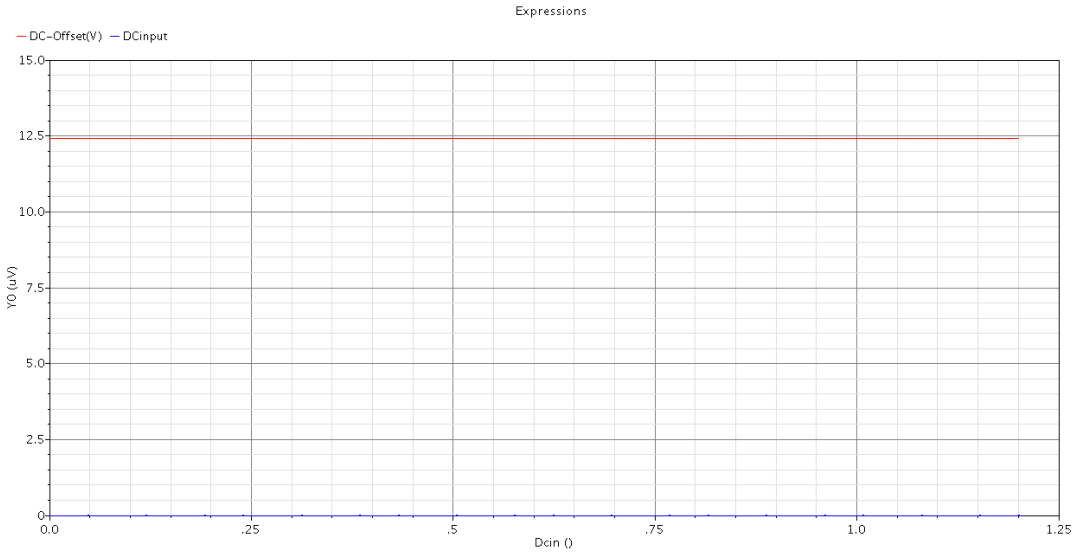


Fig.68 DC-offset output without the correction network.

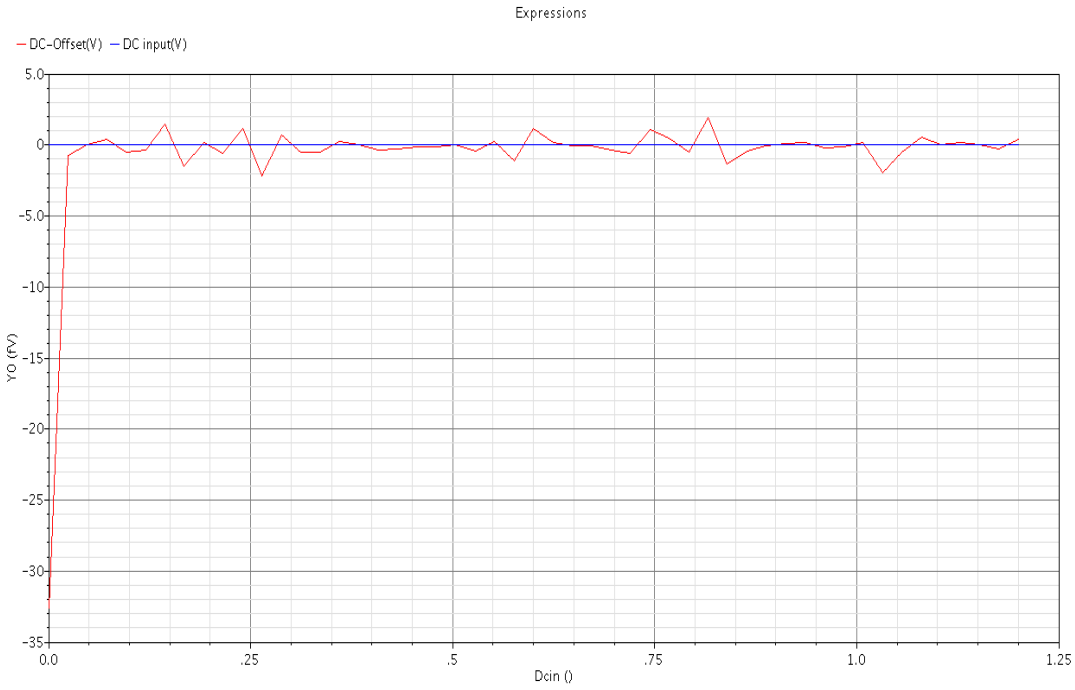


Fig.69 DC-offset output with the correction network.

Figure 70 illustrates the squared output noise of the system. The outcome is quite encouraging as the presence of noise is only at the frequencies of 1 to 200Hz.Even in that frequencies the strength of the noise signal is at the range of $10^{-9}V^2/Hz$.

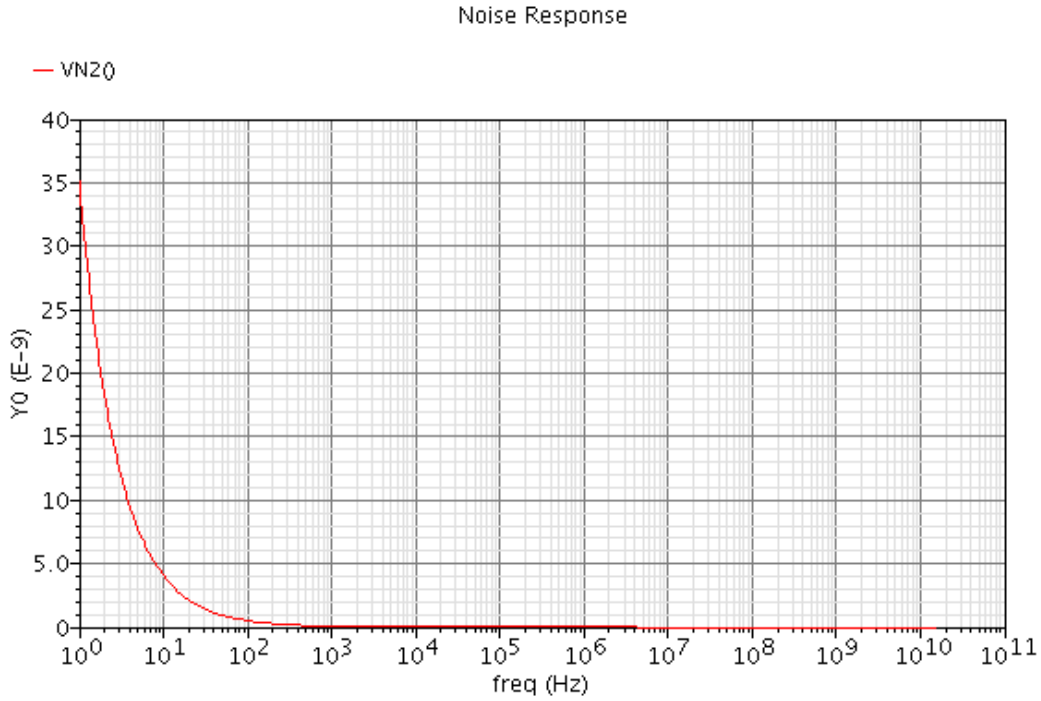


Fig.70 Squared output noise of the system.

4.3 Worst case assumptions

When designing a system, worst case scenario should be taken into consideration in order to simulate the system's performance under formidable conditions such as overheating or voltage drop. The cases that are examined at this work are extreme temperature conditions and a voltage drop. When simulating the gain verse temperature conditions the margins are -25^{o} C and 75^{o} C, Figure 71.It can be noticed that the overall gain has its greatest value at the temperature of -25^{o} C. However, as temperature rises up the gain drops dramatically. This is mainly caused by the thermal noise.

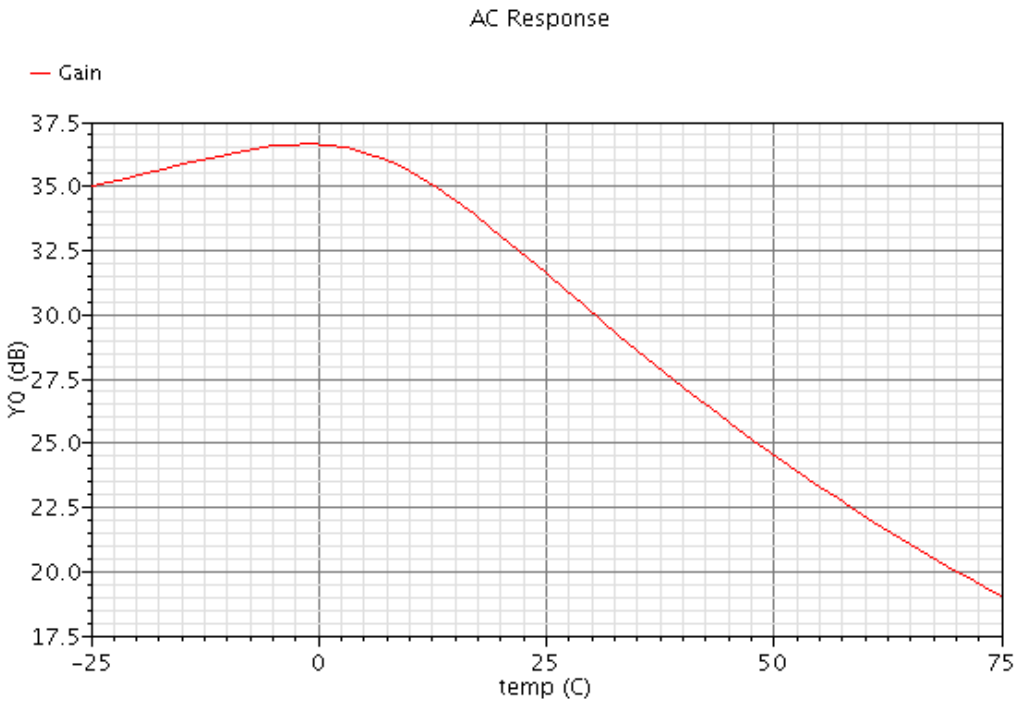


Fig.71 Worst case assumption: gain versus temperature

As far as voltage drop is concerned, the test was about simulating a drop to 1V from to 1.2.Of course the gain severely dropped since the circuit has too many transistors and the voltage headroom has become obsolete. As a result, reduction due to voltage drop will degrade the gain severely, Figure 72.

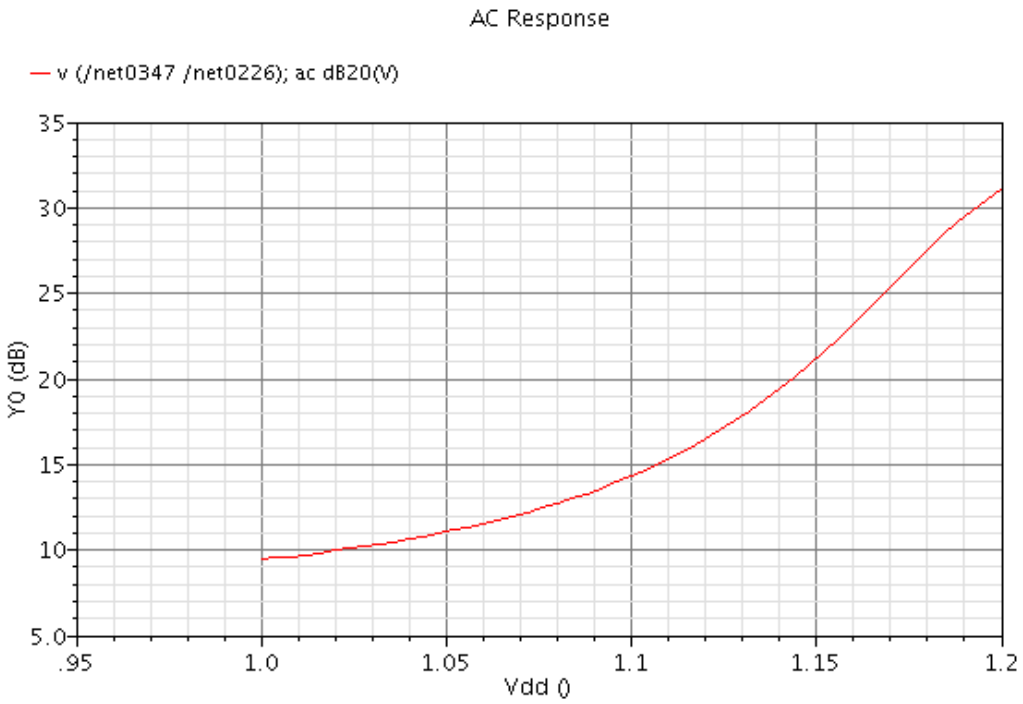


Fig.72 Worst case assumption: voltage drop

CHAPTER 5

CONCLUSION

A RF receiver VGA in 90nm CMOS technology is presented in this thesis. The gain of this VGA is varied by changing the value of R_D which is the load resistance of the circuit and as a result affects the total gain. A PMOS, biased in the triode region by the control voltage V_c, is in parallel with R_D, utilizing a tuneable resistance. The amplifier is comprised of three gain cells of the inductorless Cherry-Hooper amplifier, a high pass filter for feedforward DC-Offset correction and a negative loop feedback, combined of a low-pass filter and a feedback amplifier, for automatic DC-Offset correction. The VGA exhibits a combination of 2.1 GHz bandwidth and a gain range of 41.9dB (-10.6~31.3), having a low-noise performance with high slew rate. Inverse scaling and negative feedback techniques are employed, which not only increase the bandwidth but also provide offset cancelation. Due to the fact that the VGA is a multistage amplifier, frequency compensation is of vital importance and it is achieved by using a Miller capacitance and a nulling resistor on each stage. Last but not least, the first gain cell was designed using the inversion coefficient as a guide in order to meet the initial specifications. The results as shown below prove to be very interesting compared to other similar works.

5.1 System's performance

Table 9 System's Measured Performance

Parameter	**Value**
Gain Range	(-10.6~31.3)dB
f_{-3dB}	2.1 GHz
PM	38 deg
f_T	6.9 GHZ
Voltage Supply	1.2 V
Power Dissipation	1.9 mW
Slew Rate	13.900 V/usec

Table 10. Performance Comparison of VGA Architectures

Reference	[20]	[13]	[21]	[22]	[5]	This Work
Process	90nm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.35µm CMOS	90nm CMOS
Gain (dB)	13.5~67.5	-16~34	-39~55	-8~32	-30~50	-10.6~31.3
BW(GHz)	0.1	2	0.9	0.018	0.02	2.1
Power(mW)	13.5	40	11.4	11.6	7	1.9
Supply(V)	1.8	1.2	2.7	1.6~2	3	1.2

5.2 Future work and suggestions

- Integration of the VGA with the other building blocks of an RF receiver (LNA, mixer, VCO,filter)
- Substitution of the valued resistances used in the filters with sub-threshold resistors [20].
- Digitally controlled with calibration of V_c signal.
- Optimization using the EKV model[24,25].
- Physical design of the circuit (layout).

5.3 Appendix

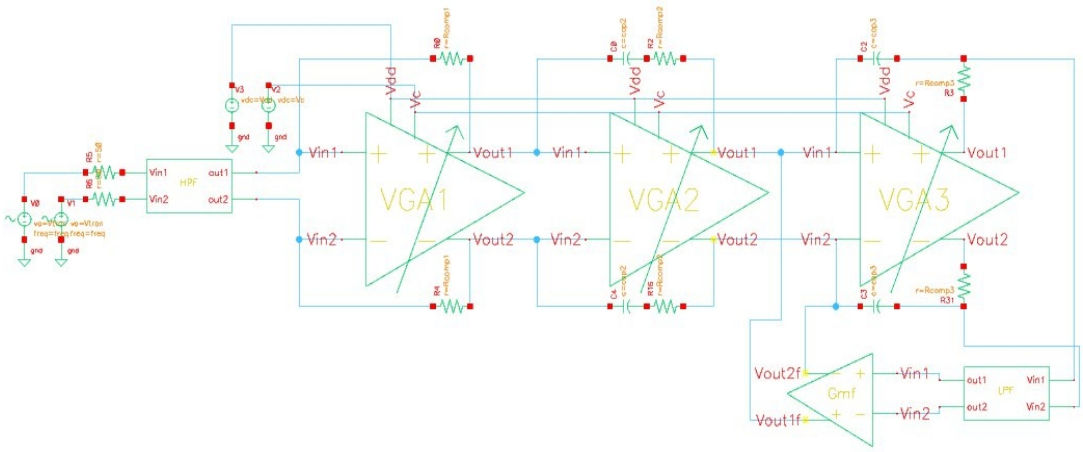


Fig.73 VGA Hierarchy Design

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