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THESIS

Design Of Current Mode CMOS Integrated Filters

Georgios Smaragdos

Abstract

The new technologies in electronics have forced transistors to smaller and smaller sizes.The consequences of this trend are often researched for digital design, because of its wider usage. Yet analog design is equally important. Analog circuits are required for the connection between the natural(analog) world and the digital and are often useful for low precision application. The influence of new technology trends are, however, often neglected.A main issue with the lowering of sizes is the simultaneous scaling of the voltage supplies. One solution is the use of current mode instead of voltage mode circuits. In this thesis the application of the idea is explored in the design of active high frequency ladder filters. Two design strategies are used: The Gm-C strategy and the implementation using current mode operational amplifiers. The first strategy was done based on a previously designed 1MHz filter, previously implemented in 1.2um process, redesigned now in 0.25um with a frequency of 4.2MHz. The CM OpAmp implementations were based on the voltage mode counterparts and two design examples are shown with operating frequencies of 155MHz and 7.2GHz. All filters were then redesigned using the Inversion Coefficient (IC) as a guide for the transistor aspect ratio choices to achieve better behavior. The evaluation of the design was done in terms of supply voltage, transistor area, power consumption, general stability(phase margin), frequency tunability and transistor matching. Compared to the original Gm-C filter, made in older technology, the new designs had a reduction of 50-74% in terms of supply voltage and significanlty lower transistor area.The power consumption was about 3 mW for the Gm-C filters and around 20mW for the CM OpAmp implementations. The final Gm-C filter designs could cover operating frequencies between 0.77MHz and 4.2MHz, while the 2 CM OpAmp designs can operate from 158MHz to 28MHz for the first design and from 9.2GHz to 100KHz for the second.

Department of Electronics and Computer Engineering

Design Of Current Mode CMOS Integrated Filters

THESIS

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by

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The new technologies in electronics have forced transistors to smaller and smaller sizes.The consequences of this trend are often researched for digital design, because of its wider usage. Yet analog design is equally important. Analog circuits are required for the connection between the natural(analog) world and the digital and are often useful for low precision application. The influence of new technology trends are, however, often neglected.A main issue with the lowering of sizes is the simultaneous scaling of the voltage supplies. One solution is the use of current mode instead of voltage mode circuits. In this thesis the application of the idea is explored in the design of active high frequency ladder filters. Two design strategies are used: The Gm-C strategy and the implementation using current mode operational amplifiers. The first strategy was done based on a previously designed 1MHz filter, previously implemented in 1.2um process, redesigned now in 0.25um with a frequency of 4.2MHz. The CM OpAmp implementations were based on the voltage mode counterparts and two design examples are shown with operating frequencies of 155MHz and 7.2GHz. All filters were then redesigned using the Inversion Coefficient (IC) as a guide for the transistor aspect ratio choices to achieve better behavior. The evaluation of the design was done in terms of supply voltage, transistor area, power consumption, general stability(phase margin), frequency tunability and transistor matching. Compared to the original Gm-C filter, made in older technology, the new designs had a reduction of 50-74% in terms of supply voltage and significanlty lower transistor area.The power consumption was about 3 mW for the Gm-C filters and around 20mW for the CM OpAmp implementations. The final Gm-C filter designs could cover operating frequencies between 0.77MHz and 4.2MHz, while the 2 CM OpAmp designs can operate from 158MHz to 28MHz for the first design and from 9.2GHz to 100KHz for the second.

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1 Introduction

Digital design of integrated circuits, due to their wide usage, have defined technology trends for some time now. Recent trends dictate to constantly achieve smaller and smaller transistor sizes. The reduction helps the digital designer to create more dense,complex and efficient systems. This strategy, though, leads to a reduction of supply voltages in circuits. Yet technology does not rely only on digital systems.

Although the digital plane is the most widely used in processes, analog solutions are still quite attractive mainly for 2 reasons:

- Analog designs are quite useful and efficient for low precision systems [2, 29]
- The analog circuits work naturally as 'buffers' between the natural world and the digital one that seeks to process it(Figure 1.1). Analog circuits such as filters, converters and amplifiers are and will be used for acquiring and preparing the data coming from the outside world for digital processing[25].

A good example of such applications, relying in analog circuitry, are wireless communication systems that would include devices needing analog-to-digital conversions and back and communications devices, such as mobile phones.[18] For these reasons efficient analog designs are important for complete systems-on-chip, if it is to keep the costs as low as possible.An additional problem would also be the shortage in analog engineers despite the importance of the field.The digital design is not really affected by the current trends lowering the supply values but for the analog designer makes it quite hard to design high performance circuits.One of the main difficulties to be analyzed are constraints issued by the reduction of the breakdown voltages ,stemming from the lower supply voltages and sizes. It greatly affects the design complexity because of:

- The faster scaling of the maximum voltage swing in comparison to the supply voltage reduction.[4]
- The ability to stack transistors is limited , limiting the architectural options of a system.
- The lower inversion coefficient achievable because of the smaller channel length and gate override voltage.[5]

These can affect the transistor's correct operation, distortion and although some of them can be overcome(by increasing the transistor length for example) some remain and such strategies can only be done in low frequency operations. Furthermore usually designs demand the explicit use of active components.

The most used component in analog circuits is that of the operational amplifier.

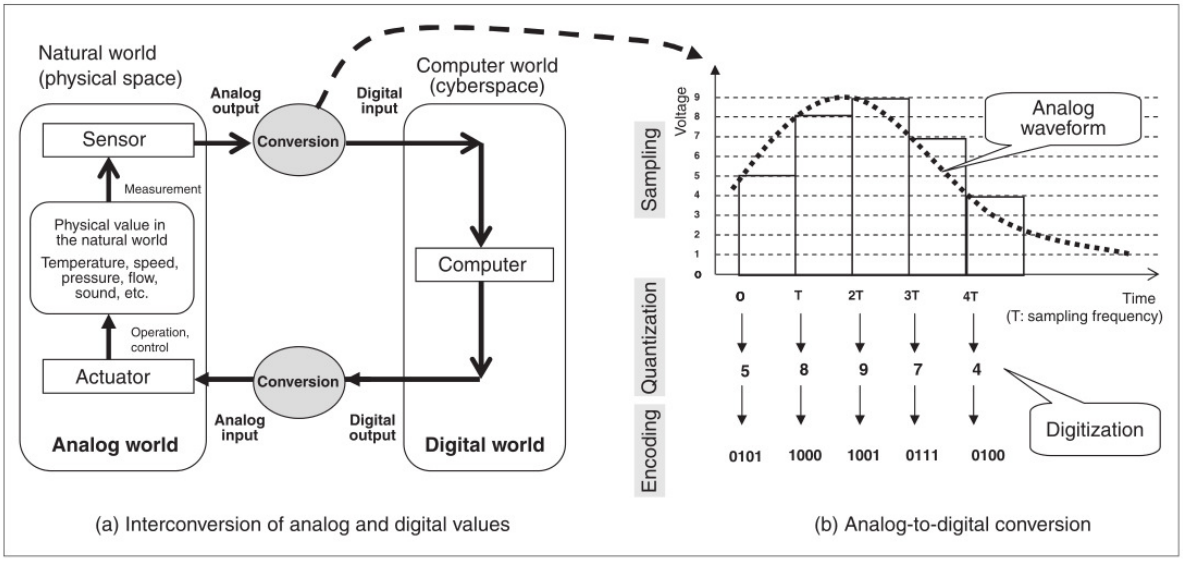

Figure 1.1: Interconversion of analog and digital values [18]

For applications needing high gains the bandwidth of an operational amplifier is limited. This, alongside the limited slew rate, affects high frequency operation. So in applications that high frequency and wide bandwidth are required simultaneously with the low voltage requirement, because of the transistor sizes, complex solutions are needed. This would also increase the power consumption. These facts indicate that new techniques are needed to overcome the consequences resulting from the technology trends that typical strategies cannot always cope with.

1.1 Thesis Motivation

Based on what was described, solutions are needed that could simplify circuits designs in these new circumstances. On straightforward solution would be to use current signal for processing instead of voltages, as it was proposed with the first current conveyors(Figure 1.2). In other words to use current mode devices. This procedure has the ability to create simpler realizations of working circuits. First of all MOS transistors are mode suitable to process currents than voltages because:

- Typical configurations have suitable current outputs
- MOS current mirrors are more accurate and less sensitive to process variations

In more detail common source and common gate configuration have current outputs making them suitable for current mode circuits while the common drain amplifier is practically useless in low voltages because of the bulk effect, making it an unsuitable option when such a requirement is present. Also MOS current mirrors are more accurate compared to bipolar circuits because of the presence of the base current in the latter. Plus they are less sensitive to process variations than bipolar processes and so it

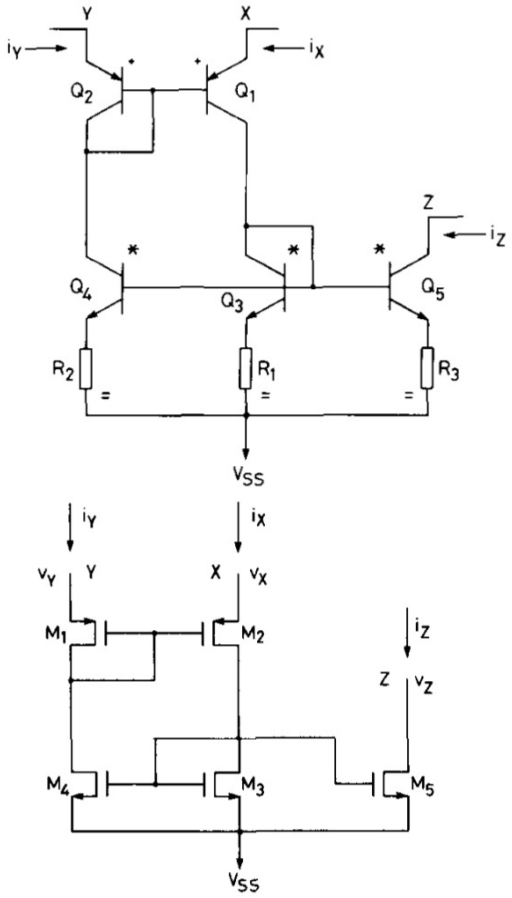

Figure 1.2: The first Current Conveyors in bipolar and MOS transistor implementations [23]

is possible that migrations from voltage to current processes would keep MOS circuits simple.

An additional issue that would make the usage of current instead of voltage a good idea, would be the parasitic capacitances' influence in each case. When using voltage signals one pays the price of full voltage swing charging/discharging the parasitic capacitances leading to higher power consumption and limited speed. In current mode devices , though, the circuits processes the current signals variations and can avoid some of the voltages swing.Still high voltage swing cannot be avoided completely but it has the potential to be smaller and localized.As a result current mode circuits have the potential of greater speed and better efficiency when it comes to dynamic power consumption.

In particular when transistors work in the saturation region the voltages are proportional to the square root of the current signal in MOS and to the log of the signal in Bipolar transistors. This makes the reduction of the voltage swing possible when using current mode solutions. This is already used in some cases. This advantage , on the other hand, created some issues that could balance out the benefit in some cases. Device

mis-matches can create more distortion. This non-linear behavior is problematic when hard linear requirements are present. In such cases additional circuitry is required to linearized the device balancing out the voltage swing benefit of the current signal usage.

Of course there are also more drawbacks in the simple idea of using current mode circuits. The voltage swing reductions make the devices more sensitive to mis matches leading influencing correct functionality. Also some of the solutions need extra bipolar structures to function properly in a complete system that have high supply voltages in applications requiring batteries, balancing out the power consumption benefit. Also many techniques are actually very old and can only be used as part of voltage mode processing devices instead of a pure current mode device. Lastly on some applications that off chip impedance levels are fixed such techniques can only be used on-chip for signal processing. Such an example would be applications using radio frequencies. Despite these issues the needs coming for the reduction of supply voltages still make the current mode option an attractive alternative to be considered.

1.2 Problem Statement

One of the most important application field in analog design is filters. So here as in other devices the size reduction trends have created needs for low supply and power devices. So the use of current mode alternatives can be applicable.

A main building block of filter circuits is often a integrator circuit. Typically, in voltage mode circuits , they are made using Operational Amplifiers alongside with passive components.So a good bet on managing to create current mode alternatives is to use integrators created by current mode circuits. In this thesis we explore 2 kind of design strategies:

- Gm(or OTA) based integrators
- Integrator equivalents based on current mode operational amplifiers.

One design strategy that could be used is the Gm-C (or OTA) approach. Here passive and active components are used to create a Transconductance Amplifier (or alternatively OTA) as the main amplification element. Transconductors are essentially a Voltage Control Current Sources(VCCS) that can operate in both voltage and current mode relatively similarly and are quite suitable for high frequency operations. So one could use current-to-voltage and Gm structures to process current signals and implement integrators using current as inputs(Figure 1.3). This is one strategy that its implementation would be interesting to investigate in sub-micron technologies.

The other strategy is to use current mode operational amplifiers. These are essentially current control current sources(CCCS) operating similarly to its voltage mode counterpart just with current as the processed signal (Figure 1.4). Using such circuits allows us to directly implement integrator designs, and thus filters, using voltage mode OpAmps designs with little architectural change.

Filters operating in high frequencies seem to present more difficulties since in voltage mode they tend to require higher supply voltages. Thus such filters are a good candidate

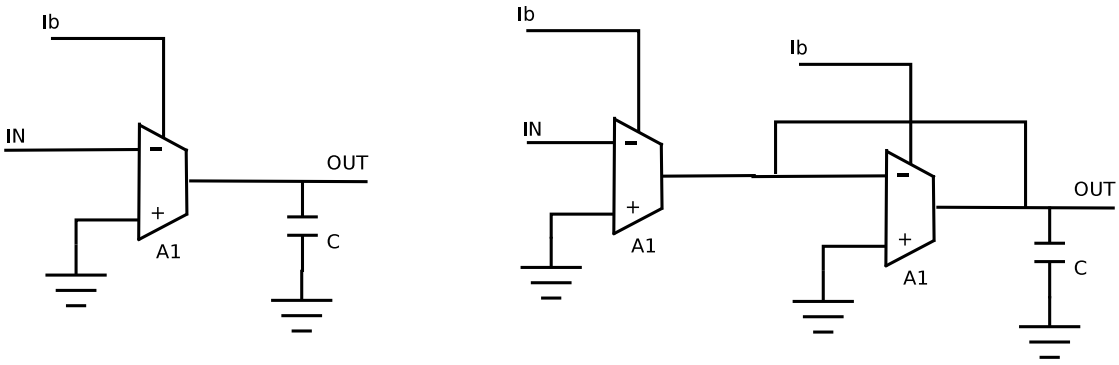

Figure 1.3: OTA integrator examples

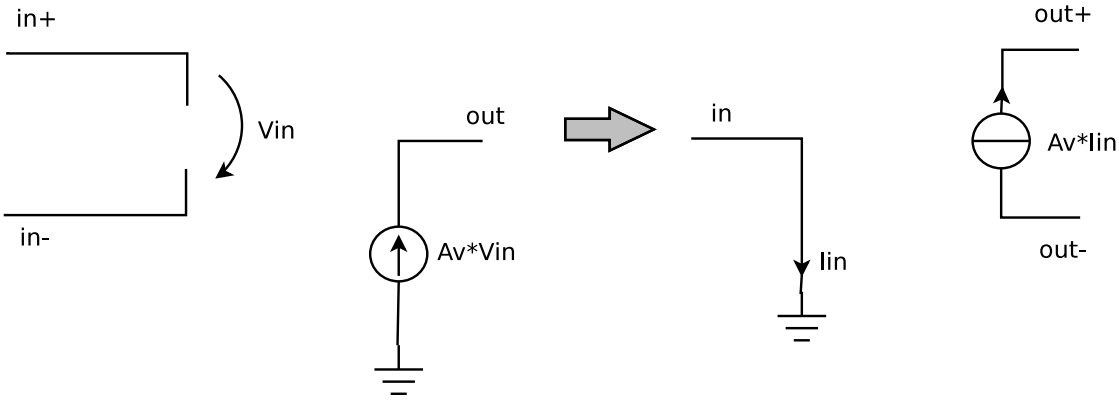

Figure 1.4: Voltage mode and Current Mode operational Amplifiers functionality

for the 2 design strategies, especially if one considers that OTAs are ideal for high frequencies. In this work we shall explore a high frequency filter design implemented in 0.25um transistor technology to prove the applicability of the current mode paradigm in such sizes and voltage supplies using both the Gm-C and CM OpAmps as main building blocks and produce designs to minimize the supply voltages and thus power consumption.

1.3 Thesis Goals

This thesis seeks to make the following contributions:

- Use a high frequency filter design to implement with current mode circuits that can exploit some of the benefits of the strategy.
- Implement the circuit using the Gm-C paradigm that uses Transconductors as main amplifier blocks for its integrators on 0.25um transistor technology. Gm-C filters are ideal for high frequency filters.
- Implement the same filter design using integrator equivalent structures using the CM operational amplifiers as their main building block that makes the migration

from voltage to current mode design straightforward.

- Choose transistor new sizes using the Inversion Coefficient (IC) as the main parameter to minimize the supply voltages and improve behavior of the circuits.
- Analyze the operation and performance of the resulting designs.

1.4 Thesis Overview

This thesis is organized as follows.In chapter 2 some related work is presented that refer to filter designs and evolution and history of current mode circuits used to cope with the technology trends. In chapter 3 some background knowledge is presented that is required to follow the reminder of this thesis. In chapter 4 the filter type used is described alongside its implementations using the Gm-C strategy and the CM Operational amplifiers, the IC calculation, IC analysis and the re-designing of the filters by choosing new transistor sizes, chosen according to the ICs to achieve minimum supply voltages and more optimal operation. Chapter 5 is dedicated to presenting the behavior and performance results for all filters implemented. Finally chapter 5 presents the conclusions, based on the evaluation of the results and also some future work suggestions.

Related Work 2

In the previous chapter the motivations and goals of this thesis were presented. Current mode approaches have a long history. The idea of using current signals for processing was firstly considered in the end of the 60s with the creation of the current conveyor with the purpose of correct voltage-to-current conversion.Since then there was a variety of such solutions developed for many applications, including , of course, filter applications. This chapter will try to present some of these researches.

The chapter is organized as follows.In the first section the first current mode solutions are presented that are a part of the history and evolution of the approach.These include implementations for current conveyors, integrators and CM Operational Amplifiers.(Figure 2.1) In the second section the same solutions are presented especially in the filtering field. In more detail the subject covered are some research examples on Gm-C filters,current mode based filters, switch current filters and log domain filters. Finally a summary of the chapter is provided in the last section.

2.1 Current Mode Designs

The approach of current mode applications was first considered in 1968. It was introduced as a solution of creating a more linear and precise circuits to create a suitable voltage-to-current converter.

The current conveyor is a 3-port device[22]. It has the ability to force the voltages and currents in the 2 inputs to become equal and creates a replica of the current in the 3rd input. This makes it useful not only for its initial use but also as a general building block.These applications, besides the initial one, included digital-to-analog conversion and dc offset control. The researches also considered a number of other applications to prove its worth as a building block for analog designs.

What they came up with was a number of possible applications and the 2nd generation current conveyor.[24] The first implemetation had 2 low impedance inputs. As a result very careful grounding was needed, if only one input was used, while it was also unsuitable for applications needing high impedance inputs. Thus the new design had one low and one high impedance input. Thus one input could be used as a high impedance voltage input, the other as both current and voltage input, while the output remained a current. There were also 2 types of designs. A positive one where the current input and output had the same direction and the negative that had opposite directions.As a result , between the 2 versions of the device, a number of current mode application were presented such as integrators, differentiators, amplifiers etc. Moreover applications were presented for voltage or current sources, either voltage or current controlled. The concept unfortunately coincided with the introduction of the integrated voltage mode operational amplifier that became the main building block for analog devices and was

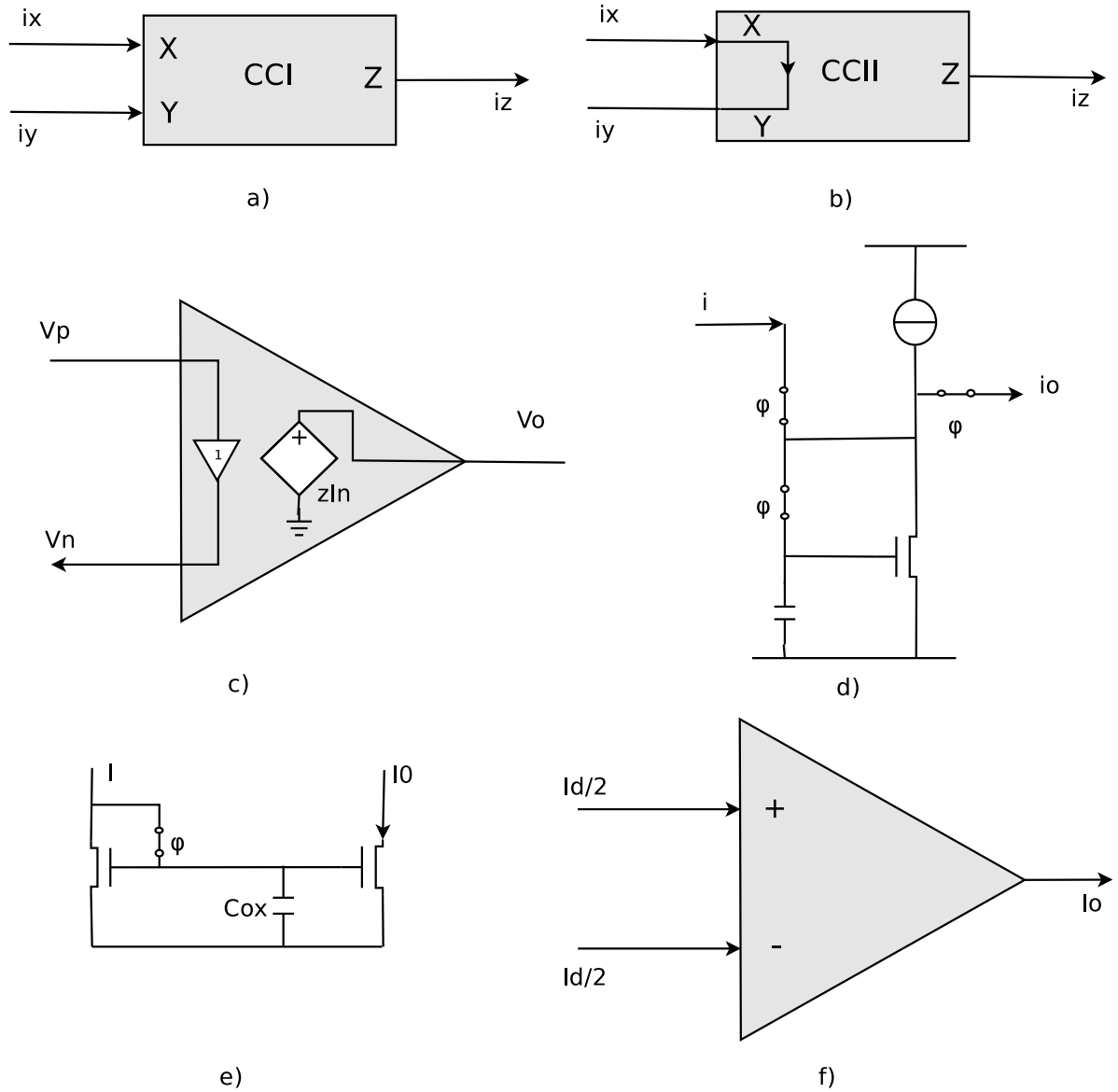

Figure 2.1: Current Mode Device Examples.a)Current Conveyor. b)2nd generation Current Conveyor. c)Current Feedback Operational Amplifier. d)Switched Current memory cell. e)2nd generation switch current, current store f)Current mode OpAmp.

not made very popular. An other reason was the technology limitations of the time that made the designs difficult to realize.

In the 1980s with new technology trends and the beginning of the realization that the typical OpAmp cannot not always be the optimal solution in some cases, the use of current conveyors and the current mode circuits approach, in general, was revisited.One interesting result was the current feedback operational amplifier, which also became a commercial product.[6] This circuit is different to the typical Opamp because of 2 aspects:

- The input stage is actually a voltage buffer with unity gain and practically forcing one input the follow the other.
- The amplification is done by a trans-conductor sensing the buffer current and providing the respective voltage output.

The current feedback operational amplifier boasts the advantage of high slew rate and wide bandwidth and was used mainly in video amplifier applications.

A large step was the creation of current mode designs in MOS technology. One interesting result was the MOS current copier that achieved the use of mos-only analog circuit processing sampled data.[7]

In 1989 the switched current strategy was introduced.It is a current mode equivalent of the switched capacitor principle for the voltage mode designs. There the voltage sample signals are processed according to an algorithm given by linear difference equations. In the switched current the same manipulation is done in current signals.The strategy could be used to create delay circuits, current memories and even integrators[10] Later the second generation of switch current filters were presented. This generation wished to solve the problems the initial idea had when it came to transistor mismatches. Also the initial designs had a problem when the clock frequency of the system was much higher than the cut-off frequency in filters.[12] Eventually for the memory cell created with this technique an alternative strategy was proposed to reduce precision and linearity issues, present with the previous strategies. These issues were solved with a 2 step sampling process that adds up resulting error and incorporates a detection and suppression of combined error.[11]

Lastly an important step was the design of current mode operational amplifiers. Such an example is proposed by Eric Bruun in [3].Here we have a single ended input differential output CM OpAmp.It was made by a combination of a 2nd generation current conveyor and a current source output stage. The design boasts high speed and gain of 94db. The supply of the design and power consumption was low taking advantage of the current mode technique.It was implemented at a commercial transistor technology for the time, that of 2um. An even more interesting proposal for a current mode operational amplifier is that of [32]. Here we have a direct equivalent of the voltage mode OpAmp. A differential input , single output design. The operation and design follows the ideas of the typical OpAmp including an input gain part, a current-to-voltage gain level and the output structure producing the current output of the OpAmp. The design boasts high gain, but the most interesting aspect is the easy duplication of its output that make it quite useful in translating the filters to the current mode principle. This will be discussed further later on as this design is chosen for one of the filter implementations in this thesis.

2.2 Filter Designs

In this part we will present a number of previous works on filter designs. Filters can be separated into 2 types:

- Sample Data Filters

- Continuous Time Filters

Sample Data Filters,such as switched current and capacitor filters, boast high performance and programmability. From some occasions continuous time filters have the advantage. First of all they can operate at high frequencies with the absence of a clock that would otherwise be needed and have a frequency higher that the bandwidth of the signals processed. Also in CT filters, since there is no sampling, there is no aliasing that can be a problem when using sampled signals. Their main disadvantages are, on the other hand, that they are temperature dependent and are not that precise.

In the rest if this section we present some examples of 4 design principles for filter design:

- Switch Current Filters
- Filters Based on Current Mirrors
- Gm-C Filters
- Log Domain Filters

2.2.1 Switch Current Filters

One of the main devices achieved with switch current principle is that of an integrator. With this, direct implemetation of filters can be done by translating the switch capacitor designs to this principle. As an example in [10] the authors created a 6th order Chebyshev low pass filter. To simulate the resulting design they used a in-house CAD tool designed for switch capacitor filters and used the models and ideal components.The end filter had a 0.5db ripple and a cut off frequency of 1MHz. The device operated with a 10MHz clock frequency. Later in [12] the 2nd generation of the design strategy was presented, coping with the disadvantages of the method.This leads to a redesigning of the universal integrator of the previous work. The new filter designs derived directly translated by the switch capacitor model. The new design was again a 6th order Chebyshev low pass filter with 5MHz cut off frequency and a operating clock of 20MHz.

2.2.2 Filters Based on Current Mirrors

After the introduction of sampled data filters using the current mode approach, devices using the continuous time filter principle based on current mirrors were also developed.

One such research has resulted in the creation of filter examples using simple current mode structures for their implementations, having advantages on high frequencies to their respective voltage mode designs. Specifically the method uses current mirrors and single driver transistors to operate as transconductor elements.[20]. The implemented design was a passband filter with high quality factor and a frequency up to 20MHz (Figure 2.2).

Other works that can be noted are [16] and [26].In the first paper the integrators for the filters are using a prototype differential current integrator based on current mirrors.

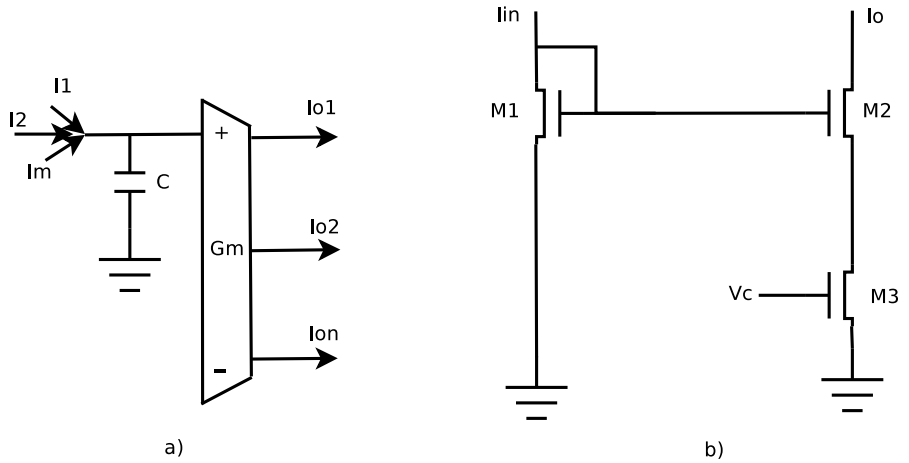

Figure 2.2: Circuits examples presented in [20].a)Current transconductance integrator. b)Programmable current mirror

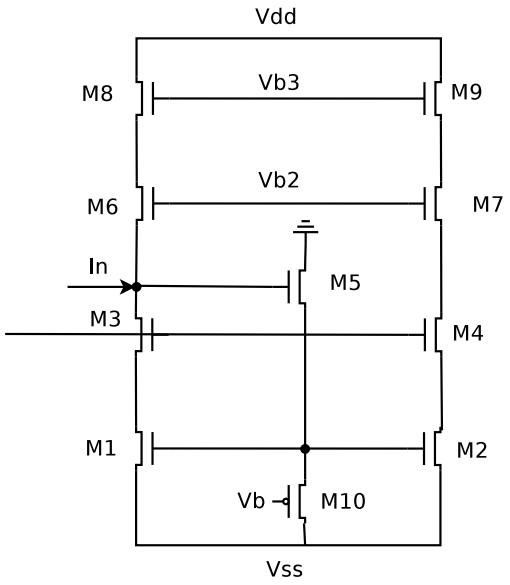

Figure 2.3: Current Amplifier used for integrator design in [16]

The experimental device was implemented in 2um technology and was a 5th order ladder low pass elliptical filter (Figure 2.3). It had a frequency of 42MHz and was tunable from 24-42MHz though adjusting the respective bias current. The filter was operating on 5V supply.In the 2nd paper a differential current mode integrator based on current mirrors is also targeted at high frequency filters. The integrators were designed to achieve high speeds and low distortion.The end filter had a frequency range from 7 to 13MHz and a supply voltage of 3.3V.

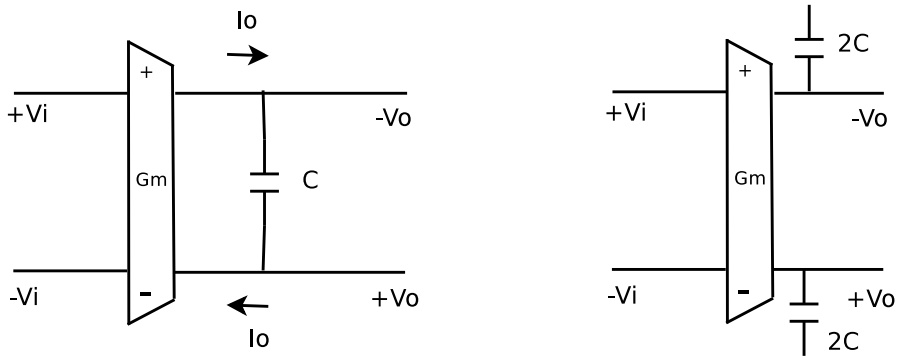

Figure 2.4: Gm-C integrator examples

2.2.3 Gm-C Filters

In the Gm-C filter principle, as mentioned previously, filters are made with the integrators consisted of a transconductor and one or two capacitors (Figure 2.4). It produces an output current of value Io = Gm*Vi. So it is essentially a Voltage Control Current Source (VCCS) [28]. This strategy is widely used in filter designs.[12] Basically the technique could be also using an Operational Transconductance Amplifier in the same model although it is not exactly the same type of device. Yet for this reason OTA-C filters using the same ideas are referred often as Gm-C filter and visa-versa.Operating in high frequencies the techniques are suitable for both current and voltage mode operations with little change. Such filter designs have,on the other hand, linearization problems that can lead to distortions problems, often leading to additional linearization techniques to compensate.

Initially in the sub-micron technology the supply voltages were around 5 volts such as in [27] where a 7 MHz low pass filter was implemented suitable for video frequency applications.Some other examples are proposed in [15] with a 20MHz Bassel filter and in [1] that a 2nd order low pass filter is implemented with a 2um technology. Further research has achieved reduction in the supply voltages. One such example is a tunable filter based on a tunable transconductor achieving a frequency of 5.5MHz in 3.3V of supply voltage [17].In 1996 a new transconductor was developed boasting high linearity and low voltage supply. The device was presented in an implementation of a 7th order Bessel filter with a 600KHz cut off frequency and 2.5V in supply voltage [30].Lastly there are also the cases of a low pass and a band pass tunable filters of [31]. Here the filters work with a 1.5V supply and have a tunable cut off frequency of 300kHz-1MHz.

Dominique Python in [19] has also proposed 2 Gm-filter designs with reduced supply voltage. The first filter is a Gm-C filter using complementary transistors. This way the design used the current reuse principle and reduced power consumption at a cost in accuracy. This technique has the demand that transconductance in the complementary devices is very well matched, that for complementary circuits can be a problem. This is addressed with a dedicated circuit to ensure the matching in transconductance. The end circuit has a voltage swing of 1V and a supply voltage of 2.5V. The final filter is a low frequency low pass filter in 0.25um technology with a cut off frequency of 70KHz.The

second filter implemented in the same reasearch was characterized as a pseudo-differential filter, meaning that single ended structures processed one half of a differential signal. The supply voltage targeted was very low so no linearization structures could be added.The end result was a 100kHz 5th order Bessel filter running with 1V supply voltage with small power consumption and area.

2.2.4 Log Domain Filters

The idea of log domain filters was proposed by Adams. The principle was that one can use the logarithm of a linear signal to process it and derive the logarithm of the filtered linear signal, only through diodes, capacitors, current sources and OpAmps. Then one can derive the linear filtered signal by the one in the log domain. By processing in the log domain designers can make filter frequency tunable for more decades since the log signal is more compressed than its linear counterpart. The log domain approach can only be implemented in current mode since a logarithmically compressed voltage is not an accurate representation of the original linear one, unlike current signals.

One of the first notable uses of the log domain approach we can see in [8] where we have an implementation a 7th order Chebyshev low pass filter to demonstrate the method. The filter was tested in several frequencies to prove the fact that it can be tuned accurately over a wide range due to the log domain processing.

An interesting filter implementation is also presented in [19] . The filter here is realized in a pseudo-differential structure using single ended integrators. The filter is a Butterworth 2nd order filter implemented in 0.35um technology. Its nominal cut off frequency is at 4KHz and operated in supply voltage of 1.5V. The testing of the circuit gave very promising results and also revealed some of the problems on the principle such as the device's sensitivity to mismatches and general non-idealities of the transistors, the impracticality of strong inversion operation and parasitic capacitances among others.

2.3 Summary

In this chapter we presented a number of previous works concerning current mode designs and filter implementations created using various design principles.The Current Mode designs references covered the basic history and evolution of the current mode paradigm.This begins with the 1st and 2nd generation of current conveyors and goes all the way until the switch current and current OpAmp implementations.Later this chapter presents some filter designs developed under 4 design strategies: switch current, current mirror based filters, Gm-C and log domain filters. All useful principles on current mode filter design.In the next chapter some of the basic theoretical background is presented, needed for the remainder on this thesis.

3 Background

In the previous chapters the motivation and characteristics of current mode design and filter design,in particular, was discussed. Later a number of previous research was shown using the current mode paradigm and also a number of design principles for filters alongside with them. There are a number of design notions that are needed to comprehend this field of applications. This chapter has the purpose of presenting some of these basic notions and thus also help in the comprehension of the rest of this document.

The chapter is organized as follows.In the first section a brief presentation of the Operational Amplifier, or OpAmp, will take place. The OpAmp is one of the basic design blocks in analog design and in filter design especially. The current mode counterpart has also a similar behavior to the traditional one. Later will follow an explanation of how integrators and differentiators are created using OpAmps and specifically the RC-integrator and Differentiator which will be used in the later filter design. In the next section the current mirror circuit will be briefly explained, useful for the design in many circuits, including transconductors and OpAmps. Then we shall also refer to the adjoint principle which is an easy way to translate voltage mode circuits to current mode counterparts. Finally the chapter will end with a summary of the subjects discussed.

3.1 The Operational Amplifier

Negative feedback is the process of connecting the output of a structure to the input to cancel out some of the input. This does practically lower gain, in case of circuits, but gives the network wanted characteristics such as linearity, cancellation of noise and predictability. If the network is chosen correctly one can even end up with a circuit that its behavior is only dependent on the network itself. The operational amplifier is one building block that is used more often with a negative feedback.

An operational amplifier is essentially a differential input single output amplifier working as a voltage controlled voltage source (Figure 3.1). The ideal OpAmp has some certain characteristics:

- Infinite Input Impedance
- Zero Output Impedance
- Infinite Voltage Gain
- Zero Common Mode Voltage Gain
- Zero output voltage when input voltages are equal
- Infinite slew rate (instant output changes).

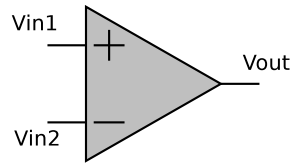

Figure 3.1: The Operational Amplifier

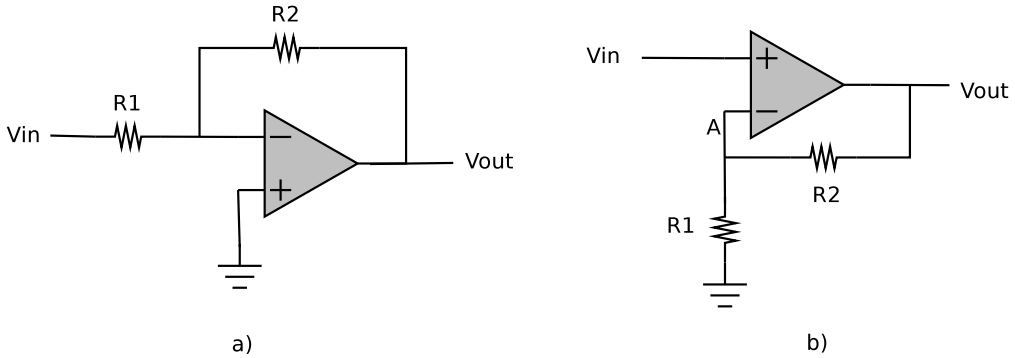

Figure 3.2: The inverting and non-inverting amplifier

A simpler way to predict OpAmp behavior is to use the golden rules as stated in [9]:

- *The output attempts to do whatever is necessary to keep the voltage difference between the two inputs zero.*The inputs of course do not change but what is happening is that the amplifier has the necessary output to cancel out the input difference through the negative feedback.
- *The inputs do not draw any currents.*

Based on these rules many useful topologies can be described using the OpAmp.Most common are the inverting and the non inverting amplifiers.

3.1.1 The Inverting Amplifier

This topology involves a negative feedback from the output to the negative input and the positive input connected to the ground (Figure 3.2a).Since the the positive input is connected to the ground and so the other input is a virtual ground also. As a result the voltage in R_2 is V_{out} and in R_1 is V_{in}.Since inputs do not draw any current we have:

I_2 = -I_1 which is equal to

V_{out}/R_2 = -V_{in}/R_1 and so:

Gain = V_{out}/V_{in} = -R_2/R_1

When a positive voltage is given in the input there is a voltage difference with the input connected to the ground. This pushes the output to a negative voltage becoming low enough to cancel the voltage in the inverting (negative) input. The voltage needed for this cancellation is analogous to the R_2/R_1 ratio.Input impedance is equal R_1 and the output impedance is very low. This network works also as a dc amplifier so if someone is interested for the ac signals it is a good idea to use a blocking capacitor to block the dc signals.This is the inverting amplifier. It has one major disadvantage is the low input impedance since in many amplifiers the input load tends to be low and could create problems in functionality.

3.1.2 The non-Inverting Amplifier

A different amplifier network that copes with the problem of the low input impedance is the non-Inverting Amplifier. Here instead of giving the voltage input in the inverting input, we issue the voltage in the in non-inverting input (Figure 3.2b). Since we have:

$V_A = V_{in}$

Because of the voltage divider:
$V_A = V_{out} * R_1/(R_1 + R_2)$

By setting $V_A = V_{in}$ the gain is :

G = $V_{out}/V_{in} = 1 + R_2/R_1$

In this case the input impedance is very high(theoretically infinite) while the output impedance is still kept very low. This is still also a dc amplifier so a blocking capacitor with a resistor in parallel with an escape to the ground must be placed in the voltage input if the input source is ac-coupled. Here also if only ac signals are needed then a blocking capacitor can be used. An alternative to this would be to just raise the value of the resistor. The capacitor values can be kept relatively low since the current in the input that is needed to escape is relatively low.

3.1.3 Other Typical Networks

There are a number of other simple uses for the OpAmp. Some more examples are the usage as a Follower, a current source, a differential amplifier and a summing amplifier (Figure 3.3). The voltage follower is practically a non-inverting amplifier with infinite resistor values. When the follower has unity gain is called a buffer since it has the infinite input and zero output impedance and so it practically isolates input and output.On other possibility is the creation of current source. The one depicted in the figure produces a current equal to I = V_{in}/R. One problem here is that the load is not connected to the ground that could create limitations. When circumstance allows one

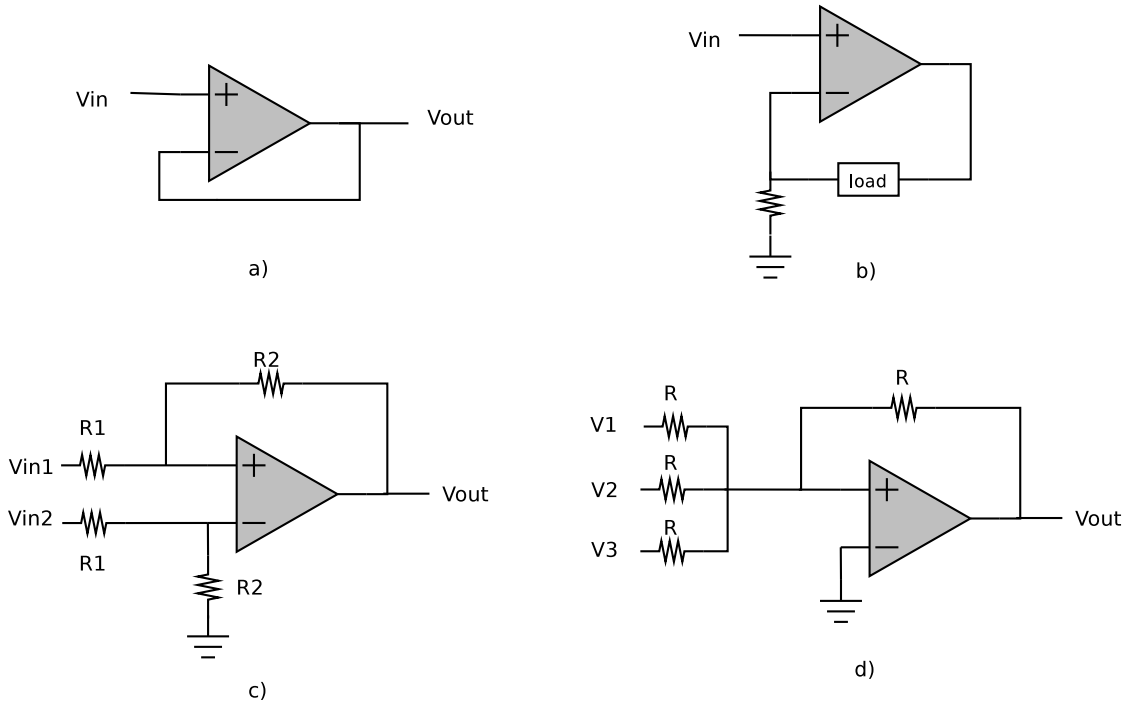

Figure 3.3: OpAmp Typical Networks: a) Follower. b) Current Source. c) Differential Amplifier. d) Summing Amplifier

could use a design that all elements are "floating" and connecting the load to the ground to cope with the problem.Lastly typical applications are differential and summing amplifiers. The example of the differential amplifier produces an output of :

$$V_{out} = \frac{R_2}{R_1}(V_2 - V_1) \tag{3.1}$$

The summing amplifier is a variation of the inverting amplifier that the input voltage is provided by separate nodes. As seen in the figure and with the inverting amplifier in mind the input current is:

$$\frac{V_1}{R} + \frac{V_3}{R} + \frac{V_3}{R} \tag{3.2}$$

Which results to output voltage of :

$$V_{out} = -(V_1 + V_2 + V_3) \tag{3.3}$$

The resistors do not have to be equal. If not the resulting voltage will be a weighted sum of the initial voltages according to the resistor values.

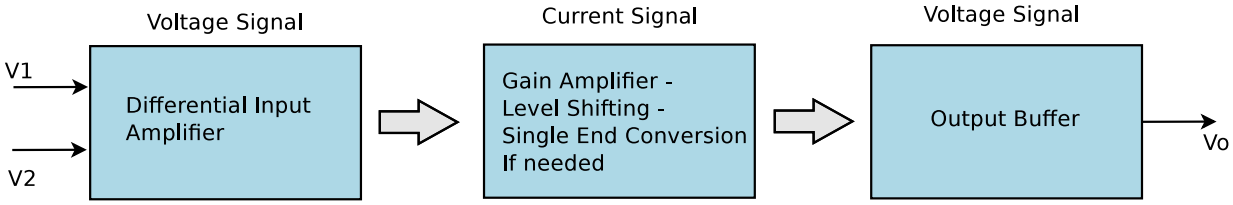

Figure 3.4: OpAmp 3 Stage Structure

3.1.4 The Real Life (non-ideal) OpAmp

It is natural that the ideal OpAmp is not achievable. A non-ideal OpAmp only comes close to the ideal characteristics.The various non-ideal factors of a real OpAmp are:

- *Finite Gain*: Real OpAmps have finite voltage gain. Typically practical designs try to have high gain to achieve behavior as close as possible to the ideal.
- *Limited Linear Range*: The gain of the OpAmp is actually linear only in a part of the output voltage values.
- *Common-Mode Rejection Ratio or CMRR*: This ratio measures the ability of the OpAmp to reject common mode signals, that usually represent noise.
- *A Frequency Response*: The non-ideal circuit has its gain reduced at high frequencies.
- *Limited Slew Rate*: Although the ideal version changes its output instantly, the real life counterpart changes in a finite rate, represented by the slew rate.
- *Non-zero output impedance*
- *Noise*: Transistors generate noise. This adds a noise voltage offset to the output of the amplifier.
- *Dynamic Range*: Because if the non-linear gain behavior there is a maximum input signal that the amplifier can use without generating forbidding amount of distortion
- *Power Supply Rejection Ratio or PSRR*: A power supply also generates noise. This noise will create an additional voltage added the the Amp's output. The ratio measures the ability of the OpAmp to suppress this noise.

To accomplish a near as possible performance to the ideal OpAmp there is a general template when one designs an Operational Amplifier. It is basically comprised by three blocks (Figure 3.4). The first block is a differential amplifier stage. It is designed for providing high input impedance high CMRR and PSRR, low offset voltage and noise and provide the gain for the OpAm. It is a good idea that its output is single ended, to reduce complexity in the next stage but it is not obligatory.The second block is used typically for level shifting and adding additional gain to achieve high general gain. In the circuits

that the first stage's output remains differential it is here also that the differential-to-single ended conversion is done. The third stage is the output buffer. This stage provides the amplifier the low output impedance and high current needed if the OpAmp needs to drive a heavy load, as it is the case in some applications like filters. It is typical, but not necessary, that the output buffer does not provide any additional gain to the amplifier.

3.2 The RC Integrator

A basic block in filter design, as previously mentioned, are integrators. An integrator is a circuit that its output is a function of the integral of the input.

The passive circuit integrator can be realized with a resistor and a capacitor (Figure 3.5) .In this circuit the voltage in R is V_{in} - V. According to this the current running through the R and C is:

$$I = C\frac{dV}{dt} = \frac{V_{in} - V}{R} \tag{3.4}$$

If V is much smaller that V_{in} we can consider $V_{in} - V \approx V_{in}$. So:

$$C\frac{dV}{dt} = \frac{V_{in}}{R} \tag{3.5}$$

Hence :

$$V = V_{out} = \frac{1}{RC}\int V_{in}dt + C \tag{3.6}$$

Using Operational Amplifiers we can create active integrator without the $V_{in} - V \approx V_{in}$ approximation.These are called RC integrators since they use resistors and capacitors in the Amplifier network (Figure 3.6). As before $I_R = I_C$. Hence:

$$I_R = \frac{V_{in}}{R} = I_C = -C\frac{dV_{out}}{dt} \tag{3.7}$$

From here we can derive the output which is:

$$V_{out} = -\frac{1}{RC}\int V_{in}dt + C \tag{3.8}$$

Using the Laplace transformation here we can also derive the transfer function or in other words the gain of the integrator:

$$V_{out}(s) = \frac{-V_{in}(s)}{sRC} => \tag{3.9}$$

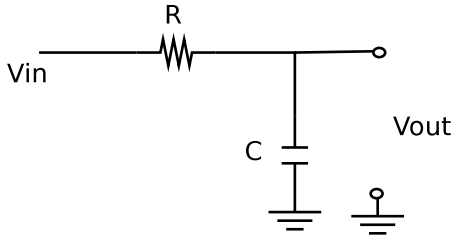

Figure 3.5: Passive Integrator

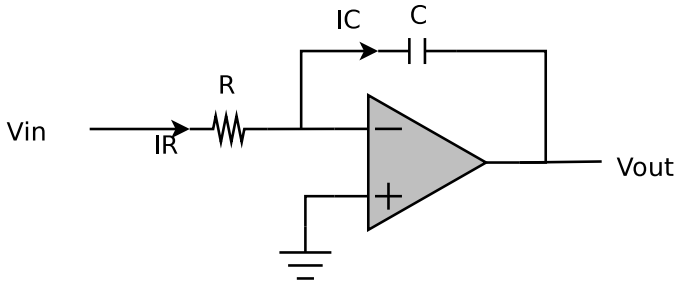

Figure 3.6: Active RC Integrator

$$G(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{1/RC}{s} \tag{3.10}$$

The integrator behaves in terms of frequency as a first order low-pass filter.Other uses of the integrator, besides filter design, include applications in in control systems, feedbacks, analog-to-digital conversion and waveform generation.

3.3 The RC Differentiator

Another useful design block in applications is the differentiator. Here the output is a function of the derivative of the input.

The passive circuit integrator can be realized with a resistor and a capacitor (Figure 3.7). Here the voltage in C is V_{in} - V. According to this the current running through the R and C is:

$$I = C\frac{d(V_{in} - V)}{dt} = \frac{V}{R} \tag{3.11}$$

If dV_{in}/dt is much larger than dV/dt then we can assume :

$$C\frac{dV_{in}}{dt} = \frac{V}{R} \tag{3.12}$$

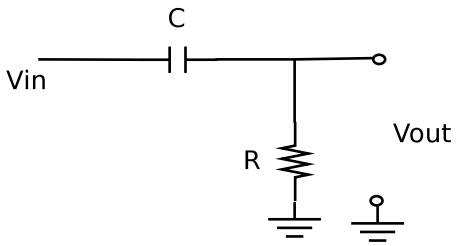

Figure 3.7: Passive Differentiator

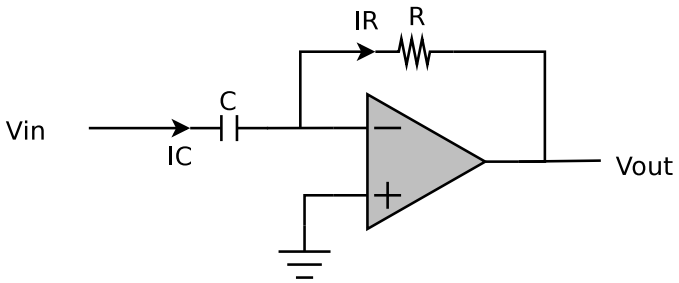

Figure 3.8: Active RC Differentiator

So :

$$V = V_{out} = RC\frac{dV_{in}}{dt} \tag{3.13}$$

This can also be realized with an operational amplifier using RC elements without the approximation (Figure 3.8). As before the currents running though the R and C are equal and so:

$$I_C = C\frac{dV_{in}}{dt} = I_R = \frac{V_{out}}{R} \tag{3.14}$$

Hence :

$$V_{out} = RC\frac{dV_{in}}{dt} \tag{3.15}$$

The differentiator in the frequency domain operates as a first order high-pass filter. Except its usage in the analog domain this circuit is also useful in digital application ,such as in applications needing to detect leading and trailing edges of pulse signals.

3.4 The Current Mirror

In many occasions in analog circuits we need to use constant multiples of existing currents for various applications, like device biasing and current gain amplifiers etc. One of the

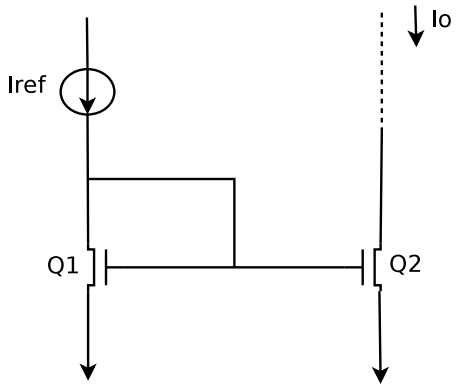

Figure 3.9: The Simple Current Mirror

most important building block is that of the current mirror. The current mirror uses an input current reference and produces a current output that is the initial current(so it mirrors the reference current) multiplied by a factor defined by the mirror's architecture.

The simplest form of a current mirror is using two transistors. If one uses MOSFETS the transistors have their gate connected and the first transistor's(Q1) drain is also connected to its gate (Figure 3.9). The devices should be of the same technology, meaning having the same threshold voltage (V_t). The mirror's current gain is dependent on the transistor ratios.

More specifically if I_{ref} is the circuit input then it is equal to :

$$I_{ref} = K_1(V_{GS} - V_t) \tag{3.16}$$

Where K_1 is the equal to $\mu_1 C_{ox}$

Respectively if we consider the ideal infinite impedance of Q_2 then I_0 is also :

$$I_0 = K_2(V_{GS} - V_t) \tag{3.17}$$

So we can derive that :

$$\frac{I_{ref}}{K_1} = \frac{I_0}{K_2} \tag{3.18}$$

Hence:

$$I_0 = I_{ref}\frac{K_2}{K_1} \tag{3.19}$$

The ratio K_2/K_1 is actually equal to $\frac{(W/L)_2}{(W/L)_1}$. So in conclusion the mirror output is:

$$I_0 = I_{ref}\frac{(W/L)_2}{(W/L)_1} \tag{3.20}$$

If we consider the non-ideal characteristics then (3.20) is only true when the V_{GS} is equal to V_{DS}. In other circumstances, because of the finite impedance of Q_2, the current output will drift from theoretical value. The amount of this change depends on the current mirror's output resistance. In this case the output impedance is equal to the resistance of Q_2

3.4.1 Typical Ways To Increase Output Impedance

Naturally the higher an output impedance is achieved in a current mirror the more it comes near to the theoretical behavior. The are a few simple ways to do this. Two straight forward ways to do so are the source degenerate and cascode current mirror topologies.

The source degenerate approach has to to with inserting a resistor in the sources of both transistors in the simple current mirror circuit (Figure 3.10). If we produce the small signal model of the topology we can derive the total output impedance of the current mirror. This time is not longer equal to the impedance of Q_2 but equal to:

$$R_{out} = r_{ds2}(1 + R_S(g_{m2} + g_{ds2})) \tag{3.21}$$

If we consider that g_{ds2} is actually $g_m = 1/r_s$, which is by far less than the g_m, R_{out} is approximately equal to :

$$R_{out} = r_{ds2}(1 + R_S g_{m2}) \tag{3.22}$$

So as a result of the insertion of the 2 resistors in the simple topology, the output impedance is multiplied by a factor of (1+ $R_S g_{m2}$)

An other way to increase the output resistance of the current mirror is the cascode current mirror topology (Figure 3.11). This topology can increase the output resistance much higher than the source degenerate technique.Here instead of inserting resistor in the sources of the current mirror we insert two additional transistors connected also with the simple current mirror topology. Here the output node is the collector of Q_4. If we consider Q_2 as a resistor like we did in the source degenerate example we can use (3.21) to calculate the output impedance:

$$R_{out} = r_{ds4}(1 + r_{ds4}(g_{m4} + g_{s4} + g_{ds4})) \tag{3.23}$$

Hence:

$$R_{out} = r_{ds4}(1 + r_{ds4}(g_{m4} + g_{s4} + g_{ds4})) =>$$

$$R_{out} = r_{ds4}(1 + r_{ds4}(g_{m4} + g_{s4})) =>$$

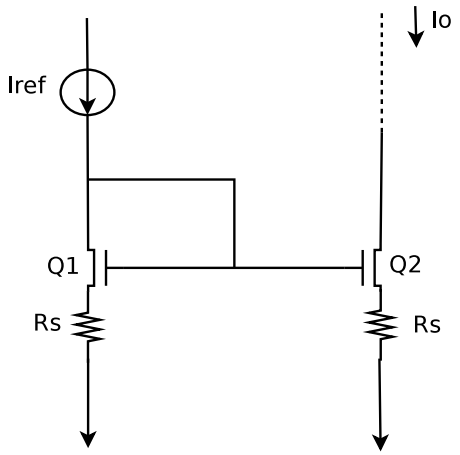

Figure 3.10: Source Degenerate Current Mirror

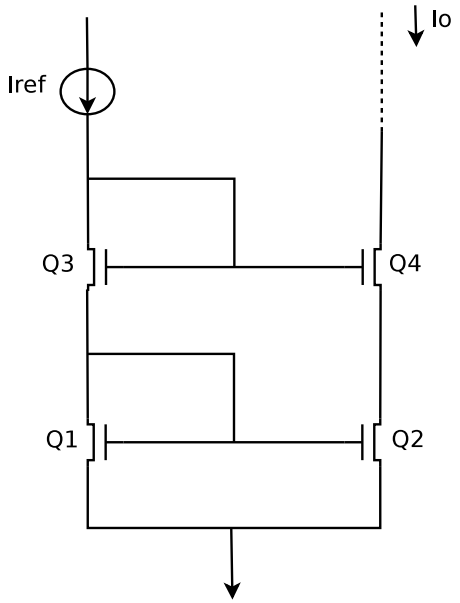

Figure 3.11: Cascode Current Mirror

$$R_{out} = r_{ds4}(1 + r_{ds4}g_{m4}) =>$$

$$R_{out} = r_{ds4}(r_{ds4}(g_{m4}) => \tag{3.24}$$

considering that g_{ds4} and g_{s4} are much lower than g_{m4} and the factor $r_{ds4}g_{m4}$ is larger than 1.

So in this case the increase in the output impedance is by a factor of $(r_{ds4}(g_{m4})$ which is usually between 10 and 100 and significantly larger that in the source degeneration

and it is dependent on the transistor sizes. An increase that it is required in a number of applications. like high gain amplifiers.

This topology has one major disadvantage. It has limited output signal range if the transistors are not in the triode region , which is often the case. Because of the cascode topology and the demand that V_{DS} must be higher than V_{eff} for the transistors to be in the saturation region a lower limit of the output voltage for the transistors to work in the saturation region is created. This can be a problem if the application technology works in voltages less than 3 volts, which is the case with the sub-micron technology. For this reason there are a number of improvements to these circuits than cope with problem. Such examples are Wilson mirrors and wide-swing cascode current mirrors.

3.5 The Adjoint Principle

The Adjoint Principle exists to make current mode design easier. There already is a number of designs and strategies that exist in the voltage domain. A straightforward way to design current mode circuits is to translate the existing voltage circuits to a current mode counterpart, instead of designing the circuits from scratch. This is the purpose of the Adjoint Principle. It contains a set of rules to translate voltage amplifiers and passive components to the respective current amplifiers and passive components that have the same signal behavior.

The ideal voltage amplifier has infinite input impedance and zero output impedance. The opposite is true for a current amplifier. So direct replacement of the amplifier lead to incorrect behavior. According to the principle the voltage mode circuit can be translated into a current mode one by replacing the voltage mode network according to the principle rules and changing the input voltage node into the current response and the voltage response node into the current input of the network (Figure 3.12).Simply put the input becomes the output and visa-versa [21]. This will lead to a network with exactly the same transfer function:

$$H_v(s) = \frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} = H_i(s) \tag{3.25}$$

The N and N_a network are characterized as inter-reciprocal to one another. If the network are actually identical they are reciprocal. This happens with purely passive circuit. Passive elements are inter-reciprocal to each other meaning that they have themselves as their adjoint counterpart. If it is for the transfer function to remain the same then the impedance level to both the original network and its adjoint counterpart must be identical. Hence the signal flow must be reversed and a voltage sensing element is changed to a current source. In the same way a voltage source is converted to a current sensing element. Each type of element can be transformed in a similar way. Some examples can be seen in Figure 3.13.

With the same principle controlled sources can also be converted. Reversing the signal flow and maintaining the impedance levels the same. A voltage amplifier is converted to a current amplifier and visa-versa though the principle. Trans-resistance and

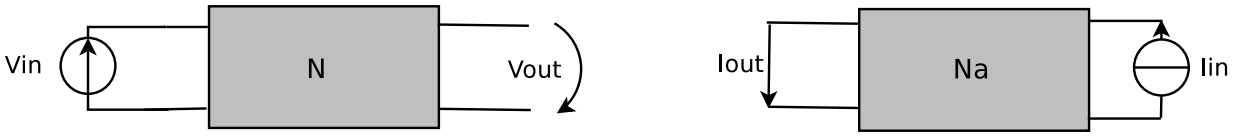

Figure 3.12: Network conversion according to the adjoint principle

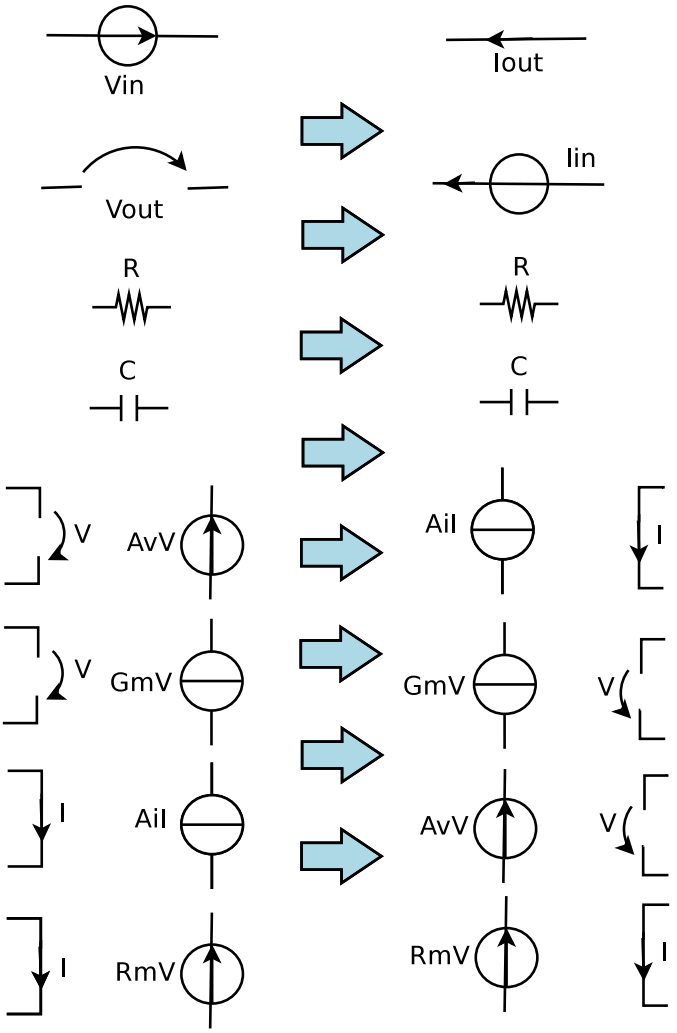

Figure 3.13: Circuit elements and their adjoint counterparts

transconductance amplifiers, are in the other hand, inter-reciprocal and in such networks conversion of the signal flow and type is only needed.

Finally the adjoint principle is also suitable for current mode conversion even in transistor level. So for example a bipolar common emitter configuration is inter-reciprocal to itself, while a common collector configuration is converted to common base.There is also the option when converting a bipolar circuits to also convert the transistors to MOSFET ones. It can greatly improve low voltage operation since less source follower circuits are

needed with MOSFET, that are greatly affected by the bulk effect. The common collector and common emitter amplifier stages are converted to common gate and common source topologies for their current mode counterparts with MOSFET transistors.

3.6 Summary

In this chapter we explained some basic theoretical foundations required for the reading of this work. In the beginning the ideal and non-ideal OpAmp's basic characteristics were presented alongside with some basic uses, highlighting its functionality.In the later sections the integrator and differentiator circuits were discussed and also their RC implementations using Operational Amplifiers. Then we referred to one of the most basic building block in analog design, that of the current mirror and some of its different simple implementations. Finally an easy way of translating voltage mode circuits directly into current mode circuits, while maintaining the transfer function of the original network the same, the Adjoint Principle. In the next chapter we shall present the filter design used for this thesis, the 2 versions of it we implemented using Gm-C integrators and current mode OpAmps and the IC analysis used to suitably choose the transistor sizes of our implementations.

4 Filter Implementations

As mentioned before the purpose of this thesis is to implemented high frequency low-pass filter realizations in the current mode strategy. The design chosen was a 3rd order low-pass elliptical filter. Two realizations of the filter were implemented. One using the Gm-C paradigm, as previously designed and implemented in 1.2um technology but now with a 0.25um process.The second realization uses current mode operational amplifiers. The implemetation was done by the direct translation of the voltage mode circuit of the original ladder design using OpAmps. The main design choices would be the correct choice of the CM OpAmp and the translation of the voltage mode design to the current mode aspect to achieve similar frequency behavior in the new circuit. Finally we seek to optimize the designs by using the Inversion Coefficient(IC) as the main design parameter to judge the new transistor sizes.

The rest of the chapter is organized as follows. In the first section we have a presentation of the ladder filter used in our implemetation and how it is normally implemented in the voltage case using voltage mode OpAmps. Next we present the first implementation of the filter design, initially proposed by Koli and Halonen, implemented in the newer 0.25um technology.In the next section the second filter design is described, based on a Current Mode Operational Amplifier.Then we develop the method of acquiring the parameters needed for the IC analysis for our designs and its results. According to the IC of the filters' initial design, the transistor sizes are updated seeking to make the designs more efficient. The updated designs are then presented. Finally a small summary of the chapter is provided.

4.1 The Low-pass Elliptical Filter

Ladder filters are a typical way of filter design.They are passive prototypes in use from the beginning of last century. The total impedance, characterizing the filter behavior, is a combination of sections comprised of components in series and in parallel to the input and output ports of the complete network. The network usually resembles a ladder, hence the name ladder filters. The idea is to translate the passive filter realizations through the voltage and current Kirchoff laws. The resulting equations can be used to implement the designs with active components. The method can be used for many types of filter implementations, including OpAmp integrator filters, switch capacitor, switch current filters and current mode filters.

Usually with correct feedbacks one can create the sums, stemming from the KCL and KVL applied in the passive circuit, and implement the factors in the s domain(bound to be present because of the C and L elements in the passive filter) using integrators. The method is straightforward and theoretically it can implement any high order filter circuits. The circuit used here is a low-pass third order elliptical filter. The passive

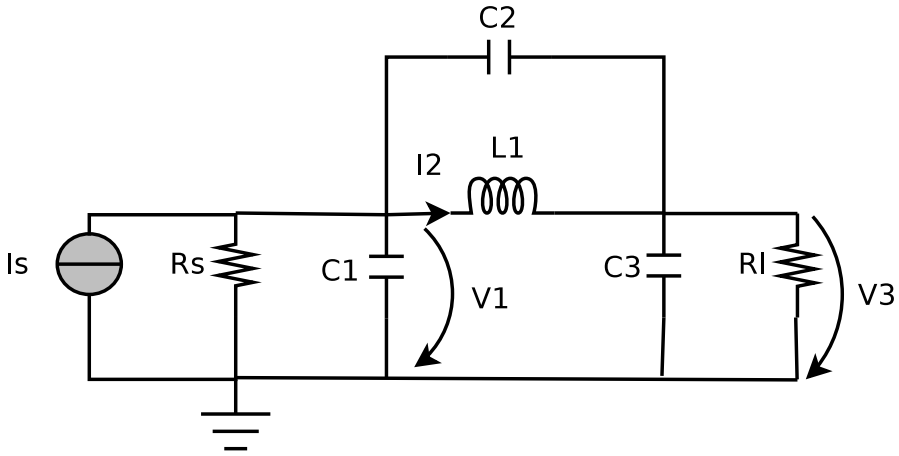

Figure 4.1: The Passive 3rd order low-pass elliptical filter

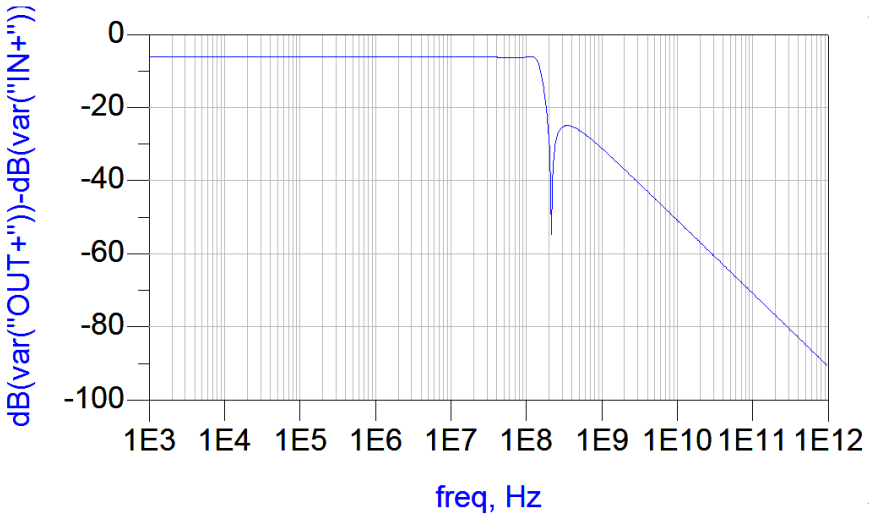

Figure 4.2: The Passive 3rd order 150 MHz low-pass elliptical filter frequency response

realization includes R,C and L elements. By keeping the source and load resistors at 1 ohm then the filter characteristics, mainly the ripple, cut-off frequency and attenuation node, are defined by the capacitor and L values.Basically in terms of operation the lower the L and C values are, the higher the cut off frequency of the filter. The circuit can be seen in Figure 4.1.The frequency response of a high frequency operating example for the passive circuit can be seen in Figure 4.2. If we use 1 ohm resistors, $C_1 = C_3 = 1.29nF$, $C_2 = 0.56nF$ and $L_1 = 0.98nH$, the resulting filter has a cut - off frequency of about 150MHz (Figure 4.2). In this circuit we apply KCL to calculate I_2 and the KVL to calculate V_1 and V_3 in the corresponding circuit nodes. By the KL we have:

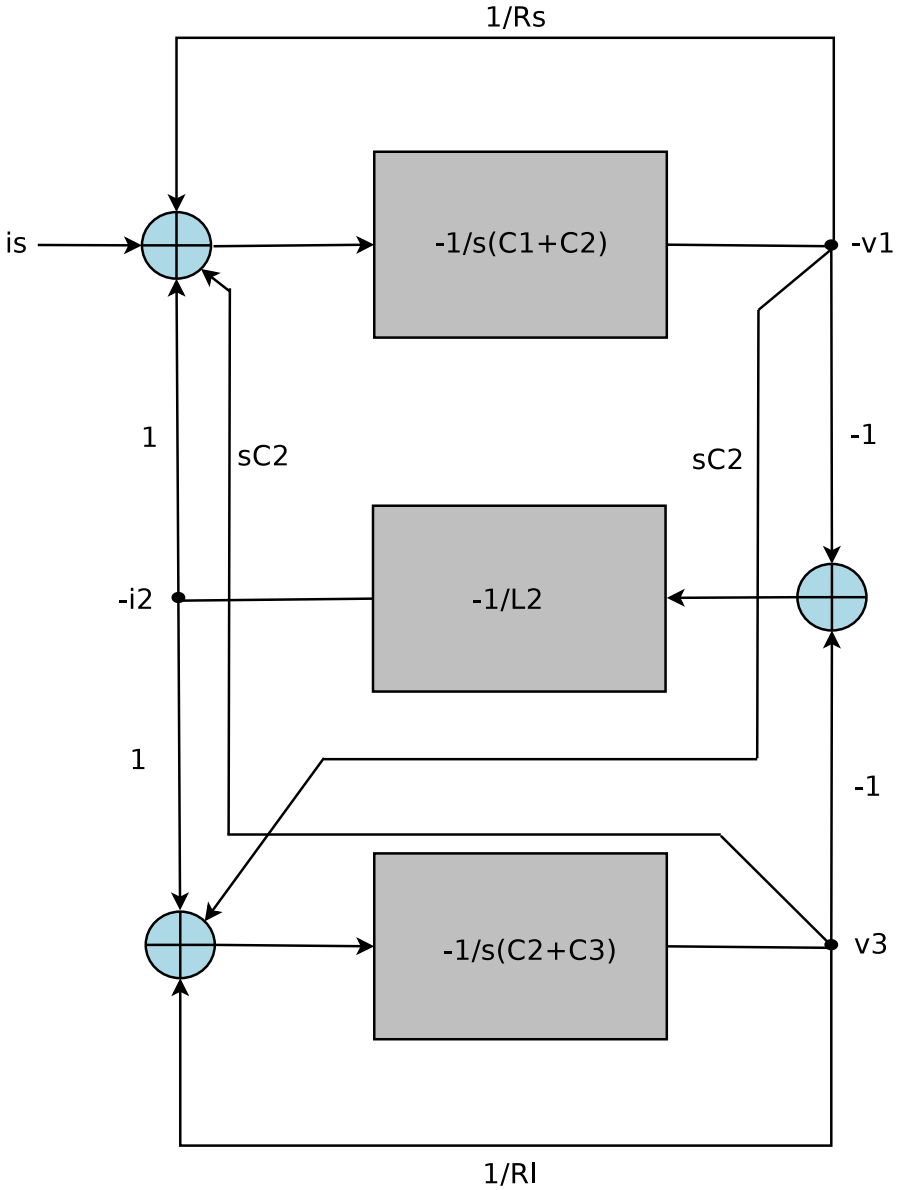

Figure 4.3: The filter Block Diagram as derived by KVL and KCL.

$$-V_1 = \frac{-1}{s(C_1 + C_2)}\left(\frac{V_{in} - V_1}{R_s} + sC_2V_3 - I_2\right) \tag{4.1}$$

$$-I_2 = \frac{-1}{sL_2}(V_1 - V_3) \tag{4.2}$$

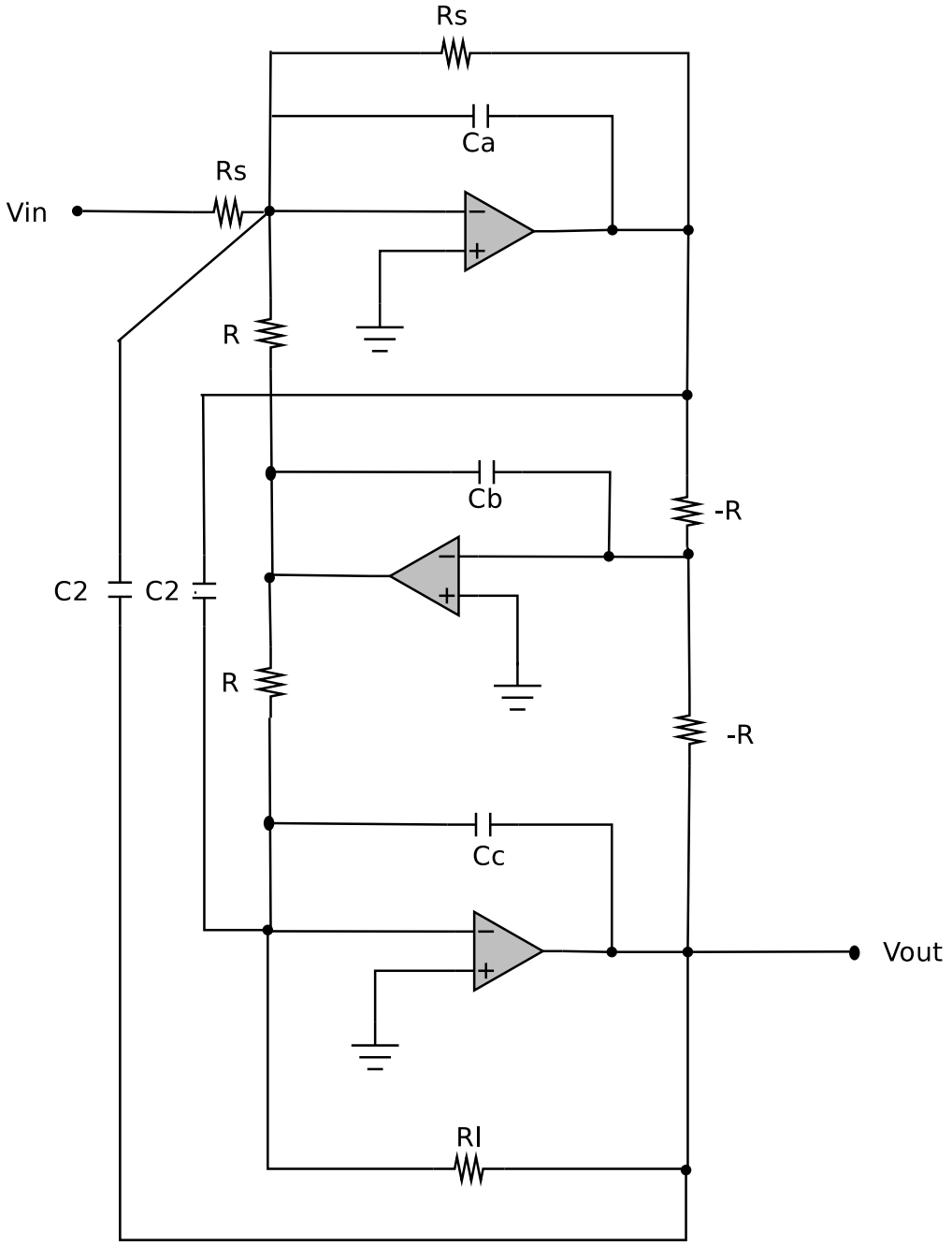

Figure 4.4: The active RC implementation of the elliptical filter, using OpAmps

$$-V_3 = \frac{-1}{s(C_2 + C_3)}(\frac{V_3}{R_L} - sC_2V_1 - I_2) \tag{4.3}$$

The V_1 can be derived by integrating the sum of $\frac{V_{in}-V_1}{R_s} + sC_2V_3 - I_2$ with the

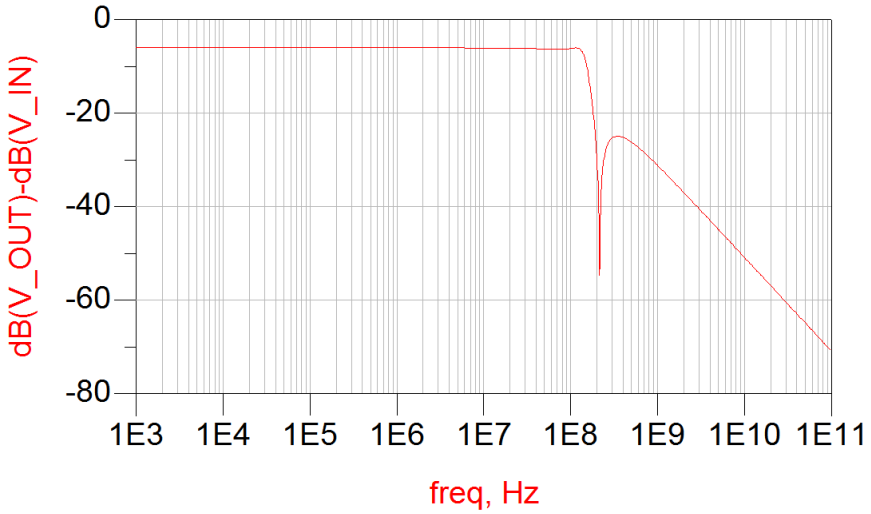

Figure 4.5: The active RC 3rd order 150 MHz low-pass elliptical filter frequency response

help of an inverting integrator providing the $\frac{-1}{s(C_1+C_2)}$ factor. Similarly the I_2 and V_3 by integrating the corresponding sum as seen in the KL equations integrated with the $\frac{-1}{sL_2}$ and $\frac{-1}{s(C_2+C_3)}$ factors. According to these we can now design the complete filter and produce the block diagram of its architecture.The filter block digram can be seen in Figure 4.3. From this block digram we can then derive an active implementation. A straight forward way of doing that would be to use RC - active integrators with their resistor at 1 ohm. Besides the classic RC integrator also a lossy version of the component can be used to incorporate the load and source resistor's influence. Yet if resistors of 1Ω are used the resistor are only useful to define current direction and the integration factors are derived by the capacitor values of the integrators, practically also defining filter behavior. Specifically the capacitance values are derived by the integration factors as seen in the block digram. The circuit using RC integrators can be seen in Figure 4.4.The element values for the equivalent filter are:

$$C_A = (C_1 + C_2)$$

$$C_B = \frac{L_2}{R^2} = L_2, for R = 1ohm$$

$$C_B = (C_3 + C_2)$$

Using the values as above we can derive the same 150MHz low pass filter. Its transfer function can be seen in Figure 4.5. From the active RC filter we can also derive other similar versions of the filter such as, the current mode counterparts. Two possible options

to create current mode filters similar to this voltage mode version would be to either produce new integrators that are inter-reciprocal and use them in a similar block diagram as the original or produce the inter-reciprocal circuits directly using the adjoint principle and current mode operational amplifier implementations.In the following sections we shall describe these implementations.

4.2 The Current Mode Gm-C implementation

As stated previously, Gm-C filters is a typical method for realizing current mode filters. The advantage,in our case, is that Gm topologies can be used as they are for both voltage mode and current mode implementations according to the Adjoint Principle. So by just changing the signal type and direction the resulting network has the same behavior in the frequency domain. The problem is that typical OTA structures don't really have any meaning and create design problems in the current mode paradigm. For example the resulting network in current form for the typical OTA has a single ended input and differential output. Moreover there is the problem of the output sharing, which is typical in ladder filter designs. To share a voltage output is straightforward and easy,but with current it is not the case. Unless you have a multiple output device one would need a different OTA structure for each direction a current output is needed. This problem was address by Koli and Halonen in [13], by a design of a multiple output integrator using a linearized multiple output transconductor with differential inputs and outputs. A filter using the ladder filter previously described was implemented in 1.2um technology to present the design. Our first implemetation is based on this filter design in 0.25um technology.

The researchers here try to find linearization techniques to implement the needed transconductors. Two techniques were basically considered:

- Linearization by Drain Current Difference
- Linearization by Dynamic Biasing

The design has some certain requirements. The circuits needs to have large voltage swing and be able to be scalable to easily replicate the current output for ladder filter implementations. One such linearization technique is the drain current difference that can be presented by a MOSFET pair with its sources connected to the ground(Figure 4.6). Here the pair is driven by a differential input and the drain current can be calculated as such:

$$V_{gs1} = \frac{V_d}{2} + V_{CM}$$

$$V_{gs2} = -\frac{V_d}{2} + V_{CM}$$

Hence if we consider that the MOS drain currents are :

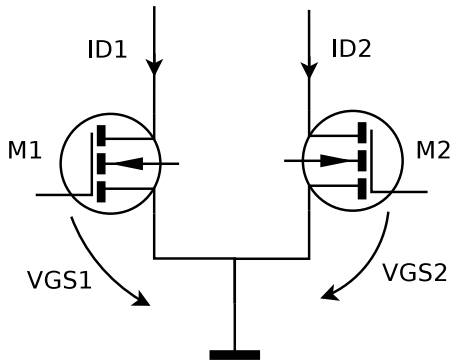

Figure 4.6: MOSFET pair presenting the Drain Current Difference linearization principle.

$$I_d = \frac{\beta}{2}(V_{gs} - V_T)^2 \tag{4.4}$$

Then the current difference is :

$$I_{D1} - I_{D2} = \beta V_d (V_{CM} - V_T) \tag{4.5}$$

A simple way to implement this is by a typical CMOS inverter. This design, though, has a couple of issues. First of all the transconductance is controlled by the supply voltage that can be difficult on some occasions. The second and more important issue it that the linearization can only happen theoretically in single ended circuits because of the parameter differences between PMOS and NMOS devices. So this was unsuitable for the integrator design.

What was implemented instead was linearization by dynamic biasing. The idea is to produce a bias current and subtracting it from the differential output, so that the resulting outputs are both linear.If the bias current produced is the average of the drain currents this can be possible. Such a bias current is equal to :

$$I_{DB} = \frac{I_{D1} - I_{D2}}{2} = \frac{\beta}{2}(V_{CM} - V_T)^2 + \frac{\beta}{8}V_d^2 \tag{4.6}$$

If this current is subtracted from the 2 outputs then the resulting output currents are:

$$I_{O+} = I_{D1} - I_{DB} = \frac{\beta}{2}V_d(V_{CM} - V_T) \tag{4.7}$$

$$I_{O-} = I_{D2} - I_{DB} = -\frac{\beta}{2}V_d(V_{CM} - V_T) \tag{4.8}$$

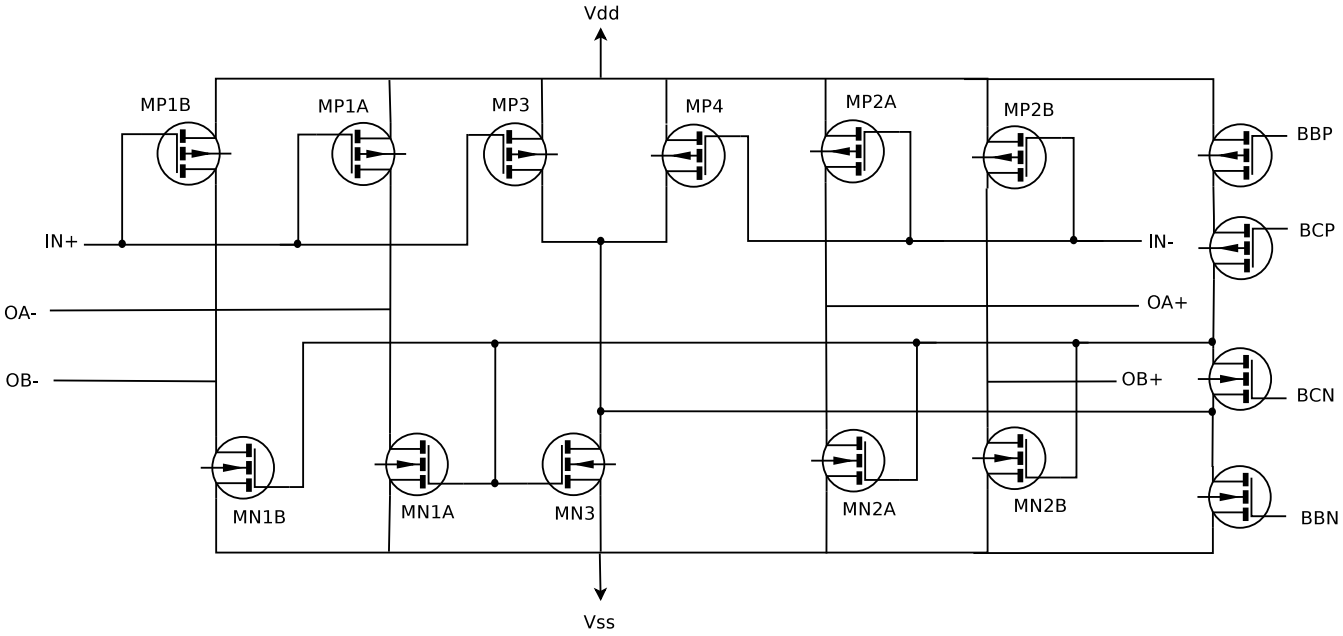

Figure 4.7: Linearized Transconductor implemented for the current mode Integrator design.

Ideally all additional non-linearities can be canceled out if the output is converted to single ended. The design should be affected by device mismatches in the biasing circuitry but distortion should be kept under control. The practical implementation uses PMOS differential pairs to produce the transconductance. An additional PMOS pair (MP3, MP4) generates the bias current. NMOS current mirrors can then be used with a 1/2 ratio to subtract the bias current from the output. By replicating the transconductance pair(MP1x, MP2x) and current mirror transistors(MN1x, MN2x) additional identical differential outputs can be produced(Figure 4.7). Using this transconductor, current mode integrators can be realized to implement the ladder filter.

From equation (4.6) it is apparent that the bias current is dependent on the voltage difference and the quiescent current depends on the common mode input voltage. Thus for the transconductor to sustain its linearity a stable differential input is required. For this reason the integrator also includes a driver amplifier providing stable and controlled voltage input to the transconductor according to the current input of the integrator. Finally to reduce the effect of channel length modulation, the common drain node between MP3,MP4 and MN3 is set to the same signal amplitude as the input of the driver amplifier(described below) by transistors MP5-6 and MN4-5.

The driver amplifier controls the quiescent current and transconductance of the transconductor by a common mode feedback loop and increases gain by providing high output impedance. The schematic of the driver can be seen in Figure 4.8. The high impedance is achieved by a cascode current source(MN1-MN4 and complementary ones). The common mode feedback loop is achieved by the double pair NMOS transistors MNC1-4, which senses the output of the driver and drive the feedback accordingly.

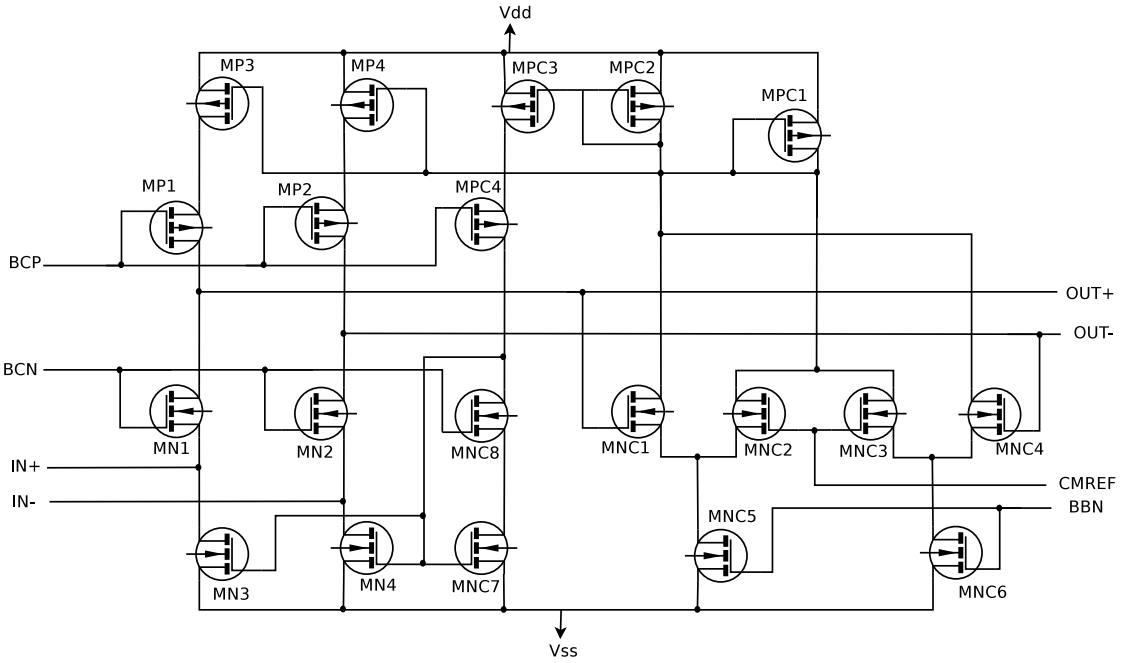

Figure 4.8: The driver amplifier.

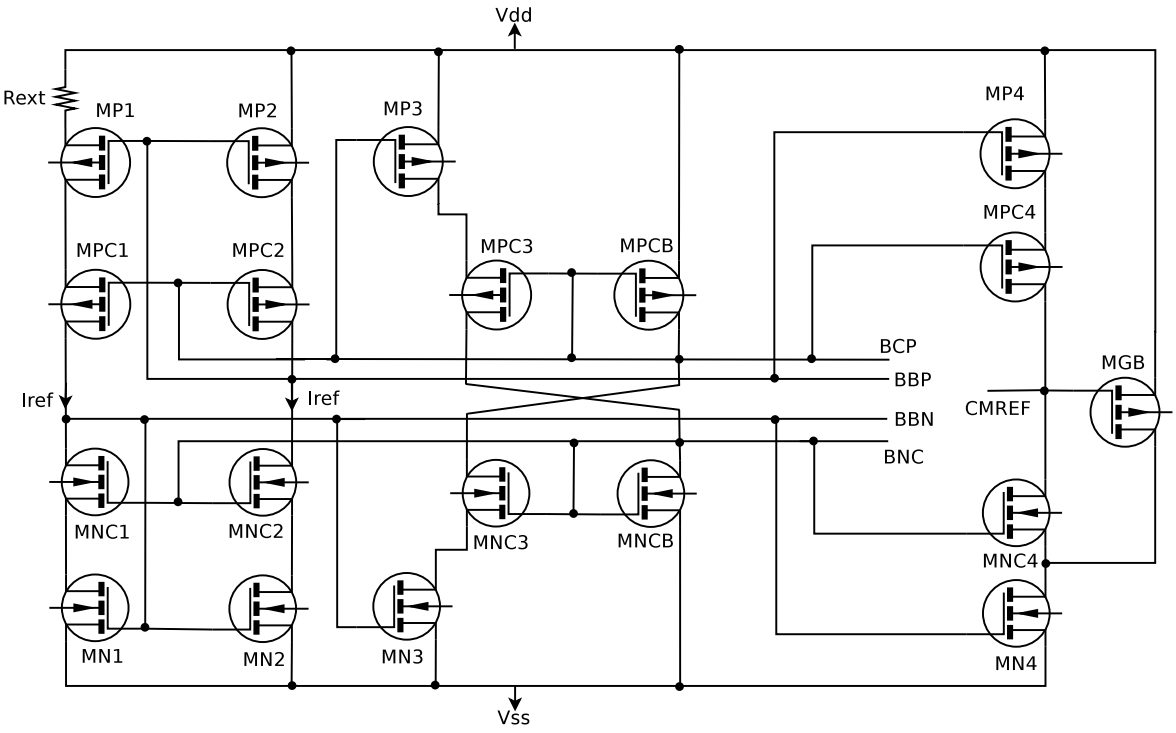

Figure 4.9: The current reference circuit.

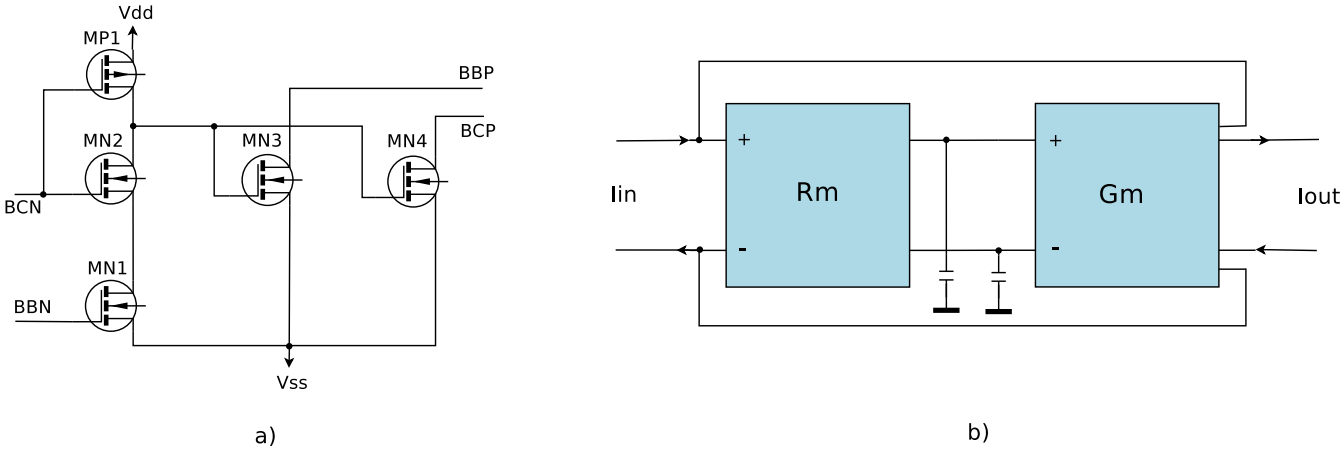

Figure 4.10: a) Start up circuit b) Gm current mode integrator.

In order to reduce sensitivity to supply voltage oscillations the drain currents of the feedback loop are mirrored symmetrically to the PMOS and NMOS section of the current amplifier. Transistors MNC7-8 and MPC1-4 are the ones that mirror the feedback output. Because of oscillation in the common mode feedback loop, that could create instabilities, grounded capacitors are required in the output of the driver to ensure a stable signal for the transconductor. Another way to prevent these oscillations is also to keep the sensing transistors' ratio relatively lower to the rest of the circuit to reduce its signal bandwidth. The integrator transconductance is tuned according to the CMREF voltage coming as input in the driver amplifier.

To produce the needed CMREF voltage a circuit is applied that gives the ability to use an external resistor in real life realization to tune the integrator(Figure 4.9). The idea is that the R_{ext} can be used to compensate for temperature variations by tuning it and always ensuring a stable reference voltage to the sensing circuit of the driver, ensuring also stable transconductance. This is done by a CMOS cascode current mirror. The NMOS part has an aspect ratio of 1 but the MP1-2 mirror ratio has a significantly larger ratio. The R_{ext} is then used to compensate to difference in ratio and produce 1 to 1 current reference. Thus by adjusting the resistor the reference current can be stable despite temperature variations. The reference current is then symmetrically converted to a voltage. To ensure that the DC - voltage would be similar in magnitude to the transconductor 's, 5 additional transistors are used to finally produce the sensing circuit control voltage(MP4,MPC4,MN4,MNC4,MGB).

Besides the stable point that creates a stable reference circuit, the reference circuit has also one other stable point. When all devices are off and no current passes. To prevent that from happening an extra small circuit is used to ensure that the reference current does not become zero(Figure 4.10a). Here MP1,MN2 and MN1 transistor take input in their gate the BBN and BCN voltages. When these voltage became too low the reference current shift towards lower values. If this happens the MN3 and MN4 transistor operate and increase the BBP and BCP current that end up in the PMOS mirrors in the current reference circuits. This increases the reference current as well as

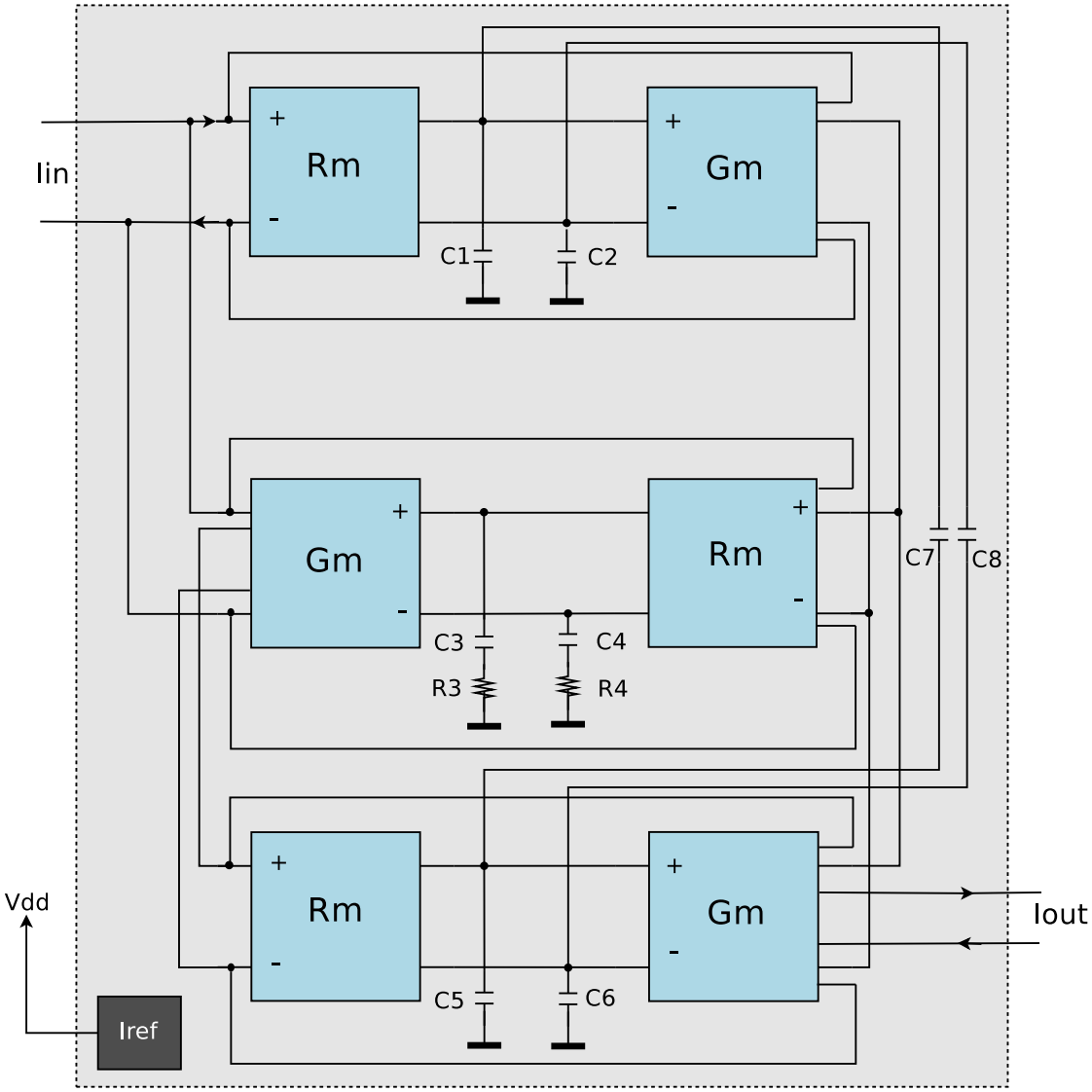

Figure 4.11: Gm current mode filter block diagram.

the BBN and BCN voltages. When they become high enough and no compensation is needed the start up circuit switches off.

The final integrator design includes the driver amplifier receiving differential current inputs and providing the transconductor with the suitable voltage inputs and resulting in the differential current output. The outputs are also used as feedback to the driver inputs(Figure 4.10b). Present, of course, are the current reference and start up circuits, which in the case of a design with more than one integrators, they can be shared between them, instead of having a replica for each integrator.Using this integrator design we can now implement ladder filters using the filter block diagrams as a guide. The block diagram of the filter produced by our original filter, as depicted in Figure 4.3, realized with these current mode integrators can be seen in Figure 4.11.In order to incorporate

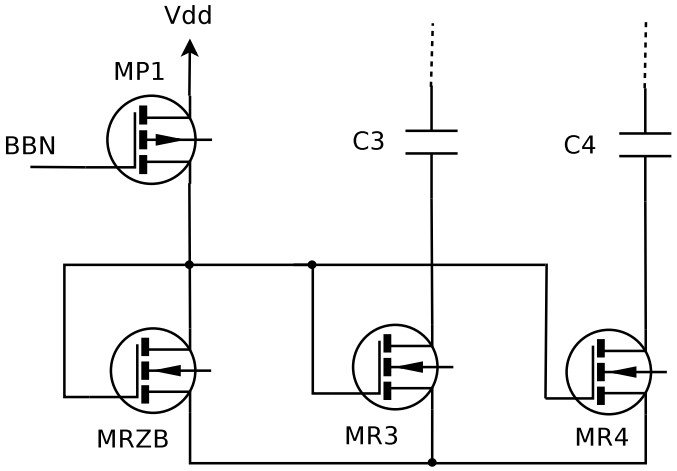

Figure 4.12: NMOS resistor circuit.

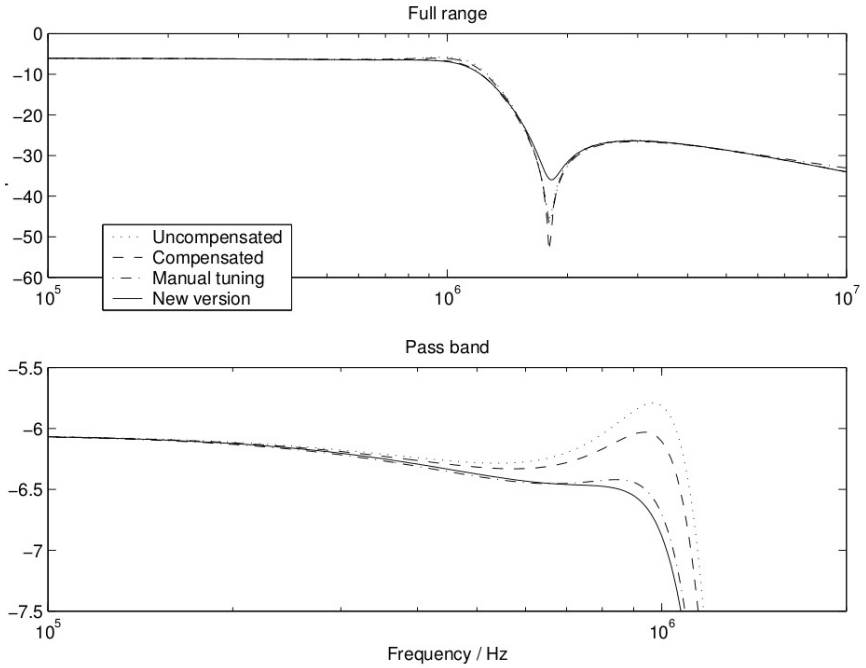

Figure 4.13: The 1.2um filter frequency response[14]

the multiple direction of the integrator outputs, the design utilizes two integrators with 2 identical differential outputs and one with 3 for the bottom integrating block.

To improve the quality factor for the filter one can add resistors in series to the integrating capacitors. This addition will reduce phase errors. Additionally since the second integrator (Figure 4.11) has a feedback loop to each of the other integrators, only resistors in middle are needed to reduce the errors.The resistors are implemented

Driver Transistors	Aspect Ratio um/um
MN1,MN2 and MNC8	20.8/0.25
MN4,MN3 and MNC5-7	5.2/0.63
MNC1-4	0.52/2.1
MP3,MP4 and MPC4	5.2/0.25
MP1,MP2 and MPC 1-3	5.2/0.63

Start up Transistors	Aspect Ratio um/um
MN1 and MN2	5.2/0.25
MN3 and MN4	0.52/0.83
MP1	0.52/4.2

Transconductor Transistors	Aspect Ratio um/um
MN1A-2B	6.25/0.63
MN3	12,5/0.63
MN4	2.6/0.63
MN6	10.4/0.25
MP1A-2B,MP3 and MP4	6.25/1.25
MP5	2.6/0.63
MP6	10.4/0.25

Current Reference Transistors	Aspect Ratio um/um
MN1-4	5.2/0.63
MNC1-3	5.2/0.25
MN4	2.6/0.63
MNC4	5.2/0.25
MNCB	0.83/0.63
MP1	28.6/0.63
MP2 and MP3	5.2/0.63
MPC1-3	5.2/0.25
MP4	2.6/0.63
MPC4	2.6/0.25
MPCB	1/0.63
MGB	6.25/1.25

Table 4.1: Gm-C Filter Transistors' new aspect ratios

with NMOS transistors. The control voltage for the transistor is generated by a diode-connected NMOS according the an internal reference signal (Figure 4.12). This method has the advantage that the MOS resistor is sensing variations (either from devices or temperature) and makes the filter less sensitive to them.

The filter the researchers created was implemented with a 1.2um technology. The simulated results show a 1MHz cut-off frequency.The passband ripple was calculated in simulation to be very small (although at the actual chip it was found about 0.6db).

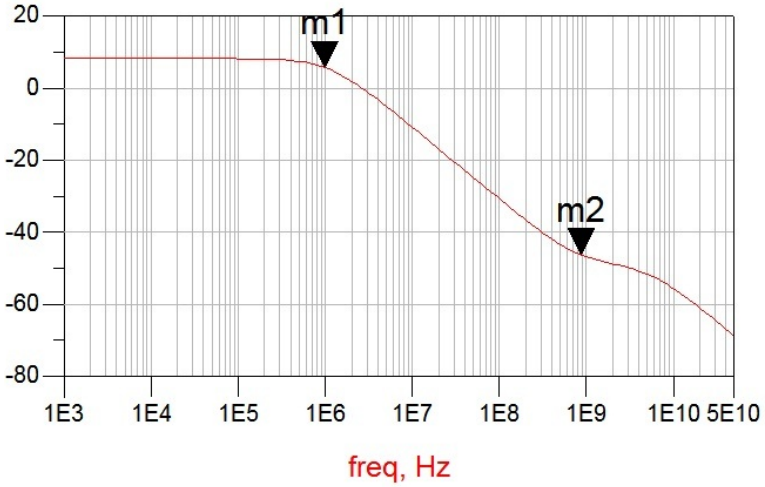

Figure 4.14: Frequency response for the redesigned filter with the driver amplifier in 1.42 supply voltage. The cut-off point is at 5.2db and 986.4KHz

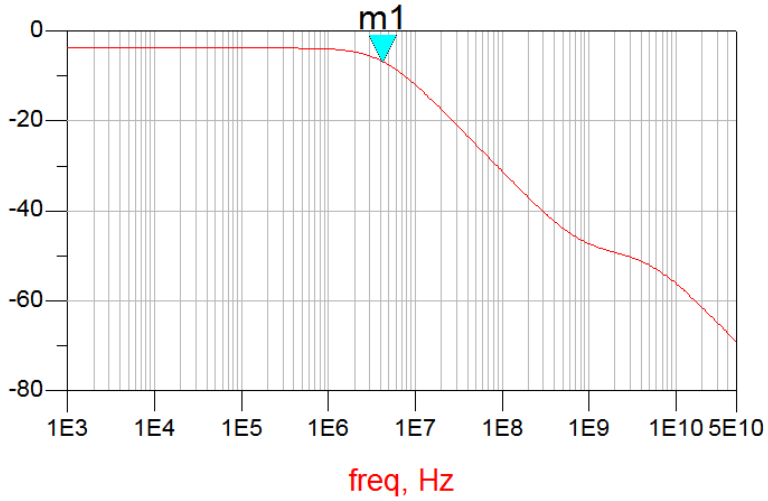

Figure 4.15: Frequency response for the redesigned filter with the driver amplifier in 1.5 supply voltage. The cut-off point is at -6.8db (similar to the original design) and 4.2MHz

The circuit operated with a 3V operating frequency and had a chip area of 2.2mm.The frequency response of the filter can be seen in (Figure 4.13). In our case we seek to redesign the circuit for a smaller newer 0.25um device technology. To compensate for the device differences intuitively the ratios should be 2-3 times smaller than the actual ones in the 1.2um version. We choose to reduce the transistors' aspect ratios by half. Then reduced the dimensions to bring them closer to the new technology, while keeping

the new ratios the same. The resulting transfer function we expect to be close to the initial behavior and later, by IC analysis, to achieve better and more correct behavior through more correct ratio choices, guided by the calculated ICs. The resulting filter should be able to operated similarly with much less transistor area and supply voltages. The new transistor aspect ratios for each sub-circuit of the filter can be seen in Table 4.1.

Then final design that resulted by the new ratio choices started working with the Driver Amplifier in a supply voltage between 1.4-1.5V and the rest of the sub-circuits with a supply of 0.5V. Since the driver amplifier controls the transconductance of the filter tweaking the supply would not only cause differences in amplitude but also in cut-off frequency. Specifically the filter has a 1MHz cut-off frequency with the driver having a supply voltage of 1.42V (Figure 4.14). The filter achieves similar behavior to the original with a 1.5V supply and a cut-off frequency of 4.2MHz (Figure 4.15). From the frequency response it is obvious that the filter function is not as it would be expected. Although the filter works and there is a very small ripple, the slope is smaller and the stop-band notch is almost nonexistent. Later with the Inversion Coefficient analysis we will seek to make new choices to achieve more correct and efficient functionality.

4.3 The Current Mode Operational Amplifier Implementation

Besides the option of implementing the integrators with a Gm element that makes the translation to current mode straightforward there is also the option of directly translating the typical integrator used in our voltage mode paradigm using the adjoint principle. Following the principle, what is needed to get the inter-reciprocal circuit is to reverse the inputs turning the signals to currents with the appropriate network for the respective current mode function(Figure 3.12).

Because of the symmetry of the function it is obvious that by reversing input and output in a integrator the resulting network is the same as a voltage differentiator.In truth differentiator topology causes the current signal to have the same frequency response to a voltage signal in an voltage integrator topology. So we use the voltage differentiator topology with a current mode Operational amplifier with respective behavior. In other words the output of the CM OpAmp again here tries to cancel out the input current difference (Figure 4.16).So since the positive input is connected to the ground in the differentiator topology the feedback produces an equal and opposite current to the current entering the other amplifier input. This leads to a slightly different differentiator than the typical:

$$I_{out} = I_R = \frac{V_R}{R} = \frac{V_{out}}{R} \tag{4.9}$$

and

$$I_R = -I_C = -C\frac{dV_{in}}{dt} \tag{4.10}$$

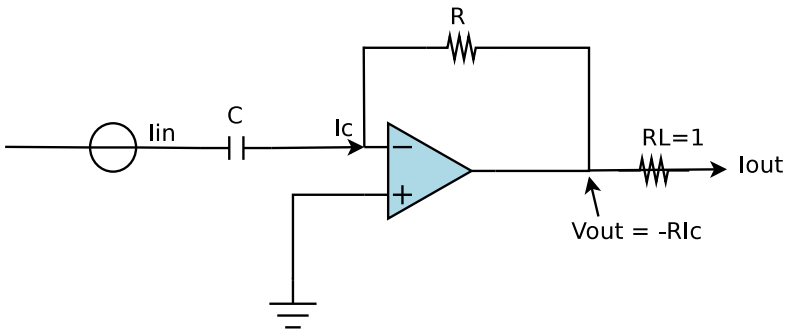

Figure 4.16: Differentiator topology working inter-reciprocal to the voltage mode integrator

So:

$$V_{out} = -RC\frac{dV_{in}}{dt} \tag{4.11}$$

What is needed now is the use the suitable current mode operational amplifier for the differentiator. From there we can use the initial ladder filter block diagram to recreate the filter in current mode form.

The straightforward idea would be to try and recreate to CM OpAmp directly using the adjoint principle. The transformation idea can be seen in (Figure 1.4). It can be implemented with various methods. A simple one was to use current conveyor with the Y input grounded and the Z input sent to high impedance load, such as a differential stage. This idea, unfortunately is unsuitable. First of all, the resulting circuit is complex and creates problem when high loads are driven by such structures. More important the resulting structure has single ended input and differential output , not very compatible for the translation of the OpAmp ladder filter implementation. Lastly output sharing which is present in the filer implementation is quite difficult since multiple instances of the CM OpAmp will be needed to replicate the outputs.In order to simplify the design a CM OpAmp with differential input and single ended output is required. Preferably the circuit should be able to replicate its output easily, so there would be no need for multiple instances of the same differentiator stage. Such an example of current mode operational amplifier was proposed in [32].

The strategy is to follow the typical voltage mode 3-stage operational amplifier design template (Figure 3.4) and implement it for current signals. The current mode OpAmp has infinite current gain and output impedance and zero input impedance and common mode current gain. In the typical voltage mode OpAmp the voltage signal is transfered to current for the second and main amplification stage and back to voltage through the output buffer to produce the final output signal. The CM OpAmp follows this idea by tranforming the current signal in the main stage as a voltage and producing the current output though the final stage buffer(Figure 4.17). The three stages can be implemented with simple MOS circuits combined to achieve the required functionality. The initial I-V conversion can be done by a simple current mirror. Each input stage

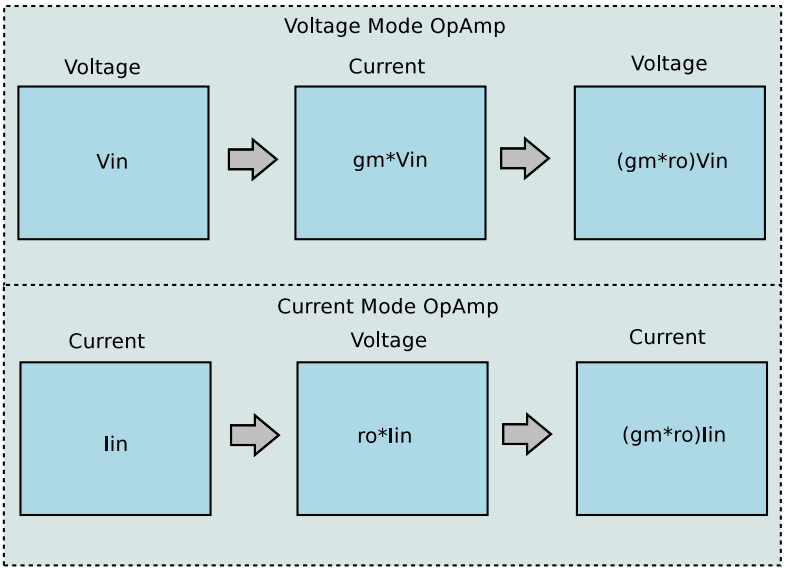

Figure 4.17: Signal Flow in voltage and current mode OpAmp

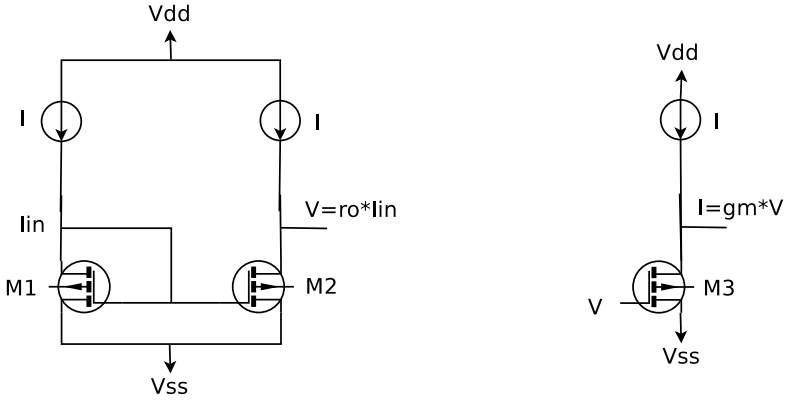

Figure 4.18: I-V conversion with simple current mirror and V-I conversion with simple current source

can include one current mirror. The voltage signal can then be amplified by a third current mirror providing also the amplifier gain. Finally the V-I conversion in the output buffer is achieved by a simple source amplifier implemented by one MOS transistor (Figure 4.18). Since the second stage mirror has a voltage output this voltage can be shared between multiple output buffers and produce multiple copies of the amplifier outputs, useful for the sharing that is needed in the design of the ladder filter. A double output version of the circuit can be seen in Figure 4.19. The output current for the CM OpAmp is :

$$I_{out} = A(I_{in+} - I_{in-}) \tag{4.12}$$

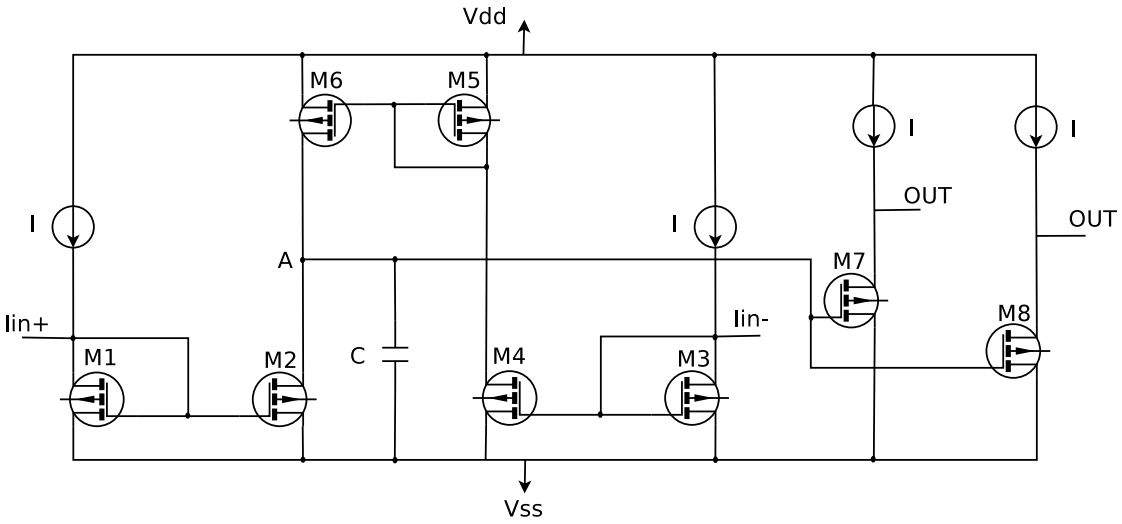

Figure 4.19: Detail schematic of the current mode OpAmp

Where A is the current gain equal to:

$$A = g_{mo} * r_{oa} \tag{4.13}$$

with g_{mo} the transconductance of the output buffer transistor(s) and r_{oa} impedance in node A.The g_{mo} is equal to :

$$g_{mo} = \sqrt{2 I_B K \frac{W}{L}} \tag{4.14}$$

Since the gain is dependent on the g_{mo} it can be control by either manipulating the buffer's bias current(I_B) or its transistors aspect ratios($\frac{W}{L}$). Increased bias current or aspect ratios lead to higher gain with the expense of either power consumption or area die.

This CM OpAmp implementation is straightforward, simple and practical because of the easy output replication. But it also comes with some disadvantages. First of all there is a certain lack of symmetry in its two inputs. Basically in closed loop configurations the inverting input has smaller input impedance than the non inverting, which in the case of the voltage mode counterpart the input impedance is the same in both inputs. This can create difficulty in the application of the circuits. More significantly the presence of the compensation capacitor and the fact that on occasion high bias currents might be needed for correct functionality, decrease power efficiency and distortion performance.

Guided by the block diagram(Figure 4.3) we can now derive a current mode implementation of the same filter using this Operational Amplifier design.The respective new block diagram can be seen in Figure 4.20. The load and output resistors are 1Ω and both capacitors also are 1pf. As before the design requires differentiators with double

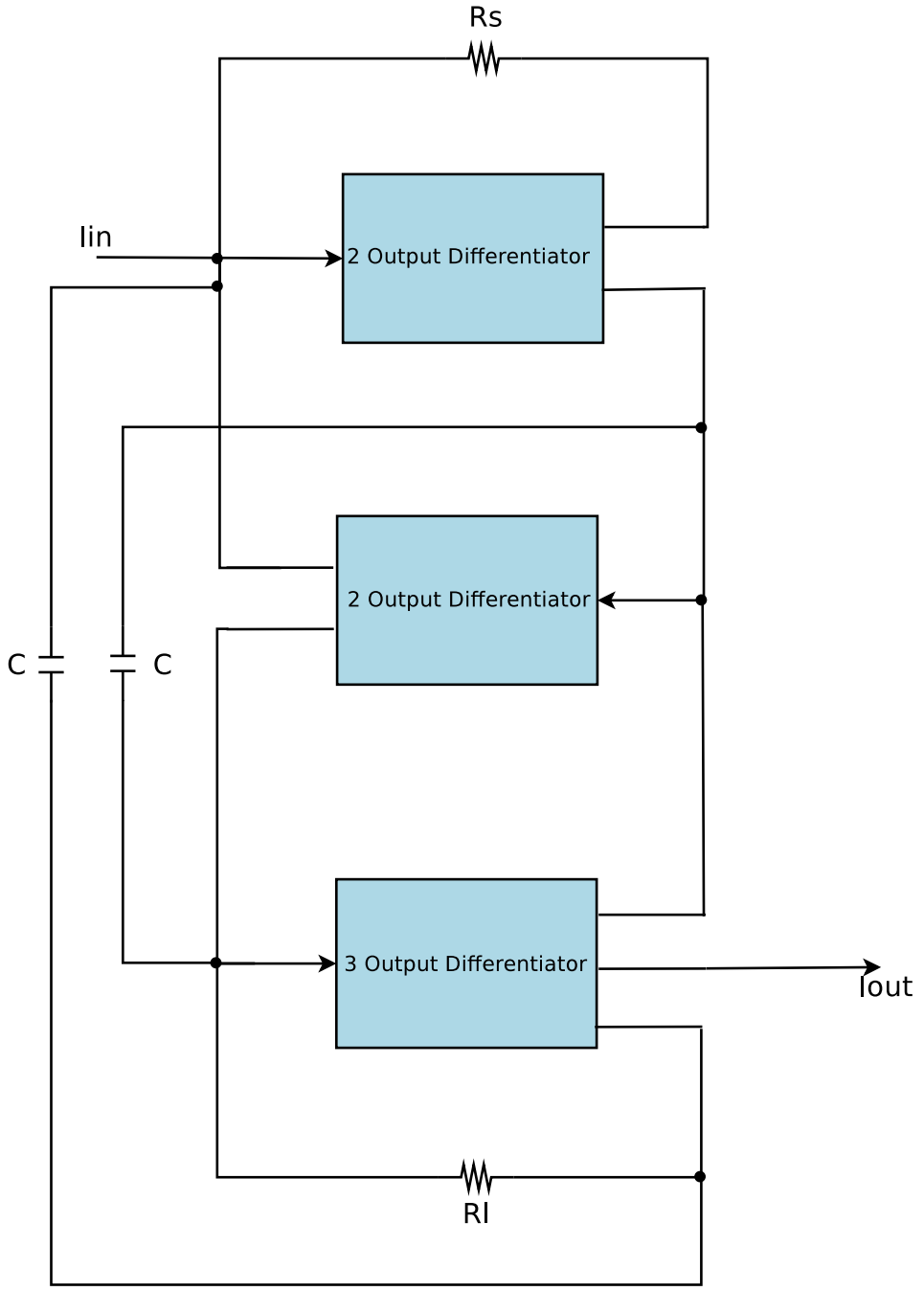

Figure 4.20: Filter block diagram for the current mode operational amplifier implemetation

output and one with three for the bottom stage of the ladder filter. As a start we used aspect ratios similar to those of the transconductor transistors of the Gm-C filter, to keep the current magnitude similar to the previous filter(Table 4.2). The target

CM Operational Amplifier transistors	Aspect Ratio um/um
PMOS	6.25/1.25
NMOS	6.25/0.63

Table 4.2: Current mode Operational amplifier's starter aspect ratios

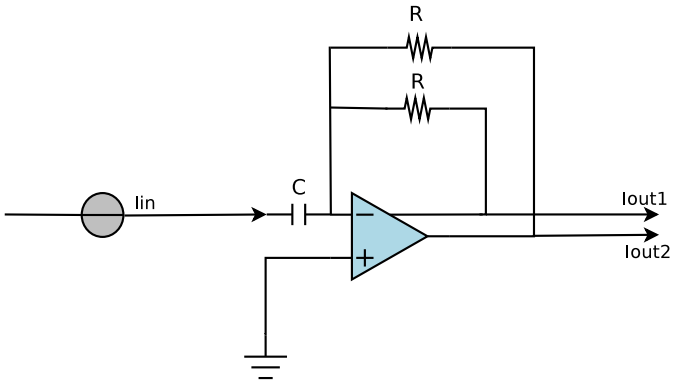

Figure 4.21: 2-output CM OpAmp differentiator

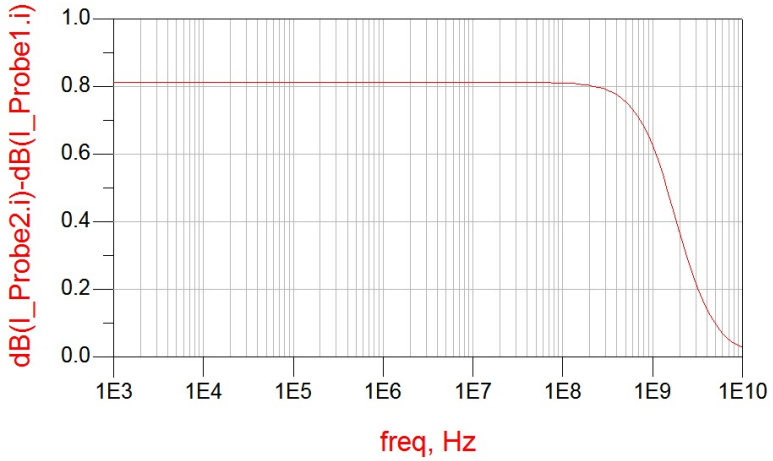

Figure 4.22: Current mode differentiator frequency response

cut-off frequency is around the same to the passive and voltage mode implementation described in the beginning of the chapter. The differentiator has one feedback loop from each identical output passing through one resistor(Figure 4.21).The resulting differentiator has similar frequency response to the voltage mode integrator, as expected, which is that of a 1st order low-pass filter (Figure 4.22). The magnitude of the resistor in the differentiator can control the cut-off frequency of the filter. The capacitor values in all instances are kept in 1pf value. The filter can have a wide range of cut-off frequencies. As the resistor values increase the cut-off frequency also reduces. For

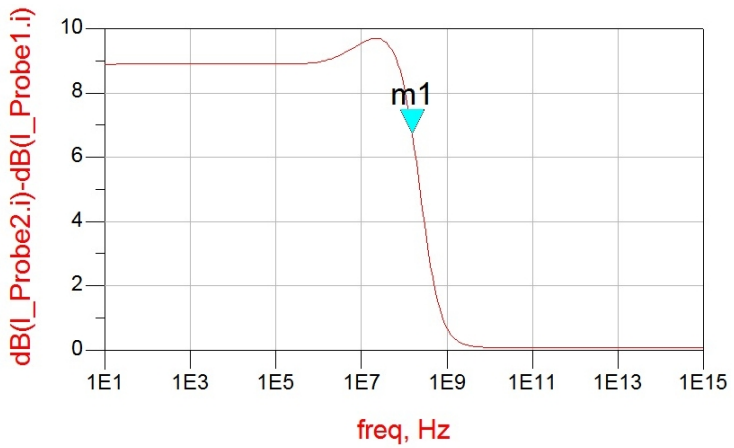

Figure 4.23: 155MHz CM filter frequency response. -3db point at 6.7db at 155.1 MHz frequency point.

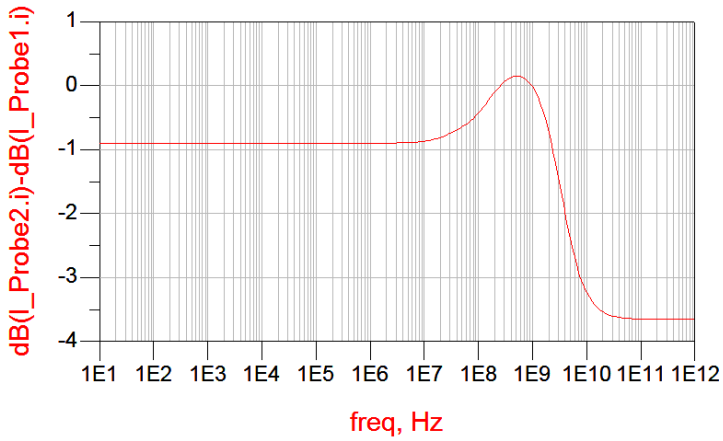

Figure 4.24: 7.2GHz CM filter frequency response. -3db point at -2.92db at 7.197GHz frequency point.

instance with the differentiator resistors at 500KΩ the cut-off frequency of the filter is at 20MHz with a passband ripple of about 0.9db. To replicate the initial passive filter the resistor values are found to be at 50KΩ. The passband ripple is around 0.8db. The cut-off frequency is at 155MHz and the power supply is just at 1V for all circuits blocks(Figure 4.23). In this configuration the Bias current of the operational amplifiers is at 1mA.

We can also produce high frequency filters by tweaking the gain of the amplifiers, either by changing the bias current or the output transistors aspect ratios. The first

option is quite tempting since it also improves power efficiency. By reducing the bias current from 1mA to 650uA and using 5KΩ resistors in the differentiators, the resulting filter has the its cut-off point at -3db with a frequency of 7.2GHz. This comes at the expense of the passband ripple since the OpAmp's gain is reduced. The ripple is about 1db. The power supplies here are 1.5V. The frequency response of this version can be seen in Figure 4.24.

These filter implementations have interesting simplicity and can translate the voltage mode OpAmp ladder filter implemetation directly to current mode inheriting the benefits of the strategy. Also the reduction in voltage supply and area in these filters compared to the filter implemented in 1.2um technology is considerable in the expense of the higher passband ripple which in original 1MHz CM filter was lower 0.2db in simulations and 0.6db in the actual realized filter. The general behavior of both filters implementations and power efficiency can be improved more with a better choice of transistor ratios in the design. A good guide for the updated choices is the Inversion Coefficient.

4.4 Inversion Coefficient (IC) Calculation and Analysis

Conventional approaches have usually interpreted MOSFETs in a voltage-current model, describing MOSFET behavior as a cluster of effects influencing device functionality. In sub-micron and deep sub-micron technologies these models are not accurate enough to describe transistor behavior. Typical equations are now less valid and transistor behavior becomes more complex. Adding to that is the lower supply voltage range that designers have in smaller technologies.

Usually this gives researches two ways to cope with these problems. One solution is to choose device dimensions by the arbitrary selection of the transistor biasing and choose width and length accordingly. Then through trial and error process choose different current and design parameters until the circuits come as close as possible to the desired behavior. This strategy is not only a very uncontrolled process, but it can lead to transistors working in weak and moderate inversion still, without having a way to be interpreted sufficiently. The other option is to completely avoid the problem by making sure that the transistors work in strong inversion.This strategy cannot incorporate the possibility of transistors working in other inversion regions and its possible benefits. Moreover in the lower sizes of newer transistor technology, which leads to reduction in supply voltages, the option to work in strong inversion may not be the optimal, if it is available altogether.

A different idea for the design process, used more recently, is to use the inversion level as a basic guide for the design choices. If the inversion level can be identified, it can also be used to identify operating region and also with this parameter different behavioral characteristics of the designs can be predicted. It can basically be used as a general variable to characterize transistor behavior. Moreover it also provides the means to relate transconductance to current, in transistors working in saturation mode, by:

$$g_{ms} * U_T/I_d = g_m * n * U_T/I_d = (0.5 + \sqrt{0.25 + IC})^{-1} \tag{4.15}$$

Constant	NMOS	PMOS
μ_0	$540[cm^2/V_s]$	$185[cm^2/V_s]$
n factor	1.47	1.44
I_0	$6.4 * 10^{-3}$[A]	$2.1 * 10^{-3}$[A]

Table 4.3: Constants needed for hand calculation of IC

This expression is valid from weak through moderate inversion and onset of strong inversion(In the area in which IC is higher than 10 , neglecting high field effects like vertical field mobility, velocity saturation etc). This shows that transconductance is maximum for a low level of inversion (for a given current).This can be of fundamental importance for designing in moderate inversion, in which classical methods fail. By this principle, the previous model, that leads to indeterministic and limiting design strategies and require larger error assumptions,is replaced by a relatively simple model that is more deterministic. The inversion level can be characterized by the Inversion Coefficient.

4.4.1 Inversion Coefficient Calculation

The value determining inversion level is the Inversion Coefficient or IC. It is defined as such:

$$IC = \frac{I_d}{I_0(W/L)} \tag{4.16}$$

with I_d being the drain current of the transistor in question and (W/L) the transistor dimensions.I_0 is defined as the drain current of a transistor with W/L = 1, or unity shape factor device, operating in the middle of moderate inversion (IC = 1). This current is obviously dependent on the technology and is equal to :

$$I_0 = 2nK_pU_T^2 \tag{4.17}$$

Here n is the device slope factor. U_T is defined as the thermodynamic voltage and is equal to :

$$U_T = \frac{KT}{q} \tag{4.18}$$

with K the Boltzzmann constant, T the temperature in Kelvin degrees and q the Magnitude of electron charge. K_p is calculated by the low-field mobility factor and the oxide capacitance:

$$K_p = \mu_0 C_{ox} \tag{4.19}$$

The oxide capacitance is calculated by the E_{ox} and T_{ox} by:

$$C_{ox} = \frac{E_{ox}}{T_{ox}} \tag{4.20}$$

Also a simple way to practically calculate the n factor by simulation for the device technology is to use a transistor in saturation mode and produce the $I_d vs V_g$ plot.From there we can measure the $g_m * U_T/I_d$ value. Specifically we first derive the derivative of logarithm of I_d by V_g which is :

$$\frac{d[ln(I_d)]}{dV_g} = g_m/I_d \tag{4.21}$$

Then we multiply with the thermodynamic voltage and draw the $g_m * U_T/I_d$ vs I_d plot. By observing the $g_m * U_T/I_d$ value in weak inversion we can estimate the n factor by :

$$g_m * U_T/I_d = \frac{1}{n} \tag{4.22}$$

The constant values required for the IC theoretical calculation can be seen in Table 4.3

A simpler way of calculating IC is by simulation, using the specific current or I_{spec}. It is defined as :

$$I_{spec} = I_0 \frac{W}{L} \tag{4.23}$$

And so the inversion coefficient is equal to :

$$IC = \frac{I_d}{I_{spec}} \tag{4.24}$$

The I_{spec} can be derived by simulation again using a transistor with the specific dimensions in saturation mode. This time through the $\sqrt{I_d}$ which is equal to:

$$\sqrt{I_d} = \sqrt{\frac{n * \beta}{2}} * (V_p - V_s) = \frac{\sqrt{I_{spec}}}{2 * U_T} * (V_p - V_s)$$

If we compute the slope of the plot of the $\sqrt{I_d}$ vs V_g it is equal to :

$$Slope = \frac{\sqrt{I_{spec}}}{2 * U_T * n}$$

And so :

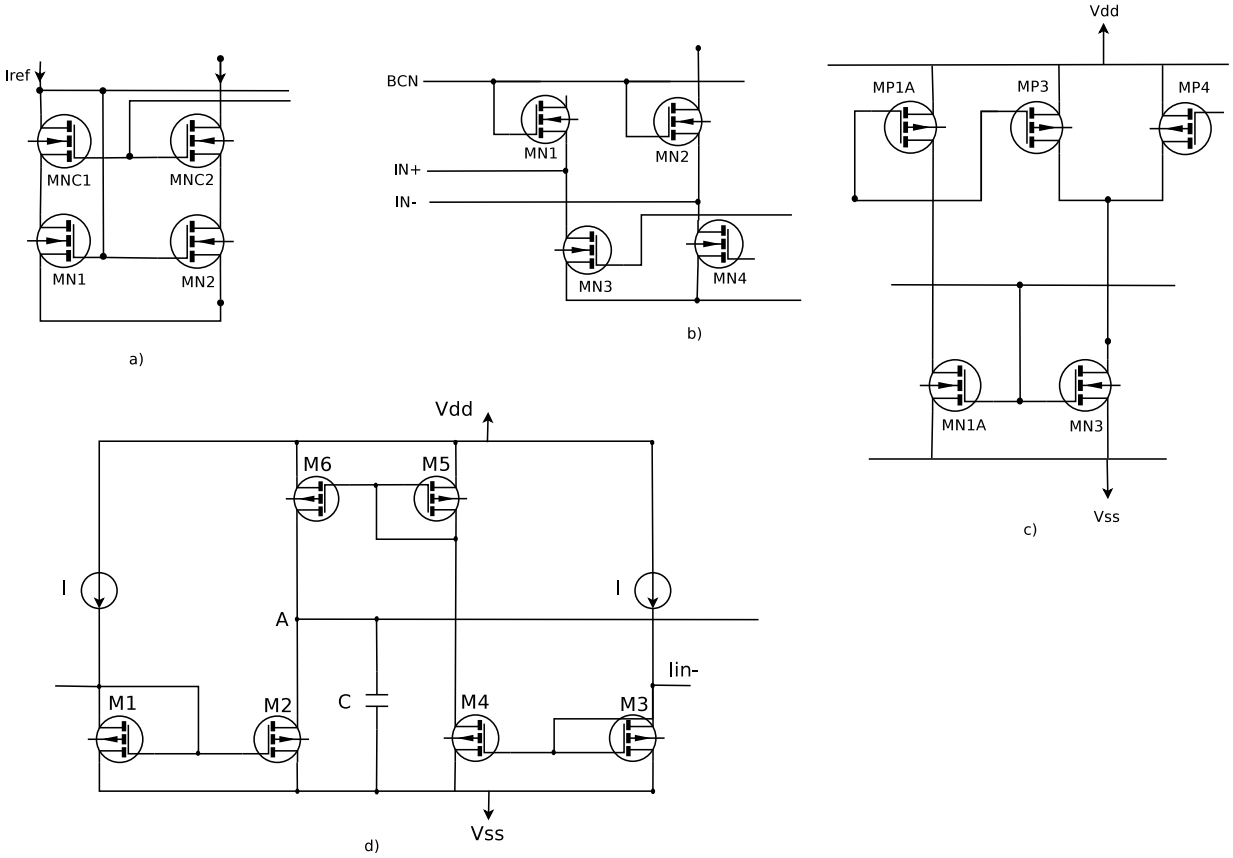

Figure 4.25: Circuit parts included to the IC analysis.a) Current reference b) Driver c) Transconductor d) CM OpAmp

$$I_{spec} = (Slope * 2 * U_T * n)^2 \tag{4.25}$$

In the $d\sqrt{I_d}$ vs dV_g we use the maximum slope for equation 4.25 and derive the I_{spec} for every aspect ratio of the transistors we want to analyze in the circuit. By this method we calculated the Inversion Coefficients in our filter implementations. Next we shall describe which parts of the filters circuit we considered critical to be used the IC analysis and present the results of the measurements.

4.4.2 Inversion Coefficient Analysis

Our implementations are comprised mostly by current sources and mirrors and differential pairs, which provide the main functionality. So it is natural to concentrate the analysis on these essential parts of the circuits. For the current mirrors and source for the best behavior the inversion level should be relatively high. Around the onset of strong inversion so to have good functionality but on the same time not increase V_{DSsat} too much. For the differential pair on the other hand the best inversion level would be

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
MP3	6.25/1.25	$5.158 * 10^{-7}$	$6.994 * 10^{-8}$	0.675	0.135
MP4	6.25/1.25	$5.158 * 10^{-7}$	$6.994 * 10^{-8}$	0.675	0.135
MN3	12.5/0.63	$1.022 * 10^{-5}$	$1.23 * 10^{-7}$	0.23	0.012
MN1A	6.25/0.63	$5.118 * 10^{-6}$	$2.652 * 10^{-8}$	0.051	0.0051
MN2A	6.25/0.63	$5.118 * 10^{-6}$	$2.652 * 10^{-8}$	0.051	0.0051
MP1A	6.25/1.25	$5.158 * 10^{-7}$	$6.672 * 10^{-8}$	0.64	0.128
MP2A	6.25/1.25	$5.158 * 10^{-7}$	$6.672 * 10^{-8}$	0.64	0.128

Table 4.4: IC calculations for the transconductor of the Gm-C filter top integrator block

around moderate to just before the begging of strong inversion. In this case the matching and noise performance reach the best trade-off circumstances.

We need to specifically define the essential transistors of the circuits which will be the ones that will determining the new aspect ratios.For the Gm-C filter the transistors to be analyzed are:

- For the driver amplifier essential are the current sources structures(both complementary structures) of the input circuits that can limit linearity and influence gain and power efficiency (Figure 5.1b).
- In the trans-conductor obviously most essential are the differential pairs and the structures mirroring the outputs that implement the dynamic biasing (Figure 5.1c).
- Lastly in current reference circuit the current mirrors producing the I_{ref} can be a source of limitation and so they are also considered essential for the analysis (Figure 5.1a).

For the current mode OpAmp filter implementation is it important to analyze the current mirror transistors in the input and 2nd stages, that can influence behavior and power efficiency(Figure 5.1d).

The following tables list the IC measurements and computations in detail for each transistor of the circuits of the two filter implementations(Tables 4.4-4.16). First for the 4.2MHz Gm-C filter for each integrator block and the current reference. Then the tables are presented for ICs of the two CM OpAmp implementations for each of the differentiators. The transistor name and aspect ratio, I_{spec}, I_d and IC value are depicted in the tables alongside the I_d/I_0 value required further on for the new dimension calculations. The current measurements were done on simulation using current probes of the ADS design tool.

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
MP3	6.25/1.25	$5.158 * 10^{-7}$	$5.933 * 10^{-8}$	0.55	0.11
MP4	6.25/1.25	$5.158 * 10^{-7}$	$5.933 * 10^{-8}$	0.55	0.11
MN3	12.5/0.63	$1.022 * 10^{-5}$	$1.146 * 10^{-7}$	0.23	0.012
MN1A	6.25/0.63	$5.118 * 10^{-6}$	$7.878 * 10^{-8}$	0.155	0.015
MN2A	6.25/0.63	$5.118 * 10^{-6}$	$7.878 * 10^{-8}$	0.155	0.015
MP1A	6.25/1.25	$5.158 * 10^{-7}$	$2.219 * 10^{-8}$	0.205	0.041
MP2A	6.25/1.25	$5.158 * 10^{-7}$	$2.219 * 10^{-8}$	0.205	0.041

Table 4.5: IC calculations for the transconductor of the Gm-C filter middle integrator block

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
MP3	6.25/1.25	$5.158 * 10^{-7}$	$7.049 * 10^{-8}$	0.675	0.135
MP4	6.25/1.25	$5.158 * 10^{-7}$	$7.049 * 10^{-8}$	0.675	0.135
MN3	12.5/0.63	$1.022 * 10^{-5}$	$2.484 * 10^{-7}$	0.476	0.024
MN1A	6.25/0.63	$5.118 * 10^{-6}$	$3.957 * 10^{-9}$	0.0076	0.0008
MN2A	6.25/0.63	$5.118 * 10^{-6}$	$6.1 * 10^{-9}$	0.0196	0.0019
MP1A	6.25/1.25	$5.158 * 10^{-7}$	$1.829 * 10^{-9}$	0.175	0.035
MP2A	6.25/1.25	$5.158 * 10^{-7}$	$2.278 * 10^{-9}$	0.175	0.035

Table 4.6: IC calculations for the transconductor of the Gm-C filter bottom integrator block

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
MN1	20.8/0.25	$5.374 * 10^{-5}$	$2.832 * 10^{-6}$	4.326	0.052
MN2	20.8/0.25	$5.374 * 10^{-5}$	$2.832 * 10^{-6}$	4.326	0.052
MN3	5.2/0.63	$4.257 * 10^{-6}$	$4.332 * 10^{-6}$	8.336	1.01
MN4	5.2/0.63	$4.257 * 10^{-6}$	$4.332 * 10^{-6}$	8.336	1.01
MP1	5.2/0.63	$9.43 * 10^{-7}$	$3.857 * 10^{-9}$	0.033	0.004
MP2	5.2/0.63	$9.43 * 10^{-7}$	$3.857 * 10^{-9}$	0.033	0.004
MP3	5.2/0.25	$3.048 * 10^{-6}$	$1.235 * 10^{-8}$	0.083	0.004
MP4	5.2/0.25	$3.048 * 10^{-6}$	$1.235 * 10^{-8}$	0.083	0.004

Table 4.7: IC calculations for the driver amplifier of the Gm-C filter top integrator block

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
MN1	20.8/0.25	$5.374 * 10^{-5}$	$2.3 * 10^{-7}$	0.349	0.0042
MN2	20.8/0.25	$5.374 * 10^{-5}$	$2.3 * 10^{-7}$	0.349	0.0042
MN3	5.2/0.63	$4.257 * 10^{-6}$	$9.276 * 10^{-8}$	0.179	0.022
MN4	5.2/0.63	$4.257 * 10^{-6}$	$2.466 * 10^{-7}$	0.47	0.057
MP1	5.2/0.63	$9.43 * 10^{-7}$	$9.486 * 10^{-8}$	0.825	0.1
MP2	5.2/0.63	$9.43 * 10^{-7}$	$9.486 * 10^{-8}$	0.825	0.1
MP3	5.2/0.25	$3.048 * 10^{-6}$	$1.487 * 10^{-7}$	0.998	0.048
MP4	5.2/0.25	$3.048 * 10^{-6}$	$1.487 * 10^{-7}$	0.998	0.048

Table 4.8: IC calculations for the driver amplifier of the Gm-C filter middle integrator block

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
MN1	20.8/0.25	$5.374 * 10^{-5}$	$2.3 * 10^{-7}$	0.349	0.0042
MN2	20.8/0.25	$5.374 * 10^{-5}$	$2.3 * 10^{-7}$	0.349	0.0042
MN3	5.2/0.63	$4.257 * 10^{-6}$	$9.276 * 10^{-8}$	0.179	0.022
MN4	5.2/0.63	$4.257 * 10^{-6}$	$2.466 * 10^{-7}$	0.47	0.057
MP1	5.2/0.63	$9.43 * 10^{-7}$	$9.486 * 10^{-8}$	0.825	0.1
MP2	5.2/0.63	$9.43 * 10^{-7}$	$9.486 * 10^{-8}$	0.825	0.1
MP3	5.2/0.25	$3.048 * 10^{-6}$	$1.487 * 10^{-7}$	0.998	0.048
MP4	5.2/0.25	$3.048 * 10^{-6}$	$1.487 * 10^{-7}$	0.998	0.048

Table 4.9: IC calculations for the driver amplifier of the Gm-C filter bottom integrator block

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
MNC1	5.2/0.25	$1.152 * 10^{-5}$	$1.099 * 10^{-8}$	0.02	0.001
MNC2	5.2/0.25	$1.152 * 10^{-5}$	$1.019 * 10^{-8}$	0.018	0.0009
MN1	5.2/0.63	$4.257 * 10^{-6}$	$8.155 * 10^{-9}$	0.016	0.0019
MN2	5.2/0.63	$4.257 * 10^{-6}$	$8.749 * 10^{-9}$	0.017	0.002
MPC1	5.2/0.25	$3.048 * 10^{-6}$	$2.064 * 10^{-9}$	0.014	0.0007
MPC2	5.2/0.25	$3.048 * 10^{-6}$	$3.768 * 10^{-9}$	0.025	0.0012
MP1	28.6/0.63	$6.458 * 10^{-6}$	$7.678 * 10^{-9}$	0.054	0.0012
MP2	5.2/0.63	$9.43 * 10^{-7}$	$4.847 * 10^{-9}$	0.042	0.0051

Table 4.10: IC calculations for the current reference of the Gm-C filter

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
M1	6.25/0.63	$5.118 * 10^{-6}$	0	0	0
M2	6.25/0.63	$5.118 * 10^{-6}$	$1.315 * 10^{-5}$	24.8	2.5
M3	6.25/0.63	$5.118 * 10^{-6}$	$6.288 * 10^{-4}$	1210	122
M4	6.25/0.63	$5.118 * 10^{-6}$	$3.229 * 10^{-5}$	62.5	6.3
M5	6.25/1.25	$5.158 * 10^{-7}$	$9.901 * 10^{-6}$	95	19
M6	6.25/1.25	$5.158 * 10^{-7}$	$1.315 * 10^{-5}$	109.5	21.9

Table 4.11: IC calculations for 155MHz current mode filter top differentiator block

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
M1	6.25/0.63	$5.118 * 10^{-6}$	0	0	0
M2	6.25/0.63	$5.118 * 10^{-6}$	$1.299 * 10^{-5}$	24.8	2.5
M3	6.25/0.63	$5.118 * 10^{-6}$	$6.186 * 10^{-4}$	1190	120
M4	6.25/0.63	$5.118 * 10^{-6}$	$3.186 * 10^{-5}$	61.5	6.2
M5	6.25/1.25	$5.158 * 10^{-7}$	$9.801 * 10^{-6}$	94.5	18.9
M6	6.25/1.25	$5.158 * 10^{-7}$	$1.299 * 10^{-5}$	121.5	24.3

Table 4.12: IC calculations for 155MHz current mode filter middle differentiator block

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
M1	6.25/0.63	$5.118 * 10^{-6}$	0	0	0
M2	6.25/0.63	$5.118 * 10^{-6}$	$1.387 * 10^{-5}$	26.8	2.7
M3	6.25/0.63	$5.118 * 10^{-6}$	$6.186 * 10^{-4}$	1290	130
M4	6.25/0.63	$5.118 * 10^{-6}$	$3.186 * 10^{-5}$	68.5	6.9
M5	6.25/1.25	$5.158 * 10^{-7}$	$9.801 * 10^{-6}$	94.5	18.9
M6	6.25/1.25	$5.158 * 10^{-7}$	$1.299 * 10^{-5}$	128	25.6

Table 4.13: IC calculations for 155MHz current mode filter bottom differentiator block

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
M1	6.25/0.63	$5.118 * 10^{-6}$	0	0	0
M2	6.25/0.63	$5.118 * 10^{-6}$	$2.604 * 10^{-6}$	4.96	0.5
M3	6.25/0.63	$5.118 * 10^{-6}$	$5.548 * 10^{-4}$	1071	108
M4	6.25/0.63	$5.118 * 10^{-6}$	$3.106 * 10^{-6}$	5.95	0.6
M5	6.25/1.25	$5.158 * 10^{-7}$	$4.269 * 10^{-6}$	56	11.2
M6	6.25/1.25	$5.158 * 10^{-7}$	$4.407 * 10^{-6}$	41.85	8.37

Table 4.14: IC calculations for 7.2GHz current mode filter top differentiator block

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
M1	6.25/0.63	$5.118 * 10^{-6}$	0	0	0
M2	6.25/0.63	$5.118 * 10^{-6}$	$3.407 * 10^{-6}$	6.55	0.66
M3	6.25/0.63	$5.118 * 10^{-6}$	$4.245 * 10^{-4}$	813.5	82
M4	6.25/0.63	$5.118 * 10^{-6}$	$3.275 * 10^{-6}$	6.25	0.63
M5	6.25/1.25	$5.158 * 10^{-7}$	$2.618 * 10^{-6}$	25	5
M6	6.25/1.25	$5.158 * 10^{-7}$	$9.041 * 10^{-6}$	81	16.2

Table 4.15: IC calculations for 7.2GHz current mode filter middle differentiator block

Trans	**Aspect Ratio [um/um]**	$I_{spec}[A]$	$I_d[A]$	$I_d/I_0[A]$	**IC**
M1	6.25/0.63	$5.118 * 10^{-6}$	0	0	0
M2	6.25/0.63	$5.118 * 10^{-6}$	$1.288 * 10^{-5}$	24.8	2.5
M3	6.25/0.63	$5.118 * 10^{-6}$	0.001	813.5	195
M4	6.25/0.63	$5.118 * 10^{-6}$	$2.811 * 10^{-6}$	6.25	0.54
M5	6.25/1.25	$5.158 * 10^{-7}$	$8.253 * 10^{-6}$	107.5	21.5
M6	6.25/1.25	$5.158 * 10^{-7}$	$1.342 * 10^{-5}$	128.5	25.7

Table 4.16: IC calculations for 7.2GHz current mode filter bottom differentiator block

4.5 Re-designing of the filter implementations

With the ICs known we can now re-design the filters to achieve better behavior and power efficiency. As mentioned before current mirrors are better suited to work at the beginning of strong inversion. A good span for that are values between 15 and 30. Differential pairs are more suited to work between moderate and strong inversion. A good choice would be an IC value between 2 and 10. These spans can work as target for the inversion level of the redesigned transistors and guide the choices of the new ratios. The strategy would be to use I_d, L and IC and derive according to them a new W(as opposed to the traditional idea that design is based on I_d, W and L), and so achieve the wanted level of inversion without significant change in the transistor length.In other words from equation 4.16 we have:

$$IC = \frac{I_d}{I_0} * L/W \tag{4.26}$$

and so:

$$\frac{W}{L} = \frac{1}{IC}\frac{I_d}{I_0} \tag{4.27}$$

4.5.1 For the Gm-C filter

For the Gm-C filter there are a few issues with the ICs and its characteristics. First of all it is obvious that the transistors work in deep WI or sometimes in Ultra Deep WI.

Driver Transistors	Aspect Ratio um/um
MN1,MN2 and MNC8	2.08/0.25
MN4,MN3 and MNC5-7	0.52/0.63
MNC1-4	0.52/21
MP3,MP4 and MPC4	0.52/0.25
MP1,MP2 and MPC 1-3	0.52/0.63

Start up Transistors	Aspect Ratio um/um
MN1 and MN2	0.52/0.25
MN3 and MN4	0.52/8.3
MP1	0.52/42

Transconductor Transistors	Aspect Ratio um/um
MN1A-2B	0.625/0.63
MN3	1.25/0.63
MN4	0.33/0.63
MN6	1.04/0.25
MP1A-2B,MP3 and MP4	0.625/1.25
MP5	0.33/0.63
MP6	1.04/0.25

Current Reference Transistors	Aspect Ratio um/um
MN1-4	0.52/0.63
MNC1-3	0.52/0.25
MN4	0.33/0.63
MNC4	0.52/0.25
MNCB	0.83/6.3
MP1	2.86/0.63
MP2 and MP3	0.52/0.63
MPC1-3	0.52/0.25
MP4	0.33/0.63
MPC4	0.33/0.25
MPCB	1/6.3
MGB	0.625/1.25

Table 4.17: Gm-C Filter Transistors' new aspect ratios guided by the IC values

This would explain the speed of the filter and its differences with the original Gm-C 1MHz filter. In order to reach the target inversion level would mean that the new ratios would be very low and technology restrictions would prevent us to do this just by adjusting the transistor width.The minimum allowed width is 0.33um for the used technology. To reach the target spans, as mentioned before, would mean to increase the transistor lengths substantially(sometimes even to 60um-100um) which should avoided. Besides that an increase of the IC, pushing the inversion level towards moderate inversion,

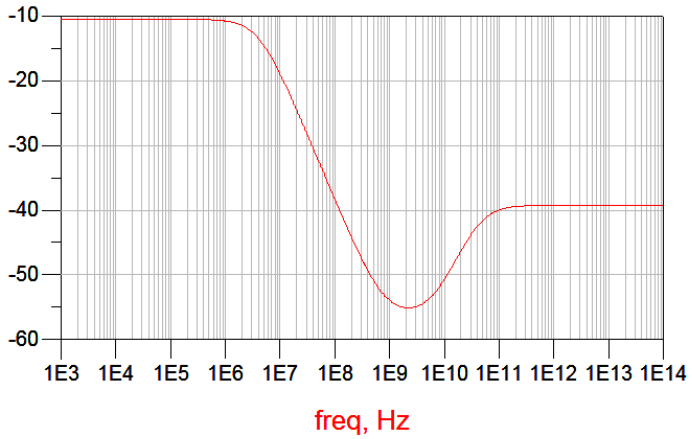

Figure 4.26: 4.2MHz Gm-C frequency response after IC analysis filter. -3db point at -13.5db at 4.2 MHz frequency point.

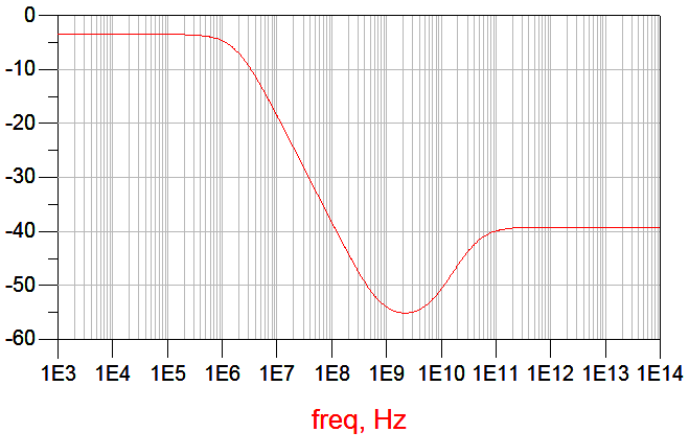

Figure 4.27: 1.7MHz Gm-C frequency response after IC analysis filter. -3db point at -6.4db at 1.76 MHz frequency point.

would certainly lead to a better behavior for the filter and the achievement of similar amplitudes with less of a power supply. So what was done was the reduction of the W/L ratio for all transistors by a factor of 10(or close to that if the technology restrictions would not allow it).

An other matter is the fact that the voltage supply of the driver has direct influence

Trans	Aspect Ratio [um/um]
M1	0.52/0.63
M2	0.52/0.63
M3	50.8/0.63
M4	1.3/0.63
M5	6.25/1.25
M6	6.25/1.25

Table 4.18: 155MHz Current mode Operational amplifier filter new aspect ratios after IC analysis

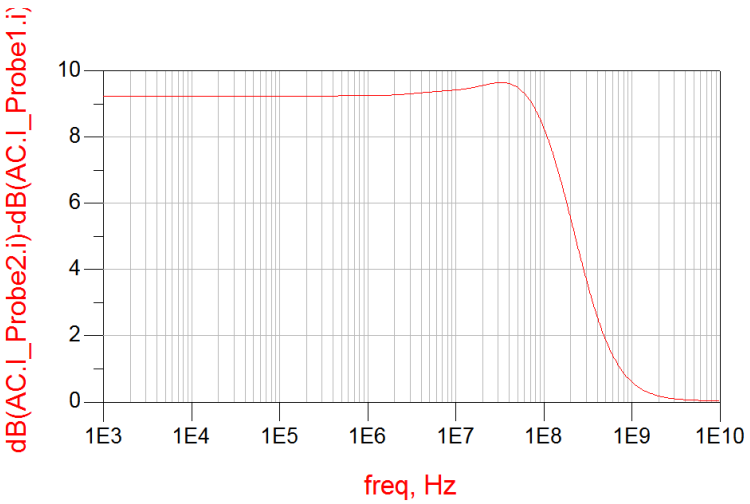

Figure 4.28: 155MHz CM filter frequency response for the updated aspect ratios. -3db point at 6.6db at 154.9 MHz frequency point.

on the cutoff frequency of the filter and hence even a small difference in it can alter it.What would be expected is that in order to have the similar filter, as the one created before in 4.2MHz, would mean that supply values should be kept the same but the resulting filter's amplitude in db would be lower. On the other hand if the filter would be to have the same amplitude as before the cut-off frequency would be lower, possibly closer to the original filter by Koli and Halonen. The new ratios can be seen in Table 4.17

In the new filter simulation we get a 4.2MHz filter with an amplitude of about 5.5db less than before and a frequency response more to the expected one and closer to the original filter in 1.2um technology(Figure 4.26). The supply voltages are still the same as with the previous implementations. If we reduce the driver supply voltage to 1.45V, in order to result in a filter with similar amplitude as before the new filter has a cut-off frequency of 1.7MHz, closer to the original 1.2um filter(Figure 4.27).

It is interesting that now the filter operates at the span of 1.4V-1.6V for the driver amplifier supply voltage. That being said, still after the 1.5V point the amplitudes

Trans	Aspect Ratio [um/um]
M1	0.33/1.46
M2	0.33/1.46
M3	30.6/0.63
M4	0.33/0.83
M5 - M5 (bottom)	3.3/1.25 - 6.25/1.25
M6 - M6 (bottom)	3.3/1.25 - 6.25/1.25

Table 4.19: 7.2GHz Current mode Operational amplifier filter new aspect ratios after IC analysis

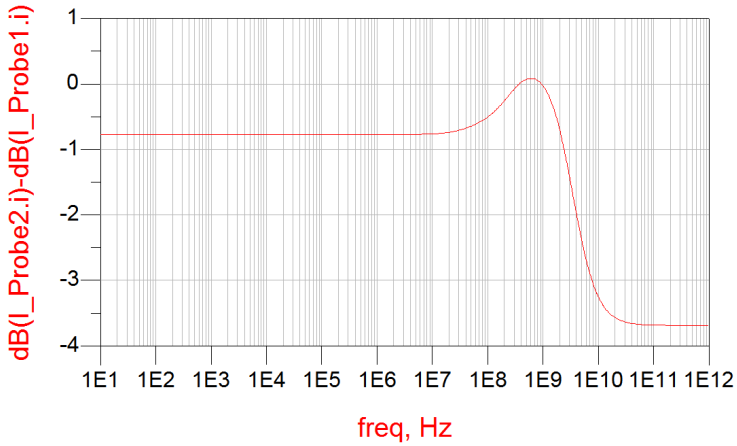

Figure 4.29: 7.2GHz CM filter frequency response for the updated aspect ratios. -3db point at -2.93db at 7.21 frequency point.

become considerably low(considerably lower than -13db for the cut-off point).

4.5.2 For the current mode OpAmp filter

In the Cm OpAmp filter the structures in question are current mirrors only. So the new ratios should target the span of 15 to 30 in IC values. Most of the transistors are actually in(or close) to moderated inversion. So in this case it is easy to achieve the wanted inversion level without the need to change the length significantly. Especially in the case of the M3 transistor in all CM OpAmp in both filters the transistor works in high strong inversion. In some occasions even higher than 100. This needs to be reduced, because in such high level of inversion the possibility of error because of self heating also arises, besides the fact that we would like to have a value in the desired value span. In all differentiator blocks the inversion levels are quite close. This enables us to use the same aspect ratios for all blocks in a filter and still have more or less the desired functionality. For the current mode OpAmp 155MHz filter we can make the design choices for the current mirror transistors as depicted in Table 4.18.

The new filter has the same amplitude and frequency with the original while working with a 0.78V supply voltage and 11kΩ resistors instead of 50kΩ. The frequency response can be seen in Figure 4.28.

The same process was done for the 7.2GHz filter. In this case also the aspect ratios are common in all differentiators since the IC values are relatively close in all cases, except for the M6 and M5 transistors of bottom the differentiator. The updated aspect ratios can be seen in Table 4.19.

The updated filter has similar frequency response as can be seen in Figure 4.29. Here the supply voltage is reduced to 1.35 V from 1.5 V and the filter uses 2.55kΩ resistors instead of the 5kΩ used before.

4.6 Summary

In this chapter we described the filter implementations created in the process of the thesis. We begun by describing the high frequency low pass elliptic passive filter that was implemented with the current mode active circuits later on and its voltage mode implementation with RC- integrators. Following were our two filter implementations. For the Gm-C filter the main architecture of the filter in [13], which was the basis of our implementation, and our version implemented in 0.25um technology were described. Then we described the design of a current mode version of the filter, but implemented this time with a CM operational amplifier, directly translated from the voltage mode counterpart. Lastly we described the process and usefulness of the IC analysis in circuit design and used it to redesign transistor dimensions of our filters to achieve better behavior and minimum voltage supplies and presented their new versions. In the next chapter we shall present some performance results for the filters designed and do some comparisons and evaluation based on them.

5 Results and Evaluation

Until this point we described the filter characteristics and main architecture of the passive and voltage mode implementations. Later two current mode implementations of filter were developed based on the Gm-C strategy and on the direct translation of the voltage mode RC-integrator implementation with the help of a current mode OpAmp. Then the IC analysis was discussed and was used to re-design the produced filters to optimize supply and efficiency. In this chapter we seek to present the results and characteristics of the designs and evaluate them in comparison to other related examples.

The chapter is organized as follows. In the first section we describe the performance of our filters in terms of voltage supply, area and power consumption. Results are compared to the original 1Mhz filter implemented in [13], which we used as a reference.In the next section the phase response are shown and the phase margin is provided to judge the stability of the circuits. In the next section tunability graphs are presented for out filter implementations.Finally a estimation is made to asses transistor mismatch in the final version of the implemented filters. The chapter ends with a brief summary.

5.1 Area,Power and Voltage Supply Results

In this section we summarize again the supply voltages of the implemented filters and present area and power consumption results. Data are given for 7 filters of the two implementations. The two 4.2MHz filters made with the Gm-C strategy for the initial design and the updated one after the IC analysis and the last 1.7MHz filter made with the same strategy after the IC analysis. Lastly the 4 filter versions(before and after IC calculation) made with the current mode OpAmps of 155MHz and 7.2MHz.

In terms of supply voltage of the filters the values are from 1.5V to 1V. Specifically For the Gm-C implementations the initial 4.2MHz filter operates at 1.5V. In more detail 3 of the sub circuits, startup circuit, the current reference and the transconductor are operating with a 0.5V supply. The driver in order for the filter to operate needs to work at 1.5V for this cut-off frequency. For the implementation after the new choice of transistor dimensions voltage supply is actually less for the same amplitude. The 4.2MHz filter still operates at 1.5V with an amplitude of about 5.5db less. Equal behavior to the original filter we get at 1.45V supply for the driver amplifier at a cut-off of 1.7MHz as mentioned before. Compared to the original 1MHz current mode filter all supply voltages are lower. The original implementation had a 3V supply voltage. That shows 50% reduction in supply voltage for the two 4.2MHz Gm-C filters and 52% for the 1.7MHz. Compared to the current mode OpAmp implementations the difference is greater. The 155MHz filter has a 66% lower supply before and 74% after re-designing compared to the first filter. For the 7.2GHz filters the difference is 50% and 55% before and after the IC analysis.

Filter	Supply Voltage [V]	Area [mm^2]	Power cons.[mW]
Original Gm-C 1MHz	3	21.51	-
First Gm-C 4.2MHz	1.5	0.55	3
Gm-C 4.2MHz after IC	1.5	0.098	2.8
Gm-C 1.7MHz after IC	1.45	0.098	2.7
First CM OpAmp 155MHz	1	0.121	21.7
First CM OpAmp 7.2GHz	1.5	0.121	22.1
CM OpAmp 155MHz after IC	0.78	0.13	17.3
CM OpAmp 7.2GHz after IC	1.35	0.1	19.4

Table 5.1: Voltage supply, Area and Power result of the original filter and all Gm-C and current mode operational amplifier implementations.

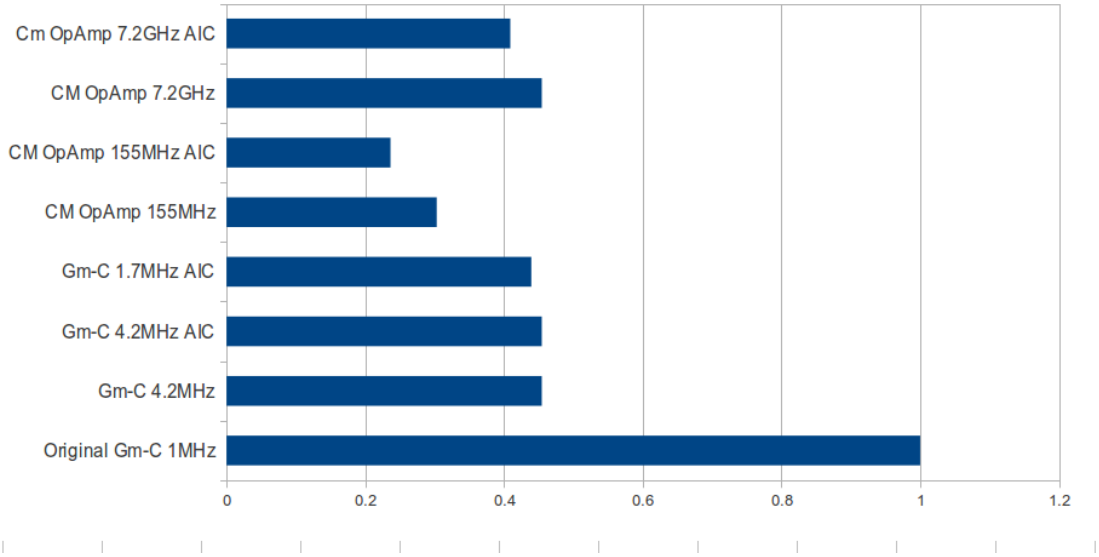

Figure 5.1: Voltage Supply of filters normalized to the supply of the original 1MHz filter(AIC - After IC analysis).

In terms of area we shall consecrate purely on the transistor area which is directly linked to the design.Then this will also be compared to the original Gm-C filter. The initial filter has a transistor area of $21.51mm^2$.In detail the 3 integrator blocks have a transistor area of $18.69mm^2$, the current reference about $2.56mm^2$ and the startup circuit has an area of $0.26mm^2$. Naturally the implemented filters will have substantially less transistor area since the used technology is a 0.25um process, plus that the CM OpAmp is considerably less complex than the Gm-C design.

For the Gm-C filter the initial design has a total area for the integrator structures of $0.38mm^2$. The current reference about $0.048mm^2$ and the startup circuit of about $0.006mm^2$. This adds to a total transistor area of $0.55mm^2$. For the second implemen-

Filter	Phase Margin [degrees]
First Gm-C 4.2MHz	135.4
Gm-C 4.2MHz after IC	135.6
Gm-C 1.7MHz after IC	135.4
First CM OpAmp 155MHz	156.1
First CM OpAmp 7.2GHz	170.1
CM OpAmp 155MHz after IC	150.5
CM OpAmp 7.2GHz after IC	169.9

Table 5.2: Phase margin for all implemented filters

tation, made according to the ICs analysis, the total area was $0.098mm^2$.

Total integrator area was $0.055mm^2$, the current reference area $0.012mm^2$ and start up circuit about $0.031mm^2$.

For the current mode implementation we initially have the same transistor area for both 155MHz and the 7.2Mhz filters. For the 2 initial implementations each 2 output differentiator has a transistor area of $0.039mm^2$ and the 3 output has an area of $0.043mm^2$.This accounts for a total area of $0.121mm^2$.For the implementations after the IC analysis, the 155Mhz filter has a total transistor area of $0.13mm^2$($0.042mm^2$ for the 2 output differentiator and $0.046mm^2$ for the 3 output one). For the 7.2GHz the 2 output block has a transistor area of $0.032mm^2$ and the 3 output $0.036mm^2$. This accounts for total transistor area of $0.1mm^2$.

In terms of power dissipation we can see that the Gm-C implementation is at the levels of 3mW. The versions after IC show a slight decrease at 2.7 and 2.8mW. The CM OpAmp filters have higher level of power consumption. The initial 155MHz filter has a consumption of about 21.7mW while the 7.2Ghz around 22.1. Although this implementation is much simpler and achieves lower supply voltages the power is higher, due to the presence of high bias currents. For the versions after the IC analysis we can see a small decrease because of the lower voltages. About 20% for the 155MHz filter at 17.3mW and 12% for the second implementation at 19.4mW.

5.2 Phase Response and Margin

The phase response indicates the phase of the output in relevance to the input as a function of the frequency, measured in degrees. It is quite important for the behavior of systems using electronic amplifier, thus also active filters. One of the main reasons is that from the phase response the phase margin can be derived. The phase margin is the difference of the phase with -180 degrees, for filters at the point of the cut-off frequency. The importance lies in that it is an indication of stability for the filter. Because of the intermediate blocks of the filter there is a time difference between input and output in the occurrence of a change in the input. If this difference is large enough the presence of the feedback will cause the oscillations in the filter. The phase margin can indicate relative stability, showing the tendency of the system to oscillate in the case of a input

change.

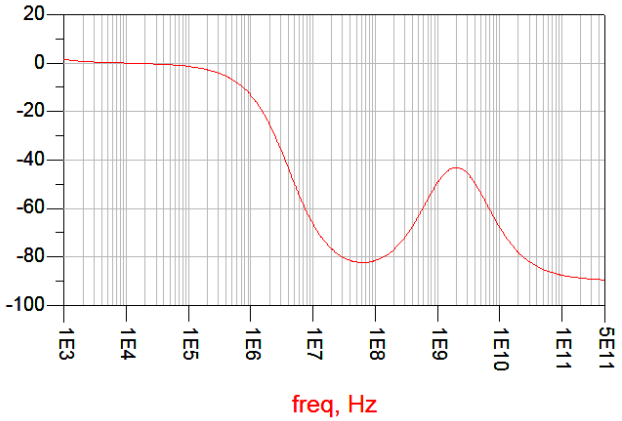

Figure 5.2: Phase Response for the first 4.2MHz Gm-C filter. Cut-off point at -44.6 degrees.

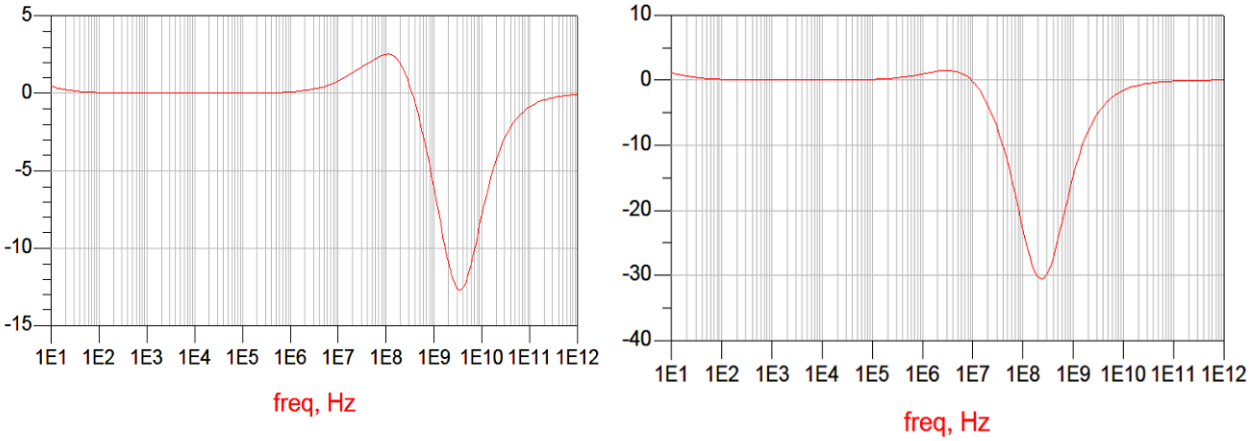

Figure 5.3: Phase Response for initial CM OpAmp 7.2GHz and 155MHz filters.Cut-off points at -9.9 and -28.4 degrees respectively.

In theory any value of the phase margin above 0 degrees is considered stable. In truth the theoretical margin can often be reduced by other factors, such as loads for example. That is why the margin needs to be substantially larger that 0, at least 45 degrees. Often circuits are theoretically designed to have a margin around 60 degrees to make sure that in practice the minimum 45 degrees are achieved.

The phase responses of all filter can be seen in following figures(5.2-5.5) and from there calculate the phase margins.

Phase margin results can be seen in Table 5.2.We can see that the phase margin for our first Gm-C implementation (4.2MHz) is 135.4 degrees. For the 2 CM OpAmp

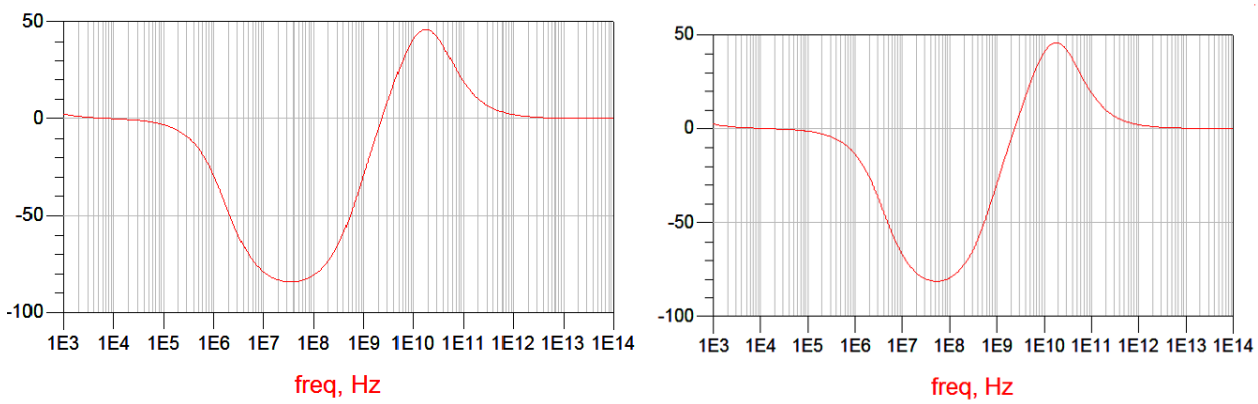

Figure 5.4: Phase Response for 1.7MHz and 4.2MHz Gm-C filters after IC analysis..Cut-off points at -44.6 and -45 degrees respectively.

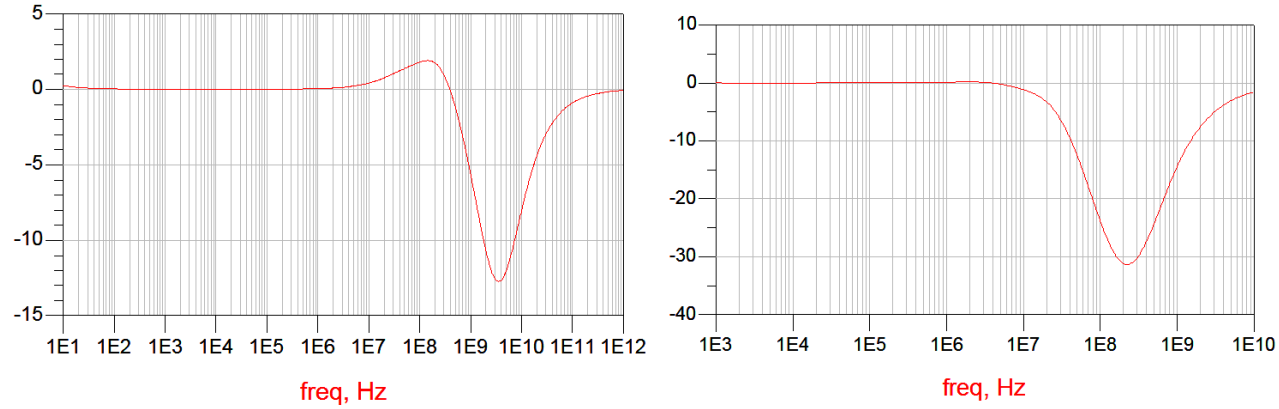

Figure 5.5: Phase Response for CM OpAmp 7.2GHz and 155MHz filters after IC analysis.Cut-off points at -10.1 and -29.5 degrees respectively.

implementations, the 155MHz filter has a phase margin of 156.1 degrees and the 7.2GHz a phase margin of 170.1. For the filter version created after the IC analysis the phase margin is similar. Specifically the 1.7MHz Gm-C filter has a phase margin of 135.6 and the 4.2MHz filter 135.4. For the CM OpAmp implementations the margins are 150.5 and 169.9 degrees for the 155MHz and the 7.2GHz filter respectively.

5.3 Filter Tunability

One interesting aspect is the tunability of the final filters in terms of cut-off frequency. Specifically in the Gm-C implementation it is the driver supply voltage that plays a significant role in filter behavior, basically the cut-off frequency. The filter in this configuration operates with a voltage supply between 1.4V-1.6V for the driver with an

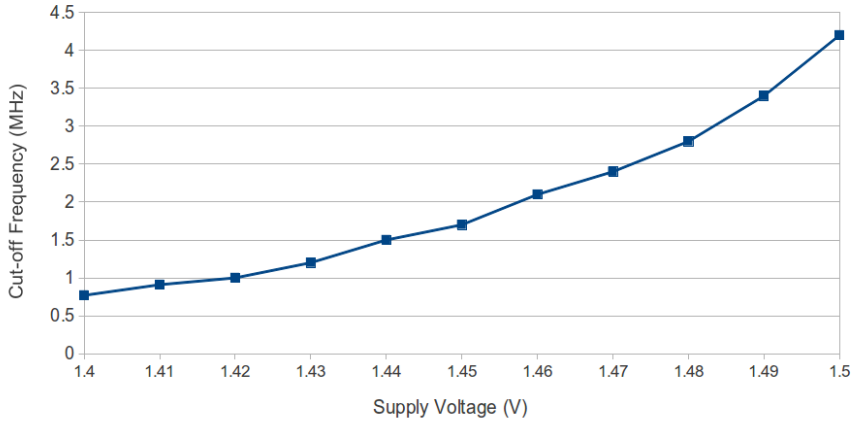

Figure 5.6: Gm-C filter tunability in relation to (Driver) supply voltage.

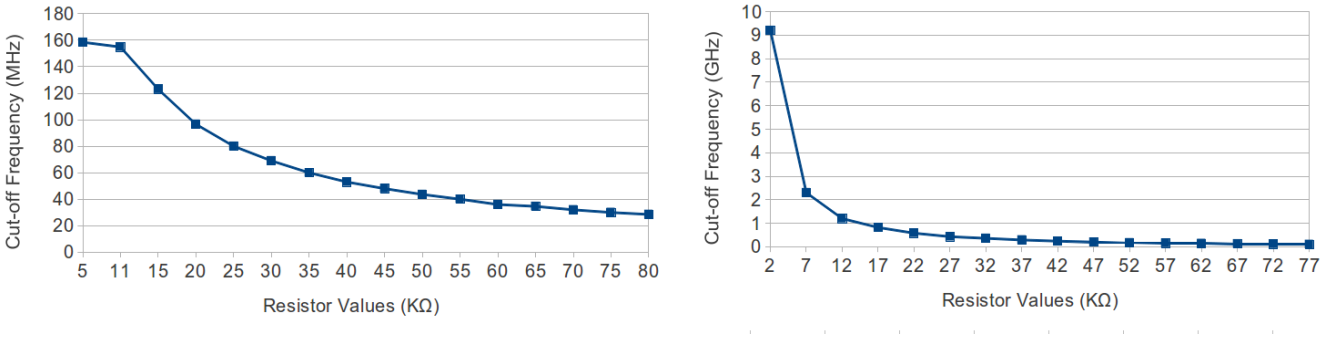

Figure 5.7: CM OpAmp filters' tunability in relation to differentiator resistor values.

appropriate change in cut-off frequency. The OpAmp implementations, on the other hand, follow a behavior similar to its voltage mode counterpart. Differentiator behavior is linked to the resistor values on each differentiator block in the filter. So it would be useful to assess the filter operating frequency in relevance to the resistor values in the filter sub-parts.

Figures 5.6-5.7 show this aspect for the final filters designed according to the IC analysis.In the graph for the Gm-C filter we can see the cut-off frequency as a function of the driver supply voltage in the span between 1.4V-1.5V. For the CM OpAmp filter the frequency is showed as a function of differentiator resistor values in the span between 5KΩ and 80KΩ for the 155MHz implementation and the span of 2KΩ to 77KΩ for the 7.2GHz implementation.

For the Gm-C filter, for this voltage span, the cut-off frequency has a relative steady increase with cut-off the frequencies ranging from 770KHz at 1.4V to 4.2MHz at 1.5V of supply voltage. For the first CM OpAmp implementation the cut-off frequency decreases, as the resistors increase, by a relatively smooth rate, from 158MHz at 5KΩ to 28.5Mhz at 80KΩ. For the second implementation the decrease rate is quite high for 2KΩ to

12KΩ resistors and this rate steadily became quite low as the resistor values increase. The cut-off frequency is at 9.2GHz at 2KΩ and at 100KHz at 77KΩ.

5.4 Transistor Mismatch Estimation

One important aspect in analog design is the matter of transistor matching. In real life devices there are time independent differences in behavior between devices of the same technology and dimensions. These differences are defined as transistor mismatches. Even the slightest difference in threshold voltage, for example, between two identically designed and used transistors may have impact in circuit performance, for both analog and digital designs. The constant reduction in size makes mismatch an increasingly important matter.

Mismatch can occur either by systemic sources, that have to do with the mechanical or chemical effect of the fabrication process, or by random errors during the the same fabrication process. Mismatch analysis is done based on two parameters that are characterized by the device technology. The threshold voltage mismatch (or A_{VT}) and the current factor mismatch (or A_B). For the differential pair, for a given drain current, it is the gate voltage mismatch(which is basically the threshold voltage mismatch) that is crucial, while the drain current mismatch, for a given gate voltage, is the crucial matter in a current mirror. The mismatch calculation is done by the standard threshold voltage(or current factor for the current mismatch) variation, σ_T (or σ_B for the current mismatch). These are equal to :

$$\sigma_T = \frac{A_{VT}}{\sqrt{WL}} \tag{5.1}$$

and

$$\sigma_B = \frac{A_B}{\sqrt{WL}} \tag{5.2}$$

From these we calculate now either the current or voltage mismatch by the equations:

$$\sigma(\delta V_g) = \sqrt{\sigma_T^2 + (\frac{I_d}{g_m} * \sigma_B)^2} \tag{5.3}$$

and

$$\sigma(\frac{\delta I_d}{I_d}) = \sqrt{\sigma_B^2 + (\frac{g_m}{I_d} * \sigma_T)^2} \tag{5.4}$$

When can simplify the equations by assuming that mismatch is equal to:

$$\sigma(\delta V_g) = \sigma_T + (\frac{I_d}{g_m} * \sigma_B) \tag{5.5}$$

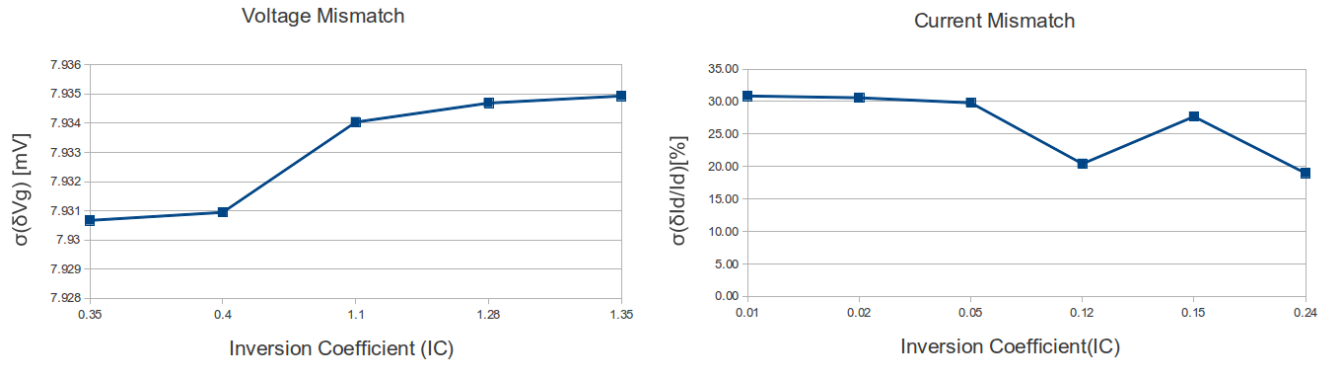

Figure 5.8: 1.7MHz Gm-C filter Current Mismatch for current mirrors and Voltage Mismatch for the differential pairs in the transconductor.

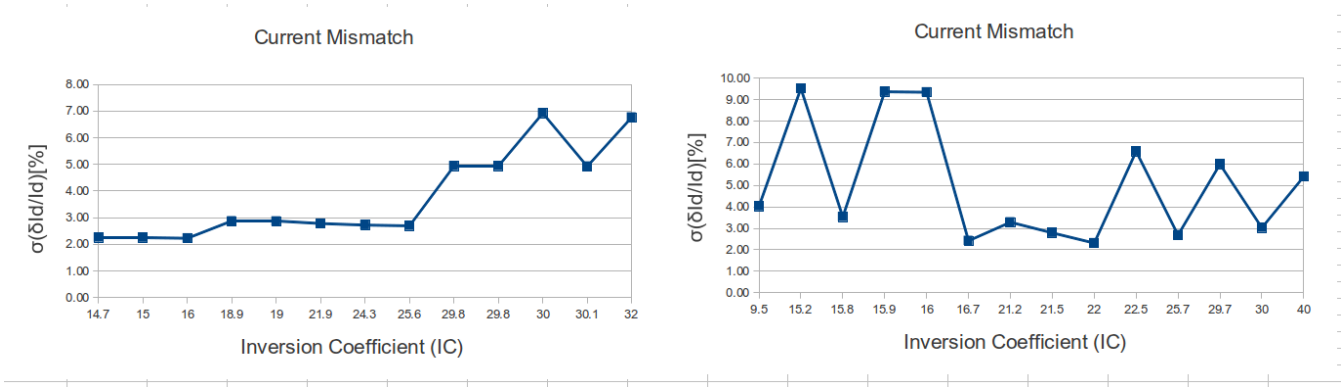

Figure 5.9: CM OpAmp filters'Current Mismatch for its current mirrors. The mismatch for the 155MHz and 7.2GHz filters are shown here respectively.

and

$$\sigma(\frac{\delta I_d}{I_d}) = \sigma_B + (\frac{g_m}{I_d} * \sigma_T) \tag{5.6}$$

Then using the normalized transconductance function G(IC) equal to :

$$G(IC) = \frac{1}{0.5 + \sqrt{0.25 + IC}} = \frac{g_m}{I_d} nU_T \tag{5.7}$$

We can now derive an expression that enables us to calculate mismatch as a function of the inversion coefficient. Specifically equations 5.5 and 5.6, using 5.1,5.2 and 5.7, become:

$$\sigma(\delta V_g) = (A_{VT} + A_B nU_T(0.5 + \sqrt{0.25 + IC}))/\sqrt{WL} \tag{5.8}$$

and

$$\sigma(\frac{\delta I_d}{I_d}) = (A_B + \frac{A_{VT}}{nU_T}\frac{1}{0.5+\sqrt{0.25+IC}})/\sqrt{WL} \tag{5.9}$$

Unfortunately the design kit used in the simulation does not have parameters for transistor mismatching. So accurate calculation of matching in simulation cannot be done. But if we assume logical values for the A_{VT} and A_B parameters we can make an estimation of matching for our final designs. The mismatch estimation was done for the crucial parts of the 2 filter designs. Basically we are interested in the matching of the differential pairs and current mirrors of the transconductors for the 4.2MHz Gm-C filter and the current mirrors of the 2 final CM OpAmp implementations. For the mismatch calculation we use A_{VT}= 7mVum and A_B = 1.5%um

In figures 5.8 and 5.9 we can see the results of the mismatch estimation in relation to the transistors' inversion coefficient. The Gm-C filter implementation has a reasonable mismatch in terms of voltage mismatch in the differential pairs around 7.9mV. In the current mirrors though the mismatch is significant ranging from 18% to almost 31%. In the two CM OpAmp implementation since we have only current mirrors we derive an estimation only in current mismatch. For the 155MHz filter the mismatch is estimated between 2.23% and 6.9%. For the 7.2GHz filter it is slightly larger between 2.3% and 9.5%.

5.5 Summary

In this chapter the characteristics and performance of the implemented filters were discussed.Firstly results were presented concerning the filters' supply voltage and transistor area and compared to the initial 1MHz Gm-C filter in which our first implementation was based. Also the power consumption of all implemented filters was shown. Then the phase response of the filters were shown and phase margins, which reflect stability, were computed. Finally the filter tunability was discussed. The Gm-C tunability graph was presented as a function of supply voltage, while the CM OpAmp implementations' tunability was presented as a function of the differentiator resistor values. In the final section we have a general estimation of current and voltage mismatch in the current mirrors and differential pairs of the final filter implementations. The next chapter concludes this thesis by drawing conclusions on the work and suggesting additional work on the subject.

6 Conclusions

In the process of this thesis we described the idea behind the current mode paradigm and its use in active filters. We attempted to explore the possibility of implementing filters previously designed for the voltage mode paradigm. For this purpose we described a ladder filter and its implementation with voltage mode operational amplifiers. Then we described a previously presented paradigm that implemented the ladder filter using current mode integrators based on the Gm-C strategy and attempted to recreate it with a newer, smaller 0.25um process. Then we also describe a CM OpAmp implementation and created another version of the filter directly translated from the voltage mode OpAmp implementation. Finally we optimized the all filters by doing a IC analysis to re-design transistor dimension to improve power and supply performance and behavior. Lastly data of all filters concerning transistor area, supply voltage, power, stability, tunability and transistor matching were presented. In the present chapter we shall make some conclusions based the results of the implementations and propose suggestions for future work.

6.1 Evaluation Conclusions

The purpose of using a smaller transistor process was to minimize supply voltage and area with reasonable power consumption and behavior. The question of how well a filter in current mode form could be implemented in smaller technology.

Especially for the Gm-C filter implementation this was an interesting matter since the transfer was from a 1.2um process to a 0.25um.It was obvious that the first design of the 4.2MHz filter, although generally worked, was not behaving close enough to the original design. This can be attributed to the fact that in that low voltage and currents transistors worked in deep or ultra deep weak inversion. Best operating level would be the beginning of strong inversion for the current sources and between strong and moderate inversion for the differential pairs. But in order not to radically change the length of the transistors we could not bring the transistor ratios to the values that were needed to reach these levels of inversion. The technology was limiting us in a minimum width of 0.33um. Yet, even if the needed spans could not be reached, the increase of the IC would still lead to better behavior. Just changing the ratios by a factor of 10 the new filter was improved in behavior coming closer to the expected.Also the low level of inversion would have a good effect in the differential pairs in the transconductor, as matching in low ICs is better for the pairs, although mismatch is still expected to be significant for the current mirrors since the transistors still worked generally in weak inversion.

The CM OpAmp filters were simpler to implement and could be translated directly from the voltage mode counterpart. Here the IC levels were high enough that the optimal

span of the IC for its current mirrors could easily be reached without significant change on the transistor lengths, providing good balance between matching and noise for the current mirrors, despite the low supply voltages. This design is quite simpler, as easily scalable as the Gm-C implementation and easily applicable to ladder filter designs. The simplicity on the other hand means that there would be a cost in behavior. One of these costs is the presence of a high passband ripple. Almost 0.8db for the 155MHz filter. The ripple is even higher at the 7.2GHz version almost at 1db. This is attributed to the fact that the decrease on the bias currents also leads to reduced OpAmp gain. After the IC analysis, the new choice of dimensions improved this aspect of performance. The passband ripple in the 155MHz is reduced to only 0.3db and even the high frequency filter has a reduction at about 0.8-0.9db.

In terms of supply voltage the reduction both from the use of the new technology and the IC analysis is quite high, compared the the original Gm-C filter of 1MHz. The original filter operated at 3V supply. This leads to a reduction between 50 and 52% in supply voltage,for the Gm-C implementation.For the CM OpAmp filters the reduction is even greater with maximum reduction in the 155MHz filter after the IC analysis of about 74%.Great was the reduction in area also, as would be expected with the newer technology. There should be mentioned here that this is just the transistor area. A huge part of the chip area would also be the passive components and especially capacitors that depending on how the are realized could have a great effect in total area.

In terms of power consumption we can see that the Gm-C has the lowest one, just in 2.8-2.7mW for the final versions. The CM OpAmp implementations are at 21.7 and 22.1 mW, quite higher than the Gm-C implementation due to the high bias current needed. The 155MHz filter has actually slightly better power consumption even though it has higher bias currents. This is attributed to the fact that the high frequency filter, even though it has lower bias, it also has lower gain and requires higher supply voltages.All versions seem to be slightly more efficient after the IC analysis. About 10% less for the Gm-C filters and 12-20% for the CM OpAmp designs.

General stability can be judged by the phase margin for each filter. All version are seen to be sufficiently stable, the lowest margin being that of the Gm-C filter at around 135 degrees. The 155MHz filter around 150 and the 7.2GHz one almost at 170 degrees. Also the phase margins seem to be quite unaffected by the new choice of dimensions after the IC analysis.

In terms of tunability the Gm-C implementation can produce filters operating from 0.77MHz to 4.2MHz for the voltage span from 1.4V to 1.5V, by tweaking the driver amplifier voltage. Greater tunability can be seen in the CM OpAmp implementations although in different frequency magnitudes. Using almost the same resistor value spans for both filters we have frequencies from 158 to 28MHz for the first version and 9.2GHz to 100KHz for the second. It must be pointed here that the Gm-C and first CM OpAmp filter have a relatively smooth tunability graph. On the other hand the slope of the graph for the high frequency OpAmp filter is very steep in the span between 2 and 12 kΩ, requiring very accurate resistors for correct tuning at these frequencies.

In the matching estimation we would expect reasonably good matching for the differential pairs in the Gm-C implementation, because of the low level of inversion while significant mismatch is expected in the current mirrors. Indeed the voltage mismatch for

the differential pairs transistors of the transconductors in the Gm-C filter is reasonable, around 7.9mV.Yet the mismatch of the current mirrors is significantly high at values from 18 to 30%. For the CM OpAmp implementations we expected much better mismatch estimations since the IC analysis in the original designs gave us a much more accommodating results to reach the IC values most optimal for transistor behavior. Especially for the 155MHz version that we expected the best matching results. For the 7.2GHz filter the current mismatch ranges from 2.3% to 9.5%, while better matching is provided in the 155MHz filter with a current mismatch from 2.23% to 6.9%.

All in all we can see that the Gm-C implementation is complex and works at low inversion levels, not achieving the best matching/noise trade-off(especially for the current mirrors of the transconductor), but has better behavior and power consumption than the CM OpAmp versions. They on the other hand have higher passband ripple, higher power consumption and potentially greater total area because of the presence of the compensation capacitors, but boast more design simplicity, greater tunability , lower voltage supplies and operation at more a optimal inversion level for the current mirrors leading to better matching, although also working at higher frequency levels. All versions have sufficient general stability. Both techniques can easily be used for a variety of different filters and can easily be used to implement all ladder active filter implementations.

6.2 Thesis Contributions

Through this thesis we achieved :

- To explore the possibility of using current mode strategies to implement active high frequency filter designs. The two strategies used were Gm-C filters and filters based on current mode operational amplifiers.
- To implement active filters using the Gm-C paradigm, that uses Transconductors as main amplifier blocks for its integrators, on 0.25um transistor technology. The filter design was a 3rd-order elliptical low-pass filter that operated at 4.2MHz.
- To implement the same filter design using integrator equivalent structures using the CM operational amplifier as their main building block that makes the migration from voltage to current mode design straightforward. The same filter type was used and the result were two filter versions: one at 155MHz and one at 7.2GHz.
- To do a Inversion Coefficient(IC) analysis of the critical parts of the circuit to use as a guide to re-design transistor dimensions for all implemented filters to optimize characteristics and behavior.
- To re-design the filters according to the IC parameter and produce the same filters, plus an additional example of the Gm-C filter at a cut-off frequency of 1.7MHz.
- To derive behavior and performance results to asses filter operation. The filters were analyzed and compared in terms of supply voltage, transistor area, power consumption, general stability, tunability and transistor matching.

6.3 Future work

Based on previous conclusions we can now make some suggestions on future work on the same subject:

- The assessments for the filter designs are made by simulation. An important factor would be how much the behavior shown in simulation can be preserved in real life. A realization of the filter on chip could give important conclusions on the filters' performance.
- The transistor process used here was a 0.25um technology. An interesting question would be the behavior of these filters implemented with even newer and smaller technologies, such as 0.18um, 0.13um and 0.09um technologies.
- These 2 strategies can also be used for any integrator based and ladder filter design. It would be an interesting question to explore the behavior of other ladder filters and of higher order implemented with these strategies in the current mode paradigm. Additionally these same filters could also be attempted to be designed and realized with newer technologies as mentioned above.
- Improvements could be made in the integrator designs to improve filter efficiency and performance. For example one suggestion would be to improve the CM OpAmp's gain to accomplish better behavior. This could be done by trying to increase impedance r_{oa} (in gain equation 4.13) by incorporating cascode current mirrors instead of the basic current mirror design in the original OpAmp. This would have the potential to achieve the same gain for lower bias currents in the circuit, thus potentially achieving same filter behavior with less power. Another idea would be to explore the possibility of better designs for the Gm-C integrator that improve transistor matching which seem to be a major issue in the design in such low dimensions and voltages.

Appendix: Parameter Information

A

A.1 Physical Constants and I_{spec} Estimation

Following are the tables presenting the measurements for the N factor and I_{spec} estimation and physical constants required for hand "theoretical" calculation of the Inversion Coefficient.

Constant	**Value**
Magnitude of electron charge q	$1.602 * 10^{-19}[C]$
Boltzmann constant K	$1.381 * 10^{-23}[J/K]$
Silicon Dioxide Permittivity E_{ox}	$3.45 * 10^{-11}[F/m]$
T_{ox}	$5.65 * 10^{-9}[m]$

I_d[**A**]	V_g[**V**]	**SQRT**(I_d)	**d**(**SQRT**(I_d))	**d**V_g	**d**(**SQRT**(I_d))/**d**V_g
1.01E-10	0.2	1.01E-005	1.51E-004	0.2	7.54E-04
2.59E-08	0.4	1.61E-004	1.66E-003	0.2	8.32E-03
3.33E-06	0.6	1.82E-003	6.81E-003	0.2	3.40E-02
7.45E-05	0.8	8.63E-003	8.50E-003	0.2	4.25E-02
2.93E-04	1	1.71E-002	7.78E-003	0.2	3.89E-02
6.20E-04	1.2	2.49E-002	6.71E-003	0.2	3.36E-02
1.00E-03	1.4	3.16E-002	5.79E-003	0.2	2.90E-02
1.40E-03	1.6	3.74E-002	6.63E-003	0.2	3.31E-02
1.94E-03	1.8	4.40E-002	4.94E-003	0.2	2.47E-02
2.40E-03	2	4.90E-002	5.78E-003	0.2	2.89E-02
3.00E-03	2.2	5.48E-002	3.54E-003	0.2	1.77E-02
3.40E-03	2.4	5.83E-002	4.94E-003	0.2	2.47E-02
4.00E-03	2.6	6.32E-002	3.84E-003	0.2	1.92E-02
4.50E-03	2.8	6.71E-002	3.63E-003	0.2	1.81E-02
5.00E-03	3	7.07E-002	-	-	-

Table A.1: Physical constants needed for hand calculation of IC and measurements for I_{spec} in NMOS with aspect ratio 12.5/0.63

I_d[**A**]	V_g[**V**]	**SQRT**(I_d)	**d**(**SQRT**(I_d))	**d**V_g	**d**(**SQRT**(I_d))/**d**V_g
4.76E-11	0.2	6.90E-06	1.02E-04	0.2	5.11E-04
1.19E-08	0.4	1.09E-04	1.14E-03	0.2	5.69E-03
1.56E-06	0.6	1.25E-03	4.76E-03	0.2	2.38E-02
3.61E-05	0.8	6.00E-03	6.01E-03	0.2	3.01E-02
1.44E-04	1	1.20E-02	5.52E-03	0.2	2.76E-02
3.07E-04	1.2	1.75E-02	5.02E-03	0.2	2.51E-02
5.09E-04	1.4	2.26E-02	4.59E-03	0.2	2.29E-02
7.37E-04	1.6	2.71E-02	4.20E-03	0.2	2.10E-02
9.82E-04	1.8	3.13E-02	3.30E-03	0.2	1.65E-02
1.20E-03	2	3.46E-02	4.09E-03	0.2	2.04E-02
1.50E-03	2.2	3.87E-02	2.50E-03	0.2	1.25E-02
1.70E-03	2.4	4.12E-02	3.49E-03	0.2	1.75E-02
2.00E-03	2.6	4.47E-02	2.18E-03	0.2	1.09E-02
2.20E-03	2.8	4.69E-02	3.10E-03	0.2	1.55E-02
2.50E-03	3	5.00E-02	-	-	-

Table A.2: Measurements for I_{spec} in NMOS with aspect ratio 6.25/0.63

I_d[**A**]	V_g[**V**]	**SQRT**(I_d)	**d**(**SQRT**(I_d))	**d**V_g	**d**(**SQRT**(I_d))/**d**V_g
3.71E-09	0.2	6.09E-05	8.05E-04	0.2	4.03E-03
7.50E-07	0.4	8.66E-04	6.87E-03	0.2	3.43E-02
5.98E-05	0.6	7.73E-03	1.75E-02	0.2	8.75E-02
6.37E-04	0.8	2.52E-02	1.95E-02	0.2	9.74E-02
2.00E-03	1	4.47E-02	1.01E-02	0.2	5.03E-02
3.00E-03	1.2	5.48E-02	8.47E-03	0.2	4.24E-02
4.00E-03	1.4	6.32E-02	1.42E-02	0.2	7.11E-02
6.00E-03	1.6	7.75E-02	6.21E-03	0.2	3.10E-02
7.00E-03	1.8	8.37E-02	5.78E-03	0.2	2.89E-02
8.00E-03	2	8.94E-02	9.55E-03	0.2	4.78E-02
9.80E-03	2.2	9.90E-02	5.89E-03	0.2	2.94E-02
1.10E-02	2.4	1.05E-01	4.66E-03	0.2	2.33E-02
1.20E-02	2.6	1.10E-01	4.47E-03	0.2	2.24E-02
1.30E-02	2.8	1.14E-01	8.46E-03	0.2	4.23E-02
1.50E-02	3	1.22E-01	-	-	-

Table A.3: Measurements for I_{spec} in NMOS with aspect ratio 20.8/0.25

I_d[**A**]	V_g[**V**]	**SQRT**(I_d)	**d**(**SQRT**(I_d))	**d**V_g	**d**(**SQRT**(I_d))/**d**V_g
3.92E-11	0.2	6.26E-06	9.23E-05	0.2	4.61E-04
9.71E-09	0.4	9.85E-05	1.03E-03	0.2	5.16E-03
1.28E-06	0.6	1.13E-03	4.33E-03	0.2	2.16E-02
2.98E-05	0.8	5.46E-03	5.48E-03	0.2	2.74E-02
1.20E-04	1	1.09E-02	5.03E-03	0.2	2.52E-02
2.55E-04	1.2	1.60E-02	4.58E-03	0.2	2.29E-02
4.23E-04	1.4	2.06E-02	4.19E-03	0.2	2.09E-02
6.12E-04	1.6	2.47E-02	3.84E-03	0.2	1.92E-02
8.17E-04	1.8	2.86E-02	3.04E-03	0.2	1.52E-02
1.00E-03	2	3.16E-02	3.02E-03	0.2	1.51E-02
1.20E-03	2.2	3.46E-02	2.78E-03	0.2	1.39E-02
1.40E-03	2.4	3.74E-02	2.58E-03	0.2	1.29E-02
1.60E-03	2.6	4.00E-02	3.59E-03	0.2	1.79E-02
1.90E-03	2.8	4.36E-02	2.24E-03	0.2	1.12E-02
2.10E-03	3	4.58E-02	-	-	-

Table A.4: Measurements for I_{spec} in NMOS with aspect ratio 5.2/0.63

I_d[**A**]	V_g[**V**]	**SQRT**(I_d)	**d**(**SQRT**(I_d))	**d**V_g	**d**(**SQRT**(I_d))/**d**V_g
8.02E-10	0.2	2.83E-05	3.76E-04	0.2	1.88E-03
1.63E-07	0.4	4.04E-04	2.96E-03	0.2	1.48E-02
1.14E-05	0.6	3.37E-03	9.02E-03	0.2	4.51E-02
1.54E-04	0.8	1.24E-02	8.19E-03	0.2	4.09E-02
4.23E-04	1	2.06E-02	6.66E-03	0.2	3.33E-02
7.42E-04	1.2	2.72E-02	5.93E-03	0.2	2.96E-02
1.10E-03	1.4	3.32E-02	4.65E-03	0.2	2.33E-02
1.43E-03	1.6	3.78E-02	4.40E-03	0.2	2.20E-02
1.78E-03	1.8	4.22E-02	3.87E-03	0.2	1.93E-02
2.12E-03	2	4.61E-02	3.74E-03	0.2	1.87E-02
2.48E-03	2.2	4.98E-02	3.36E-03	0.2	1.68E-02
2.83E-03	2.4	5.32E-02	3.03E-03	0.2	1.52E-02
3.16E-03	2.6	5.62E-02	2.95E-03	0.2	1.47E-02
3.50E-03	2.8	5.92E-02	2.73E-03	0.2	1.37E-02
3.83E-03	3	6.19E-02	-	-	-

Table A.5: Measurements for I_{spec} in NMOS with aspect ratio 5.2/0.25

I_d[**A**]	V_g[**V**]	**SQRT**(I_d)	**d**(**SQRT**(I_d))	**d**V_g	**d**(**SQRT**(I_d))/**d**V_g
-3.98E-04	-3	2.00E-02	-1.33E-03	0.2	-6.67E-03
-3.47E-04	-2.8	1.86E-02	-1.39E-03	0.2	-6.94E-03
-2.97E-04	-2.6	1.72E-02	-2.24E-03	0.2	-1.12E-02
-2.25E-04	-2.4	1.50E-02	-7.08E-04	0.2	-3.54E-03
-2.04E-04	-2.2	1.43E-02	-1.57E-03	0.2	-7.83E-03
-1.62E-04	-2	1.27E-02	-1.62E-03	0.2	-8.12E-03
-1.23E-04	-1.8	1.11E-02	-1.70E-03	0.2	-8.48E-03
-8.84E-05	-1.6	9.40E-03	-1.76E-03	0.2	-8.81E-03
-5.84E-05	-1.4	7.64E-03	-1.83E-03	0.2	-9.16E-03
-3.38E-05	-1.2	5.81E-03	-1.90E-03	0.2	-9.52E-03
-1.53E-05	-1	3.91E-03	-1.95E-03	0.2	-9.74E-03
-3.83E-06	-0.8	1.96E-03	-1.51E-03	0.2	-7.54E-03
-2.03E-07	-0.6	4.51E-04	-4.07E-04	0.2	-2.03E-03
-1.94E-09	-0.4	4.40E-05	-4.09E-05	0.2	-2.05E-04
-9.56E-12	-0.2	3.09E-06	-	-	-

Table A.6: Measurements for I_{spec} in PMOS with aspect ratio 6.25/1.25

I_d[**A**]	V_g[**V**]	**SQRT**(I_d)	**d**(**SQRT**(I_d))	**d**V_g	**d**(**SQRT**(I_d))/**d**V_g
-6.61E-04	-3	2.57E-02	-2.23E-03	0.2	-1.12E-02
-5.51E-04	-2.8	2.35E-02	-1.06E-03	0.2	-5.32E-03
-5.02E-04	-2.6	2.24E-02	-1.78E-03	0.2	-8.88E-03
-4.26E-04	-2.4	2.06E-02	-1.87E-03	0.2	-9.33E-03
-3.52E-04	-2.2	1.88E-02	-1.97E-03	0.2	-9.83E-03
-2.82E-04	-2	1.68E-02	-2.07E-03	0.2	-1.04E-02
-2.17E-04	-1.8	1.47E-02	-2.18E-03	0.2	-1.09E-02
-1.58E-04	-1.6	1.25E-02	-2.30E-03	0.2	-1.15E-02
-1.05E-04	-1.4	1.03E-02	-2.41E-03	0.2	-1.21E-02
-6.14E-05	-1.2	7.84E-03	-2.54E-03	0.2	-1.27E-02
-2.80E-05	-1	5.30E-03	-2.63E-03	0.2	-1.32E-02
-7.08E-06	-0.8	2.66E-03	-2.05E-03	0.2	-1.02E-02
-3.75E-07	-0.6	6.12E-04	-5.53E-04	0.2	-2.76E-03
-3.54E-09	-0.4	5.95E-05	-5.83E-05	0.2	-2.91E-04
-1.54E-12	-0.2	1.24E-06	-	-	-

Table A.7: Measurements for I_{spec} in PMOS with aspect ratio 5.2/0.63

I_d[**A**]	V_g[**V**]	**SQRT**(I_d)	**d**(**SQRT**(I_d))	**d**V_g	**d**(**SQRT**(I_d))/**d**V_g
-1.80E-03	-3	4.24E-02	-1.20E-03	0.2	-5.98E-03
-1.70E-03	-2.8	4.12E-02	-2.50E-03	0.2	-1.25E-02
-1.50E-03	-2.6	3.87E-02	-2.67E-03	0.2	-1.34E-02
-1.30E-03	-2.4	3.61E-02	-2.89E-03	0.2	-1.44E-02
-1.10E-03	-2.2	3.32E-02	-2.20E-03	0.2	-1.10E-02
-9.59E-04	-2	3.10E-02	-3.09E-03	0.2	-1.55E-02
-7.77E-04	-1.8	2.79E-02	-3.34E-03	0.2	-1.67E-02
-6.02E-04	-1.6	2.45E-02	-3.60E-03	0.2	-1.80E-02
-4.38E-04	-1.4	2.09E-02	-3.89E-03	0.2	-1.94E-02
-2.91E-04	-1.2	1.71E-02	-4.20E-03	0.2	-2.10E-02
-1.65E-04	-1	1.28E-02	-4.56E-03	0.2	-2.28E-02
-6.86E-05	-0.8	8.28E-03	-4.74E-03	0.2	-2.37E-02
-1.26E-05	-0.6	3.55E-03	-2.91E-03	0.2	-1.45E-02
-4.12E-07	-0.4	6.42E-04	-5.92E-04	0.2	-2.96E-03
-2.51E-09	-0.2	5.01E-05	-	-	-

Table A.8: Measurements for I_{spec} in PMOS with aspect ratio 5.2/0.25

I_d[**A**]	V_g[**V**]	**SQRT**(I_d)	**d**(**SQRT**(I_d))	**d**V_g	**d**(**SQRT**(I_d))/**d**V_g
-3.60E-03	-3	6.00E-02	-3.43E-03	0.2	-1.72E-02
-3.20E-03	-2.8	5.66E-02	-4.61E-03	0.2	-2.30E-02
-2.70E-03	-2.6	5.20E-02	-4.00E-03	0.2	-2.00E-02
-2.30E-03	-2.4	4.80E-02	-4.37E-03	0.2	-2.18E-02
-1.90E-03	-2.2	4.36E-02	-4.86E-03	0.2	-2.43E-02
-1.50E-03	-2	3.87E-02	-4.09E-03	0.2	-2.04E-02
-1.20E-03	-1.8	3.46E-02	-4.95E-03	0.2	-2.48E-02
-8.81E-04	-1.6	2.97E-02	-6.89E-03	0.2	-3.45E-02
-5.20E-04	-1.4	2.28E-02	-4.12E-03	0.2	-2.06E-02
-3.49E-04	-1.2	1.87E-02	-5.95E-03	0.2	-2.97E-02
-1.62E-04	-1	1.27E-02	-6.18E-03	0.2	-3.09E-02
-4.29E-05	-0.8	6.55E-03	-4.97E-03	0.2	-2.48E-02
-2.50E-06	-0.6	1.58E-03	-1.42E-03	0.2	-7.11E-03
-2.53E-08	-0.4	1.59E-04	-1.49E-04	0.2	-7.47E-04
-9.63E-11	-0.2	9.81E-06	-	-	-

Table A.9: Measurements for I_{spec} in PMOS with aspect ratio 28.6/0.63

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