NANOSCALE RF CMOS TRANSCEIVER DESIGN

Angelos Antonopoulos

Dipl. Eng., MSc.

A dissertation submitted for the degree of Doctor of Philosophy
in the Electronics & Computer Engineering Department,
Technical University of Crete
Chania, February 2013

Examinatory Committee:

Assistant Professor Matthias Bucher, Supervisor
Professor Yannis Papananos, Co-Supervisor
Professor Christian Enz, Co-Supervisor
Assistant Professor Aggelos Bletsas
Associate Professor Spyros Vlassis
Professor Alexis Birbas
Professor Michael Schröter

Η παρούσα έρευνα έχει συγχρηματοδοτηθεί από την Ευρωπαϊκή Ένωση (Ευρωπαϊκό Κοινωνικό Ταμείο - ΕΚΤ) και από εθνικούς πόρους μέσω του Επιχειρησιακού Προγράμματος «Εκπαίδευση και Δια Βίου Μάθηση» του Εθνικού Στρατηγικού Πλαισίου Αναφοράς (ΕΣΠΑ) – Ερευνητικό Χρηματοδοτούμενο Έργο: Ηράκλειτος ΙΙ . Επένδυση στην κοινωνία της γνώσης μέσω του Ευρωπαϊκού Κοινωνικού Ταμείου.

Acknowledgements

This work has been performed under financial support from the Research Funding Program HERACLEITUS II, co-financed by the European Union (European Social Fund-ESF) and Greek national funds through the Operational Program "Education and Lifelong Learning" of the National Strategic Reference Framework (NSRF).

I would like to express my gratitude to Professor Matthias Bucher, who has been an inspiration for me over the last 8 years. We started working together through my Master Thesis and ended up with this work. All over these years his ideas and supervision have been instructive and his persistence crucial on realizing that failure may lead to success. He has always been there for his students and I strongly believe that without his guidance this Thesis would not have been completed. I feel blessed to be given the chance to work with him.

Special thanks go to Professors Christian Enz and Yannis Papananos who accepted being co-supervisors of this Thesis. Their work on analog design and modeling is invaluable and has helped me in many ways. Moreover, they have made themselves available when needed.

I would also like to thank the members of the examination committee, Professors Angelos Bletsas, Alexis Birbas and Spyros Vlassis. Professor Birbas was one of the first to investigate thermal noise in MOSTs and his contribution on understanding the noise physics has been critical for the microelectronics community.

Professor Schröter and Dr. Sakalas have played an important role in this Thesis. They were willing to make their lab at TU Dresden available. Moreover through their useful comments their contribution has been crucial in several publications.

The microelectronics group of the Electronics laboratory of Technical University of Crete consists of colleagues with great knowledge and excellent character. We have been united all these years and have succeeded many things through our collaboration. So, Nikolaos Mavredakis, Konstantinos Papathanasiou, Rupendra Sharma, Marianna Chalkiadaki, it was a pleasure to work with you. Among all colleagues I would like to thank Nikolaos Makris whose contribution on setting up the lab, from equipment to software, has been of great significance. He is a colleague and friend of exceptional quality and has stood next to me, in difficult times.

My friends, Georgios Papoutsoglou, Yannis Zisos, Periklis Syros have been next to me all these years and I feel grateful for this. Anastasia Verganelaki has beared a lot standing next to me and I hope I will be able to give this back to her.

Finally, I would like to thank me beloved parents Sotiria and Kostas. I owe them everything, and dedicate them this work.

Abstract

Over the years CMOS has prevailed as the dominant technology for analog and radio frequency integrated circuit (RFIC) design, due to its high performance-to-cost ratio and the fast pace of market introduction, compared to other technologies. With the integration of digital and analog blocks on a single chip (SoC), the technology choice is dictated by the digital domain since it highly benefits from the advantages of downscaling. Thus, CMOS technologies down to the deca-nanometer regime have been proposed and implemented, with technologies of 45 nm and 30 nm currently being state-of-the-art. However, a large amount of RFIC design is still performed using technology nodes with channel length of 180 nm and 90 nm. The latter is widely considered as sweet-spot for RF CMOS circuit design and hence has been widely used for mm-wave circuit design, covering frequencies up to 100 GHz and even above.

The demand for ultra low voltage/ultra low power circuits becomes more imperative with technology scaling and supply voltage reduction, requiring advanced design techniques to exploit the scaling capabilities and alleviate its limitations. This thesis provides guidelines for low-power (LP) RFIC design, focusing on low-noise amplifier (LNA) design, by implementing, measuring, characterizing, and modeling a 90 nm CMOS LP process, from DC to RF. De-embedding is applied to RF and noise measurements in order to remove parasitics inserted from pads and interconnect lines from the device-under-test (DUT).

The RF noise behavior of the examined technology node, has been covered by modeling the measured noise parameters, namely NF_{min}, R_n, Γ_{opt}, over a wide range of measured frequencies, bias points, and channel lengths. Power spectral densities of drain current noise, gate current noise, as well their correlation are presented. Model parameters essential for circuit design, e.g., excess noise factor, γ, and thermal noise parameter, δ are verified with measurements for the first time, for various channel lengths over the channel inversion level. The influence of short-channel effects on the noise characteristics is presented and RF noise scaling trends are introduced. The optimum bias point for noise matching of the investigated 90 nm CMOS process is obtained close to moderate inversion (M.I.) and is shown to be shifted to inversion levels within the M.I. region, as channel length decreases.

Small signal characterization and modeling of active devices is performed and conventional as well as more complex figures of Merit (FoMs), recently proposed, such as transconductance frequency product, are examined. Measurements, for the 90 nm case, and technology computer-aided design (TCAD) simulations for technology nodes of nominal channel lengths ranging from 180 nm to 22 nm are used, revealing the great potential of downscaling on the overall performance of RF circuits, despite their certain drawbacks. The upper bound of dynamic range, set by the device non-linearities, and exported by DC as well as RF measurements is also

examined in terms of 1 dB compression point, P_{1dB}, and third-order intercept points, P_{IP3} and V_{IP3}, and their scaling trends with respect to inversion level are indicated.

Results are validated with the charge-based EKV3 compact model which takes into account short channel effects such as channel length modulation, velocity saturation and carrier heating and its accuracy and scalability are demonstrated.

Eventually, circuit implications of the above-mentioned individual and combined MOSFETs' characteristics are presented. Optimum design of a low power cascode LNA at 5 GHz is achieved using the extracted EKV3 model and following the guidelines resulting from the noise and small-signal analysis of the investigated process. The circuit is biased in the M.I. region showing an overall exceptional performance in terms of power consumption, noise, and gain. Moreover a single-stage 30 GHz LNA is implemented and measured in 90 nm CMOS, achieving high performance, compared to multi-stage architectures.

Περίληψη

Τα τελευταία χρόνια, η τεχνολογία CMOS έχει επικρατήσει, αποκτώντας κυρίαρχο ρόλο στην σχεδίαση αναλογικών κυκλωμάτων και ολοκληρωμένων κυκλωμάτων πολύ υψηλών συχνοτήτων (RFIC). Αυτό συμβαίνει κυρίως λόγω του υψηλού λόγου απόδοσης προς κόστος και της γρήγορης εισαγωγής και ενσωμάτωσης τους στο πεδίο της μικροηλεκτρονικής, συγκριτικά με άλλες τεχνολογίες. Με την ενσωμάτωση και συνύπαρξη στο ίδιο chip, αναλογικών και ψηφιακών κυκλωμάτων, η επιλογή της τεχνολογίας σχεδίασης καθορίζεται από το ψηφιακό κομμάτι, αφού αυτό εκμεταλλεύεται στο έπακρο τα πλεονεκτήματα της μείωσης του μήκους καναλιού. Έτσι λοιπόν, CMOS τεχνολογίες της τάξης των δεκάδων νανομέτρων έχουν προταθεί και υλοποιηθεί, με τεχνολογίες των 45 nm και 30 nm, να θεωρούνται αιχμή της τεχνολογίας. Ωστόσο, σημαντικός αριθμός σχεδίασης RF κυκλωμάτων πραγματοποιείται κάνοντας χρήση δομών με μήκος καναλιού 180 nm και 90 nm. Η τεχνολογία των 90 nm θεωρείται κομβική για την σχεδίαση RF κυκλωμάτων κι έτσι χρησιμοποιείται ευρέως, ακόμα και σε συχνότητες άνω των 100 GHz.

Η ανάγκη για κυκλώματα πολύ χαμηλής τροφοδοσίας και κατανάλωσης γίνεται πιο επιτακτική με την σμίκρυνση των CMOS τεχνολογιών και την αντίστοιχη μείωση της τάσης τροφοδοσίας, απαιτώντας προηγμένες τεχνικές σχεδίασης για την αξιοποίηση των πλεονεκτημάτων που προκύπτουν από την μείωση του μήκους καναλιού και την ελάφρυνση των αντίστοιχων μειονεκτημάτων. Η παρούσα διατριβή, παρέχει κατευθυντήριες γραμμές για σχεδίαση RF κυκλωμάτων, πολύ χαμηλής κατανάλωσης, εστιάζοντας στην σχεδίαση ενισχυτών χαμηλού θορύβου (LNA). Για τον σκοπό αυτό, έχει υλοποιηθεί, μετρηθεί, χαρακτηριστεί και μοντελοποιηθεί τεχνολογία 90 nm της TSMC, από συνθήκες μηδενικής συχνότητας (DC) μέχρι RF. Οι παρασιτικές χωρητικότητες που εμφανίζονται στις μετρήσεις RF και θορύβου, λόγω της ύπαρξης των δομών για την ηλεκτρική επαφή (pads) και των γραμμών μεταφοράς, έχουν αφαιρεθεί από τις δομές που μελετήθηκαν, μέσω συγκεκριμένων τεχνικών (de-embedding).

Η συμπεριφορά του RF θορύβου της εξεταζόμενης τεχνολογίας έχει καλυφθεί μοντελοποιώντας τις μετρούμενες παραμέτρους θορύβου, συγκεκριμένα του ελάχιστου παράγοντα θορύβου (NF_{min}), της ισοδύναμης αντίστασης θορύβου (R_n) και του παράγοντα ανάκλασης στην είσοδο (Γ_{opt}), σε ένα μεγάλο εύρος συχνοτήτων, σημείων πόλωσης και μήκους καναλιού. Η φασματική πυκνότητα ισχύος του θορύβου του ρεύματος καναλιού, του ρεύματος πύλης και της συσχέτισης τους αναλύεται εκτενώς. Παράμετροι θορύβου, με βαρύνουσα σημασία στην σχεδίαση RF κυκλωμάτων, όπως ο παράγοντας θορύβου γ, και η παράμετρος θερμικού θορύβου, δ, μοντελοποιούνται και επαληθεύονται μέσω μετρήσεων για πρώτη φορά, για διάφορα μήκη καναλιού, ως προς έναν χαρακτηριστικό δείκτη αντιστροφής στο κανάλι του MOS transistor, ονόματι δείκτης

αναστροφής. Η επίδραση των φαινομένων κοντού καναλιού στα χαρακτηριστικά του θορύβου μελετάται και η συμπεριφορά των χαρακτηριστικών αυτών με την μείωση του μήκους καναλιού εισάγεται και παρουσιάζεται. Το βέλτιστο σημείο πόλωσης για την ελαχιστοποίηση του θορύβου, της εξεταζόμενης 90 nm CMOS τεχνολογίας, επιτυγχάνεται κοντά σε μέτρια επίπεδα αναστροφής και φαίνεται να μετατοπίζεται προς το μέσο της περιοχής μέτριας αναστροφής, με την μείωση του μήκους καναλιού.

Η RF απόδοσή των ενεργών δομών της τεχνολογίας μελετάται μέσω του χαρακτηρισμού και της μοντελοποίησης μικρού σήματος. Κλασσικοί, αλλά και πιο προηγμένοι δείκτες απόδοσης, που έχουν προταθεί πρόσφατα, χρησιμοποιούνται για να περιγράψουν τις δυνατότητες των δομών να ενισχύουν ασθενή σήματα έως πολύ υψηλές συχνότητες. Για τον σκοπό αυτό, έχουν χρησιμοποιηθεί μετρήσεις για την 90 nm τεχνολογία, καθώς επίσης και δεδομένα μέσω προσομοίωσης σε υπολογιστή (TCAD), για τεχνολογίες με ονομαστικά μήκη καναλιού από 180 έως 22 nm. Απ΄ τα εν λόγω δεδομένα προκύπτουν τα σημαντικά πλεονεκτήματα της σμίκρυνσης του μήκους καναλιού, μέσω της εισαγωγής προηγμένων τεχνολογιών, στη συνολική RF απόδοση των ολοκληρωμένων κυκλωμάτων. Το άνω όριο του δυναμικού εύρους των κυκλωμάτων, το οποίο καθορίζεται από τις μη-γραμμικότητες, και το οποίο εξάγεται από DC και RF μετρήσεις, αναλύεται επίσης μέσω αντίστοιχων δεικτών απόδοσης. Τέτοιους δείκτες αποτελούν το σημείο συμπίεσης κατά 1 dB, και το σημείο τομής των προϊόντων τρίτης τάξης με τη συνιστώσα του σήματος στην κύρια συχνότητα. Όλοι οι δείκτες εξετάζονται ως προς το μήκος καναλιού και τον δείκτη αντιστροφής, παρουσιάζοντας αντίστοιχη συμπεριφορά με τους δείκτες θορύβου.

Τα αποτελέσματα επικυρώνονται με το συμπαγές μοντέλο EKV3, το οποίο βασίζεται στην θεωρία φορτίων και το οποίο λαμβάνει υπόψη τα φαινόμενα κοντού μήκους καναλιού, όπως η διαμόρφωση μήκους καναλιού, ο κορεσμός της ταχύτητας και η αύξηση της θερμότητας των φορέων. Η ακρίβεια και επεκτασιμότητά του, επιδεικνύονται σε όλο το εύρος των διαθέσιμων μετρήσεων, ως προς το μήκος καναλιού, την συχνότητα και το σημείο πόλωσης.

Εντέλει, παρουσιάζονται εφαρμογές όλων των παραπάνω δεικτών απόδοσης σε ολοκληρωμένα κυκλώματα ενισχυτών χαμηλού θορύβου. Η βέλτιστη απόδοση ενός cascode LNA στα 5 GHz επιτυγχάνεται κάνοντας χρήση του εξαχθέντος EKV3 μοντέλου, χρησιμοποιώντας τις κατευθυντήριες γραμμές που προτείνονται στα πλαίσια της διατριβής. Ο ενισχυτής πολώνεται στην περιοχή της μέτριας αναστροφής, επιτυγχάνοντας πολύ υψηλή απόδοση, λαμβάνοντας υπόψη όλους τους επιμέρους δείκτες απόδοσης, όπως κέρδος, θόρυβος, κατανάλωση, κτλ. Επιπλέον, ένας ενισχυτής χαμηλού θορύβου, μονού σταδίου, στα 90 nm, για λειτουργία στα 30 GHz, έχει υλοποιηθεί και μετρηθεί, επιτυγχάνοντας υψηλή απόδοση σε σύγκριση με αρχιτεκτονικές πολλαπλών σταδίων.

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Chapter 1

Introduction

The design of analog and RF integrated circuits is a complex procedure in which many steps have to be carefully taken into account for a successful and efficient implementation. At first, the individual radio frequency integrated circuits (RFIC) are components of entire transceivers. Hence, they have to comply with certain specifications. These result from the system level analysis of the transceiver and are determined by the application the transceiver has to serve. After extracting the specifications, the appropriate circuit topology has to be chosen to achieve the desired functionality. The most important step is to afterwards properly bias and size the investigated circuit. These design quantities are directly interdependent, imposing trade-offs in analog/RF design, according to the RF design hexagon, shown in Figure 1.1. This actually means that the individual figures of merit, such as gain, noise, linearity, power consumption are interdependent. Hence, methodologies for achieving the optimum performance have to be derived, rather than relying on the commonly used trial and error method. The latter has serious limitations regarding the time that is required for the circuit to converge to the expected functionality. Hand calculations can also be made prior to circuit simulations. For both hand calculations and simulations, a compact model describing the transistor operation is of utmost importance. The model should be characterized by simplicity, accuracy, and scalability over a large range of geometries, bias points and frequencies. In practice, a compact model acts as a bridge between the device and circuit.

With the aggressive technology scaling, the need for circuits operating under low voltage/low power becomes more and more imperative. In some of recent designs the operating point of MOSTs is moving from strong inversion (S.I.) to lower inversion levels, within moderate inversion (M.I.) or even the subthreshold region, also known as weak inversion (W.I.) - though, this is mostly the case for analog rather than RF. In weak inversion, specific problems occur in terms of leakage current which dramatically increases as channel length decreases. This may have catastrophic consequences for circuit design, since the gate current becomes comparable to the channel

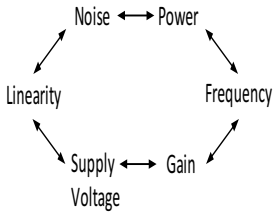

Figure 1.1: RF design hexagon.

current. This is why older technology nodes are often still preferable for analog design. Even in the case of integrated system on a chip (SoC), where the analog and digital parts should co-exist, the dictation of using modern CMOS technologies imposed by the digital domain, has resulted in employing design techniques with which the emerging disadvantages can be suppressed [2] . On the other hand, for RFIC design, operation under such small current level should generally be avoided since this dramatically decreases the device and thus the circuit RF and noise performance, through the decrease in the device transit frequency. Recently, RFICs with exceptional performance operating within the M.I. region have been reported [3]. Moving towards M.I. offers several advantages some of which are presented below [4]:

- Increase of the transconductance efficiency which in turn results in minimization of power consumption.
- Lower electrical fields within the device due to the decrease in bias voltages. This way velocity saturation (VS) and the corresponding hot electron effects phenomena can be avoided. Thus, the scaling trend of transit frequency (f_T) becomes such that f_T increases with the inverse of the square of channel length ($f_T \sim 1/L^2$) rather than the inverse of channel length, which is the case when VS is present [5]. This has a direct implication in circuit design since MOSTs can be used as amplifiers in much higher frequencies.
- The combination of current efficiency with transit frequency and intrinsic gain of the device, results in figures of merit describing the overall performance of the MOST device. We prove that the peak values of these FoMs are moving towards inversion levels close to the center of M.I. with technology scaling.
- Reduced electron heating results in lower excess noise factor, meaning that the overall device noise levels, usually expressed via minimum noise figure, NF_{min}, will be decreased.
- With technology scaling optimum performance regarding non-linearity metrics is shown to appear in the vicinity of the transition region from M.I. to S.I.

Therefore, M.I. represents the ideal trade-off between power consumption, noise and linearity, especially as technology scaling is driven towards the deca-nanometer regime.

The objective of this thesis is to prove that moving towards ultra-deep-submicron (UDSM) technologies, while their bias point is shifted to lower inversion levels, ultra-low power RFICs achieving high overall performance can be realized. Therefore, we start from a top-down approach with the system level analysis of a receiver block for the WiMAX wireless protocol. Following the requirements set by the protocol, the individual specifications of the component blocks are derived. Then, we focus on the first stage of the receiver front end, namely the low-noise amplifier. We then focus on the design of a cascode topology, based on a methodology which is using the inversion coefficient, IC, as the critical design parameter. IC stands as a convenient and direct way to compute the channel inversion level, independently of device type, geometry, and technology node. This methodology simplifies things from the circuit designer's perspective. The LNA circuit is the first in the receiver chain and thus should provide a low noise figure along with a high power gain and a low power consumption, so that the attenuated incoming signal can be efficiently received and amplified. Therefore it is imperative to investigate each of these individual FoMs as well as combinations among them in order to study their trend with channel length and bias. A single-stage LNA operating at 30 GHz has also been implemented as a part of an RF chip containing several structures, using 90 nm CMOS process from TSMC. The chip also includes DC, CV, and RF structures, from which we will mainly focus on the latter. Dummy structures of a known response have also been fabricated on-wafer to allow for the de-embedding of RF and noise measurements from parasitics.

We then measure the investigated structures for a wide range of frequencies, bias points and channel lengths and obtain their RF and noise characteristics. Noise parameters are extensively studied with and without accounting for short-channel effects, so that their impact on the noise behavior becomes clear. We show that optimum noise performance is achieved close to the M.I. region for the minimum channel length available MOSTs. Additionally, small- as well as large-signal analysis is performed in the investigated structures and the extracted RF FoMs are also studied with respect to scaling and inversion level. It proves that both domains, expressed by specific design metrics achieve their optimum performance in lower IC values, close to or within the M.I. region. This is of great significance since these FoM describe the overall performance of LNAs.

The thesis is organized as follows:

Chapter 2 is dedicated to the presentation of the specifications of the receiver front end and the corresponding LNA design, using the inversion coefficient as a design guide. Existing design techniques widely used by industry and academia are presented as well. A comparison between the fabricated single-stage 30 GHz LNA and multi-stage architectures is made to show the advantages and disadvantages

incurred by the choice of each architecture [6, 7].

Chapter 3 concentrates on the implementation and measurement of the RF chip. The design techniques that were used in laying out the devices are addressed. The RF as well as dummy structures are also described. The latter are used for the de-embedding of the actual device-under-test (DUT) from the pads and interconnection lines. The S-parameters and noise de-embedding methodologies are presented in detail and their influence on the high frequency and noise behavior of the MOS devices is shown.

Chapter 4 addresses the small- and large-signal analysis of the investigated 90 nm process. Additionally, TCAD simulations have been performed to derive the trend for RF FoMs for technology nodes ranging from 180 to 90, 45 and 22 nm. These FoMs include conventional as well as more advanced performance metrics. The product of transconductance to current ratio and transit frequency f_T, standing as an overall FoM for LNA design is studied for all technology nodes. Interestingly, its peak value is achieved close to the center of M.I. experiencing the same trend as NF_{min}: That is, the optimum values are gradually moving towards lower inversion levels. Moreover non-linearities are studied over the channel inversion domain for the 90 nm process as well as the TCAD data, through metrics such as the 1 dB compression point and 3rd order intermodulation intercept points [8–10].

Chapter 5 gives a detailed description of thermal noise in MOS devices providing the theoretical background of noise sources in MOSTs as well as the existing models. The EKV3 compact model is thoroughly presented in terms of its noise part and improvements that have been made are discussed. Measured noise parameters are then presented along with the model and power spectral densities are extracted. Modeling approaches for the excess noise factor, which is essential for RF circuit design, are validated with measurements for the first time and the impact of short-channel effects on it are shown. All noise parameters are presented versus channel length and inversion coefficient, experiencing a shift in the minimum value of noise figure, in the transition region between S.I. and M.I [8, 11].

Finally, chapter 6 gives the conclusion and the future work.

The present Thesis aims at providing a general framework for efficiently exploiting the advantages emerging by the downscaling of CMOS devices in low power RFIC design. We show that the analog and particularly the RF domain can benefit from the integration of analog and digital parts and the corresponding adaption of state of the art technologies from the former. Through a qualitative study of noise and small-signal analysis we prove the significance of noise as well as RF FoMs on LNA design and validate the excess noise factor with on-wafer measurements. The M.I. region has undoubtedly a high potential for designing RFICs with an overall exceptional performance and this is confirmed by the design of an LNA operating within this region. These contributions have resulted in several publications, listed below:

1. **A. Antonopoulos**, M. Bucher, K. Papathanasiou, N. Mavredakis, N. Makris, R. K. Sharma, P. Sakalas, M. Schroter, "CMOS Small-Signal and Thermal Noise Modeling at High Frequencies", *IEEE Trans. Electron Devices*, Vol. 60, No. 11, November 2013.

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4. **A. Antonopoulos**, M. Bucher, K. Papathanasiou, N. Makris, R. K. Sharma, P. Sakalas, M. Schroter, "CMOS RF Noise, Scaling, and Compact Modeling for RFIC Design", *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 53-56, Seattle, June 2013.

5. R.K Sharma, **A. Antonopoulos**, N. Mavredakis, M. Bucher, "Impact of Design Engineering on RF Linearity and Noise Performance of Nanoscale DG SOI MOSFETs", *14th International Conference on Ultime Integration on Silicon (ULIS),* pp. 145-148, Coventry, 2013.

6. **A. Antonopoulos**, K. Papathanasiou, M. Bucher, K. Papathanasiou, "CMOS LNA Design at 30 GHz – A Case Study", *8th International Caribbean Conference on Devices Circuits and Systems (ICCDCS)*, pp. 1-4, Playa Del Carmen, 2012.

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Chapter 2

Low Noise Amplifier Design

This chapter aims to introduce the reader in the design of low noise amplifiers (LNA). We start by presenting existing receiver topologies and describe the noise and nonlinearity of cascaded stages. Thus, the impact of noise, gain and nonlinearity of the LNA circuit in the overall receiver performance is studied. Then critical parameters for LNA design are introduced. Existing LNA topologies, such as common gate, common source, and cascode, are discussed and compared. Increasing the operation frequency close to mm-wave becomes a challenge and hence an overview on recent LNA design close to 30 GHz is given. Based on that, we show the implementation of a 30 GHz LNA presenting its simulated as well as measured results. The advantages of biasing an RF circuit within the moderate inversion region are exemplified by the design of a cascode LNA operating at 5 GHz. The specifications of the circuit are derived from the system level analysis of a direct conversion receiver for WiMAX applications.

2.1 Receiver Architectures

A typical receiver consists of an antenna, a band-pass filter, an LNA, one or more down-conversion stages with or without filtering and an analog-to-digital (ADC) converter with or without variable gain amplification. The number of the down-converting stages is determined by the receiver architecture. Heterodyne receivers down-convert the incoming signal at a nonzero intermediate frequency (IF), but suffer from the problem of image [12], demanding an extra image-reject filter for suppressing the image problem. On the other hand, direct conversion (or zero-IF) receivers [13, 14] use only one down-conversion stage and have become popular over the last decade. Compared to the heterodyne receivers, direct-conversion receivers are simpler due to the absence of an image. Moreover, channel selection is performed by low pass filters which can be realized on-chip as active circuit topologies. The

schematic diagram of a typical zero-IF receiver, included in a transceiver, is shown in Figure 2.1.

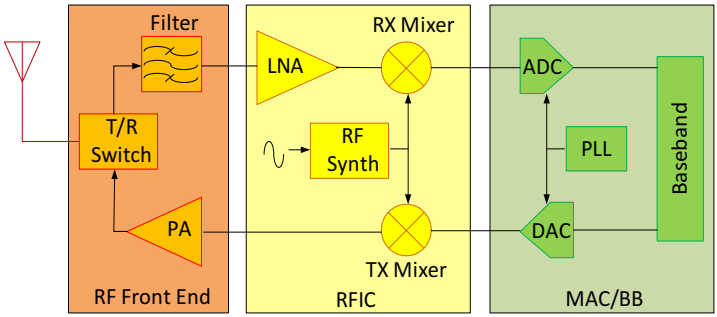


Figure 2.1: Typical Transceiver.

2.1.1 Noise of Cascaded Stages

According to "Friis equation", the total noise figure in a cascade of stages, e.g. the receiver of Figure 2.1, is given by:

$$NF = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{P1}} + \frac{NF_m - 1}{A_{P1} \ldots A_{P(m-1)}} \tag{2.1}$$

NF_m and A_{Pm} are the noise figure and power gain of stage m. Equation (2.1) suggests that the noise contributed by each stage decreases as the gain of the preceding stages increases. Thus, the first stage plays the most critical role in a receiver chain. Conversely, if a stage provides attenuation rather than amplification, then the NF of the following stages is amplified by the attenuation quantity.

2.1.2 Nonlinearity of Cascaded Stages

In a cascade of nonlinear stages, the overall nonlinearity, expressed by the amplitude of the third order input intercept point A_{IIP3} is given by (2.2). If each stage has a gain greater than unity, the nonlinearity of the latter stages has the greatest contribution on the overall nonlinearity. The IIP3 of each stage is scaled down by the total gain preceding the stage. α_1 and β_1 is the small-signal gain of the first and second stage, respectively, e.g. the LNA and mixer in Figure 2.1.

$$\frac{1}{A^2_{IIP3}} = \frac{1}{A^2_{IIP3,1}} + \frac{\alpha_1^2}{A^2_{IIP3,2}} + \frac{\alpha_1^2 \beta_1^2}{A^2_{IIP3,2} A^2_{IIP3,3}} + \ldots \tag{2.2}$$

2.2 LNA Requirements

From the equations above, we conclude that an LNA should provide the minimum possible noise figure, since it has the greatest contribution in the overall receiver noise. On the other hand, its nonlinearity may be kept at a moderate level, depending on the application. When low noise and high linearity are strong requirements for a receiver, the LNA gain, should be adjusted so that it decreases noise contribution of the latter stages while it does not significantly deteriorate the nonlinearity imposed by the same stages. Except for the noise, gain and linearity, equally important design characteristics for LNA design, such as matching and stability, are described below.

2.2.1 Matching

There are three different types of matching in an LNA, namely impedance matching, power matching and noise matching. The latter occurs when the source admittance is equal to the optimum admittance and will be analytically presented in Chapter 5. Power matching maximizes power transfer to a load. Consider the case of a voltage source with a source impedance Z_S driving a load impedance Z_L. From basic circuit theory, the value of Z_L that maximizes the power dissipation in the load is achieved when $Z_L = Z_S^*$ [15]. The input signal source of the LNA is usually a band-select filter or an antenna. A band-select filter is typically designed and characterized with a standard termination of 50 Ω. If the load impedance seen by the filter deviates from 50 Ω, then the filter may exhibit performance degradations such as loss and ripple [16]. In the absence of a filter the antenna directly provides the incoming signal to the LNA. The antenna is also designed for a certain real load impedance, typically equal to 50 Ω. When the LNA input impedance is also equal to 50 Ω, the situation is called impedance matching. Note that in this case power matching is identical to impedance matching. Poor matching at the receiver input causes reflections, loss and possibly voltage attenuation. The quality of the input match is expressed by the input return loss. It is defined as the ratio of the reflected voltage to the incident voltage and is expressed by (2.3). Z_{in} denotes the input impedance and R_S is the source impedance. Ideally, for $Z_{in} = R_S \Rightarrow \Gamma = 0$, and no reflection occurs. Similarly to input impedance matching, output impedance matching should also be achieved when the LNA is considered as a standalone circuit. Usually, to facilitate measurements, output impedance is also set to 50 Ω. Otherwise, the output impedance of the LNA, should match that of the mixer, which in the case of Gilbert-cell-type implementations, is always capacitive.

$$\Gamma = \left|\frac{Z_{in} - R_S}{Z_{in} + R_S}\right| \tag{2.3}$$

2.2.2 Stability and Reverse Isolation

LNAs may become unstable due to ground and supply parasitic inductances from the packaging. Feedback paths from the output to the input may also lead to instability issues for certain combinations of input and output impedances. The "Stern stability factor", K, is often used to describe the stability of amplifier circuits. It is defined in (2.4). Δ is the determinant of the S-parameters matrix and equals: $\Delta = S_{11}S_{22} - S_{12}S_{21}$.

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \tag{2.4}$$

When $K > 1$ and $\Delta < 1$ the circuit is unconditionally stable. K should remain greater than one at all frequencies, not only the LNA operation frequency. Equation (2.4) implies that as couping (S_{12}) decreases or reverse isolation (-S_{12}) increases, stability improves. Reverse isolation is also important for the forward gain of the LNA. Often a low inverse isolation reduces the signal efficiency and thus the LNA gain. Moreover a high reverse isolation reduces the spurious local oscillator tone at the antenna, which reaches the antenna through the mixer and the reverse gain of the LNA.

2.2.3 Power Gain

Since the mixer is usually driven by a voltage, it is the voltage gain that should be optimized in an LNA. However, in the case of a 50 Ω input and output impedance matched LNA, voltage and power gain are the same. Several types of power gain can be found in literature and are commonly used in LNA design. Transducer power gain, G_T, is the ratio of the the power delivered to the load to the power available from the source. Operating power gain, G_P, is the ratio of the power delivered to the load to the power absorbed at the input. Available power gain, G_{av}, is the ratio of the available output power to the available power of the source. The simplified expressions for all power gain expressions in terms of S-parameters can be found in (2.5), (2.6), and (2.7). This is the way Spectre© simulator calculates the power gain quantities. In most cases the LNA power gain is represented by the transducer power gain, and is equal to S_{21}^2. Increasing the power/voltage gain in an LNA suppresses the noise contribution of succeeding stages. However, maximizing the gain of the LNA regardless of other building blocks is not advisable. This would increase the signal levels in the mixer and could potentially create linearity problems. Therefore, a careful choice of the LNA gain should be made, depending on the application and the respective specifications.

$$G_T = |S_{21}|^2 \tag{2.5}$$

$$G_P = \frac{1}{1 - |S_{11}|^2}|S_{21}|^2 \tag{2.6}$$

$$G_{av} = |S_{21}|^2 \frac{1}{1-|S_{22}|^2} \tag{2.7}$$

2.2.4 Noise

LNAs are being used to receive and amplify weak signals. The attenuated signal received at their input non only consists of the signal sent from the transmitter but also of the noise signal generated from the antenna. To obtain a sufficiently high level of signal power with a reasonable signal to noise ratio (SNR) the noise produced by the amplifier should be kept as low as possible. The noise performance of an amplifier is expressed by its noise factor, which is the SNR at its input divided by the SNR at its output, $F = SNR_{in}/SNR_{out}$. The noise figure is the noise factor expressed in decibels: $NF = 10 \times logF$. Ideally, the noise factor of a noiseless LNA equals unity. Low noise is also desirable, since the noise contribution of the LNA has the greatest impact on the total receiver noise (Section 1.1.1). The low noise required for LNAs limits the choice of circuit topology. This means that in cases of very strict noise specifications, some of the existing LNA topologies become inappropriate and limitations on the number of amplifying stages arise.

2.2.5 Power Dissipation

The need for circuits consuming less power becomes more intense with technology scaling. However, as the supply voltage is reduced, the available voltage headroom may become too small to design circuits with sufficient signal integrity at reasonable power consumption. The LNA consumes only a small fraction of the overall receiver power. However, when power is of primary interest, e.g. in portable devices, power dissipation should be minimized. For LNA design, power dissipation has to be considered along with other figures of merit (FoMs), such as noise, linearity, and gain, and trade-offs among them should be handled efficiently by circuit designers.

2.3 LNA Topologies

There are several circuit topologies that fulfill the principal targets in LNA design. In this section, basic principles of amplifier topologies, such as classical common gate, common source, and cascode stages will be presented, and their advantages, problems and adjustments to fulfill specifications will be discussed.

2.3.1 Common-Gate LNA

The common-gate (CG) topology is attractive for LNA design, due to its low input impedance. If channel length modulation and body effect are neglected, the input

impedance is equal to $1/g_m$, where g_m is the gate transconductance of M1. g_m can be chosen so that $1/g_m$=50 Ω. Due to the resistive nature of input impedance, CG LNAs can be used for broadband matching. Here, a CG stage with inductive load is presented (Figure 2.2), with R_1 representing the inductor loss. The voltage gain can be easily calculated from the equivalent small-signal circuit. The voltage gain at the resonant frequency equals:

$$\frac{V_{out}}{V_X} = g_m R_1 = \frac{R_1}{R_S} \tag{2.8}$$

Therefore,

$$A_v \equiv \frac{V_{out}}{V_{in}} = \frac{R_1}{2R_S} \tag{2.9}$$

Thermal noise of M1 can be modeled by a voltage source in series with the gate, with a power spectral density equal to: $\overline{V_{n1}^2} = 4kT\gamma/g_m$. γ is a bias dependent parameter called thermal noise excess factor and will be extensively presented in Chapter 5. The noise at the output due to M1 can be found by multiplying $\overline{V_{n1}^2}$ by the square of gain.

$$\overline{V_{n1}^2} = \frac{4kT\gamma}{g_m}\left(\frac{R_1}{R_S + \frac{1}{g_m}}\right)^2 = kT\gamma\frac{R_1^2}{R_S} \tag{2.10}$$

The output noise due to R_1 is $\overline{V_{nR1}^2} = 4kTR_1$.The noise of the source is $4kTR_S$. The noise factor, which is equal to the ratio of the total output noise to the output noise due to the source, is derived by dividing the output noise due to M1 and R_1 by the gain times $4kTR_S$ and adding unity to the result. It is found to be:

$$F \equiv \frac{total\ output\ noise}{output\ noise\ due\ to\ the\ source} = 1 + \gamma + 4\frac{R_S}{R_1} \tag{2.11}$$

Even if $4\frac{R_S}{R_1} \ll 1 + \gamma$, for a value of γ equal to unity a noise figure of 3 dB is obtained. However, this is a very optimistic scenario, since γ values much greater than one were recently reported [8]. Similar results have also been shown in [16, 17], regarding the noise figure of a CG LNA topology with resistive load. Specifically, noise factor equals: $F = 1 + \frac{\gamma}{\alpha}$, where $\alpha = \frac{g_m}{g_{dso}}$. g_{dso} is the output conductance under zero drain-source voltage. For long channel devices, α equals unity and thus a noise figure of about 2.2 dB can be achieved, assuming γ=1. With channel length scaling, α decreases and γ increases. Hence, the high levels of noise figure renders CG topology inappropriate for realizing LNAs with very low noise levels [18]. A lower noise figure can be achieved if g_m is increased. However, this would also give a lower input resistance. For wide-band applications, e.g. UWB applications, the CG structure is widely used [19, 20]. To suppress the generated noise, noise-canceling stages may be used between the LNA and mixer [19].

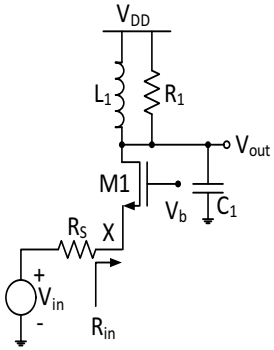


Figure 2.2: CG stage.

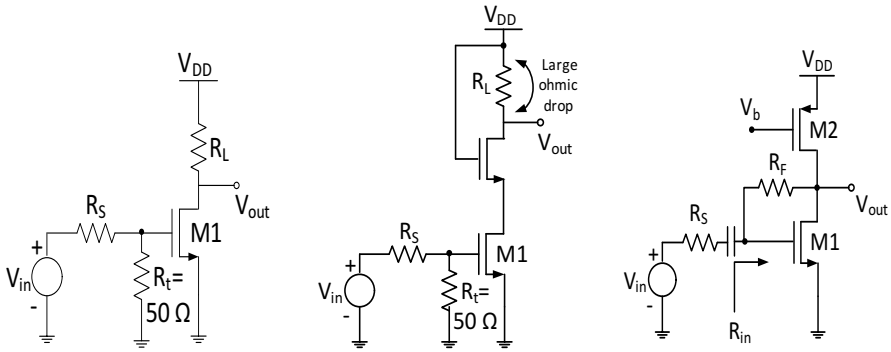
Several techniques for improving the gain and noise figure of CG LNAs have been proposed, based on current bleeding [21] and noise cancellation [18]. An inverting amplification (with gain A) can also be introduced between the source and gate nodes of the MOSFET. This way the effective transconductance looking into the source terminal is boosted by an amount of (1+A) while the noise factor is reduced by the same quantity [16].

2.3.2 Common-Source LNA

A simple baseband one-transistor common-source topology with a resistive load, is shown in Figure 2.3a. The problem is that the circuit has a purely capacitive input impedance, and thus input matching cannot be achieved. To create a real 50 Ω component, it suffices to place a termination resistor in parallel to the LNA input. The input impedance is given by (2.12), where ω_p is equal to: $\omega_p = \frac{1}{R_S(C_{gs}+MC_{gd})}$. M, is the Miller factor ($M = 1 + g_{m1}R_L$). This topology strongly limits the frequency response and gives rise to a very poor reverse isolation.

$$Z_{in} = \frac{R_S}{1 + \frac{j\omega}{\omega_p}} \tag{2.12}$$

To neutralize the problem of poor reverse isolation, which results from the capacitive feedback from the output to the input, through C_{gd}, a parallel resonance can by used. However, since C_{gd} is relatively small, a large inductance would be required, thereby introducing significant parasitic capacitances. Alternatively, a cascode transistor, reducing the Miller effect, can be added (Figure 2.3b). The problem still existing is that for a high gain, R_L needs to be high. However, this will cause a large DC voltage drop over R_L. The voltages of M1 and M2 should be large enough to ensure operation in saturation, that is, the drain-source voltage should be at least: $V_{DS,sat} = V_{GS} - V_T$. Therefore, R_L is limited to: $R_L < \frac{V_{DD} - V_{DS,sat1} - V_{DS,sat2}}{I_D}$ [15]. Supposing a realistic



(a) CS stage (b) Cascode stage (c) CS with resistive feedback

Figure 2.3: (a) CS stage, (b) cascode stage with resistive load, and (c) cascode stage with resistive feedback.

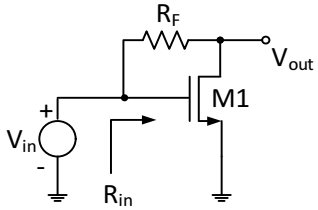
scenario of $V_{DS,sat}$=0.25 V and V_{DD}=1.2 V, and operation in strong inversion, the voltage gain of the topology is limited to 15 dB. This is analyzed below:

$$A_v = g_{m1}R_L = \frac{2I_D}{V_{DS,sat1}} \cdot \frac{V_{DD} - V_{DS,sat1} - V_{DS,sat2}}{I_D} = \\ = 2 \cdot \frac{V_{DD} - V_{DS,sat1} - V_{DS,sat2}}{V_{DS,sat1}} = 5.6 \tag{2.13}$$

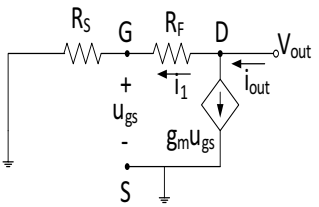
The voltage drop across R_L can be reduced by replacing the resistive load with an inductor load [22, 23]. The equivalent load resistance becomes: $R_L = R_{L,S}(Q_L^2 + 1)$, where $R_{L,s}$ is the series resistance modeling the inductor loss and Q_L is the quality factor of the inductor, equal to: $Q_L = \frac{\omega_0 L_D}{R_{L,s}}$. ω_0 is the frequency of operation and L_D is the inductance which is chosen so that it resonates with the output capacitance at ω_0. The problem with this topology is that it suffers from poor input matching, since a capacitive component, due to C_{gs}, is still present at the input impedance. Moreover, the resistive termination at the gate increases noise.

2.3.3 Common-Source LNA with Resistive Feedback

For frequencies well below the transit frequency the feedback CS stage, depicted in Figure 2.3c, can be used [24, 25]. The feedback transistor R_F senses the output voltage and returns a current to the input. To resolve the problem of gain limitation due to the resistive load, previously discussed, M2 is used instead of a resistor. From



(a) Simplified circuit of CS resistive feedback



(b) Small-signal equivalent circuit for R_{out} calculation

Figure 2.4: (a) Simplified circuit for calculation of R_{in} and (b) equivalent circuit for calculation of R_{out}.

the simplified circuit of Figure 2.4a, and since only one current flows into the circuit, the input resistance is equal to $1/g_m$.

$$R_{in} \equiv \frac{U_{in}}{i_{in}} = \frac{U_{in}}{g_m u_{gs}} = \frac{U_{in}}{g_m U_{in}} = \frac{1}{g_m} \tag{2.14}$$

The voltage gain can be derived by a simple KVL from input to output through R_F:

$$V_{in} - g_m u_{gs} R_F = U_{out} \Rightarrow A_V \equiv \frac{U_{out}}{U_{in}} = 1 - \frac{R_F}{R_S} \tag{2.15}$$

The output resistance, R_{out} of the topology can be found by setting the input voltage source to zero (Figure 2.4b).

$$i_{out} = i_1 + g_m u_{gs} \tag{2.16}$$

$$U_{out} - i_1(R_F + R_S) = 0 \Rightarrow i_1 = \frac{U_{out}}{R_F + R_S} \tag{2.17}$$

$$0 + i_1 R_S - u_{gs} = 0 \Rightarrow u_{gs} = U_{out} \frac{R_S}{R_F + R_S} \tag{2.18}$$

From (2.17), (2.18), the output resistance is given by:

$$R_{out} \equiv \frac{U_{out}}{i_{out}} = \frac{R_F + R_S}{2} \tag{2.19}$$

The output noise current due to both M1 and M2 is equal to:

$$\overline{I^2_{n|M1,M2}} = \overline{I^2_{n,M1}} + \overline{I^2_{n,M2}} = 4kT\gamma(g_{m1} + g_{m2}) \tag{2.20}$$

The noise due to M1, M2 expressed in terms of its Thevenin equivalent, is the product of $\overline{I^2_{n|M1,M2}}$ with R^2_{out}.

$$\overline{V^2_{n,out|M1,M2}} = \overline{I^2_{n|M1,M2}} R^2_{out} = 4kT\gamma(g_{m1}+g_{m2})\frac{(R_F+R_S)^2}{4} \tag{2.21}$$

The noise due to R_F is equal to $4kTR_F$. The overall noise factor due to all noisy components is calculated through (2.22). Even for small values of γ, NF exceeds 3 dB, which is a prohibitive value when extremely noise level is required. Moreover, the circuit also suffers from poor input impedance mismatch, since the capacitive component due to C_{gs} has not been canceled.

$$F = 1+4\frac{R_S}{R_F}+\gamma(g_{m1}+g_{m2})R_S \tag{2.22}$$

2.3.4 Common-Source LNA with Thermal Noise Cancellation

The noise contribution of the input transistor can be canceled by applying the thermal noise cancellation technique introduced in [26, 27]. The technique is based on the CS topology with resistive feedback. The key point with noise cancellation is to observe that the noise current at points X and Y have equal sign, whereas signal voltages at the same points have opposite sign [28]. This is because the gain of the stage is negative. Recall from (2.15) that for $g_m R_F = \frac{R_F}{R_S} > 1, A_v < 0$. This difference in sign for noise and signal makes it possible to cancel the noise of the matching device, while simultaneously adding the signal contributions constructively [26]. This is done by creating a scaled negative replica of the voltage at node X which is added to the voltage at node Y, creating a new output (Figure 2.5). The scaled negative replica is implemented using an ideal feedforward voltage amplifier with a gain $-A_V$. The device noise voltages at node X and Y are given by (2.23) and (2.24), respectively, where $0 < \alpha < 1$.

$$V_{X,n} = \alpha(R_S g_m)\cdot I_n R_S \tag{2.23}$$

$$V_{Y,n} = \alpha(R_S g_m)\cdot I_n (R_S+R_F) \tag{2.24}$$

The output noise voltage due to the noise of the transistor is:

$$V_{out,n} = V_{Y,n} - V_{X,n}A_V \tag{2.25}$$

Output noise cancellation, $V_{out,n} = 0$ is obtained for:

$$A_{vc} = \frac{V_{Y,n}}{V_{X,n}} = 1+\frac{R_F}{R_S} \tag{2.26}$$

,where the index c, denotes cancellation. On the other hand, the signals along the two paths add constructively. The output, V_{out}, is equal to the sum of the signal at node X

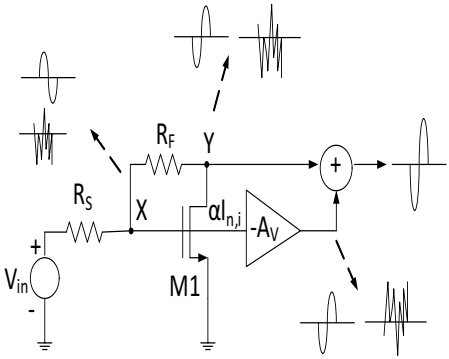


Figure 2.5: CS LNA exploiting noise cancelling.

multiplied by the signal gain from (2.15), plus V_X multiplied by A_{Vc}. Therefore the overall gain is given by (2.28)

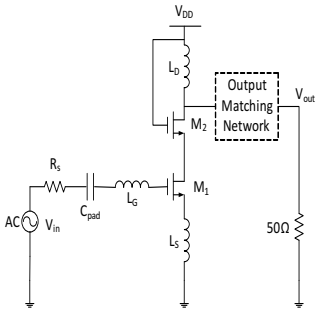
$$V_{out} = V_X(1 - \frac{R_F}{R_S}) - V_X A_{vc} \Rightarrow \tag{2.27}$$

$$\Rightarrow A_{VFc} = \frac{V_{out}}{V_X} = -2\frac{R_F}{R_S} \tag{2.28}$$

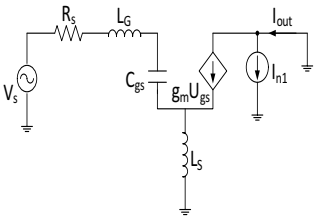
From (2.26), two characteristics of noise canceling are evident. Noise canceling depends on the absolute value of the real impedance of the source, R_S (e.g., the impedance seen "looking into" a properly terminated coax cable). The cancellation is independent on the quality of the source impedance match. This is because any change of g_m equally affects the noise voltages $V_{X,n}$ and $V_{Y,n}$ [26].

2.3.5 Cascode CS with Inductive Degeneration

To counteract the capacitive part of the input impedance, an inductor L_S is placed between the source of the input transistor and ground. A resistive part is also created, being equal to $\omega_T L_S$, where ω_T is the transit frequency, given by: $\omega_T = \frac{g_m}{C_{gs}}$. The input impedance can now be calculated through the equivalent small-signal circuit (Figure 2.6b) via (2.29). The real part of the input impedance can now be adjusted through L_S. However, an extra degree of freedom is needed in order to cancel the input capacitance. Adding L_G, between the gate of M1 and the input signal, serves this goal, since the input impedance becomes equal to (2.30). At the operating frequency, the imaginary part of the input impedance should equal zero, resulting in (2.31). Therefore, L_S is chosen so that $\Re(Z_{in}) = 50\,\Omega$ while L_G is used to satisfy that $\Im(Z_{in}) = 0$, at f_0. The input impedance is purely resistive only at ω_0, hence the method can provide a narrow-band impedance match. The circuit topology is called



(a) Inductively degenerated cascode stage



(b) Small-signal equivalent circuit forthe inductively degenerated cascode LNA

Figure 2.6: The inductively degenerated cascode LNA.

inductively degenerated cascode LNA (Figure 2.6), and can be found in numerous publications [29–42], due to its simplicity and high performance, compared to standard CG and CS topologies. The one and only current path makes the topology ideal for low-power applications, as will be shown in Chapter 4. For simplicity reasons, the pad capacitance, has not been taken into account in input impedance calculation. However in a tape-out design its value should be considered in determining Z_{in}.

$$Z_{in} = \frac{1}{sC_{gs}} + sL_S + \omega_T L_S \tag{2.29}$$

$$Z_{in} = \frac{1}{sC_{gs}} + s(L_S + L_G) + \omega_T L_S \tag{2.30}$$

$$\omega_0(L_G + L_S) = \frac{1}{\omega_0 C_{gs}} \tag{2.31}$$

Noise of the inductively degenerated cascode topology is slightly influenced by transistor M2, and thus its contribution on the total noise is disregarded in the analysis [43]. The equivalent small-signal circuit of the CS stage is shown in Figure 2.6b, with I_{n1} representing the thermal noise of M1. Induced-gate noise has not been considered in noise calculations. The output current I_{out} is equal to:

$$I_{out} = g_m U_{gs} + I_{n1} \tag{2.32}$$

The input current is given by: $i_{in} = sC_{gs}U_{gs}$. From KVL we get:

$$U_{in} = (R_S + sL_G)sC_{gs}U_{gs} - U_{gs} - sL_G(I_{out} + sC_{gs}U_{gs}) = 0 \tag{2.33}$$

From (2.32), $U_{gs} = \frac{I_{out} - I_{n1}}{g_m}$. Therefore, (2.33) becomes:

$$U_{in} = sL_S I_{out} + (I_{out} - I_{n1}) \frac{sR_S C_{gs} + s^2(L_G + L_S)C_{gs} + 1}{g_m} \tag{2.34}$$

At resonance (s=jω$_0$), (2.31) raises: $-\omega_0^2(L_G + L_S)C_{gs} + 1 = 0$. Thus,

$$U_{in} = I_{out}(j\omega_0 L_S + \frac{j\omega_0 R_S C_{gs}}{g_m}) - I_{n1}\frac{j\omega_0 R_S C_{gs}}{g_m} \tag{2.35}$$

If we neglect the noisy part of output current, the transconductance gain of the circuit $|\frac{I_{out}}{U_{in}}|$ can be easily derived:

$$|\frac{I_{out}}{U_{in}}| = \frac{1}{\omega_0(L_S + \frac{R_S C_{gs}}{g_m})} \tag{2.36}$$

Recall from (2.30) that at resonance $\frac{g_m}{C_{gs}}L_S = R_S \Rightarrow L_S = R_S\frac{C_{gs}}{g_m}$. Hence, for a matched input, the transconductance remains independent of inductances L_S and L_G.

$$|\frac{I_{out}}{U_{in}}| = \frac{\omega_T}{2\omega_0} \cdot \frac{1}{R_S} \tag{2.37}$$

In order to calculate the output noise due to M1, we set $U_{in} = 0$. Then, from (2.35), we get:

$$|I_{n,out}|_{M1} = |I_{n1}|\frac{R_S C_{gs}}{L_S g_m + R_S C_{gs}} \tag{2.38}$$

, which due to $\frac{g_m}{C_{gs}}L_S = R_S$ becomes:

$$|I_{n,out}|_{M1} = \frac{|I_{n1}|}{2} \tag{2.39}$$

and hence

$$\overline{I_{n,out}^2} = \frac{\overline{I_{n1}^2}}{4} = kT\gamma g_m \tag{2.40}$$

The noise of the input voltage source is equal to $4kTR_S$. To translate the output noise to its appropriate form $\overline{V_{n,out}^2}$, we need to divide $I_{n,out}^2$ by the square of the circuit's transconductance and by $4kTR_S$ and add unity. The result in (2.41), holds only at the input resonant frequency and if the input is matched. Interestingly, for a fixed operating frequency, the noise factor and thus the noise figure reduce with technology scaling, since the transit frequency increases. The impact of excess noise factor in F, is clear from (2.41) and thus accurate modeling is required, rather than assuming its long channel value, which is the case in many published work [17, 24].

$$F = 1 + \frac{\overline{V_{n,out}^2}}{4kTR_S} = 1 + \frac{\overline{I_{n,out}^2}}{(\frac{\omega_T}{2\omega_0}\cdot\frac{1}{R_S})^2} = 1 + g_m\gamma R_S(\frac{\omega_0}{\omega_T})^2 \tag{2.41}$$

The voltage gain of the cascode topology is equal to the product of the transconductance of the circuit and the load resistance R_L. Using (2.36), we end up with (2.42). The power gain, A_P is derived via (2.44). Power gain increases with ω_T. Hence, for a specific frequency of operation, moving towards deep-submicron technologies improves the gain of the LNA. The power gain can be rewritten according to (2.44), to introduce an important quantity for the cascode LNA, namely the effective quality factor of the amplifier input circuit, Q_{in} [17].

$$A_V \equiv \frac{V_{out}}{V_{in}} = \frac{\omega_T}{2\omega_0} \cdot \frac{R_L}{R_S} \tag{2.42}$$

$$A_P = \frac{V_{out}^2/R_L}{V_{in}^2/R_S} = (\frac{\omega_T}{\omega_)})^2 \frac{R_L}{4R_S} \tag{2.43}$$

$$A_P = Q_{in}^2 g_m^2 R_L R_S \tag{2.44}$$

, where

$$Q_{in} = \frac{U_{gs}}{U_{in}} = \frac{1}{2\omega_0 C_{gs} R_S} \tag{2.45}$$

In the foregoing analysis, the induced-gate noise has not been taken into account in noise calculations, for simplicity reasons. However, as the operating frequency increases, induced-gate noise becomes a remarkable part of the total noise of the input device. Such noise is enhanced by the quality factor of the input circuit. A high Q_{in} is beneficial for reducing channel current noise. However, in a design where the gate induced current noise is disregarded one might end up with a large Q_{in}, and a noise totally dominated by the gate induced current noise [43]. To resolve the problem, an additional capacitance is inserted in parallel to the intrinsic gate capacitance C_{gs} of M1. Therefore Q_{in} is decoupled from C_{gs}, allowing for an adjustable reduction of Q_{in} for any given C_{gs}. This is crucial since induced-gate noise increases with the square of C_{gs}. This method achieves noise reduction, without deteriorating power consumption.

In the previous analysis, power minimization was not considered as a constraint for efficient LNA design. If an LNA is designed for input impedance matching and noise matching, regardless of power dissipation, large devices demanding extremely high bias current (even in the order of hundreds of mA) are required [17]. To develop a power-constrained noise optimization technique, Shaeffer and Lee expressed noise figure in a way that takes power consumption into account. According to this technique, the optimum device width, $W_{opt,P}$ for power constrained noise optimization, is approximately equal to:

$$W_{opt,P} \simeq \frac{1}{3\omega L C_{ox} R_S} \tag{2.46}$$

With a device of width W_{opt} the noise figure obtained within the power constraint is given by (2.47). For a fixed frequency, the value of $F_{min,P}$ is about 0.5 - 1 dB higher compared to the value obtained for the minimum achievable noise [24].Therefore the noise penalty for power optimization can be tolerated.

$$F_{min,P} \simeq 1 + 2.4\frac{\gamma}{\alpha}(\frac{\omega}{\omega_T}) \tag{2.47}$$

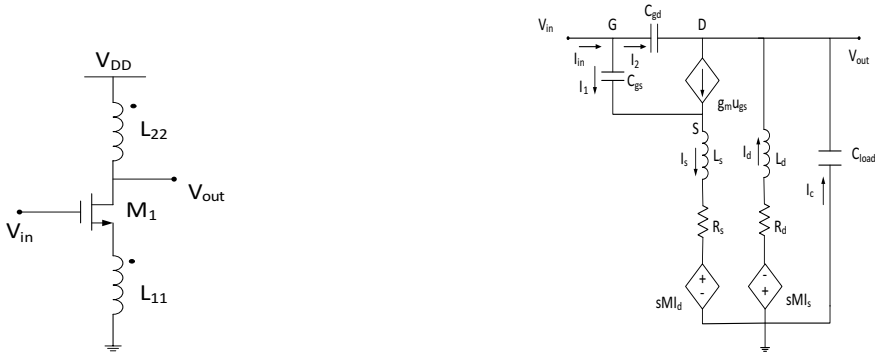
Power constrained simultaneous noise and input impedance matching was first introduced by Andreani [43] with the addition of an extra capacitance in parallel with C_{gs}. The technique has also been used in [44–46]. An interstage inductor between the CS and CG stage, increasing gain, decreasing noise and providing good isolation has been proposed and implemented in [47–50].

2.3.6 Transformer-Feedback LNA

The gate-drain overlap capacitance C_{gd} reduces MOST and thus amplifiers' performance through several ways. As already discussed, C_{gd} adds a signal path which reduces LNA's reverse isolation. It also reduces the device f_T, which in turn deteriorates noise and gain. To mitigate the effect of C_{gd} circuit techniques are separated into two categories: unilateralization and neutralization [51]. Cascoding of a CS and CG stage is a common circuit technique for unilateralization. Neutralization cancels signal flow through C_{gd} by adding additional signal paths from the output to the input so that the signal flow through C_{gd} and the additional signal path is zero [51].

The most commonly used circuit employing neutralization is the magnetic feedback LNA [51–53], depicted in Figure 2.7. The topology is ideal for low-voltage supply operation. Magnetic-feedback LNA is a quite simple structure which consists of an active device and a transformer [54]. Primary and secondary coils at drain and source terminals, are coupled with a coupling coefficient, k. Figure 2.7b represents the small-signal equivalent circuit, which also includes the series resistance of each inductor. The operation of magnetic feedback is based on cancellation of the existing path between drain and gate - due to C_{gd} - by introducing a negative feedback with the addition of an alternative signal pathway. More specifically, when a small signal, V_{in}, is applied at the transistor's gate, the drain current I_D increases. This in turn results in an increase of the current controlled voltage source (sMI_D). Since the source potential increases, the gate-source voltage (V_{GS}) decreases, which constitutes a negative feedback. According to [51], the reverse signal flow through the transformer cancels the reverse signal flow through C_{gd} when:

$$\frac{n}{k} = \frac{C_{gs}}{C_{gd}} \tag{2.48}$$



(a) Magnetic-feedback LNA

(b) Small-signal equivalent circuit for the magnetic-feedback LNA

Figure 2.7: The magnetic-feedback LNA.

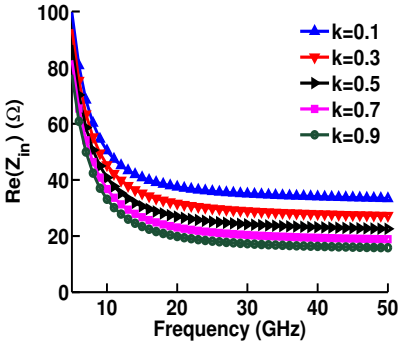


Figure 2.8: Real part of input impedance versus frequency for a magnetic-feedback LNA.

, where n is the transformer's turn ratio, equal to $n = \sqrt{L_{22}/L_{11}}$ and k is given by $k = M/\sqrt{L_{11}L_{22}}$, with M being the mutual inductance. In TSMC's 90 nm CMOS process the ratio of the gate-source capacitance to the gate-drain capacitance equals about 0.3, so for a given k the inductance of each coil can be computed. Attention should be paid to the secondary coil, which is also used as source degeneration to match the input impedance to 50 Ω. This simplifies the calculation of the primary coil's inductance. Choosing the proper value for k is a procedure which stems from small signal circuit theoretical calculation of input impedance, output impedance and voltage gain. The equations that result are complex, and not presented here. For the detailed expressions the reader can be directed to [51, 52]. To give some insight, Figure 2.8 demonstrates how k affects the input impedance, for specific values

of L_{11} and L_{22}. The same happens for output impedance and voltage gain, thus a compromise among all FoMs should be made.

2.3.7 Ultra Low-Voltage/Power LNAs

With technology downscaling, low-voltage operation becomes imperative for RFICs. LNAs with two cascaded stages, each of which is supplied by its individual voltage have been shown in [55, 56]. However the reduction of the supply voltage is obtained at the price of current increase. Folded-cascode LNAs operating under extremely low-voltage, even at 0.5 V, have been reported in [57–59]. Despite the usual design techniques dictating biasing the LNA in strong inversion, operation in lower inversion levels has revealed the capabilities of realizing high-performance RFICs with extremely low power dissipation. This is proven in [3, 21, 41, 45, 60–63] where conventional LNA topologies, such as inductively degenerated CS and cascode LNAs consuming much less than 1mW, while operating in low inversion levels are shown. Alternative design techniques for input impedance matching employ usage of parallel LC network, or series L and parallel L, as well as the parasitic gate resistance to tune the input impedance at 50 Ω [64, 65].

2.4 mm-wave LNA Design - An Overview

Since the basic requirements (NF, gain, linearity, stability, power dissipation) are the same regardless the operating frequency, the design methodologies at mm-wave frequencies (above 30 GHz) do not change. However, the circuit topologies are different to account for the three fundamental differences at mm-wave, compared to lower frequency design. These are:

1. Designing using transistors close to their cut-off frequency, f_{T}.
2. Operating with signals at small wavelengths resulting in distributed effects.
3. Designing with parasitic elements, which result in high impedances, on a given node.

Transistors operating close to their cut-off frequency have smaller gain and higher NF. A useful formula to compute the available gain at an operating frequency is through (2.49) [66]. As an example, a transistor with a unity power gain frequency of 240 GHz has 18 dB of power gain at 30 GHz.

$$G_{MAG} = 20log\frac{f_{max}}{f_0} \tag{2.49}$$

When signals traverse components which are an appreciable size of wavelength, they result in a noticeable phase delay across the component. Therefore, distributed effects should be considered as part of the design process. Another implication is

that any interconnect within the circuit which is an appreciable size of wavelength should be treated as a transmission line and accurately modeled through EM simulation. The undesired parasitic components at a circuit node are shunt capacitance and serial inductance creating admittance and impedance proportional to frequency, respectively.

A fundamental objective of the LNA is to achieve a simultaneous input power match and input noise match. To obtain a low NF the LNA should provide a low minimum NF as well as an input matching network which transforms the source impedance/admittance to the optimum impedance (Z_{opt})/admittance (Y_{opt}) [66, 67]. Moreover, for maximum power transfer, Z_{opt} should be the complex conjugate of the input impedance of the amplifier. The most common way to express the noise factor is through the noise parameters, as shown below:

$$F = F_{min} + \frac{R_n}{G_S}|Y_S - Y_{opt}|^2 \tag{2.50}$$

At mm-wave the device physics of the transistor have not changed. Thus the design for optimum noise performance remains the same. Attention during the design procedure should be paid on the assumption that the amplifier is unilateral. This only holds for cascade amplifiers and not for single-transistor amplifiers, since their output impedance matching network does affect their input impedance. Several design topologies around 30 GHz have been reported lately, spanning from single-transistor common source topologies to multi-stage topologies.

When a high gain is not required, e.g. in the case of a receiver where the mixer circuit drives an additional amplifier, a single-stage transistor common source topology can be used. This kind of topology also serves for ultra low noise design, since it consists of a single active device. An example of an LNA operating at 24 GHz can be found in [68]. The 90nm CMOS LNA is based on inductive degeneration and achieves 7.5 dB power gain, with 3.2 dB NF. The circuit works with a 1 V supply consuming 10.6 mA. Lower gain and higher NF have also been reported in [69] for a single-stage LNA at 20 GHz.

Many reported mm-wave amplifiers use the cascode topology. One advantage of the cascode topology is that it provides unconditional stability at the operating frequency, simplifying matching networks. Moreover a good output-input isolation is obtained. However, though in low frequencies the cascode topology is used to increase gain, at mm-wave frequencies, the pole introduced by the cascode transistor reduces gain and degrades NF [70]. The introduced pole depends on the common gate transistor's transconductance and the parasitic capacitance at the cascode node. In the equation below, indexes 1 and 2 correspond to the CS and CG transistors of the cascode topology, respectively.

$$\omega_p = \frac{g_m}{2C_{gd1} + C_{gs2} + C_{ds1}} \tag{2.51}$$

The parasitic capacitance on the cascode node can be tuned out using an inductor in series to the capacitance. An alternative approach is to use a series inductance between the CS and CG devices. This is preferred as it enhances noise performance, rejecting noise over a broad range of frequencies [66]. Inductive degeneration increases stability, decreases NF and improves linearity of the LNA. In addition, the degenerating inductor forces optimum noise and gain points close together. On the other hand the effective transconductance of the input stage is reduced also resulting in reduced gain. A new input matching technique for cascode LNAs at mm-wave, reported in [71, 72], provides moderately high gain with low NF and good input and output matching . Cascode amplifiers operating at mm-wave have also been reported in [71–75]

Increasing the number of stages increases power gain exponentially, but at the expense of power consumption, which increases linearly [66]. Therefore, the design of multi-stage amplifiers requires a proper choice of the topology and the biasing of each stage. A two-stage amplifier at 31-34 GHz, comprising of two individual cascode stages with interstage matching has been reported in [70]. The interstage matching boosts the power gain by 20% and the overall performance of the LNA is satisfactory, providing high gain and gain BW, low NF and power dissipation. A two-stage amplifier at 30 GHz with the first stage being a CS amplifier and the second stage a cascode amplifier also shows a high gain and noise performance, occupying a small area [76]. Both designs use microstrip transmission lines for input, output and interstage matching [76]. A two-stage and three-stage amplifier employing two and three transistors in CS topology are reported in [77, 78]. The two-stage topology has a peak gain frequency of 24 GHz at which the power gain is 13.1 dB and the NF 3.9 dB. The three-stage LNA has been fabricated for operation in two different frequencies, both in the K-band. As expected the three-stage amplifier exhibits higher NF and dissipates more power. Multi-stage LNAs operating at mm-wave frequencies have also been reported in [77, 79–84]

2.5 30 GHz LNA - Implementation and Results

2.5.1 Schematic Design

Cascode LNA has extensively been used in RF applications up to 5 GHz using several design methodologies [67]. However, recently published work [74, 75] also shows that there is space to exploit the advantages of the topology, even at mm-wave frequencies. This work also indicates that even under low voltage supply, at 1.2 V, implementing a high performance cascode LNA is still possible. The cascode LNA consists of three blocks, the input matching network, the gain stage and the output matching network. Since the implemented LNA will be measured as a standalone circuit, both input and output impedance are matched to 50 Ω. The analysis of the equivalent small-signal circuit including the input pad's capacitance, yields an input

impedance equal to:

$$Z_{in} = s(L_G + L_S) + \frac{1}{sC_{gs}} + \frac{1}{sC_{pad}} + \frac{g_m L_S}{C_{gs}} \tag{2.52}$$

From the two-port noise theory, the simultaneous noise input matching (SNIM) scheme which is used in this work, occurs when the input conductance reaches each optimum value,

$$G_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} \tag{2.53}$$

, where α is the ratio of gate conductance to output conductance for zero drain bias, δ and γ are noise parameters, to be analytically presented in Chapter 5, depending on the channel inversion level, and c is the correlation factor between gate current noise and drain current noise. A typical value of c, for the short channel regime is about 0.4 [17]. To achieve both input matching and minimize NF, the steps to be followed are described below:

1. The real part of Z_{opt} should equal the real part of source impedance. From this requirement the gate-source capacitance and channel width are calculated.

2. The real part of Z_{in} should equal the real part of source impedance. This step gives the inductance of L_S for a given power constraint.

3. From the last step, where the imaginary part of Z_{in} should equal the imaginary part of source impedance, the inductance of L_G is calculated.

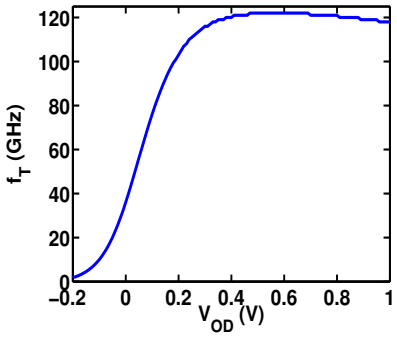


Figure 2.9: f_T versus overdrive voltage.

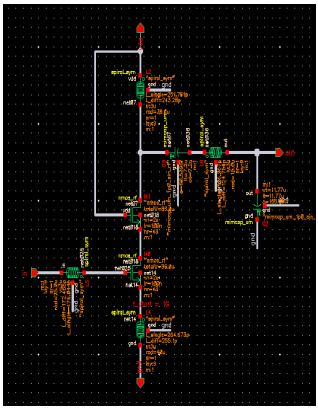


Figure 2.10: Schematic diagram of the LNA.

The optimum DC bias voltage for the common source transistor (M1) bias is found by plotting the unity gain frequency (f_T) with respect to the overdrive voltage (V_{OD}). f_T is a critical parameter since it affects both power gain and NF. Figure 2.9 shows that when $V_{OD} > 0.3V$, f_T remains constant. This gives $V_{GS} = 0.65V$. The gain stage, consisting of M1 and M2 cannot be considered unilateral (S_{12}=0). Thus there is strong interaction between input and output stages. The latter needs to deliver a purely real impedance. Therefore, an inductance L_D is used to tune out the overall capacitance at the LNA output, at 30 GHz. To further adjust the output impedance at 50 Ω, a T network is also used [31, 68, 73]. The schematic diagram is shown in Figure 2.10. The inductors values and transistors geometries are included in Table 2.1.

Component	Value		
	L (pH)	W (um)	L (nm)
L_G	176		
L_S	264		
L_D	251		
L_{out}	127		
M1		43x2	100
M2		43x2	100

Table 2.1: Values of the LNA components.

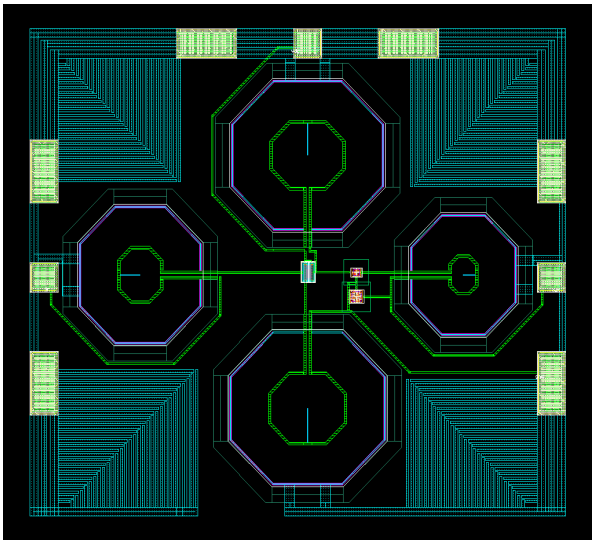


Figure 2.11: Cascode LNA Layout.

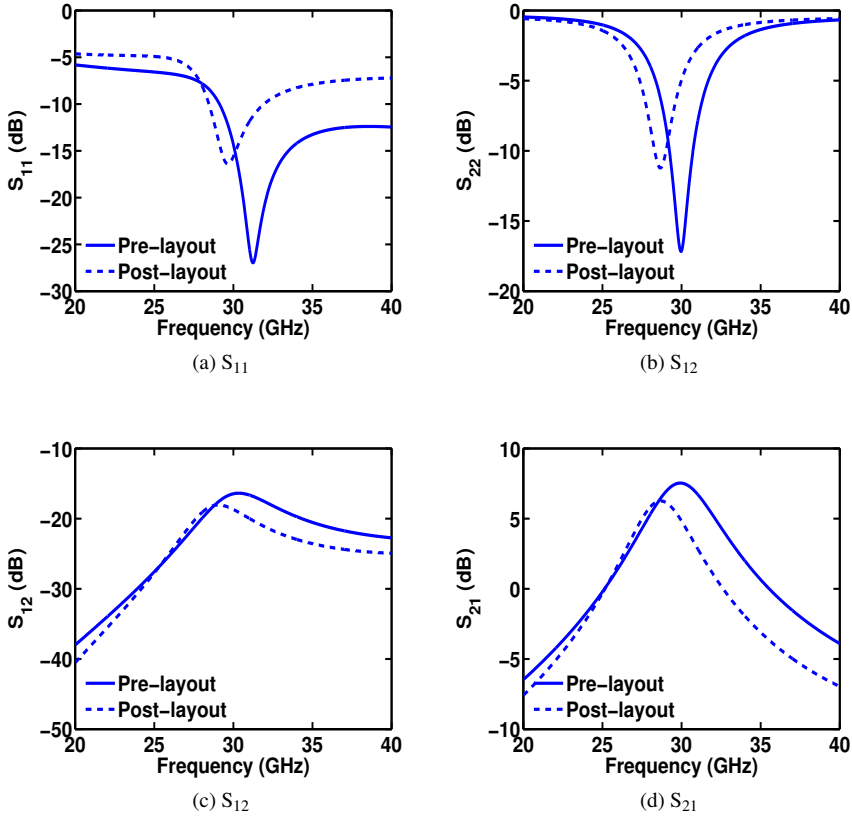
2.5.2 Layout Design

The uppermost metal of the design process (M9) is used for the interconnection lines. To ensure a good matching the same orientation is used for all components and a minimum distance is kept to reduce interaction between transmission lines and inductors. The width of the lines is determined by the maximum current that they have to drive. The pads have been designed so that their capacitance is kept at an acceptable low level. The total space that the layout occupies including pads is $0.37mm^2$ [6] and is presented in Figure 2.11.

2.5.3 Post-Layout Simulation Results

The simulation results were performed in Spectre simulator and corner analysis was used to validate the design. The scattering parameters of the LNA result from the small-signal analysis of the circuit. The input impedance match is represented by S_{11} and is shown in Figure 2.12a. Equivalently, S_{22} represents the output match and is depicted in Figure 2.12d. Values close to 12 dB are obtained for both. Reverse isolation($-S_{12}$) is plotted in Figure 2.12b and is about 18 dB. The LNA forward gain, which is the same with its voltage and power gain is 6 dB in the frequency range of 29 GHz, and is shown in Figure 2.12c. The 3-dB bandwidth is 4.5 GHz. The noise figure is 3.9 dB, exported by both small- and large-signal analysis and is presented in Figure 2.13. The LNA is unconditionally stable over the entire bandwidth as shown in Figure 2.14. The linearity of the circuit is high enough, so that the LNA can

receive a signal of -12 dBm, without being compressed (Figure 2.15a). The 3rd order intercept point is 4.9 dBm (Figure 2.15b). P_{1dB} and P_{IIP3} are exported through single and two-tone analysis, respectively. The total power consumption is limited to 7.2 mW from a voltage source of 1.2 V. The frequency shift in S-parameters between pre- and post-layout data is due to the RC parasitics generated after the layout simulation with Assura.



(a) S_{11} (b) S_{12}

(c) S_{12} (d) S_{21}

Figure 2.12: Scattering parameters of the LNA. Pre- and post-layout results.

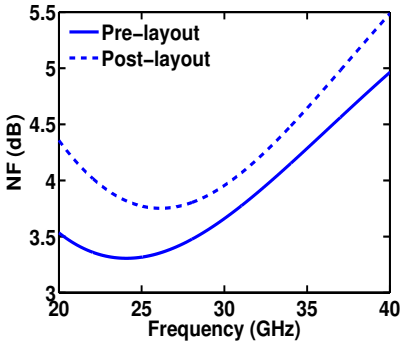


Figure 2.13: Noise figure of the LNA. Pre- and post-layout results.

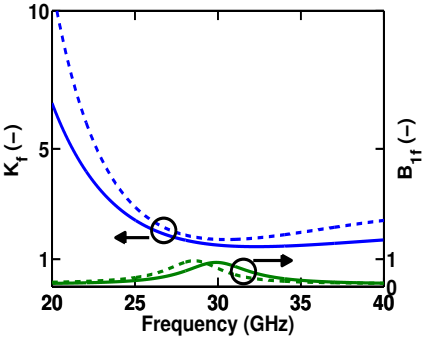
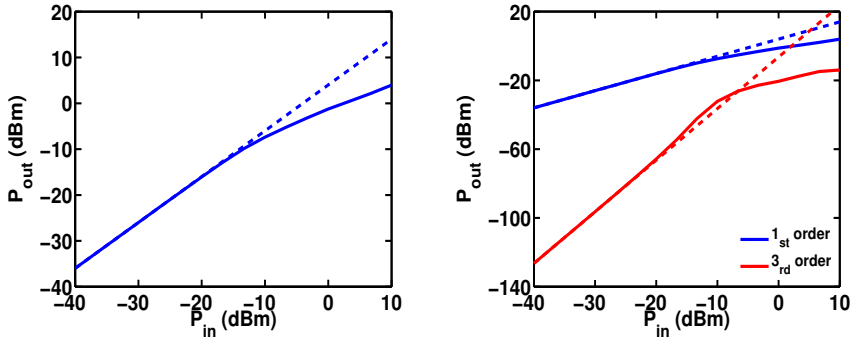


Figure 2.14: Stability factors of the LNA. Pre- and post-layout results.



(a) P_{1dB} (b) P_{IIP3}

Figure 2.15: 1 dB compression point and 3rd order input intercept point of the LNA. Post-layout results.

To compare this work with other published LNAs in K_a band, an overall FoM incorporating all individual FoM is used (2.54). The summarized results as well as comparison with other published work are presented in Table 2.2.

$$FoM = \frac{Gain\,(dB) \cdot IIP3\,(mW) \cdot f_c\,(GHz)}{(NF-1)\,(abs) \cdot P_{DC}(mW)} \tag{2.54}$$

	Summarized Results					
	This work (Cascode)	**This work (MF)**	[76]	[85]	[74]	[70]
Process (nm)	90	90	90	180	130	90
Freq. (GHz)	28.9	30	28.5	25.7	30	32.5
S_{21} (dB)	5.9	3.5	20	8.9	7.4	18.6
NF (dB)	3.9	2.4	2.9	6.9	3.7	3
IIP3 (dB)	4.9	5	-7.5	2.8	6	-
P_{DC} (mW)	7.2	12.5	16.2	54	7	10
Area (mm^2)	0.37	-	0.67	0.73	0.17*	0.85
FoM (-)	25.3	15.5	3.3	1.4	45.8	-

Table 2.2: Comparison of LNA performance.

2.5.4 Measurements

The LNA circuit consists of three GSG pads for input/output. The pitch is 125um.

- Left pad ("in +bias"): This is the input port (PORT 1) of the LNA. The RF signal as well as the DC bias for the common source transistor should be applied. Therefore, a bias tee is needed. The DC bias should be 0.65 V, whereas the input signal should be swept in frequency. It should be noted that the LNA works in the 30 GHz range. The input power may be varied from -35 to +10 dBm. The 1 dB compression point is expected to be about -5 dBm.
- Right pad ("out"): This is the output port (PORT 2) of the LNA. No DC bias has to be applied.
- Upper pad ("V_{DD}"): This pad is used for applying the supply voltage. Since all the ground pads are shorted in layout, a DC probe could be used. If the V_{DD} signal is provided by a DC power supply, the "-" of the channel should be shorted to the chasis ground. If instead, a RF probe is used, a second bias tee is needed to provide the bias voltage "V_{DD}". The measurement setup is depicted in Figure 2.16, where a RF probe is used for applying the voltage supply "V_{DD}".

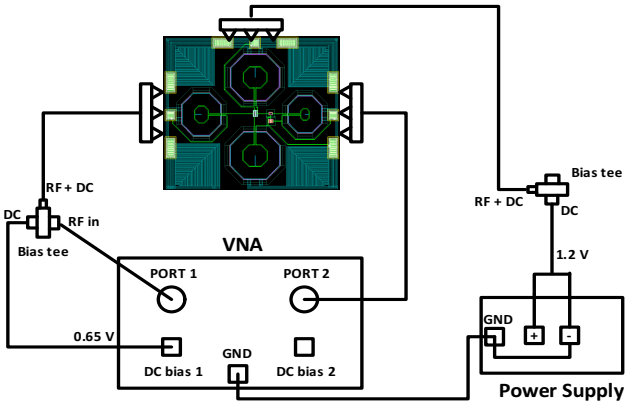
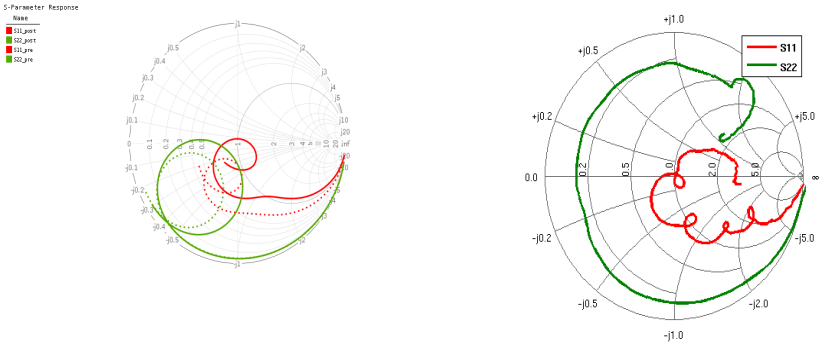


Figure 2.16: Measurement setup of the LNA.

The measured current, under V_{DS}=1.2 V and V_{GS}=0.65 V is equal to 6.5 mA, close to the simulated value of 6.2 mA. Simulation and measurement results for S_{11} and S_{22} are shown in Smith Chart diagram in Figure 2.17. The input matching network behaves as expected and an input impedance close to 50 Ω is measured. However, the output impedance experiences a significant difference between measured and simulated values. This is probably due to the output matching inductor, the model

of which seems to be unreliable. However, this is to be further investigated through additional electromagnetic simulations.



(a) $S_{11}$and S_{22} from pre- and post-layout simulations

(b) $S_{11}$and S_{22} from measurements

Figure 2.17: $S_{11}$and S_{22} for (a): pre- and post- layout simulations, and (b) measurements.

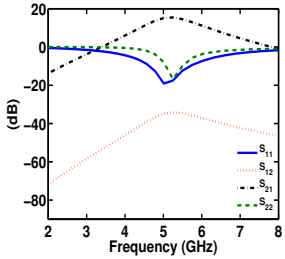
2.6 Low-power LNA Design at 5 GHz

Based on previous work from [86] a low-power LNA operating at 5.3 GHz was designed as part of a WiMAX receiver. According to the specifications obtained from the system level analysis of the WiMAX receiver [86], the LNA should have a noise figure less than 3 dB and a power gain of 18 dB, which could be relaxed if the gain of the variable gain amplifier is increased.

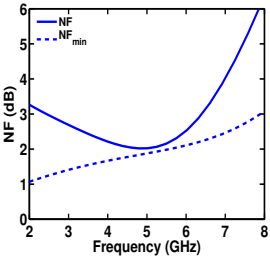
The inductively degenerated LNA exploits the great advantages of moderate inversion region, consuming a current of 1.47 mA, which corresponds to an inversion coefficient equal to 2.5. This value has been chosen following the analysis of transconductance frequency product FoM, which will be presented in Chapter 4. The LNA design has been performed using the extracted EKV3 model, rather than the commercial one. The circuit achieves a noise figure of about 2 dB, while its gain equals 15.4 dB. The circuit is matched for an input and output impedance of 50 Ω. The 1dB compression point is -18 dB. The LNA is unconditionally stable over its entire gain bandwidth. The LNA performance characteristics are summarized in Figure 2.18.

To compare this implementation with LNAs operating close to 5 GHz, we use formula (2.54). Interestingly, a high overall performance is obtained while power consumption is kept minimum and much lower compared to other work (Figure 2.19). This leads to two important conclusions. First, moderate inversion is a suitable region for high performance RFIC design. Moreover, FoM, simple to evaluate

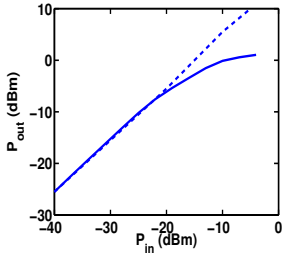
such as TFP, proves to be reliable in terms of RFIC design, since the optimum bias point can be easily calculated, using the inversion coefficient as a design guide.



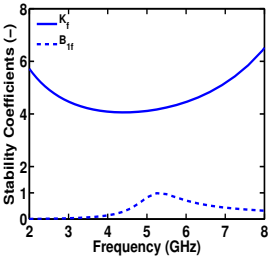
(a) S parameters



(b) NF and NF_{min}



(c) P_{1dB}



(d) Stability coefficients

Figure 2.18: Performance characteristics of the low-power 5 GHz LNA.

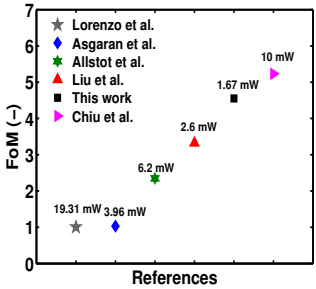


Figure 2.19: Performance comparison among this work and LNAs operating at 5 GHz.

Chapter 3

RF Test Chip: Fabrication and Measurements

3.1 Implementation of the RF Test Chip

For the needs of the thesis, several DC, CV and RF structures were designed and implemented in a single chip along with a low-noise amplifier operating at 30 GHz. The 90 nm mixed-signal (MS) low-power (LP) TSMC process was used in the context of a multi-project wafer (MPW) run. The overall chip area is 3.5 mm^2. Regarding the RF structures, which are of high interest to us, 10 NMOS and 10 PMOS multi-finger devices with channel lengths ranging from 240 to 100 nm and channel width from 10 to 200 um were fabricated. The RF MOS devices are considered as a two-port network with source and bulk being short-circuited and gate-source and drain-source acting as the input and output ports, respectively. Since the measurements were performed on wafer with a ground-signal-ground (GSG) configuration, the probing pads were designed to fit the probe pitch. Thus, dimensions of 35 um x 35 um and 75 um x 35 um were chosen, for the signal and the ground pads, respectively. All implemented devices are depicted in Figure 3.1.

To ensure a well defined ground-reference, the ground shielded technique [87, 88] was used. This was accomplished by connecting the ground pads directly to the ground shield, implemented in the bottom metal layer (M1) of the technology. The signal pad is isolated from the ground plane by using only some of the top metal layers. In this work M9, M8, and M7 were used for the signal pads. Yield is not the case in our study and thus the dissimilarity in the metal layers used for the pad design does not pose any limitation. Moreover the issue of different height between the ground and signal pads is negligible due to the high probing over-travel in CMOS measurements. The ground shield provides a low impedance path between all four ground pads. Furthermore, as both signals refer to the same ground plane, coupling

between them is reduced.

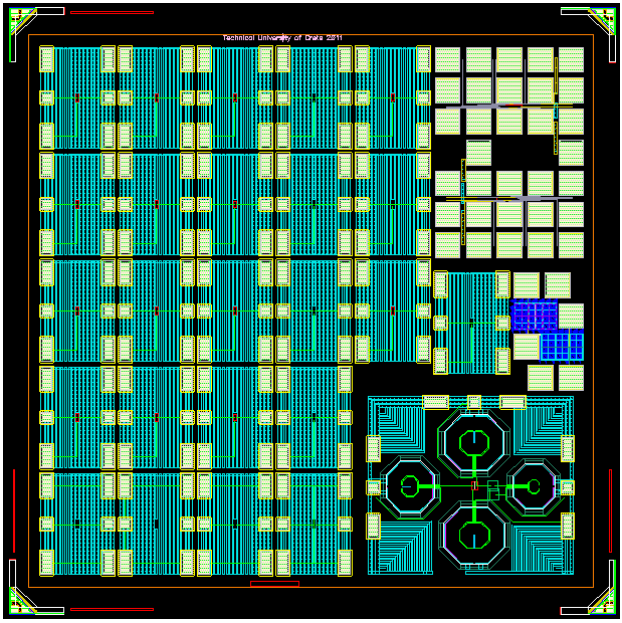


Figure 3.1: RF Test Chip.

3.2 Measurements

Noise measurements were performed in TU Dresden, using a system setup consisting of a probe station, a vector network analyzer, tuners, filters, switches, bias tees, a noise source from 1-50 GHz, and a spectrum analyzer with a noise figure measurement personality. For S-parameters measurements the tuner is set to 50 Ω, and the RF switches connect the device under test (DUT) to the VNA. For noise measurements the switches connect the noise source to the DUT input and the noise receiver to the DUT output. Maury microwave software has been used for configuring the noise setup. To apply the DC bias, a semiconductor parameter analyzer was also used. The noise measurement setup is presented in Figure 3.2. Due to the long time that is required for the noise measurements, a frequency step of 1 GHz has been chosen. Therefore, to allow for a more detailed small-signal analysis, S-parameters have

also been measured independently with a smaller frequency step. The measurement scenarios are analytically described below.

3.2.1 Noise Measurements

For noise measurements two scenarios were used:

- Drain-source and gate-source voltages constant at V_{DS}=1.2 V and V_{GS}=0.65 V, and frequency was swept from 8 to 50 GHz.
- Frequency and V_{DS} constant (f=10, 20, 30 GHz, and V_{DS}=1.2 V), and V_{GS} was swept from V_{GS}=0.3 to 1 V.

The minimum V_{GS} bias was kept at 0.3 V because at lower bias level the gain of the devices is generally not sufficient for reliable noise measurements. For all bias points the output current is also calculated. Hence, all noise characteristics can be derived versus drain current and inversion level.

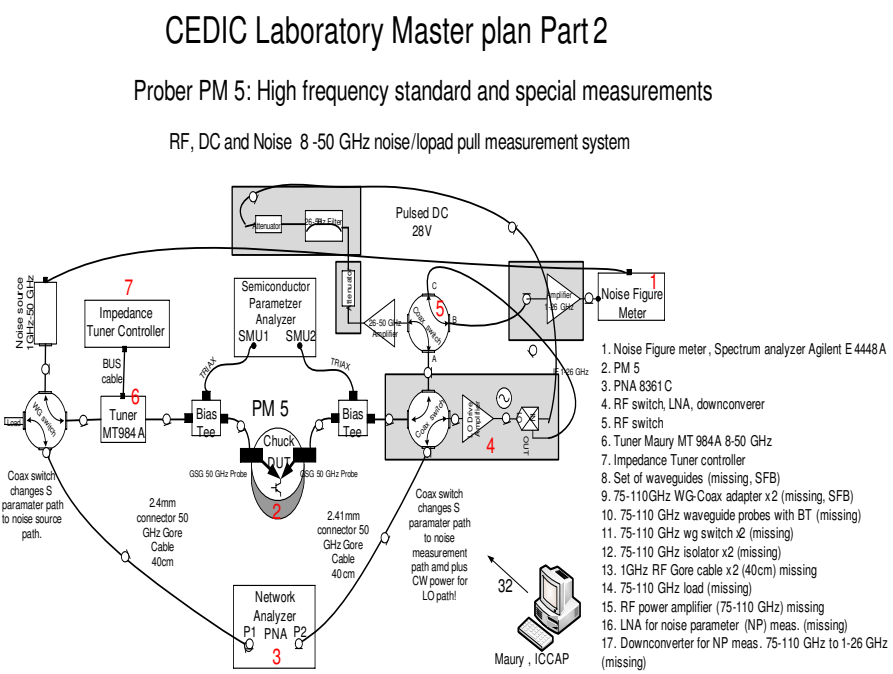


Figure 3.2: Noise measurement setup.

3.2.2 S-Parameters Measurements

For S-parameters measurements, a three-order sweep was performed in which for every combination of V_{DS} and V_{GS} values, frequency is swept. The exact values are given below. In total, 64005 points are calculated. For every combination between V_{DS} and V_{GS}, the drain current can be extracted through the DC measurements, which are performed for the same bias points.

- V_{DS}={0.05, 0.3, 0.8, 0.9, 1} V.
- V_{GS}={0:0.02:1} V.
- f={0.1:0.2:50.1} GHz.

3.3 De-embedding

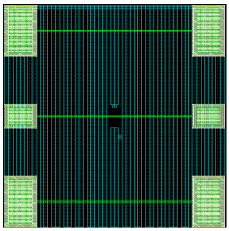
With the scaling of CMOS technology, transit frequencies up to 300 GHz have been reported [89] and thus, CMOS capabilities can be exploited for mm-wave design. In order to correctly predict the electrical behavior of RFICs, accurate modeling of MOS devices is of utmost importance. A model is developed based on measurements. Hence reliable measurements are also critical. RF MOS devices are usually measured with a ground-signal-ground (GSG) configuration. Therefore, contact pads are needed for S-parameter and noise measurements. To get the intrinsic performance of the device under test (DUT), two more steps are required, calibration and de-embedding. In order to know exactly what we are measuring all errors up to the probe tip must be removed. This includes internal VNA errors, the cables and probes.

First the reference plane should be shifted at the end of the VNA coax cables. This is done through calibration which is performed using specific standards from a substrate kit. Several calibration methods exist, depending on the standards that are used. In our case the short-open-load-through (SOLT) method was applied. In order to further move the reference plane from the probe pads to the DUT, de-embedding should be applied. Parasitics arising from interconnect lines between DUT and pads as well as pad parasitics, have to be subtracted from the measurements on the test structure. The process of removing the unwanted parasitics from measurements is called de-embedding. As already mentioned, for noise de-embedding, RF measurements have to be performed along with noise measurements to allow for the de-embedding for noise and parasitics. In the following sections the de-embedding methods that were used in this work are described and the corresponding results, for measured and de-embedded data, are presented in terms of Y-parameters, RF figures of merit and noise parameters.

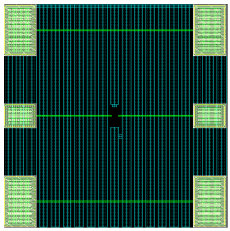
3.3.1 RF De-embedding

For de-embedding purposes dummy structures with a known RF behavior in terms of their correspondent S-parameters are used. Depending on the de-embedding technique, these dummies may include the “open”, “short”, “thru”, “open-short”, “short-open” as well as combinations among them [90].

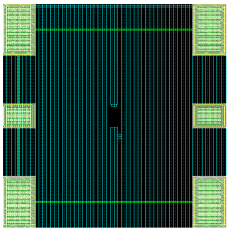
The simplest de-embedding method proposed in [91], uses only the “thru” dummy. The method has been validated up to 110 GHz. However it has only been applied to on-chip passive devices (inductors, RF capacitors etc.) and is therefore not suitable for active devices. The standard method which is widely used in industry is the simple open-short method [92], in which parallel and series parasitics are excluded from the test structure through a two-step process using Y- and Z-matrices, respectively. Eventually the procedure is validated using the “thru” dummy. Several other methods have been proposed including the four-step de-embedding process [93] and a technique employing three thru and one open dummy [94].



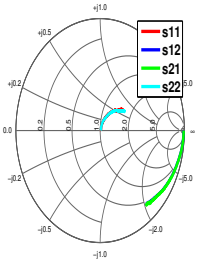
(a) “Thru” dummy



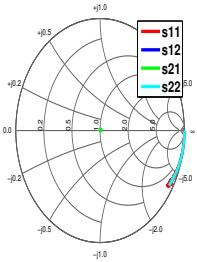
(b) “Open” dummy



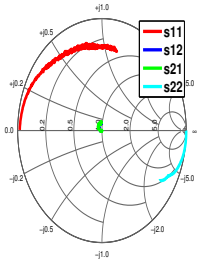
(c) “Simple short - Simple open” dummy



(d) “Thru” response



(e) “Open” response



(f) “Simple short - Simple open” response

Figure 3.3: Layout and S-Parameter response of de-embedding structures.

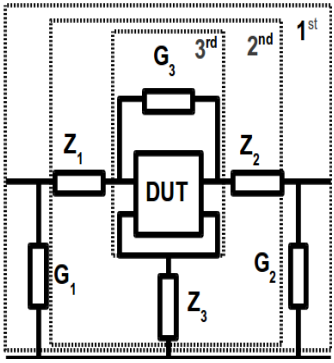
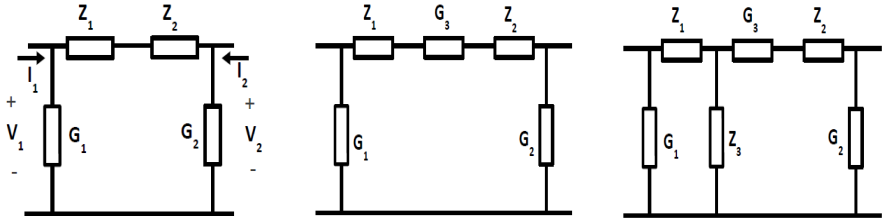


Figure 3.4: 3 step de-embedding procedure.



(a) "Thru" dummy (b) "Open" dummy (c) "Short1" dummy

Figure 3.5: Equivalent circuits for de-embedding structures.

In this work, the improved three-step de-embedding technique proposed by Vandamme et al. [95] was implemented and is presented below. The dummy structures that were fabricated and used were the "thru", "open" and "simple short-simple open". The layout of these structures is presented in Figure 3.3, with their S-parameters response in Smith Chart, up to 50 GHz. The equivalent circuits for the dummies can be found in [96]. In general, the open has a capacitive response, contrary to the short which can be modeled by lossy inductors between the two ports. The thru dummy can be represented by a transmission line with a specific impedance and time delay. For the calculation of parasitic elements, the equivalent circuit of Figure 3.4 is used. Admittances G_1, G_2, and G_3 represent the coupling via the metal interconnects and the silicon substrate between the gate-source (Port 1), drain-source (Port 2), and gate-drain, respectively. Impedances Z_1 and Z_2 stand for the series impedances between port 1 and port 2 on one hand and the DUT on the other, whereas Z_3 represents the ground leads toward the DUT. Impedances and conductances can be evaluated by analyzing and applying KVL and KCL to the equivalent circuits of the de-embedding structures, presented in Figure 3.5a. For

example one may calculate G_1 through the equivalent circuit of thru as:

$$I_1 = V_1 G_1 + \frac{V_1 - V_2}{Z_1 + Z_2} \tag{3.1}$$

$$I_2 = V_2 G_2 + \frac{V_2 - V_1}{Z_1 + Z_2} \tag{3.2}$$

From (3.1) and (3.2), the thru Y-matrix can be calculated as:

$$Y_{thru} = \begin{bmatrix} G_1 + \frac{1}{Z_1+Z_2} & -\frac{1}{Z_1+Z_2} \\ -\frac{1}{Z_1+Z_2} & G_2 + \frac{1}{Z_1+Z_2} \end{bmatrix} \tag{3.3}$$

Therefore:

$$Y_{11,thru} = G_1 + \frac{1}{Z_1 + Z_2} \tag{3.4}$$

$$Y_{12,thru} = -\frac{1}{Z_1 + Z_2} \tag{3.5}$$

$$Y_{21,thru} = -\frac{1}{Z_1 + Z_2} \tag{3.6}$$

$$Y_{22,thru} = G_2 + \frac{1}{Z_1 + Z_2} \tag{3.7}$$

Summing the left and right parts of (3.4) and (3.6), G_1 is calculated as:

$$G_1 = y_{11,thru} + y_{21,thru} \tag{3.8}$$

Similarly,

$$G_2 = Y_{21,thru} + Y_{22,thru} \tag{3.9}$$

$$G_3 = -\frac{Y_{21,open} Y_{21,thru}}{Y_{21,open} + Y_{21,thru}} \tag{3.10}$$

$$Z_2 = -\frac{1}{Y_{12,sh1}} - \frac{1}{G_3} \tag{3.11}$$

$$Z_1 = -\frac{1}{Y_{21,thru}} - Z_2 \tag{3.12}$$

$$Z_3 = -\frac{1}{Y_{21,sh1}} - Z_1 \tag{3.13}$$

Equations (3.11), (3.12), and (3.13) are derived under the assumption that: $\frac{1}{G_3} + Z_x \gg Z_3$, with $Z_x = Z_1$ *or* Z_2 [95]. It should be underlined that some of the Y-parameters cannot be used for extracting the parasitics e.g. Y_{12} of "simple short-simple open" (also referred as "Short1"), since the two ports have a very small coupling.

The three-step de-embedding process is described below.

1. First the measured S-parameters are converted to Y-parameters. Admittances G_1 and G_2 are then subtracted:
2. Y_A is then converted to its equivalent Z matrix and series impedances can be accounted through (3.15).
3. Z_B is again converted to Y_B and conductance G_3 is subsequently subtracted, resulting in the Y-parameters of the DUT, as described in (3.16).

$$Y_A = Y_{meas} - \begin{bmatrix} G_1 & 0 \\ 0 & G_2 \end{bmatrix} \tag{3.14}$$

$$Z_B = Z_A - \begin{bmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{bmatrix} \tag{3.15}$$

$$Y_{DUT} = Y_B - \begin{bmatrix} G_3 & -G_3 \\ -G_3 & G_3 \end{bmatrix} \tag{3.16}$$

Y-parameters that are meaningless in terms of determining the unwanted parasitics can be used for validating the de-embedding procedure. These are then compared to their theoretical values calculated from the equivalent circuits of Figure 3.5. The validation process is shown in Figure 3.6 for Y-parameters $Y_{11,thru}$, $Y_{22,sh1}$, and $Y_{12,sh1}$, up to 50 GHz. Symbols correspond to measurements whereas lines represent the theoretically calculated values. The agreement between measured and modeled results also indicates that the layout of the de-embedding structures is correctly represented by their equivalent circuits [95].

The importance of de-embedding DUTs from parasitics becomes evident by comparing de-embedded RF FoMs, such as transit frequency f_T, and maximum oscillation frequency, f_{max}, with measured data. These are extracted from Y-parameters, and thus it is also interesting to observe their behavior with and without de-embedding. Figure 3.7 and Figure 3.8 represent Y-parameters in terms of real and imaginary parts for NMOS and PMOS devices of channel length L=100 nm, channel width W=40x2 um, biased at $|V_{DS}|$=1 V, and $|V_{GS}|$=0.4 V, from 1 - 30 GHz. It is worth noticing the behavior of real parts of Y_{21} and Y_{22}, which correspond to gate transconductance g_m, and output conductance g_{ds} respectively, at low frequencies. A quite significant difference between measured and de-embedded f_T values is observed in Figure 3.9, for both NMOS and PMOS devices. Specifically, de-embedded f_T is about 10 GHz higher than its measured data. A smaller though still present difference is obtained

for f_{max}, as presented in Figure 3.10. Both FoMs are plotted with respect to a common measure of channel inversion level, called inversion coefficient, which results from normalizing drain current I_D to specific current I_{spec}, as IC=I_D/I_{spec} and will be analyzed in Appendix. Both f_T and f_{max} are calculated at f_{spot}=3.1 GHz.

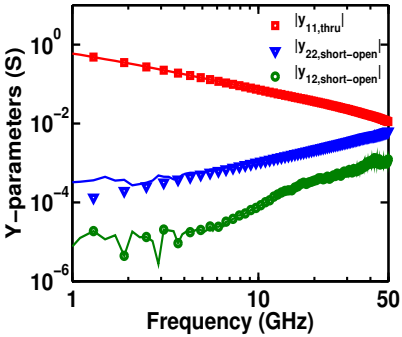
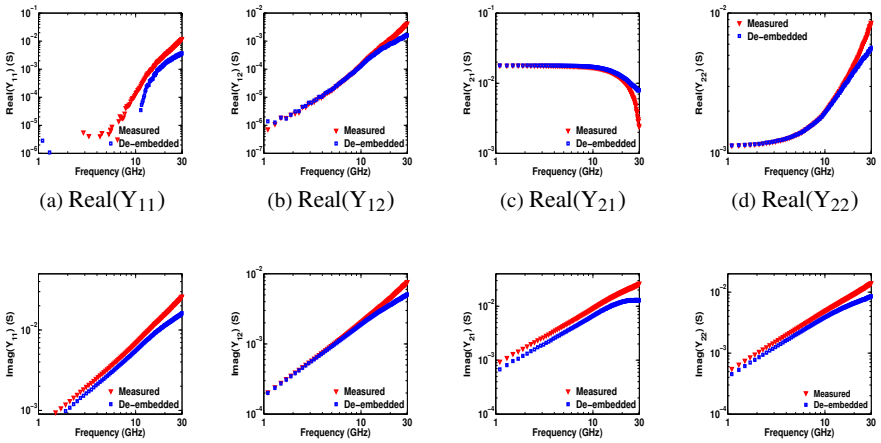


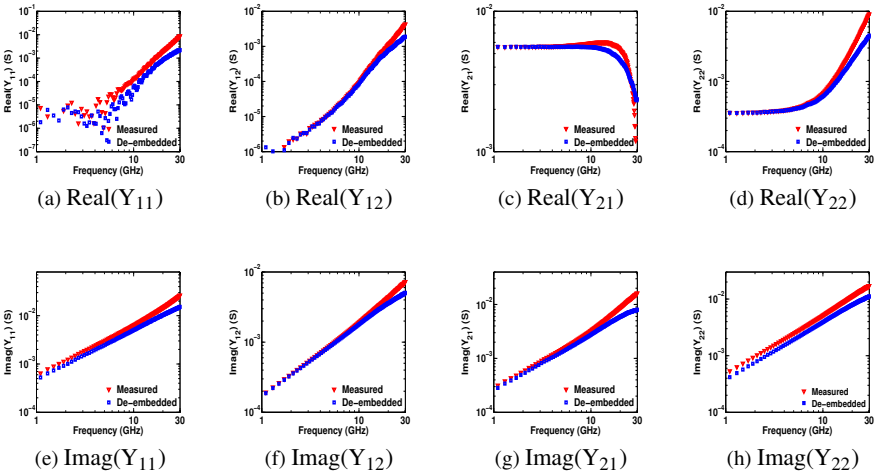
Figure 3.6: Measured and modeled Y-parameters of de-embedding structures for de-embedding verification.



(a) Real(Y_{11}) (b) Real(Y_{12}) (c) Real(Y_{21}) (d) Real(Y_{22})

(e) Imag(Y_{11}) (f) Imag(Y_{12}) (g) Imag(Y_{21}) (h) Imag(Y_{22})

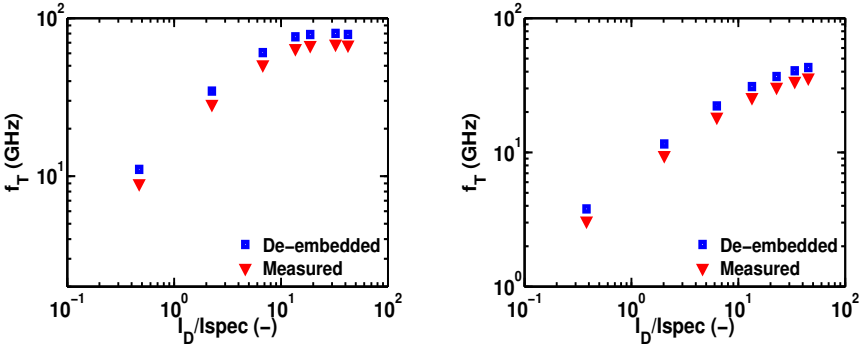
Figure 3.7: Real and Imaginary parts of Y-parameters vs. frequency, for a NMOS device of L=100 nm and W=40x2 um, biased at V_{DS}=1 V and V_{GS}=0.4 V.



(a) Real(Y_{11}) (b) Real(Y_{12}) (c) Real(Y_{21}) (d) Real(Y_{22})

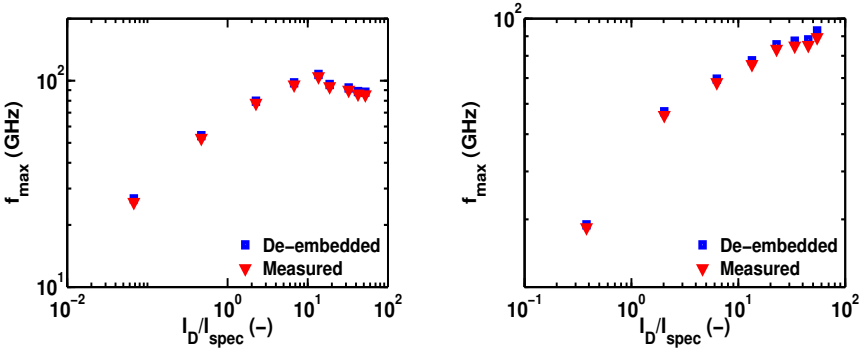
(e) Imag(Y_{11}) (f) Imag(Y_{12}) (g) Imag(Y_{21}) (h) Imag(Y_{22})

Figure 3.8: Real and Imaginary parts of Y-parameters vs. frequency, for a PMOS device of L=100 nm and W=40x2 um, biased at $|V_{DS}|$=1 V and $|V_{GS}|$=0.4 V.



(a) NMOS (b) PMOS

Figure 3.9: Measured and de-embedded data for transit frequency vs. normalized current for devices of L=100 nm and W=40x2 um, biased at $|V_{DS}|$=1V, at f=3.1 GHz.



(a) NMOS (b) PMOS

Figure 3.10: Measured and de-embedded data for maximum oscillation frequency vs. normalized current for devices of L=100 nm and W=40x2 um, biased at $|V_{DS}|$=1V, at f=3.1 GHz.

3.3.2 Noise de-embedding

For high frequency operation, the noise generated within ultra-deep-submicron MOS devices dominates the overall noise performance of analog/RF circuits [96]. Therefore it is crucial to identify noise characteristics of the DUT, excluding probe pads and interconnect lines. Noise de-embedding techniques in linear two-port networks are based on the noise power matrix, also called noise correlation matrix [96]. The correlation matrix, C_A, is defined by 3.17. In general, the DUT can be modeled either in a parallel-series configuration, or in a cascade configuration. In the former, the open and short dummy structures are used to de-embed the RF probe pad parasitics from the measured noise parameters. In the latter, the equivalent circuit is considered as a cascade of networks consisting of the probe pads, interconnections and the transistor, with each of these described by an equivalent matrix. For the cascade configuration, several noise de-embedding techniques have been proposed, employing different dummy structures [96–104]. In all cases, S-parameters measurements have to be performed along with noise measurements, at the same bias and frequency conditions, to allow for the de-embedding.

$$C_A = 2kT \begin{bmatrix} R_n & \frac{NF_{min}-1}{2} - R_n Y_{opt}^* \\ \frac{NF_{min}-1}{2} - R_n Y_{opt} & R_n |Y_{opt}|^2 \end{bmatrix} \tag{3.17}$$

In this work, noise measurements have been de-embedded using the open and thru structures, according to [96–98]. The de-embedding process includes eleven

steps which result in the correlation matrix of the intrinsic transistor, C_A. The complete proces is described below.

1. Measure the S-parameters of the DUT, open and thru, $[S^{DUT}]$, $[S^{OPEN}]$, $[S^{THRU}]$.
2. Measurre the noise parameters - NF_{min}^{DUT}, Y_{opt}^{DUT}, R_n^{DUT} of the DUT and calculate the noise correlation matrix $[C_A^{DUT}]$ using 3.17.
3. Convert $[S^{OPEN}]$ to $[Y^{OPEN}]$ and calculate $Y_{PAD} = Y_{11}^{OPEN} + Y_{12}^{OPEN}$ and the ABCD parameters of the input/output pads $[A^{PAD}] = \begin{bmatrix} 1 & 0 \\ Y_{PAD} & 1 \end{bmatrix}$.
4. Calculate $[A^{THRU}]$ from $[S^{THRU}]$.
5. Calculate the ABCD matrices:
   $[A^{IN}] = [A^{THRU}][A^{PAD}]^{-1}$and $[A^{OUT}] = [A^{PAD}]^{-1}[A^{THRU}]$, which include the parasitic effects of probe pads and interconnections connected in cascade at the input and output ports. The superscript "-1" denotes the inverse of the matrix.
6. Convert $[S^{DUT}]$ to $[A^{DUT}]$ and calculate $[A^{TRANS}] = [A^{IN}]^{-1}[A^{DUT}][A^{OUT}]^{-1}$.
7. Convert $[A^{IN}]$ and $[A^{OUT}]$ to $[Z^{IN}]$ and $[Z^{OUT}]$.
8. Calculate the correlation matrices:
   $[C_Z^{IN}] = 2kT\Re([Z^{IN}])$ and $[C_Z^{OUT}] = 2kT\Re([Z^{OUT}])$, which include parasitic effects from the probe pads and interconnects connected in cascade at the input and output ports, respectively.
9. Convert $[C_Z^{IN}]$ and $[C_Z^{OUT}]$to their correlation chain matrices:
   $[C_A^{IN}] = [T^{IN}][C_Z^{IN}][T^{IN}]^T$, and $[C_A^{OUT}] = [T^{OUT}][C_Z^{OUT}][T^{OUT}]^T$, where superscript "T" is the transpose of the matrix. $[T^{IN}]$ and $[T^{OUT}]$are given by: $[T^{IN}] = \begin{bmatrix} 1 & -A_{11}^{IN} \\ 0 & -A_{21}^{IN} \end{bmatrix}$ and $[T^{OUT}] = \begin{bmatrix} 1 & -A_{11}^{OUT} \\ 0 & -A_{21}^{OUT} \end{bmatrix}$.
10. Calculate the correlation matrix of the intrinsic transistor:
    $[C_A] = [A^{IN}]^{-1}([C_A^{DUT}] - [C_A^{IN}])([A^{IN}]^T)^{-1} - [A^{TRANS}][C_A^{OUT}][A^{TRANS}]^T$.
11. Once C_A is derived, noise parameters can be evaluated via equations (3.18), (3.19), and (3.20).

$$NF_{min} = 1 + \frac{1}{kT}(\Re(C_{12A}) + \sqrt{C_{11A}C_{22A} - (\Im(C_{12A}))^2}) \tag{3.18}$$

$$Y_{opt} = \frac{\sqrt{C_{11A}C_{22A} - (\Im(C_{12A}))^2} + i\Im(C_{12A})}{C_{11A}} \tag{3.19}$$

$$R_n = \frac{C_{11A}}{2_{kT}} \tag{3.20}$$

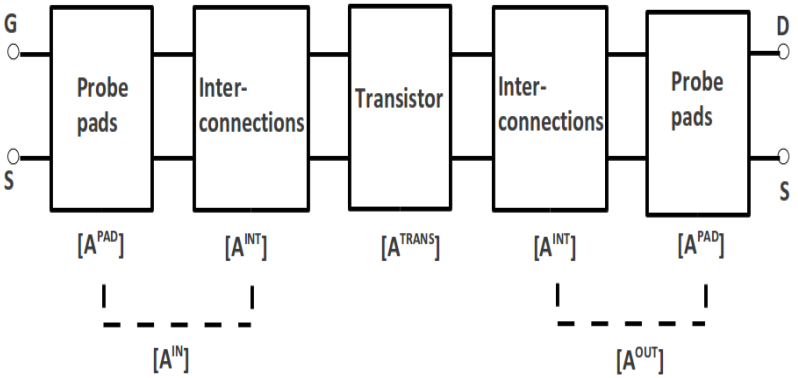
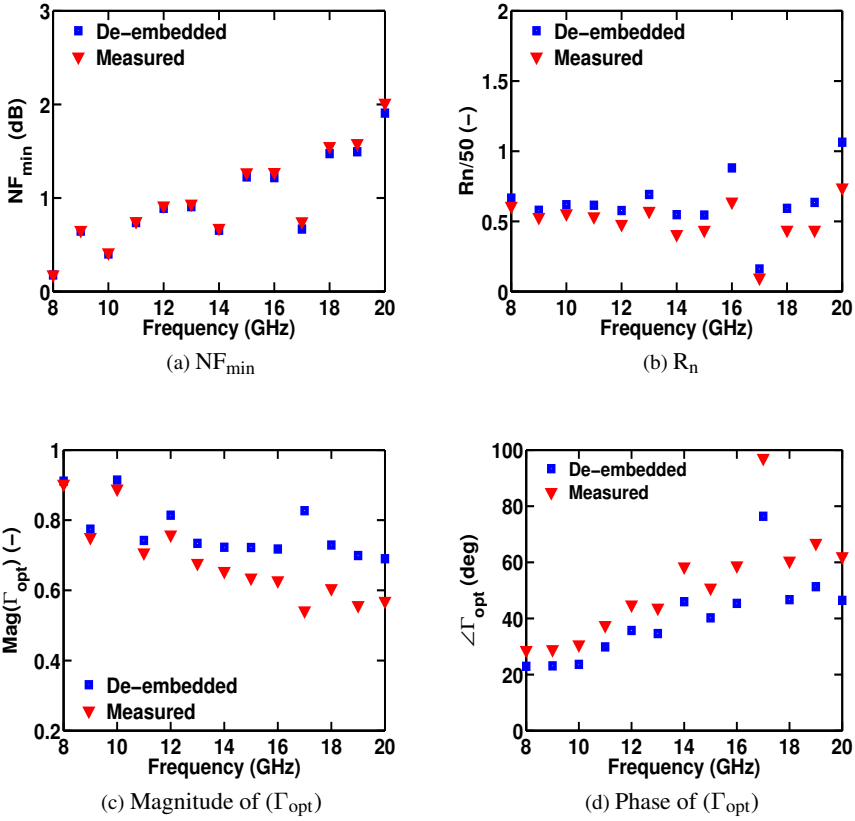


Figure 3.11: Equivalent circuit diagram of the structure of a DUT, including probe pads, metal interconnections and a transistor in a cascade configuration.

De-embedding results are presented in Figure 3.12 and Figure 3.13, for NMOS and PMOS devices, respectively, up to 20 GHz. All devices are biased at $|V_{DS}|$=1.2 V and $|V_{GS}|$=0.65 V. Noise parameters are presented with and without applying noise de-embedding, with optimum source reflection coefficient being represented by its magnitude and phase. The impact of noise de-embedding is clear in these graphs, for all noise parameters and for the entire frequency range. Results are in line with those presented in [99, 100, 103]



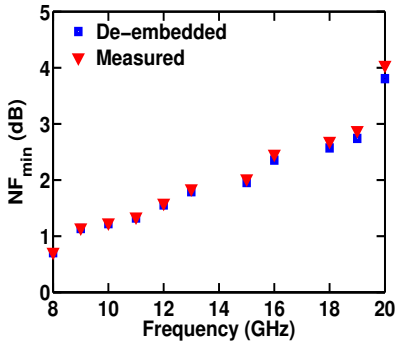
(a) NF_{min}

(b) R_n

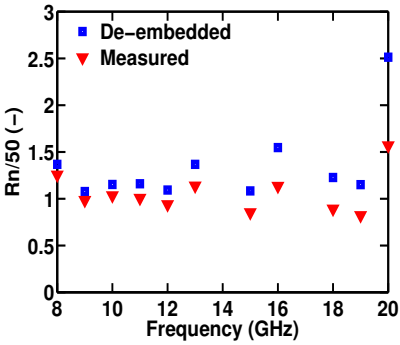
(c) Magnitude of (Γ_{opt})

(d) Phase of (Γ_{opt})

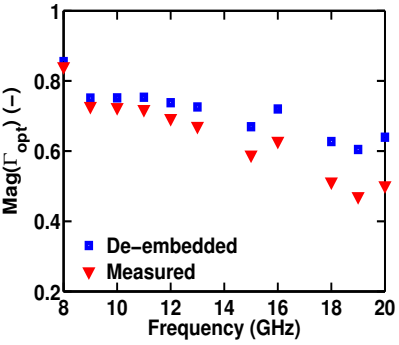
Figure 3.12: Noise parameters for NMOS device of L=100 nm and W=40x2 um, biased at V_{GS}=0.65 V and V_{DS}=1.2 V.



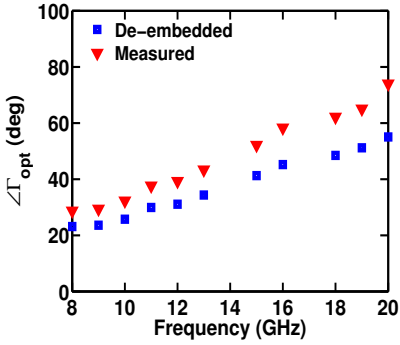
(a) NF_{min}



(b) R_n



(c) Magnitude of (Γ_{opt})



(d) Phase of (Γ_{opt})

Figure 3.13: Noise parameters for PMOS device of L=100 nm and W=40x2 um, biased at $|V_{GS}|$=0.65 V and $|V_{DS}|$=1.2 V.

Chapter 4

Figures of Merit for RFIC Design

In this chapter high frequency modeling is presented in the context of the EKV3 compact model and quasi-static (QS) and non-quasi-static (NQS) operations of the MOST are discussed. The impact of extrinsic components on CMOS RF performance is also investigated. From the circuit perspective, RF conventional FoM extracted from Y-parameters, are presented and modeled. Advanced FoM, suitable for RFIC design - particularly LNA design - such as transconductance frequency product and gain transconductance frequency product are also analyzed. All FoM are presented with respect to inversion coefficient and scaling. Additional TCAD simulation data are provided along with measurements of the investigated 90 nm process, for technology nodes of 180, 90, 45, and 22 nm. Non-linearities of the 90 nm CMOS process and TCAD data are also investigated for all available channel length n- and p-MOS devices, in terms of performance metrics such as the third order input intercept point. Non-linearities are extracted from DC as well as RF measurements and are plotted versus IC. For all FoM, a evident shift in their optimum performance to lower inversion levels is observed with channel length scaling. Particularly, for LNA, optimum performance is achieved close to the middle of moderate inversion, for the shortest device of L=22 nm.

4.1 High Frequency Modeling

With frequency increase the design characteristics of a MOS device, such as transconductance, gain, NF_{min}, start to degrade. Since both the intrinsic and extrinsic part of the device contribute to this degradation, the transistor needs to be split in its intrinsic and extrinsic parts each of which should be properly taken into account in determin-

ing its high frequency performance. At relatively low frequencies, well below the f_T the transistor operation is described as static or quasi-static . This means that for every change of voltages in the device terminals, the transit time within the channel is actually zero, and hence the device current response is immediate. Above a certain frequency, called quasi-static frequency, ω_{qs}, charges need time to adjust to voltage changes. The charge density is now dependent not only on the instantaneous voltage value but also on the past values that resulted in the specific charge density. The normalized quasi-static frequency (Ω_{qs}), in terms of normalized charges, is given by:

$$\Omega_{qs} \equiv \frac{\omega_{qs}}{\omega_{spec}} \equiv \frac{\tau_{spec}}{\tau_{qs}} = 30\frac{(q_s+q_d+1)^3}{4q_s^2+4q_d^2+12q_sq_d+10q_s+10q_d+5} \tag{4.1}$$

, where

$$\omega_{spec} = \frac{1}{\tau_{spec}} = \frac{\mu U_T}{L^2} \tag{4.2}$$

Ω_{qs} can stand as a FoM for the MOS device since it represents the frequency the device can reach without accounting for the extrinsic parasitic components [4]. The intrinsic NQS equivalent circuit is shown in Figure 4.1a. The circuit entails five admittances (Y_{GBi}, Y_{GSi}, Y_{GDi}, Y_{BSi}, Y_{BDi}) and three transadmittances (Y_m, Y_{ms}, Y_{md}) connected between drain and source and controlled by the gate. These are consequently modeled by voltage-controlled-current-sources (VCCS) defined by:

$$I_m = Y_m \Delta V_G \tag{4.3}$$

$$I_{ms} = Y_{ms} \Delta V_S \tag{4.4}$$

$$I_{md} = Y_{md} \Delta V_D \tag{4.5}$$

The equivalent QS intrinsic circuit in Figure 4.1b is derived by the NQS circuit in which admittances are replaced by capacitances. Transadmittances are now derived by:

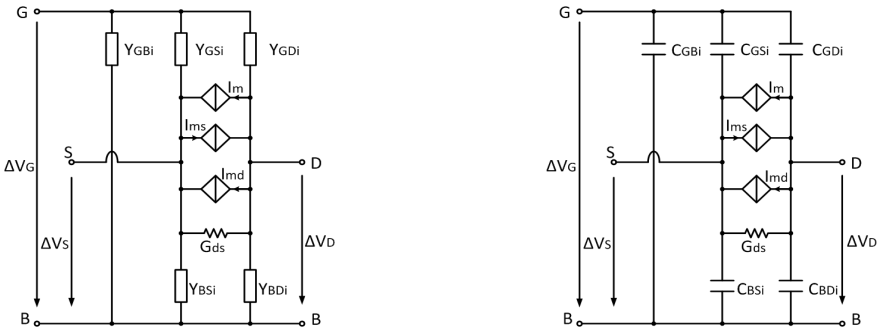
$$Y_m = G_m(1 - j\omega\tau_{qs}) \tag{4.6}$$

$$Y_{ms} = G_{ms}(1 - j\omega\tau_{qs}) \tag{4.7}$$

$$Y_{md} = G_{md}(1 - j\omega\tau_{qs}) \tag{4.8}$$

Even at RF the NQS model is seldom used due to its complexity. As a rule of thumb, in order not to have any performance degradation due to NQS, ω_{qs} has to be much higher than the operating frequency (approximately 5-7 times) [4]. Increasing

ω_{qs}, can be done by increasing the bias current but at the expense of higher power consumption.



(a) Non quasi-static (b) Quasi-static

Figure 4.1: Small-signal equivalent circuits of a MOST.

4.2 MOS Extrinsic Part

Besides the intrinsic part, which determines the device performance at relatively low frequencies, the extrinsic part of the device becomes significant with increasing frequency, specifically for short channel devices. The two parts are distinguished by the internal nodes (gi, di, si, bi) which are depicted in Figure 4.2. The connection between the intrinsic and extrinsic parts of the device is done through the source-drain extensions (SDE), as well as the source and drain diffusions [105]. These parts add some parasitic resistances which are modeled by the source and drain resistances R_S and R_D. The access to the gate can be modeled with an equivalent resistance, R_G. R_G should be kept small enough via proper layout, since it greatly affects RFIC design [106]. In order to model the substrate network, several approaches have been introduced [107–114]. The simpler entails the usage of a substrate resistance R_B, which is sufficient in most of the cases. However in certain circumstances, e.g. in the slope of the unilateral power gain, which changes from the -20 dB/decade at low inversion levels, more detailed substrate network modeling is needed.

Because of the SDE, parasitic capacitances are also present in the extrinsic device part. The overlap capacitances between gate and source C_{GSo} and gate and drain, C_{GDo} are due to the overlap of the gate oxide over the SDE. In short channel devices and strong inversion, parasitic capacitances contribute about half of the total capacitance, and thus need to be accurately modeled. The gate to bulk capacitance, C_{GBo}, which is due to the extension of the gate electrode above the field oxide and on top of the substrate [4], slightly affects the total capacitance.

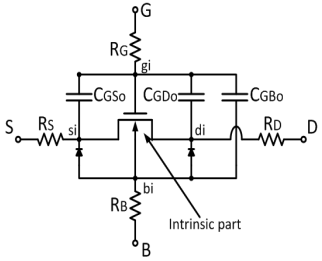


Figure 4.2: Equivalent circuit of the extrinsic part of a MOST.

4.3 Transistor Figures of Merit

Small-signal analysis is investigated and validated through on-wafer measurements of S-parameters. Subsequently, S-parameters are converted to Y-parameters. Y-parameters offer a convenient way to extract transistor FoM, such as transit frequency, maximum oscillation frequency and unilateral gain. Additionally, critical model parameters, such as overlap capacitances and parasitic resistances, previously described, can also be derived. Analytical expressions for the Y-parameters of a MOSFET in saturation are presented in the equations below. A detailed circuit analysis on the extraction of Y-parameters, can be found in [105].

$$Y_{11} \cong \omega^2 R_G C_G^2 + j\omega C_G \tag{4.9}$$

$$Y_{12} \cong -\omega^2 R_G C_{GD} C_G - j\omega C_{GD} \tag{4.10}$$

$$Y_{21} \cong G_m - \omega^2 R_G C_G (C_{GD} + C_m) - j\omega (C_{GD} + C_m) \tag{4.11}$$

$$Y_{22} \cong G_{ds} + \omega^2 R_G (C_G C_{BD} + C_G C_{GD} + C_{GD} C_m) + j\omega (C_{BD} + C_{GD}) \tag{4.12}$$

C_m is the intrinsic gate transcapacitance. C_G is the total gate capacitance, including both the intrinsic and extrinsic capacitances:

$$C_G \equiv C_{GS} + C_{GD} + C_{GB} \tag{4.13}$$

C_G and C_{GD} are extracted from (4.9) and (4.10) as:

$$C_G = \frac{Imag(Y_{11})}{\omega} \tag{4.14}$$

$$C_{GD} = \frac{Imag(Y_{12})}{\omega} \tag{4.15}$$

C_{GS} is then calculated via (4.13) assuming operation in strong inversion and saturation, where C_{GB} is negligible. Parasitic gate resistance can be derived from (4.9) as:

$$R_G = \frac{Real(Y_{11})}{(Imag(Y_{11}))^2} \tag{4.16}$$

4.3.1 Transit Frequency

A commonly used RF FoM for transistors is the unity gain frequency. It corresponds to the frequency where the current gain of a common-source amplifier falls to unity. The current gain is calculated through the h_{21} hybrid parameter of the two-port network as:

$$h_{21} \equiv \frac{I_2}{I_1} \mid_{V_2=0} = \frac{Y_{21}}{Y_{11}} \cong \frac{G_m}{j\omega C_G} = \frac{\omega_t}{j\omega} \tag{4.17}$$

ω_t is the unity gain frequency in rad/sec given by the ratio of gate transconductance to the total gate capacitance:

$$\omega_t = \frac{G_m}{C_G} \tag{4.18}$$

Given the S-parameters, the transit frequency in Hz can be calculated by first converting S- to H-parameters and then taking the imaginary part of h_{21} as:

$$f_T = Imag(h_{21}) f_{spot} \tag{4.19}$$

, where f_{spot} is a relatively low frequency, approximately in the range of 1-5 GHz. Alternatively, f_T can be extracted by extrapolating h_{21} in strong inversion and saturation, where the slope is known to be -20 db/dec. The frequency point where h_{21} equals one (or zero dB) is the f_T.

4.3.2 Maximum Oscillation Frequency

Maximum oscillation frequency stands as a FoM to compare RF performance among MOS devices. It is directly connected to unilateral gain, U. The latter is the maximum available gain of a two-port network, assuming its feedback admittance Y_{12} is neutralized (Y_{12}=0). For maximum gain to occur, source and load impedances should be matched, that is: $Y_S = Y_{11}^*$ and $Y_G = Y_{22}^*$. U can be derived via Y-, Z-, or H-parameters in a similar way [115, 116]. f_{max} can then be calculated according to (4.21). Similarly to f_T anf h_{21}, f_{max} is derived by extrapolating U in strong inversion and saturation.

$$U = \frac{|Y_{21} - Y_{12}|^2}{4[real(Y_{11})Real(Y_{22}) - Real(Y_{12})Real(Y_{21})]} \tag{4.20}$$

$$f_{max} = \sqrt{U} f_{spot} \tag{4.21}$$

4.3.3 FoM for LNA Design

The transconductance to drain current ratio G_m/I_D represents the current efficiency of a transistor, i.e. the transconductance you get for a specific current. G_m/I_D is useful in terms of analog design, e.g. in operational transconductance amplifiers (OTA). The normalized current efficiency can be expressed as a function of inversion coefficient through (4.22), where n is the slope factor. Current efficiency is maximum in weak inversion and equal to 1/n, whereas it reduces as the gate-source voltage increases.

$$\frac{G_m}{I_D} = \frac{2}{n(\sqrt{4IC+1}+1)} \tag{4.22}$$

Shameli et al. [117] combined G_m/I_D with speed, introducing a unique FoM for MOS transistors. This FoM is called transconductance frequency product, $TFP = (G_m/I_D)f_T$, and is used to optimize ultra-low power RF circuits. Interestingly, for the 180 nm CMOS process in [117], optimum performance was achieved within moderate inversion region. Based on [117], Taris et al. investigated TFP in terms of RFIC design [60]. They concluded that TFP stands as a FoM for LNA design, incorporating all individual FoM, namely voltage gain, operating frequency, noise and power consumption, in a single one. Their analysis was applied in a common-source LNA, but it can also be extended to cascode topology. Voltage gain G_v is found to be proportional to $f_T/(R_S f)$ [118], where R_S is the input impedance, typically equal to 50 Ω, and f is the operating frequency. Power consumption, P_{cons}, is equal to $V_{DD}I_D$. Minimum noise factor of a MOS transistor is proportional to $1 + \frac{1}{G_m R_S}$. Therefore following (4.23), TFP proves to be an easy and representative way to characterize the overall performance of a CS LNA. Recently, measurements on TFP were presented down to 40 nm with respect to inversion coefficient and juxtaposed with BSIM6 [113, 119]. In [120] the effect of velocity saturation on TFP was introduced via analytical equations, based on the charge-based EKV3 model. In this work, TFP is further investigated down to 22 nm.

$$FoM_{LNA} = \frac{G_v f}{(F-1)P_{cons}} \propto \frac{G_m}{I_D} f_T \tag{4.23}$$

Song et al proposed an even simpler way to describe the overall LNA performance [121]. Based on the cascode topology they analyzed the FoM expressed in (4.23), without including the frequency of operation and ended up to (4.24). G_P in (4.24) is the power gain which is proportional to G_m^2. The noise factor is found

to vary with I_D/G_m^2. The important thing with this simpler expression is that DC measurements are sufficient to describe the RF performance of an LNA, via the ratio G_m^2/I_D. Previous work has only shown the width dependence on G_m^2/I_D, with respect to gate-source voltage V_{GS}. The length dependence of the FoM, versus inversion coefficient, as well as the comparison of this FoM to TFP will be shown in Section 1.5.3. G_V and G_P in (4.23), and (4.24) are the same when the LNA is matched to 50 Ω, at its input and output.

$$FoM_{LNA} = \frac{G_P}{(F-1)P_{cons}} \propto (\frac{G_m^2}{I_D})^2 \tag{4.24}$$

4.3.4 Gain Transconductance Frequency Product

Additionally to TFP, which represents a trade-off between power and bandwidth, another FoM was recently proposed [9]. Gain transconductance frequency product (GTFP) is defined as the product of TFP with intrinsic voltage gain: $GTFP = (G_m/I_D)(G_m/G_{ds})f_T$. GTFP can be mainly used as a performance metric among different devices [10] as well as a FoM for OTA design. The decrease in G_m/G_{ds} with technology scaling, affects the GTFP value which increases with a slower rate, compared to TFP with technology scaling [8]. However, its optimum value experiences the same behavior as TFP, progressively moving towards lower inversion levels.

4.4 Nonlinearity

In a transceiver chain, there are circuits operating in small-signal (LNA), while others operate under large-signal excitation (e.g. VCO, power amplifiers etc.). Therefore it is useful to identify the sources of non-linearities in the MOS device. Non-linearities can be described by harmonics and intermodulation. In each case, different metrics are used to describe the performance of a circuit.

In the case of a single signal, the 1 dB compression point is usually used as a FoM. An amplifier maintains a constant gain for low-level input signals. However, at higher input levels, the amplifier goes into saturation and its gain decreases. The 1 dB compression point (P_{1dB}) indicates the power level that causes the gain to drop by 1 dB from its small signal value.

When two interferers (at frequencies ω_1 and ω_2) accompany the desired signal, the output exhibits components that arise from mixing of the two components. A measure of intermodulation is the third intercept point. It is the point where the amplitude of the third order intermodulation products (at $2\omega_1$-ω_2, $2\omega_2$-ω_1) becomes equal to that of the fundamental tones at the output. The input and output third intercept points are used for receivers and transmitters, respectively.

In a MOSFET, the nonlinearities mainly arise from harmonics [122–124] induced by higher order derivatives of the channel current I_D with respect to V_{GS},

especially by the 3rd order derivative G_{m3}, calculated via (4.25). It has been shown that non-linearities due to the non-linear I_D-V_{DS} characteristic slightly contribute to the total non-linearities of the device [125]. Extrinsic components, such as capacitances are non-linear as well, since they are bias dependent. However, keeping all extrinsic components constant does not significantly change the model results [4]. Non-linearity analysis in MOSTs is usually expressed in terms of 3rd order intermodulation input intercept points P_{IP3} and V_{IP3}, as well as the 1dB compression point. P_{IP3}, V_{IP3} and P_{1dB} are derived via (4.26), (4.27), and (4.28) and have been extensively investigated in literature [126–131]. R_S is the input impedance, typically equal to 50 Ω.

$$G_m = \frac{\partial I_D}{\partial V_{GS}},\ G_{m2} = \frac{\partial^2 I_D}{\partial V_{GS}^2},\ G_{m3} = \frac{\partial^3 I_D}{\partial V_{GS}^3} \tag{4.25}$$

$$P_{IP3} = \left| \frac{2G_m}{3G_{m3}R_S} \right| \tag{4.26}$$

$$V_{IP3} = \sqrt{\frac{24G_m}{G_{m3}}} \tag{4.27}$$

$$P_{1dB} = \left| \frac{G_m}{13.8G_{m3}R_S} \right| \tag{4.28}$$

In general, with increasing gate bias, P_{IP3} and V_{IP3} increase to a maximum value followed by a local minimum [123]. With technology scaling, contradicting results have been observed even from the same groups. Specifically, in [123], V_{IP3} is shown to obtain its optimum value at lower overdrive voltages with channel length scaling. However, in [132], the same group reports that maximum V_{IP3} is achieved at higher current densities, and thus inversion levels, with technology scaling. At high drain current density, velocity saturation and series resistance dominate V_{IP3}[123, 132].

4.5 Results and Discussion

A compact model should predict the electrical behavior of MOS devices over a large range of frequency, geometry, and bias. Former work showed the EKV3 model's validity up to 30 GHz, for 110 [116] and 180 nm [115] CMOS processes. In this thesis, the EKV3 compact model is presented for RF FoM essential for RFIC design, with respect to inversion level. This facilitates a comparison of devices of different geometry, channel types, and over many technology generations. For this purpose, multifinger n- and p-MOS devices of several geometries have been measured over a wide range of bias points. For analog/RF applications, intrinsic gain G_m/G_{DS}, gate transconducance G_m and output conductance G_{DS}, transconductance efficiency G_m/I_D, intrinsic gate and Miller capacitances C_{gint} and C_{Miller} , transit frequency f_T ,

and maximum oscillation frequency f_{max} are of utmost importance for circuit performance. The product $(G_m/I_D)f_T$ (TFP) and f_{max} are considered important FoM for the RF performance of devices. The limitation of f_{max} is in turn critically dependent on C_{gint}/C_{Miller} and G_m/G_{DS} [133]. Recently, the GTFP $(G_m/G_{ds})(G_m/I_D)f_T$ was proposed [9, 10] as a performance metric. GTFP is easy to evaluate and combines the HF capability of the device with transconductance efficiency and intrinsic gain. To study the scaling effect on these performance characteristics, CMOS technology nodes covering 180, 90, 45, and 22 nm were simulated using the ATLAS simulator and modeled with EKV3. For the 90 nm case used in this paper, measured data are presented as well. The FoMs are represented with respect to inversion coefficient, defined as $IC = I_D/I_{spec}$, providing a common measure of comparison across all channel dimensions and over technology nodes.

The models activated in the TCAD simulation comprise inversion layer Lombardi CVT mobility model with doping and temperature dependence. Shockley–Read–Hall, Auger recombination model for minority carrier recombination, and Fermi–Dirac statistics are used. Inversion layer quantum effects are considered. The physical parameters for TCAD simulations for different technology nodes are presented in Table 4.1. TCAD simulations and measurements of the 90 nm CMOS process have been verified with experimental results from other researchers [89, 134], as well as ITRS 2011 data [135]. This is shown in Figure 4.3 and Figure 4.4 for f_T and f_{max}, respectively. A good agreement is observed among different measurements. The trend for f_T, even for the shortest devices, remains the same, i.e. it increases with the inverse of channel length.

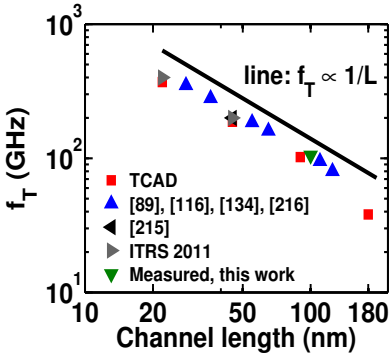


Figure 4.3: TCAD simulations and measurements for transit frequency f_T.

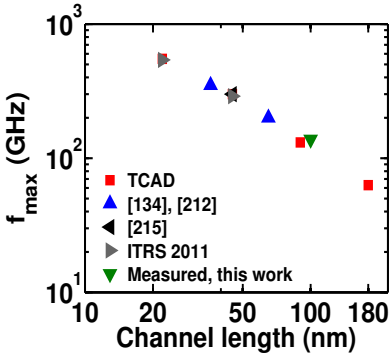


Figure 4.4: TCAD simulations and measurements for maximum oscillation frequency f_{max}.

Parameter	Value			
Channel length (nm)	22	45	90	180
EOT (nm)	1.1	1.3	2.1	3.1
Substrate doping (cm^{-3})	2.5×10^{18}	1.25×10^{18}	7×10^{17}	5×10^{17}
Junction depth (nm)	10	15	30	50
Slope factor	1.6	1.4	1.31	1.27
Technology current I_0 (nA)	574	549	461	439

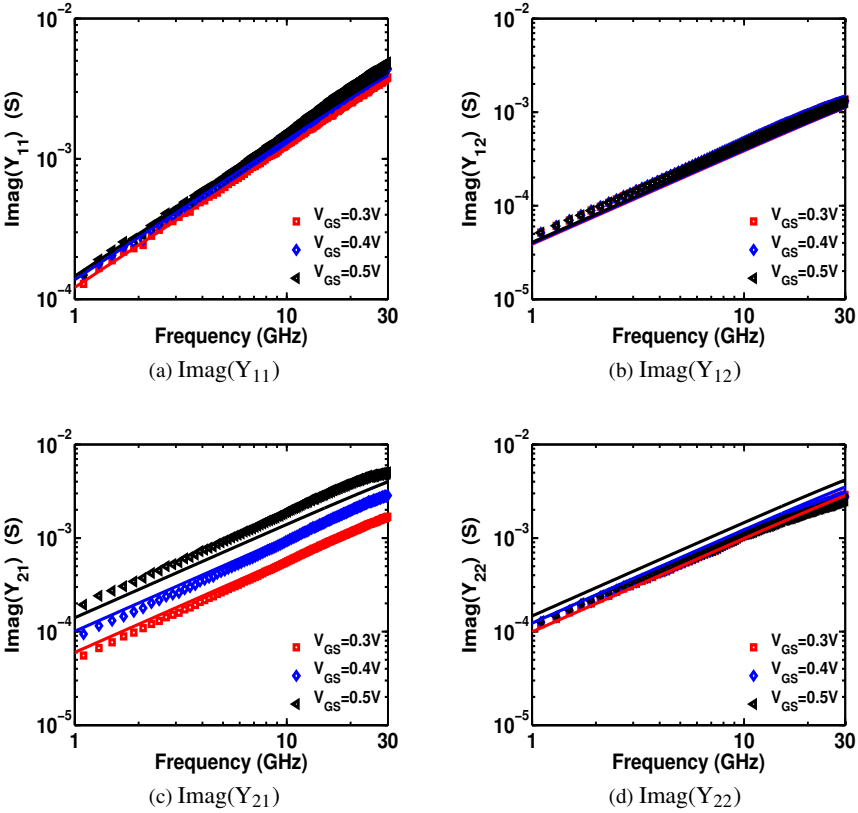
Table 4.1: Parameters for n-MOSFETs simulated in this work.

4.5.1 Parasitic Resistances and Overlap Capacitances

In short channel MOSFETs the extrinsic components greatly affect the device performance. Therefore it is prerequisite to correctly model parasitic resistances and capacitances. Since extrinsic components result from Y-parameters, it is imperative that Y-parameters should also be accurately modeled. Figure 4.5 and Figure 4.6 represent measured and modeled data for Y-parameters, in terms of their real and imaginary parts, respectively. For convenience, a n-MOS device of L = 100 nm and W = 10 x 2 um is shown here, biased at V_{DS} = 1 V. Three bias points are presented, namely V_{GS} values ranging from 0.3 - 0.5 V. This corresponds to an inversion level ranging from moderate, which is the region of interest to us, to strong inversion. The EKV3 model satisfactorily covers the frequency response for a wide range of frequencies, from 1 - 30 GHz. Gate resistance, R_G, has a great influence on the real part of Y_{21} and Y_{22}, especially at high frequencies. This is described in (4.11), (4.12) and is represented in Figure 4.6c and Figure 4.6d. The same holds for parasitic capacitance C_{GD}. Both R_G and C_{GD} are extracted in strong inversion

and saturation, according to [136] and are depicted in Figure 4.7 versus frequency from 1 - 30 GHz. The total gate capacitance C_G is also presented in the same Figure. Overlap capacitance C_{GS} can be easily calculated by a simple subtraction, via (4.13), since C_{GB} is negligible in strong inversion. Figure 4.7 verifies that the plotted extrinsic components are frequency independent and the extraction method is accurate and reliable.

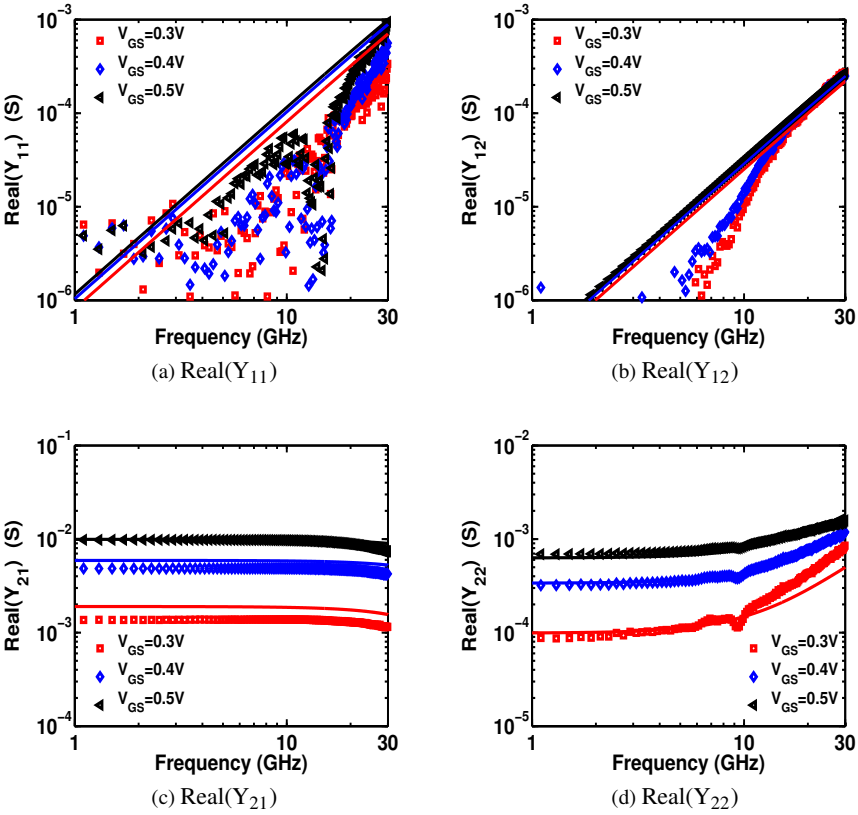
A good approximation of the DC values of gate transconductance (G_m) and output conductance (G_{ds}), for every bias point, can be achieved through (4.11) and (4.12), for $\omega^2 = 0$. These values coincide to the values extracted from relatively low frequencies, at which the real part of Y_{21} and Y_{22} remain constant.



(a) Imag(Y_{11}) (b) Imag(Y_{12})

(c) Imag(Y_{21}) (d) Imag(Y_{22})

Figure 4.5: Imaginary parts of Y-parameters vs. frequency for a n-MOS device of L=100 nm, W=10x2 um, biased at V_{DS}=1V.



(a) Real(Y_{11}) (b) Real(Y_{12})

(c) Real(Y_{21}) (d) Real(Y_{22})

Figure 4.6: Real parts of Y-parameters vs. frequency for a n-MOS device of L=100 nm, W=10x2 um, biased at V_{DS}=1V.

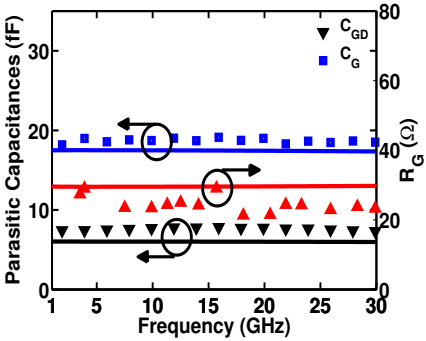


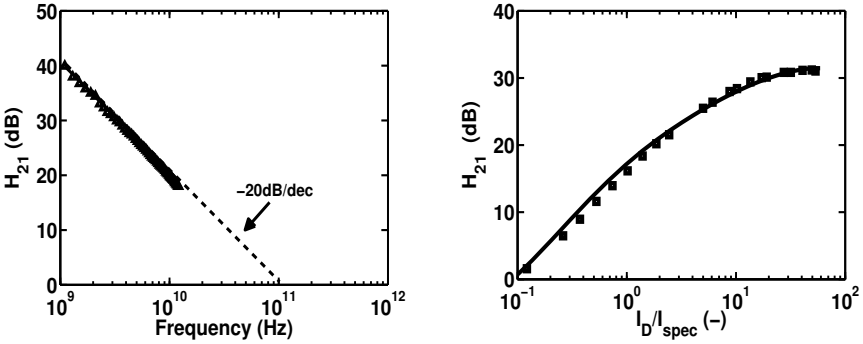
Figure 4.7: Gate resistance and parasitic capacitances vs. frequency for a n-MOS device of L=100 nm and W=10x2 um, biased at V_{DS}=V_{GS}=1V.

4.5.2 Transit Frequency and Maximum Oscillation Frequency

Transit frequency is an easy way to describe the RF performance of a MOS device. A high f_T is desirable, since it represents the frequency limit up to which the transistor can operate as an amplifier. f_T is also related to noise, via noise factor [4]. Generally, the higher the f_T, the lower the noise factor. In the present section, transit frequency is presented versus bias and channel length for the measured as well as the simulated devices. Figure 4.8a, demonstrates the direct relation between current gain h_{21} and f_T. The extrapolated value of h_{21} in which it crosses the zero dB point corresponds to the f_T of the device. This holds when the device is biased in strong inversion and saturation, where the slope of the h_{21} is -20 dB/dec. Indeed, as shown in Figure 4.9, the f_T of the measured n-MOS device at V_{DS} = 1 V is very close to the value obtained by the linear extrapolation of h_{21}. In Figure 4.9 f_T is plotted for several V_{DS} values, including the linear region. h_{21} is also plotted versus inversion coefficient in Figure 4.8b. In order to study the behavior of f_T over different technology nodes, TCAD simulated data are used together with measured data. TCAD data include CMOS technologies of L=180, 90, 45 and 22 nm. Figure 4.10, shows that for the shortest simulated n-MOS device of L = 22 nm, an f_T of about 400 GHz is achieved, demonstrating the extensive possibilities offered by such CMOS technologies in terms of analog/RF design. Moreover maximum f_T values are obtained at lower IC values with channel length scaling.

The same trend is observed for the maximum oscillation frequency, presented in Figure 4.12. Unilateral gain is shown in Figure 4.11a and Figure 4.11b versus frequency and IC, respectively. For the measured device of L=100 nm, f_{max} is approximately equal to 120 GHz, whereas for the the 22 nm channel length device,

f_{max} approaches 600 GHz. The scalability and high accuracy of the EKV3 model is proven in all cases since it efficiently describes all FoM over frequency and bias domains, for all investigated channel lengths. TCAD simulated data are validated by comparing the 90 nm TCAD data with the measurement results of the 90 nm CMOS process. These are shown to be in close proximity.



(a) h_{21} vs. frequency (b) h_{21} vs inversion coefficient

Figure 4.8: h_{21} for a n-MOS device of L=100 nm and W=10x2 um, biased at V_{DS}=1 V.

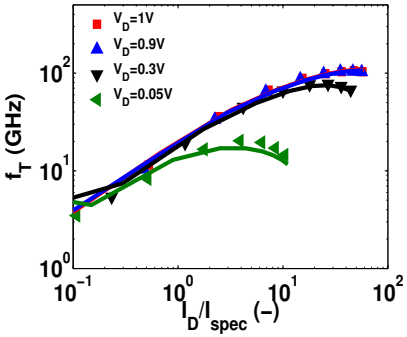
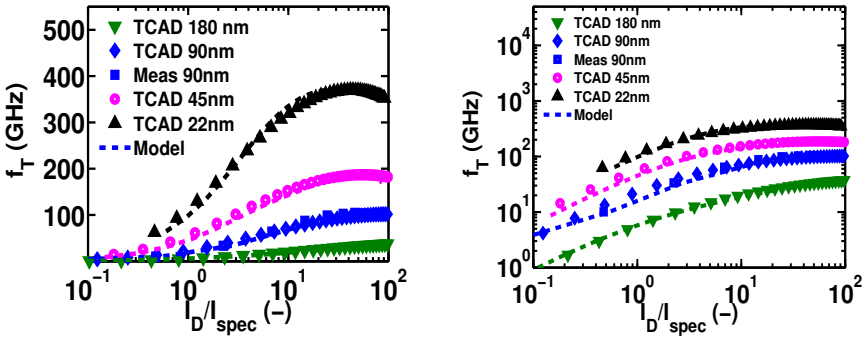
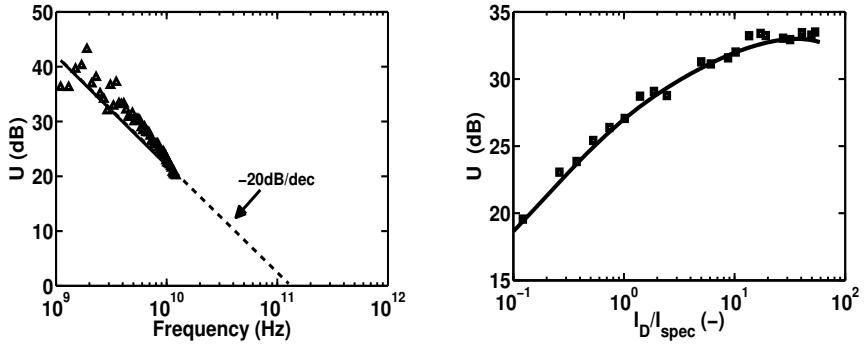


Figure 4.9: f_T vs. inversion coefficient for a n-MOS device of L=100 nm and W=10x2 um, biased at different V_{DS}.



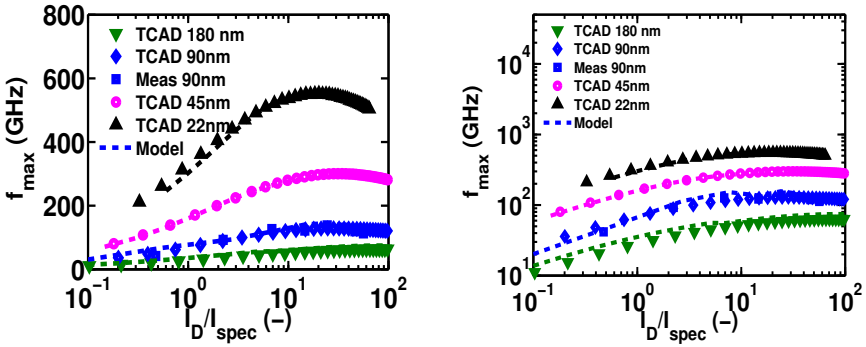
(a) f_T in semilog axis. (b) f_T in log-log axis

Figure 4.10: f_T vs. inversion coefficient for n-MOS device of several technology nodes with W=10x2 um, biased at different V_{DS}= 1 V.



(a) U vs. frequency (b) U vs. inversion coefficient

Figure 4.11: Unilateral gain for a n-MOS device of L=100 nm and W=10x2 um, biased at V_{DS}=1 V.



(a) f_{max} in semilog axis

(b) f_{max} in log-log axis

Figure 4.12: f_{max} vs. inversion coefficient for n-MOS devices of several technology nodes with W=10x2 um, biased at different V_{DS}= 1 V.

4.5.3 FoM for LNA Design and GTFP

Several techniques have been introduced for optimizing the performance of LNAs. Depending on the specifications, the LNA circuit can be designed for noise matching, input and noise matching, or input and noise matching while taking into account power consumption as well. Every optimization scheme experiences certain disadvantages, already explained in Chapter 2. In this thesis, we show that an LNA circuit can be simply optimized by properly choosing its operation point within the moderate inversion region. This is shown by inspecting the behavior of a representative FoM, namely the TFP. TFP is easy to calculate and describes the overall performance of a CS LNA, in terms of noise, power, operation frequency and gain. TFP is firstly investigated in the context of available measured n-MOS devices of the 90 nm process. This is shown in Figure 4.13, where TFP is plotted versus inversion coefficient for devices with channel length ranging from 240 to 100 nm, and W=40x2 um, biased at V_{DS}=1 V. It is shown that within the same technology node, maximum TFP appears in M.I. region and is progressively moving from higher to lower inversion levels, with channel length scaling. For the shortest device of L=100 nm, this practically means that a CS LNA biased with a current of 2.7 mA and thus a power consumption of 2.7 mW can be achieved at a frequency of 10 GHz. The shortest available p-MOS device has a much lower TFP, due to its lower cut-off frequency. This value is achieved at higher inversion levels, specifically in the vicinity of M.I. and S.I. (Figure 4.14). TFP has also been extracted for different technology nodes and is shown in Figure 4.16. Transconductance efficiency, used in the TFP calcula-

tion, is presented in its normalized form in Figure 4.15. TFP with respect to inversion coefficient is shown in Figure 4.16. Peak values are observed within the higher decade of moderate inversion; the optimum operating point is progressively shifted toward the center of M.I. (IC = 1). This is of major importance as the demand for lower supply voltages as well as lower power consumption becomes more stringent. The ratio of G_m^2/I_D which includes all individual FoM but the operation frequency, experiences the same behavior with TFP: that is, its peak value is obtained close to the center of M.I. with channel length scaling. This is depicted in both Figure 4.17 and Figure 4.18 for measured and simulated data, respectively. This also proves that M.I. is ideal for realizing optimum LNA implementations.

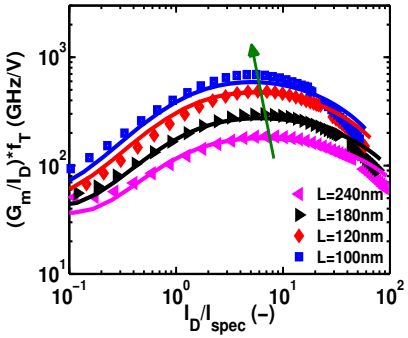


Figure 4.13: TFP vs. inversion coefficient for n-MOS devices with channel length ranging from 240 nm to 100 nm, in saturation.

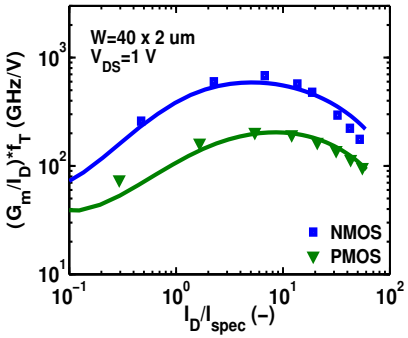


Figure 4.14: TFP vs. inversion coefficient for a n-MOS and a p-MOS device of L=100 nm, in saturation.

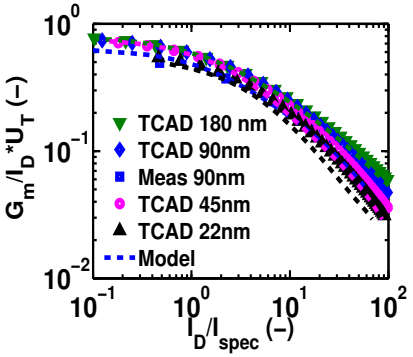


Figure 4.15: Normalized transconductance efficiency: TCAD data, and EKV3 model for minimum length n-MOS devices of 180-, 90-, 45-, and 22-nm CMOS technologies, and measured data (for 90-nm minimum device), with channel width W = 10 × 2 um, biased at V_{DS} = 0.9 V.

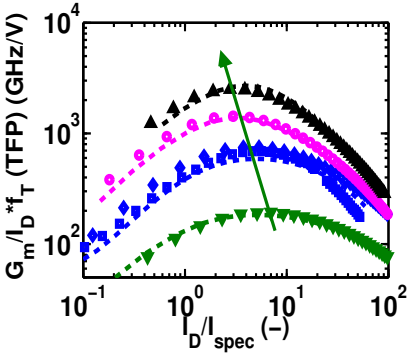


Figure 4.16: TFP vs. inversion coefficient: TCAD data, and EKV3 model for minimum length n-MOS devices of 180-, 90-, 45-, and 22-nm CMOS technologies, and measured data (for 90-nm minimum device), with channel width W = 10 × 2 um, biased at V_{DS} = 0.9 V.

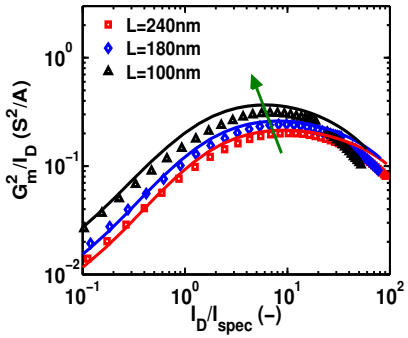


Figure 4.17: G_m^2/I_D vs. inversion coefficient: Measured data and model for n-MOS devices with channel length of 240-, 180-, and 90-nm and W = 40 × 2 um, biased at V_{DS} = 1 V.

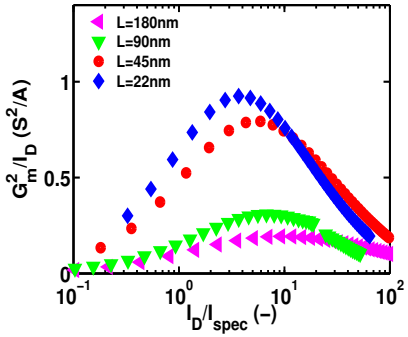


Figure 4.18: G_m^2/I_D vs. inversion coefficient: TCAD data for minimum length n-MOS devices of 180-, 90-, 45-, and 22-nm CMOS technologies, with channel width W = 10 × 2 um, biased at V_{DS} = 0.9 V.

While TFP reflects the increase in f_T when scaling down the technology, the GTFP - which in terms of analog design could be useful in operational transconductance amplifiers - of 45 and 22 nm nodes remains almost the same, as the degradation of G_m/G_{ds} in the latter almost outweighs the increase in f_T (Figure 4.19). This is evident in Figure 4.20, where maximum values of TFP and GTFP are plotted for all technology nodes with respect to effective gate voltage V_{EFF}. IC and V_{EFF} are related via (4.29).

$$IC = [\ln(1 + e^{\frac{V_{EFF}}{2nU_T}})]^2 \tag{4.29}$$

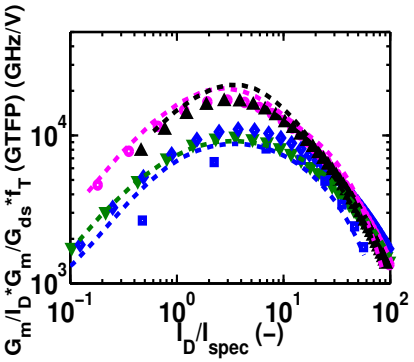


Figure 4.19: GTFP vs. inversion coefficient: TCAD data, and EKV3 model for minimum length n-MOS devices of 180-, 90-, 45-, and 22-nm CMOS technologies, and measured data (for 90-nm minimum device), with channel width W = 10 × 2 um, biased at V_{DS} = 0.9 V.

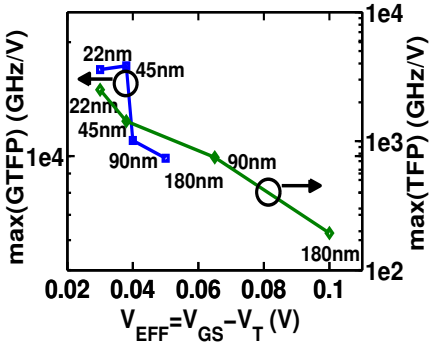


Figure 4.20: Maximum of TFP and GTFP vs. effective gate voltage: TCAD data, and EKV3 model for minimum length n-MOS devices of 180-, 90-, 45-, and 22-nm CMOS technologies, and measured data (for 90-nm minimum device), with channel width W = 10 × 2 um, biased at V_{DS} = 0.9 V.

4.5.4 Third Order Intercept Points and 1 db Compression Point

Linearity is not the main concern in an LNA circuit. However, it is desirable for obtaining its optimum overall performance. Moreover, in the last stages of a transceiver chain (e.g. mixer, variable gain amplifier, power amplifier), it becomes of major importance. Therefore, it is useful to study its behavior with bias and scaling, through distortion FoM. In general, linearity FoMs are exported from DC measurements. However it is also useful to study these metrics at high frequency, since this would be more meaningful in terms of RFIC design. Therefore RF measurements were performed for several V_{DS} and V_{GS} values and linearity metrics were extracted at 1.1 GHz. G_m, G_{m2} and G_{m3} measurements as well as EKV3 simulation data are shown in Figure 4.21 versus IC for the shorter device of L=100 nm biased in saturation. P_{IP3} and V_{IP3} are calculated through (4.26) and (4.27) and presented in Figure 4.22 and Figure 4.23, respectively, for the longest and shortest measured devices. The 1 dB compression point is plotted in Figure 4.24, experiencing the same behavior with P_{IP3} and V_{IP3}. P_{1dB} falls approximately 10 dB below the third order intercept point. The model results are in close proximity with measurements and recent published work [123, 124, 137]. Since for low distortion operation all linearity FoMs should be as high as possible, it is worth noticing that moving towards shorter length devices, the peak value of linearity metrics is moving to lower inversion levels, experiencing the same shift as other FoM previously presented, which for L=100 nm approaches the center of M.I. region (IC=1). To validate the trend, non-linearity FoM were also derived for the TCAD simulated data. Maximum values of P_{IP3} and P_{1dB} are also shown to be shifted to lower inversion levels with channel length decrease. This is depicted in Figure 4.25 and Figure 4.26. For the TCAD case, P_{1P3} and P_{1dB} have been extracted from DC rather than data, but this has practically no impact on the results. The extracted distortion behavior of CMOS actually means that the trade-off between power and linearity can become more relaxed with technology scaling.

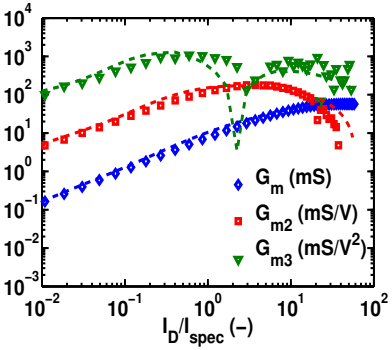


Figure 4.21: G_m, G_{m2}, and G_{m3} vs. inversion coefficient for a n-MOS device of L=100 nm and W=40x2 um, biased at V_{DS}=1 V, extracted at f=1.1 GHz.

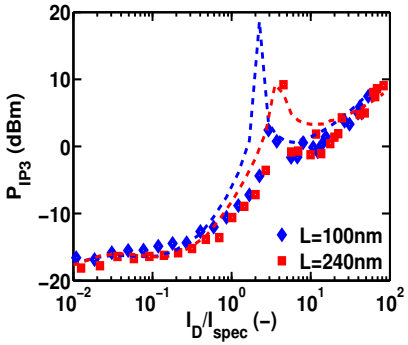


Figure 4.22: P_{IP3} vs. inversion coefficient for n-MOS devices ofW=40x2 um, biased at V_{DS}=1 V, extracted at f=1.1 GHz.

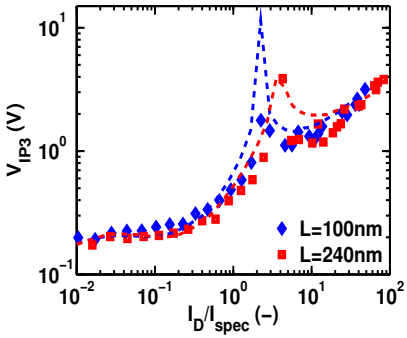


Figure 4.23: V_{IP3} vs. inversion coefficient for n-MOS devices of W=40x2 um, biased at V_{DS}=1 V, extracted at f=1.1 GHz.

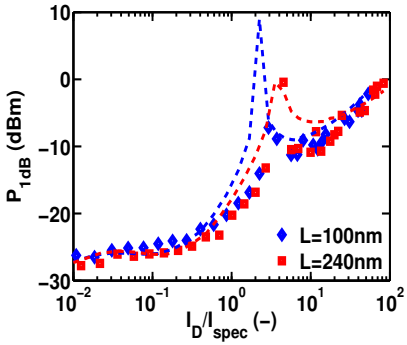


Figure 4.24: P_{1dB} vs. inversion coefficient for n-MOS devices of W=40x2 um, biased at V_{DS}=1 V, extracted at f=1.1 GHz.

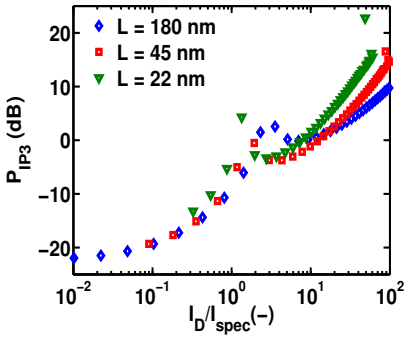


Figure 4.25: P_{IP3} vs. inversion coefficient for n-MOS devices biased at V_{DS}=0.9 V.

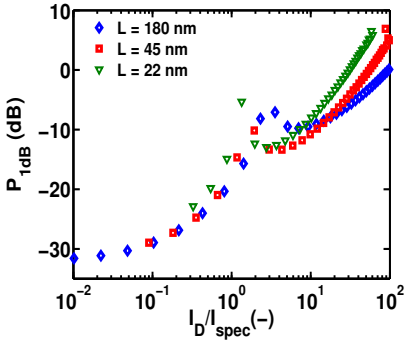


Figure 4.26: P_{1dB} vs. inversion coefficient for n-MOS devices biased at V_{DS}=0.9 V.

4.6 Contribution

A lot of research effort has been lately given on exploring the possibilities of high performance RFICs, while keeping the power consumption low [113, 117, 119]. This effort is driven by the increasing demand for low-power RFICs. In this chapter we demonstrate that moderate inversion is the proper operation region for circuit biasing. This is shown through several design-oriented FoM, which are explored over many CMOS generations. In particular, extremely high f_T and f_{max} values are obtained at lower inversion levels, with technology scaling. Optimum LNA performance has been studied through simple and qualitative design metrics, such as TFP and G_m^2/I_D. Both are presented for the first time down to 22 nm and confirm that it is feasible to combine high performance with power minimization. Both FoM obtain their maximum values within moderate inversion and specifically, at IC values close to 3, for the 22 nm n-MOS device. GTFP, which is useful for comparing different devices, is also shown to have a similar behavior. Non-linearities, for which contradicting results have been reported regarding their trend with bias and scaling, are also presented for the fabricated 90 nm CMOS process as well as the TCAD data. All distortion FoM are shown to obtain their optimum values within moderate inversion. The EKV3 model accurately describes this behavior with scaling and biasing, validating both measured and simulated data.

In conclusion, all investigated FoM show that optimum analog/RF performance is gradually shifted toward lower levels of MI, closer to around-threshold operation, as planar bulk CMOS scales toward the 20 nm regime.

Chapter 5

Noise in MOS Devices

The dynamic range of a receiver is limited by its sensitivity and the maximum signal strength allowable at its input. Sensitivity is related to noise, which determines the minimum signal that the receiver can detect. Due to its random nature, noise is characterized by its average power. Thus its power spectral density will be described in the following section. Moreover, noise in MOS devices will be presented in detail and the derivation of channel thermal noise as well as the impact of short-channel effects on it will be shown. The extraction of noise parameters will be addressed in the context of two-port network theory and noise parameters having circuit implications will be introduced. Next, modeling issues will be covered to validate noise measurements and display the trend of noise characteristics with inversion level and length scaling, providing guidelines for RFIC design.

5.1 Noise as a Random Process

Noise is a random process and hence even if its past values are known, its instantaneous value cannot be predicted. Let's consider the current of a resistor of value R=1 kΩ, biased by a 1 V voltage source. Ideally, a constant current of 1 mA will flow across the resistor independent of time. However, in a physical resistor the current experiences thermal agitation, due to the random collision of electrons with lattice atoms. The noise current is depicted in Figure 5.1. By observing the noise for a long time, a statistical model can be built from which the average power of noise can be extracted. This is defined in (5.1), where n(t) represents the noise waveform. Noise consists of different frequencies and thus a large time is required to obtain several cycles of the lowest frequency [138]. For example, the noise of human voices may span from 20 Hz - 20 kHz. In such a case, for capturing 10 cycles of 20 Hz, the time period should be equal to 0.5 s. From the frequency perspective, spectrum is used to characterize the average power the signal carries at every frequency. Spectrum is

also called power spectral density (PSD) and for the rest of the text the PSD term will be used. For n(t), its PSD, $S_n(f)$, is defined as the average power the noise waveform carries in a bandwidth (BW) of 1 Hz, around frequency f [139]. To obtain the noise PSD for frequency f_1, the noise waveform is passed trough a band-pass filter with a BW of 1 Hz, centered around f_1, and then its output is squared and averaged to obtain $S_n(f_1)$. The process is repeated for all frequencies resulting in the PSD of n(t), $S_n(f)$. The most common type of noise PSD is the white noise, where the frequency response of PSD is flat, meaning it has the same value for all frequencies, resulting in a spectrum similar to white light [139]. It is important to mention that when two noise sources are uncorrelated, the average power of the total noise is derived by summing the average power of each.

$$P_{av} = \lim_{T\to\infty} \frac{1}{T} \int_0^T n^2(t)dt \tag{5.1}$$

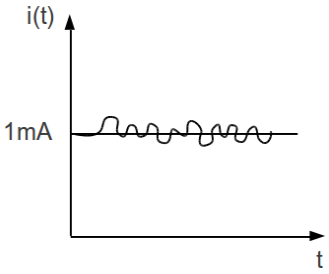


Figure 5.1: Noise current generated in a resistor.

Thermal noise in conductors was first measured by J. B. Johnson, while Nyquist was the first to derive an expression for it based on Johnson's measurements. This explains why thermal noise is also called Johnson or Nyquist noise. Van der Ziel extensively investigated noise using a resistor in parallel with a capacitor to calculate the PSD of thermal noise [140]. For a resistor, thermal noise can be described by the equivalent Thevenin and Norton models. In the first, noise is represented by a noisy voltage source, V_n, in series with a resistor R_1, having a PSD of $S_{v_n}(f) = \overline{V_n^2} = 4kTR_1$. The Norton equivalent consists of a noisy current source, in parallel with R_1, with its PSD given by: $\overline{I_n^2} = \overline{V_n^2}/R_1^2 = 4kT/R_1$. The units for each representation are V^2/Hz and A^2/Hz, respectively. k is the Boltzmann's constant, and T stands for the absolute temperature. The quantity kT is called the available noise power [139] having a dimension of power per unit bandwidth and is independent of resistor's value. As indicated by the above equations, resistor's thermal noise is white. In reality $S_{v_n}(f)$ is flat up to a frequency of 100 THz, dropping at higher frequencies.

5.2 Modeling of Thermal Noise in MOSTs: A Short History

Modeling of thermal noise in solid-state devices has always been an issue of high interest for the microelectronics community. The first to analyze thermal noise in junction field-effect transistors (JFETs) was Van der Ziel [141] in 1962. Subsequently, Jordan and Jordan developed his theory for MOSFETs in [142]. Induced gate noise was also analyzed by Van der Ziel for JFETs in [143] and then by Shozi for MOSFETS [144]. From that point on, several groups were involved in the derivation of compact models for thermal noise in MOSTs. Some of them are summarized in Table 5.1. Ideally, a compact model should provide explicit description of noise at the terminals of the device as a function of device geometry, bias and scaling. Practically, this is a complicated task and this explains the controversies that can be found in literature. For compact modeling of noise in devices, three approaches are usually adopted. An equivalent circuit based-approach, the classical Langevin or Klaassen-Prins approach, and the impedance field method. For long-channel devices all three methods yield the same results. Recently, it has been shown that when mobility degradation is included in noise derivations, the same drain and induced gate noise are extracted, demonstrating the equivalence of all methods [145].

A matter of great discrepancy is the short-channel phenomena that affect thermal noise and the way they impact on it. Abidi firstly reported thermal noise measurements down to 0.7 um in [146] with an excess noise 5 times higher than the respective value for devices of channel length equal to 5 um. He attributed this increase to hot electron effects being in line with Jindal [147, 148]. Hot electron effect has also been adopted by many other groups, indicatively in [149–151]. On the other hand, in [152–155] it is argued that carrier heating plays a significant role in excess noise, due to the opposite impact velocity saturation effect has on it. In these surveys it is shown that only channel length modulation accounts for the excessive noise, especially for channel lengths shorter than 0.5 um [152]. Similar controversies can be found on the noise contribution coming from the velocity saturation region. Based on Abidi's measurements, Triantis et al. [156],[157] and Klein [158] fitted their proposed model reporting that excess noise was due to both the non-saturated and the velocity saturated region. Even though this approach is also used in [159], numerous recent publications have experimentally and analytically proven that only the non-saturated region contributes to channel thermal noise [5, 145, 152, 160–163]. Moreover in [156, 158], the drain-source conductance is assumed to be constant along the channel, making the derivation of channel thermal noise questionable. The measurements in [146] give a greatly overestimated excess thermal noise, and hence modeling approaches based on [146] have to be revisited. In [150], the effective mobility of carriers is mistakenly assumed to be same in both regions. Han et al. [164] consider the channel field effect on mobility. However they questionably use Einstein equation in MOST channel. It is due to the above-mentioned controversies that

excess noise parameters used to characterize thermal noise, experience variations in some cases, e.g. see in [146], and [165–167], though they generally are in line.

Thermal noise was first analyzed at higher frequencies in 1967 by Klaassen [168]. Due to the increased usage of MOSTs in mm-wave applications [169], at frequencies higher than 100 GHz, it is imperative to predict noise behavior up to this frequency range. However, due to measurement limitations, it is extremely difficult to experimentally reach these limits. Recently, thermal noise modeling at frequencies comparable to the device f_T, was presented in [4, 170]. The contribution of extrinsic resistances, particularly the gate resistance, to the the device thermal noise has been qualitatively investigated in [1, 171–173]. An other issue of interest is on the number of noise parameters that need to be measured in order to characterize thermal noise. Despite the classical noise theory [174], according to which four noise parameters are necessary, there are publications reporting that three noise parameters are adequate [175, 176]. However, this is achieved at the expense of certain limitations [177].

The quantitative as well as qualitative work that has been done on noise over the last 30 years has resulted in the incorporation of thermal noise in compact models extensively used by industry (such as PSP, EKV and BSIM), e.g. see in [161, 178–182], validating HF measurements over a large range of technology nodes, down to 40 nm [183]. Despite the great progress on the understanding of thermal noise mechanisms, a lot of issues still remain unclear and need to be clarified. Part of this task will be developed within the next sections.

Group	Noise Model
Tsividis [184]	$S_{id} = \frac{4kT}{L_{eff}^2}\mu_{eff}(-Q_{inv})$
Van der Ziel [140]	$S_{id} = \frac{4kT}{L_{eff}^2 I_{DS}} \int_0^{V_{DS}} (1 + \frac{E}{E_{crit}})^n g^2(V) dV$
Chen - Deen [152]	$S_{id} = \frac{4kT}{L_{eff}^2}\mu_{eff}(-Q_{inv}) + \delta \frac{4kTI_{DS}}{L_{eff}^2 E_{crit}^2} V_{DS}$
Klaassen - Prins [149]	$S_{id} = \frac{4kT}{L_{eff}^2} \int_0^{V_{DS}} g^2(V) dV$
Klein [158]	$S_{id} = 4kT \frac{\mu_{eff} Q_I}{L_{eff}^2} + \frac{8}{3} q v_{sat} \tau_e \frac{I_{DS}}{L_{eff}}$
Scholten [161]	$S_{id} = \frac{1}{L_{eff}^2 I_{DS}} \int_0^{V_{DSat}} 4kT_e(x) g^2(V) dV$

Table 5.1: Summary of the channel noise equations of several publications.

5.3 Modeling of Thermal Noise in MOSTs: The EKV3 Model

Noise in MOS devices can be separated into flicker (or 1/f) and thermal noise. The frequency point where the two noise sources meet, having equal PSDs is called corner frequency and falls in the range of tens or even hundreds of MHz in modern CMOS technologies [139]. Thermal noise in MOSTs is due to local random fluctuations of the carrier velocity, which can be modeled by adding a random current to the DC local current [4]. These fluctuations are transferred to the device terminals resulting in fluctuations in voltages and currents around the device DC operating point. For the drain current fluctuations, its noise PSD can be derived by adding the PSDs of each of the local current sources within the channel. This can only be done by assuming linear analysis so that superposition can be applied. A general modeling approach is shown in Figure 5.2, where a local noisy source exists between x and x+Δx from the source end and L-x and L-(x+Δx) from the drain end. Assuming a finite equivalent resistance ΔR, this region can be represented by a noisy current source, δI_n in parallel with ΔR (Norton equivalent), with a PSD of $S_{\delta I_n^2}$. The transistor can be split into two transistors T1 and T2, at the source and drain ends, with channel lengths equal to x and L-x, respectively. Since the voltage fluctuation on ΔR is small enough compared to thermal voltage U_T, small-signal analysis can be used in noise derivation, according to which, T1 and T2 can be replaced by conductances G_1 and G_2 equal to: $G_1 = \frac{1}{G_{md1}}$ and $G_2 = \frac{1}{G_{ms2}}$. The total channel conductance is then calculated by summing the two series conductances as $\frac{1}{G_{ch}} = \frac{1}{G_1} + \frac{1}{G_2}$.

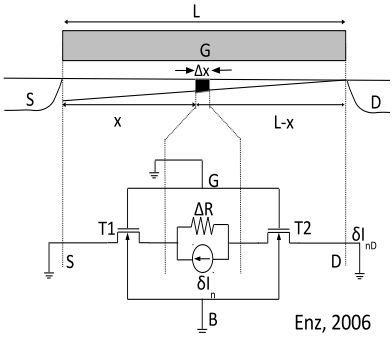


Figure 5.2: Local noise source and its equivalent model.

The drain fluctuation, δI_{nD}, and its corresponding PSD, $S_{\delta In_D^2}$, due to the local noisy current source δI_n, are calculated according to (5.2) and (5.3), respectively. $S_{\delta In_D^2}$ is a function of frequency and distance along the channel. The PSD of drain

current due to all local noisy sources within the channel, results by adding the contributions of the individual noise sources, assuming they are uncorrelated. Hence, the overall noise drain current PSD, $S_{\Delta In_D^2}$, is calculated by integrating (5.3), from x=0 to x=L. The term Δx is introduced to represent the contribution of δI_n per unit length. $S_{\Delta In_D^2}$ in (5.4) is independent of the position x, since it is the interval along the channel, solely depending on frequency [4, 5].

$$\delta I_{nD} = G_{ch} \Delta R \delta I_n \tag{5.2}$$

$$S_{\delta In_D^2}(\omega, x) = G_{ch}^2 \Delta R^2 S_{\delta I_n^2}(\omega, x) \tag{5.3}$$

$$S_{\Delta In_D^2}(\omega) = \int_0^L G_{ch}^2 \Delta R^2 \frac{S_{\delta I_n^2}(\omega, x)}{\Delta x} dx \tag{5.4}$$

The simple two-transistor approach described above has been adopted for frequencies well below the transit frequency of the device in our case (up to 24 GHz, while f_T is approximately 100 GHz). However it is also applicable for frequencies well beyond f_T as has been shown in [170, 185–188], in which the non-quasi-static (NQS) model is derived using the same two-transistor approach. However, the equivalent NQS circuit is much more complicated in this case [4].

5.3.1 Thermal Noise of Long Channel Devices

For a long channel approximation of $S_{\Delta In_D^2}$ carrier mobility, μ, is assumed to have a constant value, which is not the case in short channel devices. Therefore, channel conductance at point x is the derivative of drain current, I_D, with respect to voltage V, $G_{ch} = \frac{dI_D}{dV}$. Drain current is equal to: $I_D = \mu W(-Q_i)\frac{dV}{dx}$ [189, 190], where W is the channel width, and Q_i is the inversion charge. Thus:

$$G_{ch} = \frac{dI_D}{dV} = \mu(-Q_i)\frac{W}{L} = G_{spec} q_i \tag{5.5}$$

, where $G_{spec} = \frac{I_{spec}}{U_T} = 2n\beta U_T$. I_{spec} is the specific current, n is the slope factor and $\beta = \mu C_{ox}\frac{W}{L}$ is the transconductance function or transfer parameters of the transistor, depending on the device dimensions. q_i is the normalized inversion charge, resulting by dividing Q_i by the specific charge density Q_{spec}, which is: $Q_{spec} = -2nC_{ox}U_T$ [4, 190]. Resistance ΔR is equal to:

$$\Delta R = \frac{\Delta V}{I_D} = \frac{\Delta x}{W\mu(-Q_i)} \tag{5.6}$$

From (5.3), (5.5), (5.6), the PSD of the drain current fluctuations due to δI_n is calculated via (5.7). The PSD of noise drain current due to all local noise sources is then

given by (5.8).

$$S_{\delta I_{nD}^2}(\omega,x) = G_{ch}^2(x)\Delta R^2(x) S_{\delta I_n^2}(\omega,x) \tag{5.7}$$

$$S_{\Delta I_{nD}^2}(\omega) = \int_0^L (\frac{\Delta x}{L})^2 \frac{S_{\delta I_n^2(\omega,x)}}{\Delta x} dx = \frac{1}{L^2}\int_o^L \Delta x S_{\delta I_n^2}(\omega,x) dx \tag{5.8}$$

In general, the PSD of drain current due to all local noise sources along the channel can be written according to (5.9). G_{nD} stands for the thermal noise conductance and is significant in terms of circuit design, as we will show in the next sections.

$$S_{\Delta I_{nD}^2} = 4kTG_{nD} \tag{5.9}$$

To derive a long channel expression for G_{nD} we first write the PSD of each δI_n using (5.6) as:

$$S_{\delta I_n^2} = \frac{4kT}{\Delta R} = 4kT\frac{W\mu(-Q_i)}{\Delta x} \tag{5.10}$$

Then, according to (5.10), (5.8) becomes:

$$\begin{aligned} S_{\Delta I_{nD}^2}(\omega) = \frac{1}{L^2}\int_o^L \Delta x S_{\delta I_n^2}(\omega,x) dx = \frac{1}{L^2}\int_o^L \Delta x 4kT\frac{W\mu(-Q_i)}{\Delta x} dx = \\ = 4kT\mu\frac{W}{L^2}\int_o^L (-Q_i) dx \end{aligned} \tag{5.11}$$

From (5.9) and (5.11) the thermal noise conductance is derived:

$$G_{nD} = \mu\frac{W}{L^2}\int_o^L (-Q_i) dx = \frac{\mu}{L^2}|Q_I| \tag{5.12}$$

, where $Q_I = W\int_0^L Q_i(x)dx$, is the total inversion charge in the channel.

5.3.2 Short Channel Thermal Noise

The long channel approximation of thermal noise in MOSTs is no longer valid when channel length decreases below a certain value, which is approximately equal to 1 um. Below this value short channel effects influence not only the DC but also the noise characteristics, and this impact becomes more evident with technology scaling. As technology scales down to the deca-nanometer regime, the voltage supply and thus the electric fields within the channel do not scale proportionally with channel length. Therefore the carrier mobility cannot be assumed to be constant. Over the

last decades there has been a discrepancy among the scientific community regarding noise behavior of short channel MOSTs. Thermal noise is underestimated with Van der Ziel model [140, 141, 143, 191] and overestimated with the Klaassen-Prins based method [149, 168, 192–194], especially at low gate voltages [152]. In recent modeling approaches, a lot of effort has been placed in determining the source for excess noise in short channel devices. Different noise mechanisms-diffusion noise model and drifting dipole layer model have been proposed for noise calculation in the velocity saturation region (for more details refer in [152]). However noise contribution of the velocity saturation region has been proven to be negligible as already discussed. In this thesis, we show that excess noise in 90 nm CMOS is due to specific short channel effects, namely velocity saturation (VS), channel length modulation (CLM) and carrier heating (CH), which are presented and discussed below.

5.3.2.1 Velocity Saturation and Carrier Heating

Electrons and holes in bulk CMOS technologies have a characteristic electric field, E_c, and saturation drift velocity, u_{sat}, given in Table 5.2. When the longitudinal field, E_x, along the channel becomes comparable to E_c, then the drift velocity u_{drift}, starts to saturate. The critical field is related to the saturated drift velocity and the mobility at low longitudinal field, μ_z, as: $E_c = \frac{u_{sat}}{\mu_z}$. For high lateral electrical field, the carriers gain higher energy randomizing collisions with the lattice [1]. Thus the carrier temperature increases as a function of the electric field. Therefore, higher carrier temperature induces higher thermal noise, yielding that VS and CH are interdependent phenomena. EKV3 [189, 190] accounts for the impact of VS and CH on thermal noise via the dimensionless critical field parameter λ_c, given by (5.13) [4, 5]. L_{eff} is the effective channel length and will be presented in the CLM section. Assuming constant critical field, λ_c increases with technology scaling, being approximately equal to $\lambda_c = 0.5$, for L_{eff}=100 nm. For a specific technology node it holds that the higher the λ_c value the stronger the short channel effects.

	u_{sat} (m/s)	E_c (V/um)
Electrons	10^5	1
Holes	8x10^4	3

Table 5.2: Characteristic critical field and saturation velocity of electrons and holes in bulk.

$$\lambda_c = \frac{2U_T}{L_{eff}E_c} \tag{5.13}$$

5.3.2.2 Channel Length Modulation

With the MOSFET biased in strong inversion, as V_{DS} increases the channel pinches off. As the electrical field further increases the pinch off point is moving towards the source and hence the electrical channel length shrinks. This effect is called channel length modulation [1] and greatly affects thermal noise. The CLM effect is closely related to VS. This is because the point where the drift velocity of carriers saturates is close to the drain end. This is actually the point where the channel is split into two regions. The first is the non-saturated region whereas the second is the VS or pinch off region, close to the drain. The length of the non-saturated region is called effective channel length, L_{eff}, whereas ΔL is used to represent the length of the VS region. ΔL depends on the longitudinal field and hence on gate and drain bias voltages. Both regions are depicted in Figure 5.3 The EKV3 model accounts for CLM, through a corresponding parameter. Since the carriers in the VS region have reached their maximum velocity, noise voltage fluctuations in the VS region do not propagate to the drain. Therefore, only the active region contributes to channel thermal noise [4, 5, 163, 195, 196].

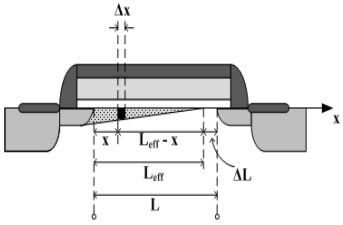


Figure 5.3: MOSFET cross section with the VS region shown to accountfor CLM.

5.3.3 Derivation of Drain Noise Current in Short Channel Devices

To incorporate SCE in thermal noise calculations, the same steps, as for the longer device are followed under the assumption of operation in strong inversion, where SCE are dominant. However the model can be extended covering all operation regions, as described in [197]. The channel conductance, G_{ch} is calculated using the two-transistor approach as: $\frac{1}{G_{ch}} = \frac{1}{G_s} + \frac{1}{G_d}$. G_s (G_1 in the long-channel approximation) is the drain transconductance of T1 after having been isolated it from T2. It is calculated via (5.14) with I_D given by (5.15). Subsequently, G_d (G_2 in the long-channel approximation), corresponding to the source transconductance of T2 is defined in (5.16), with I_D now depending on L_{eff}-x (5.17).

$$G_s = G_{md1} = \frac{dI_D}{dV} \tag{5.14}$$

$$I_D = \frac{W}{x}\int_{V_S}^{V}(-Q_i)\mu_{eff}dV' \tag{5.15}$$

$$G_d = G_{ms2} = -\frac{dI_D}{dV} \tag{5.16}$$

$$I_D = \frac{W}{L_{eff}-x}\int_{V}^{V_{Deff}}(-Q_i)\mu_{eff}dV' \tag{5.17}$$

Therefore, channel conductance at position x is then obtained by (5.18). The channel slice resistance ΔR, is computed, according to [160] by (5.19). μ_{eff} is the effective mobility, and $\mu'_{eff} = \frac{\partial \mu_{eff}}{\partial E_x}$. Differential mobility is defined as $\mu_{diff} = \frac{du_{drift}}{dE_x}$, whereas V_{Deff} is given by (5.20). Both (5.18), and (5.19) are simplified to (5.5), and (5.6), for $\mu'_{eff} = 0$.

$$G_{ch} = \frac{\mu_{eff}(-Q_i)W}{L_{eff} + \int_{V_S}^{V_{Deff}} \frac{\mu'_{eff}}{\mu_{diff}}dV'} \tag{5.18}$$

$$\Delta R = \frac{\Delta x}{W(-Q_i)\mu_{diff}} \tag{5.19}$$

$$V_{Deff} = \begin{cases} V_D, & for\ V_D < V_{Dsat} \\ V_{Dsat}, & for\ V_D \geq V_{Dsat} \end{cases} \tag{5.20}$$

$$L_{eff} = \begin{cases} L, & for\ V_D < V_{Dsat} \\ L - \Delta L, & for\ V_D \geq V_{Dsat} \end{cases} \tag{5.21}$$

Thermal noise conductance, G_{nD}, of short channel MOSTs is derived following the analysis described in [4] and is defined in (5.22). T_C and T_L are the carrier and lattice temperature with their ratio given in (5.23) and factor M is described in (5.24). G_{nD} also simplifies to its long channel value when $\mu'_{eff} = 0$ which in turn results in T_C=T_L.

$$G_{nD} = M\frac{W}{L_{eff}^2}\int_0^{L_{eff}} \mu_z \frac{T_C}{T_L}(-Qi(x))dx \tag{5.22}$$

$$\frac{T_C}{T_L} = \left(\frac{\mu_z}{\mu_{eff}}\right)^2 = \begin{cases} (1+\frac{|E_x|^2}{2E_c}), & for\ |E_x| < 2E_c \\ (\frac{|E_x|}{E_c})^2, & for\ E_x \geq 2E_c \end{cases} \tag{5.23}$$

$$M = \frac{1}{(1 - \frac{V_{Deff} - V_S}{2L_{eff}E_C})^2} \tag{5.24}$$

An analytical expression of thermal noise, in the context of the charge-based

EKV3 compact model, accounting for short-channel effects is given in (5.25). Normalized noise conductance, g_n, is expressed in terms of normalized inversion charges, facilitating the understanding of thermal noise expression by IC designers. If g_n is derived then the PSD of drain current noise is easily calculated by formula (5.27).

$$g_n = \frac{2}{(1+\frac{2U_T(q_s-q_d)}{E_cL_{eff}})^2(q_s+q_d+1)} \times \\ \times \left(\begin{array}{c} \frac{q_s^2+q_sq_d+q_d^2}{3} + \frac{U_T^2i^2}{E_c^2L_{eff}^2} + \frac{(\frac{2U_Ti}{E_cL_{eff}}+1)(q_s-q_d)}{4} + \\ +(\frac{2U_Ti}{E_cL_{eff}}-1)\frac{U_Ti}{2E_cL_{eff}}(q_s+q_d+1)ln\frac{q_s+\frac{1}{2}-\frac{U_Ti}{E_cL_{eff}}}{q_d+\frac{1}{2}-\frac{U_Ti}{E_cL_{eff}}} \end{array} \right) \tag{5.25}$$

$$i = q_s^2+q_s-q_d^2-q_d \tag{5.26}$$

$$S_{id} = 4kTg_n\frac{I_{spec}}{U_T} \tag{5.27}$$

5.3.4 Contribution of Parasitic Resistances to Drain Noise Current

Parasitic gate and substrate resistances have their own part of contribution to drain current noise. The impact of R_G on noise was first studied by Jindal [198], who proposed a complex gate matrix layout to compute voltage fluctuations on gate resistance. According to his theory, in a multi-finger layout as the one in Figure 5.4 the correlated voltage fluctuations in every resistor due to the corresponding fluctuations across each interconnect and gate resistor can be modeled by a simple parameter, $A_{u_{ij}}$. $A_{u_{ij}}$ is the average of the voltage fluctuation in the two ends of the ith distributed gate resistor due to a voltage fluctuation across the jth interconnect or gate resistor, divided by the voltage fluctuation across this jth resistor. The overall R_G, generates a noise voltage of: $S_v = 4kTR_G$, which transfers to the drain current via g_m^2. The contribution of R_G to the drain current noise is: $\Delta S_{I_d} = 4kTR_Gg_m^2$.

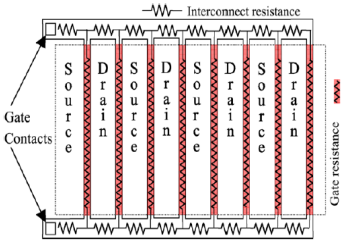


Figure 5.4: A typical resistive gate matrix. Reprinted from [1].

Similarly, for the substrate resistance, R_B, $\Delta S_{I_d} = 4kTR_B g_{mb}^2$, where g_{mb} is the bulk conductance. Because $g_{mb} \ll g_m$, the effect of R_B on the drain current noise is small, provided proper layout. This is analytically presented in [172].

5.3.5 Thermal Noise Parameters

Van der Ziel [140] first characterized thermal noise in MOSTs introducing a thermal noise parameter, γ, and a thermal noise excess factor, α. In this thesis thermal noise parameter and thermal noise excess factor are renamed as δ and γ, respectively, in agreement with [4, 5], and are defined through:

$$\delta = \frac{G_{nD}}{G_{ds0}} \tag{5.28}$$

$$\gamma = \frac{G_{nD}}{G_m} \tag{5.29}$$

In literature, δ is referred as γ and is wrongfully treated as the excess noise factor. G_{ds0} is the output conductance corresponding to zero V_{DS}. This means that when computing δ, G_{nD} is probably evaluated at a different operating point compared to G_{ds0}. Therefore, δ is not so useful for analog/RF design but is mostly used for modeling purposes. Actually, the thermal noise parameter shows how much the thermal noise of a MOST deviates from the value it takes when operating as a passive resistor of conductance G_{ds0}.

On the other hand, thermal noise excess factor γ has been underestimated by the scientific community and has only been presented in [4, 5, 166]. However, no experimental results are available within these references. Albeit, γ is of major importance for the noise performance of circuits, since it represents the noise that is generated at the drain of a transistor, for a given gate transconductance. In (5.29), the thermal noise conductance G_{nD} and gate transconductance G_m are evaluated for the same operating point. In practice, γ can be used to characterize the noise performance of every circuit acting as a transconductor [4]. Additionally, as shown in Section 1.5.3, γ is also of major importance in terms of LNA design [8, 11]. As a rule of thumb, the

smaller γ, the better the noise performance of the device. γ dramatically increases in linear operation since in this region gate transconductance decreases. In the marginal case when V_D tends to V_S, γ approaches an infinite value, due to zero G_m. Therefore it is meaningful to study the excess noise factor behavior in saturation.

Since both parameters depend on noise conductance, G_{nD}, SCEs have a great impact on their value, especially in strong inversion. This will be analytically presented in Section 5.5.3.

5.4 High Frequency Noise Parameters

In the measurement and characterization of RF transistors, the source and bulk terminals are usually short-circuited. Therefore, the device can be thought of as a two-port network with the source acting as the common terminal and the gate and drain terminals being the input and output, respectively. Hence we need to describe the theory of noisy two-port network in which two noise sources, a series current source and a shunt voltage source, as well as their correlation admittance are required to characterize it [24]. The minimum noise figure, the equivalent noise resistance and the optimum source reflection coefficient, usually expressed by its real and imaginary part or by its magnitude and phase, result from this two-port noise analysis. The minimum noise figure is obtained by imposing the input admittance to get its optimum value for noise matching.

5.4.1 Noisy Two-Port Theory

The noise generated by any two-port device can be modeled by a noiseless network with two partially correlated noise sources at its input [199, 200]. This is the cascade equivalent circuit for the noisy-two port. The current and voltage configurations can also be found in [199]. All three implementations are equivalent. These representations are equivalent to the T-parameter, Y-parameter, and Z-parameter, respectively. In the cascade configuration of Figure 5.5, V_n is a noise source representing all the input referred noise of the device when the source impedance is zero, whereas I_n is the input referred noise when the source admittance is zero. The two noise sources are partially correlated since they have the same physical origin and thus I_n can be written as the sum of one uncorrelated (I_{nu}) and one correlated part (I_{nc}). The correlation between I_n and V_n is expressed by the correlation admittance, Y_c.

$$I_n = I_{nu} + I_{nc} = I_{nu} + Y_c V_n \tag{5.30}$$

If we multiply both sides in (5.30) with the conjugate of V_n, V_n^*, and average we can derive an expression for Y_c.

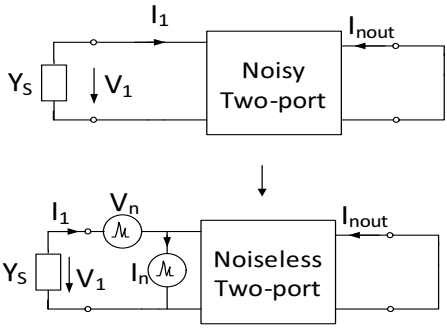


Figure 5.5: Equivalent circuit for a noisy two-port device.

$$I_n V_n^* = I_{nu} V_n^* + Y_c V_n V_n * \Leftrightarrow \overline{I_n V_n^*} = \overline{I_{nu} V_n^*} + \overline{Y_c V_n V_n^*} \Leftrightarrow$$
$$\Leftrightarrow \overline{I_n V_n^*} = \overline{Y_c |V_n|^2} \tag{5.31}$$

$$Y_c = \frac{I_n V_n^*}{|V_n|^2} \tag{5.32}$$

The correlation between the two noisy sources is also represented by the correlation factor, c, which is equal to:

$$c = \frac{\overline{I_n V_n^*}}{\sqrt{\overline{|I_n|^2}\,\overline{|V_n|^2}}} = Yc\sqrt{\frac{\overline{|V_n|^2}}{\overline{|I_n|^2}}} \tag{5.33}$$

Using (5.33), (5.30) can be rewritten as:

$$\overline{|I_{nu}|^2} = \overline{|I_n|^2} - |Y_c|^2 \overline{|V_n|^2} = (1 - |c|^2)\overline{|I_n|^2} \tag{5.34}$$

,where

$$\overline{|I_{nc}|^2} = |Y_c|^2 \overline{|V_n|^2} = |c|^2 \overline{|I_n|^2} \tag{5.35}$$

If we use the PSDs of noise sources V_n and I_n, and rewrite, the above equations we get:

$$S_{iu} = S_i - |Y_c|^2 S_v \tag{5.36}$$

$$S_{ic} = |Y_c|^2 S_v \tag{5.37}$$

$$S_i = S_{ic} + S_{iu} \tag{5.38}$$

The noise sources can be treated as they were thermal sources:

$$S_v = 4kTR_v \tag{5.39}$$

$$S_i = 4kTG_i \tag{5.40}$$

$$S_{iu} = 4kTG_{iu} \tag{5.41}$$

$$S_{ic} = 4kTG_{ic} \tag{5.42}$$

Equivalently, we can write for the noise conductances and resistances:

$$G_{iu} = G_i - |Y_c|^2 R_v \tag{5.43}$$

$$G_{ic} = |Y_c|^2 R_v \tag{5.44}$$

$$G_i = G_{ic} + G_{iu} \tag{5.45}$$

5.4.2 The Noise Factor

The noise factor (F) of a two-port network is defined as the ratio of the total output noise to the output noise due to the source. If we use N_s for the output noise due to the source and N_a for the noise added by the two-port, then F may be written as:

$$F = \frac{total\ output\ noise}{output\ noise\ due\ to\ the\ source} = \frac{N_a + N_s}{N_s} \tag{5.46}$$

If we transform the noisy two-port into a noiseless two-port, then we can use $I_{n,tot}$ for the overall noise current at the input of the two-port. If I_{ns} is the current noise contribution coming from the source, then $I_{n,tot}$ can be calculated applying Kirchoff's Current Law (KCL) [4]:

$$\begin{aligned} I_{n,tot} = I_{ns} + I_n + Y_s V_n \Rightarrow \overline{|I_{n,tot}|^2} = \overline{|I_{ns} + I_n + Y_s V_n|^2} = \\ = \overline{|I_{ns}|^2} + \overline{|I_{nu} + I_{nc} + Y_s V_n|^2} = \\ = \overline{|I_{ns}|^2} + \overline{|I_{nu} + (Y_c + Y_s) V_n|^2} \end{aligned} \tag{5.47}$$

$$\Rightarrow \overline{|I_{n,tot}|^2} = \overline{|I_{ns}|^2} + \overline{|I_{nu}|^2} + |Y_c + Y_s|^2 \overline{|V_n|^2} \tag{5.48}$$

Therefore, F becomes:

$$F = \frac{\overline{|I_{n,tot}|^2}}{\overline{|I_{ns}|^2}} = 1 + \frac{\overline{|I_{nu}|^2} + |Y_c + Y_s|^2 \overline{|V_n|^2}}{\overline{|I_{ns}|^2}} \tag{5.49}$$

Y_s in (5.49) corresponds to the input admittance. The PSD of I_{ns}, S_{ns}, equals: $S_{ns} = 4kTG_s$, where G_s is the source conductance. Thus, if we substitute (5.39) and (5.41) into (5.49) we get:

$$F = 1 + \frac{G_{iu} + |Y_c + Y_s|^2 R_v}{G_s} = 1 + \frac{G_{iu}}{G_s} + \frac{R_v}{G_s}[(G_c + G_s)^2 + (B_c + B_s)^2] \tag{5.50}$$

In order to calculate the optimum values of source admittance, Y_s, for which F becomes minimum (F_{min}), resulting in noise matching, we first differentiate F w.r.t. B_s and set it equal to zero. This way the optimum value of B_s, B_{opt}, is obtained.

$$\frac{\partial F}{\partial B_s} = 0 \Leftrightarrow \frac{2R_v}{G_s}(B_c + B_s) = 0 \tag{5.51}$$

$$B_{opt} = -B_c \tag{5.52}$$

Similarly, by differentiating F w.r.t. G_s and using B_{opt} from (5.52), G_{opt} is also extracted.

$$\frac{\partial F}{\partial G_s} = 0 \Leftrightarrow -\frac{G_{iu}}{G_s^2} - \frac{R_v G_c^2}{G_s^2} + R_v = 0 \tag{5.53}$$

that is,

$$G_{opt} = \sqrt{\frac{G_{iu}}{R_v} + G_c^2} = \sqrt{\frac{G_i - |Y_c|^2 R_v}{R_v} + G_c^2} = \sqrt{\frac{G_i}{R_v} - B_c^2} \tag{5.54}$$

Substituting (5.54) and (5.52) into (5.50) and taking into account (5.43) and (5.44) F_{min} is obtained.

$$F_{min} = 1 + 2R_v(G_{opt} + G_c) \tag{5.55}$$

The inverse relationships for the calculation of the correlated conductance, G_c, and the uncorrelated part of G_i, G_{iu}, yield:

$$G_c = \frac{(F_{min} - 1)}{2R_v} - G_{opt} \tag{5.56}$$

$$G_{iu} = (G_{opt}^2 - G_c^2)R_v \tag{5.57}$$

If we then substitute (5.52), (5.56), and (5.57) into (5.50), an expression for the noise factor in terms of F_{min}, R_n, G_{opt}, and B_{opt} is easily derived:

$$F = F_{min} + \frac{R_v}{G_s}[(G_s - G_{opt})^2 + (B_s - B_{opt})^2] = F_{min} + \frac{R_v}{G_s}|Y_s - Y_{opt}|^2 \tag{5.58}$$

According to (5.58), for the noise factor to reach its minimum value, both conditions G_s=G_{opt} and B_s=B_{opt} should hold. This situation is called noise matching and is desirable in low-noise amplifier circuits. The optimum admittance Y_{opt}, in (5.58) is evaluated through the optimum source reflection coefficient, Γ_{opt}:

$$Y_{opt} = Y_0 \frac{1 - \Gamma_{opt}}{1 + \Gamma_{opt}} \tag{5.59}$$

Therefore, four noise parameters, namely F_{min}, R_v, and Γ_{opt} (in real/imaginary or magnitude/phase) are required to describe the noise figure of a noisy two-port network [174].

In [175] an invariant noise parameter, called Lange invariant (N) is used instead of R_n, reducing the number of HF noise parameters to three. At first F is rewritten from (5.58) as:

$$F = F_{min} + \frac{N|Y_s - Y_{opt}|^2}{G_s G_{opt}} \tag{5.60}$$

N can be obtained by measuring the 50 Ω noise figure, $F(Y_0)$. It holds that:

$$F(Y_0) = F_{min} + N\frac{4|\rho|^2}{1 - |\rho|^2} = F_{min} + N\frac{(V-1)^2}{V} \tag{5.61}$$

, where V is the voltage standing wave ratio: $V = \frac{1+|\rho|}{1-|\rho|}$, and ρ is the reflection coefficient. Thus,

$$N = (F(Y_0) - F_{min})\frac{V}{(V-1)^2} = (F(Y_0) - F_{min})\frac{1 - |\rho|^2}{4|\rho|^2} \tag{5.62}$$

N depends only on the magnitude of reflection coefficient and not on its phase, reducing the number of noise parameters required to model HF noise to three. When the transit frequency is much higher than the operating frequency ($f_T \gg f$) and gate-drain capacitance is much smaller than gate-source capacitance ($C_{gd} \ll C_{gs}$) and $|c| = 0$, then N can be further simplified to: $N = \frac{F_{min}-1}{2}$ [177].

5.5 Results and Discussion

Results are presented both for the de-embedded and modeled data and the accuracy of the model is proven from strong to moderate inversion and for all available channel lengths. We first start with HF noise parameters, from which PSD of drain and gate current noise is obtained. Then, measurements of noise parameters, γ and δ, are validated with the EKV3 model and SCEs on their behavior are shown. For the purpose of this work n-MOS devices have been given more attention compared to p-MOS, due to the available measurements. Nevertheless, results for p-MOS transistors are also presented and their noise behavior is also disclosed. The extraction process for the calculation of all noise characteristics is given in Figure 5.6. As already explained in Chapter 3, S-parameters are also needed for de-embedding noise parameters. For the verification of S-parameters and noise measurements a well defined and expected behavior should be confirmed. This can be done through parasitic resistances and capacitances for S-parameters and through the PSD of drain current noise for noise, since their frequency response is known to be flat.

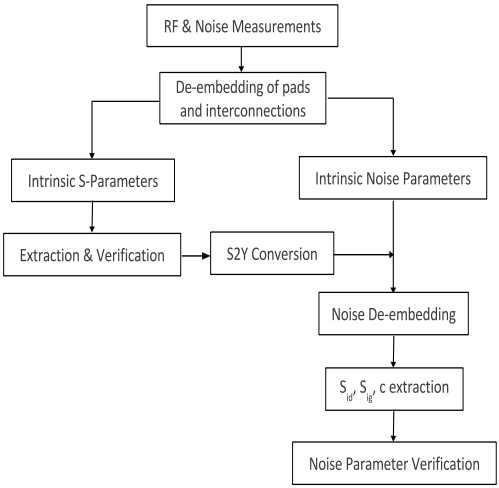


Figure 5.6: Noise Parameter Extraction.

5.5.1 High Frequency Noise Parameters

The minimum values of NF_{min} for different nominal gate length n-MOS and p-MOS devices are shown in Figure 5.7. The results correspond to fixed $|V_{DS}|$ = 1.2 V and a frequency of 10 GHz, while $|V_{GS}|$ is swept. The remarkable difference between n-MOS and p-MOS devices can be explained by the tremendous difference in their

transit frequency values and in the different nature of velocity saturation among the two channel types. The model's scalability is depicted in Figure 5.8, where NF_{min} is plotted versus frequency for 3 different channel length n-MOS devices. Contrary to Figure 5.7, results in Figure 5.8 are extracted for a fixed V_{GS}. This consequently explains the difference for the NF_{min} values obtained at 10 GHz. Minimum noise figure, normalized equivalent noise resistance and real and imaginary parts of optimum source reflection coefficient are presented in Figure 5.9 and Figure 5.10 versus frequency, for the shortest and longest available n-MOS devices. This is also done for p-MOS devices of L=100 and 240 nm, as shown in Figure 5.11 and Figure 5.12, respectively. Measured data are symbols and modeled data are lines (holds throughout the rest of the text).

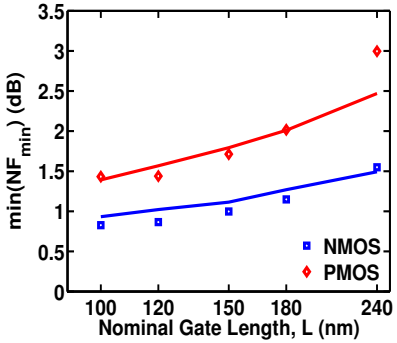


Figure 5.7: Minimum values of NF_{min} for n-MOS and p-MOS devices of channel length ranging from 240 nm to 100 nm, at 10 GHz.

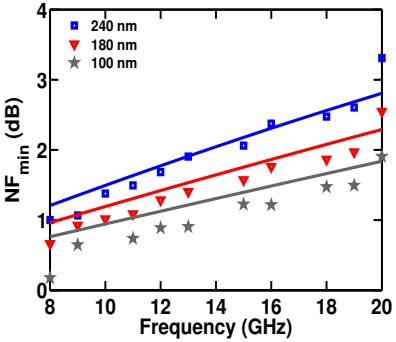
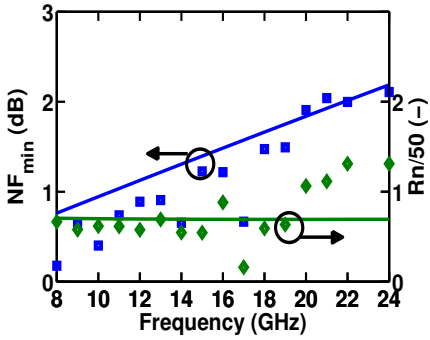
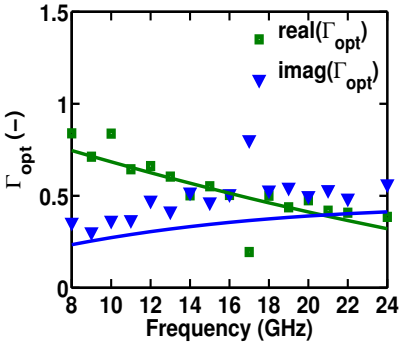


Figure 5.8: NF_{min} versus frequency for n-MOS devices of W=40 x 2 um, biased at V_{DS}=1.2 V and V_{GS}=0.65 V.

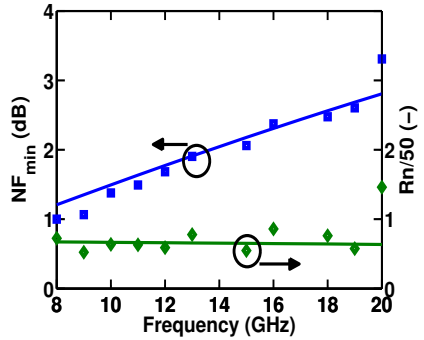


(a) NF_{min} and $R_n/50$

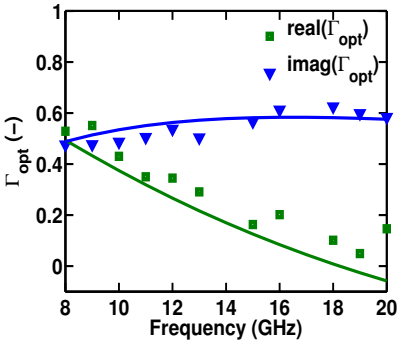


(b) Real (G_{min}) and Imag (G_{min})

Figure 5.9: Noise parameters versus frequency for a n-MOS device of channel length L=100 nm and channel width W=40 x 2 um, biased at V_{GS}=0.65 V and V_{DS}=1.2 V.

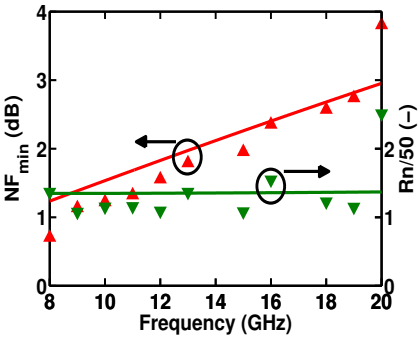


(a) NF_{min} and $R_n/50$

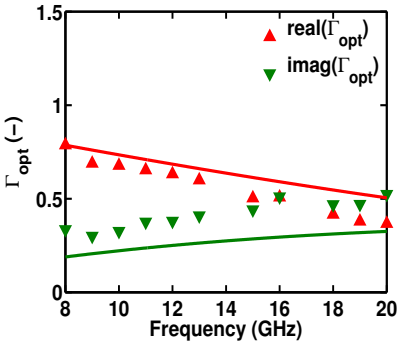


(b) Real (G_{min}) and Imag (G_{min})

Figure 5.10: Noise parameters versus frequency for a n-MOS device of channel length L=240 nm and channel width W=40 x 2 um, biased at V_{GS}=0.65 V and V_{DS}=1.2 V.

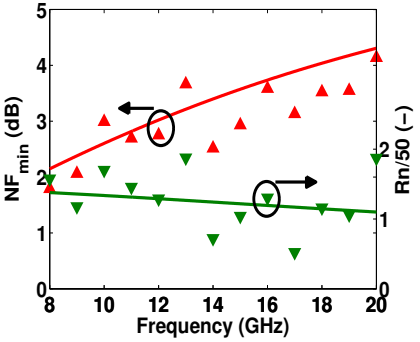


(a) NF_{min} and $R_n/50$

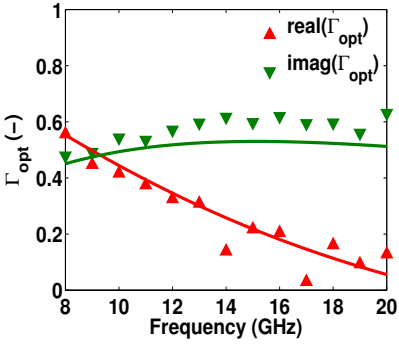


(b) Real (G_{min}) and Imag (G_{min})

Figure 5.11: Noise parameters versus frequency for a p-MOS device of channel length L=100 nm and channel width W=40 x 2 um, biased at V_{GS}=-0.65 V and V_{DS}=-1.2 V.



(a) NF_{min} and $R_n/50$



(b) Real (G_{min}) and Imag (G_{min})

Figure 5.12: Noise parameters versus frequency for a p-MOS device of channel length L=240 nm and channel width W=40 x 2 um, biased at V_{GS}=-0.65 V and V_{DS}=-1.2 V.

From the circuit perspective, it is interesting to study noise parameters with respect to bias and specifically inversion level in the channel. NF_{min} is plotted together with the associated power gain (G_{ass}) in Figure 5.13. G_{ass} is the tuned gain of the device when it is matched at the input for optimum noise figure and matched at the output for minimum reflection, and is calculated through (5.63). A minimum noise figure of 0.82 dB with an associated gain of about 11 dB is obtained at 10 GHz for a n-MOS device of L = 100 nm and W= 40 × 2 um. Optimum values of both metrics are obtained at the same inversion level.

$$G_{ass} = \frac{(1-|\Gamma_{opt}|^2)|S_{21}|^2}{|1-S_{11}\Gamma_{opt}|^2} \tag{5.63}$$

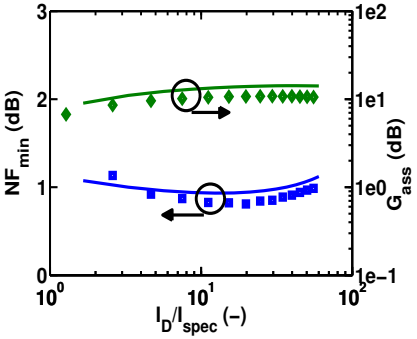
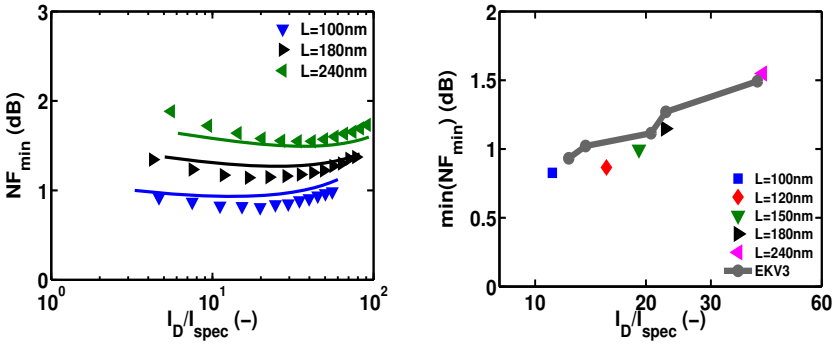


Figure 5.13: NF_{min} and G_{ass} versus inversion coefficient for a n-MOS device of L=100 nm and W=40 x 2 um, biased at V_{DS}=1.2 V.



(a) NF_{min} versus inversion coefficient for n-MOS devices

(b) Minimum NF_{min} versus inversion coefficient with length scaling

Figure 5.14: NF_{min} trend for n-MOS devices of W=40 x 2 um, biased at V_{DS} =1.2 V, at 10 GHz.

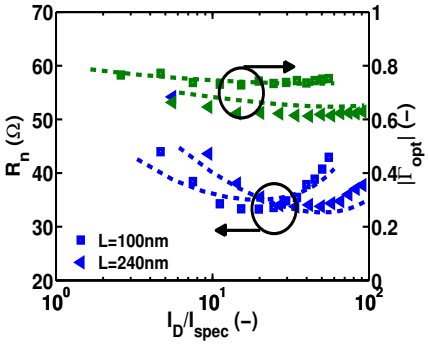


Figure 5.15: R_n and $|\Gamma_{opt}|$ versus inversion coefficient for n-MOS devices of channel length L=100 and 240 nm.

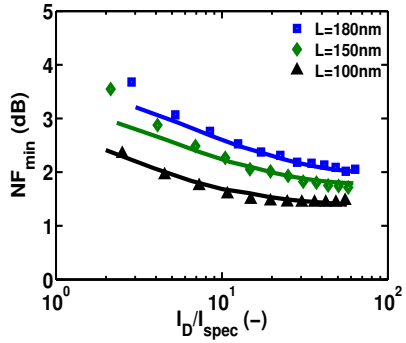


Figure 5.16: NF_{min} versus inversion level and scaling for p-MOS devices of W=40 x 2 um, biased at $|V_{DS}|$=1.2 V, at 10 GHz.

The relation among NF_{min}, scaling and channel inversion level is displayed in Figure 5.14a and Figure 5.14b, where the NF_{min} of different gate length n-MOS devices is plotted versus IC. The available bias points cover a range from the center of M.I. to deep S.I. The minimum NF_{min} value is moving to lower inversion levels as L decreases. This becomes clearer in Figure 5.14b, where for L = 240 nm, the minimum NF_{min} is observed at $IC =\sim 30$, whereas the respective value for L = 100 nm is obtained in the vicinity of moderate to strong inversion ($IC =\sim 11$). This clearly indicates that for more advanced technology nodes (e.g., 65 or 45 nm), the optimum NF_{min} value is expected within the moderate inversion region, shifting closer to its center. Thus, the compromise between power consumption and noise performance is plainly relaxed when compared with former technology nodes [201]. The same trend is observed in Figure 5.15, where equivalent noise resistance, R_n and

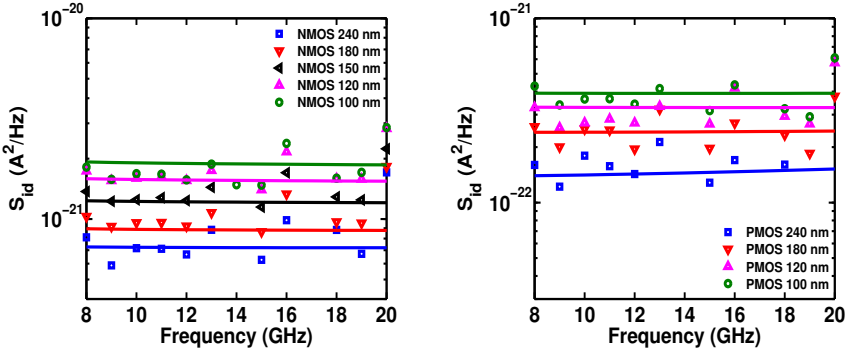
magnitude of optimum source reflection coefficient, $|\Gamma_{opt}|$, are presented for n-MOS devices of L=100 nm and L=240 nm. Interestingly, optimum R_n is also achieved at lower IC values when L is decreased. The trend remains the same however not so clear for p-MOS devices (Figure 5.16) in which optimum NF_{min} for the shortest available MOST corresponds to an IC approximately equal to 30, which means operation in S.I.

5.5.2 Power Spectral Density of Drain Noise Current

The PSD of drain noise current, S_{id}, can be extracted directly from the de-embedded data according to (5.64). Since S-parameters are measured along with noise parameters, at the same bias points and frequencies, S_{id} can be computed at any operating point and frequency. S_{id} formula for EKV3 model is given by (5.65), where g_{nD} is the normalized noise conductance, expressed in terms of normalized inversion charge [190]. I_{spec}/U_T is the normalization quantity for conductances (in A/V), called specific conductance. The PSD of drain current noise is presented in Figure 5.17a for n-MOS devices of channel length ranging from 240 to 100 nm and frequency range up to 20 GHz, while Figure 5.17b presents the equivalent S_{id} for p-MOS devices.

$$S_{id} = 4kTR_n|Y_{21}|^2 \tag{5.64}$$

$$S_{id} = 4kT\frac{I_{spec}}{U_T}g_{nD} \tag{5.65}$$



(a) n-MOS devices

(b) p-MOS devices

Figure 5.17: S_{id} versus frequency for devices of W=40 x 2 um, biased at $|V_{GS}|$=0.65 V and $|V_{DS}|$=1.2 V.

Figure 5.18 demonstrates S_{id} versus bias, expressed in terms of normalized current. S_{id} is accurately modeled from moderate to strong inversion for all devices, which is essential for the correct modeling of design parameters as well. S_{id} is only slightly dependent on V_{DS} in saturation [172]. Its bias dependence on V_{GS} at 10 GHz is shown in Figure 5.19 . The noticeably lower drain current noise level in p-MOS devices is due to their lower mobility compared with n-MOS devices.

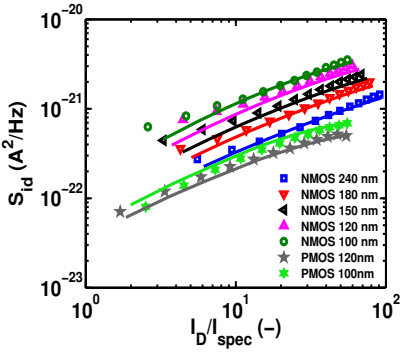


Figure 5.18: S_{id} versus inversion coefficient for n-MOS and p-MOS devices, biased at $|V_{DS}|$=1.2 V, at 10 GHz.

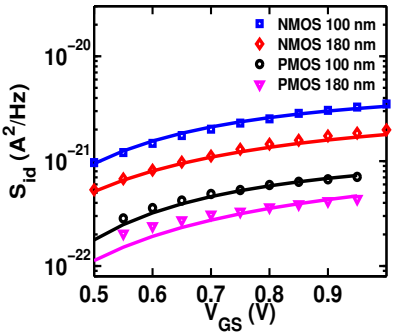


Figure 5.19: S_{id} versus $|V_{GS}|$ for n-MOS and p-MOS devices of W=40 x 2 um, biased at $|V_{DS}|$=1.2 V, at 10 GHz.

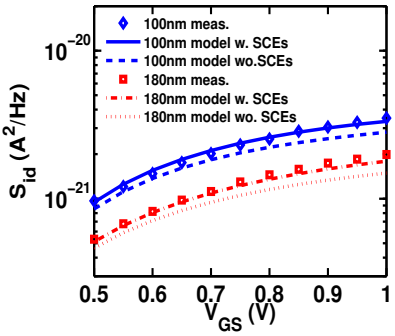


Figure 5.20: S_{id} versus V_{GS} for n-MOS devices of W=40 x 2 um, biased at $|V_{DS}|$=1.2 V, at 10 GHz, with (w.) and without (wo.) accounting for SCEs.

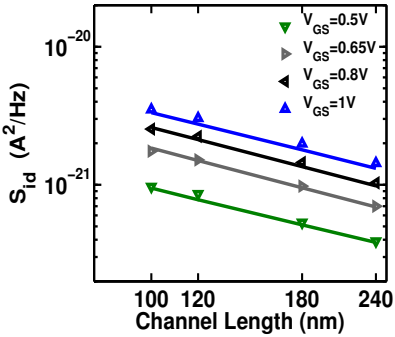


Figure 5.21: S_{id} versus channel length for n-MOS devices of W= 40 x 2 um, biased at V_{DS}=1.2 V, at 10 GHz.

The behavior with and without accounting for SCEs in the noise model is shown in Figure 5.20. When VS and CLM effects on noise are deactivated (while the dc model remains unaffected, i.e., conserves all SCEs such as VS and CLM), the model predicts a significantly decreased S_{id} at high gate voltage, particularly for the shorter channel device. This is accomplished by introducing a parameter accounting for SCEs on the noise model only, without affecting its DC part. Without the inclusion of SCEs, the PSD of drain noise current is significantly underestimated. This has also been reported in [152] for 0.18 um CMOS. The dependence of S_{id} on channel length is shown in Figure 5.21, where S_{id} is plotted for n-MOS devices with channel length of L = 100, 120, 180, and 240 nm for different V_{GS}, at V_{DS} = 1.2 V at 10 GHz. The slope of the figure is 1/L, as recently reported for longer devices in [202]. The layout dependences of S_{id}, which have been shown, e.g., in [172, 203, 204], are not

within the scope of this thesis. However, these are covered by the scaling parameters of the EKV3 model.

5.5.3 Design Parameters

In this thesis, both thermal noise parameter and excess noise factor, δ and γ , respectively, are presented with respect to channel length and bias. The SCEs on thermal noise—such as CLM, VS, and carrier heating— affect mobility and hence G_m, effective length, and γ [4, 5]. Modeling of γ is validated versus measurements for the first time, for n-MOS devices with channel length from 240 to 100 nm.

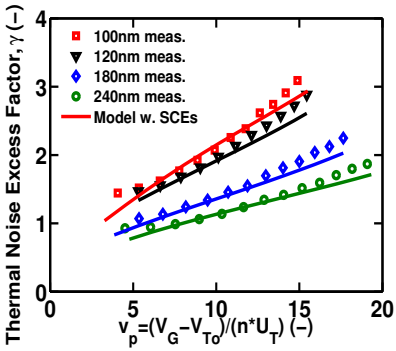


Figure 5.22: Thermal noise excess factor versus normalized pinch-off voltage for n-MOS devices of W=40 x 2 um, biased at V_{DS}=1.2 V.

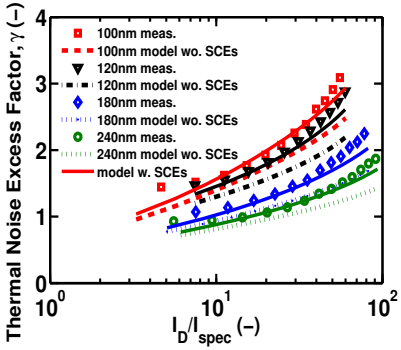


Figure 5.23: Thermal noise excess factor versus inversion coefficient for n-MOS devices of W=40 x 2 um, biased at V_{DS}=1.2 V, with and without accounting for SCEs.

Figure 5.22 shows γ versus the pinchoff voltage V_P/U_T, where $V_P = (V_G – V_{TO})/n$. The vertical field mobility effects [4] do not seem to be noticeable and hence have not been included in the model. Figure 5.23 shows γ versus drain current I_D/I_{spec}. When SCEs are ignored in the noise model, γ is underestimated by up to 20% (which could be significantly more in more scaled technology). The effect of length scaling on γ is shown in Figure 5.24 . The exact value of thermal noise excess factor for specific geometries and bias conditions is essential for RFIC designers; γ is used for determining the minimum noise factor of a common-source (CS) low-noise amplifier (LNA), as shown in (5.66) [4]. Therefore, assuming its long-channel value, as it is more or less the case in literature [24] will result in inaccurate hand calculations. β_G is defined in (5.67), standing for the induced gate noise parameter, with G_{nG} and G_{Gi} being the thermal noise conductance at the gate and the conductance seen at the gate, respectively. S_{ig} cannot be ignored in noise calculations, since the outcome would be nonphysical (F_{min} = 1) [205]. Results presented here for γ are in close proximity with [4, 5], which are the only sources from literature that have taken into account, parameter γ rather than δ, to predict the excess noise in integrated circuits. In these references, γ is presented versus the pinch-off voltage, as well. However, measurements for γ are not available in [4, 5]. Hence we prove here that modeling approaches in the context of the EKV3 compact model, previously used by Enz and Roy, which are similar to those adopted in this thesis - since the core model is the same - are reliable and accurate. This is done by validating them with measurements of the investigated 90 nm process.

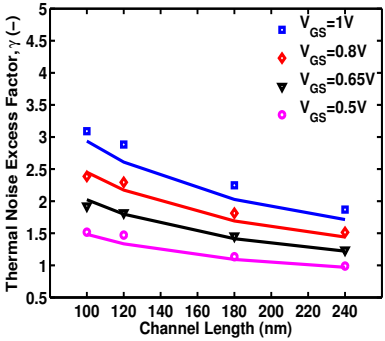


Figure 5.24: Thermal noise excess factor versus channel length for n-MOS devices of W=40 x 2 um, biased at V_{DS}=1.2 V.

$$F_{min} = 1 + 2\gamma\frac{\omega}{\omega_T}\sqrt{\frac{\beta_G}{\gamma}(1-c)^2} \tag{5.66}$$

$$\beta_G = \frac{G_{nG}}{G_{Gi}5n} \tag{5.67}$$

The thermal noise parameter δ obtained for n-MOS devices with channel width W = 40 × 2 um, operating in saturation (Figure 5.25), deviates from its theoretical long-channel value (2/3), and is in agreement with the results presented earlier in [172, 196], for 180 and 250 nm channel lengths. Figure 5.25 shows that δ is slightly dependent on V_{GS} in saturation for a given channel length [4]. The thermal noise parameter is shown to be only slightly dependent on V_{DS} in saturation, while it is significantly dependent on V_{DS} in linear operation [164, 206]. The initial rise for δ in the linear region is believed to be due to carriers getting hotter. As the device enters the saturation region this increase slows down pointing perhaps to a change in the noise mechanism [1, 148]. Since this remark back in 1985, numerous experimental papers have reported measurements of δ. Results for some of the most cited among them are plotted in Figure 5.26, along with measurements of the 90 nm process. Most of the results are reproduced from [1] with some necessary corrections. Thermal noise parameter measured and modeled in this thesis is in agreement with a large set of data, demonstrated in the graph. Additionally, it is proven that for constant V_{DS}, δ decreases when V_{GS} increases. Thermal noise parameter seems to increase for n-MOS devices down to 40 nm, recently reported in [173, 183, 207] for operation in strong inversion and saturation.

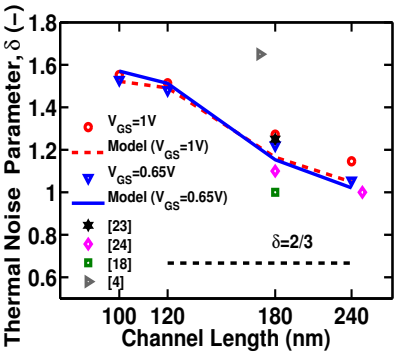


Figure 5.25: Thermal noise parameter factor versus channel length, for n-MOS devices biased at V_{DS}=1.2 V, at 10 GHz.

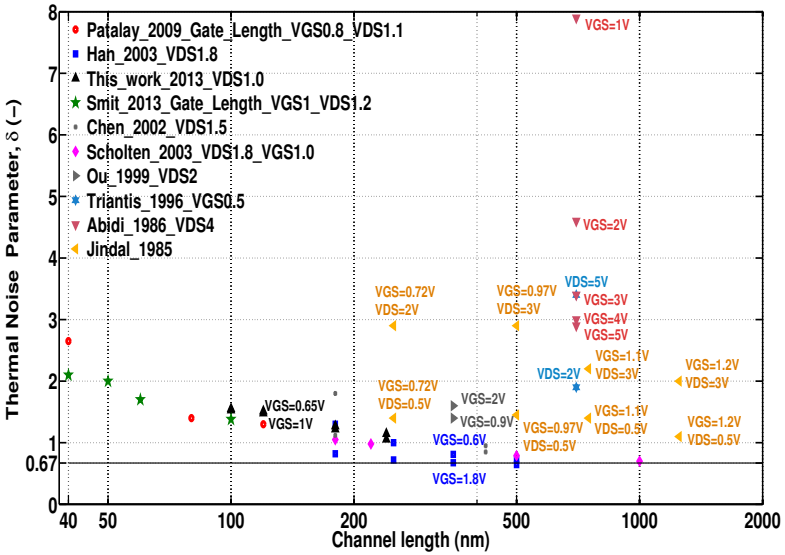


Figure 5.26: Noise parameter δ, versus channel length. Partially reproduced from [1].

5.5.4 Gate Current Noise

The two main contributions to the total gate current noise are the parasitic gate resistance R_G and the induced gate noise of the intrinsic MOSFET. According to [172], R_G dominates gate current thermal noise, by contributing more than 60% to the overall gate current noise. This holds for the specific case shown in [172] where a n-MOS device of L=0.18 um, at f=3 GHz, biased at $V_{DS} = 1.8V$, and $V_{GS} = 1V$ is investigated. Almost half of this amount is layout dependent. Thus, to minimize R_G, devices with a large number of narrow gate fingers (N_f) [172] have been designed since R_G varies proportionally to $1/(N_f)^2$ [133]. Moreover, careful layout has been performed by double-sided contacting the gate so that R_G can be further reduced [172]. EKV3 accounts for scaling of multi-finger devices and covers layout-dependent effects [190].

At radio frequencies, thermal noise from the drain is transferred to the gate, due to the capacitive coupling existing between the channel and the gate, resulting in induced gate noise [208, 209]. The induced gate noise is correlated with the channel noise, because of their same origin. The PSD of induced gate noise (S_{ig}) can be described in terms of the noise ans S-parameters through:

$$S_{ig} = 4kTR_n\{|Y_{opt}|^2 - |Y_{11}|^2 + 2Re[(Y_{11} - Y_{cor})Y_{11}^*]\} \tag{5.68}$$

The correlation admittance Y_{cor} is derived by the measured noise parameters:

$$Y_{cor} = \frac{NF_{min} - 1}{2R_n} - Y_{opt} \tag{5.69}$$

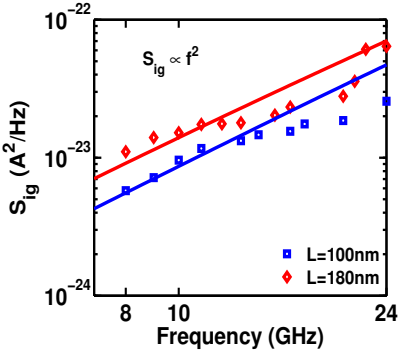


Figure 5.27: S_{ig} versus frequency for n-MOS devices of W=40 x 2 um, biased at V_{DS}=1.2 V and V_{GS}=0.65 V.

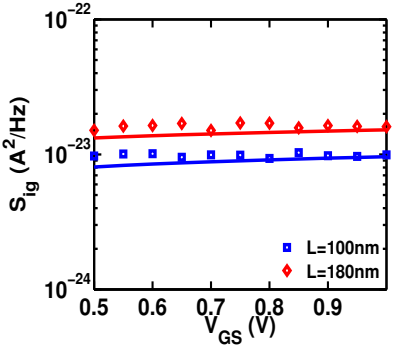


Figure 5.28: S_{ig} versus V_{GS} for n-MOS devices of W=40 x 2 um, biased at V_{DS}=1.2 V, at 10 GHz.

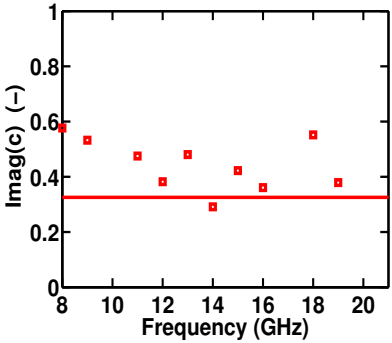


Figure 5.29: Imaginary part of correlation coefficient versus frequency for a n-MOS device of L=100 nm and W=40 x 2 um, biased at V_{DS}=1.2 V and V_{GS}=0.65 V.

Modeling induced gate noise requires an equivalent noise circuit. In this work, this was implemented using a noise subcircuit, consisting of a MOSFET, RF chokes, and a dc voltage source together with a polynomial current controlled voltage source, which was used to sense the noise at the gate terminal. The model behaves as expected, since S_{ig} increases with the square of frequency [143, 210]. This is shown in Figure 5.27, where n-MOS devices with channel length of L = 100 and 180 nm, and channel width W = 40 × 2 um, biased at V_{DS} = 1.2 V and V_{GS} = 0.65 V are shown. S_{ig} decreases with channel length since C_{GS} also decreases. Contrary to S_{id},which depends on V_{GS}, S_{ig} has only a slight dependence on V_{GS}, as shown in Figure 5.28. The correlation between channel noise and induced gate noise is usually specified by the correlation factor, c, which is given by (5.29), where S_{igid^*} is the PSD of the correlation noise

$$c = \frac{S_{igid^*}}{\sqrt{S_{ig}S_{id}}} \tag{5.70}$$

The imaginary part of the correlation factor, for an n-MOS device of channel length L = 100 nm in strong inversion and saturation is close to its theoretical value (0.4j), as reported in [4, 211], and shown in Figure 5.29.

5.6 Contribution

Measurements and modeling of high-frequency (HF) noise, especially at frequencies close to the millimeter-waveband (30 - 300 GHz) should provide circuit designers insight into the scalability of noise behavior of MOS devices under given bias conditions and channel length. There is a considerable number of publications on the subject highlighting many aspects of HF noise in MOSFETs [89, 160, 161, 163, 196, 203, 204, 212–231]. RF noise parameters essential for circuit design have been analyzed [160, 161, 212–215] and RF noise modeling of modern CMOS technologies with channel length smaller than 90 nm has been discussed for a frequency range up to 18 GHz [203, 216–219]. Noise measurements up to 27 GHz have also been reported [204, 220–222]. However, in all these cases, certain limitations on modeling and measurements are observed, regarding frequency and bias coverage of RF noise characteristics, e.g., power spectral densities (PSD) of drain (S_{id}) and gate (S_{ig}) noise currents are not shown in detail [203, 219], or shown only for specific bias conditions [216–218]. So far, the excess noise factor has not been given enough attention and, to the best of our knowledge, has never been verified with measurements.

This situation clearly calls for a deeper investigation of RF noise in MOSFETs. In this thesis, a 90-nm CMOS technology was used in the context of a millimeter-wave project for wireless broadband transmission at 60–65 GHz. Critical RF noise parameters for RFIC design were investigated over scaling and channel inversion level. Thermal noise excess factor measurements were reported for the first time and SCEs on its behavior were examined. Moreover, drain and gate current noise as well as their correlation are thoroughly covered over a wide range of frequencies, bias points, and channel lengths. For the investigated frequency range, automotive and industrial applications have been reported [232].

With CMOS downscaling, extremely high f_T has been achieved but at the expense of high power consumption, which has become a critical specification for ultra low power devices. With the decrease in the power supply and the corresponding decrease in the overdrive voltage, the operating point of RFICs is progressively moving towards lower inversion levels, away from the classical strong inversion region. Moreover, RF circuit design in deep-submicrometer CMOS technologies relies heavily on accurate modeling of thermal noise [183]. Therefore, as is concluded in [233], "the channel noise models for transistors working in these regions has become important for low-power applications. Finally the scaling issues and the temperature characteristics of the active noise sources in the transistor are another research area for future studies". In this work, all aspects of drain and gate current noise were modeled in the context of circuit design and optimum performance of the investigate 90 nm process was achieved close to M.I. region, while according to the trend minimum noise is expected to shift to even lower inversion levels at more advanced technologies. This is of tremendous importance for RFIC design, since a good tradeoff between noise and power can be achieved within this region.

Chapter 6

Conclusions and Future Work

In this thesis nanoscale RF CMOS transceiver design was explored in the context of radio frequency integrated circuits operating under low-power while achieving superior performance. The work was focused on low-noise amplifier design, which is the most critical component of a receiver. A test chip including an LNA operating at 30 GHz as well as individual RF transistors of several geometries was implemented in 90 nm CMOS process from TSMC. A large number of high-frequency and noise measurements was performed in order to study the behavior of the incorporated devices with channel length scaling and inversion level. Figures of merit related to LNA design were extracted and optimum performance was found to be achieved in moderate inversion. With technology scaling, a trend towards lower levels of moderate inversion is observed.

First small-signal behavior of the investigated 90 nm process was analyzed addressing fundamental design characteristics. Figures of merit recently proposed, such as the transconductance frequency product and transconductance efficiency multiplied by the gate transconductance have been shown to be proportional with the overall performance of cascode LNA. Their maximum values were obtained within moderate inversion region, for the shortest available measured devices. As technology roadmap leads to ultra-deep-submicron technologies, TCAD simulation data were also used to explore the behavior of the above-mentioned FoM down to 22 nm. Interestingly we prove that with technology scaling the optimum bias point is progressively moving towards the center of moderate inversion. The same is observed for non-linearity figures of merit.

Thermal noise of MOS transistors remains a hot topic as contradicting results and interpretations on the impact of short-channel effects on it are still found in literature. In this work, thermal noise of MOS transistors was analyzed over a wide range of geometries, bias points and frequencies. We mainly focused on n-MOS devices for which optimum performance in terms of their minimum noise figure was also found just above the high limit of moderate inversion. This means that in the case of a

noise matched LNA, the noise figure will be also achieved at the same operating point. To the best of our knowledge, this is the first time noise is presented in a way circuit designers can easily understand and benefit from. This was made possible by presenting noise metrics versus inversion coefficient, whose value demonstrates the device inversion level. The significance of the thermal noise excess factor was highlighted, by verifying it with measurements for the first time. Thermal noise excess factor is a key parameter for LNA design as it is found in the formula of its minimum noise figure. Thus, it is really critical to distinguish it from the thermal noise parameter, which is wrongly treated as the excess noise factor in literature.

The EKV3 physics-based compact model was used to validate measurements. The impact of short-channel effects, namely velocity saturation, channel length modulation and carrier heating on the excess noise factor was presented. The model was validated through all investigated domains, i.e. frequency, scaling and bias, from technology nodes of 180 nm down to 22 nm.

Using the extracted model parameters, an LNA operating at 5 GHz was designed, biased close to the center of moderate inversion. Its overall high performance and minimum power consumption proves the validity of this work. Indeed, the trend of all individual FoM with channel length and scaling are correctly applied to RFIC design.

In summary, we have shown that despite the certain difficulties arising from downscaling, design trade-offs among certain FoM become more relaxed as CMOS scales down to the deca-nanometer regime, since optimum performance is obtained around the threshold voltage. Therefore ultra low power nanoscale RFICs can be obtained by properly choosing their biasing points according to qualitative FoM.

Following the philosophy of this thesis the investigated performance characteristics of RF devices can be further expanded in measuring and modeling state-of-the-art technologies, e.g. 40 nm or 28 nm CMOS, or beyond. For example, the excess noise factor whose importance was highlighted here, can be investigated in devices where short-channel effects will be even more dominant. Since the optimum performance of such advanced CMOS technologies is expected to be achieved close to the center of moderate inversion, the realization of RFICs - particularly LNAs - biased within this region will also substantiate that low-power operation and high RF performance are two concepts that can co-exist constructively.

Appendix A

Basics of the EKV3 Model

The Appendix introduces basic definitions of the EKV3 charge-based model. The relation between inversion charge and voltages is presented. Expressions for the channel current are derived and inversion coefficient, which is massively used in the thesis, is determined.

A.1 Charges and Potentials in MOSFET

The gate voltage, V_G, of a MOS device is given by (A.1). ϕ_{MS} is the gate work function difference between the gate and the substrate. Ψ_{ox} and Ψ_s is the oxide and surface potential, respectively.

$$V_G = \phi_{MS} + \Psi_{ox} + \Psi_s \tag{A.1}$$

The mobile inversion charge Q_i which is obtained by integrating the electron mobility $n_P$below the surface of the silicon is given by (A.2). The inversion charge can be normalized by introducing a specific charge Q_{spec}.

$$Q_i = -q \int_0^{\infty} n_P \, dz \tag{A.2}$$

$$q_i = Q_i / Q_{spec} \tag{A.3}$$

, where Q_{spec} is given by (A.4):

$$Q_{spec} = -2nU_T C_{ox} \tag{A.4}$$

The slope factor, n, is given in (A.5), where Ψ_{sp} is the pinch-off surface potential.

$$n = \left[\frac{\partial \Psi_{sp}}{\partial V_G} \right]^{-1} \tag{A.5}$$

The pinch-off voltage V_P can be approximated by (A.6), in which V_{TO} is the threshold voltage. The normalized pinch-off, v_P voltage is calculated by dividing V_P with the normalization constant for voltages, which is the thermal voltage U_T. Thus, $v_P = V_P/U_T$.

$$V_P \simeq \frac{V_G - V_{TO}}{n} \tag{A.6}$$

The relation between normalized inversion charge and normalized local channel voltage, u_{ch} is given in (A.7).

$$2q_i + ln(q_i) = v_P - u_{ch} \tag{A.7}$$

In weak inversion, it holds that: $q_i << 1$. Thus, the linear term in (A.7) becomes negligible. The mobile inverted charge can be approximated by:

$$q_i = exp(u_P - u_{ch}) \tag{A.8}$$

In strong inversion: $q_i >> 1$. Thus, q_i is equal to:

$$q_i = \frac{u_P - u_{ch}}{2} \tag{A.9}$$

A.2 Static Drain Current and Inversion Coefficient

Drain current, including its drift and diffusion components and assuming constant mobility, μ, is given by (A.10). The transfer parameter, β, of the transistor is equal to (A.11). Equation (A.10) shows that I_D can be obtained directly from $Q_i(V)$ as depicted in Figure A.1. The integral in (A.10) can be rewritten according to (A.12).

$$I_D = \beta \int_{V_S}^{V_D} \frac{-Q_i}{C_{ox}} dV \tag{A.10}$$

$$\beta \equiv \mu C_{ox} \frac{W}{L} \tag{A.11}$$

$$I_D = \beta \int_{V_S}^{\infty} \frac{-Q_i}{C_{ox}} dV - \beta \int_{V_D}^{\infty} \frac{-Q_i}{C_{ox}} dV = I_F - I_R \tag{A.12}$$

Therefore drain current can be expressed as the difference between a forward current, I_F and a reverse current I_R. I_F depends on V_P and V_S, while I_R depends on V_P and V_D.

All currents can be normalized to the specific current which is given by (A.13). The quantity $2nU_T^2\mu C_{ox}$ is called technology current, I_0. Forward and reverse normalized currents are expressed by (A.14) and (A.15), respectively, as functions of normalized inversion charges in source (q_s) and drain (q_d).

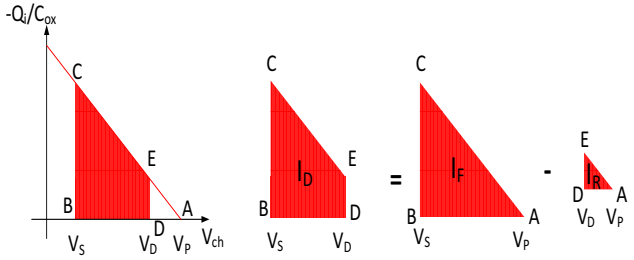


Figure A.1: Drain current expressed through its forward and reverse components.

$$I_{spec} = 2nU_T^2 \mu C_{ox} \frac{W}{L} = 2n\beta U_T^2 \tag{A.13}$$

$$i_f = \frac{I_F}{I_{spec}} = q_s^2 + q_s \tag{A.14}$$

$$i_r = \frac{I_R}{I_{spec}} = q_d^2 + q_d \tag{A.15}$$

The inversion level of the whole transistor can by characterized by a quantity called inversion coefficient, IC. In forward saturation, where $I_F >> I_R \Rightarrow I_D = I_F$. Therefore $IC = i_f$. The value of IC directly indicates the inversion level of the transistor, independently of device type and geometry. Specifically:

- For $IC < 0.1$, the device is in weak inversion.
- For $IC > 10$, the device is in strong inversion.
- For $0.1 < IC < 10$, the device is in moderate inversion.

A.3 Transconductances and Charges

Drain current can be rewritten with respect to drain, source, and gate voltage, according to (A.16).

$$\begin{aligned} \Delta I_D &= \frac{\partial I_D}{\partial V_S}\Delta V_S + \frac{\partial I_D}{\partial V_G}\Delta V_G + \frac{\partial I_D}{\partial V_D}\Delta V_D = \\ &= -g_{ms}\Delta V_S + g_m \Delta V_G + g_{md}\Delta V_D \end{aligned} \tag{A.16}$$

g_{ms}, g_m and g_{md} are the source, gate and drain transconductances, respectively, given by (A.17).

$$g_{ms} = -\frac{\partial I_D}{\partial V_S}, \quad g_m = \frac{\partial I_D}{\partial V_G}, \quad g_{md} = \frac{\partial I_D}{\partial V_D} \tag{A.17}$$

Relations between drain and source transconductances and normalized inversion charges are expressed in (A.18) [234]. G_{spec} is a normalization quantity, given as the ratio of specific current to thermal voltage (A.19). g_m is expressed as a function of g_{ms} and g_{md}, according to (A.20). In saturation, where $I_R << I_F$, and hence $g_{md} << g_{ms}$, (A.20) simplifies to $g_m = g_{ms}/n$.

$$g_{ms(d)} = G_{spec} q_{s(d)} \tag{A.18}$$

$$G_{spec} = \frac{I_{spec}}{U_T} \tag{A.19}$$

$$g_m = \frac{g_{ms} - g_{md}}{n} = \frac{G_{spec}}{n}(q_s - q_d) \tag{A.20}$$

A.4 Capacitances and Charges

Relations among intrinsic capacitances and normalized inversion charges are extensively presented in [234]. The general expressions for gate-source, gate-drain, gate-bulk, bulk-source and bulk-drain normalized capacitances, valid in all inversion regions are given below. The total gate capacitance, is then derived by (A.26).

$$c_{GSi} = \frac{q_s}{3}\frac{2q_s + 4q_d + 3}{(q_s + q_d + 1)^2} \tag{A.21}$$

$$c_{GDi} = \frac{q_d}{3}\frac{2q_d + 4q_s + 3}{(q_s + q_d + 1)^2} \tag{A.22}$$

$$c_{GBi} = \frac{n-1}{n}(1 - c_{GSi} - c_{GDi}) \tag{A.23}$$

$$c_{BSi} = (n-1)c_{GSi} \tag{A.24}$$

$$c_{BDi} = (n-1)c_{GDi} \tag{A.25}$$

$$c_{GI} = c_{GSi} + c_{GDi} + c_{GBi} \tag{A.26}$$

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Curriculum Vitae

Angelos Antonopoulos

Date of Birth	31 May 1981
Nationality	Greek
Contact Details	*aanton@electronics.tuc.gr* *www.electronics.tuc.gr*

Work Experience

2008-2014	Doctoral Assistant, ECE Dept., Technical University of Crete
2010-2014	Researcher, Telecommunications Systems Institute, Technical University of Crete
2006-2013	Teaching Assistant (Electronics II, Analog CMOS Design), ECE Dept., Technical University of Crete

Education

2007–2010	MSc. ECE Dept. Technical University of Crete. Thesis: "System Level Analysis of a Direct Conversion WiMAX Receiver and Corresponding Mixer Design"
2000-2005	M. Eng. ECE Dept., Technical University of Crete. Grade: 8.02/10

Technical & Computer Skills

TECHNICAL SKILLS:	RFIC Design and modeling of advanced CMOS technologies On-wafer measurements. DC, CV and RF setup and measurements. RF noise measurements
COMPUTER SKILLS:	Experienced user of Linux distributions (Ubuntu and Suse). Cadence IC and Spectre. ADS and ICCAP. Matlab. Dolphin Smash. Administrative duties for Cadence and Agilent Products. Co-administrator (2006 to now) of license server hosting licenses for Cadence and Agilent's products

Scholarships & Distinctions

09/2011–08/2013	Heracleitus II program co-financed by the European Social Fund (ESF) and Greek national funds, through the operational program "Education and Lifelong Learning", within the National Strategic Reference Framework (NSRF)
2001	Scholarship for one out of three highest grades during the 1st year of studies

Language Skills

FLUENT:	English
BASICS:	French
MOTHER TONGUE:	Greek

Personal Interests

Sports, cinema, LyX-ing

Publications

Journals

1. **A. Antonopoulos**, M. Bucher, K. Papathanasiou, N. Mavredakis, N. Makris, R. K. Sharma, P. Sakalas, M. Schroter, "CMOS Small-Signal and Thermal Noise Modeling at High Frequencies", IEEE Trans. Electron Devices, Vol. 60, No. 11, pp. 3726-3733, November 2013.

2. **A. Antonopoulos**, M. Bucher, K. Papathanasiou, N. Makris, N. Mavredakis, R. K. Sharma, P. Sakalas, M. Schroter, "Modeling of High Frequency Noise of Silicon MOS Transistors for RFIC Design", International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, special issue on Modeling of high-frequency silicon transistors, in press.

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