Analysis of radiation effects in CMOS technology at high Total Ionizing Dose (TID)

Diploma thesis by
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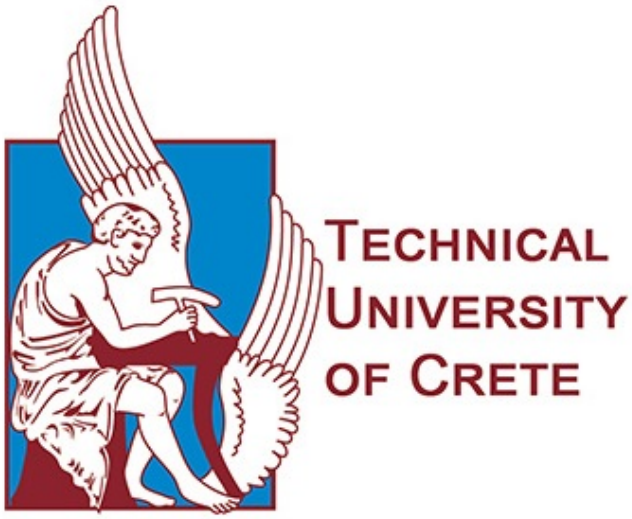

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Ευχαριστίες

Θα ήθελα να ευχαριστήσω αρχικά, τον επιβλέπων καθηγητή μου, Ματιάς Μπούχερ που μου εμπιστεύθηκε το θέμα της διπλωματικής και για την καθοδήγηση του πάνω σε αυτό, καθώς και τους δύο καθηγητές κ. Καλαϊτζάκη και κ. Μπάλα που ήταν στην επιτροπή. Επίσης θα ήθελα να ευχαριστήσω τους μεταπτυχιακούς φοιτητές του εργαστηρίου, τον Άρη, την Αλεξία, το Λουκά και τον Άγγελο για την βοήθεια μου προσέφεραν και για τη φιλοξενία στο εργαστήριο όλο αυτό το διάστημα. Για τη βοήθεια τους με τη LaTeX και το κείμενο τον αδερφό μου, τον Έκτορα, το Βασίλη τον Κώστα και την Αγγελική.

Η παρούσα διπλωματική εργασία για εμένα αποτέλεσε την τελευταία πράξη της φοιτητικής μου ζωής στα Χανιά. Βλέποντας λοιπόν την παράσταση να τελειώνει δε θα μπορούσα να μην ευχαριστήσω αυτούς που συνέβαλαν με τον τρόπο τους στη διαμόρφωση αυτού που είμαι σήμερα. Ευχαριστώ τους φίλους μου, τους παιδικούς αλλά και αυτούς που γνώρισα στα Χανιά. Αυτούς της γενιάς του 92, τους μεγαλύτερους και τους μικρότερους.

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Ευχαριστώ την Ενωτική Πρωτοβουλία, τους συντρόφους μου που μου έμαθαν και μου μαθαίνουν τι θα πει συλλογικότητα και στη ζωή μου να μη σκύβω ποτέ το κεφάλι.

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Abstract

In the last decade a number of applications in environments with high ionizing radiation have been developed worldwide. Applications span medical technology equipment to space applications and high energy physics experiments such as the Large Hadron Collider (LHC). These have brought many significant scientific achievements that can impact the evolution of mankind. To enable further development, the optimization of electronics in these applications is of great importance.

It could be said that this constitutes the springboard of many studies and experiments about high ionizing radiation impact in CMOS technology, which is prevalent in electronic circuit design.

This thesis, which attempts to contribute to this field, is related to research by CERN, the European organization of Nuclear Research. It is based on experimental data acquired at CERN, comprising measured electrical characteristics of MOSFETs exposed to X-rays up to very high Total Ionizing Dose (TID). Specific methods for the extraction of electrical parameters of different transistor geometries and under increasing levels of TID have been implemented. These parameters are important for both digital and analog integrated circuit design. A simple modelling approach is proposed to evaluate the high dose effects for different geometries and levels of TID. Evaluations show different impact of high TID on nMOS and pMOS devices. This research provides new insight into geometry-related TID effects in the examined CMOS technology, and the developed models and parameters are shown to be suitable for estimating geometry-dependent TID effects.

Περίληψη

Την τελευταία δεκαετία, έχουν αναπτυχθεί παγκοσμίως ένα πλήθος από εφαρμογές που λειτουργούν σε συνθήκες υψηλού επιπέδου ιονίζουζας ακτινοβολίας. Οι περιοχές εφαρμογών εκτείνονται από βιοϊατρικό εξοπλισμό μέχρι διαστημικές εφαρμογές και πειράματα φυσικής υψηλής ενέργειας, όπως ο Μεγάλος Επιταχυντής Αδρονίων (Large Hadron Collider - LHC). Αυτές οι εφαρμογές έχουν επιφέρει πολλά επιστημονικά επιτεύγματα, τα οποία μπορούν να έχουν σημαντικές επιπτώσεις στην εξέλιξη της ανθρωπότητας. Για την επιδίωξη περεταίρω ανάπτυξης αυτών καθώς και καινούριων εφαρμογών, η βελτίωση των ηλεκτρονικών σε τέτοιες συνθήκες είναι μείζονος σημασίας.

Το παραπάνω αποτελεί το εφαλτήριο πολλών ερευνών και πειραμάτων σχετικά με την επίδραση υψηλής ιονίζουσας ακτινοβολίας σε τεχνολογία CMOS, η οποία είναι η κυρίαρχη στη σχεδίαση ηλεκτρονικών κυκλωμάτων.

Η παρούσα διπλωματική, η οποία επιδιώκει να συμβάλει σε αυτό το πεδίο, σχετίζεται με την έρευνα του CERN, τον Ευρωπαϊκό Οργανισμού Πυρηνικών Ερευνών. Βασίζεται σε δεδομένα που προκύπτουν από πειράματα που διεξάγονται στο CERN, τα οποία περιλαμβάνουν μετρήσεις ηλεκτρικών χαρακτηριστικών MOSFET, τα οποία εκτίθενται σε ακτίνες X (X rays) σε πολύ υψηλή συνολική ιονίζουσα δόση (Total Ionizing Dose - TID). Υλοποιούνται συγκεκριμένες μέθοδοι για την εξαγωγή ηλεκτρικών παραμέτρων τρανζίστορ διαφορετικών γεωμετριών και κάτω από την επίδραση αυξανόμενων επιπέδων συνολικής ιονίζουσας δόσης. Οι εξεταζόμενοι παράμετροι είναι σημαντικοί για ψηφιακή καθώς και αναλογική σχεδίαση ολοκληρωμένων κυκλωμάτων. Μία προσέγγιση με απλό μοντέλο προτείνεται για την εκτίμηση των επιπτώσεων της υψηλής ακτινοβολίας σε συνάρτηση με την γεωμετρία και το επίπεδο TID. Οι εκτιμήσεις δείχνουν διαφορετική επίδραση της υψηλής ακτινοβολίας σε τρανζίστορ τύπου nMOS και pMOS. Αυτή η έρευνα προσφέρει καινούρια στοιχεία σχετικά την επίδραση της ακτινοβολίας στην εξέταση διαφορετικών γεωμετριών της εν λόγω τεχνολογίας. Τα μοντέλα και οι παράμετροί τους αποτιμούνται χρήσιμα στην εκτίμηση της ιονίζουσας ακτινοβολίας σε διαφορετικές γεωμετρίες και επίπεδα TID.

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Chapter 1

Introduction

1.1 MOSFET Devices

MOSFET (Metal Oxide Semiconductor – Field Effect Transistor) transistors were introduced in the decade of 1960 and today CMOS (Complementary Metal Oxide Semiconductor) technology (combination of nMOS and pMOS transistors in circuits) is dominant in the area of semiconductors, since it covers more than 90% of analog and digital integrated circuits.

MOSFETs contain four terminals, where the voltage supply is applied, namely the Gate (G), the Drain (D) and Source (S), as well as the "bulk" or the "body" (B). Two complementary types of transistors exist, namely nMOSFETs and pMOSFETs, according to the type of the doping of the semiconductor channel.

An nMOSFET is fabricated in a p-type substrate, which is the "bulk", or possibly a local p-type well. Two heavily–doped n+ regions form the Source and Drain terminals. A heavily–doped (conductive) piece of polysilicon (poly-cristalline silicon, often simply called "poly") operates as the Gate, which is separated from the channel by a thin layer of silicon dioxide (SiO2) insulating the Gate from the substrate. The useful action of the device occurs in the channel region under the Gate oxide, which can vary from a state with very low conductance (off-state) to high conductance (on-state). The structure is symmetric with respect to Source and Drain terminals.

The semiconductor path between Drain and Source terminals constitutes the channel of the transistor. The dimension of the Gate terminal along the channel is called channel's length (L) and that perpendicular to the length is called channel's width. In figures 1.1 and 1.2 the structure of an nMOS transistor is depicted.

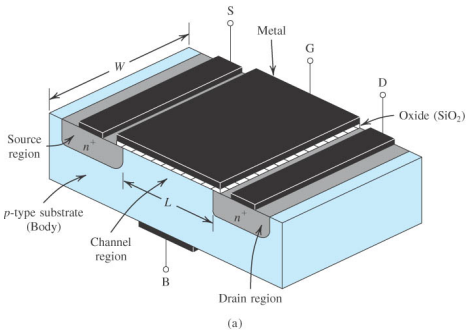

Figure 1.1 3D depiction of an nMOS structure

The operation of MOS transistors is characterized as a charge-controlled device. According to voltages applied at the terminals, mobile charges are created in the channel. These are then used to create channel current.

For a voltage supply of 0V at the Gate terminal, the channel is depleted of mobile charges. The current flow from drain to source is prevented by the p-n junctions (drain-substrate, source-substrate), which operate as two diodes. In an nMOS transistor, as V_G increases, the holes in p-substrate (electrons in n-substrate for pMOS) are repelled from the gate area leaving negative ions behind so as to mirror the charge on the Gate. So, a depletion region is created. No mobile charges are available to create channel current. The device channel is in "off"-state.

With the increase of V_G, the width of the depletion region increases and so does the potential at the oxide-silicon interface. Eventually, a small amount of electrons in nMOS form a weakly inverted channel. When applying a certain voltage among drain and source, a channel current results, where electrons are supplied by the Source, flow through the channel, and are eventually absorbed at the Drain. The device operates in the weak inversion or subthreshold region. When V_G reaches a sufficiently positive value, a strongly inverted channel is formed. From this point the channel is in “on”-state. At low values of V_{DS}, the transistor operates in the linear mode. When increasing V_{DS}, the mobile charge at the drain end decreases, resulting in increased channel current. For higher values of V_{DS} and after a specific value ($V_{D,SAT}$) the channel is pinched-off at the drain. A further increase of V_{DS} then leaves the channel current unchanged, and the transistor operates in saturation mode. In pMOS devices, holes instead of electrons form the mobile charges, when negative gate voltage is applied.

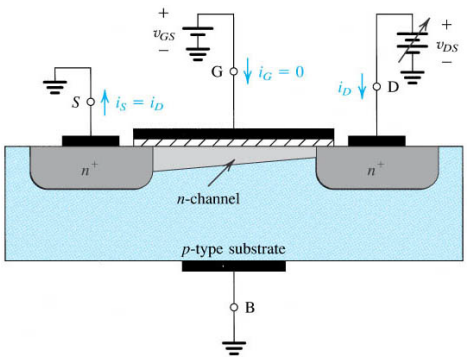

Figure 1.2 depiction of an nMOS structure voltage supply

1.2 Radiation

Initially, levels of radiation will be discussed, so that it will be better understood which radiation levels this thesis is occupied with.

Radiation is separated in ionizing and non-ionizing types. The type of radiation that this thesis is occupied with, belong to the first group.

Non-ionizing radiation includes different types, from very low radiation levels such as from led light, infrared, lasers, WI-FI, cell phones to higher radiation levels such as microwave ovens, radio, sunlight (UVA rays, IR-A, IR-B, IR-C). Ultraviolet radiation is considered as a non-ionizing radiation, at the most of its stages, such as UVA, UVB, UVC, near and middle ultraviolet. These radiation levels have as a result sunburns and melanoma but also increase of vitamin D. Additionally, non-ionizing radiation is separated in non-thermal, thermal and optical.

The main characteristic of ionizing radiation is that in atom particles after the exposure to it, electrons are liberated and removed from the particle and so, ions are created. In other words, ionizing radiation is the radiation which carries enough energy to result in a loss of electrons. There are not specific values which designate whether a radiation is ionizing or not because it depends on the material it will be applied on. In this group, radiations that are included are X-rays, Gamma-rays, highest ultraviolet radiation. Except the lowest levels which can be found in medical applications, ionizing radiation exposure is very dangerous to humans and other living creatures.

The unit that is used for ionizing radiation in SI (International System of Units) is grey (Gy) which is defined as the absorption of joules of energy per kilograms of matter (1J / kg). Also in SI another unit for ionizing radiation is Sieverts (Sv), which is mainly used for health effect of ionizing radiation and its ration over Grey is 1. This study's data for Total Ionizing Dose absorption are measured in Rad (Rad), which is defined as ergs of energy per grams of matter (erg/gr) and its relation with Grey unit is 1 Gy = 100 Rad.

Other characteristic samples of ionizing radiation more specific:

- dental X-ray (0.01 mGr, 1 mRad)
- chest X-ray (0.1 mGr, 10 mRad)
- Annual exposure for a human (2.4mGr, 0.24 Rad)
- Abdominal X-ray (4 mGr, 0.4 Rad)
- Full body CT scan (10 mGr, 1 Rad)
- Exposure to Chernobyl residents during the explosion (350 mGr, 35 Rad)
- Exposure to Chernobyl workers who died in one month (6 Gr, 600 Rad)

The data that this study is occupied have been exposed to X-rays and the measurements refer to Total Ionizing Dose (TID) which is the cumulative radiation that our devices has been exposed to. These levels fluctuate between 100 Mrad and 500 Mrad. These high TID levels may be encountered for electronics in Large Hadron Colliders (LHC) on long term experiments spanning many years of operation.

1.3 Radiation effect on MOSFET physical structure

A large number of application specific integrated circuits (ASICs) will be needed in the upgraded detector systems where they will be exposed to very high levels of radiation. Experimental needs reach to TID levels of 100, 300 and even 500 Mrad and even higher, that MOSFET devices are exposed to.

The main impact of ionizing radiation, takes place when energy deposited in a semiconductor or in insulating layers, chiefly SiO_2, frees charge carriers (electron-hole pairs), which diffuse or drift to other locations where they may get trapped, leading to unintended concentrations of charge and parasitic fields. This kind of damage is the primary effect of exposure to X and gamma-rays and charged particles.

Effects of radiation on MOSFET devices can be either Total dose effects or Single event effects. Total dose effects consist to the progressive build-up of trapped charge in insulating layers or at the Si/SiO_2 interface (as a consequence of ionization phenomena) or of defects in the bulk of the devices (originating from accumulation of displacement events). Single event dose effects are due to charge deposition induced by a single particle that crosses a sensitive device region. The effects may lead to destructive or non-destructive damage of the device.

Also, a MOSFET exposed to an ionizing radiation environment, typically suffers degradation in one or more of its parameters (threshold voltage, gate voltage to drain current gain, or transconductance, channel leakage, noise). Changes may not be constant with time after irradiation and may

depend on the dose rate. An integrated CMOS circuit may slow down, show higher leakage (parasitic) currents, or even cease functioning properly (catastrophic failure). Damage responsible for these total dose effects occurs in the insulating layers (SiO_2) of the device structures and at the interface between the silicon substrate of the device and the oxide, and consists of three components:

1. buildup of (positive) charge trapped in the oxide (the gate oxide and/or the field oxide, used to isolate devices from each other).
2. increase in the number of interface traps.
3. increase in the number of traps in the oxide bulk.

In the physical structure of a MOSFET device under TID leakage currents are observed. In an nMOS device, positive charge trapping (negative for pMOS) in the field oxide due to ionizing radiation can invert the underlying P doped region and form an N-type conducting channel between the source and drain terminals, therefore increasing the drain leakage current.

Further research and studies have demonstrated which impact radiation has on the MOSFET physical structure. As is presented in [1] [2], an impact of radiation on narrow channel transistors, both pMOS and nMOS, is the charge trapping in the lateral shallow trench isolation oxide (STI), which is more intense in narrow channel transistors. According to [3] and the above research there is also impact of radiation on the spacer oxide of the devices and mainly in pMOS structures.

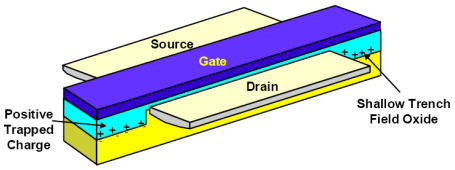

Figure 1.3 Depiction of trapped charges in an nMOS structure

Furthermore, with the contribution of the above, it is observable, that radiation impacts the thin gate oxide too. This impact on the transistors oxides leads to macroscopic effects such as source-drain or inter-diffusion leakage currents, ultimately limiting the radiation tolerance of conventional CMOS circuits.

Holes trapped in the SiO_2 of an MOS structure are not truly permanently trapped. Actually, they are observed to disappear from the oxide over times from milliseconds to years. This discharge of the hole traps, commonly observed near room temperature, is the major contributor to the so-called long-term annealing of radiation damage in MOS devices.

There are several techniques of MOSFET transistor design, which have as purpose the limitation of TID impact on the devices. A result of them is the thinning of gate oxides of transistors used for radiation applications. Characteristic example are Hardness-by-design (HBD) layout techniques, which constitute a widespread and recognized subject internationally. In [4] can be found successful examples of HBD in 250nm and 180nm nodes.

The measurements, on which this study was based were performed at CERN in an X-ray irradiation cabinet for total dose testing and the devices has been exposed under 8,8 Mrad/h as referred in [10][8] Specifically, about exposure time of the levels that this study examines:

- 100 Mrad TID - 11 hous 22 minutes and 36 seconds
- 300 Mrad TID - 34 hours 5 minutes and 24 seconds
- 400 Mrad TID - 45 hours 27 minutes and 16 seconds
- 500 Mrad TID - 56 hours 49 minutes and 5 seconds

As referred in [9] about the setup of the measurements, the equipment that has been used contains:

- X-ray irradiation system (SEIFERT RP149), in which a 3 kW X-ray tube uses a tungsten target typical of radiation effects studies on semiconductors.
- Semiconductor parameter analyzer (HP 4145B) performs the static transistor measurements, applying and measuring currents and/or voltages (typically, is measured as a function of V_{GS} and V_{DS})
- Voltage source to keep the transistors under bias (V_{GS} = V_{DS} = 1.2V for nMOS, V_{GS} = V_{DS} = -1.2V for pMOS) during the irradiation and annealing steps.
- Temperature control system. For the present work, temperature during irradiation and test is kept at 25 deg. C.
- Keithley 707 switching matrix connects the measuring channels of the HP 4145B, or the output of the voltage source, to the appropriate pads in the TID structure

In the figures below, the equipment of the measurements (1.4) and the placement of the testchip, in the probe station is depicted (1.5).

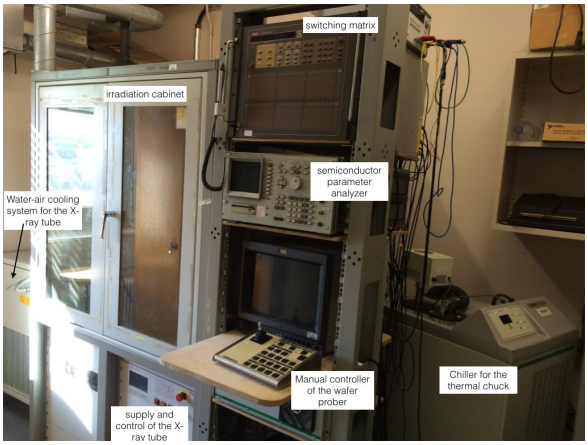

Figure 1.4 Scheme of Irradiation and Measurement Setup from CERN EP-ESE

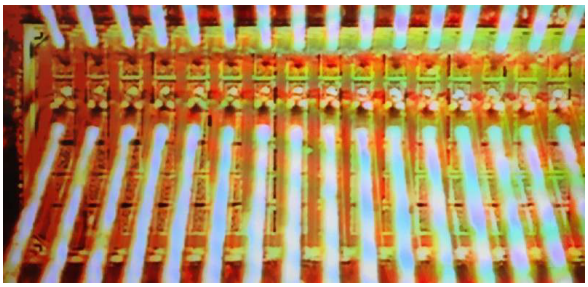

Figure 1.5 Test chip under measurement probes

Chapter 2

The data of the research

This study has been based on measurements of a number of MOS transistors of a commercial 65nm CMOS technology with nominal oxide thickness and standard threshold Voltage. The measurements were performed at CERN and contain transfer and output characteristics of nMOS and pMOS devices with different geometries. These regard to drain current of each device after a specific Voltage supply on gate terminal. Measurements have been taken in linear mode and in saturation. Voltage on drain terminal is constant for all the devices and equal to 0.02V in linear mode for nMOS devices and -0.02 for pMOS devices. Constant is also the drain Voltage in saturation mode and equal to 1.2V for nMOS structures and -1.2 for pMOS structures.

Also, each measurement has been taken under different conditions according to the Total Ionizing Dose (TID) the device is subject to. The radiation levels examined, except the Pre-rad condition (0 rad), are 100 Mrad, 300 Mrad, 400 Mrad, and 500 Mrad.

Specifically, the transistors of this study are presented in table 2.1 and figure 2.1 below, the devices according to their channel sizes are opposed.

L	W	Structure	TID(Mrad)	Structure	TID(Mrad)
60nm	120nm	nMOS	0,100,300,500	–	–
60nm	240nm	nMOS	0,100,300,500	pMOS	0,100,400
60nm	360nm	nMOS	0,100,300,500	pMOS	0,100,400
60nm	480nm	nMOS	0,100,300,500	pMOS	0,100,400
60nm	600nm	nMOS	0,100,300,500	pMOS	0,100,400
60nm	1um	nMOS	0,100,300,500	pMOS	0,100,400
10um	120nm	nMOS	0,100,400	pMOS	0,100,400
10um	240nm	nMOS	0,100,400	pMOS	0,100,400
10um	360nm	nMOS	0,100,400	pMOS	0,100,400
10um	480nm	nMOS	0,100,400	pMOS	0,100,400
10um	600nm	nMOS	0,100,400	pMOS	0,100,400
10um	1um	nMOS	0,100,400	pMOS	0,100,400
10um	4um	nMOS	0,100,400	pMOS	0,100,400
10um	10um	nMOS	0,100,400	pMOS	0,100,400
120nm	1um	nMOS	0,100,300,500	pMOS	0,100,400
240nm	1um	nMOS	0,100,300,500	pMOS	0,100,400
360nm	1um	nMOS	0,100,300,500	pMOS	0,100,400
480nm	1um	nMOS	0,100,300,500	pMOS	0,100,400
800nm	1um	nMOS	0,100,300,500	pMOS	0,100,400
1um	1um	nMOS	0,100,300,500	pMOS	0,100,400
10um	1um	nMOS	0,100,300,500	pMOS	0,100,400
60nm	20um	nMOS	0,100,400	pMOS	0,100,400
120nm	20um	nMOS	0,100,400	pMOS	0,100,400
240nm	20um	nMOS	0,100,400	pMOS	0,100,400
600nm	20um	nMOS	0,100,400	pMOS	0,100,400
1um	20um	nMOS	0,100,400	pMOS	0,100,400
10um	20um	nMOS	0,100,400	pMOS	0,100,400

Table 2.1 Dimensions and structure of the devices

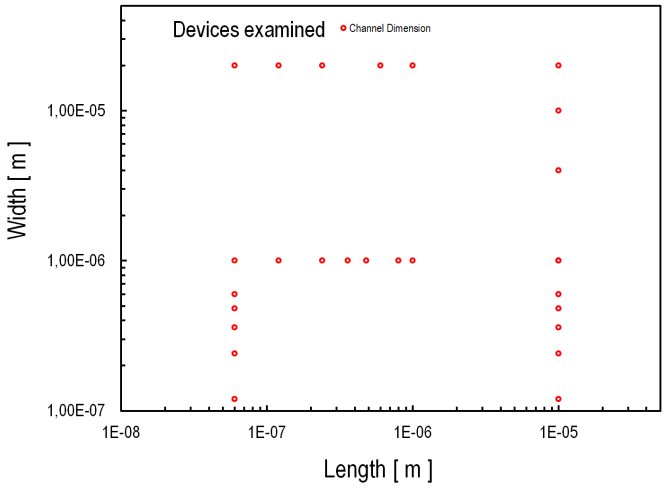

Figure 2.1 Depiction of devices on a diagram according their channel dimensins

In figures 2.2, 2.3, 2.4, 2.5 $I_D - VG$ and $ID - VD$ characteristics are presented for an nMOS, L=60nm, W=120nm transistor at different TID levels. From these, the operation of the devices through different TID levels.

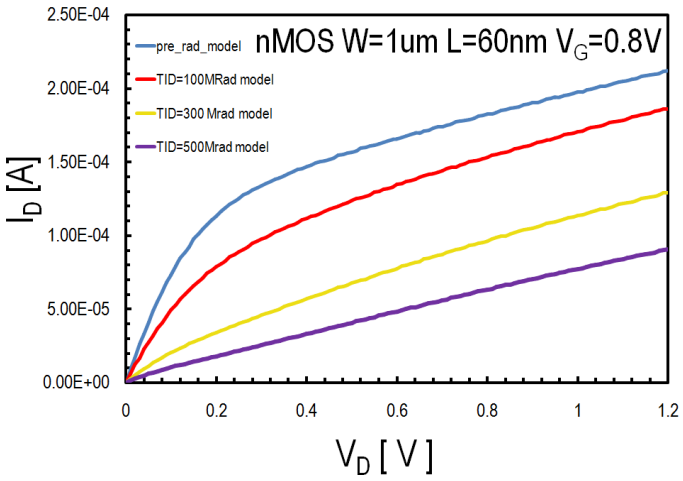

Figure 2.2 $I_D - V_D$ characteristic for nMOS,L=60nm, W=1um under four TID levels (0Mrad, 100Mrad, 300Mrad, 500Mrad), V_G=0.8V

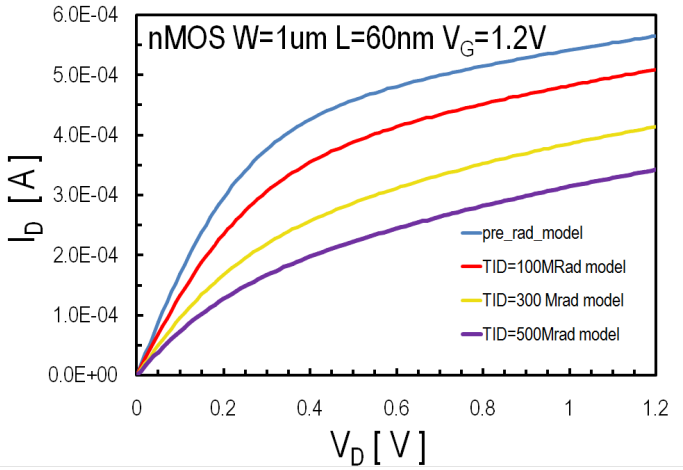

Figure 2.3 $I_D - V_D$ characteristic for nMOS,L=60nm, W=1um under four TID levels (0Mrad, 100Mrad, 300Mrad, 500Mrad), V_G=1.2V

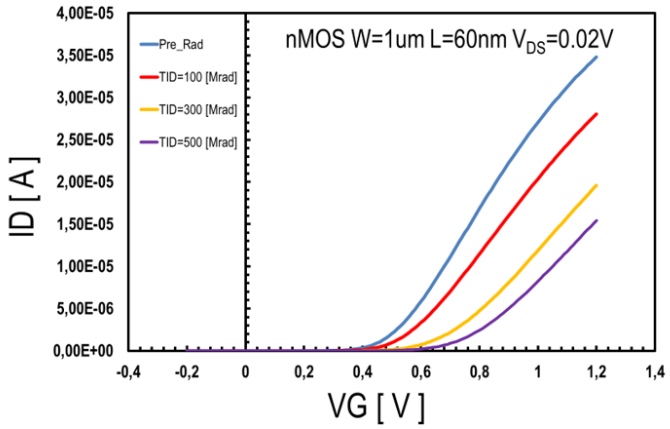

Figure 2.4 $I_D - V_G$ characteristic for nMOS,L=60nm, W=1um under four TID levels (0Mrad, 100Mrad, 300Mrad, 500Mrad), linear mode

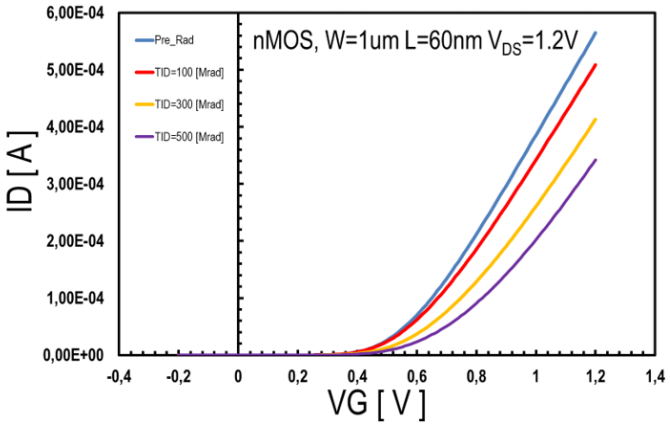

Figure 2.5 $I_D - V_G$ characteristic for nMOS,L=60nm, W=1um under four TID levels (0Mrad, 100Mrad, 300Mrad, 500Mrad), saturation mode

Chapter 3

Purpose of research

From the measurements that have been received, as described above, several parameters have been extracted: Threshold Voltage, Slope factor and Mobility in linear and saturation mode for each one of the devices and for each TID level. The extraction of the three parameters is described in the next chapter of the thesis.

The examination of the three parameters has been done on Width scaling and Length scaling for both nMOS and pMOS structures. Length scaling is examined on geometries with W=1um and W=20um and the lengths that were studied fluctuate between 60nm and 10um. Width scaling is examined on geometries with L=60nm and L=10um and the widths range from 120nm to 10um. Note that lengths and widths scaling do not cover the whole specter that has been referred above. In the tables below, the devices which were used for width scaling and length scaling procedures are presented.

L	W	Structure
60nm	1um	nMOS,pMOS
120nm	1um	nMOS,pMOS
240nm	1um	nMOS,pMOS
360nm	1um	nMOS,pMOS
480nm	1um	nMOS,pMOS
800nm	1um	nMOS,pMOS
1um	1um	nMOS,pMOS
10um	1um	nMOS,pMOS
60nm	20um	nMOS,pMOS
120nm	20um	nMOS,pMOS
240nm	20um	nMOS,pMOS
600nm	20um	nMOS,pMOS
1um	20um	nMOS,pMOS
10um	20um	nMOS,pMOS

L	W	Structure
60nm	120nm	nMOS
60nm	240nm	nMOS,pMOS
60nm	360nm	nMOS,pMOS
60nm	480nm	nMOS,pMOS
60nm	600nm	nMOS,pMOS
60nm	1um	nMOS,pMOS
10um	120nm	nMOS,pMOS
10um	240nm	nMOS,pMOS
10um	360nm	nMOS,pMOS
10um	480nm	nMOS,pMOS
10um	600nm	nMOS,pMOS
10um	1um	nMOS,pMOS
10um	4um	nMOS,pMOS
10um	10um	nMOS,pMOS

Table 3.1 Table of devices studied for length (left) and width (right) scaling

Chapter 4

Parameter Extraction

In this section the process that has been followed to extract each one of Threshold Voltage, Slope Factor, Mobility and a factor based on DIBL from the measurements of voltage supply and Drain current is described.

4.1 Threshold Voltage extraction

Threshold Voltage of a MOS transistor is defined as the value of the minimum Gate Voltage for which the channel between Drain and Source is "turned on", so there is communication between the source and drain terminals by electrons for nMOS (holes for pMOS) in the channel. Threshold Voltage for zero Source Voltage is called V_{TO}. In this study, since Source Voltage is zero the extracted threshold Voltage is specifically V_{TO}.

There are several methods for the extraction of threshold voltage. The method that has been chosen for the extraction of V_{TH} in this thesis is a constant current method, which is interpreted in [7] and also referred in [6]. According to the method above, a constant current($I_{contant}$) is considered and multiplied with $\frac{W}{L}$. The product of this relation is specific current (I_{spec}). From the equation below (5.1) comes out a drain current.

$$I_{spec} = I_{constant} \cdot \frac{W}{L} \tag{4.1}$$

From the measurements of drain current and gate voltage, the gate voltage that corresponds at the drain current value, is the threshold voltage of the transistor examined. This I_{spec} value is equal to the drain current, the corresponding gate Voltage supply of which is the threshold Voltage of the device. For the values of I_{spec} that there were not in the I_D measurements, the respective gate Voltage and by extension the threshold Voltage was calculated with an interpolation procedure.

In figure 4.1 is presented a part of the I_D-VG characteristic of a short nMOS transistor in pre-rad, 100Mrad, 300Mrad and 500Mrad conditions and in linear mode. It is shown that the influence of TID degrades the I_D and the V_{TH} value is bigger as the TID increases. More specifically in pre-rad condition V_{TH}= 0.67V, under 100Mrad V_{TH}= 0.69V, under 300Mrad V_{TH}=0.77V and under 500Mrad V_{TH}=0.82V.

In figure 4.2 is presented a part of the I_D-VG characteristic of the short nMOS transistor in the same four TID levels as above. It is observed that the drain current values are higher than these in linear mode and the threshold Voltage values are lower. More specifically, in pre-rad condition V_{TH}=0.45V, under 100Mrad V_{TH}=0.46, under 300Mrad V_{TH}=0.502V and under 500Mrad V_{TH}=0.542. At this point it should be noted that for the study of threshold Voltage in pMOS devices the absolute value has been used. The reason is that V_{TH} values in pMOS are negative and the above conversion facilitates the comparison between nMOS and pMOS devices.

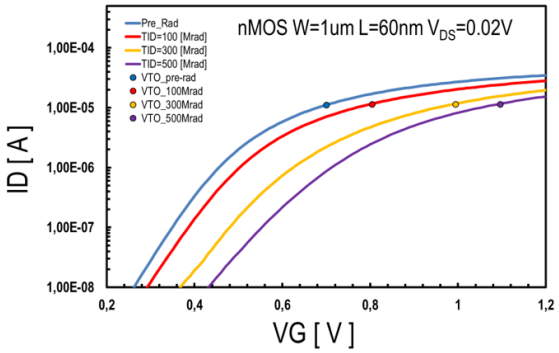

Figure 4.1 I_D-VG characteristic in four TID levels (0 Mrad, 100 Mrad, 300 Mrad, 500 Mrad), with marked VTH for every level for W=1um, L=120nm, nMOS transistor, linear mode.

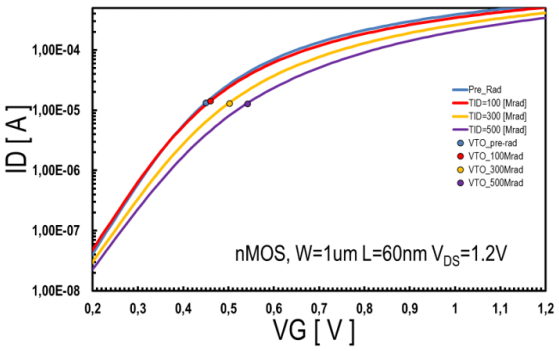

Figure 4.2 $I_D - V_G$ characteristic in four TID levels (0 Mrad, 100 Mrad, 300 Mrad, 500 Mrad), with marked V_{TH} for every level for W=1um, L=600nm, nMOS transistor, saturation mode.

4.2 Slope Factor extraction

Slope factor could be defined as the inverse slope of the $I_D - V_G$ characteristic (I_D logarithmic scale) in the subthreshold region.

The value of the normalized transconductance to current ratio versus normalized current curve in weak inversion is $\frac{1}{n}$. The minimum value of slope factor is 1 and the maximum is approximately 2. For the extraction of slope factor the following equation 5.2 was used, which is also the equation which defines g_m:

$$g_m = \frac{dI_D}{dV_{GS}} \tag{4.2}$$

Also the relation 5.3 below:

$$max(\frac{g_m}{I_D} \cdot U_T) = \frac{1}{n} \tag{4.3}$$

From the application of the two above relations over the I_D data, slope factor (n) is extracted.

In figures 4.3 and 4.4 the (gm/I_D)UT - I_D characteristics of a short channel nMOS transistor for the four different TID levels are examined. On the max value of each characteristic is the max value of 1/n at every TID level. It is observed that its value reduces after the radiation influence, so the slope factor (n), increases during the increase of TID.

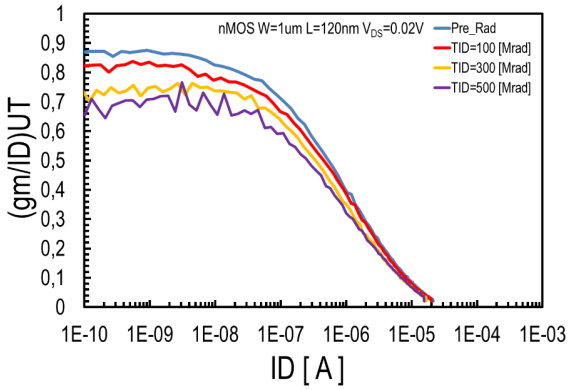

Figure 4.3 $(\frac{g_m}{I_D}) \cdot U_T$ - I_D characteristic in four TID levels (0 Mrad, 100 Mrad, 300 Mrad, 500 Mrad), for every level for W=1um, L=120nm, nMOS transistor, linear mode.

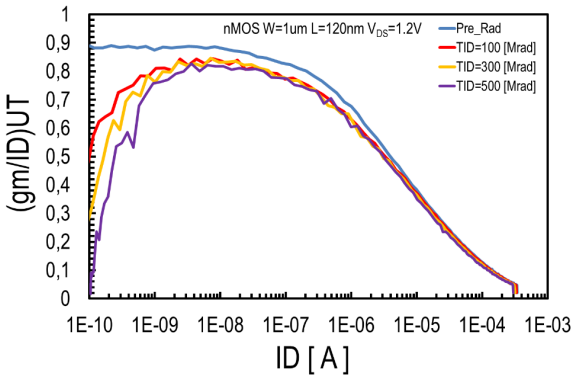

Figure 4.4 $(\frac{g_m}{I_D}) \cdot U_T$ - I_D characteristic in four TID levels (0 Mrad, 100 Mrad, 300 Mrad, 500 Mrad), for every level for W=1um, L=120nm, nMOS transistor, saturation mode.

4.3 Mobility extraction

Carrier mobility (μ), in MOSFET transistors is a factor which refers to the mobility of electrons and holes in the channel between Drain and Source terminals. Mobility extraction from measurements of drain current (I_D) and gate voltage (V_G) that were received was a procedure that was not the same in linear and in saturation mode. This is because the equation that contains mobility (μ) is different in linear and in saturation mode.

Extracting mobility in linear mode

For linear mode the equation that has been used is the following 5.4:

$$I_D = \beta \cdot [V_G - V_{TO} - \frac{n}{2} \cdot (V_D + V_S)] \cdot (V_D - V_S) \tag{4.4}$$

Applying the derivative of V_G over I_D the result is 5.5:

$$\frac{dI_D}{dV_G} = \beta \cdot (V_D - V_S) \tag{4.5}$$

Also 5.6:

$$\beta = \mu \cdot C'_{ox} \cdot \frac{W}{L} \tag{4.6}$$

From the above, the initial equation becomes 4.7:

$$\frac{dI_D}{dV_G} = \mu \cdot C'_{ox} \cdot \frac{W}{L} \cdot V_{DS} \tag{4.7}$$

Solving for mobility 4.8:

$$\mu = \frac{dI_D}{dV_G} \cdot \frac{1}{C'_{ox} \cdot V_{DS}} \cdot \frac{L}{W} \tag{4.8}$$

Using the last equation above mobility in linear mode is extracted for the transistors examined.

Extracting mobility in saturation mode

In saturation mode the equation 4.8 above exist:

$$I_D = \frac{\beta}{2n} \cdot [V_G - V_{TO} - n \cdot V_S]^2 \tag{4.9}$$

Afterwards, applying square root on both sides and the fact that V_S=0 gives 4.10:

$$\sqrt{I_D} = \sqrt{\frac{\beta}{2n}} \cdot (V_G - V_{TO}) \tag{4.10}$$

Applying the derivative of VG over the square root of I_D, so the equation becomes 4.11:

$$\frac{d\sqrt{I_D}}{dV_G} = \sqrt{\frac{\beta}{2n}} \tag{4.11}$$

Raising to the power 2 both sides and replacing β as in linear mode has as a result the below 4.12:

$$(\frac{d\sqrt{I_D}}{dV_G})^2 = \frac{\mu \cdot C'_{ox} \cdot \frac{W}{L}}{2n} \tag{4.12}$$

And rearranging the equation for mobility redounds to the following relation 4.13:

$$\mu = (\frac{d\sqrt{I_D}}{dV_G})^2 \cdot \frac{2n}{C'_{ox}} \cdot \frac{L}{W} \tag{4.13}$$

Mobility in saturation mode has been extracted according to the last equation.

In the figures 4.5 and 4.6 the characteristics of the corresponding derivative for linear and saturation respectively are shown, that has been used for the equations above for the extraction of mobility. In the figures the max points are marked, which are the values that have entered the equations.

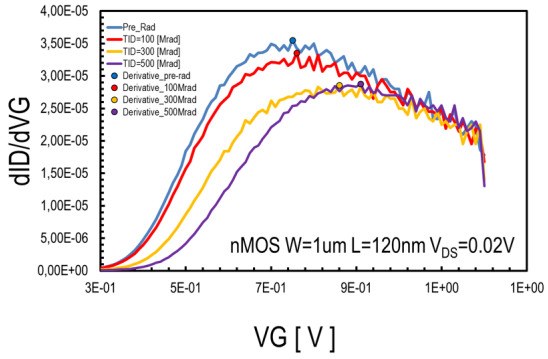

Figure 4.5 $\frac{dI_D}{dV_G} - V_G$ characteristic in four TID levels (0 Mrad, 100 Mrad, 300 Mrad, 500 Mrad), with marked max points for every level for W=1um, L=120nm, nMOS transistor, linear mode.

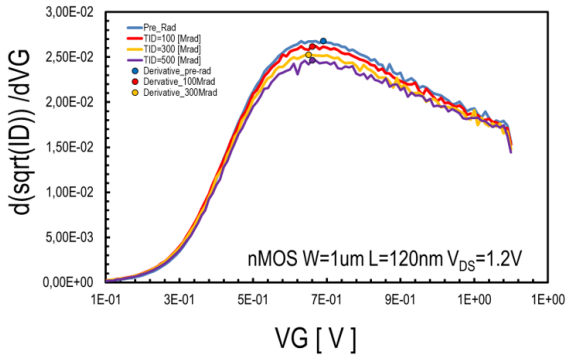

Figure 4.6 $\frac{\sqrt{dI_D}}{dV_G} - V_G$ characteristic in four TID levels (0 Mrad, 100 Mrad, 300 Mrad, 500 Mrad), with marked max points for every level for W=1um, L=120nm, nMOS transistor, linear mode

4.4 d factor extraction - DIBL

DIBL (Drain Induced Barrier Lowering) is an effect, which is referring to the threshold voltage shift to lower values for increased Drain voltage. This effect is more intense in short channel transistor and this is the cause that it has been characterized as short channel effect. The mathematical definition of DIBL comes from the equation below:

$$DIBL = \frac{\Delta V_{TH}}{\Delta V_D} \tag{4.14}$$

For this thesis and the data that are examined, the DIBL from linear to saturation mode would be expressed mathematically from the equation 4.15 below:

$$DIBL = \frac{V_{TH(sat)} - V_{TH(lin)}}{V_{D(sat)} - V_{D(lin)}} \tag{4.15}$$

For the needs of this research d factor will be defined as below 4.16:

$$d = V_{TH(lin)} - V_{TH(sat)} \tag{4.16}$$

The definition of this factor and its study has been preferred over DIBL. There are several reasons which explain the previous. Given the fact, that the difference of drain Voltage in linear mode minus this in saturation mode is steady in all the devices examined and equal with 1,18V, d factor has a deviation of 18% from DIBL. The stability of drain voltage variation from linear to saturation mode allows the d factor to show the variation of DIBL among the devices examined. Also, d factor shows a straight comparison of linear and saturation mode, through length and width.

Chapter 5

Models

Since the data of the three parameters were transferred in graphs for every scaling and mode, graphs for difference of linear mode minus saturation mode in threshold voltage were also produced, which depict the d Factor as it was defined above. The purpose is the extraction of a mathematical model which would contain all the TID levels in each scaling and could evaluate the behavior of every transistor in the range of the measured channel sizes. The essential goal is a simple model with few parameters. Parameter extraction based on a compact model would not be supposed to have any parameter for the TID effects. Starting from the threshold voltage measurements for pMOS, W=20um, the extraction of an equation for the model with an approximate method, was pursued. For the equation new parameters have to be defined. After tests the study resulted in the following equation for threshold Voltage. The same equation also covers the other two parameters (slope factor and mobility), but individual parameters for each one have to be defined as presented below. The mathematical model for d Factor comes from the difference of threshold Voltage models in linear minus saturation mode.

Threshold Voltage models:

The equation for Length scaling is:

$$V_{TH} = V_0 + (TID) \cdot VT_0 + (V_1 + VT_1 \cdot (TID)) \cdot (\frac{L_1}{L})^{Ve_1} + (V_2 + VT_2 \cdot (TID)) \cdot (\frac{L_2}{L})^{Ve_2} \tag{5.1}$$

The equation for Width scaling is:

$$V_{TH} = V_0 + (TID) \cdot VT_0 + (V_1 + VT_1 \cdot (TID)) \cdot (\frac{W_1}{W})^{Ve_1} + (V_2 + VT_2 \cdot (TID)) \cdot (\frac{W_2}{W})^{Ve_2} \tag{5.2}$$

Slope Factor models:

The equation for Length scaling is:

$$n = n_0 + (TID) \cdot nT_0 + (n_1 + nT_1 \cdot (TID)) \cdot (\frac{L_1}{L})^{ne_1} + (n_2 + VT_2 \cdot (TID)) \cdot (\frac{L_2}{L})^{ne_2} \quad (5.3)$$

The equation for Width scaling is:

$$n_{TH} = n_0 + (TID) \cdot nT_0 + (n_1 + nT_1 \cdot (TID)) \cdot (\frac{W_1}{W})^{ne_1} + (n_2 + nT_2 \cdot (TID)) \cdot (\frac{W_2}{W})^{ne_2} \quad (5.4)$$

Mobility models:

The equation for Length scaling is:

$$m = m_0 + (TID) \cdot mT_0 + (m_1 + nT_1 \cdot (TID)) \cdot (\frac{L_1}{L})^{me_1} + (m_2 + mT_2 \cdot (TID)) \cdot (\frac{L_2}{L})^{me_2} \quad (5.5)$$

The equation for Width scaling is:

$$m_{TH} = m_0 + (TID) \cdot mT_0 + (m_1 + mT_1 \cdot (TID)) \cdot (\frac{W_1}{W})^{me_1} + (m_2 + mT_2 \cdot (TID)) \cdot (\frac{W_2}{W})^{me_2} \quad (5.6)$$

Below there are apposed the parameters of the models :

For the Length scaling:

- **L1:** Parameter that influence the length according to e_1 parameter.
- **L2:** Parameter that influences the length according to e_2 parameter.

For Width scaling

- **W1:** Parameter that influence the width according to e_1 parameter.
- **W2:** Parameter that influences the width according to e_2 parameter.

Threshold Voltage	Slope Factor	Mobility
V0	n0	m0
V1	n1	m1
V2	n2	m2
Ve1	ne1	me1
Ve2	ne2	me2
VT0	nT0	mT0
VT1	nT1	mT1
VT2	nT2	mT2

Table 5.1 Individual model parameters of each parameter

Chapter 6

Analysis with adjusted models

In this chapter the analysis through channel length and width of Threshold Voltage, Slope factor, Mobility and d factor is presented, according to the models adjusted to the measurements.

6.1 Threshold Voltage analysis

Length Scaling

Linear mode

Concerning length scaling for V_{TH}, it is observed that V_{TH} is larger at short channel lengths in linear mode. Specifically, the largest values of threshold Voltage are noted at 60nm length for all the transistors. A decrease of V_{TH} is noticed as Length increases which is less intense as Length gets larger. Generally, the most intense change is between 60nm and approximately 600nm length. After these lengths a more ailing decrease of V_{TH} is taking place.

The above is observed in figure 6.1. At the length of 60nm V_{TH} is 0.67V. As the length levels increase the V_{TH} falls, its value at 800nm length is at 0.5V. Through the examination of V_{TH} between the lengths of 800nm and 10um, its value incurs a negligible fall. At the length of 10um V_{TH}= 0.48V.

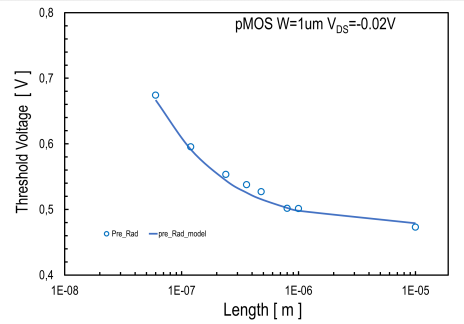

Figure 6.1 Isolated pre rad measurement and model characteristic for V_{TH} over Length for W=1um pMOS , linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

The above behavior of V_{TH} on pMOS, W=1um, linear mode is similar with nMOS, W=1um and for both nMOS and pMOS, W=20um. There is a small difference between the values, which is shown in the table below.

Threshold Voltage (V)					
Linear	**Transistors**	**L=60nm**	**L=10um**	**Smallest Value**	**Largest Value**
nMOS	W=1um	0.717	0.519	0.519V(10um)	0.717V(60nm)
	W=20um	0.7	0.52	0.52(10um)	0.7(60nm)
pMOS	W=1um	0.67	0.48	0.48(10um)	0.67(60nm)
	W=20um	0.79	0.52	0.52(10um)	0.79(60nm)

Table 6.1 V_{TH} values in linear mode for smallest and biggest Length examined

Looking at the table 6.1 something remarkable is noticed. At W=1um, V_{TH} is higher for the nMOS than the pMOS structures for both lengths (smallest and biggest). On the other hand, at W=20um,

V_{TH} is lower in the nMOS than the pMOS structure at the smallest length (60nm) and at the biggest length (10um), V_{TH} values are the same for the nMOS as for the pMOS.

Radiation Effects

The impact of exposure to TID in general, is an increase of V_{TH}, as the TID increases. This increase of V_{TH} is smaller, as the device length gets bigger, or zero depending on the device.

Specifically, figure 6.2 shows V_{TH} for W=1um, pMOS structures in different radiation levels through different lengths. There is difference between the radiation levels at all the lengths which are examined. For L=60nm V_{TH}=0.67V in pre-rad condition, 0.715V under 100Mrad and 0.87V under 400Mrad. As the transistor length gets bigger the variation from one TID to another is smaller, so for L=240nm it is observed that V_{TH}=0.54V in pre-rad condition, 0.569V under 100Mrad and 0.63V under 400Mrad. For L=10um it is noticed that the differences of V_{TH} are very small, to wit, in pre-rad condition V_{TH}=0.473V, under 100Mrad is 0.487V and under 400Mrad is 0.51V.

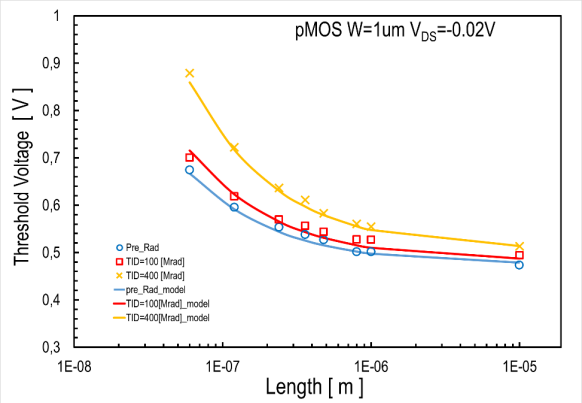

Figure 6.2 Measurement and model characteristic in three radiation levels(pre rad, 100Mrad, 400Mrad) for V_{TH} over Length for W=1um pMOS , linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um)

In figure 6.3 are apposed the measurements and the model charactristic for W=20um, nMOS structure, where is noticed that the variation of V_{TH} among the different TID levels is smaller than above. For 60nm length, V_{TH} in pre-rad condition is 0.717V, under 100Mrad is 0.742V and under 400Mrad is 0.816V. The difference is decreasing as the length gets larger and it gets zero for L=240nm.

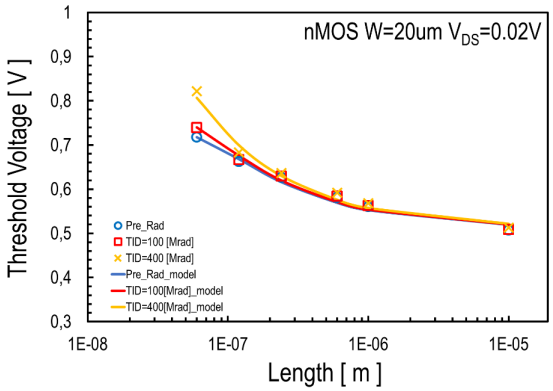

Figure 6.3 Measurement and model characteristic in three radiation levels(pre rad, 100Mrad, 400Mrad) for V_{TH} over Length for W=1um pMOS , linear mode. (Lengths : 60nm, 120nm, 240nm,600nm, 1um, 10um).

Threshold Voltage TID impact (V)				
nMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
L=60nm	0.712	0.8	0.994	1.09
L=240nm	0.6	0.62	0.66	0.7
L=1um	0.552	0.56	0.569	0.585
L=10um	0.52	0.529	0.533	0.539
pMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.67	0.715	0.87	
L=240nm	0.54	0.569	0.63	
L=1um	0.5	0.526	0.547	
L=10um	0.473	0.487	0.51	
nMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.717	0.742	0.816	
L=240nm	0.63	0.63	0.63	
pMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.7	0.72	0.79	
L=6um	0.54	0.55	0.577	
L=10um	0.51	0.51	0.52	

Table 6.2 V_{TH} values in linear mode for different TID levels

In the table 6.2 above are shown in numbers the differences of V_{TH} among the different TID levels, through length scaling for the devices that were examined. Comparing the nMOS to pMOS measurements, it is observed that the difference of V_{TH} between the TID levels in small lengths (clearer in 60nm) is larger in nMOS than pMOS. As the examined lengths increasing it is barely noticed that V_{TH} variation through the TID levels, is slightly larger in pMOS than nMOS (specifically for channel lengths larger than 240nm). Although it would not be a safe outcome that exists generally.

Saturation mode

In saturation mode it is noticed that the change of V_{TH} through the length is less than the change in linear mode. It is common for both the Widths that were examined in pMOS and nMOS structures, that as the length increases, in the length area between 120nm to 240nm and 10um, V_{TH} undergoes a negligible fall which gets even smaller as the device length gets smaller. Characteristically, in some cases V_{TH} in length area between approximately 6um and 10um may be considered as stable.

In the length area between 60nm and 120 to 240nm an ailing fall, that may be considered zero fall, is observed in W=1um, pMOS devices. Contrariwise, at the rest of devices that are examined, an increasing strain is observed which is more intense in W=20um, nMOS devices and less at W=1um nMOS devices. At W=20um, pMOS devices this trend is so negligible that V_{TH} at these lengths may be considered stable.

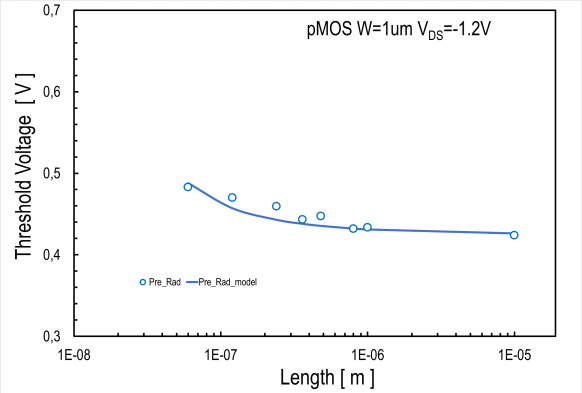

Figure 6.4 Isolated pre rad measurement and model characteristic for V_{TH} over Length for W=1um pMOS , saturation mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

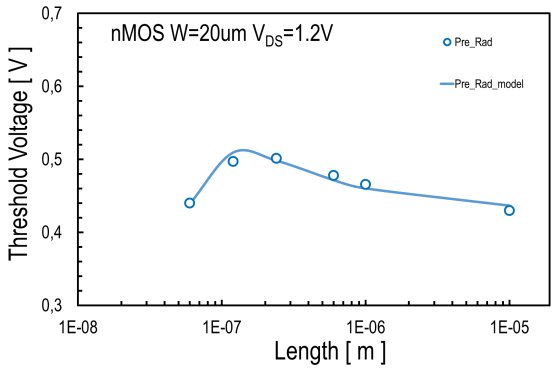

Figure 6.5 Isolated pre rad measurement and model characteristic for V_{TH} over Length for W=20um nMOS , saturation mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

In figure 6.4 is collocated the variation of V_{TH} through the length for W=1um, pMOS structure. In specific for L=60nm, V_{TH}=0.48V. As the length increases a slight fall of V_{TH} is noticed up to L=360nm where V_{TH}=0.443V. For the bigger lengths till L=10um V_{TH} keeps stable.

In figure 6.5 is shown that in W=20um, nMOS devices for L=60nm V_{TH}=0.44V.Examining larger lengths it is observed that V_{TH} increases, and so for L=120nm V_{TH}=0.497V. After 120nm V_{TH} increases a bit more and at 240nm V_{TH}=0.501V. From 240nm up to 800nm length a slight fall of V_{TH} is noticed, and so for L=600nm V_{TH}=0.477V. As the length heightens the fall of V_{TH} languishes and for L=10um V_{TH}=0.429V.

Threshold Voltage (V)					
Saturation	**Transistors**	**L=60nm**	**L=10um**	**Smallest Value**	**Largest Value**
	W=1um	0.456	0.435	0.435(10um)	0.51(120nm)
nMOS	W=20um	0.44	0.429	0.429(10um)	0.501(240nm)
	W=1um	0.48	0.43	0.43(10um)	0.48(60nm)
pMOS	W=20um	0.497	0.45	0.45(10um)	0.507(120nm)

Table 6.3 V_{TH} values in saturation mode for smallest and biggest Length examined

With the contribution of the Table 6.3 above,it could be extracted that in pMOS structures are encountered larger values of V_{TH} at the minimum lengths that are examined. More specifically between 60nm and 120 to 240nm. At the rest of the lengths not any clear differences between nMOS and pMOS structured are noticed, so not any safe result could be educed.

Radiation effect

The consequences of TID on V_{TH} in saturation mode, are the same as in linear mode. Although the magnitude of the increase of V_{TH} in the radiation induced devices is different.

Specifically, in figure 6.6, examining the W=1um, pMOS structures , the largest difference between the TID levels is detected , for L=60nm where, V_{TH} in the pre-rad condition is 0.487V, under 100Mrad V_{TH}=0.51V and under 400Mrad V_{TH}=0.57V. At bigger lengths the difference is lower and the lowest difference incurs at 10um length where is noticed that, in pre-rad condition V_{TH}=0.43V, under 100Mrad V_{TH}=0.438V and under 400Mrad V_{TH}=0.448V. It is also remarkable that the increase of V_{TH} is clearly bigger proportionately.

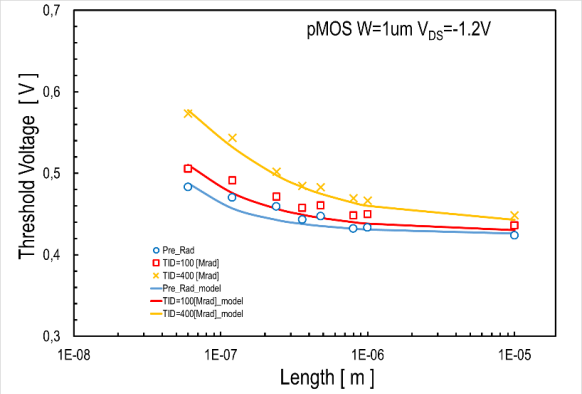

Figure 6.6 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad) for V_{TH} over Length for W=1um pMOS , saturation mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

Typical, are also the diagrams of W=20um, nMOS structures, figure 6.7,where is noticed the smallest discrepancy among the different TID levels. At the length of 60nm V_{TH} in pre-rad condition is equal with V_{TH} under 100Mrad with the value of 0.444V and under 400Mrad is 0.46V. As the length augments more than 60nm, the difference of V_{TH} from one TID level to another becomes zero and stays zero for all the other lengths examined.

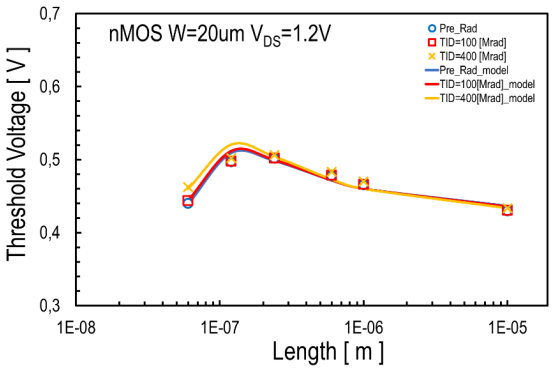

Figure 6.7 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad) for V_{TH} over Length for W=20um nMOS , saturation mode. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um, 10um).

Threshold Voltage TID impact (V)				
nMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
L=60nm	0.44	0.46	0.5	0.54
L=360nm	0.499	0.499	0.499	0.499
pMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.487	0.51	0.57	
L=240nm	0.44	0.47	0.497	
L=1um	0.43	0.44	0.46	
L=10um	0.43	0.438	0.448	
nMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.444	0.444	0.46	
L=120nm	0.5	0.5	0.5	
pMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.483	0.5	0.55	
L=6um	0.46	0.46	0.48	
L=10um	0.45	0.45	0.455	

Table 6.4 V_{TH} values in saturation mode for different TID levels

With the assistance of the table 6.4 above, where are presented analytically the values of V_{TH} at the different TID levels, it is observed that the impact of TID is more effective on pMOS structures than nMOS. It is clear that there are greater differences of V_{TH} on pMOS devices than nMOS and this is conspicuous more intensively at small lengths, and mainly 60nm length.

Width Scaling

Linear mode

From the study of V_{TH}, at nMOS and pMOS structures with 60nm and 10um length, through Width scaling, it could be noticed in general, that for widths from 120nm to 10um there is an ascending trend, mainly at small widths examined (120 to 480nm). At bigger widths (up to 1 to 10um) this trend is very ailing or even zero depending on the device. The second one is noticed at L=10um, nMOS devices and L=60nm, pMOS devices, where after a slight anode of V_{TH} through the width increase (from 120nm to 360nm and from 240nm to 480nm in respect), a stabilization of V_{TH} up to 10um and 1um in respect, is observed. It is also noticed that in L=60nm,nMOS devices V_{TH} value is stable for all the widths examined.

It can be marked from figure 6.8 that in L=10um, pMOS devices V_{TH} incurs an increase as widths increase, which is more ailing as larger widths are examined. V_{TH} at 120nm width is 0.44V and at 10um width V_{TH}=0.527V.

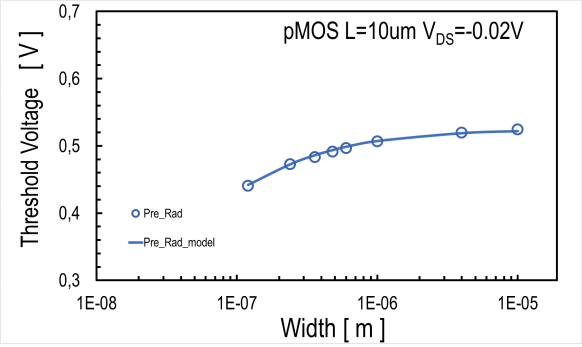

Figure 6.8 Isolated pre rad measurement and model characteristic for V_{TH} over Width for L=10um pMOS, linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um)

		Threshold Voltage (V)			
Linear	**Transistors**	**W=120nm (W=240nm-pMOS 60nm)**	**W=10um-L=60nm W=1um-L=10um**	**Smallest Value**	**Largest Value**
	L=60nm	0.67V	0.67V	0.67V	0.67
nMOS	L=10um	0.47	0.5046	0.47(120nm)	0.51(360nm)
	L=60nm	0.557	0.6	0.557(240nm)	0.64 (480nm)
pMOS	L=10um	0.44	0.527	0.44(120nm)	0.527(10um)

Table 6.5 V_{TH} values in linear mode for smallest and biggest Width examined

Table 6.5 contributes to the observation, that for low length (L=60nm), nMOS structures have clearly greater V_{TH} for all the widths examined. Although at L=10um models it is marked that in low widths (120nm-360nm) V_{TH} is higher at nMOS than pMOS structures, as for L=60nm devices, but at the wider devices(widths 1um-10um) it is noticed that the highest V_{TH} value is presented at pMOS structures.

Radiation effect

It could be indicated that there differences are great enough among the devices that are examined, concerning their behavior under different TID levels.

For L=10um, nMOS devices, there is not any impact of TID through the different TID levels examined, on V_{TH}. V_{TH} values through widths in pre-rad condition are equal with the values for TID=100Mrad and TID= 400Mrad.

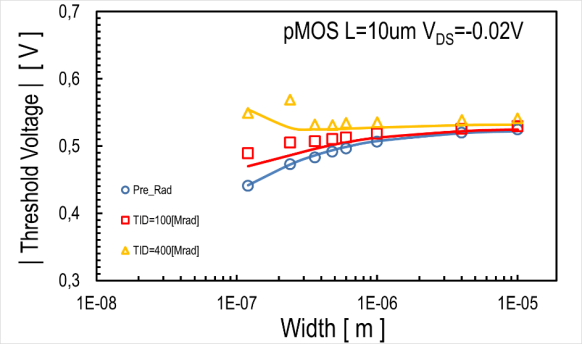

Figure 6.9 Measurement and model characteristic in three radiation levels(pre rad, 100Mrad, 400Mrad) for V_{TH} over Width for L=10um pMOS , linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 10um).

At L=10um, pMOS devices, as shown in figure 6.9, there is an impact of radiation on V_{TH}, which is shown at widths between 120nm and 1um. Specifically, at 120nm width V_{TH} in pre-rad condition is 0.44V, under 100 Mrads V_{TH}=0.48V and under 400Mrad V_{TH}=0.55V. Examining the bigger widths up to 360nm V_{TH} in pre-rad condition has a rising trend. The same happens under 100Mrad but more gently. It is remarkable that under 400Mrad, V_{TH} at these widths shows the opposite behavior from the other two TID levels since, a falling trend is presented. So at 360nm width in pre-rad condition V_{TH}=0.483V, under 100Mrad V_{TH}=0.5V and under 400Mrad V_{TH}=0.53V. From 360nm up to 4um where the difference among the TID levels is annihilated, V_{TH} at 0 and 100Mrad continues the ascending trend, which is smaller as widths are bigger, and at 400Mrad keeps stable. From 4um up to 10um width there is not any impact of radiation on V_{TH}.

At L=60nm, nMOS devices, figure 6.10, there are great differences of V_{TH} among the TID leves at all Widths examined. At 120nm width, in pre-rad condition V_{TH}=0.67V, under 100Mrad V_{TH}=0.764V, under 300Mrad V_{TH}=1.01V and under 500Mrad V_{TH}=1.1V. At 240nm width is noticed an increase of V_{TH} in the irradiated devices, and at the larger widths, V_{TH} comes back at former values and remains stable up to 1um width. V_{TH} in pre-rad condition keeps stable for all the widths examined. Under the influence of 300 and 500Mrad after 240nm, V_{TH} has a falling trend till 1um width. So at 1um width, in pre-rad condition V_{TH}=0.679V, under 100Mrad V_{TH}=0.746V, under 300Mrad V_{TH}=0.88V and under 500Mrad V_{TH}=0.97V.

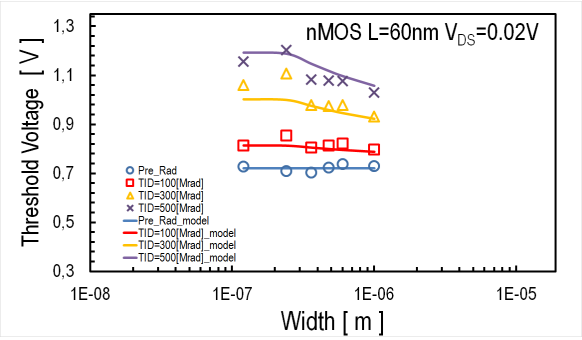

Figure 6.10 Measurement and model characteristic in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad) for V_{TH} over Width for L=60nm nMOS , linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um).

In figure 6.11 it is observed that there are great differences of V_{TH} from one TID level to another, at the small lengths(240nm-480nm), which are decreasing at the rest of the widths up to 1um. At 240nm width in pre-rad condition V_{TH}= 0.55V, under 100Mrad V_{TH}=0.617V and under 400Mrad V_{TH}=1.18V. After 240nm, at bigger widths in pre-rad condition is observed a small increase of V_{TH} up to 480nm, under the influence of 100Mrad V_{TH} keeps approximately stable through the widths and under 400Mrad V_{TH} incurs a fall up to 1um, which could be noticed that is less intense as widths become greater. So for 480nm width, in pre-rad condition V_{TH}=0.621V , under 100Mrad V_{TH}=0.642 and under 400Mrad V_{TH}=0.749V. From 480nm width up to 1um the pre-rad characteristic incurs a slight fall , the 100Mrads characteristic a negligible fall and the 400Mrad characteristic a clear fall. So the values of V_{TH} in respect for W=1um are , 0.6V, 0.62V, and 0.66V.

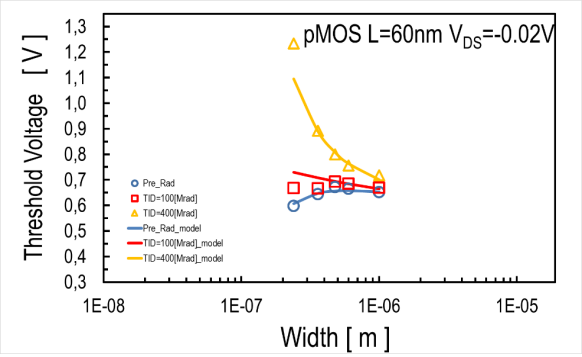

Figure 6.11 Measurement and model characteristic in three radiation levels(pre rad, 100Mrad, 300Mrad) for V_{TH} over Width for L=60nm pMOS , linear mode. (Widths : 240nm, 360nm, 480nm, 600nm, 1um).

Threshold Voltage TID impact (V)				
nMOS | L=60nm	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
W=120nm	0.67	0.764	1.01	1.1
L=4800nm	0.67	0.76	0.92	1.028
W=1um	0.67	0.74	0.88	0.97
pMOS | L=60m	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=240nm	0.55	0.617	1.18	
W=480nm	0.621	0.642	0.749	
W=1um	0.6	0.619	0.667	
nMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=120nm	0.47	0.47	0.47	
pMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=120nm	0.44	0.48	0.55	
W=480nm	0.49	0.501	0.525	
W=4um	0.54	0.54	0.54	

Table 6.6 V_{TH} values over width scaling in linear mode for different TID levels

From the above diagrams and table 6.6 it could be indicated that at the small widths (120-360nm) V_{TH} of pMOS notes larger radiation influence than nMOS, mainly for TID=300Mrad and higher. At

the big widths(1-10um) it could be extracted from the models of L=60nm that the impact of TID is larger in V_{TH} of nMOS than pMOS structures.

Saturation mode

In saturation mode is presented, in general, an increasing trend of V_{TH} as devices width augments. Although a more specific study of different lengths and structures shows some differences among them. Exception constitute L=60nm, nMOS devices, the V_{TH} of which keeps stable through width scaling.

In figure 6.12 it is shown that V_{TH} is increasing through the width scaling and also the increase is less intense as width augments. For 120nm width V_{TH}=0.38V and at 10um width V_{TH}=0.44V.

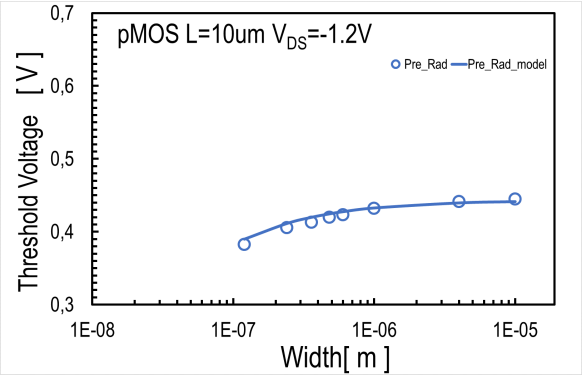

Figure 6.12 Isolated pre rad measurement and model characteristic for V_{TH} over Width for L=10um pMOS , saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

It is observed that L=10um, nMOS devices have the same behavior through width scaling as above, but as it is shown in figure 6.13 the ascending trend at the small lengths(120-360nm) is slightly more intense than this at the L=10um,pMOS structures. For W=120nm V_{TH}=0.34V. Also the increase of V_{TH} stops for W=1um at the value of 0.41V. From there up to W=10um, V_{TH} remains at the same levels.

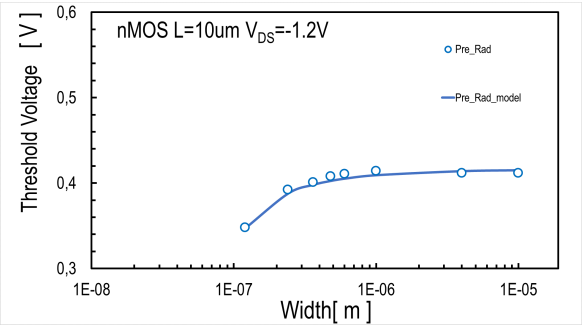

Figure 6.13 Isolated pre rad measurement and model characteristic for V_{TH} over Width for L=10um nMOS , saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

In figure 6.14 it is noticed that V_{TH} of L=60nm, pMOS devices increases as width increases from 240nm to 480nm width, from 0.394V to 0.459V in respect. Afterwards from 480nm width, V_{TH} indicates a trend of cathode up to 1um for which V_{TH}=0.444V.

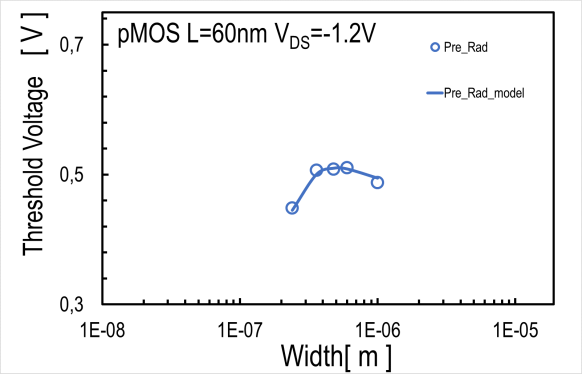

Figure 6.14 Isolated pre rad measurement and model characteristic for V_{TH} over Width for L=60nm pMOS , saturation mode. (Widths : 240nm, 360nm, 480nm, 600nm, 1um).

Threshold Voltage (V)					
Saturation	**Transistors**	**W=120nm (W=240nm-pMOS 60nm)**	**W=10um-L=60nm W=1um-L=10um**	**Smallest Value**	**Largest Value**
nMOS	L=60nm	0.448V	0.465V	0.448V(120nm)	0.465(1um)
	L=10um	0.34	0.413	0.34(120nm)	0.413(10um)
pMOS	L=60nm	0.394V	0.444V	0.394V(240nm)	0.459V (480nm)
	L=10um	0.38	0.44	0.38(120nm)	0.44(10um)

Table 6.7 V_{TH} values in saturation mode for smallest and biggest Width examined.

It could be noted from the above table 6.7 that at L=60nm devices, V_{TH} has higher values in nMOS structures than pMOS and at L=10um devices the opposite is happening and the values of V_{TH} in pMOS are higher than nMOS.

Radiation effect

As in linear mode, so in saturation, different behaviors of V_{TH} are presented under the influence of different TID levels.

For L=10um nMOS it is noticed, from figure 6.15, that at 120nm length, the values of V_{TH} under 100 and 400Mrad of TID are slightly lower than the value of V_{TH} in pre-rad condition, where V_{TH}=0.347V and under TID, V_{TH}=0.331V. As the width increases this difference decreases till it vanishes for W=600nm and it remains in zero levels up to 10um.

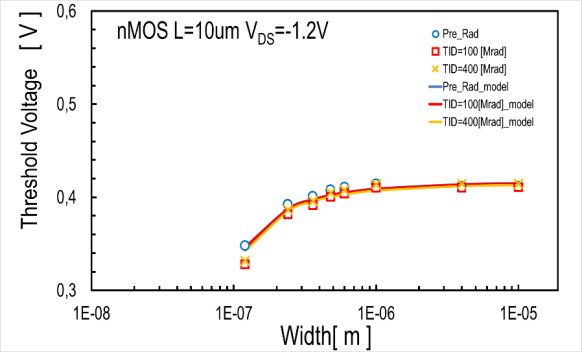

Figure 6.15 Measurement and model characteristic in three radiation levels(pre rad, 100Mrad, 400Mrad) for V_{TH} over Width for L=10um nMOS , saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 10um).

At L=10um, pMOS devices, V_{TH} through width scaling, at the different TID levels, has the same behavior as in linear mode and there is a difference in the values, which in saturation mode are lower.

At L=60nm, nMOS devices the diagrams, as presented in figure 6.16, of V_{TH} in the different TID levels are steady though all the widths examined. The difference between V_{TH} in pre-rad condition and under 100Mrad is zero. Values of V_{TH} under 300Mrad are a bit higher and under 500Mrad ever higher than these. Specifically, at 120nm width V_{TH} in pre-rad condition is 0.44V, under 100Mrad V_{TH}=0.44V, under 300Mrad V_{TH}=0.48V and under 500Mrad V_{TH}=0.52V.

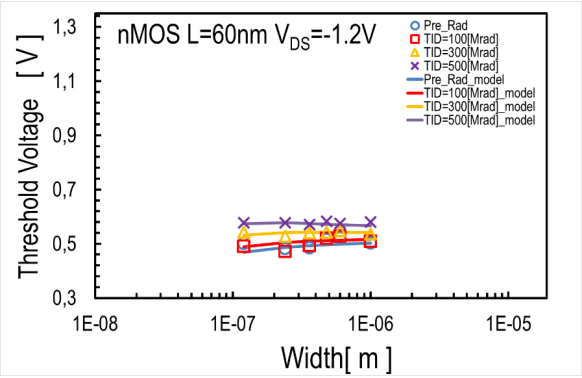

Figure 6.16 Measurement and model characteristic in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad) for V_{TH} over Width for L=60nm nMOS , saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um).

At L=60nm, pMOS devices, V_{TH}, as shown in figure 6.17, under 100Mrad TID follows the behavior of V_{TH} in pre-rad condition, increasing between 240 and 480nm width and increasing between 480nm and 1um width. Under the influence of 400Mrad, TID V_{TH} decreases as width increases for all widths examined. The largest difference among TID levels is noted at 240nm width where, in pre-rad condition V_{TH}=0.398V, under 100Mrad V_{TH}=0.457V and under 400Mrad V_{TH}=0.621V. As width augments the difference between the TID levels shrinks and at 1um width is indicated the smallest difference. Specifically, in pre-rad condition V_{TH}=0.437V, under 100Mrad V_{TH}=0.4558V and under 300Mrad V_{TH}=0.502V.

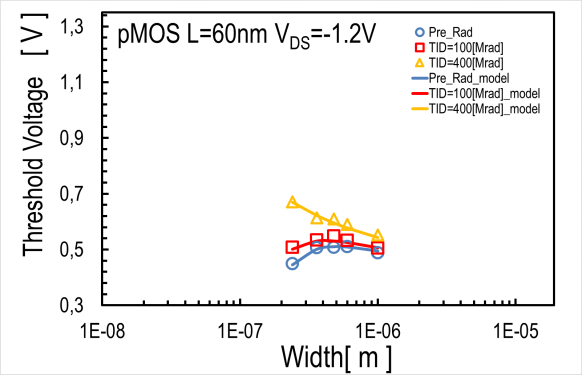

Figure 6.17 : Measurement and model characteristic in thee radiation levels(pre rad, 100Mrad, 400Mrad) for V_{TH} over Width for L=60nm pMOS , saturation mode. (Widths : 240nm, 360nm, 480nm, 600nm, 1um).

Threshold Voltage TID impact (V)				
nMOS | L=60nm	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
W=120nm	0.44	0.44	0.48	0.52
pMOS | L=60m	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=240nm	0.398	0.4578	0.621	
W=480nm	0.45	0.49	0.54	
W=1um	0.437	0.4558	0.502	
nMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=120nm	0.347	0.331	0.331	
pMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=120nm	0.39	0.41	0.47	
W=480nm	0.42	0.43	0.455	
W=4um	0.456	0.456	0.456	

Table 6.8 V_{TH} values over width scaling in saturation mode for different TID levels

From the table 6.8 above, it could be observed that the differences between the TID levels at low widths (120 to 360nm) are more intense in pMOS structures than in nMOS structures. At the rest of widths examined, there is not any result that clearly could be exported.

6.2 d factor analysis

Length scaling

Concerning the d factor, it is very clearly noticed that the values of V_{TH} are higher in linear mode than in saturation for all the structures and lengths that are examined. It is worth of mention that d is greater at the examining of small lengths (60nm-240nm) than the rest.

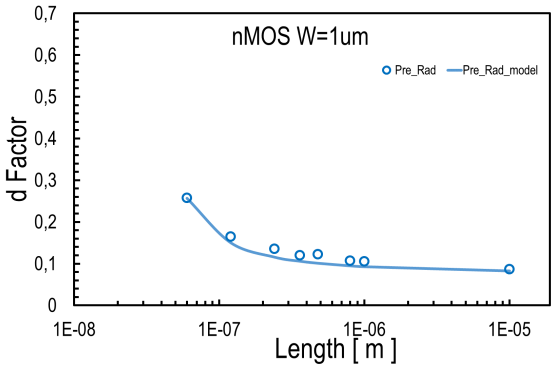

Figure 6.18 Isolated pre rad measurement and model characteristic for the difference of V_{TH} in linear and in saturation mode, over Length for W=1um nMOS. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

Figure 6.18 is a typical example of variation of d over length, which was described in general above. The largest value is noted at 60nm length and it is 0.257 and it falls as the length increases up to 10um for which d= 0.08.

Radiation effect

As for the impact of TID on d factor, it could be extracted that TID is more effective in short channel devices (60 – 240nm). The result of the TID exposure is the increase of d factor. The above is presented in figure 6.19, where at 60nm d=0.257 in pre-rad condition, under 100Mrad d=0.347, under 300Mrad d=0.492 and under 500Mrad d=0.554. As the length increases the difference among the TID levels is falling, up to 10um where is zero.

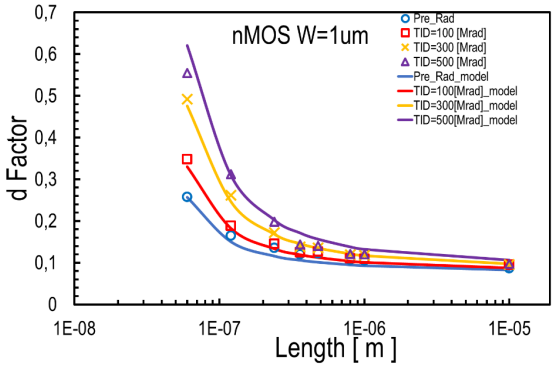

Figure 6.19 Measurement and model characteristics in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad), for d factor, over Length for W=1um nMOS. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um, 10um).

d factor TID impact				
nMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
L=60nm	0.267	0.347	0.492	0.554
L=120nm	0.16	0.19	0.25	0.312
L=10um	0.097	0.097	0.097	0.097
pMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.18	0.2	0.3	
L=800nm	0.18	0.2	0.3	
L=10um	0.057	0.061	0.072	
nMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.278	0.296	0.359	
L=120nm	0.169	0.169	0.181	
L=240nm	0.13	0.13	0.13	
pMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.224	0.227	0.241	
L=120nm	0.13	0.13	0.15	
L=600nm	0.095	0.095	0.095	

Table 6.9 d factor values for different TID levels

From the table 6.5 above it is remarkable that in the difference of the TID effectiveness between linear and saturation mode is greater in nMOS, than in pMOS. Also, the impact of TID is greater in linear than in saturation mode.

Width scaling

Considering the models that have been extracted for d factor, it is firstly observed that the values of V_{TH} are higher in linear than in saturation mode at all the different structures and widths examined. Secondary, it is noticed that the variation of d, could be characterized as stable through width scaling, something that is exported with an approximate way, from all the different lengths and structures examined.

Specifically, in figure 6.20, is presented the characteristic of d factor for L=10um, pMOS devices, which is a representative example for the rest of devices examined. It is noticed that the values of d have an ascending trend through width increase, which is so slight that could be considered negligible. At 120nm width d=0.058 and at 10um width d=0.079. Furthermore, it may be noted that the values of d are greater in nMOS structures than pMOS.

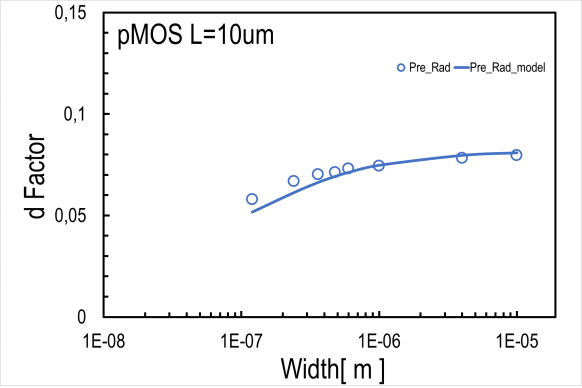

Figure 6.20 Isolated pre rad measurement and model characteristic for the d Factor, over Width for L=10um pMOS. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

Radiation effect

At L=10um devices, it is noted that the impact of radiation is zero except, L=10um, pMOS devices, in which it is indicated that there is a small difference between TID levels at 120nm and 240nm width. At 120nm width in pre-rad condition d=0,058 and at both the irradiated conditions d=0.076. At 240nm width, in pre-rad condition d=0.066, under 100Mrad d=0.073 and under 400Mrad d=0.1.

It could also be noted that in nMOS, L=10um diagram that at 120nm width, the value of d in pre-rad condition is lower than these of the irradiated conditions. And so, it could be extracted that at this width the impact of radiation is greater in saturation than in linear mode.

As for L=60nm devices, at the small widths (120nm – 360nm) are noted very perceptible differences among the TID levels, in both nMOS and pMOS structures. More specific, at L=60nm, nMOS devices, figure 6.21, the values of d are stable through widths for pre-rad and 100Mrad characteristic. Although, the 300Mrad and 500Mrad present a fall from 240nm width up to 1um width. So, the differences between the TID levels are greater in small lengths (120nm-240nm).

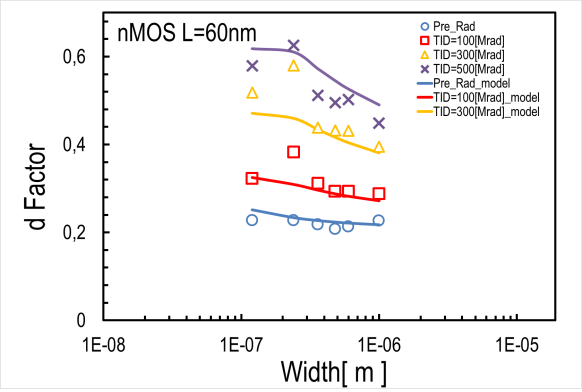

Figure 6.21 Measurement and model characteristics in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad), for d factor, over Width for L=60nm nMOS. (Lengths : 120nm, 240nm,360nm, 480nm, 600nm, 1um).

At L=60nm, pMOS devices, figure 6.22, the values of d in pre-rad condition and under 100Mrad, are stable through width scaling and equal between them. As for the values of d under 400Mrad, are much greater than the other two TID levels at small widths(240nm-480nm). As the widths examined augment, the 400Mrad characteristic falls and so the difference between the TID levels. At 1um width the difference among TID levels is zero.

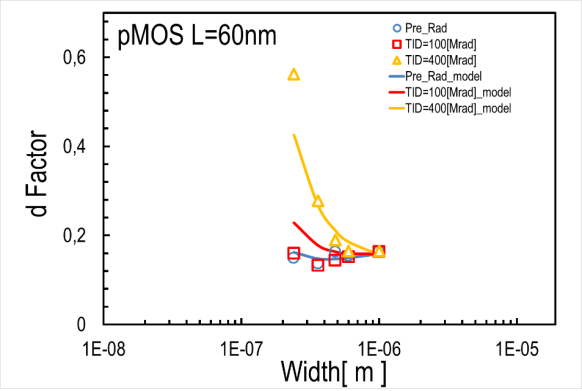

Figure 6.22 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad,) for d factor, over Width for L=60nm pMOS. (Widths : 240nm, 360nm, 480nm, 600nm, 1um).

d factor TID impact				
nMOS | L=60nm	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
W=120nm	0.22	0.32	0.51	0.57
pMOS | L=60m	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=240nm	0.15	0.16	0.56	
W=480nm	0.14	0.14	0.2	
W=1um	0.165	0.165	0.165	
nMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=120nm	0.127	0.143	0.143	
pMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=120nm	0.058	0.076	0.076	
W=480nm	0.066	0.073	0.1 V	
W=4um	0.082	0.082	0.082	

Table 6.10 d factor values for different TID levels, through width scaling

6.3 Slope factor analysis

Length Scaling

Linear mode

Examining slope factor through length scaling it can be observed in general, that at low lengths (60-120nm), as length increases slope factor endures a decrease. As for the intense of this decrease and

the rest of the lengths examined, different behaviors are noted at the variety of widths and structures studied.

From the models of W=1um devices, it is observed that through length scaling, after the fall at low lengths (60-120nm), follows an anode of slope factor as length increases. This behavior could be typically presented by W=1um, pMOS diagram in figure 6.23, where at 60nm length n=1.434. As length gets bigger, n falls up to 120nm length where n=1.3. Length increase continuous and n increases, less intensively than the fall before, up to 10um length with n=1.44.

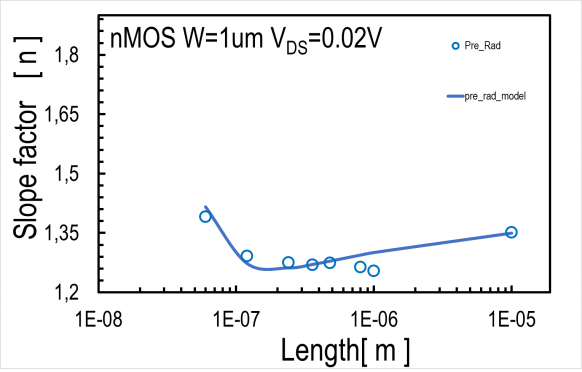

Figure 6.23 Isolated pre rad measurement and model characteristic for slope factor(n) over Length for W=1um pMOS , linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

At the diagrams of W=20um, pMOS devices, figure /reffig 6.24, it is noticed that there is a fall of n through length increase from 60nm, where n=1.44, to 10um, where n=1.19. Also, this fall is more intense at the small lengths.

Although, at W=20um, nMOS devices, figure 6.25, the fall of n, from 60nm length and n=1.35, does not last during all the lengths examined, but stops at 240nm, where n=1.23 and then keeps stable up to 10um.

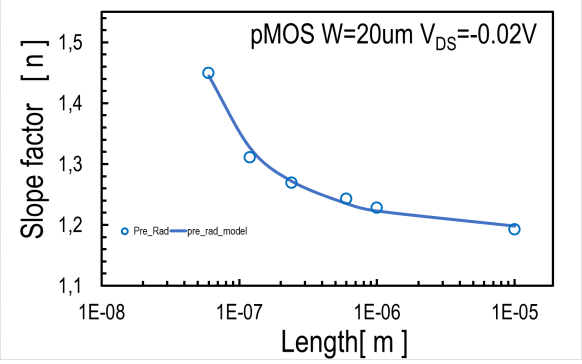

Figure 6.24 Isolated pre rad measurement and model characteristic for slope factor(n0) over Length for W=20um pMOS , linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 600nm, 1um, 10um).

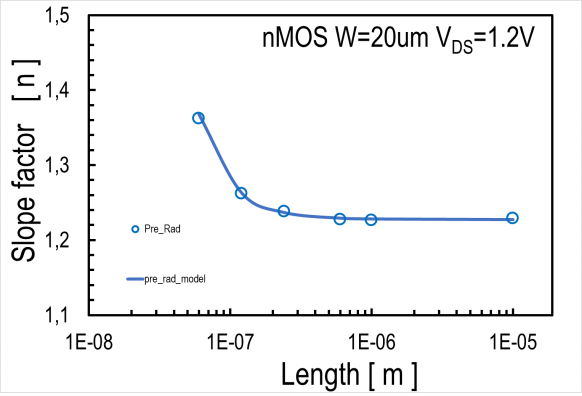

Figure 6.25 Isolated pre rad measurement and model characteristic for slope factor(n0) over Length for W=20um nMOS , linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 600nm, 1um, 10um).

Slope factor					
Linear	**Transistors**	**L=60nm**	**L=10um**	**Smallest Value**	**Largest Value**
nMOS	W=1um	1.39	1.28	1.28(240nm)	1.39(60nm)
	W=20um	1.35	1.23	1.23(240nm-10um)	1.35(60nm)
pMOS	W=1um	1.434	1.44	1.3(120nm)	1.44(10um)
	W=20um	1.44	1.19	1.19(10um)	1.44(60nm)

Table 6.11 Slope factor(n) values in linear mode for smallest and biggest Length examined.

Radiation effect

In general, as it is observed the influence of TID increases the slope factor. Also, the impact of TID is greater in W=1um devices than in W=20um devices.

At W=1um, pMOS, figure 6.26 there is a slight difference between n values in 0 and 100Mrad conditions and bigger between 100Mrad and 400Mrad. Specifically, for L=60nm in pre-rad condition n=1.434, under 100Mrad n=1.44 and under 400Mrad n=1.52. As length increases the difference among TID levels reduces until it eliminates for L=360nm. From 360nm length up to 10um the difference increases with the higher values to be noted in pre-rad condition, lower than the latter are these of 100Mrad and even lower these of 400Mrad condition. For L=10um in pre-rad condition n=1.44, under 100Mrad and 400Mrad n=1.4

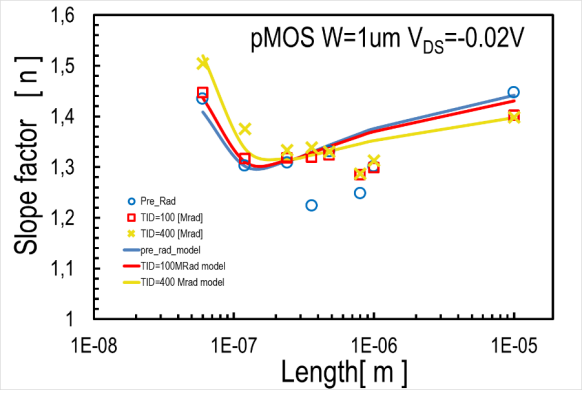

Figure 6.26 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad,) for slope factor over Length for W=1um, pMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

At W=1um, nMOS devices, figure 6.27, for L=60nm in pre-rad condition n= 1.39, under 100Mrad n=1.46, under 300Mrad n=1.5 and under 500Mrad n=1.788. As length increases the difference among the TID levels reduces but it remains perceptible. For L=10um in pre-rad condition n=1.35, under 100mrad n=1.37, under 300Mrad n=1.41 and under 500Mrad n=1.43.

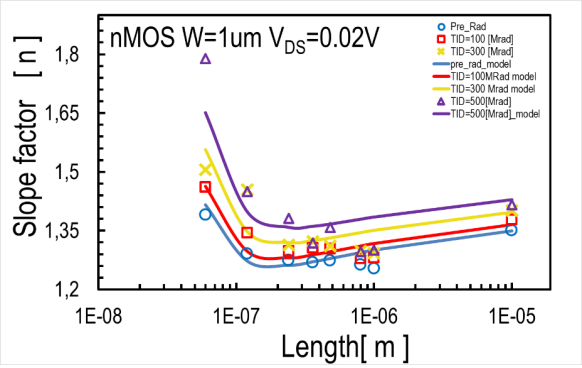

Figure 6.27 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad,) for slope factor over Length for W=1um pMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

At W=20um, pMOS the effectiveness of TID impact on n values is zero through the whole width scaling.

At W=20um, nMOS devices figure 6.28, it is observed that there is an impact of TID for L=60nm which is vanishing for L=1um after incurring a reduce for the widths between. For L=10um in pre-rad condition n=1.35, under 100Mrad n=1.38 and under 400Mrad n=1.41.

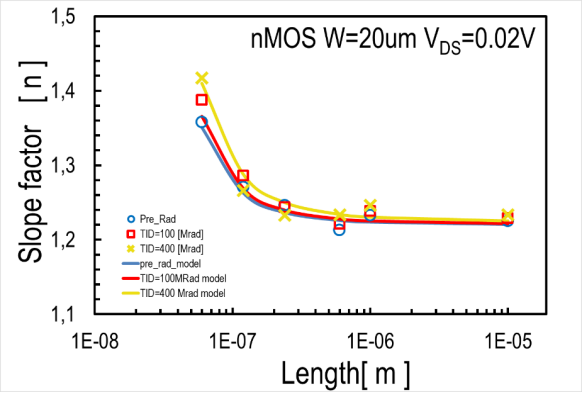

Figure 6.28 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad,) for slope factor over Length for W=20um nMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

Slope factor TID impact				
nMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
L=60nm	1.39	1.46	1.5	1.788
L=240nm	1.26	1.31	1.32	1.38
L=10um	1.35	1.37	1.41	1.43
pMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	1.434	1.44	1.52	
L=10um	1.44	1.4	1.4	
nMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	1.35	1.38	1.41	
pMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	1.425	1.425	1.425	

Table 6.12 Slope Factor(n) values in linear mode for different TID levels.

Saturation mode

Extracting the models for slope factor through length scaling in saturation mode, it is observed that slope factor moves as the length increases in a same way and at same levels, or a bit lower, as in linear mode. The exception, are W=1um, nMOS devices, which is shown in figure 6.29.

More specifically, at 60nm length n=1.36 and as length augments, n incurs a fall up to 240nm length where n=1.28. From 240nm up to 10um length, n keeps steady at the value of 1.35, in oppose with linear mode.

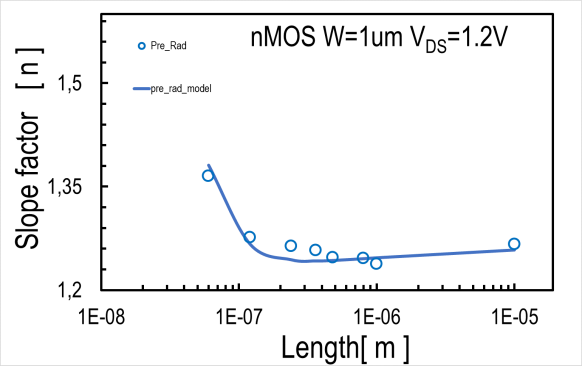

Figure 6.29 Isolated pre rad measurement and model characteristic for slope factor(n) over Length for W=1um nMOS , saturation mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

Slope factor					
Linear	**Transistors**	**L=60nm**	**L=10um**	**Smallest Value**	**Largest Value**
	W=1um	1.36	1.27	1.27(240nm-10um)	1.36(60nm)
nMOS	W=20um	1.367	1.23	1.23(600nm-10um)	1.367(60nm)
	W=1um	1.427	1.36	1.265(120nm)	1.427(60nm)
pMOS	W=20um	1.43	1.18	1.18(10um)	1.43(60nm)

Table 6.13 Slope factor(n) values in saturation mode for smallest and biggest Length examined.

With the contribution of Table 6.13, it is observed that as in linear mode, so in saturation it is clear that for low lengths(60-120nm), at pMOS structures are noted greater values of slope factor than nMOS.

Radiation effect

In saturation mode it is noticed that the impact of TID on slope factor is similar with its effectiveness in linear mode. In agreement with the linear mode, there are different behaviors of TID impact, through the widths and the structure examined.

At W=1um, nMOS devices for L=60nm devices, figure 6.30, in pre-rad condition n=1.365, under 100Mrad n=1.41, under 300Mrad n=1.53 and under 500Mrad n=1.58. As length increases more than 60nm, the TID impact is lower and from 240nm up to 10um it stays at the same levels. Mainly there is difference between pre-rad condition and irradiated. The difference among the three irradiated conditions fluctuates from very low values down to zero. For L=10um in pre-rad condition n=1.27, under 100Mrad, 300mrad and 500Mrad n=1.31.

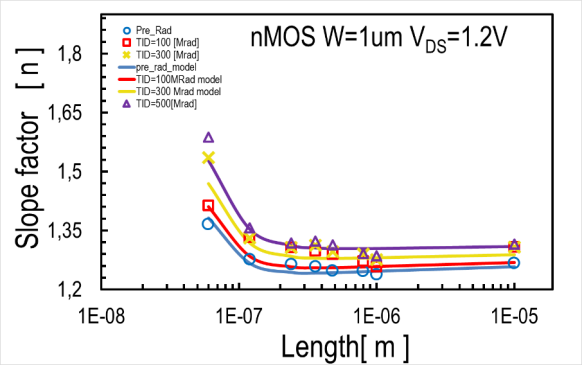

Figure 6.30 Measurement and model characteristics in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad) for slope factor over Length for W=1um nMOS, saturation mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

At W=20um, pMOS devices, as it is presented in figure 6.31 there is no difference between the two irradiated conditions through length scaling. At L=60nm in pre-rad condition n= 1.45, under 100Mrad n= 1.45 and under 400Mrad n=1.43. As length increases the difference among TID levels is getting slight bigger from 120nm till 10um length.

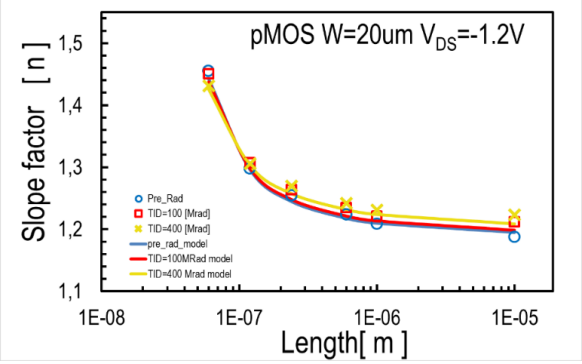

Figure 6.31 Measurement and model characteristics in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad) for slope factor over Length for W=20um pMOS, saturation mode. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um,10um).

At W=20um, nMOS devices as it is shown in figure 6.32 the TID impact is low. For L=60nm in pre-rad condition n=1.367, under 100Mrad n=1.388 and under 400Mrad n=1.407. Examining greater lengths, it is noticed that TID impact gets even lower till 10um where it can marginally be considered as zero. For L=10um in pre-rad condition n=1.23, under 400Mrad n=1.238 and under 400Mrad n=1.242.

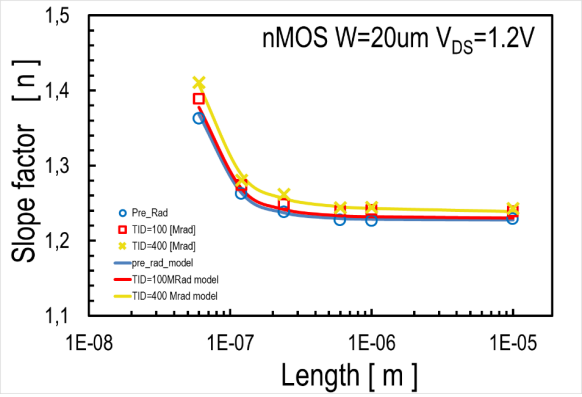

Figure 6.32 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 300Mrad) for slope factor over Length for W=20um nMOS, saturation mode. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um, 10um).

Slope factor TID impact				
nMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
L=60nm	1.365	1.41	1.53	1.58
L=240nm	1.26	1.3	1.305	1.31
L=10um	1.27	1.31	1.31	1.31
pMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	1.45	1.37	1.45	
L=10um	1.36	1.28	1.28	
nMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	1.367	1.388	1.408	
L=600nm	1.229	1.233	1.245	
L=10um	1.23	1.238	1.242	
pMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	1.425	1.425	1.425	

Table 6.14 Slope Factor(n) values in saturation mode for different TID levels.

Width Scaling

Linear mode

Examining the measurements and adjusting the models at slope factor through width scaling it is observed that at L=10um devices, slope factor decreases as width augments and at L=60nm devices slope factor values remain at same levels as width increases.

More specifically, at L=10um, pMOS devices, figure 6.33, at 120nm width n=2.03. As width increases n incurs a fall which is more intense up to 600nm width , where n=1.49, than up to 10um width where n=1.19.

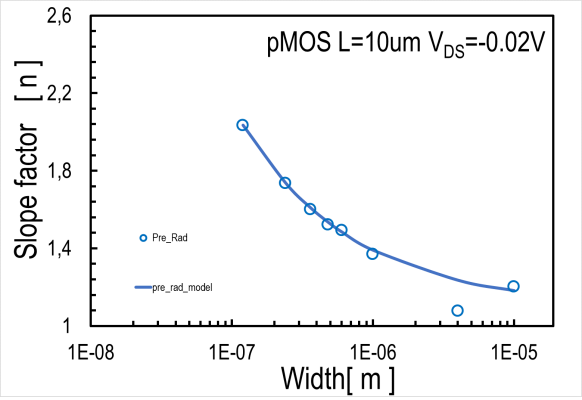

Figure 6.33 Isolated pre rad measurement and model characteristic for slope factor(n0) over Width for L=10um pMOS , linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

At L=60nm, nMOS devices, as it is presented in figure 6.34, slope factor values keeps steady as widths increase from 240nm up to 1um width. For 240nm width n=1.412 and for 1um width n=1.42.

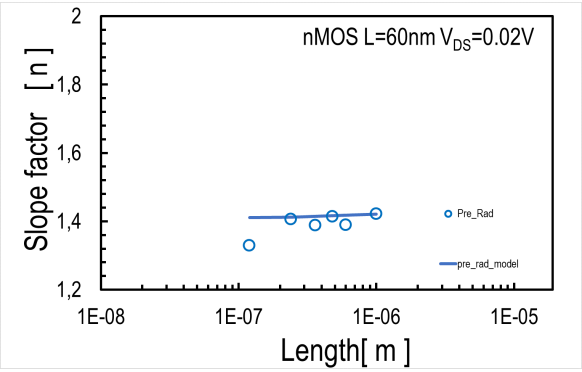

Figure 6.34 Isolated pre rad measurement and model characteristic for slope factor(n) over Width for L=60nm, nMOS , linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um).

Slope factor					
Linear	**Transistors**	**W=120nm (W=240nm-pMOS 60nm)**	**W=10um-L=60nm W=1um-L=10um**	**Smallest Value**	**Largest Value**
nMOS	L=60nm	1.412	1.42	1.412(120nm)	1.42(1um)
	L=10um	1.6(240nm)	1.22	1.22(10um)	1.6(240nm)
pMOS	L=60nm	1.46	1.492	1.46(240nm)	1.492(1um)
	L=10um	2.03	1.19	1.19(10um)	2.03(120nm)

Table 6.15 Slope Factor values in linear mode for smallest and biggest Width examined

Radiation effect

The impact of TID through width scaling in linear mode is more intense as the devices examined are narrow and is less intense for wider devices.

At L=60nm, pMOS devices, the behavior of which through width and under TID influence is presented in figure 6.35, the difference that exist for W=240nm, reduces as width increases till getting zero for W=600nm. For W=240nm in pre-rad condition n=1.47, under 100Mrad n=1.462 and under 400Mrad n=1.437.

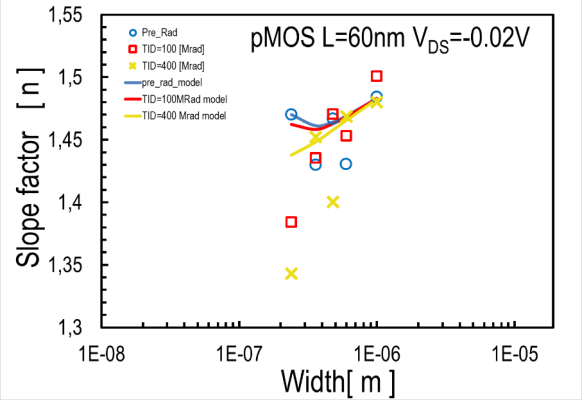

Figure 6.35 Measurement and model characteristic in three radiation levels(pre rad, 100Mrad, 400Mrad) for n over Width for L=60nm pMOS , linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um).

At W=60nm, nMOS device as it is presented in figure 6.36, is noted a great difference of n among the different TID levels through width scaling. For W=120nm in pre-rad condition n=1.328, under 100Mrad n=1.38, under 300Mrad n= 1.856 and under 500Mrad n=1.91. By the increase of width this difference is reducing but it remains at high levels. Specifically, for W=1um in pre-rad condition n=1.42, under 100Mrad n=1.46, under 300Mrad n=1.548 and under 500Mrad n=1.634.

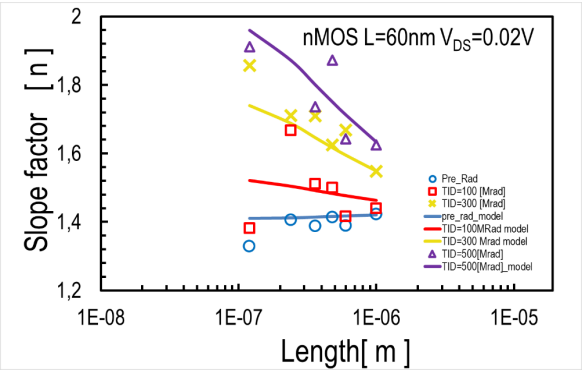

Figure 6.36 Measurement and model characteristic in three radiation levels(pre rad, 100Mrad, 400Mrad) for n over Width for L=60nm nMOS , linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um).

At L=10um it is observed that there is a slight but perceptible difference of n among the TID levels examined, which is shrinking through the increase of widths and it eliminates at the highest

from the widths examined (4um, 10um). Typical example of the above is what is presented in figure 6.37 about L=10um, pMOS devices. For W=120um in pre-rad condition n=2.03, under 100Mrad and 500Mrad n=2.3.

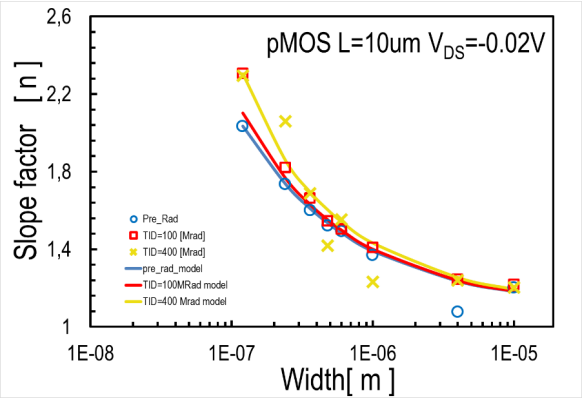

Figure 6.37 Measurement and model characteristic in three radiation levels(pre rad, 100Mrad, 400Mrad) for n over Width for L=10um pMOS , linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

Slope factor TID impact				
nMOS | L=60nm	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
W=120nm	1.328	1.38	1.856	1.91
W=480nm	1.41	1.499	1.6248	1.87
W=1um	1.42	1.46	1.548	1.634
pMOS | L=60m	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=240nm	1.47	1.462	1.437	
W=600nm	1.468	1.468	1.468	
nMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=240nm	1.58	1.64	1.67	
W=360nm	1.51	1.54	1.52	
pMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=120nm	2.3	2.3	2.3	
W=360nm	1.61	1.63	1.69	
W=10um	1.25	1.25	1.25	

Table 6.16 Slope Factor values, in linear mode for different TID levels, through width scaling.

Saturation mode

In saturation mode the behavior of slope factor through length scaling at L=10um and L=60nm devices is corresponding with these in linear mode.

More specifically, in figure 6.38 is presented that in L=10um, pMOS devices, slope factor incurs a fall as widths gets bigger that is less intense than this in linear mode. At 120nm width n=1.44.

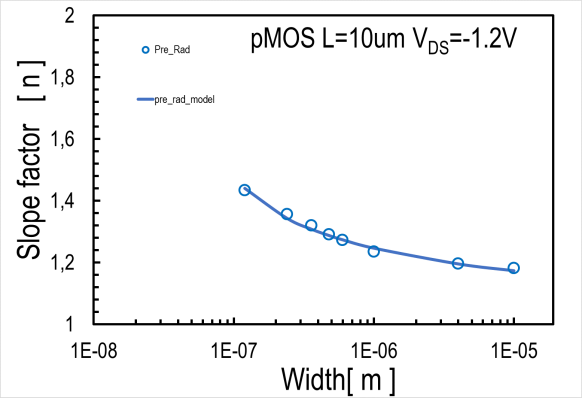

Figure 6.38 Isolated pre rad measurement and model characteristic for slope factor(n) over Width for L=10um, pMOS, saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

Slope factor					
Saturation	**Transistors**	**W=120nm (W=240nm-pMOS 60nm)**	**W=10um-L=60nm W=1um-L=10um**	**Smallest Value**	**Largest Value**
nMOS	L=60nm	1.35	1.36	1.35(120nm)	1.36(1um)
	L=10um	1.36(240nm)	1.23	1.23(10um)	1.36(240nm)
pMOS	L=60nm	1.42	1.43	1.42(240nm)	1.43(1um)
	L=10um	1.44	1.19	1.19(10um)	1.44(120nm)

Table 6.17 Slope Factor values in saturation mode for smallest and biggest Width examined.

Radiation effect

As linear mode so in saturation the TID impact is mainly effective in narrow (120nm to 360nm) and less in wide devices (1um to 4um width).

At L=60nm, pMOS structures as it is shown in figure 6.39 the TID impact, which influences increasingly the values of slope factor, is effective enough for W=240nm. For this width in pre-rad condition n=1.42, under 100Mrad n=1.24 and under 400Mrad n=1.58. As width increases the difference among the TID levels is shrinking and it eliminates for W=600nm.

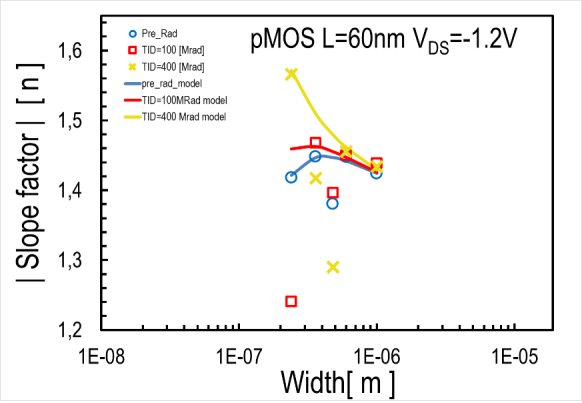

Figure 6.39 Measurement and model characteristic in three radiation levels(pre rad, 100Mrad, 400Mrad) for n over Width for L=60nm, pMOS , saturation mode. (Widths : 240nm, 360nm, 480nm, 600nm, 1um).

At L=60nm, nMOS devices, presented in figure 6.40, the difference of n among the TID levels is high through the whole width scaling. At 120nm width in pre-rad condition n=1.32, under 100Mrad n=1.44, under 300Mrad n=1.28 and under 500Mrad n=1.54. Worth of mention is the fact that the characteristics of pre-rad and 100Mrad condition keep stable through width scaling in oppose with the characteristics of 300Mrad and 500Mrad condition which incurs a fall as width increases. As a result, the difference among the TID levels is reducing but it remains very observable.

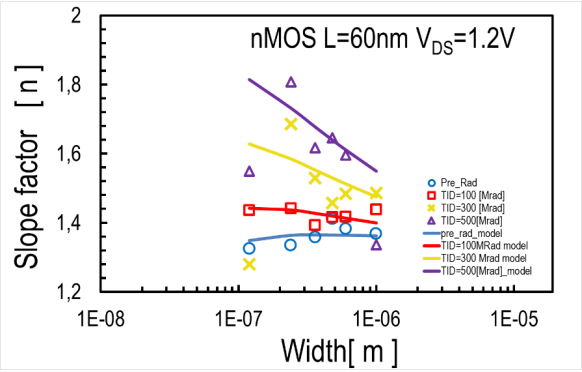

Figure 6.40 Measurement and model characteristic in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad) for n over Width for L=60nm, nMOS , saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um).

At L=10um devices is noticed that the impact of TID which is perceptible for 120nm width is reducing during the examination of wider devices up to 480nm, after which the TID effectiveness is increasing up to 10um width. Furthermore, from 480nm up to 10um width there is no difference between the two irradiated conditions. The above is shown in figure 6.41 clearly. For W= 120nm width in pre-rad condition n=1.44, under 100Mrad n=1.53 and under 400Mrad n=1.63.

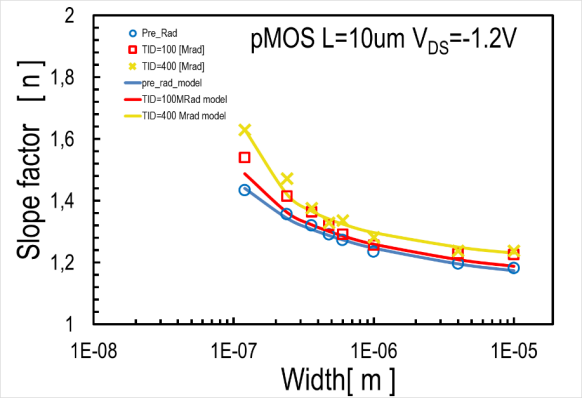

Figure 6.41 Measurement and model characteristic in three radiation levels(pre rad, 100Mrad, 400Mrad) for n over Width for L=10um, pMOS , saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

Slope factor TID impact				
nMOS | L=60nm	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
W=120nm	1.32	1.44	1.28	1.54
W=240nm	1.33	1.44	1.68	1.8
W=600nm	1.36	1.41	1.48	1.634
W=1um	1.36	1.43	1.485	1.33
pMOS | L=60m	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=240nm	1.42	1.24	1.58	
W=600nm	1.44	1.44	1.44	
nMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=240nm	1.36	1.41	1.43	
W=600nm	1.28	1.322	1.33	
W=10um	1.23	1.254	1.268	
pMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=120nm	1.44	1.53	1.63	
W=360nm	1.29	1.328	1.34	
W=10um	1.17	1.225	1.238	

Table 6.18 Slope Factor values, in saturation mode for different TID levels, through width scaling.

With the contribution of table 6.18 above, it is educed that there are not differences between linear and saturation mode, concerning the values of slope factor in pre-rad condition. There is also not any clear result that can be extracted concerning any different effectiveness of TID in linear and saturation mode.

Although it is clear that there is greater impact of TID in nMOS structures rather than in pMOS. This result is extracted in both length and width scaling from all devices that has been examined

6.4 Mobility analysis

Length Scaling

Linear mode

From the examining of the adjusted on the measurements, models in linear mode, it is observed that there is an increase of mobility as device's length increases. This increase is noticed in general between 60nm and 1um length. As devices length augments, up to 10um, the increase continues, except for W=20um, pMOS devices where mobility keeps stable. As for the rest of the devices, the raise between 1um and 10um is slight in W=1um devices and more intense in W=20um, pMOS devices.

A representational model for the latter is that of W=1um, nMOS structures, which is presented in figure 6.42. At 60nm length mobility is 0.015 $\frac{m^2}{Vs}$ and as length increases mobility increases too. So, at 1um length μ=0.0256 $\frac{m^2}{Vs}$. From this length till 10um the increase is less intense and at 10um length μ=0.0286 $\frac{m^2}{Vs}$.

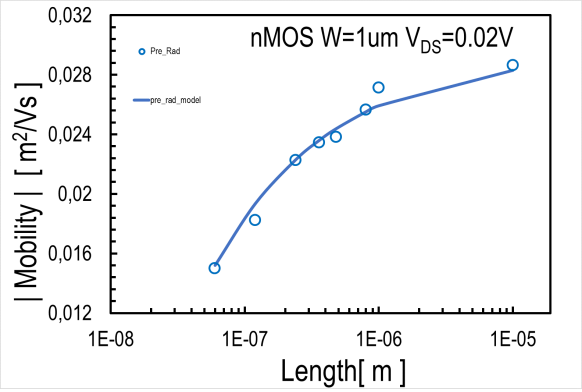

Figure 6.42 Isolated pre rad measurement and model characteristic for mobility over Length for W=1um, nMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

At figure 6.43 it is observed that the increase of mobility through length scaling, from low to high, has the same intensity from 60nm to 10um length, where the values of mobility are 0.0119 $\frac{m^2}{Vs}$ and 0.03118 $\frac{m^2}{Vs}$ respectively.

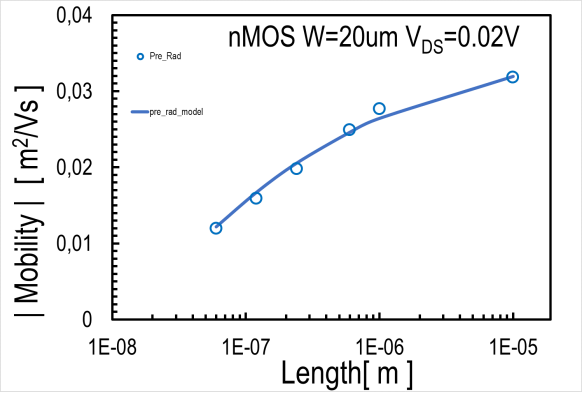

Figure 6.43 Isolated pre rad measurement and model characteristic for mobility over Length for W=20um, nMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um, 10um).

The opposite behavior is noticed in W=20um, pMOS devices, figure 6.44 where mobility after the increase between 60nm and 600nm, with values in respect 0.00555 $\frac{m^2}{Vs}$ and 0.0086 $\frac{m^2}{Vs}$, keeps stable as length augments up to 10um where μ=0.00856 $\frac{m^2}{Vs}$.

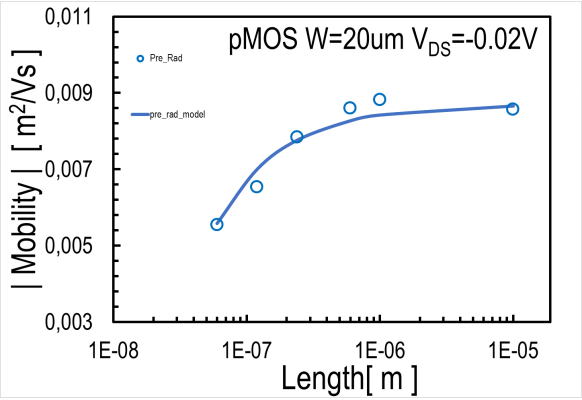

Figure 6.44 Isolated pre rad measurement and model characteristic for mobility over Length for W=20um, pMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um, 10um).

Mobility ($\frac{m^2}{Vs}$)					
Linear	**Transistors**	**L=60nm**	**L=10um**	**Smallest Value**	**Largest Value**
	W=1um	0.015	0.0286	0.015 (60nm)	0.0286(10m)
nMOS	W=20um	0.0119	0.0318	0.019(60nm)	0.0318(10um)
	W=1um	0.00607	0.0104	0.00607(60nm)	0.0104(10um)
pMOS	W=20um	0.00555	0.00856	0.00555(60nm)	0.0086(600nm)

Table 6.19 Mobility values in linear mode for smallest and biggest Length examined

With the assistance of the table 6.19 above it could be clearly extracted that the values of mobility in linear mode are higher in nMOS structures than in pMOS.

Radiation effect

The impact of TID as it is observed, is different among the widths and structures examined. Although the common element is that the impact is more intense at short devices and the most at 60nm length. The result of the effectiveness of TID in general is the fall of mobility values.

At W=1um, pMOS devices, as it is presented in figure 6.45, in pre-rad condition mobility is 0.00607 $\frac{m^2}{Vs}$, under 100Mrad 0.00525 $\frac{m^2}{Vs}$ and under 400Mrad is 0.0028 $\frac{m^2}{Vs}$. As length increases the impact of TID is lower and for 10um length, where the lowest impact is noticed, mobility values in pre-rad condition is 0.0104 $\frac{m^2}{Vs}$ and in both 100Mrad and 400Mrad conditions μ=0.0974 $\frac{m^2}{Vs}$.

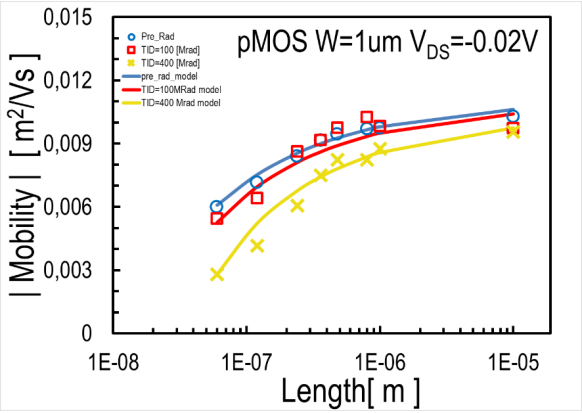

Figure 6.45 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for mobility over Length for W=1um pMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm,800nm, 1um, 10um).

At W=1um, nMOS devices the general behavior of radiation influence through length scaling is the same as the pMOS srtucture above. As it is shown in figure 6.46, for 60nm length mobility values are: in pre-rad condition μ=0.015 $\frac{m^2}{Vs}$, under 100Mrad μ=0.0119 $\frac{m^2}{Vs}$, under 300Mrad and 500Mrad μ=0.00962 $\frac{m^2}{Vs}$. As longer devices are examined, the impact of TID is lower and so for 10um length the mobility values are: in pre-rad condition μ=0.0286 $\frac{m^2}{Vs}$, under 100Mrad μ=0.0274 $\frac{m^2}{Vs}$ and under 300Mrad and 500Mrad μ=0.0269 $\frac{m^2}{Vs}$.

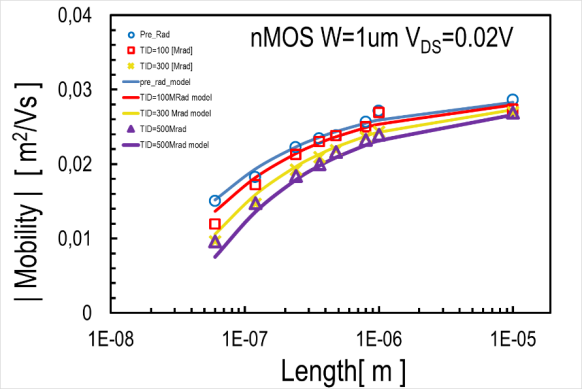

Figure 6.46 Measurement and model characteristics in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad), for mobility over Length for W=1um nMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm,800nm, 1um, 10um).

At W=20um, pMOS devices, the behavior of which is presented in figure 6.47 , it is noticed that there is a difference among the TID levels for L=60nm, where mobility in pre-rad condition is 0.00555, under 100Mrad 0.00506 and under 400Mrad is 0.00388 $\frac{m^2}{Vs}$. As the length of device raises and up to 10um length the difference of mobility among the TID levels reduces and in the largest length examined the values in pre-rad condition and under 100Mrad are equal(0.0085 $\frac{m^2}{Vs}$) and under 400Mrad is slightly lower(0.00838 $\frac{m^2}{Vs}$).

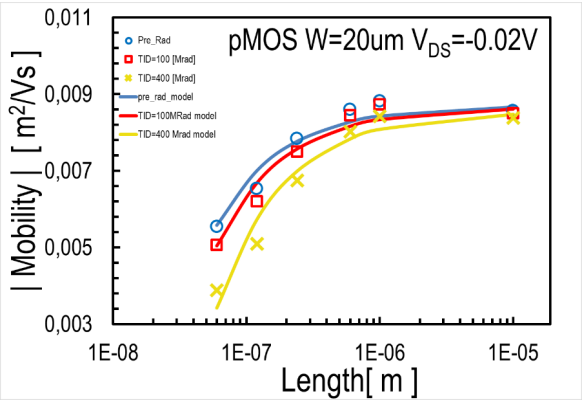

Figure 6.47 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for mobility over Length for W=20um, pMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um, 10um).

At W=20um, nMOS devices as is shown in figure 6.48 there is a difference of mobility among the TID levels, for L=60nm where in pre-rad condition mobility is 0.0119 $\frac{m^2}{Vs}$, under 100Mrad mobility is 0.0112 $\frac{m^2}{Vs}$ and under 400Mrad mobility is 0.00955 $\frac{m^2}{Vs}$. The impact of TID reduces for longer devices and it eliminates for L=240nm and keeps zero for the rest of the lengths examined up to 10um length.

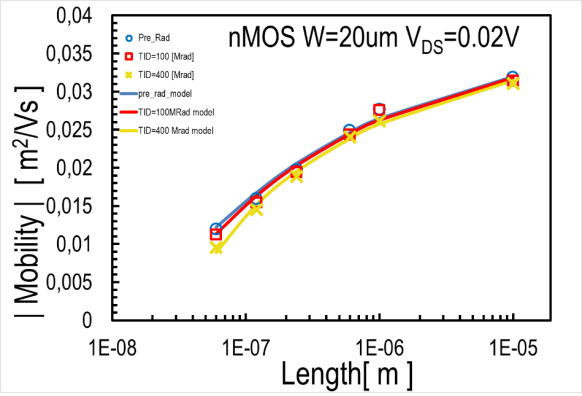

Figure 6.48 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for mobility over Length for W=20um, nMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um, 10um).

Mobility TID impact ($\frac{m^2}{Vs}$)				
nMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
L=60nm	0.015	0.0119	0.0962	0.00962
L=240nm	0.0223	0.0213	0.0184	0.0184
L=1um	0.0269	0.0244	0.0239	0.0239
L=10um	0.0286	0.0274	0.0269	0.0269
pMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.00607	0.00525	0.0028	
L=360nm	0.0091	0.0086	0.0075	
L=10um	0.0104	0.00974	0.00974	
nMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.0119	0.0112	0.00995	
L=240nm	0.0189	0.0189	0.0189	
pMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.00555	0.00506	0.00388	
L=240nm	0.00784	0.0075	0.00674	
L=10um	0.0085	0.0085	0.00838	

Table 6.20 Mobility values in linear mode for different TID levels through length scaling

Saturation mode

Through length scaling in saturation mode it is observed in general, that as the length increases the mobility incurs a raise. The only exception is the case of W=20um, pMOS devices in which the raise of mobility does not last during the whole length scaling, but up to 240nm length. Then, as length examined augments up to 10um mobility has a slight trend of fall.

For the general behavior of mobility through length scaling in saturation mode, described above a characteristic example is the diagram of W=1um, nMOS devices in figure 6.49. As it is shown for L=60nm μ=0.0154 $\frac{m^2}{Vs}$ and mobility gets higher as length increases till 10um length where μ=0.0292 $\frac{m^2}{Vs}$.

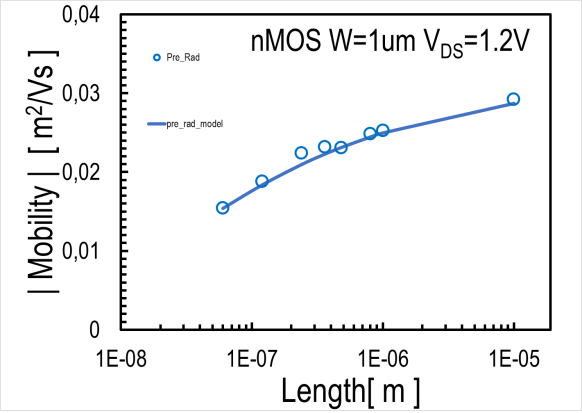

Figure 6.49 Isolated pre rad measurement and model characteristic for mobility over Length for W=1um, nMOS, saturation mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

The peculiar case of W=20um, pMOS described initially, is depicted in figure 6.50. For L=60nm μ=0.00722 $\frac{m^2}{Vs}$. As length augments, mobility increases till 240nm length for which μ=0.00881 $\frac{m^2}{Vs}$. For the rest of the lengths examined and up to 10um mobility has a small trend of fall and so for 10um length μ=0.00822 $\frac{m^2}{Vs}$.

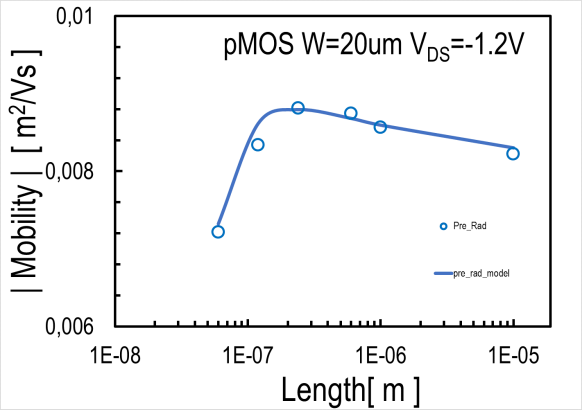

Figure 6.50 Isolated pre rad measurement and model characteristic for mobility over Length for W=20um, pMOS, saturation mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

		Mobility ($\frac{m^2}{Vs}$)			
Saturation	**Transistors**	**L=60nm**	**L=10um**	**Smallest Value**	**Largest Value**
nMOS	W=1um	0.0154	0.0292	0.0154 (60nm)	0.0292(10m)
	W=20um	0.0124	0.0299	0.0124(60nm)	0.0299(10um)
pMOS	W=1um	0.00788	0.0117	0.00788(60nm)	0.0117(10um)
	W=20um	0.00722	0.00822	0.00722(60nm)	0.00881(240nm)

Table 6.21 Mobility values in saturation mode for smallest and biggest Length examined.

As in linear mode, so in saturation it is clear that the values of mobility in nMOS devices are higher than these of pMOS

Radiation effect

After the exposure to the TID levels which are studied, it is noticed that mobility gets lower whether the TID effect is effective, as in linear mode. Thereon, different magnitudes of effectiveness are noticed in the widths and structures examined through length scaling.

At W=1um, pMOS, figure 6.51 it is noticed that there is a difference of mobility among the TID levels, the levels of which are steady as the length increases through the length scaling.

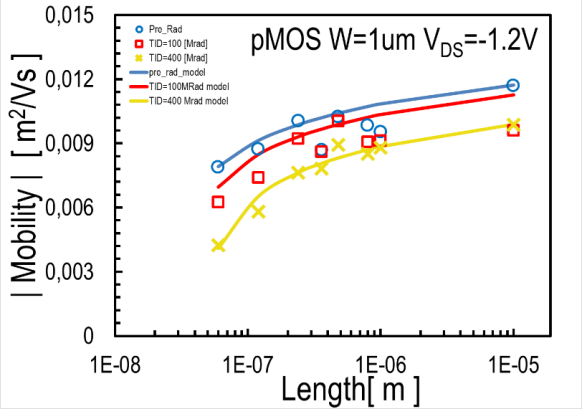

Figure 6.51 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for mobility over Length for W=1um pMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm,800nm, 1um, 10um).

At W=1um, nMOS devices the diagram of which is presented in figure 6.52 it is observed that there is a difference of mobility values among the four TID levels at 60nm length. More specifically in pre-rad condition mobility is 0.0154 $\frac{m^2}{Vs}$, under 100Mrad is 0.0135 $\frac{m^2}{Vs}$, under 300Mrad is 0.0115 $\frac{m^2}{Vs}$ and under 500Mrad is 0.00977 $\frac{m^2}{Vs}$. Through the examination of mobility in higher lengths it is noticed that as length increases from 60nm the TID differences are reducing till they get eliminated for L=360nm.The impact of TID stays at zero levels up to 10um length.

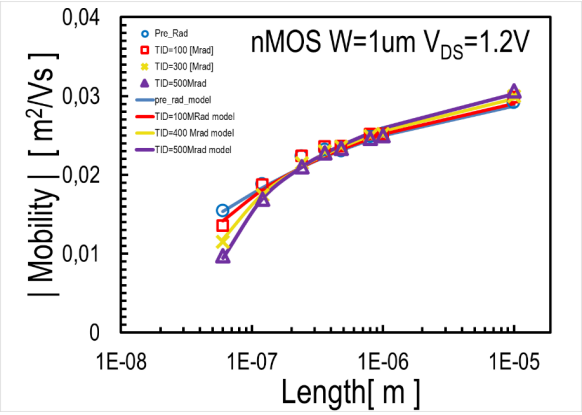

Figure 6.52 Measurement and model characteristics in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad), for mobility over Length for W=1um nMOS, saturation mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm,800nm, 1um, 10um).

Kind of the same with the above, is the appearance of TID effect on mobility of W=20um, nMOS devices, in figure 6.53. For 60nm length in pre-rad condition and under 100Mrad mobility is 0.0122 $\frac{m^2}{Vs}$ and under 400Mrad is 0.0111 $\frac{m^2}{Vs}$. As length increases the TID is less effective on mobility till it becomes zero for 120nm length. The TID impact is zero for the rest of the lengths examined up to 10um.

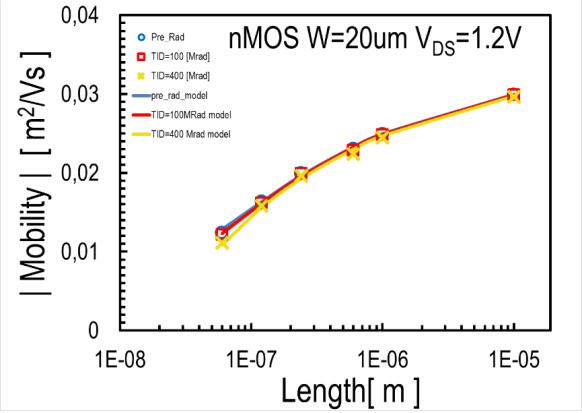

Figure 6.53 Measurement and model characteristics in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad), for mobility over Length for W=1um nMOS, saturation mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm,800nm, 1um, 10um).

At W=20um, pMOS devices for L=60nm, figure 6.54, there is a clear impact of TID on mobility. More specific, in pre-rad condition mobility is 0.00722 $\frac{m^2}{Vs}$, under 100Mrad mobility is 0.00686 $\frac{m^2}{Vs}$ and under 400Mrad mobility is 0.00531 $\frac{m^2}{Vs}$. As length examined augments the impact of TID is reducing and it becomes zero for L=10um.

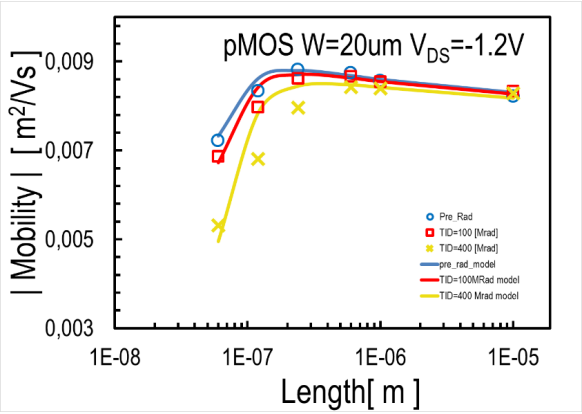

Figure 6.54 Measurement and model characteristics in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad), for mobility over Length for W=1um nMOS, saturation mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm,800nm, 1um, 10um).

Mobility TID impact ($\frac{m^2}{Vs}$)				
nMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
L=60nm	0.0154	0.013	0.0115	0.00977
L=360nm	0.0228	0.0228	0.0228	0.0228
pMOS | W=1um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.00788	0.00625	0.00424	
L=240nm	0.0101	0.00921	0.00762	
L=10um	0.0117	0.00987	0.0098	
nMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.0122	0.0122	0.0111	
L=240nm	0.0158	0.0158	0.0158	
pMOS | W=20um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
L=60nm	0.00722	0.00686	0.00531	
L=240nm	0.00881	0.00862	0.00797	
L=10um	0.00828	0.00828	0.00828	

Table 6.22 Mobility values in saturation mode for different TID levels through length scaling.

With the contribution of the table 6.22 above it could be concluded that the impact of radiation is greater in nMOS structures than in pMOS.

Width Scaling

Linear mode

In a first stage, it could be indicated that mobility levels are falling as length increases from 60nm length and it reaches the lowest value from 240 to 480nm. At the continuity of length raising, mobility incurs in a trend of fall up to either 1 or 10um, depends on the width and structure examined. Exception in this, constitutes L=10um, pMOS devices in which mobility values have a trend of fall through the whole length scaling.

Characteristic for the behavior of mobility of L=60nm devices through width is the diagram of nMOS structures, presented in figure 6.55. For W=120nm mobility value is 0.0164 $\frac{m^2}{Vs}$. With the increase of width, mobility is falling up to 240nm width, μ=0.0147 $\frac{m^2}{Vs}$. From 240nm up to 1um width mobility increases and for 1um length mobility is 0.0162 $\frac{m^2}{Vs}$.

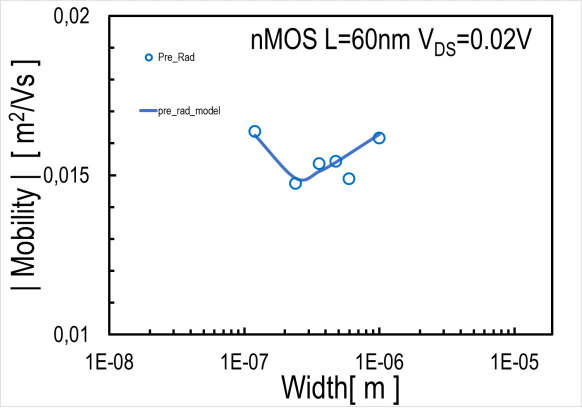

Figure 6.55 Isolated pre rad measurement and model characteristic for mobility over Width for L=60nm, pMOS, linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um).

In general lines, it could be said that the same behavior as above is followed from L=10um, nMOS structures, which are presented in figure 6.56. For W=120nm, mobility is 0.0364 $\frac{m^2}{Vs}$. For wider devices and up to 360nm width mobility falls and for W=240nm is equal to 0.0283 $\frac{m^2}{Vs}$. During the increase of width and up to 10um width, mobility is increasing and for W=10um μ=0.041 $\frac{m^2}{Vs}$.

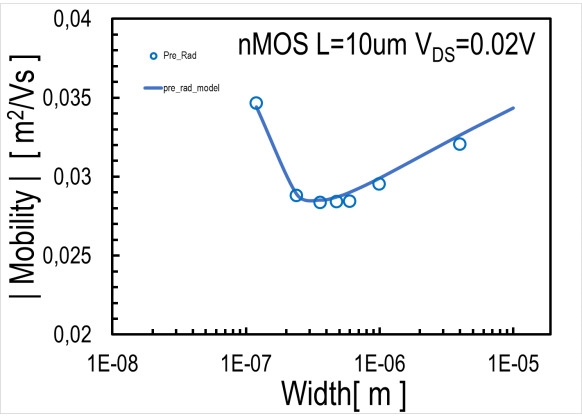

Figure 6.56 Isolated pre rad measurement and model characteristic for mobility over Width for L=10um, nMOS, linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

At L=10um, pMOS structures, figure 6.57, a fall of mobility values is observed as width increases through width scaling. Specifically, for W=120nm μ=0.0147 $\frac{m^2}{Vs}$ and for W=10um μ=0.00863 $\frac{m^2}{Vs}$.

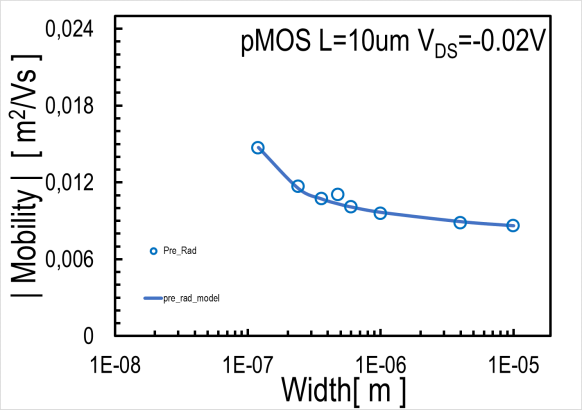

Figure 6.57 Isolated pre rad measurement and model characteristic for mobility over Width for L=10um, pMOS, linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

Mobility ($\frac{m^2}{Vs}$)					
Linear	**Transistors**	**W=120nm (W=240nm-pMOS 60nm)**	**W=10um-L=60nm W=1um-L=10um**	**Smallest Value**	**Largest Value**
nMOS	L=60nm	0.0164	0.0162	0.0147(2400nm)	0.0164(120nm)
	L=10um	0.0346	0.041	0.0283(240nm)	0.041(10um)
pMOS	L=60nm	0.00753	0.00697	0.0066(360nm)	0.00753(10um)
	L=10um	0.0147	0.0086	0.0086(10um)	0.00147(120nm)

Table 6.23 Mobility values in linear mode for smallest and biggest Width examined.

Radiation effect

The impact of radiation on mobility as it has been noted previously is that under the TID influence it gets lower values. Generally, in width scaling and in linear mode this impact is more effective in L=60nm devices and less in L=10um devices.

In L=60nm, pMOS devices, as presented in figure reffig 6.58, it is observed that there is a perceptible difference through the whole width scaling. For W=240nm in pre-rad condition μ=0.00753 $\frac{m^2}{Vs}$, under 100Mrad μ=0.00365 $\frac{m^2}{Vs}$ and under 400Mrad μ=0.000822 $\frac{m^2}{Vs}$. As the length is growing the difference among the TID levels is shrinking and the smallest difference, as it is shown, is noted for W=1um. For this width in pre-rad condition μ=0.00697 $\frac{m^2}{Vs}$, under 100Mrad is μ=0.00543 $\frac{m^2}{Vs}$ and under 400Mrad μ=0.00341 $\frac{m^2}{Vs}$.

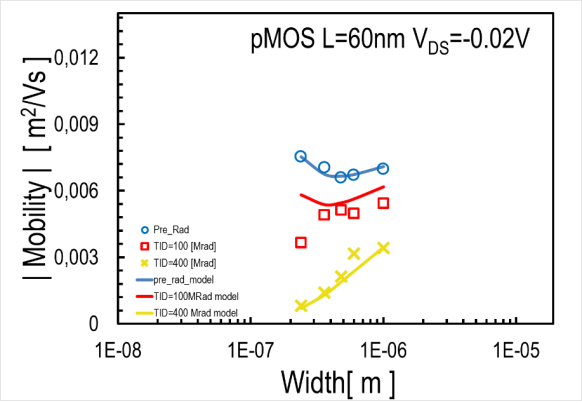

Figure 6.58 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for mobility over Width for L=60nm, pMOS, linear mode. (Widths : 120nm, 240nm, 600nm, 1um, 10um).

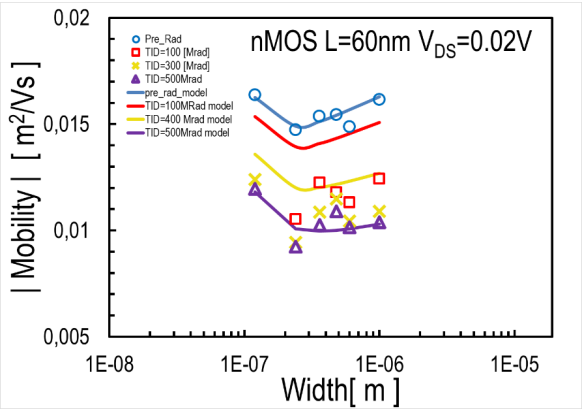

Figure 6.59 Measurement and model characteristics in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad), for mobility over Width for L=60nm, nMOS, linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um).

In L=60nm, nMOS devices, presented in figure 6.59, it is noticed that there is a very clear difference of mobility among the TID levels, which difference has a trend of increase from 360nm width till 10um. Also, the difference of mobility in pre-rad condition in compare to the irradiated conditions (100Mrad, 300Mrad, 500Mrad) is observably bigger than the difference between the mobility under 100Mrad, 300Mrad and 500Mrad. At the number's field, for W=120nm in pre-rad condition μ=0.0164 $\frac{m^2}{Vs}$, under 100Mrad μ=0.0154 $\frac{m^2}{Vs}$ and under 300Mrad and 500Mrad μ=0.012 $\frac{m^2}{Vs}$. For W=1um in pre-rad condition μ=0.0162 $\frac{m^2}{Vs}$, under 100Mrad μ=0.0124 $\frac{m^2}{Vs}$ and under 300 and 500Mrad μ=0.0104 $\frac{m^2}{Vs}$.

In figure 6.60 it is noticed that in L=10um, pMOS devices, there are not differences in the mobility values between the irradiated conditions (100Mrad, 400Mrad) from 360nm to 10um. Although the values of mobility in pre-rad condition are slightly higher the previous and as length augments this difference is shrinking and it becomes zero for W=10um. For W=360nm in pre-rad condition μ=0.0107 $\frac{m^2}{Vs}$, under 100Mrad and 400Mrad μ=0.00951 $\frac{m^2}{Vs}$.

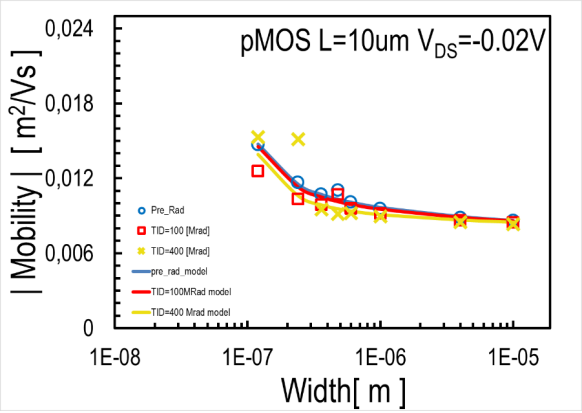

Figure 6.60 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for mobility over Width for L=10um, pMOS, linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

In L=10um, nMOS, figure 6.61, there is difference of mobility values, between the pre-rad and the irradiated conditions at narrow widths (120nm to 480nm) and for 360nm and 480nm width there is no impact of TID on mobility. For higher widths up to 10um the effectiveness of TID grows. For W=120nm in pre-rad condition μ=0.0346 $\frac{m^2}{Vs}$ and under 100Mrad and 400Mrad influence μ=0.0288 $\frac{m^2}{Vs}$. For W=10um in pre-rad condition μ=0.041 $\frac{m^2}{Vs}$, under 100Mrad μ=0.0336 $\frac{m^2}{Vs}$ and under 400Mrad μ=0.031 $\frac{m^2}{Vs}$.

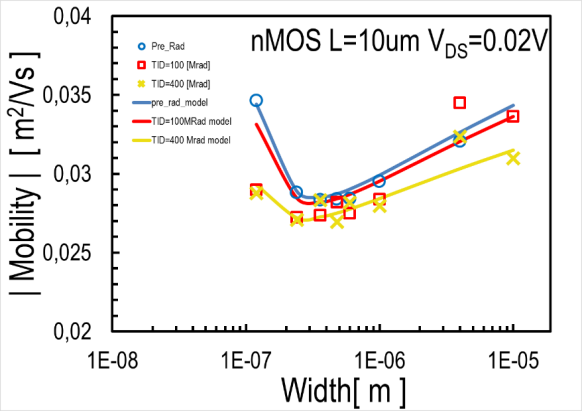

Figure 6.61 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for mobility over Width for L=10um, nMOS, linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

Mobility TID impact ($\frac{m^2}{Vs}$)				
nMOS | L=60nm	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
W=120nm	0.0164	0.0154	0.0112	0.012
W=360nm	0.0154	0.012	0.0102	0.0109
W=1um	0.0162	0.0124	0.0104	0.0104
pMOS | L=60m	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=240nm	0.00753	0.00365	0.000822	
W=10um	0.0697	0.00543	0.00341	
nMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=120nm	0.0346	0.0228	0.0228	
W=600nm	0.028	0.028	0.028	
W=10um	0.041	0.0336	0.031	
pMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=120nm	0.0107	0.00951	0.00951	
W=10um	0.00833	0.00833	0.00833	

Table 6.24 Mobility in linear mode values for different TID levels, through width scaling

Saturation mode

In saturation mode is observed a stability of mobility levels through width scaling in nMOS devices and a decrease of mobility mainly in low widths in pMOS devices.

At L=60nm, nMOS devices, mobility, which behavior through width scaling is presented in figure 6.62, for W=120nm is 0.0164 $\frac{m^2}{Vs}$ and as width augments, it's values incur a fall up to 240nm, where μ=0.0148 $\frac{m^2}{Vs}$. For the rest of the widths examined mobility keeps stable and for 10um width μ=0.0146 $\frac{m^2}{Vs}$.

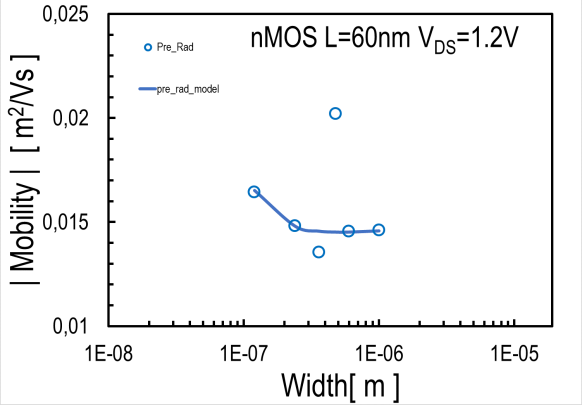

Figure 6.62 Isolated pre rad measurement and model characteristic for mobility over Width for L=60nm, nMOS, saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um).

At L=60nm, pMOS devices, figure 6.63, at 240nm width μ=0.0105 $\frac{m^2}{Vs}$ and as width increases mobility reduces up to 480nm width with μ=0.008 $\frac{m^2}{Vs}$. From 480nm width up to 1um, where μ=0.0078 $\frac{m^2}{Vs}$, mobility is kept at the same levels.

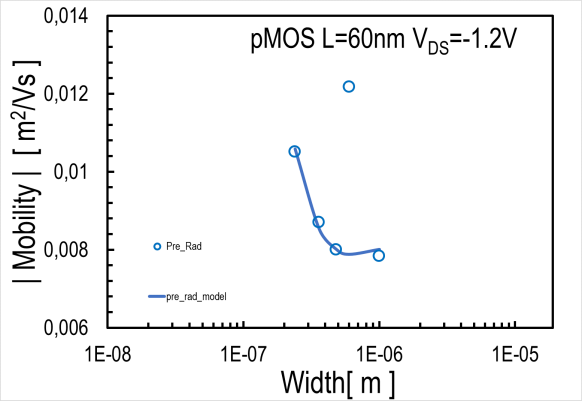

Figure 6.63 Isolated pre rad measurement and model characteristic for mobility over Width for L=60nm, pMOS, saturation mode. (Widths : 240nm, 360nm, 480nm, 600nm, 1um).

As it is observed in figure 6.64 at L=10um, nMOS devices mobility values remain at the same level from 240nm to 10um width, with μ=0.0302 $\frac{m^2}{Vs}$.

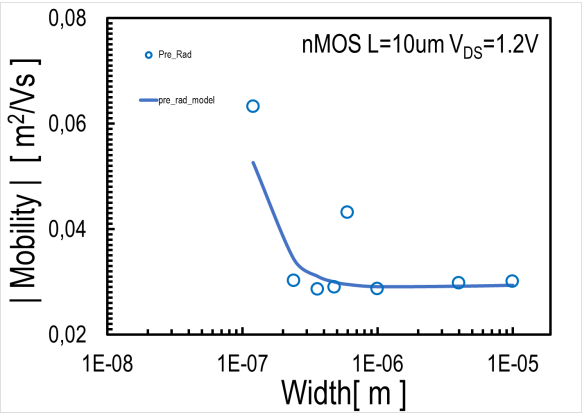

Figure 6.64 Isolated pre rad measurement and model characteristic for mobility over Width for L=10um, nMOS, saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

At L=10um, pMOS devices, presented in figure 6.65, mobility values are increasing during the whole width scaling, from 0.0179 $\frac{m^2}{Vs}$ at 120nm width up to 0.00827 $\frac{m^2}{Vs}$ at 10um width

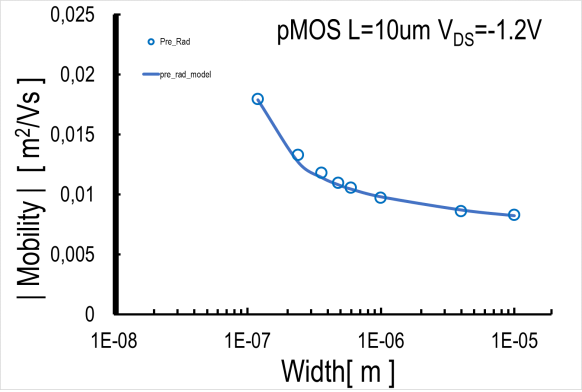

Figure 6.65 Isolated pre rad measurement and model characteristic for mobility over Width for L=10um, pMOS, saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

Saturstion	Transistors	Mobility ($\frac{m^2}{Vs}$) W=120nm (W=240nm-pMOS 60nm)	W=10um-L=60nm W=1um-L=10um	Smallest Value	Largest Value
nMOS	L=60nm	0.0164	0.0146	0.0146(1um)	0.0164(120nm)
	L=10um	0.0302(240nm)	0.0302	0.302	0.0302
pMOS	L=60nm	0.0105	0.0078	0.0078(1nm)	0.00105(2400nm)
	L=10um	0.0179	0.00827	0.00827(10um)	0.00179(120nm)

Table 6.25 Mobility values in saturation mode for smallest and biggest Width examined.

Radiation effect

As in linear mode so in saturation it can be indicated that the TID impact is clearly greater in short devices (L=60nm) than in long devices (L=10um)

At L=60nm, pMOS devices, figure 6.66, mobility values under 100Mrad are lower than these in pre-rad condition and even lower are the values of mobility under 400Mrad. At W=360nm μ=0.0087 $\frac{m^2}{Vs}$, under 100Mrad μ=0.00685 $\frac{m^2}{Vs}$ and under 400Mrad μ=0.00345 $\frac{m^2}{Vs}$. At bigger widths the difference between pre-rad and 100Mrad conditions keep steady and the difference of them with 400Mrad condition is smaller up to 1um width. At W=1um in pre-rad condition μ=0.00784 $\frac{m^2}{Vs}$, under 100Mrad μ=0.0069 $\frac{m^2}{Vs}$ and under 400Mrad μ=0.00456 $\frac{m^2}{Vs}$.

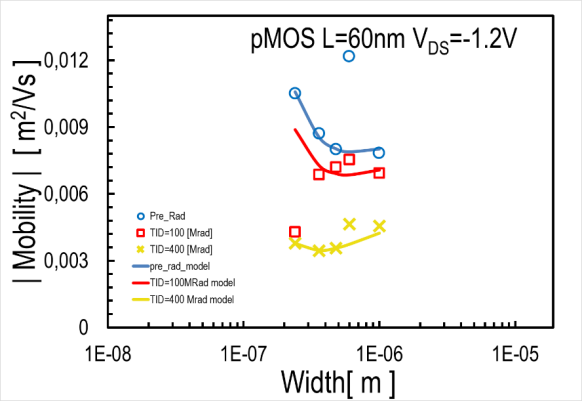

Figure 6.66 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for mobility over Width for L=60nm, pMOS, saturation mode. (Widths : 240nm, 360nm, 480nm, 600nm, 1um).

At L=60nm, nMOS, figure 6.67 devices it is observed that there are lower values for mobility in 100Mrad than in pre-rad condition. The difference between these two is kept at the same levels through width scaling. The same happens concerning the difference of mobility in pre-rad condition with 300Mrad and 500Mrad condition, but the difference with the last two conditions is much higher than with 100Mrad. At 240nm in pre-rad condition μ=0.0148 $\frac{m^2}{Vs}$, under 100Mrad μ=0.0142 $\frac{m^2}{Vs}$, under 300Mrad μ=0.012 $\frac{m^2}{Vs}$ and under 500Mrad μ=0.0111 $\frac{m^2}{Vs}$.

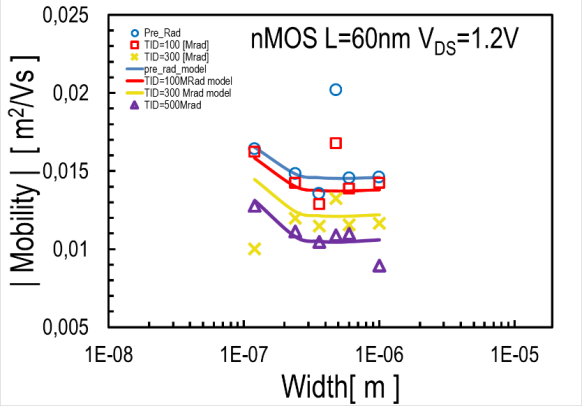

Figure 6.67 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for mobility over Width for L=60nm, pMOS, saturation mode. (Widths : 240nm, 360nm, 480nm, 600nm, 1um).

At L=10um, pMOS devices, as it is shown in figure 6.68, there is an obvious impact of TID at 120nm width. The values of mobility in irradiated conditions (100Mrad, 400Mrad) are equal and slightly lower than the value in pre-rad condition for W=360nm. More specifically in pre-rad condition μ=0.018 $\frac{m^2}{Vs}$ and under 100Mrad an 400Mrad μ=0.012 $\frac{m^2}{Vs}$. As wider devices are examined the difference between pre-rad and irradiated conditions is reducing until eliminating at W=1um. This zero TID impact is the same up to 10um width.At L=10um, nMOS devices there is not any radiation impact from 240nm width up to 10um.

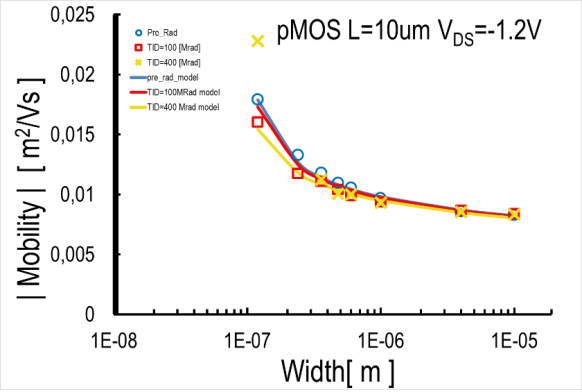

Figure 6.68 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for mobility over Width for L=60nm, pMOS, saturation mode. (Widths : 240nm, 360nm, 480nm, 600nm, 1um).

Mobility TID impact ($\frac{m^2}{Vs}$)				
nMOS | L=60nm	**TID=0Mrad**	**TID=100Mrad**	**TID=300Mrad**	**TID=500Mrad**
W=240nm	0.0148	0.0142	0.012	0.0111
W=600nm	0.0145	0.0139	0.0116	0.011
pMOS | L=60m	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=360nm	0.0087	0.00685	0.00345	
W=1um	0.0784	0.0069	0.00456	
nMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=360nm	0.018	0.012	0.012	
W=1um	0.00932	0.00932	0.00932	
pMOS | L=10um	**TID=0Mrad**	**TID=100Mrad**	**TID=400Mrad**	
W=240nm	0.0315	0.0315	0.0315	

Table 6.26 Mobility in saturation mode values for different TID levels, through width scaling.

According to the above elements in Table 6.25, it can be indicated from both width and length scaling that the impact of TID is greater and more conspicuous in linear rather than saturation mode. Although, in pre-rad condition there not seems to be any clear difference between the values of mobility. Another fact which is worth of mention is that the values of mobility are higher in nMOS devices than in pMOS, something which is extracted by all the devices that were examined. Also in the most of the devices examined it is observed that the impact of TID is greater in nMOS devices than pMOS.

6.5 Models' Error

For the investigation of models' efficacy the deviation of model evaluation from measurements data has been calculated. This calculation has been implemented firstly with an RMSE approach, according to the relation below.

for theshold voltage :

$$RMSError = \sqrt{\frac{\sum(V_{TH} - V_{TH(m)})^2}{v}} \tag{6.1}$$

For length scaling, at nMOS, W=1um:
- in linear mode, RMSE= 0.0208, 3.19%
- in saturation mode, RMSE= 0.1318, 2.76%

for d factor :

$$RMSError = \sqrt{\frac{\sum(d - d_m)^2}{v}} \tag{6.2}$$

For length scaling, at nMOS, W=1um:
- RMSE= 0.0194, 11.1%

for slope factor :

$$RMSError = \sqrt{\frac{\sum(n - n_m)^2}{v}} \tag{6.3}$$

For length scaling, at nMOS, W=1um:
- in linear mode, RMSE= 0.053, 3.93%
- in saturation mode, RMSE= 0.03, 2.31%

for mobility :

$$RMSError = \sqrt{\frac{\sum(m - m_m)^2}{v}} \tag{6.4}$$

For length scaling, at nMOS, W=1um:
- in linear mode, RMSE= 0.00093, 4.4%
- in saturation mode, RMSE= 0.00069, 3.09%

For the examining of models' evaluation success through length an absolute error has been calculated and samples of its results for each parameter examined are opposed in figures below.

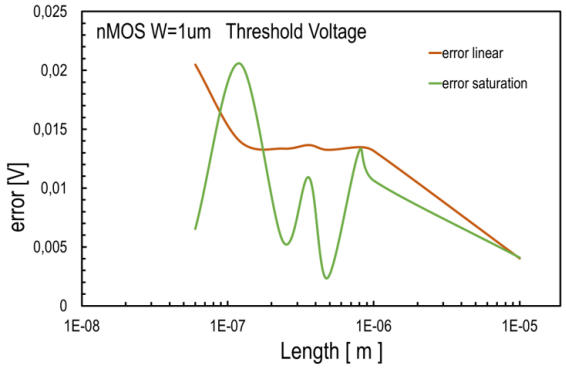

Figure 6.69 Model absolute error for threshold voltage model over length for W=1um, nMOS. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 10um).

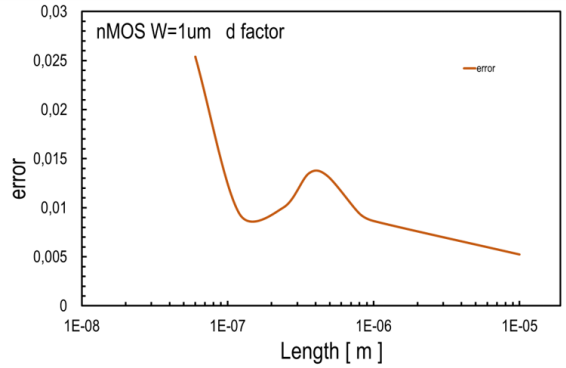

Figure 6.70 Model absolute error for d factor model over length for W=1um, nMOS. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 10um).

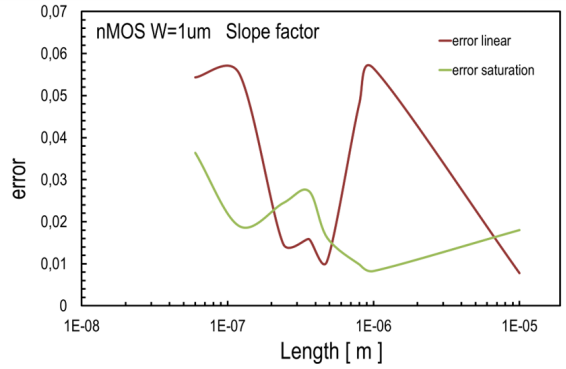

Figure 6.71 Model absolute error for slope factor model over length for W=1um, nMOS. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 10um).

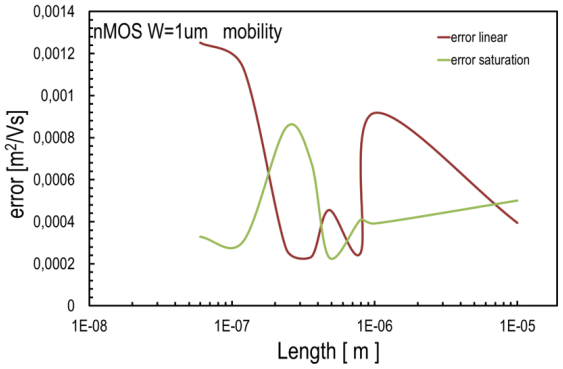

Figure 6.72 Model absolute error for mobility model over length for W=1um, nMOS. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 10um).

6.6 Results Summary

Results for Threshold Voltage

- Threshold Voltage values are greater in short and wide channel devices.
- Variation of values through width is slight
- For narrow devices, nMOS structures have higher values of V_{TO}
- For wide devices, pMOS structures have higher values of V_{TO}
- For short devices, nMOS structures have higher values of V_{TO}
- For long and wide devices, pMOS structures have higher values of V_{TO}
- Values of V_{TO} are higher in linear mode than saturation mode.
- Difference between linear and saturation mode is greater in short channel devices.
- TID impact increases the values of V_{TO} for nMOS devices.
- TID impact decreases the values of V_{TO} for pMOS devices.
- TID impact is grater in short and narrow devices.
- TID impact for wide devices is zero for medium and large lengths (240nm – 10um).
- TID impact is zero for long and wide (1um – 10um) channel devices.
- TID impact is greater for short lengths (60nm – 120nm).
- TID impact for short devices (60nm – 120nm) is greater for nMOS devices.

- TID impact in saturation mode, for nMOS devices is steady throw width and the differences among TID levels is lower than in linear mode.
- TID impact is greater in linear than saturation mode.
- TID impact variation is greater throw low widths.

Results for DIBL

- Highest values are noted in short and wide devices.
- Lowest values are noted in long and narrow devices.
- TID impact increases the values of DIBL.
- TID impact is greater in short and narrow devices.
- TID impact is lower in long and wide devices.
- TID impact is greater in nMOS than in pMOS devices.

Results for Slope factor

- Values of V_{TO} are higher for short and narrow devices.
- The smallest values are indicated for devices with channel length between 360nm and 10um and large width. Exception L=60nm, pMOS devices. .
- TID impact increases the values of slope factor
- TID impact is greater for short and narrow channel devices.
- TID impact is lower or zero for long and wide devices.
- TID impact is zero for devices with channel length between 1 and 10um and channel width between 4 and 10um.
- TID impact is greater for nMOS devices than pMOS.

Results for Mobility

- Values are lower for devices with short channel length, and medium (approximately 480nm) or wide (1 to 10um) channel width.
- Values are largest for long and narrow devices.
- Values are greater for nMOS than pMOS devices.
- TID impact decreases mobility values
- TID impact is greater for short channel devices
- TID impact has a very slight variation through width.
- TID impact is zero for long and wide devices (approximately L=10um and W=10um).
- TID impact is greater for linear mode than in saturation.
- TID impact in linear mode, is greater for nMOS than in pMOS structures.
- TID impact in saturation mode, is greater for nMOS than pMOS structure, in the most of the devices examined.

Chapter 7

Conclusion

7.1 Conclusion

In this section the behavior of Threshold Voltage, Slope Factor, Mobility and DIBL of the transistors examined for both linear and saturation mode is summarized, in pre-rad condition and under different Total Ionizing Dose levels.

In general, according to this research, its range and its object, we observe that the impact of TID is greater the shorter and narrower the transistors are. Furthermore, that nMOS devices are more influenced by the radiation over pMOS devices. Threshold Voltage is influenced more intensively in linear mode than saturation and the impact of radiation is inferior or even zero in long and wide devices. TID impact is greater in nMOS structures, although there are exceptions mainly in short and narrow devices, in which some pMOS reveal greater impact than nMOS. DIBL shows similar elements in its behavior as above. Long and wide devices are these, for which the increase of slope factor under TID, is the lowest and in most of the devices close to zero. Decrease of mobility is noted under the TID influence and most of it for the devices with the largest channel size. In linear mode, mobility values reveal a greater variation from one TID level to another. Worth of mention is also the fact that the variety of different behaviors through TID increase is significant for slope factor and mobility in opposition with threshold voltage, as well as for d factor.

This study leads to several important observations of radiation effects with width variation, mainly for slope factor and mobility. For the latter parameters, the TID impact for nMOS devices versus channel width is very weak. On the contrary, the equivalent effect is important for pMOS transistors, where TID sensitivity is highly increased for narrow channels.

Concerning the model that has been used, despite the fact that it is not perfect and may mis-evaluates some transistors, it has been shown to be very efficient. The most of the mis-evaluation are referring to the devices under the influence of 100Mrad. The main reason for not developing the model further is the need to retain the model's simplicity. The model as it stands has proven to be very useful in the extraction of several results for transistors in the range that has been examined.

These results are destined to contribute to high energy experiments and more specifically to the upgrade of the HL-LHC (High Luminosity - Large Hadron Collider) at CERN. This study should prove to be useful in designing radiation-resistant (rad-hard) electronics, such as space and biomedical applications, even though radiation doses in the latter may be significantly lower than in the present study.

7.2 Future work

Concerning future work, several directions may be suggested: namely, an evolution of the mathematical models, as well as complementing the TID effects that have been extracted.

For this study simple mathematical models have been proposed. One extension of the analysis and modeling could be to combine both length and width effect simultaneously. This could lead to a greater flexibility in foreseeing TID effects on devices that have not been included in the experiments.

A further investigation of TID effects could be profitable. This, could concern either parameters that have not been examined in this thesis or different types of MOS transistors, such as enclosed gate MOSFETs, that have a great tolerance to high levels of TID.

Finally, the investigation of TID effects in integrated circuits is a very interesting field. An approach to this could be by the study of the behavior of circuits under different levels of TID.

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Appendix A

Tables of model parameters

Threshold Voltage, length scaling

	Linear mode				Saturation mode			
	nMOS		pMOS		nMOS		pMOS	
Parameters	W=1um	W=20um	W=1um	W=20um	W=1um	W=20um	W=1um	W=20um
$\mathbf{V_0}$	0.51	0.51	0.475	0.51	0.43	0.43	0.425	0.4464
$\mathbf{V_1}$	0.06	0.055	0.04	0.036	0.05	0.04	0.012	0.0215
$\mathbf{V_2}$	-4,00E-02	-0,026	-0,005	0	-0,06	-0,07	0,006	-0,0289
$\mathbf{L_1}$	5,00E-07	6,80E-07	4,90E-07	5,00E-07	4,00E-07	6,80E-07	3,80E-07	5,00E-07
$\mathbf{L_2}$	1,00E-07	1,00E-07	1,00E-07	1,00E-07	1,20E-07	1,00E-07	1,00E-07	1,00E-07
$\mathbf{Ve_1}$	0,78	0,67	0,78	0,8	0,88	0,67	0,73	0,8
$\mathbf{Ve_2}$	2	2	2	2	2	2	2	2
$\mathbf{VT_0}$	4E-11	5E-12	8E-11	4E-11	-8E-13	-1E-11	3,5E-11	2E-11
$\mathbf{VT_1}$	7,00E-11	1,00E-11	7,80E-11	3,50E-11	1,00E-11	1,20E-11	7,80E-11	2,70E-11
$\mathbf{VT_2}$	1,75E-10	6E-11	0	-1E-11	2,8E-11	4E-13	-4E-11	-1E-11

Threshold Voltage, width scaling

	Linear mode				Saturation mode			
	nMOS		pMOS		nMOS		pMOS	
Parameters	L=10um	L=60nm	L=10um	L=60nm	L=10um	L=60nm	L=10um	L=60nm
$\mathbf{V_0}$	0,499	0,67	0,525	0,555	0,416	0,46	0,443	0,345
$\mathbf{V_1}$	0,0056	0	-0,031	0,1	-0,011	-0,02	-0,018	0,2
$\mathbf{V_2}$	-0,075	0	0,02	-0,63	-0,05	-0,0002	0,005	-1
$\mathbf{W_1}$	5,00E-07	3,00E-07	5,00E-07	3,00E-07	5,00E-07	3,00E-07	5,00E-07	3,00E-07
$\mathbf{W_2}$	1,00E-07	1,00E-07	1,00E-07	1,00E-07	1,00E-07	1,00E-07	1,00E-07	1,00E-07
$\mathbf{Ve_1}$	0,8	0,8	0,8	0,5	0,8	0,8	0,8	0,5
$\mathbf{Ve_2}$	2	2	2	2	2	2	2	2
$\mathbf{VT_0}$	1,1E-11	5E-10	2E-11	-9E-11	-5E-12	1E-10	3,6E-11	8E-11
$\mathbf{VT_1}$	1,10E-12	4,80E-10	5,00E-11	2,70E-10	-2,00E-13	8,00E-11	3,70E-11	2,70E-11
$\mathbf{VT_2}$	6E-13	-8,00E-10	1,50E-10	5,80E-09	-8,00E-12	-8,00E-11	8,00E-11	2,60E-09

Slope factor, length scaling

	Linear mode				Saturation mode			
	nMOS		pMOS		nMOS		pMOS	
Parameters	W=1um	W=20um	W=1um	W=20um	W=1um	W=20um	W=1um	W=20um
$\mathbf{n_0}$	1,4	1,22	1,495	1,19	1,27	1,227	1,41	1,19
$\mathbf{n_1}$	-0,4	0,0056	-0,12	0,0566	-0,02	0,001	-0,1	0,0396
$\mathbf{n_2}$	0,09	0,036	0,05	0,028	0,06	0,05	0,11	0,0533
$\mathbf{L_1}$	1,00E-08	5,00E-07	1,00E-06	4,00E-07	1,80E-06	5,00E-07	1,00E-06	3,00E-07
$\mathbf{L_2}$	1,00E-07	-1,00E-07	1,30E-07	1,00E-07	-1,00E-07	1,00E-07	9,00E-08	1,00E-07
$\mathbf{ne_1}$	0,3	0,3	0,35	0,6	0,3	0,3	0,3	0,6
$\mathbf{ne_2}$	2	2	2	2	2	2	2	2
$\mathbf{nT_0}$	1,5E-10	1,10E-11	-1,5E-10	1,1E-11	9E-11	9,00E-11	-2,9E-10	3,5E-11
$\mathbf{nT_1}$	7,00E-11	1,00E-11	9,00E-11	2,00E-12	2,00E-11	2,00E-11	1,60E-10	2,00E-12
$\mathbf{nT_2}$	1,00E-10	3,00E-11	4,00E-11	-3,00E-11	5,30E-11	5,30E-11	-1,00E-11	-3,00E-11

Slope, factor width scaling

	Linear mode				Saturation mode			
	nMOS		pMOS		nMOS		pMOS	
Parameters	L=10um	L=60nm	L=10um	L=60nm	L=10um	L=60nm	L=10um	L=60nm
$\mathbf{n_0}$	1,2	1,44	1,1	1,58	1,17	1,34	1,115	1,305
$\mathbf{n_1}$	0,04	-0,016	0,12	-0,057	0,41	0,02	0,23	0,6
$\mathbf{n_2}$	0,02	0,03	0,001	0,11	0,04	-0,037	0,025	-0,21
$\mathbf{W_1}$	5,00E-06	1,90E-06	5,00E-06	5,00E-06	2,00E-08	1,80E-06	2,00E-07	2,00E-08
$\mathbf{W_2}$	-1,70E-07	-6,00E-08	-1,70E-07	-1,70E-07	1,50E-07	-1,00E-07	-1,70E-07	-1,70E-07
$\mathbf{ne_1}$	0,75	0,3	0,55	0,35	0,35	0,2	0,35	0,4
$\mathbf{ne_2}$	2	2	2	2	2	2	2	2
$\mathbf{nT_0}$	4,5E-11	-6E-10	4E-13	-5E-12	9E-11	-7,5E-10	1,6E-10	1E-11
$\mathbf{nT_1}$	1,00E-12	8,50E-10	4,00E-11	5,00E-12	2,00E-10	1,00E-09	-7,00E-11	-1,00E-10
$\mathbf{nT_2}$	2,00E-10	-1,00E-09	1,80E-10	-1,80E-10	5,00E-11	-5,30E-11	2,00E-10	8,00E-10

Mobility, length scaling

	Linear mode				Saturation mode			
	nMOS		pMOS		nMOS		pMOS	
Parameters	W=1um	W=20um	W=1um	W=20um	W=1um	W=20um	W=1um	W=20um
$\mathbf{m_0}$	0,0294	0,0375	0,011	0,0087	0,0325	0,035	0,0126	0,008
$\mathbf{m_1}$	-0,011	-0,044	-0,019	-0,0006	-0,03	-0,04	-0,07	-0,0024
$\mathbf{m_2}$	-2E-06	0,0001	-3E-06	-0,004	0,0001	0,0003	-0,00015	-0,00052
$\mathbf{L_1}$	1,00E-08	1,00E-08	4,00E-07	1,00E-08	1,00E-08	4,00E-07	1,00E-08	1,00E-08
$\mathbf{L_2}$	1,90E-09	1,20E-07	1,70E-07	1,00E-08	1,20E-07	1,20E-07	1,20E-07	1,20E-07
$\mathbf{me_1}$	0,5	0,3	0,5	0,85	0,3	0,3	0,3	0,3
$\mathbf{me_2}$	2	2	2	2	2	2	2	2
$\mathbf{mT_0}$	-2,4E-12	-7,2E-13	-1,8E-12	-4E-13	4,2E-12	-4,2E-13	-4,2E-12	-2E-13
$\mathbf{mT_1}$	-1,00E-11	-4,00E-12	-2,00E-12	-1,00E-12	-9,00E-12	-9,00E-13	-3,00E-12	-9,00E-13
$\mathbf{mT_2}$	5,00E-16	-1,30E-12	-1,50E-13	1,00E-13	-2,70E-12	-1,00E-12	-9,00E-13	-1,30E-12

Mobility, width scaling

	Linear mode				Saturation mode			
	nMOS		pMOS		nMOS		pMOS	
Parameters	L=10um	L=60nm	L=10um	L=60nm	L=10um	L=60nm	L=10um	L=60nm
$\mathbf{m_0}$	0,057	0,0205	0,0076	0,0107	0,03	0,0153	0,0067	0,0115
$\mathbf{m_1}$	-0,019	-0,017	0,008	-0,017	-0,005	-0,003	0,012	-0,015
$\mathbf{m_2}$	0,0062	0,0055	0,0048	0,015	0,025	0,0038	0,0055	0,028
$\mathbf{W_1}$	0,00009	0,00000001	0,00000001	0,00000001	0,00000001	0,00000001	0,00000001	0,00000001
$\mathbf{W_2}$	0,00000015	0,0000001	0,0000001	0,0000001	0,00000012	0,0000001	0,00000012	0,0000001
$\mathbf{me_1}$	0,08	0,3	0,3	0,3	0,3	0,3	0,3	0,3
$\mathbf{me_2}$	2	2	2	2	2	2	2	2
$\mathbf{mT_0}$	-2,5E-11	-1,7E-11	8E-13	-1E-13	-2E-13	-7E-12	-2E-13	-8E-12
$\mathbf{mT_1}$	1,5E-11	2E-11	-9E-12	-3,5E-11	-4E-13	-4E-12	-2E-12	-4E-12
$\mathbf{mT_2}$	-8,5E-12	-2E-12	2E-12	-2E-11	-5E-12	3E-12	-5E-12	-4,3E-11

Appendix B

Diagrams of measurements and adjusted models that have been omitted from Chapter 6

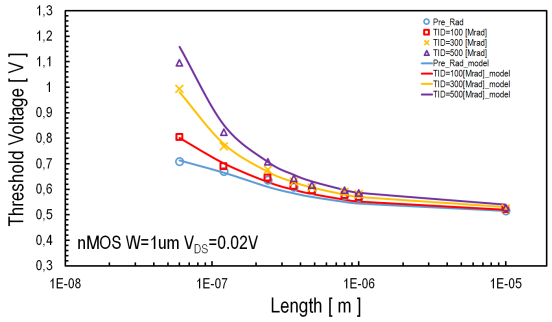

Figure B.1 Measurement and model characteristics in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad), for V_{TO} over Length for W=1um nMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm,800nm, 1um, 10um).

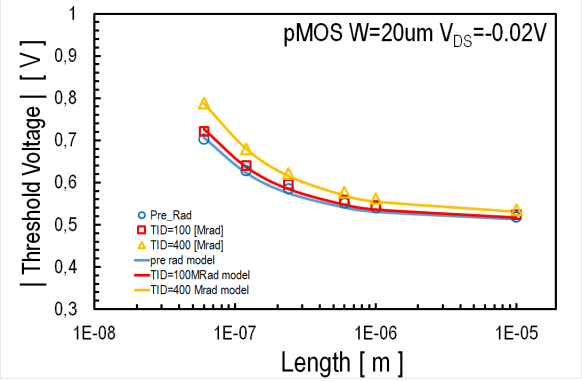

Figure B.2 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for V_{TH} over Length for W=20um pMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um, 10um).

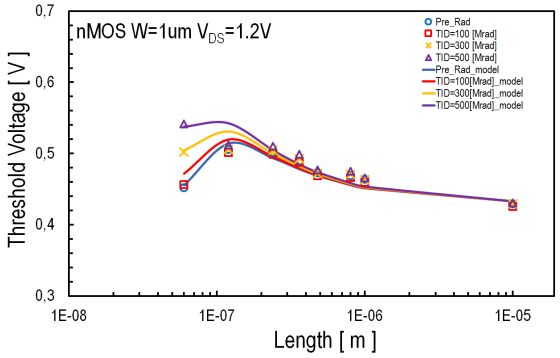

Figure B.3 Measurement and model characteristics in four radiation levels(pre rad, 100Mrad, 300Mrad, 500Mrad), for V_{TH} over Length for W=1um nMOS, saturation mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

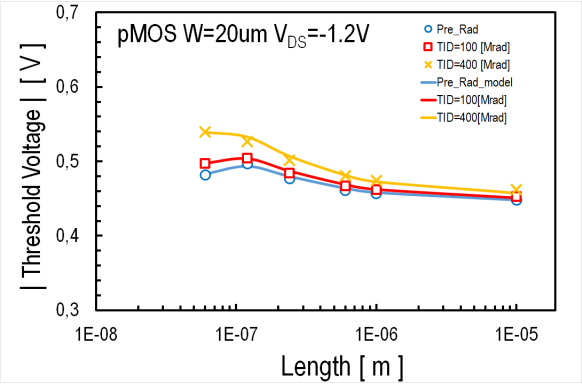

Figure B.4 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for V_{TH} over Length for W=20um pMOS, saturation mode. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um, 10um).

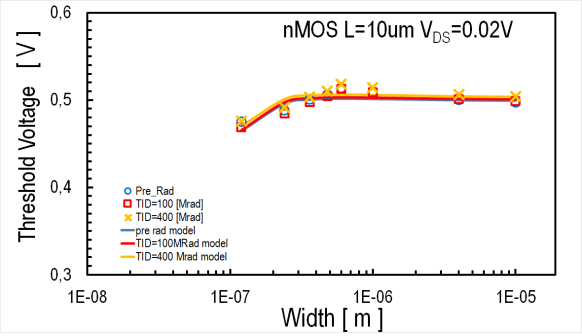

Figure B.5 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for V_{TH} over Width for L=10um nMOS, linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

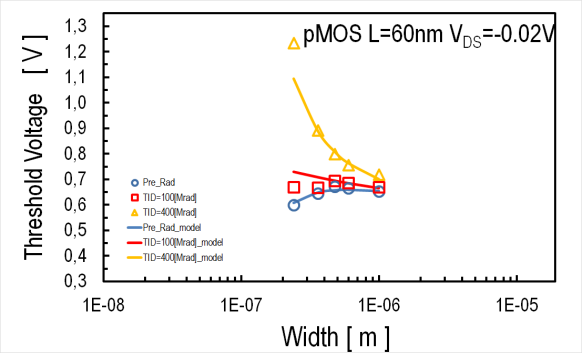

Figure B.6 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for V_{TH} over Width for L=60nm pMOS, linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

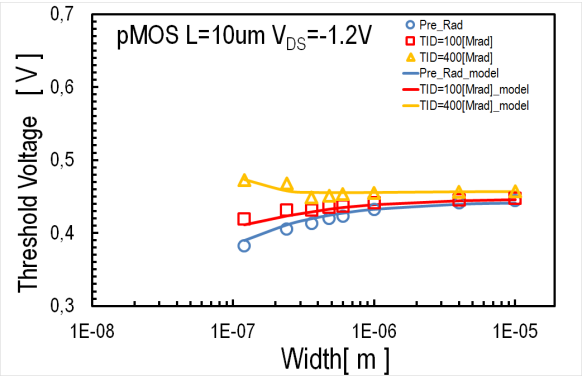

Figure B.7 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for V_{TH} over Width for L=10um pMOS, saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

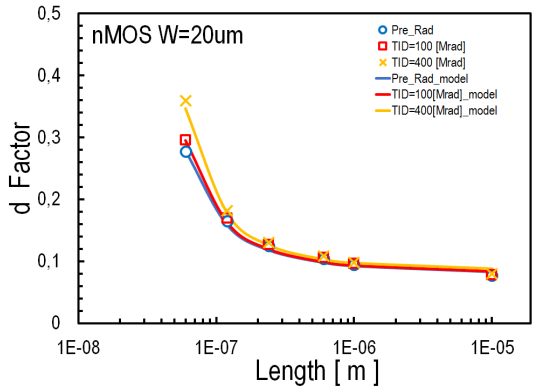

Figure B.8 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for d factor over length for W=20um nMOS. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um, 10um).

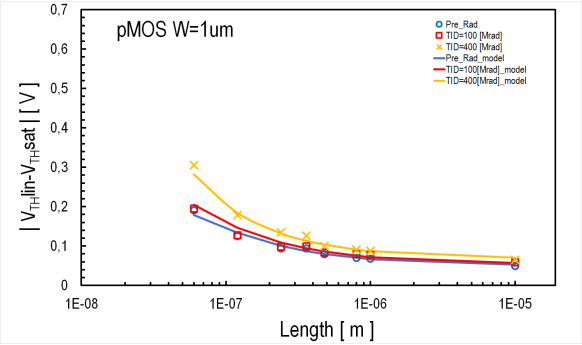

Figure B.9 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for d factor over length for W=1um pMOS. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

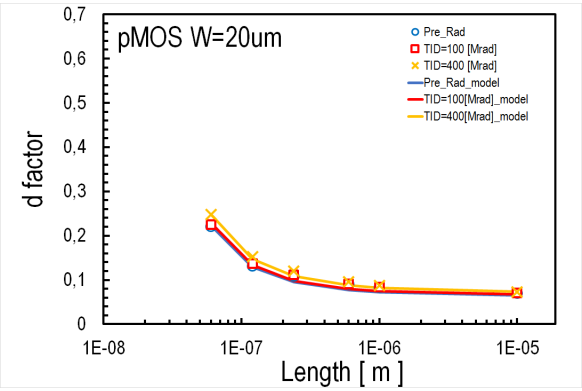

Figure B.10 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for d factor over length for W=20um pMOS. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um, 10um).

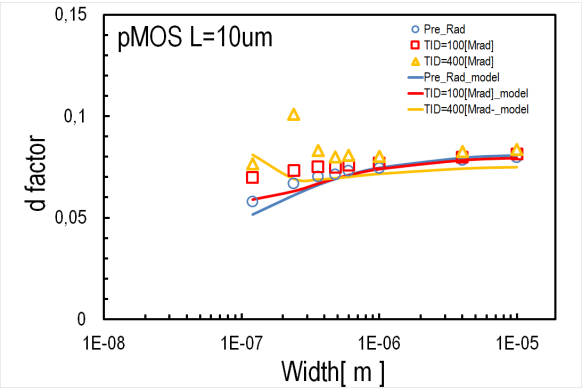

Figure B.11 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for d factor over Width for L=10um pMOS. (Widths : 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 4um, 10um).

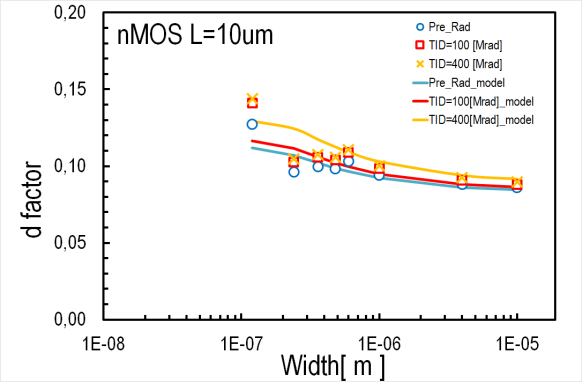

Figure B.12 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for d factor over Width for L=10um nMOS. (Widths : 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 4um, 10um).

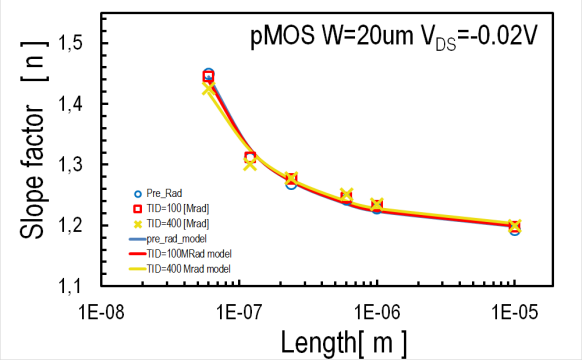

Figure B.13 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for slope factor over length for W=20um pMOS, linear mode. (Lengths : 60nm, 120nm, 240nm, 600nm, 1um, 10um).

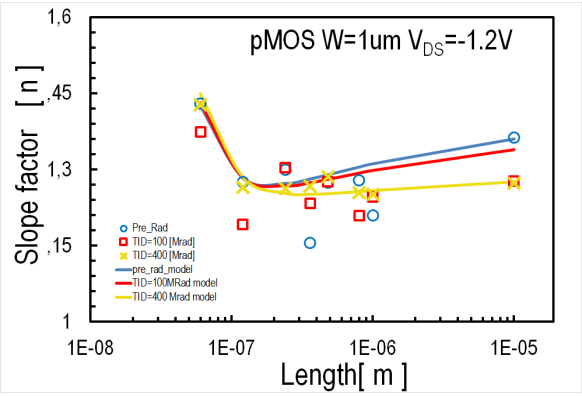

Figure B.14 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for slope factor over length for W=1um pMOS, saturation mode. (Lengths : 60nm, 120nm, 240nm, 360nm, 480nm, 800nm, 1um, 10um).

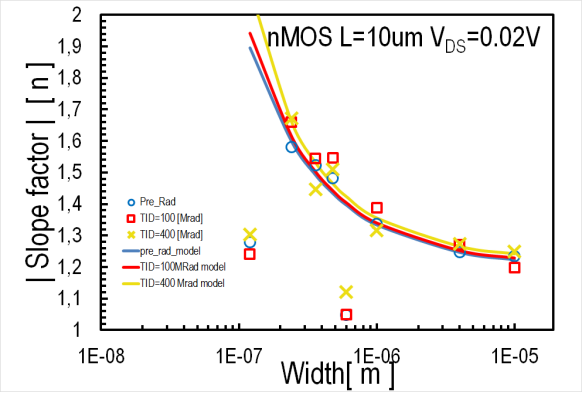

Figure B.15 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for slope factor over Width for L=10um nMOS, linear mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

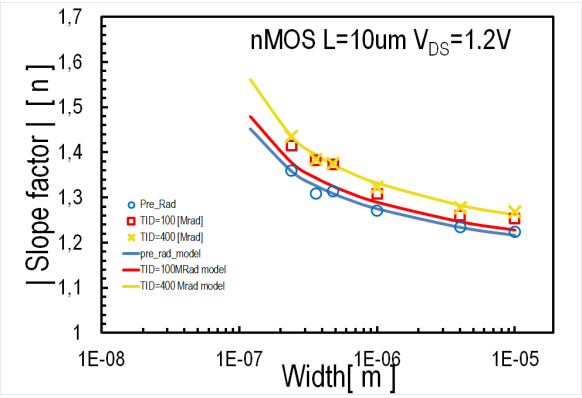

Figure B.16 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for slope factor over Width for L=10um nMOS, saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).

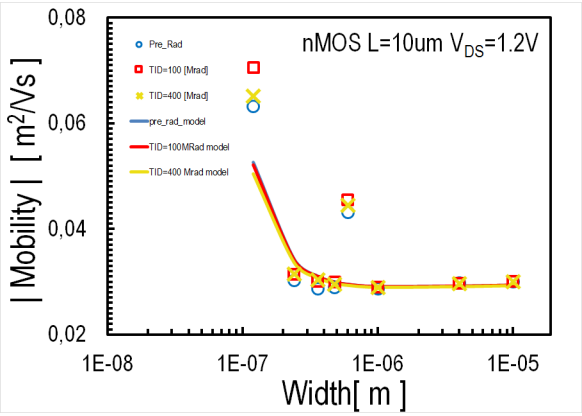

Figure B.17 Measurement and model characteristics in three radiation levels(pre rad, 100Mrad, 400Mrad), for mobility over Width for L=10um nMOS, saturation mode. (Widths : 120nm, 240nm, 360nm, 480nm, 600nm, 1um, 4um, 10um).