TECHNICAL UNIVERSITY OF CRETE
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
TELECOMMUNICATIONS DIVISION

Design and Implementation of a Low-Cost Bidirectional Embedded Backscatter Link

by

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Abstract

This work exploits low-cost, low-power and innovative hardware solutions for bidirectional backscatter links at 2.4 GHz. Moreover, a custom backscatter tag for sensing and RFID application is designed and implemented, able to send data up to 60 meters away with packet error rate (PER) in the order of 3.7%. The tag is also capable of receiving data and its power consumption can be less than 0.27 mW for 4.5 seconds of continuous operation. The tag cost per unit does not surpass 5 Euros. The receiver of the tag is based on a custom, comparator-based design, using on-off keying (OOK) modulation. In addition, a solar energy harvesting system is designed, offering an energy-autonomous link. Based on this tag, a prototype environmental humidity sensor node is implemented and demonstrated.

Acknowledgements

First of all, I would like to thank my supervisor Prof. Aggelos Bletsas for his guidance and support throughout this work and beyond that. I would also like to thank my friends and colleagues Thanos Nichoritis and Georgios Vougioukas for all the help they provided during my work in the laboratory.

A huge thank you goes to my mother for all the support during these years. I also would like to thank my brother for all the useful advice on analog circuit design he gave me during my undergraduate years.

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Chapter 1

Introduction

1.1 Internet of things

Nowadays, more and more physical devices are connected to the Internet and are capable of collecting and sharing data due to the arrival of super-cheap computer chips and the ubiquity of Wireless Sensor Networks (WSNs) forming what is known as Internet of Things (IoT) [7]. Therefore, WSNs and IoT are strongly related. With the arrival of 5G more research is expected to be devoted to subjects which are related to IoT.

1.2 Why Backscatter Radio?

Commercial products are using standardized protocols (e.g., Bluetooth, WiFi) in order to achieve connection to the internet; a typical scenario would be the appliances inside a "smart home". However, in agricultural applications where electrical supply from the power grid is not readily available, products with low-power consumption are mandatory in order to extend the battery life and achieve operating times of several years. Moreover, in smart agriculture, a conventional environmental sensor, which sends the data through standardized wireless protocols has a cost in the order of 20 Euros and its current consumption can be lower than 20 mA. So, in a scenario where it is required to monitor the soil moisture of hundreds of plants, the idea of using the hardware that is available in the market is prohibitive.

Therefore, we propose the use of backscatter radio, precisely long-range Radio Frequency Identification (RFID) links. This approach consists of:

- an unmodulated carrier transmitter (illuminator),
- multiple RFID sensor-tags (nodes),

- an embedded receiver.

1.3 State-of-the-Art Solutions

With the above-mentioned system, ranges up to 246 meters have been achieved using Frequency Domain Multiple Access (FDMA) schemes and with an average current consumption of 20 μA per tag/node.Also, each node was ambiently powered and its cost was in the order of 4 Euros [8].

1.4 Research Goals

This thesis focuses on the design of innovative, low-power and low-cost hardware solutions for RFID tags which in contrast with previous works can also receive data. Our proposal setup is like the setup we described above with the addition of a On-Off Keying (OOK) transmitter. The link where data is transmitted from the OOK transmitter to the tag is called downlink, and the link where the tag transmits data to the embedded receiver (central receiver) is called uplink (Fig. 1.1). We assume for simplicity that the carrier-emitter is a separate module from the OOK transmitter, but they can be implemented in the same embedded radio using protocol multiplexing. Another research goal is how this link can operate using ambient energy.

The main contributions of the thesis are listed below:

1. Design of an OOK receiver at 2.4 GHz for the tag (Chapter 2)
2. Design of an RFID tag which transmits data through the uplink communication channel (Chapter 3)
3. Design of an energy harvesting system for the embedded radios (Chapter 4)
4. Design of an interconnection between the tag and a soil moisture sensor, where the tag transmits the sensor's data back to the central embedded receiver (Chapter 5) (see Fig. 1.1)

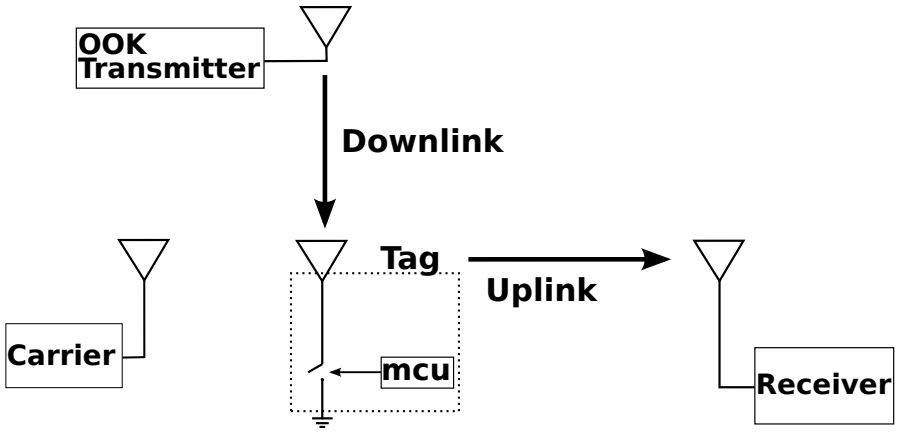

Figure 1.1: Proposed bidirectional backscatter link.

Chapter 2

Tag Receiver

The simplest approach to demodulate an amplitude-modulated (AM) signal is through an envelope detector. The OOK is the simplest version of ASK and has only two distinct values (high or low). Thus, when the carrier is transmitted, that equals a logic bit "1" and when not, that equals to a logic bit "0".

$$c(t) = A \cdot \cos(2\pi f_c t), \tag{2.1}$$

$$x(t) = m(t)c(t) = A \cdot m(t) \cdot \cos(2\pi f_c t), \tag{2.2}$$

where $c(t)$ represents the carrier signal, $m(t)$ the baseband signal, and $x(t)$ the modulated RF signal. m(t) can take only two discrete values 1 or 0.

2.1 Envelope-detector (Demodulator)

In this work, two different topologies of envelope detectors are implemented:

1. single detector (Fig. 2.2)
2. voltage-doubler (Fig. 2.3)

The detectors are "zero-biased", which means there is no need for external dc power supply. The diodes are operating in the subthreshold region (under the knee of the I(V) characteristic shown in Fig. 2.1). The diode current is described by Shockley's equation

$$I_D = I_S(e^{\frac{V_{in}}{nV_T}} - 1), \tag{2.3}$$

where I_S is the saturation current, $V_{in} = x(t)$ (RF-signal) (2.2), n is the ideality factor (quality factor) and V_T is the thermal voltage. The video or small-signal dynamic resistance $R_v \triangleq R_S + R_j$ (Fig. 2.4) of the diode with the combination of

the shunt capacitor C_1, forms a first-order low-pass filter (Fig. 2.2) with a cut-off frequency of

$$f_{-3dB} = \frac{1}{2\pi R_v C_1}. \tag{2.4}$$

From small-signal analysis, I_D can be decomposed based on the Taylor series expansion:

$$f(\alpha) + f^{'}(\alpha) \cdot (x - \alpha) + \frac{f^{''}(\alpha)}{2} \cdot (x - \alpha)^2 + \dots \tag{2.5}$$

For $\alpha = 0$, a Maclaurin series follows:

$$I_D(0) + I_D^{'}(0) \cdot x(t) + \frac{I_D^{''}(0)}{2} \cdot x^2(t) + \cdots <=> I_S \cdot x(t) + I_S \cdot \frac{x^{'}(t)}{2} \cdot x^2(t) + \dots \tag{2.6}$$

From (2.6 and 2.2) the following equation is extracted:

$$x^2(t) = A^2 \cdot m^2(t) \cdot \cos^2(2\pi f_C t) = \frac{A^2 m^2(t)}{2} \cdot [1 + \cos(4\pi f_c t)], \tag{2.7}$$

where $x(t) = V_{in}$ (RF-signal). The terms, which have frequencies above the bandwidth of $m(t)$ are blocked by the low-pass filter. So, I_D is proportional to $x^2(t)$ and, thus, the envelop detectors follow the "square law" [9]. Because of that, the output of the detector is proportional to the RF-input signal power.

I_D can be easily converted into voltage through a load-resistor R_{load}. This resistor must be high in the range of hundreds of $k\Omega$, in order to extract the largest possible voltage swing [10]. The voltage across R_{load} can be described as:

$$V_{out} = k \cdot P_{in}, \tag{2.8}$$

where k is the efficiency or the sensitivity of the detector and depends only on the characteristics of the diode [11]. For this application, special types of diodes are manufactured which have high k and I_S current in the order of several μA. These diodes are called zero-biased RF-Shottky. Furthermore, these detectors are extracting the demodulated signal in the DC band. Thus, they can be characterized as homodyne detectors.

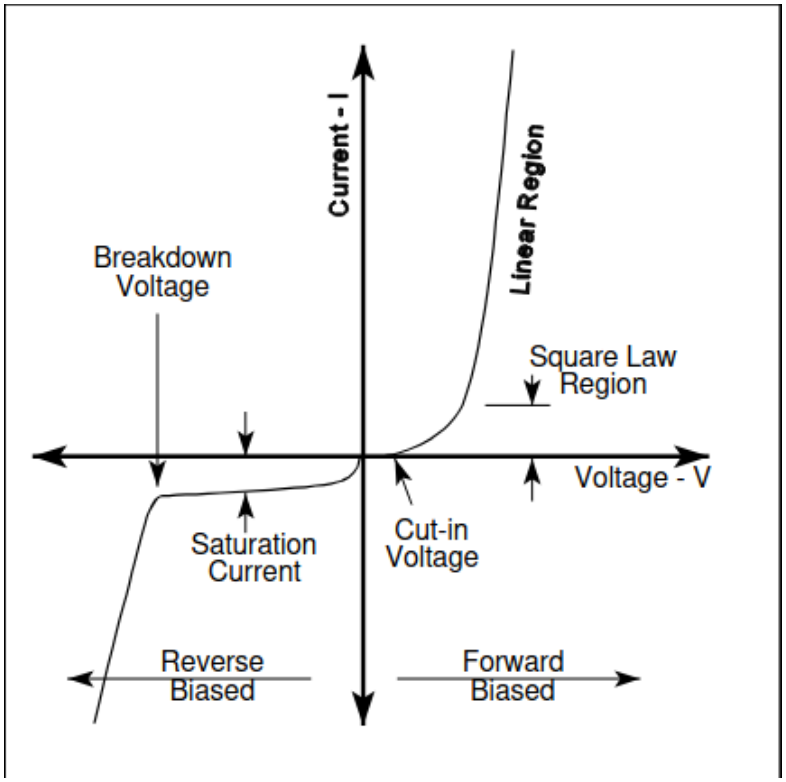

Figure 2.1: Diode's I(V) characteristic curve [1]. V(mV). The I axis and V axis are presented in absolute values. The upper I axis is given in mA, while the lower I axis in μA.

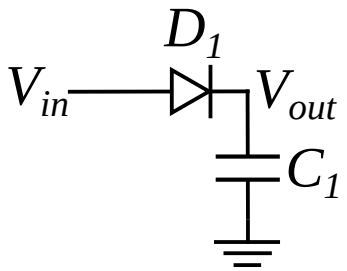

Figure 2.2: Single diode envelope-detector schematic

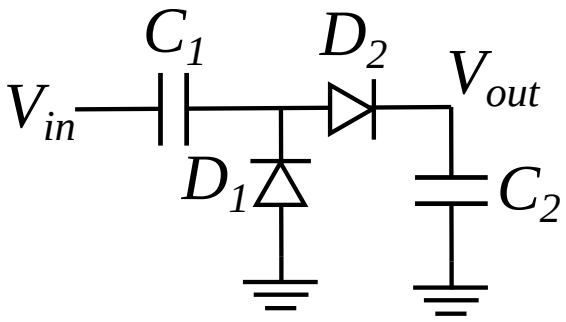

Figure 2.3: Voltage-doubler envelope-detector schematic [2].

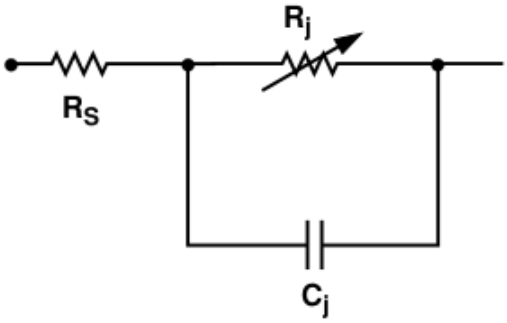

Figure 2.4: Equivalent linear circuit model of the diode. R_S is the series resistance, R_j is the junction resistance and C_j is the junction capacitance. The last two are varying according to the bias current [3].

2.1.1 Design and Simulation

For the diodes, we used the SMS7630-005LF from Skyworks because they offer good sensitivity at high frequencies up to 24 GHz at a very low price. This satisfies our requirements by a large margin because the working OOK frequency for our system is 2.4 GHz.

For simulation purposes, LTspice from Analog Devices was used, and the following SPICE parameters of the Skyworks diode were entered in the simulation software:

IS	5E-6
RS	20
N	1.05
CJ0	0.14E-12
M	0.40
EG	0.69
XTI	2
FC	0.5
BV	2
IBV	1E-4
VJ	0.34

Table 2.1: The implemented Spice-model of the diode SMS7630 in LtSpice [12].

At first, the video resistance of the diode was extracted from DC analysis and was found to be equal to $R_v = 5.43k\Omega$. The bandwidth of the detector is determined by the low-pass filter (2.4). To achieve good SNR, it is mandatory to limit the noise floor. The spectral density of the thermal noise is given by

$$N_0 = k \cdot T, \tag{2.9}$$

where k is the Boltzman's constant ($1.38 \cdot 10^{-23}$ Joule/K) and T is the temperature in Kelvin. The power of thermal noise is

$$P_{noise} = N_0 \cdot BW \cdot NF, \tag{2.10}$$

where BW is the bandwidth of the receiver and NF is the noise figure. So, by

designing the low-pass filter narrow, higher SNR is accomplished and therefore higher sensitivity. The BW must be just wide enough to allow the baseband signal m(t) to pass unattenuated (which was considered to have 100Hz bandwidth for demonstrating purposes). In conclusion, the targeted BW of the detector must be approximately 200 Hz. From (2.4) the desired value of capacitor C_1 is 150 nF. Also, the cut-off frequency of the filter needs to be $f_{-3dB} << f_c$, which is valid because 200 Hz << 2.4 GHz. Additionally, the capacitor C_1 must be large enough in order to present a short circuit for the RF-signal [10]. The impedance of C_1 at 2.4 GHz is 0.0004Ω. The two circuits were simulated for different capacitor values in Fig. 2.5-2.8.

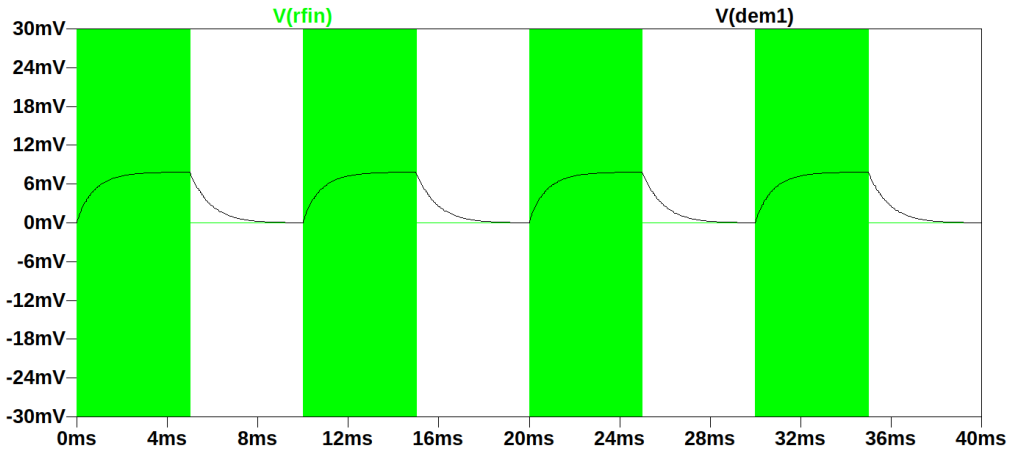

Figure 2.5: Simulation of the single-diode envelope detector (Fig. 2.2) with the capacitor of the BW filter to be equal with $C_1 = 150$ nF. The waveform which has a voltage-swing from −30 to 30 mV represents the RF-input singal, while the square waveform represents the demodulated output signal.

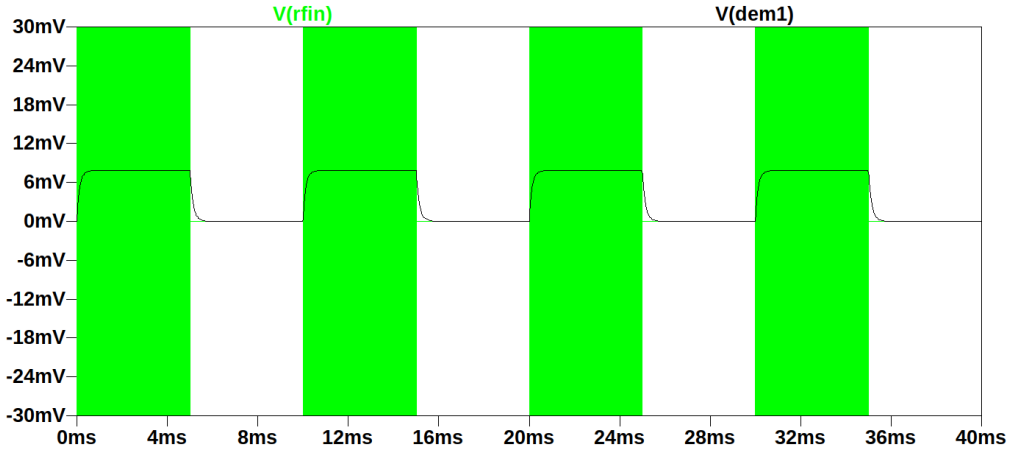

Figure 2.6: The respective simulation of the single-diode envelope detector (Fig. 2.2) with the capacitor of the BW filter to be equal with $C_1 = 1$ nF.

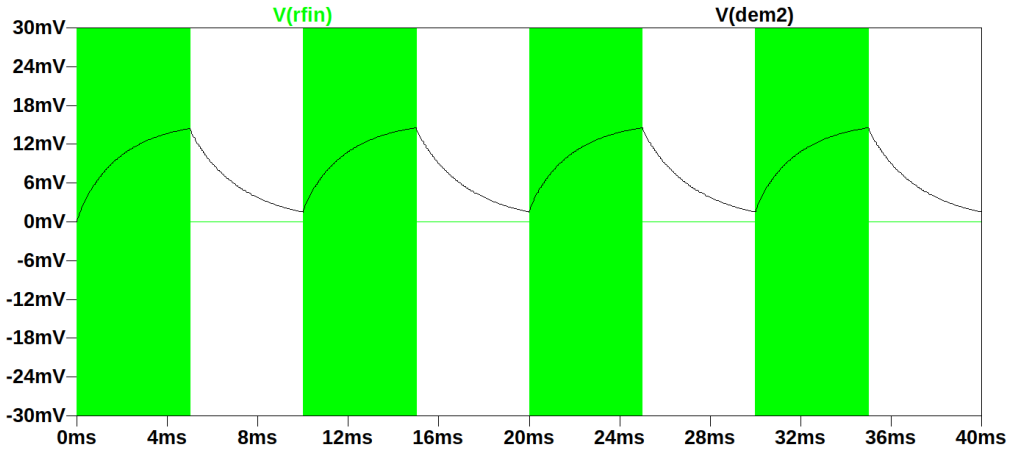

Figure 2.7: The respective simulation of the voltage-doubler envelope detector which has the filter capacitors to be equal with $C_1 = C_2 = 150$ nF.

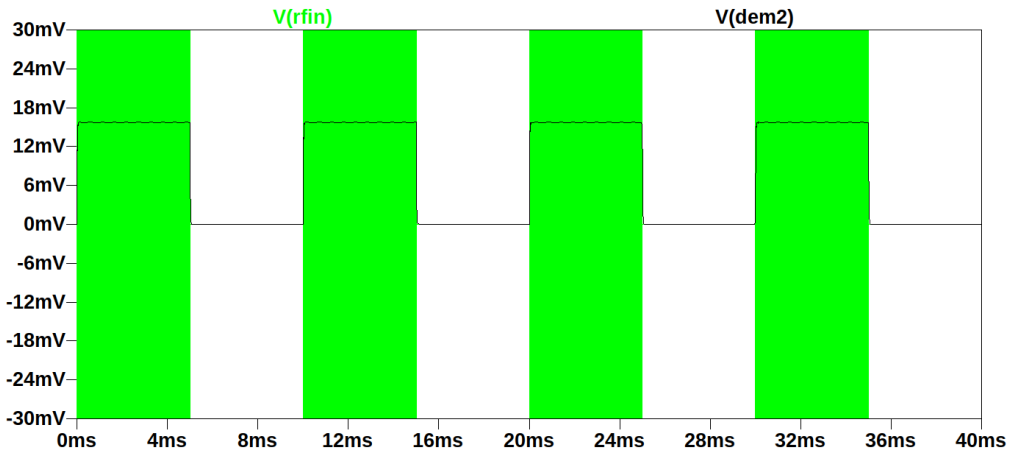

Figure 2.8: Simulation of the voltage-doubler envelope detector for $C_1 = C_2 = 1$ nF.

2.1.2 Layout

As shown in (2.8), for achieving the maximum available V_{out} at a specific power P_{in}, the impedance of the source should be matched to the impedance of the detector to eliminate reflections (3.1) [13]. For this reason, testing circuits are designed in order to measure the impedance of the envelope detector.

At the beginning, two (2-layer) PCBs were designed for the first circuit (Fig. 2.2) using the freeware KiCad software and following two different structures:

- coplanar waveguide,
- microstrip waveguide,

(fig. 2.9). Then, a calibration process took place on the Rodhe & Schwarz ZNB4 vector-analyzer (VNA) at 2.4 GHz. Next, the two PCBs were connected in the VNA for measuring the input-impedance of the detector. The impedance depends on the frequency and the input-power. Therefore, the VNA was set at a fixed 2.4GHz frequency and the power was being swept from -40 to $+10$ dBm.

For the coplanar setup, the measurement results are not promising. The marker of the impedance is on the positive half-cycle of the Smith-Chart and very unstable due to parasitic phenomena. According to the theory, the expected impedance must be in the negative half-cycle because the diode constitutes capacitive load. Thus, we consider that this waveguide is not appropriate for our design.

On the other hand, the microstrip offers better stability in the impedance and the impedance-marker is in the negative half-cycle. So, we decided to continue the design with this approach. It should be mentioned that the waveguides are matched to 50 Ω. Using KiCad's waveguide calculator for the 1.5mm FR-4 PCB at 2.4 GHz, a trace width 13.76 mils was sufficient to ensure 50 Ω matching for our mictrostrip design (Fig. 2.9).

Afterwards, the PCB for the voltage-doubler detector was designed using the microstrip waveguide (Fig. 2.10). It should be noted that the fabrication process of all PCBs was conducted inside the lab.

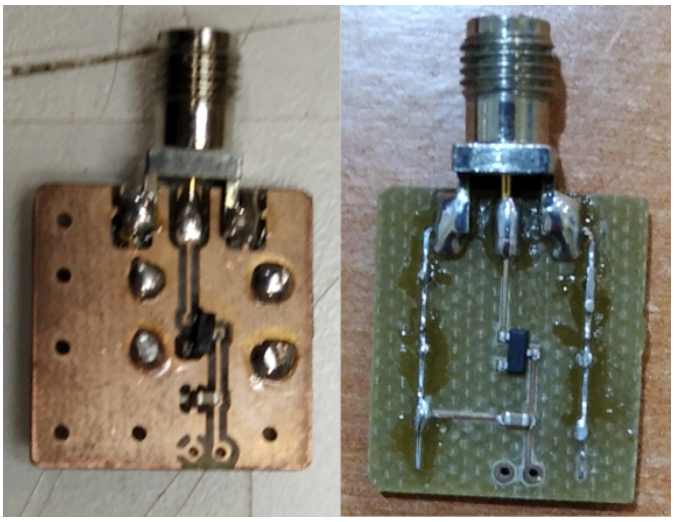

Figure 2.9: Testing PCB of the single-diode envelope-detector for the purpose of measuring the input impedance. The left picture shows the implementation with the coplanar waveguide, while the right shows the microstrip.

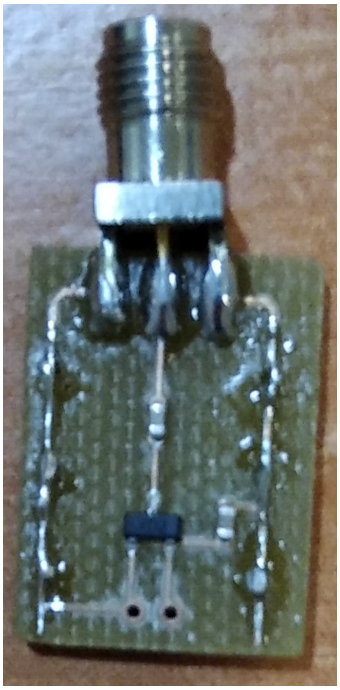

Figure 2.10: Testing PCB of the voltage-doubler envelope-detector for the purpose of measuring its input impedance.

2.1.3 Input-impedance Measurement

The two testing circuits (Fig. 2.9 and Fig. 2.10) are measured in the VNA for different values of input power (at 2.4 GHz).

P_{in} (dBm)	Z_{in} (Ω)
-40	$10 - j41$
-30	$10.226 - j37.655$
-20	$10.018 - j38$
-10	$9.761 - j39$
-5	$9.813 - j40$
0	$9.98 - j41$
5	$10 - j43$
10	$11 - j44$

Table 2.2: Input impedance measurements of the single-diode envelope-detector from the VNA.

P_{in} (dBm)	Z_{in} (Ω)
-40	$141.208 - j17$
-30	$112.628 - j86$
-20	$116.507 - j85.507$
-10	$135.20 - j70$
-5	$139 - j55$

Table 2.3: Input impedance measurements of the voltage-doubler envelope detector from the VNA.

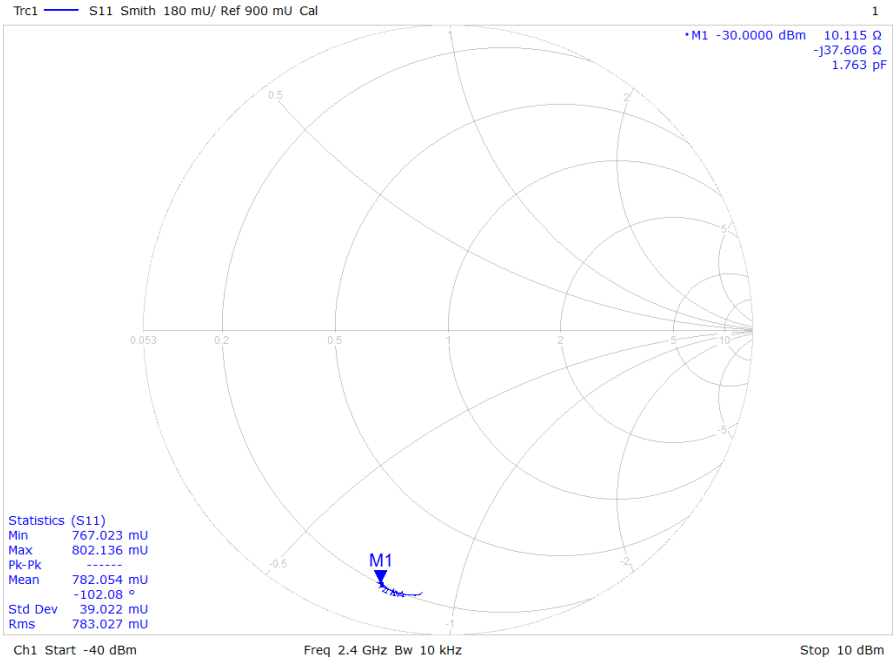

Figure 2.11: Impedance measurement of the single diode detector's input at −30 dBm input power.

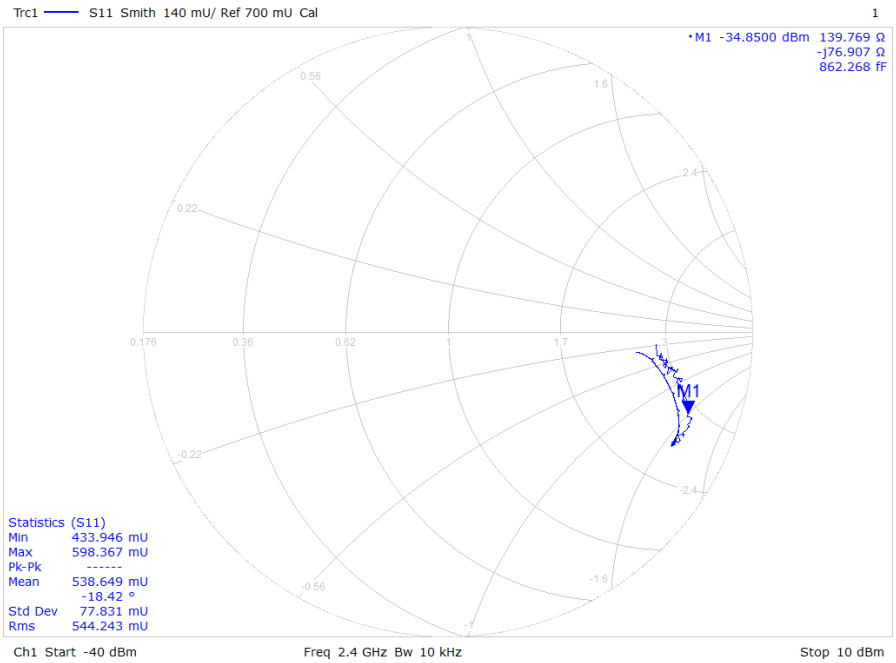

Figure 2.12: Input impedance measurement of the voltage-doubler detector's input at −34.85 dBm input power

2.1.4 Implementation

At this step the impedance of the detectors is known; the next step is to design the appropriate matching networks for the detector's impedance at 50 Ω (antenna's impedance). For the matching network, the selected topology is the low-pass L-network, which consists of a series inductor with a shunt capacitor (Fig. 2.13).

The matching procedure is followed for the case of $P_{in} = -30$ dBm at 2.4 GHz in both detectors (Fig. 2.2 & 2.3). Using a matching network calculator [14], which implements all the calculations on the Smith-Chart, the values of the network's passive components were found to be equal to: $L = 3.834$ nH and $C = 2.616$ pF. Respectively for the second circuit (Fig. 2.14) $L = 5.311$ nH and $C = 0.3118$ pF. The final component values for the network, using standard values, are given in Table 2.4.

	L (nH)	C (pF)
single-detector	3.8	2.6
voltage-doubler	5.3	0.33

Table 2.4: Standardized values of matching-network's passive components.

Next, four PCBs are constructed for the implementation of the two detectors. In particular, two versions of each detector are implemented, where each version has different filter capacitors, i.e., C_1 and C_2. These values are the same as the simulated circuits.

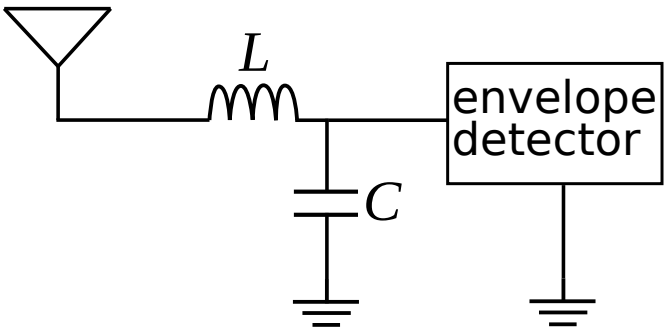

Figure 2.13: Matching-network interface with the detector.

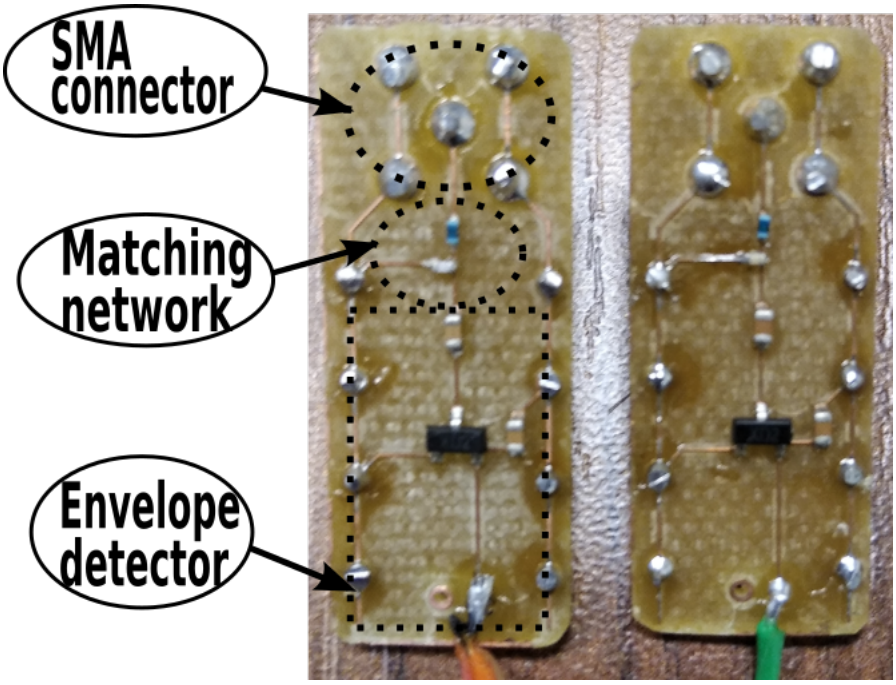

Figure 2.14: The two voltage-doubler envelope-detectors implemented on PCBs. On the left, the version with 1 nF filter capacitors is shown, while on the right lies the version with 150 nF.

2.1.5 Experimental results

The Tektronics AFG3021B signal generator is producing a square-wave signal m(t) with 50% duty cycle, 100 Hz frequency and 2 V_{pp} amplitude. This signal is being driven into the Agilent N5181A RF-generator. The RF-generator is applying amplitude-modulation on a 2.4 GHz carrier using the square-wave signal as reference. The modulated RF-signal is transmitted through a 2.4GHz antenna. At a distance of d = 2.13 m the voltage-doubler envelope-detector is placed, connected to an Agilent DSO1002A oscilloscope for monitoring its output (Fig. 2.17). By changing the power of the RF-generator, the amplitude of the detector's output voltage is being recorded (Fig. 2.15). It is observed that the detector with the $C_1 = C_2 = 1$ nF filter capacitors produces a clean square waveform due to the faster charging and discharging times of the capacitors, in contrast to the other version of the detector with 150 nF filter capacitors (Fig. 2.15). On the other hand, the detector with the 150 nF filter capacitors is achieving larger voltage

swing due to the fact that it is better matched to 50 Ω. Better matching is equivalent with larger input power at the diode and based on (eq. 2.8) can be converted into larger output voltage amplitude.

	V_p (mV)	V_p (mV)
P_{out} (dBm)	$C_1 = C_2 = 150$ nF	$C_1 = C_2 = 1$ nF
9	8	4
12	12	10
15	28	16
18	40	26
21	78	68

Table 2.5: The recorded amplitude of the output voltages of the two voltage-doubler envelope detectors for various power-levels of the RF-generator (Fig. 2.15).

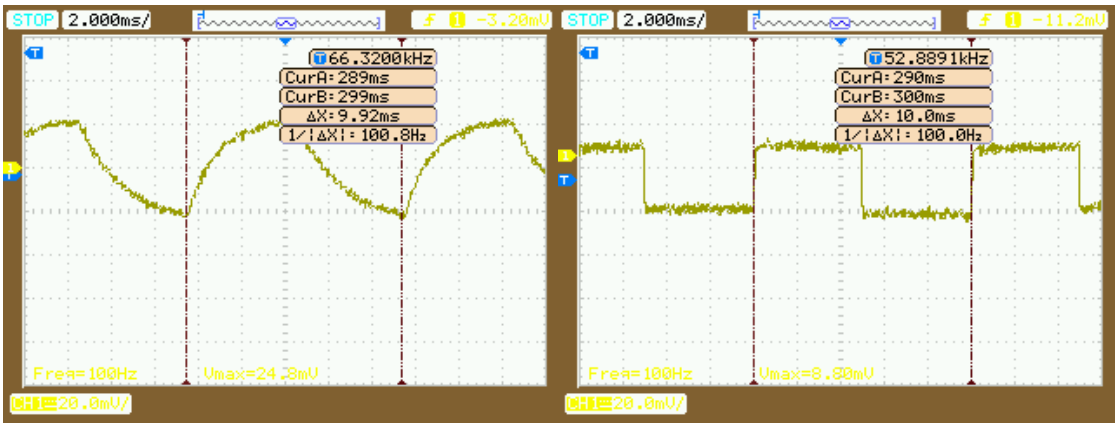

Figure 2.15: Waveforms of the output voltages of the voltage-doublers at 18 dBm transmitted power. On the left side is the version with 150 nF filter capacitors, while on the right is the one with 1 nF.

Figure 2.16: Experimental-setup.

Figure 2.17: Measuring setup of detector.

2.2 Custom Binary ADC

The output signal of the envelope detector has an amplitude of several millivolts and depends on the power of the RF signal. It is inevitable that an amplification has to be provided in order to better process the demodulated signal. The amplification stage must be implemented with as low complexity and power-consumption as possible. The first major issue is how much amplification must be applied in order to saturate the signal to the power supply's level. The amplitude of the signal varies according to the channel conditions and the distance between the OOK transmitter and the detector. The solution is to quantify the signal with a reference signal. The reference must be a proportion of the signal and not a fixed value because it has to adapt to channel's variations. Therefore, our approach uti-

lizes a dynamic voltage reference and based on that, quantifies the demodulated signal into two symbols: "1" or "0". In other words, it converts the demodulator's output into a digital signal, which can be fed into a digital processor unit. The transmitter sends pulses with 50% duty cycle at a frequency of 100 Hz and so the output signal of the demodulator is a periodical waveform. Fourier series analysis reveals that:

$$x(t) = \alpha_0 + \sum_{k=1}^{\infty} 2\,\mathrm{Re}(\alpha_k e^{jk\omega_0 t}), \tag{2.11}$$

where the $x(t)$ is the demodulated signal that goes into the digitizer, and the term $\alpha_0 = \frac{1}{\mathrm{T}} \int_0^T x(t)\,\mathrm{d}t$ describes the average dc value of the demodulated signal. This term is utilized as the *dynamic reference*.

2.2.1 Design

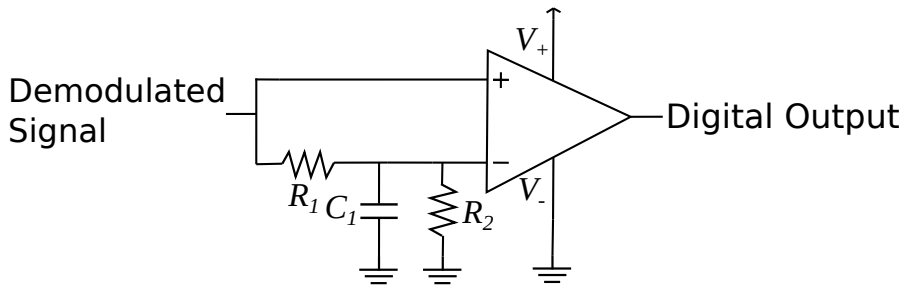

Figure 2.18: Schematic of the custom designed ADC amplifying stage [4].

A circuit is designed in order to apply the above-mentioned signal processing and produce the digital signal (Fig. 2.18). The RC network (R_1,C_1) forms a first order low-pass filter with a pole near to zero. Therefore, it allows only the average signal to be fed into the inverting input of the comparator. This circuit compares continuously the signal with its mean value and produces "1" when the signal is greater or equal than the mean, otherwise it produces a logic "0". The required time capacitor C_1 needs to reach the half voltage of the signal, can be calculated approximately as the time needed for 5 time constants, i.e., $5t_p$, where $t_p = R_1C_1$. This time specifies the minimum amount of preamble bits to be sent in order to ensure that C_1 has the appropriate voltage.

The role of the resistor R_2 is to provide a DC ground path to the inverting input in order to reduce the value of dc output voltage due to the input bias current (internally in the comparator) and not attenuate the signal [15]. It also forms a voltage divider with R_1. So, it is necessary to be orders of magnitude larger than R_1. In our case $R_2 = 10M\Omega$. The comparator introduces an upper limit in the sensitivity of the whole receiver system. Specifically, the differential input must be greater or equal with the input offset voltage of the comparator V_{OS}.

$$V_{diff} \geq V_{OS} <=> \frac{V_{signal}}{2} \geq V_{OS} <=> V_{signal} \geq 2 \cdot V_{OS}. \tag{2.12}$$

Therefore, the minimum detectable signal has a peak-to-peak amplitude of $2V_{OS}$. For example the TS881 comparator IC from ST Microrelectronics has an input offset voltage which varies from -6 to 6 mV. In the worst case scenario ($V_{OS} =$ 6mV) the $V_{signal}^{min} = 12$mV.

2.2.2 Simulation

The IC manufacturer offers all relevant simulation parameters that are entered into the LtSpice simulation software. The circuit is simulated for three different R_1C_1 time constants:

1. $R_1 = 150$kΩ, $C_1 = 220$nF (Fig. 2.19),
2. $R_1 = 300$kΩ, $C_1 = 220$nF (Fig. 2.20),
3. $R_1 = 300$kΩ, $C_1 = 470$nF (Fig. 2.21).

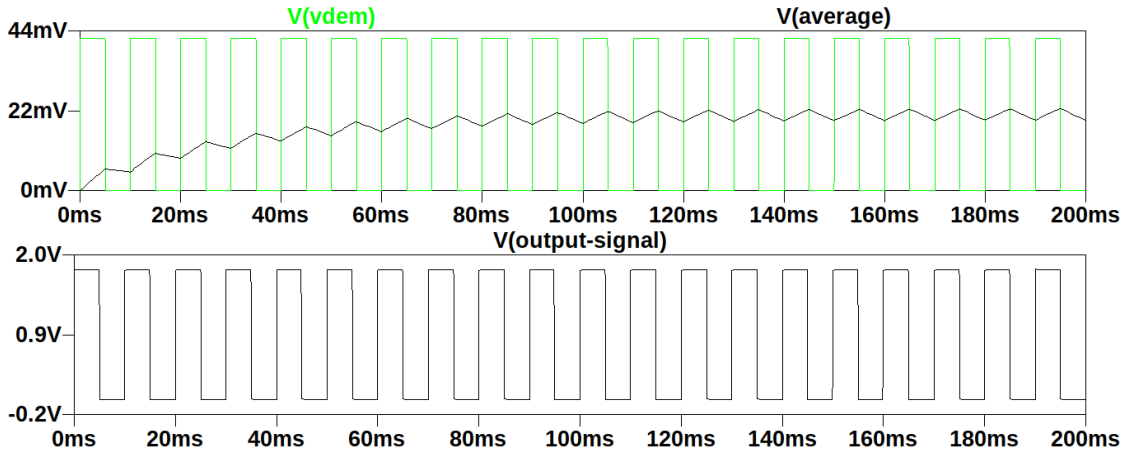

Figure 2.19: Simulation of the custom binary ADC. $R_1 = 150$ kΩ, $C_1 = 220$ nF. In the top picture, the input-signals of the comparator are shown (demodulated output from detector and its mean value). In the second picture, the produced demodulated digital signal from the output of the comparator is shown.

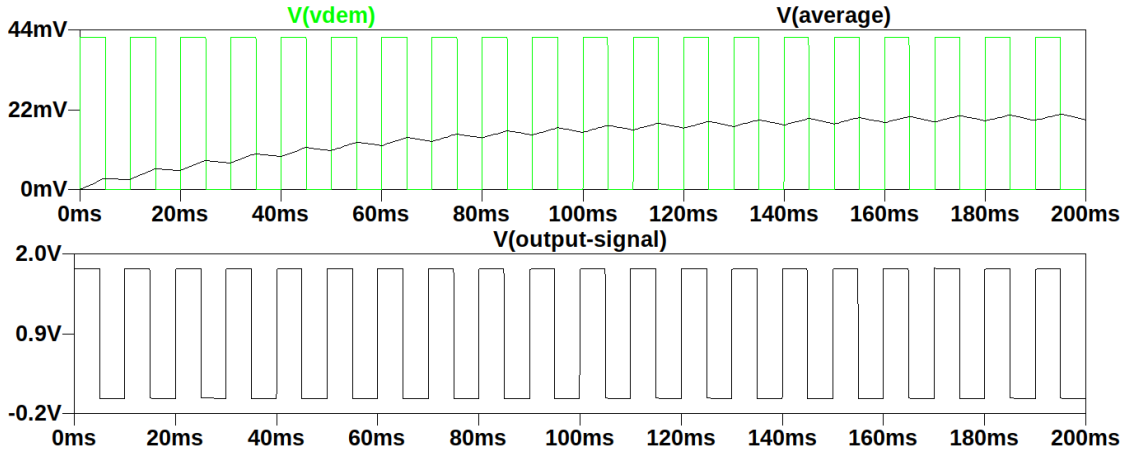

Figure 2.20: The respective simulation for $R_1 = 300$ kΩ, $C_1 = 220$ nF.

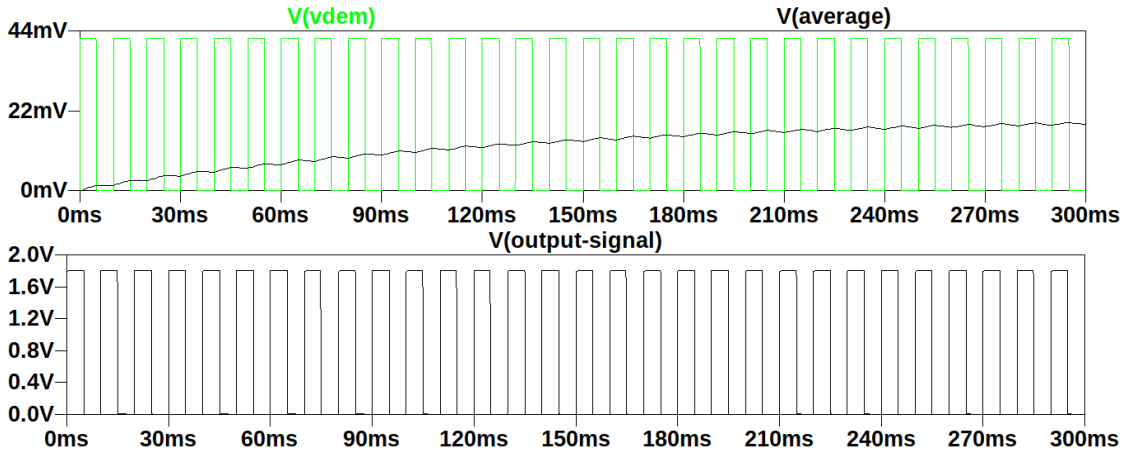

Figure 2.21: The respective simulation for $R_1 = 300$ kΩ, $C_1 = 470$ nF. In this case, it is clear that capacitor C_1 needs more time to reach the average value of the input signal.

2.2.3 Implementation

For the comparator, we choose the NCS220 IC from On Semiconductors because it offers low power consumption (10 μA), low price and has a low input-offset voltage ($V_{OS} = \pm 6$ mV) [16]. The circuit is implemented on a one-layer custom-designed PCB. The values of the passive components are the same as the first case of the simulation (i.e., $R_1 = 150\text{k}\Omega$, $C_1 = 220\text{nF}$).

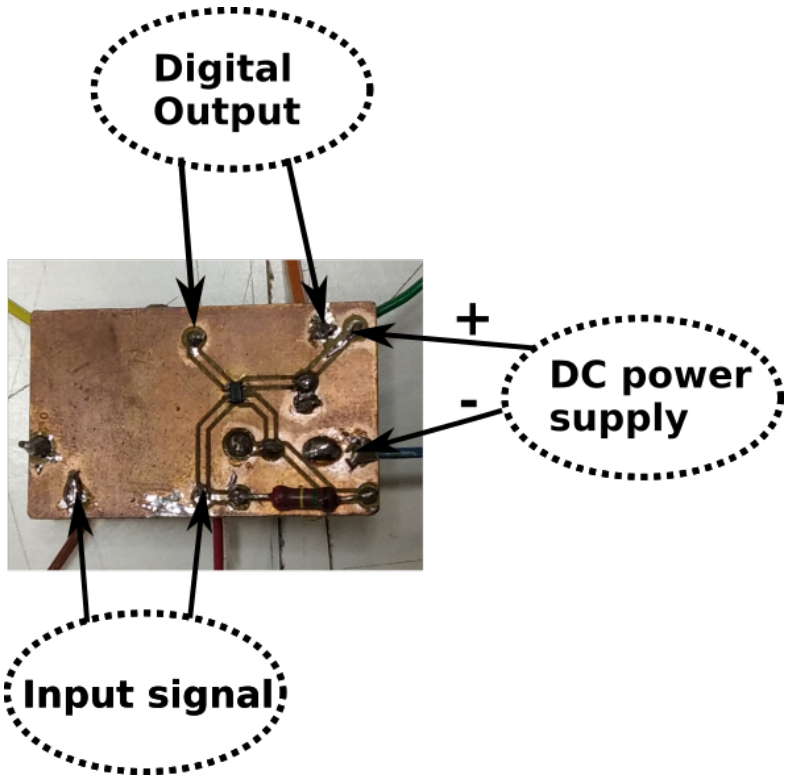

Figure 2.22: Receiver's comparator PCB.

2.2.4 Experimental results

The same setup as described in the subsection (2.1.5) is used. The only difference is that the envelope-detector (first version with $C_1 = C_2 = 150$ nF filter capacitors) is connected with the custom binary ADC circuit and the output of the digitizer is monitored through the oscilloscope. The amplifying stage (custom binary ADC) is being supplied with 1.8 V from a DC power supply (Fig. 2.23). The receiver system is detecting successfully the modulated signal for $P_{in} \geq 9.9$ dBm. Although the envelope detector (demodulator) is producing a non clear square waveform (Fig. 2.15), the output of the receiver is a clean square waveform (Fig. 2.24). This happens due to the second stage (custom binary ADC), which compares the input signal with its average value and thus the shape of the input signal waveform has no effect on the output. It is observed that for power levels of the RF-generator, which were near the minimum detectable power (9.9 dBm), the width of the demodulated pulses is getting smaller in comparison with the pulses, which are being produced by the signal generator (Fig. 2.24). This occurs, because at the demodulation stage a smaller part of the demodulated signal lies above the comparator's threshold (as we described in Eq. 2.12) which results in thinner (narrower width) pulses detected by the receiver.

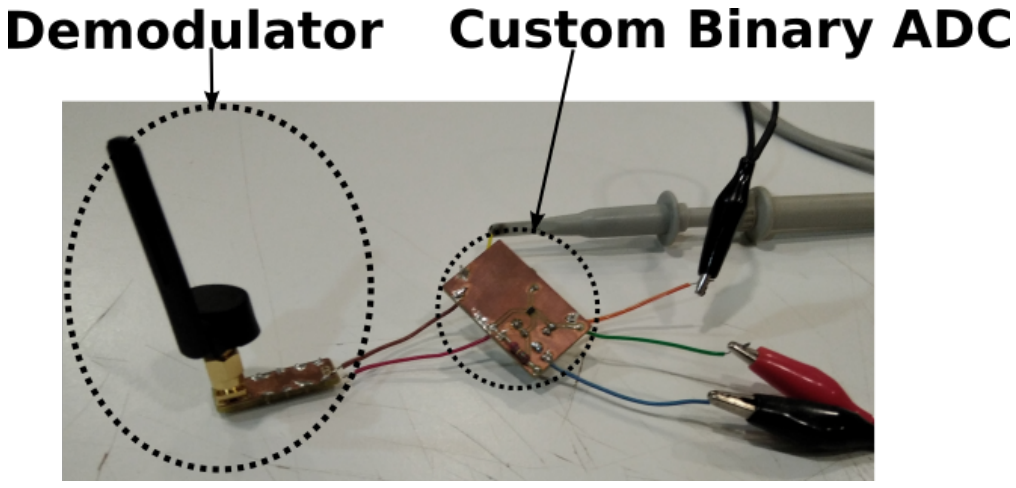

Figure 2.23: Topology of measuring setup of the receiver.

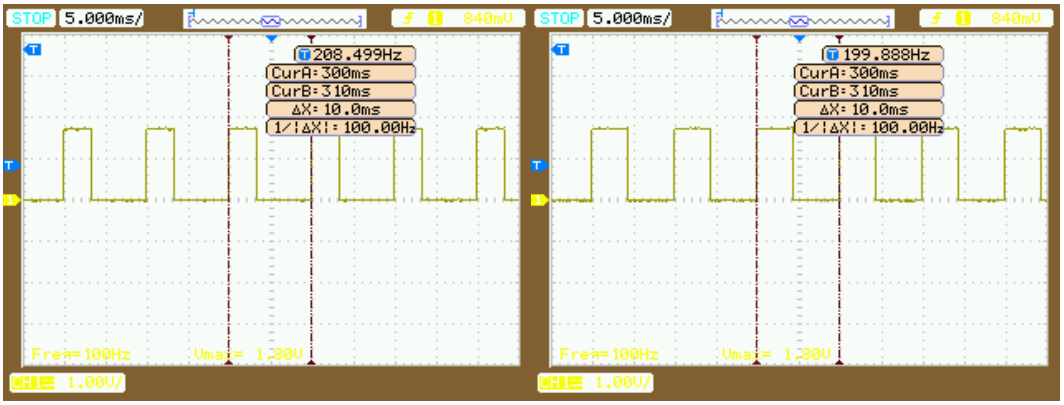

Figure 2.24: Waveform of the receiver's output. The left picture shows the output for $P_{out} = 9.9$ dBm while the right the respective output for $P_{out} = 12$ dBm.

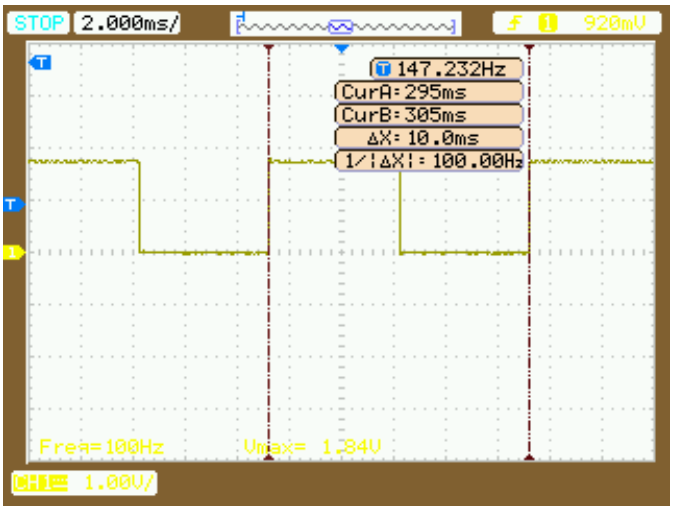

Figure 2.25: Waveform of the receiver's output for $P_{out} = 15$ dBm.

Chapter 3

Tag Uplink Backscatter Communication

3.1 Bistatic Scatter Radio

The bistatic topology consists of 3 major elements:

- a carrier emitter,
- one or multiple tags,
- a receiver.

For the communication with an embedded receiver using backscattering, a Binary Frequency Shift Keying modulation is implemented using just an RF-switch, which is connected to the antenna's terminals and controlled by a cheap 8-bit microcontroller. The carrier-emitter is illuminating the antenna with CW of frequency F_c. If an unmodulated carrier wave impinges an antenna, then the antenna reflects the induced signal [8]. Every termination load Z_i of the antenna is related to a reflection coefficient:

$$\Gamma_i = \frac{Z_i - Z_a^*}{Z_i + Z_a}, \tag{3.1}$$

where Z_a represents the impedance of the antenna [17] [13]. In this work, two antenna loads were utilized

- Z_0: Open circuit.
- Z_1: Short circuit.

When the switch is toggling between these two loads at a frequency of F_{sw}, then it modulates the carrier's signal with the switching signal. So, two subcarriers will

appear in the received frequency spectrum: one at frequency $F_c - F_{sw}$ and the other at frequency $F_c + F_{sw}$. Setting the switch to have two switching frequencies $F_{sw,0}$ and $F_{sw,1}$, two sets of subcarriers will occur in the spectrum [17, 18].

$$F_{sc,0} = F_c \pm F_{sw,0}, \tag{3.2}$$

$$F_{sc,1} = F_c \pm F_{sw,1}. \tag{3.3}$$

In this work, only the upper subcarrier from each set is used for reception by an embedded radio.

$$F_{sc,0}^{upper} = F_c + F_{sw,0}, \tag{3.4}$$

$$F_{sc,1}^{upper} = F_c + F_{sw,1}. \tag{3.5}$$

The $F_{sc,0}^{upper}$ represents bit "0" and $F_{sc,1}^{upper}$ bit "1" respectively. The time each subcarrier is present in the air constitutes the bit duration T_{bit}. So, the bit rate equals $R = \frac{1}{T_{bit}}$ [17].

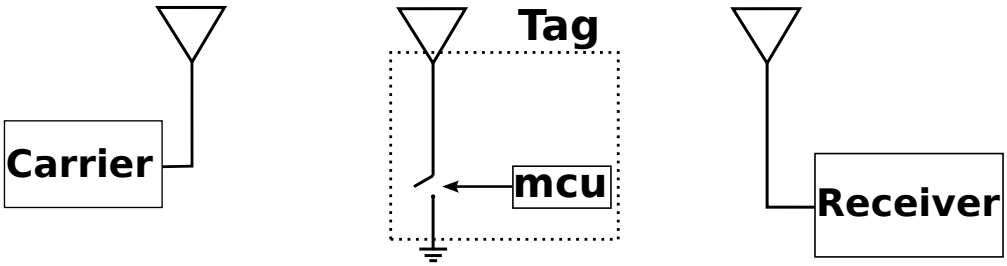

Figure 3.1: Bistatic topology.

3.2 Tag - First implementation

The tag consists of a Silabs C8051F930-DK (MCU on development kit), which controls an ADG919 RF switch from Analog Devices [19] and an antenna at 2.4 GHz (fig. 3.4).

In order to create the two switching frequencies, a special mode of the timer PCA0 is used, which is called "Frequency Output Mode" [20]. In this mode, the MCU creates a square waveform with fixed 50% duty cycle in port P0.0 with

frequency which is dependent on the reload value of the 8-bit PCA0 timer. The switching frequency can be calculated by this formula:

$$F_{sw,i} = \frac{F_{CPU}}{2PCA0CPH_i}, \tag{3.6}$$

where PCA0CPH is the register which holds the reload value [20]. Here, the used switching frequencies are $f_{sw,0} = 97.66$ kHz and $f_{sw,1} = 130.2$ kHz (fig. 3.2). The two switching frequencies are implemented by altering the register's PCA0CPH data by two distinct bytes.

The 16-bit timer0 is set to overflow every $T_{bit} \approx 0.41667$ ms ($R = 2400$ bps). This time event is mandatory for the bit duration. A custom function is written, which takes as argument the byte that has to be send. At first, it checks the MSB and creates the appropriate switching frequency and at the same time enables the timer0. Then, it holds this "on-off" burst until timer0 has overflowed. Next, a logical left shift takes place and checks the next MSB. This procedure is followed 8 times in order to transmit the byte.

Then, the packet which has to be transmitted is separated into bytes and for each byte the above-mentioned function is being called, starting from the most significant byte and going to the last significant. In the end, the port P0.0 is being driven to gnd (0 V) to save power.

The C8051F930 MCU has various clock sources. The "Internal Low Power Oscillator" is being used only for the initialization and calculation processes of the algorithm. This is a low power clock but with low frequency stability. For the packet transmitting procedure, where high frequency stability is mandatory, two different clock sources are tested [20].

1. Internal Precision Oscillator 24.5 MHz.

2. External Crystal Oscillator 25 MHz.

The second choice is offering us much better performance in PER because the crystal oscillator has much more stability than the respective internal. The decision was to use the crystal oscillator at the expense of somewhat higher static power consumption due to the larger bias current required (from 0.3mA to 2.6 mA). This increase exists only in the transmitting time section. The clock frequency

was divided by 8 providing the MCU with a system clock of 3.125 MHz, reducing significantly the dynamic power consumption.

The packet consists of 3 sections:

- Preamble,
- synchronization word, and
- payload.

The preamble is a sequence of alternating bits. Specifically, it is 40 bits with sequence "10". The receiver's timing, frame detection algorithms and control loops are tailored to this preamble [5].

The synchronization word serves as a delimiter in frame after which the demodulated bits will be stored in receiver's queue. It also implements packet filtering. The sync word is the hex value "2DD4" [5].

The useful bytes that carry the information are represented by the payload. In this implementation, the payload is composed of 5 bytes (fig. 3.3). The packet consists of total 96 bytes. Therefore, the transmission time equals with 40 ms (Fig. 3.5). The time delay between the packets equals 252 ms and is created from (16-bit) timer1.

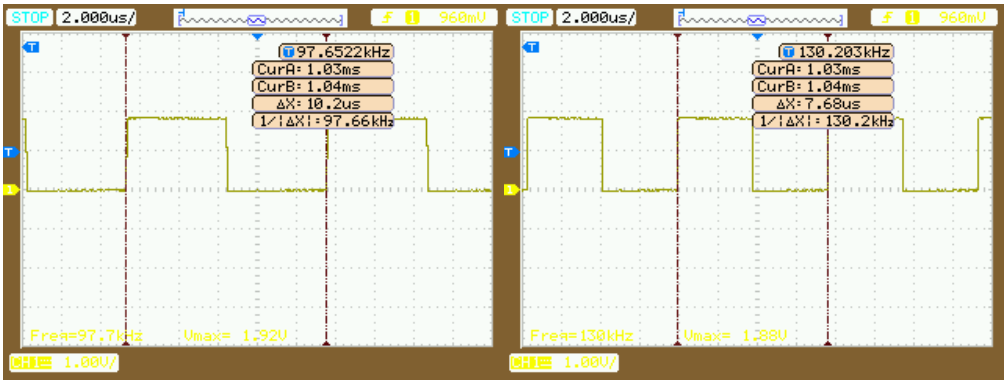

Figure 3.2: Measurement of the switching frequencies on the oscilloscope. Left is $f_{sw,0}$ while right $f_{sw,1}$.

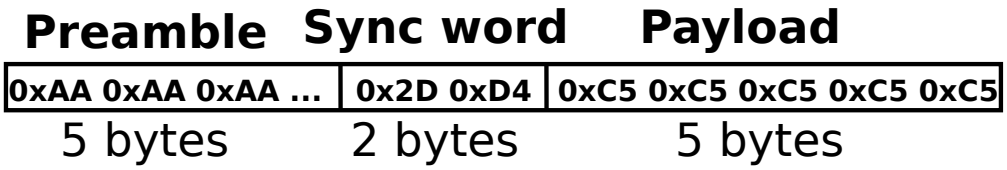

Figure 3.3: Packet format.

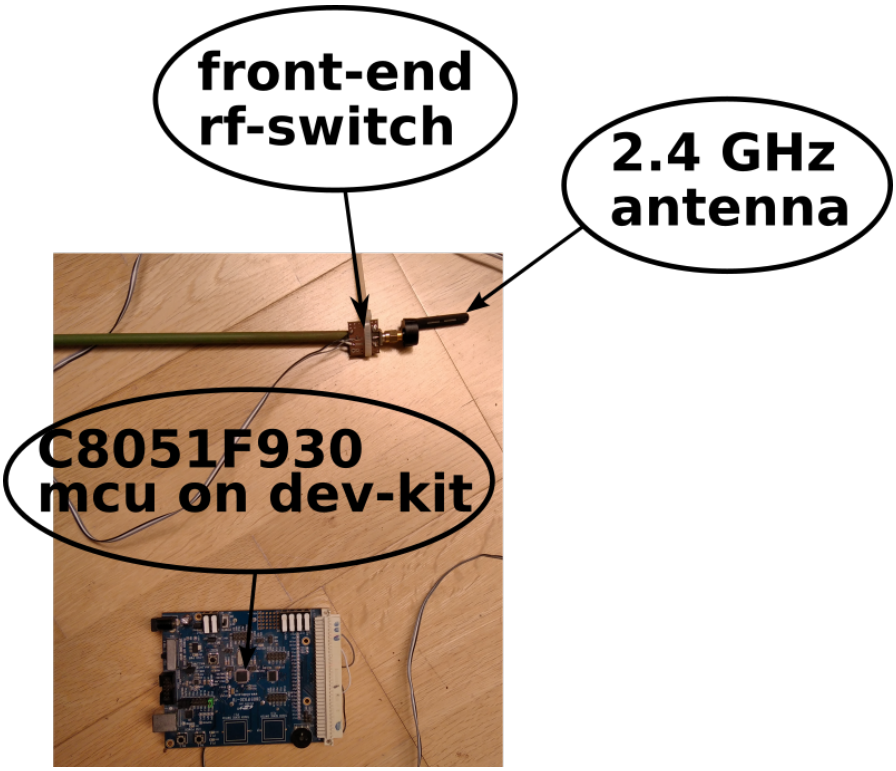

Figure 3.4: First implementation of the tag.

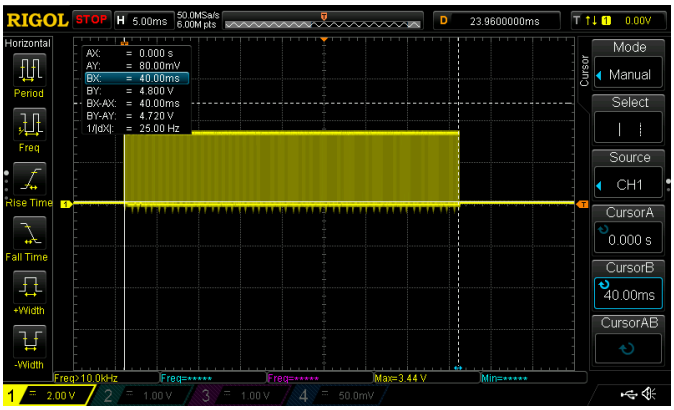

Figure 3.5: Capture of tag's packet in the oscilloscope.

3.3 Embedded Receiver

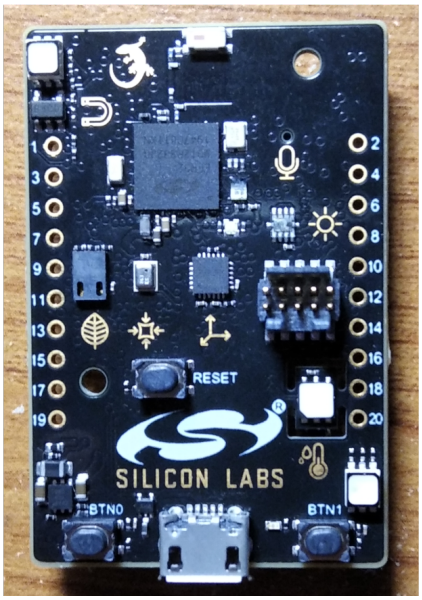

Figure 3.6: Silabs Thunderboard Sense2 [5].

For the embedded receiver we choose the Silabs Thunderboard Sense2 board, which integrates the EFR32MG12 SoC. It offers multi-protocol capabilities in the 2.4GHz band with relative low power consumption at an affordable price. Silicon Labs is providing us with the "RAIL" tool of the "Flex" library for configuring the radio in boards which belong to the EFR32M family.

The bit-rate of the link was $R = 2.4$ kbps. We assume that the deviation has to be $Dev = 4.5 \cdot R = 10.8$ kHz. The antenna of the board showed the best receiving behavior at 2450 MHz. Therefore, this frequency is defining the center frequency of the receiver. Afterwards, the ranges of the link are being monitored using different channel-bandwidth filters. After many tests we observed that the longest ranges are achieved for a channel bandwidth BW = 60 kHz. The filter has to be narrow for the reason we described in the subsection (2.1.1). The final configuration of the receiver is listed in Table 3.1.

$F_{receiver}$ (MHz)	2450
Dev (kHz)	10.8
R (kbps)	2.4
Channel-BW (kHz)	60
Target-input AGC (dBm)	−8

Table 3.1: Receiver's radio configuration.

3.3.1 Subcarriers selection

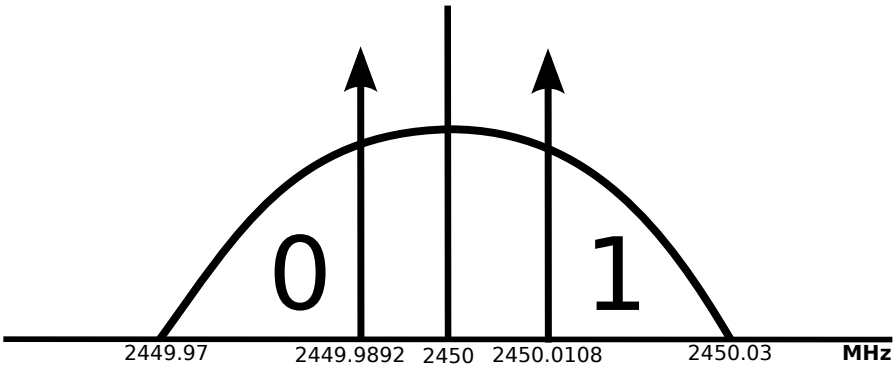

Figure 3.7: Subcarriers in frequency-spectrum.

After many trials we observed that the frequency difference $|F_{receiver} - F_c| = 110$ kHz constitutes the sweet spot for the largest ranges. Any difference larger than this would result in the same ranges but with larger power-consumption because the switching frequencies must be higher in order to produce the same subcarriers. Therefore, the carrier was set to $F_c = 2449.89$ MHz. Any frequency $< F_{receiver} -$ Dev would result in bit "0" and respectively $> F_{receicer} +$ Dev in bit "1", with the necessary condition that these frequencies are inside the receiver's bandwidth (fig. 3.7).

$$F_{rec} - \frac{BW}{2} \leq Sub_0 \leq F_{rec} - Dev <=> 2449.97 \leq Sub_0 \leq 2449.9892. \quad (3.7)$$

Respectively for Sub_1:

$$F_{rec} + Dev \leq Sub_1 \leq F_{rec} + \frac{BW}{2} <=> 2450.0108 \leq Sub_1 \leq 2450.03, \quad (3.8)$$

where Sub_0 and Sub_1 represent the subcarrier frequencies for bit "0" and "1", respectively. The switching frequencies are extracted by subtracting from (3.7 & 3.8) the F_c.

$$80 \leq f_{sw0} \leq 99.2\text{kHz}, \tag{3.9}$$

$$120.8 \leq f_{sw1} \leq 140\text{kHz}. \tag{3.10}$$

So, the switching frequencies $f_{sw,0} = 97.66$ kHz and $f_{sw,1} = 130.2$ kHz are valid according to (3.9 & 3.10). For optimal reception by the embedded receiver the frequencies of the subcarriers have to follow this equation:

$$|Sub_1 - Sub_0| = k \cdot \frac{1}{T_{bit}}, \tag{3.11}$$

where $k \in \mathbb{N}$. Because $|Sub_1 - Sub_0| = |f_{sw,1} - f_{sw,0}|$ Eq.(3.11) can be converted into the following equation

$$|f_{sw,1} - f_{sw,0}| = k \cdot \frac{1}{T_{bit}}. \tag{3.12}$$

Unfortunately, the specific MCU could not create switching frequencies which are according to the Eq.(3.12) due to the low precision of its clock divider. Therefore, we experimented with different sets of switching frequencies which can be produced by the MCU in order to achieve the longest ranges between the tag and the embedded receiver.

3.4 Experimental results

For the experimental setup, the tag is placed outdoors between the carrier emitter and the embedded receiver. The distance between the carrier-emitter and the tag is defined by the symbol d_{ct} and the distance between the tag and the embedded receiver respectively by d_{tr} (Fig. 3.8). In order to implement the carrier-emitter, a Thunderboard Sense2 is configured as the umodulated carrier transmitter at $2449,89$ MHz with 10.4 dBm power. We concluded that for $f_{sw,0} = 100$ kHz, $f_{sw,1} = 130.2$ kHz the largest range is obtained from testing different switching frequency pairs, so these frequencies were used in the remainder of the experiment.

For the range test, the receiver is configured to blink a LED every time a packet has arrived. Also, the payload of the packet is sent through the serial port in order to check for possible errors of the received packets. In order to calculate the Packet Error Rate (PER), the tag is configured to send 100 packets with a sequence number inside their payload.

From the measurements in Table 3.2, we can observe that the shortest d_{tr} distances occurred when the target input AGC is the lowest for the same d_{ct} distance. Low target-input AGC means that the AGC module expects a small signal and thus defines a high gain to amplify it. When the target-input AGC is defined to be low and signals with larger RF-power than the expected are impinging the antenna, then the AGC will amplify these signals in such a way they will be above of the dynamic region of the internal ADC and thus they will be not detected by the receiver. For this reason the above-mentioned phenomenon occurred.

d_{ct}(m)	d_{tr}(m)	$target - inputAGC(dBm)$
2.5	6	-8
2.25	41.5	-8
3.5	4.75	-8
1	60	-8
2	31	-8
3	5	-8
4	4.5	-8
5	2.5	-8
5	4.8	0
5	5	8
1	41.5	-15

Table 3.2: Tag's range test.

d_{ct}(m)	d_{tr}(m)	**PER**(%)
1	6	0
2	4.5	0
2	6	0
3	4.3	3.7

Table 3.3: PER measurement.

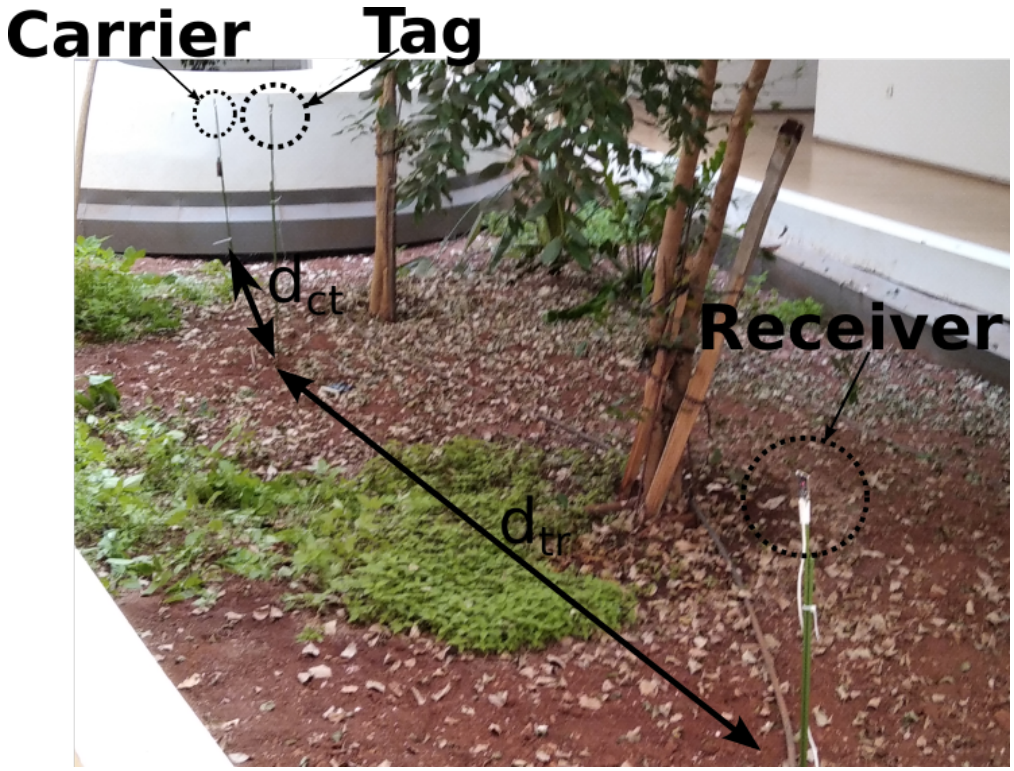

Figure 3.8: Experimental setup of bistatic backscatter radio. The antennas are placed at height of 1.20 m from the ground.

Chapter 4

Solar Harvester

Solar energy is a great opportunity to power an ambiently powered backscatter link. The concept of ambiently powered node has already been explored [8]. The most power consuming part of the link are the embedded radios. Therefore, designing an energy harvesting system for the embedded radio boards is a challenging but necessary task.

4.1 Design and Implementation

The Sense 2 board is supplied by a DC power-supply at 3 V in order to measure the current consumption. In idle and receive states the board is consuming 13 mA, while in sleep mode $I_{sl} = 8\ \mu$A [6]. In the transmit mode peaks of 57 mA are observed [6]. Thus, the average current consumption is given by

$$I_{average} = I_{active} \cdot D + I_{sl} \cdot (1 - D), \tag{4.1}$$

where D represents the duty cycle of board's operation and I_{active} is the current which is drawn from the board during active operation.

The solar harvester consists of (Fig. 4.4)

- a solar cell,
- a custom power management circuit,
- a storage element.

The characteristic curve of the solar cells is not constant and varies according to the environmental conditions (temperature, solar radiation)(Fig. 4.1). The maximum power point (MPP) is in the knee of the curve (I_{mp},V_{mp}). Thus, this

V_{mp}(V)	I_{mp}(mA)	V_{oc}(V)	I_{oc}(mA)
1.92	80	2.2	75

Table 4.1: Characteristics of the used solar-cell under full solar irradiance.

point is not constant. The used solar cell has a circular area of 26.42 cm^2. The maximum power that can be extracted from this cell is

$$P_{max} = V_{mp} \cdot I_{mp} = 153.6 \ mW. \tag{4.2}$$

For the storage element we choose NiMh battery cells because they are cheap and can store much more energy than supercapacitors. Each cell has a voltage of 1.2 V and capacity $C_{bat} = 100$ mAh. The board has an operating voltage from 2 V to 3.3 V [5]. Therefore, two cells in series with combined voltage of 2.4 V are enough to power the board. The maximum energy that can be stored is

$$E = V \cdot C_{bat} = 240 \ mWh = 864 \ J. \tag{4.3}$$

The power-management circuit has to provide a voltage > 2.4 V in order to charge the batteries and parallelly provide the appropriate voltage for the board. We set a margin of 0.4 V above the storage element's maximum voltage. So, the circuit must have 2.8 V at the output. Also, the circuit has to match the resistance of the cell at the MPP with the resistance of the batteries. The design of the power-management circuit is based on the BQ25504 IC from TI [21]. In order to extract the maximum power from the solar-cell we have to set the operating region of the IC in the MPP at full sunrise. In this region the IC will implement MPPT. For this reason a resistor divider was necessary with the following ratio:

$$\frac{R_{oc2}}{R_{oc1} + R_{oc2}} = \frac{V_{mp}}{V_{oc}}, \tag{4.4}$$

where V_{mp} is the voltage at the MPP during full sunrise, V_{oc} is the open-circuit voltage and

$$R_{oc1} + R_{oc2} = 20 \ M\Omega, \tag{4.5}$$

according to the IC datasheet [21]. From (4.4) and (4.5) the resistors must be

$R_{oc1} = 2.55$ MΩ and $R_{oc2} = 18$ MΩ

A couple of resistors R_{ov1}, R_{ov2} is defining the regulated output voltage of the circuit:

$$R_{ov1} + R_{ov2} = 10\ M\Omega, \tag{4.6}$$

$$\frac{R_{ov1}}{R_{ov2}} = \frac{2V_{BATov}}{3V_{BIAS}} - 1, \tag{4.7}$$

where $V_{BATov} = 2.8$ V and $V_{BIAS} = 1.25$ V [21]. From (4.6) and (4.7), it can be calculated that $R_{ov1} = 3.3$ MΩ and $R_{ov2} = 6.65$ MΩ. Furthermore, the IC was configured to have thermal shutdown at 60^oC in order to protect the batteries from high temperature. Also, the power management circuit features an efficiency of 91% with this setup configuration [21].

A 2-layer custom designed PCB is fabricated in order to implement the circuit (Fig. 4.3).

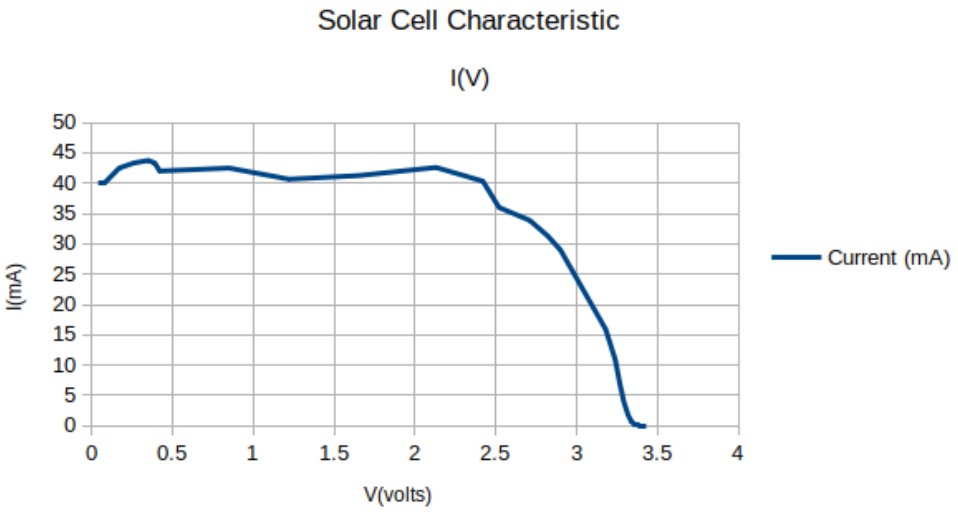

Figure 4.1: I(V) characteristic of a solar cell with $V_{OC} = 3.43$ V found in the laboratory's equipment, under full sunrise from experimental data.

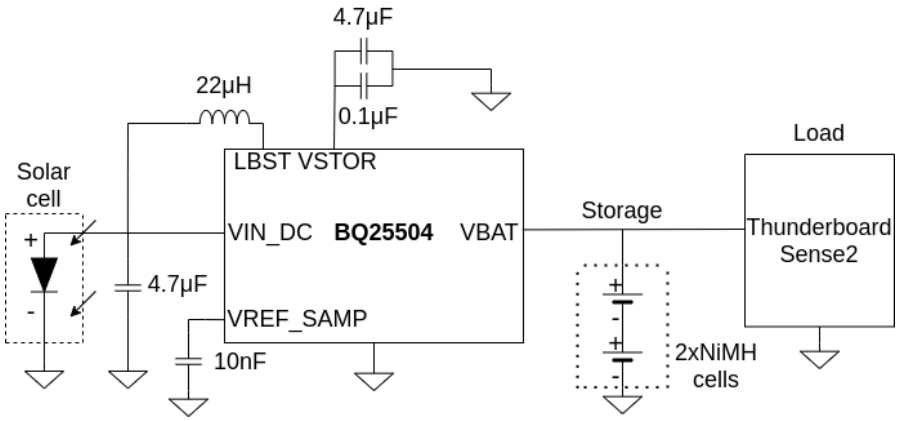

Figure 4.2: Schematic of the harvester [6].(more details on Chapter Appendix 7.1.6)

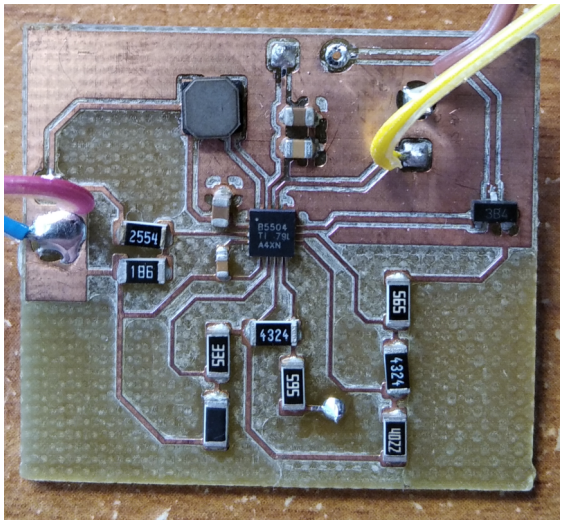

Figure 4.3: Custom designed PCB for the implementation of the harvester's power-management circuit [6].

4.2 Experimental results

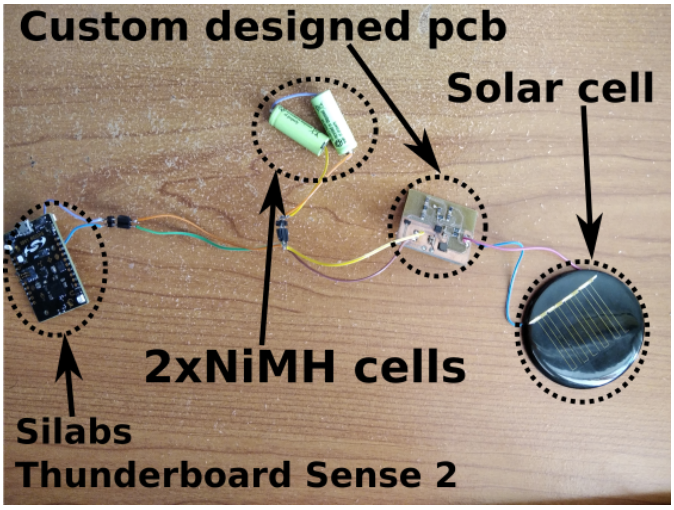

Figure 4.4: Solar harvester system [6].

With the help of a pyranometer we observed that the harvester operates properly when solar radiation ≥ 368 W/m^2. The output voltage is measured at 2.79 V. It took 4 hours for a partially depleted pair of batteries (at 1.37 V initial voltage) to fully charge to 2.4 V with no load attached. This is equivalent to have a zero duty cycle ($D = 0$). [6].

If the receiver has a duty cycle of 50% then, based on (Eq. 4.1) $I_{average} = 6.504$ mA. Based on the above and the fact that the capacity of the batteries is known, it can be calculated that the receiver can operate 15.38 hours without the need of the sun! This is valid only when the batteries are initially fully charged.

In the cold-start mode (batteries are partially depleted) we assume the leakage current due to sleep mode to be negligible. So, for a time duration (1−D) the harvester will charge its batteries and for the remaining time, D, the batteries will provide the board with energy. If we account for the duty cycle during normal operation, then the charging time can be estimated according to [6]:

$$t_{ch} = 4 \cdot \frac{1}{1 - D}. \tag{4.8}$$

Now, the charging percentage of the battery can be also estimated from [6]:

$$\theta_{ch} = \frac{actual\ charging\ hours}{t_{ch}}. \tag{4.9}$$

We assume that the available capacity of the batteries is [6]:

$$C_{av} = C \cdot \theta_{ch}. \tag{4.10}$$

.

For the specific day scenario (Fig. 4.5), there are 11 available hours when the harvester can operate properly. The harvester-system begins its operation in 9:00 am. Having the embedded receiver at a duty cycle of $D = 50\%$ we can estimate from (4.8) that $t_{ch} = 8$ h. From (4.9) $\theta_{ch} = 1$. Therefore, until 19:00 the batteries will remain fully charged. Please note that the actual hours of operation are the hours when the solar radiation is proper to power the system plus the hours when the board is powered only by the batteries [6]. So, $T_{sun} = 11$ h and $T_{bat} = 15.38$ h from the initial analysis. The total hours of receiver's operation are

$$T_{total} = T_{sun} + T_{bat}, \tag{4.11}$$

and in this case equals to 26.38 hours.

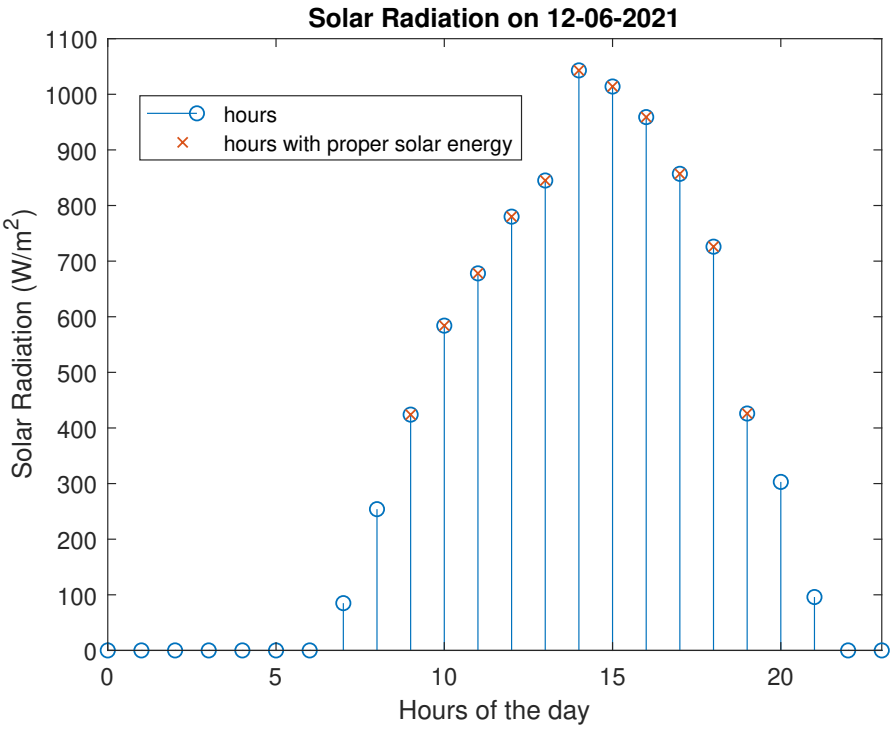

Figure 4.5: Solar radiation in the university campus at the day 12-06-2021 [6].

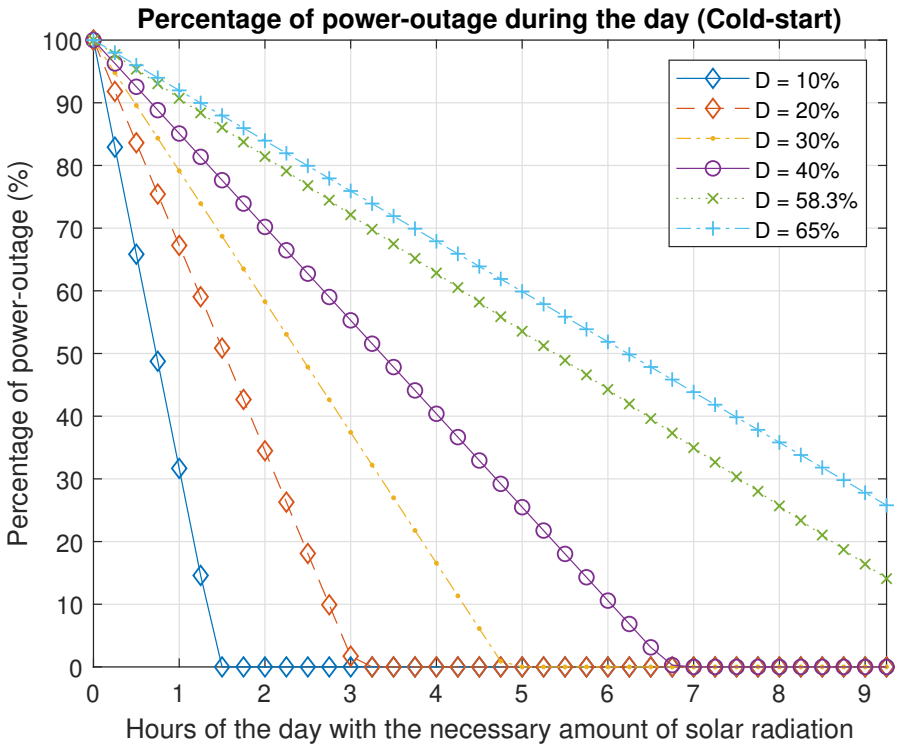

Figure 4.6: Probability of power outage of WSN-node, which runs consensus algorithm, as function of numbers of hours, during which the solar radiation is proper in order to power the harvester [6].

Chapter 5

Application: Humidity Sensing

The humidity sensor is a passive device, which varies its electrical permittivity ϵ_r according to the humidity. In other words, its capacitance becomes proportional to the measured humidity and can thus be modeled as a variable capacitor [22].

5.1 Sensor Interface

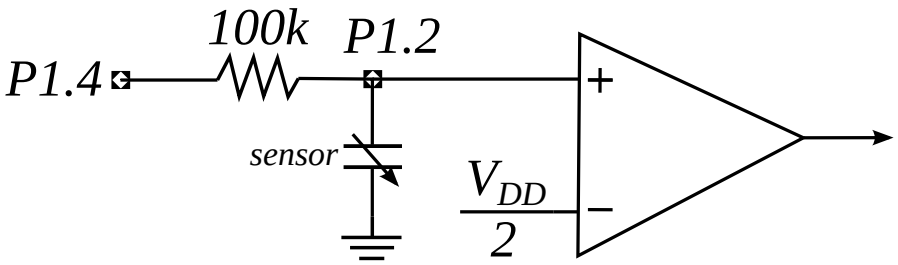

Figure 5.1: Humidity sensor interface with the tag.

The capacitance of the sensor has to be converted in such a form that it can be read from a MCU. For this reason, a RC network is implemented where the sensor constitutes the capacitor of the network (fig. 5.1). The voltage of the capacitor during charging equals:

$$V_c(t) = V_s(1 - e^{-\frac{t}{RC}}). \tag{5.1}$$

Considering that the targeted voltage of $V_c(t)$ is $\frac{V_{DD}}{2}$, the required time that capacitor needs in order to be charged at this voltage can be calculated from (5.1) and is equal to:

$$t_{\frac{1}{2}} = \ln(2) \cdot RC. \tag{5.2}$$

. With this setup the capacitance of the sensor is being converted into a time delay and can be read from the MCU. Larger capacitance simply corresponds to

a larger time delay.

At the start of the measurement procedure, port P1.4 is going high and starts to charge the capacitor. P1.2 is connected to the non-inverting input of the internal comparator Comp0. The inverting input is connected to a $\frac{V_{DD}}{2}$ internal voltage-reference in order to reduce the power consumption and the use of external components. When the capacitor reaches half of the supply, then the comparator fires an internal interrupt.

5.2 Tag Final Implementation

5.2.1 Operating Cycle

At first, the tag operating with the low power 2.5 MHz clock, enables the internal comparator (Comp0). Then, the MCU pulls the P1.4 high for charging the RC network and starts the 16-bit timer2. When the interrupt occurs, the timer is stopped and the port P1.4 is pulled to GND in order to discharge the capacitor. After, the MCU stores the timer's value, resets the timer and waits for 0.16 ms $> t_{\frac{1}{2}}$ in order to fully discharge the capacitor. This time event is produced also from timer2. This constitutes the measuring procedure but we cannot rely on only one measurement. Therefore, the above-mentioned procedure is followed 16 times and all the data (saved value of timer2) are summed in one 16-bit variable. Then 4 logical right shifts happen in this variable. In this way, the tag extracts the average value of 16 humidity measurements without using division. This is critical because the division is computational achy operation for an 8-bit MCU. This 16-bit variable is stored in the two least-significant-bytes of the payload. At this stage the creation of one packet has finished.

In the next stage the tag enables the crystal oscillator and changes its clock to the 3.125 MHz clock. Then it transmits the packet through backscattering, as we described in (Chapter 3). In order to return to the default 2.5 MHz clock, a two-step procedure must be followed, otherwise the MCU will stall. At the first step, the MCU changes its clock into the 10 MHz clock (faster clock) produced by the low-power oscillator and waits for clock-synchronization to take place. In the second step, it changes the prescaling factor into clk / 8 and returns into the

default clock. This way the tag sends 10 measurement packets.

After this, the MCU disables the comparator in order to save power, saves the interrupt-states and disables all the interrupts. Then the running clock settings are saved and the MCU clock is changed into the 10 MHz clock (low power oscillator). In the end, port P1.0 is configured as wake-up source and after this the MCU operates in sleep mode.

It should be noted that the main role of timer2 is to sample the charging time with sampling frequency equal with $f_{clk} = 2.5$ MHz (until capacitor reaches $\frac{V_{DD}}{2}$). For example, when a packet contains the value 0x85. This value is the mean value of the timer ticks. So, the requested time can be extracted as

$$t_{\frac{1}{2}} = ticks \cdot T_{clk}. \tag{5.3}$$

From (5.3) $t_{\frac{1}{2}} = 133 \cdot 4 \cdot 10^{-7} = 53.2$ μs. Also, the capacitance of the sensor during this measurement can be calculated from (5.2) as $C = 767.5$ pF.

5.2.2 Power Consumption

The MCU has a dynamic current consumption of 226 μA/MHz [20]. For the static consumption in sleep mode, the current consumption is 0.05 μA, the comparator consumes 23 μA [20] and the RF-switch has a consumption under 1 μA [19]. The bias current for the crystal oscillator is 2.6 mA [20]. The dynamic current consumption for the worst case scenario, where the MCU is operating with 3.125 MHz clock, is equal to

$$I_{dynamic} = 226 \cdot 3.125 = 706.25 \ \mu A. \tag{5.4}$$

The maximum active current consumption is

$$I_{active} = I_{dynamic} + I_{Comp0} + I_{osc} + I_{switch} = 3.33 \ mA. \tag{5.5}$$

For the sleep mode the maximum current is

$$I_{sleep} = I_{sl} + I_{switch} = 1.05 \ \mu A. \tag{5.6}$$

A two-layer custom PCB was designed and fabricated for the final implementation of the tag (Fig. 5.2).

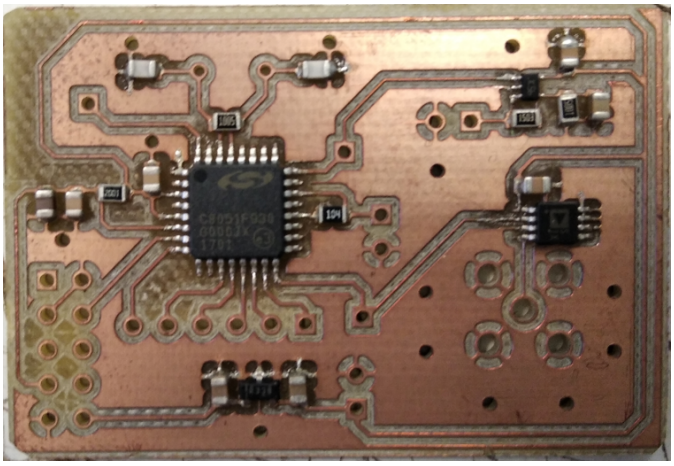

Figure 5.2: Implementation of the tag on custom designed pcb.

5.3 Experimental Results

5.3.1 Sensor data

For the experimental setup we used a breadboard to implement the connections for the RC-network and the push-button (fig. 5.3). The button is connected in series between the P1.0 and the GND with a 10 μF filter capacitor in parallel. The role of the switch is to simulate the low transitions of the tag's receiver (Chapter 2). Every press of this button equals a low transition in port P1.0 and this transition is the wake-up event for the MCU. When the MCU wakes up, it sends 10 measurements to the embedded receiver and goes again into sleep mode. The experiment is conducted under 3 conditions:

- sensor is in the open air (Fig. 5.4),
- sensor is 50% submerged in water (Fig. 5.5),
- sensor is 100% submerged in water (Fig. 5.6).

It is observed that when the comparator is enabled for the first time, then the first measurement is slightly off than the others. There is the trade-off of having a relative error in the first measurement but saving 23 μA of current consumption.

5.3.2 Power Consumption

The setup is operating at 1.8 V supply voltage and is powered from an on board boost-converter. The converter is supplied by a 1.5 V battery cell. In this experiment, the current which flows from the battery is measured during the operation with the humidity sensor on board. The active mode lasts for 4.5 seconds and in this time the average current consumption is $I_{active} = 2$ mA with peaks of 2.45 mA. In sleep mode, on the other hand, the current consumption is just 65 nA!

For a sleep time of 1 minute, the duty cycle $D = \frac{4.5}{60} = 7.5\%$. It can be calculated from Eq. (4.1) that $I_{average} = 0.15 + 6 \cdot 10^{-8} \approx 0.15$ mA. The average power consumption is $P = V \cdot I_{average} = 0.27$ mW. Lower power consumption can be achieved utilizing smaller duty cycles.

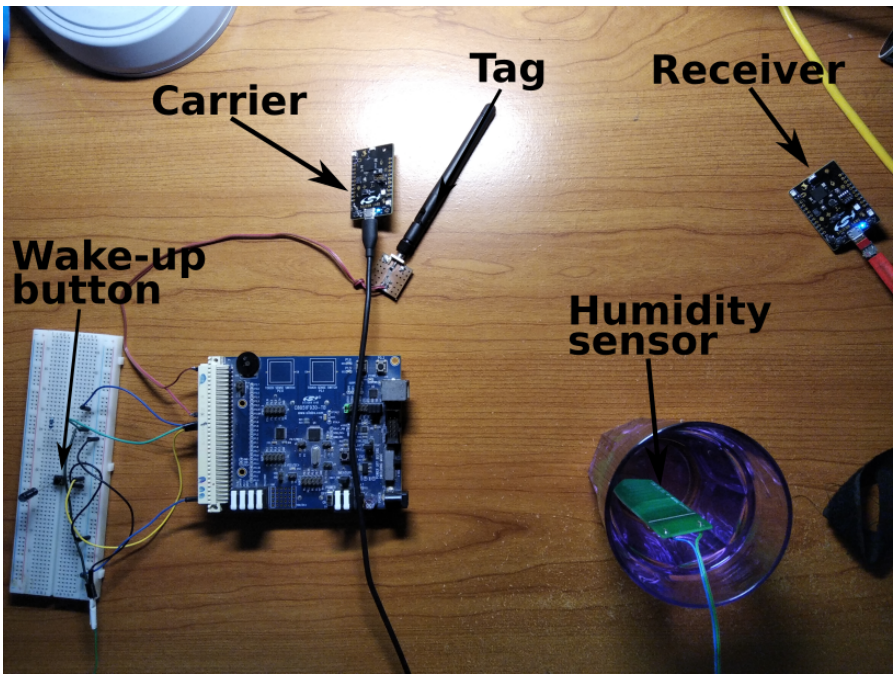

Figure 5.3: Experimental setup for backscattering humidity-sensor's data.

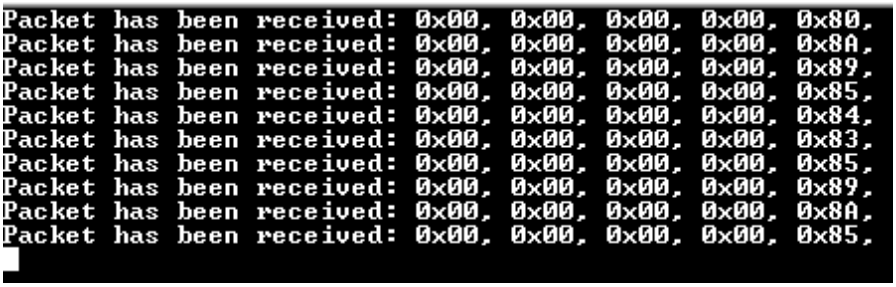

Figure 5.4: Packets are carrying the humidity data when the sensor is in the air.

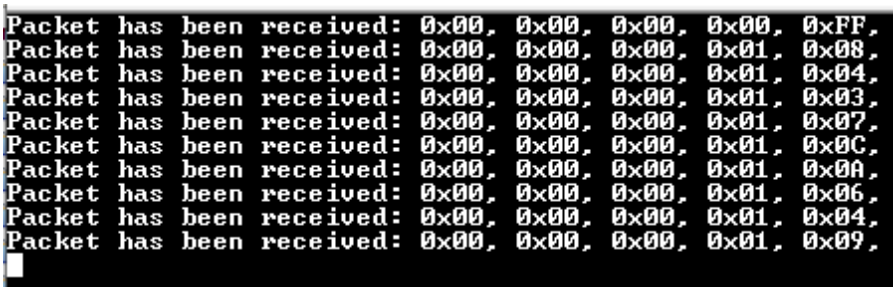

Figure 5.5: Packets are carrying the humidity data when half of the sensor element is inside the water.

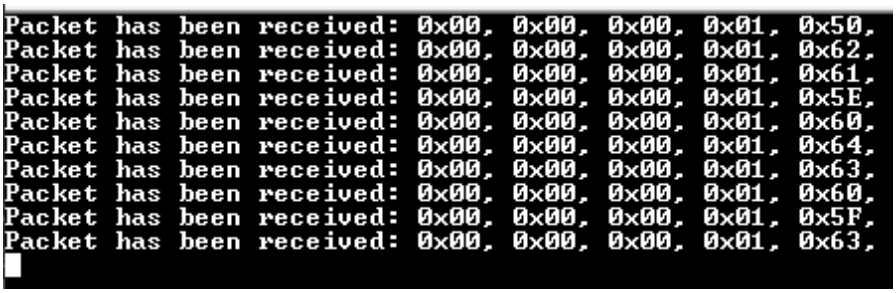

Figure 5.6: Packets are carrying the humidity data when the whole sensor element is inside the water.

Chapter 6

Conclusion

Bidirectional tags can achieve much lower power-consumption than the conventional RFID tags because they can operate with a non-deterministic duty cycle and can wake-up whenever necessary. This work proves that not only energy autonomous tags are feasible, but more importantly, that the entire communication link, i.e. tag and embedded radio, can be achieved using ambient solar energy. It was shown that this kind of radio deployment shows great promise in precision agriculture applications and a proof-of-concept prototype was designed that can very easily interface with soil moisture sensors.

In previous implementation without OOK that rely on Frequency Domain Multiple Access (FDMA) sheme [8], all RF tags wake up periodically (every 17 seconds) and back-scatter their data simultaneously on different subcarriers, which leads to unnecessary power dissipation that scales up with subcarrier frequency and the number of tags deployed. In contrast, the proposed solution in this thesis allows each tag to wake up as needed based on the identification code of the OOK transmitter and results in a dramatic reduction of the overall power consumption as only one tag is selected for backscattering at a time. Furthermore, this allows easier system scheduling simply by changing the OOK packet and offers simpler receiving process because the embedded receiver can listen only in one channel.

6.1 Thesis Contributions

1. 2.4 GHz OOK receiver for the tag (Chapter 2).
2. Uplink backscatter communication at 2.45 GHz using 2-FSK (Chapter 3).
3. Solar harvesting system for the embedded radio boards (Chapter 4).

4. Extremely low power interface between the tag and the humidity sensor (Chapter 5).

5. Dynamic changes in the clock source of the tag's MCU having the capability to work with crystal oscillator and going into sleep mode (Chapter 5).

6.2 Future Work

The implementation of a backscatter link at 2.4 GHz is offering the advantage of interfacing with existing protocols in that frequency band (i.e. Wifi, Bluetooth, Zigbee). Therefore, our approach can be combined with Wireless Sensor Networks which implement these protocols [23] with the vision that custom low-cost ultra-low-power tag sensors can be compatible with existing IoT infrastructure.

The improvement of the tag's receiver sensitivity in order to achieve longer ranges is not an easy task. A better matching network between the demodulator and the antenna will improve slightly the sensitivity in a specific case where specific power and distance are encountered. The threshold of the custom binary ADC constitutes the bottleneck in the sensitivity of the receiver (2). So, we believe the approach must be focused on increasing the amplitude of the demodulator's output voltage and thus increasing the headroom for detection. This increase can be achieved with the addition of multiple cascading stages of voltage doublers but at the expense of increased noise figure.

Finally, a network based on Time Domain Multiple Access (TDMA) scheme can be implemented with this setup with the combination of algorithms for varying duty cycle. This approach offers the capability of programming the switching frequencies of each tag individually through the downlink communication. Also, only one tag can produce multiple sets of subcarriers and thus communicate with multiple receivers.

Chapter 7

Appendix

7.1 Schematics, PCBs & Bill of Materials

7.1.1 Single Diode Detector Test Circuit

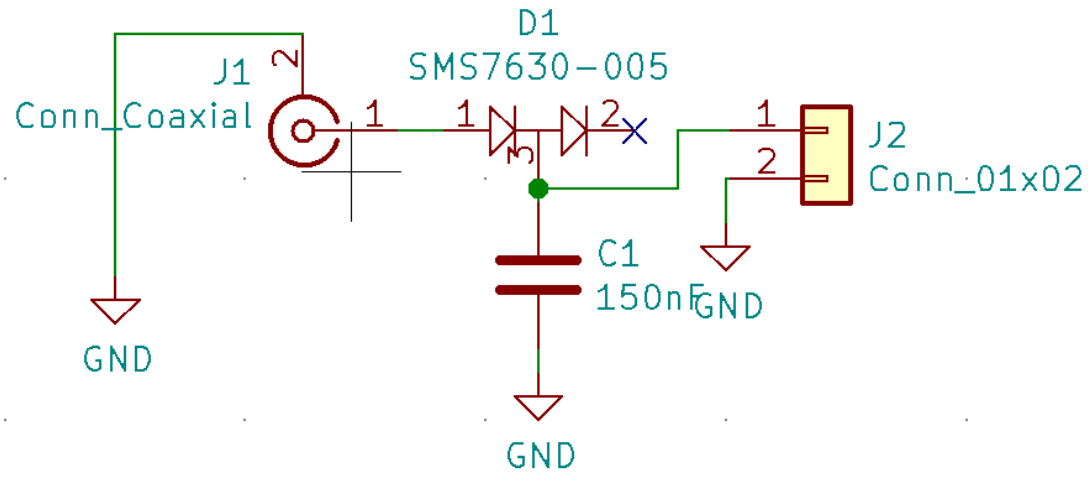

Figure 7.1: Schematic of the single diode detector testing circuit.

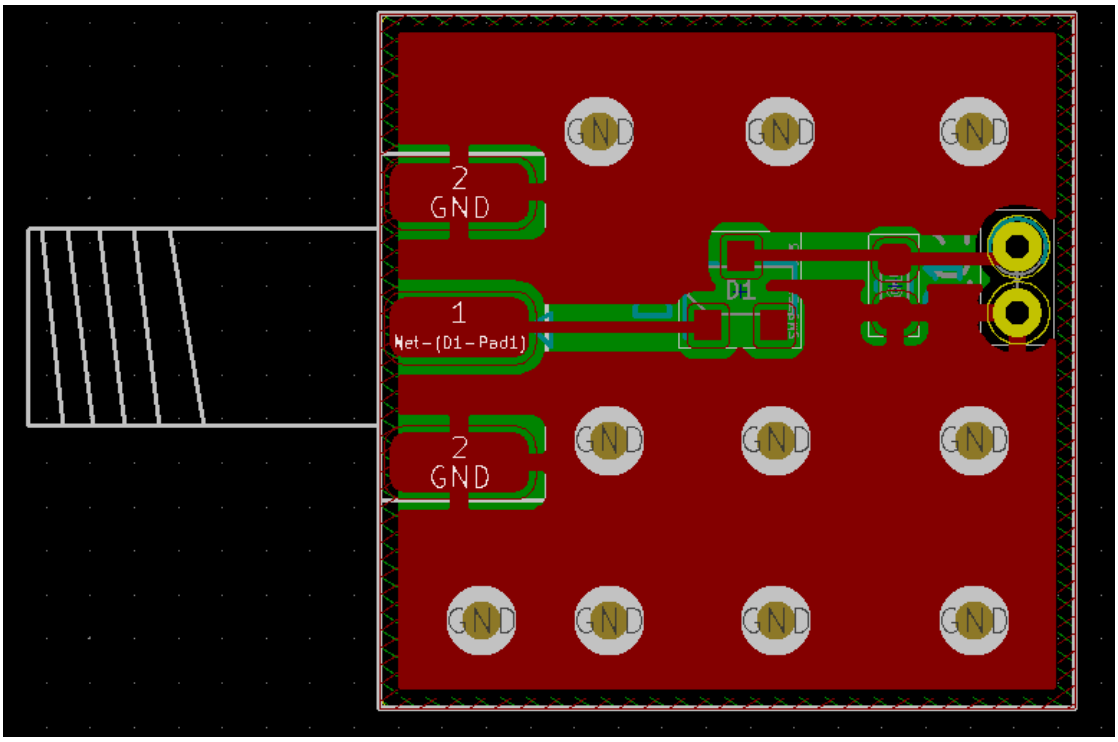

Figure 7.2: Layout of the single diode detector testing circuit with coplanar waveguide.

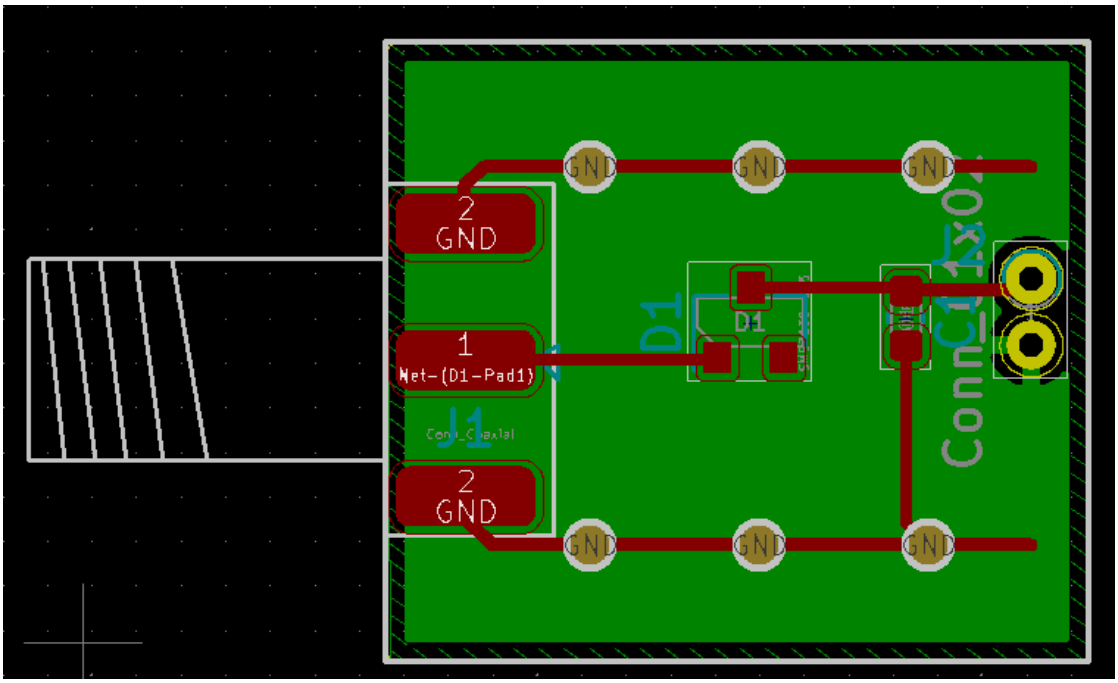

Figure 7.3: Layout of the single diode detector testing circuit with microstrip waveguide.

7.1.2 Voltage Doubler Detector Test Circuit

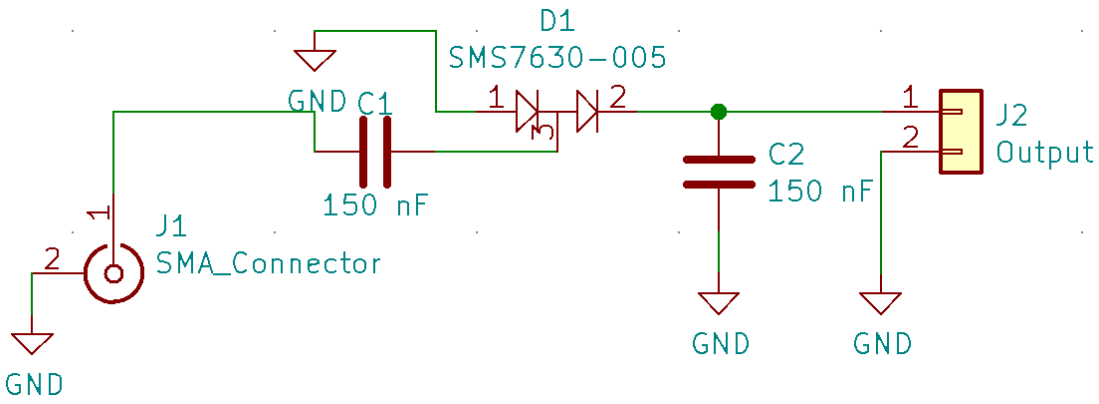

Figure 7.4: Schematic of the voltage doubler detector testing circuit.

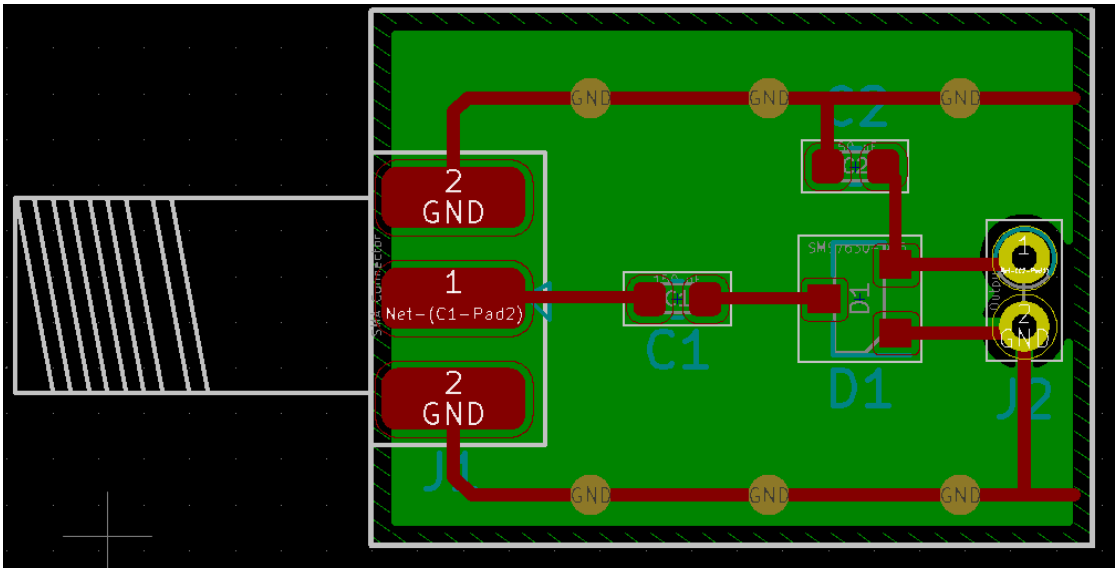

Figure 7.5: Layout of the voltage-doubler detector testing circuit.

Reference	Quantity	Value	Footprint	MFR	MFR Code
C1 C2	2	150 nF	0603_1608Metric	Wurth Elektronik	885012206072
D1	1	SMS7630-005	SOT-23	Skyworks	SMS7630-005LF
J1	1	SMA_Connector	SMA(F)_Taoglas_EdgeMount	Taoglas	EMPCB.SMAFSTJ.C.HT

Figure 7.6: Bill of materials of the voltage doubler detector testing circuit.

7.1.3 Single Diode Envelope Detector Circuit

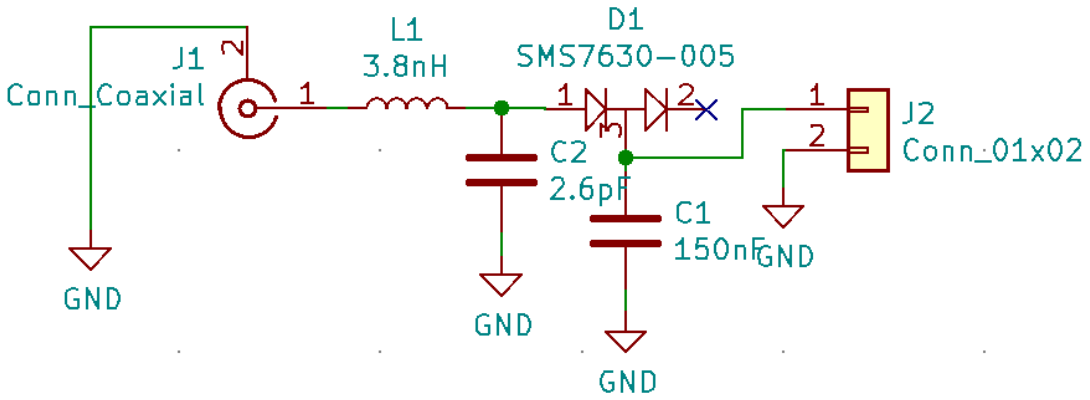

Figure 7.7: Schematic of the single diode envelope detector.

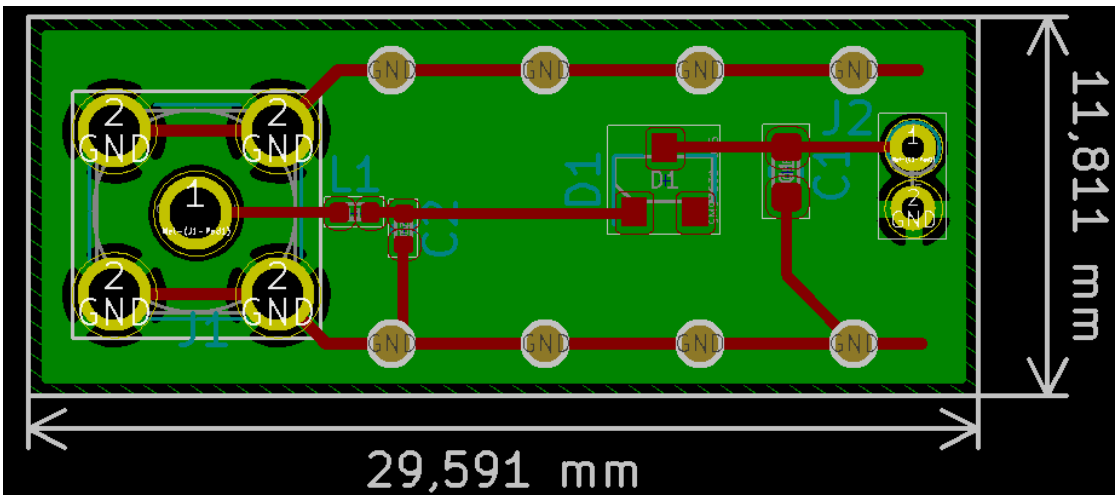

Figure 7.8: Layout of the single diode envelope detector.

Reference	Quantity	Value	Footprint	MFR	MFR Code
C1	1	150nF	0603_1608Metric	Wurth Elektronik	885012206072
C2	1	2.6pF	0402_1005Metric	Murata Electronics	GJM1555C1H2R6BB01D
D1	1	SMS7630-005	SOT-23	Skyworks	SMS7630-005LF
J1	1	Conn_Coaxial	SMA(F)_Taoglas_Vertical	Taoglas	PCB.SMAFSTJ.A.HT
L1	1	3.8nH	0402_1005Metric	Murata Electronics	LQW15AN3N8B80D

Figure 7.9: Bill of materials of the single diode envelope detector.

7.1.4 Voltage Doubler Envelope Detector

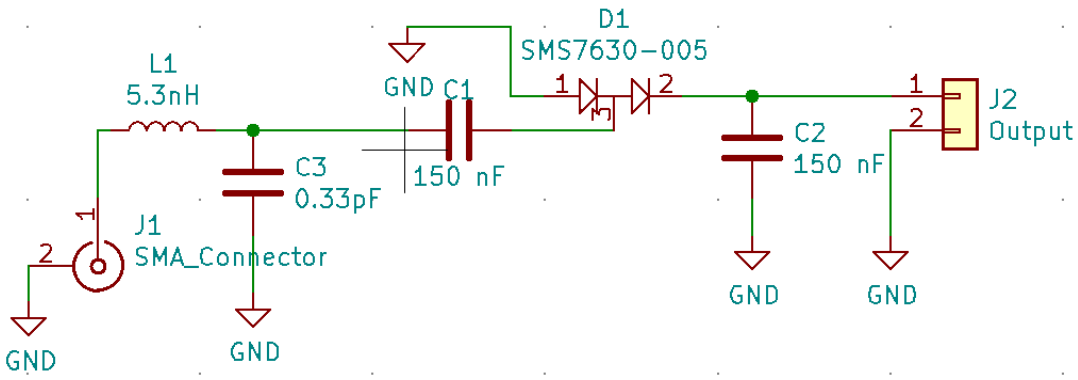

Figure 7.10: Schematic of the voltage doubler envelope detector.

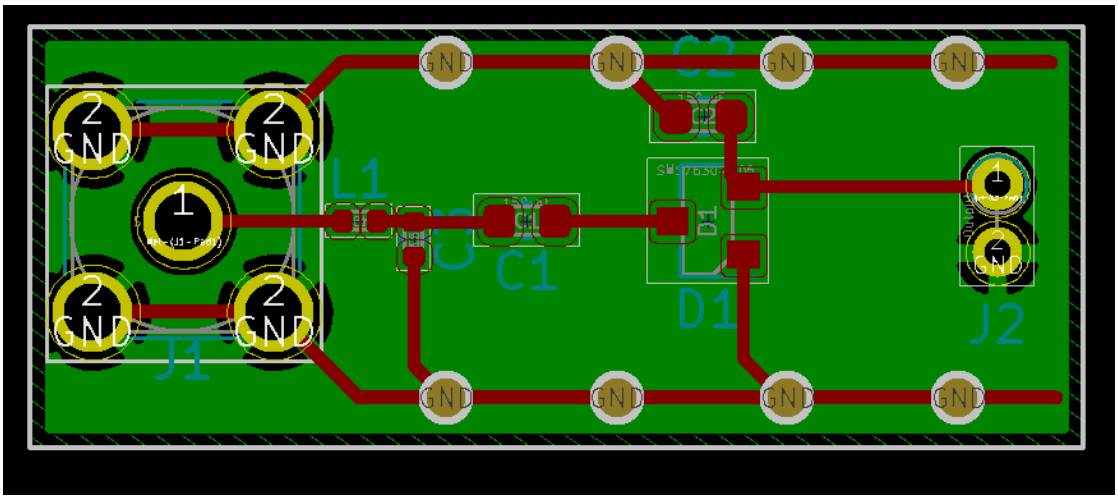

Figure 7.11: Layout of the voltage doubler envelope detector.

Reference	Quantity	Value	Footprint	MFR	MFR Code
C1 C2	2	150 nF	0603_1608Metric	Wurth Elektronik	885012206072
C3	1	0.33pF	0402_1005Metric	Murata Electronics	GJM1555C1HR33BB01J
D1	1	SMS7630-005	SOT-23	Skyworks	SMS7630-005LF
J1	1	SMA_Connector	SMA(F)_Taoglas_Vertical	Taoglas	PCB.SMAFSTJ.A.HT
L1	1	5.3nH	0402_1005Metric	Murata Electronics	LQW15AN5N3C10D

Figure 7.12: Bill of materials of the voltage doubler envelope detector.

7.1.5 Custom Binary ADC Circuit

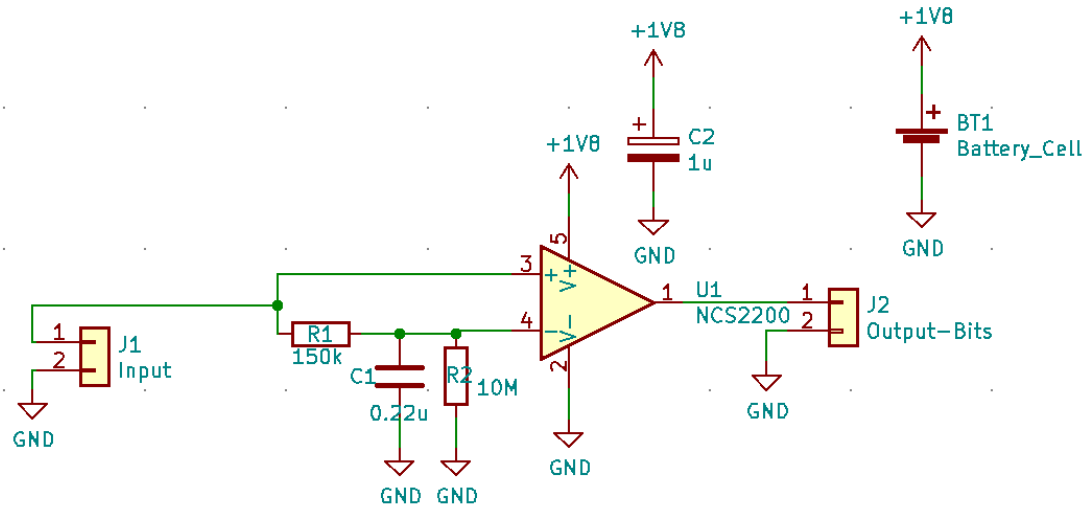

Figure 7.13: Schematic of the custom binary ADC circuit.

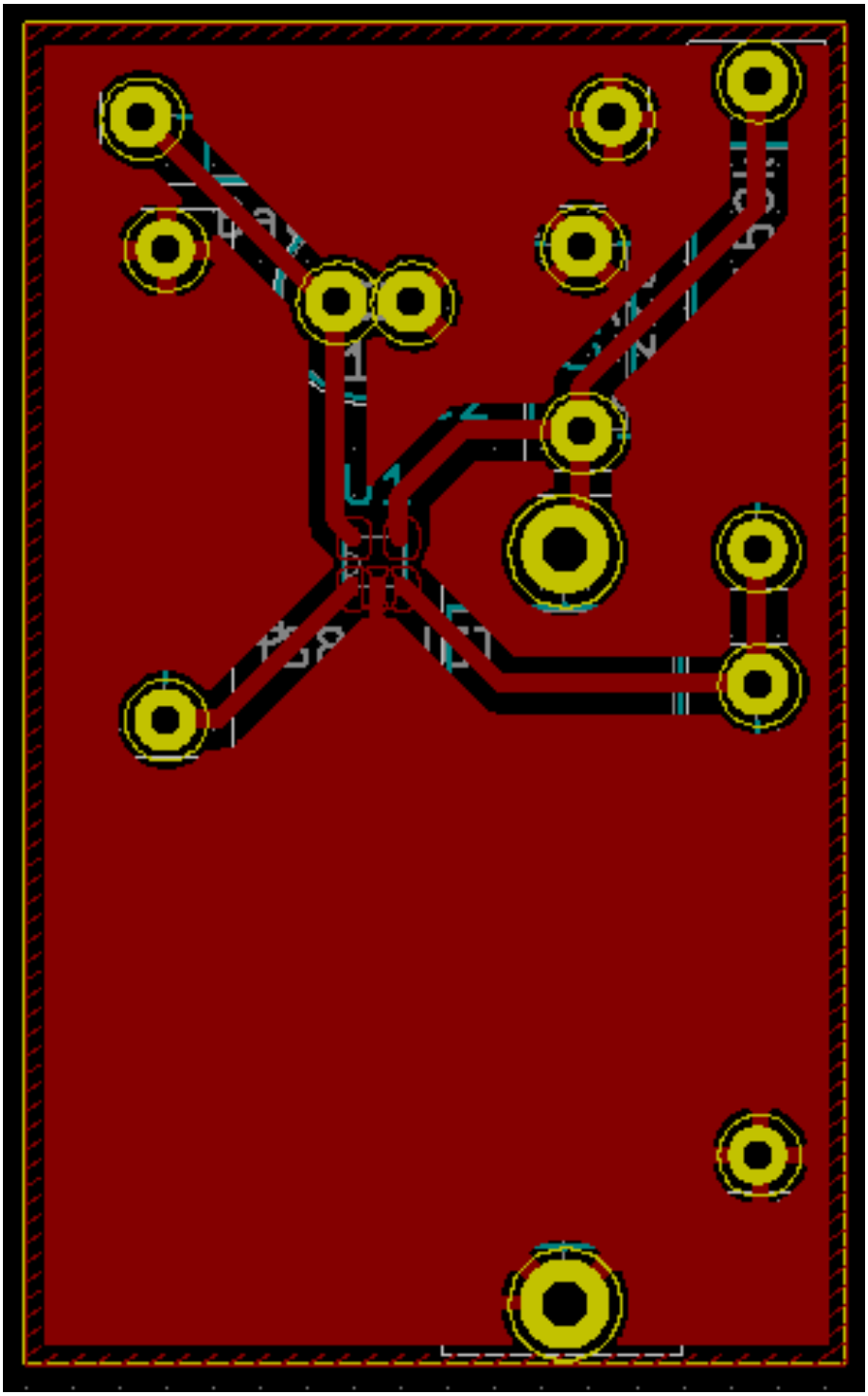

Figure 7.14: Layout of the custom binary ADC circuit.

Reference	Quantity	Value	Footprint	MFR	MFR Code
C1	1	0.22u	THT:C_Disc_D5.0mm_W2.5mm_P5.00mm	Vishay / BC Components	K224K20X7RF5TH5
C2	1	1u	THT:C_Radial_D5.0mm_H11.0mm_P2.00mm	Lelon	REA010M2CBK-0511P
R1	1	150k	THT:R_Axial_DIN0309_L9.0mm_D3.2mm_P12.70mm_Horizontal	Vishay / Dale	CCF07150KGKE36
R2	1	10M	THT:R_Axial_DIN0617_L17.0mm_D6.0mm_P20.32mm_Horizontal	Ohmite	ON1065E-R58
U1	1	NCS2200	SC-70-5	ON Semiconductor	NCS2200SQ2T2G

Figure 7.15: Bill of materials of the custom binary ADC circuit.

7.1.6 Solar Harvester: Power Management Circuit

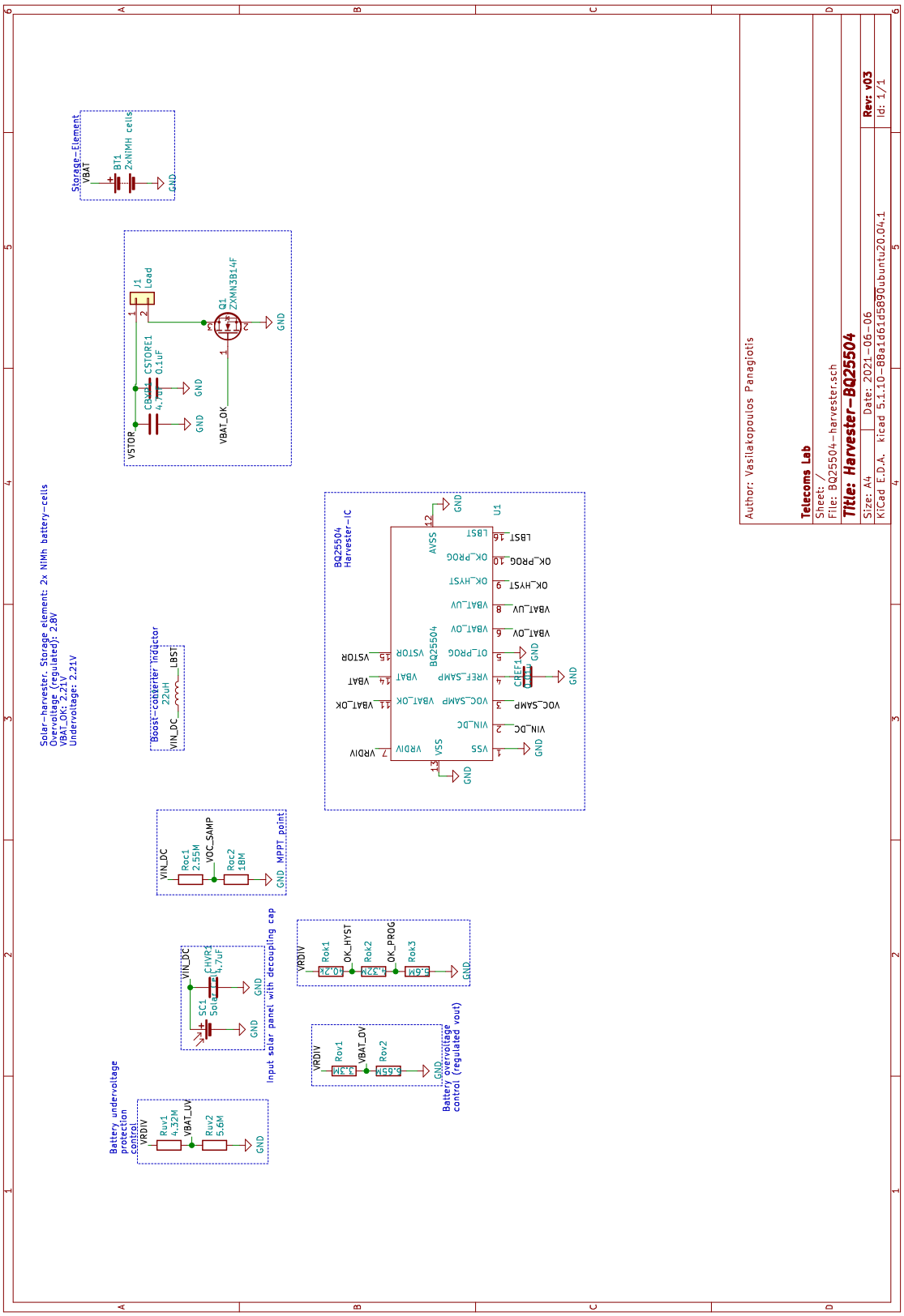

Figure 7.16: Schematic of the harvester's power management circuit.

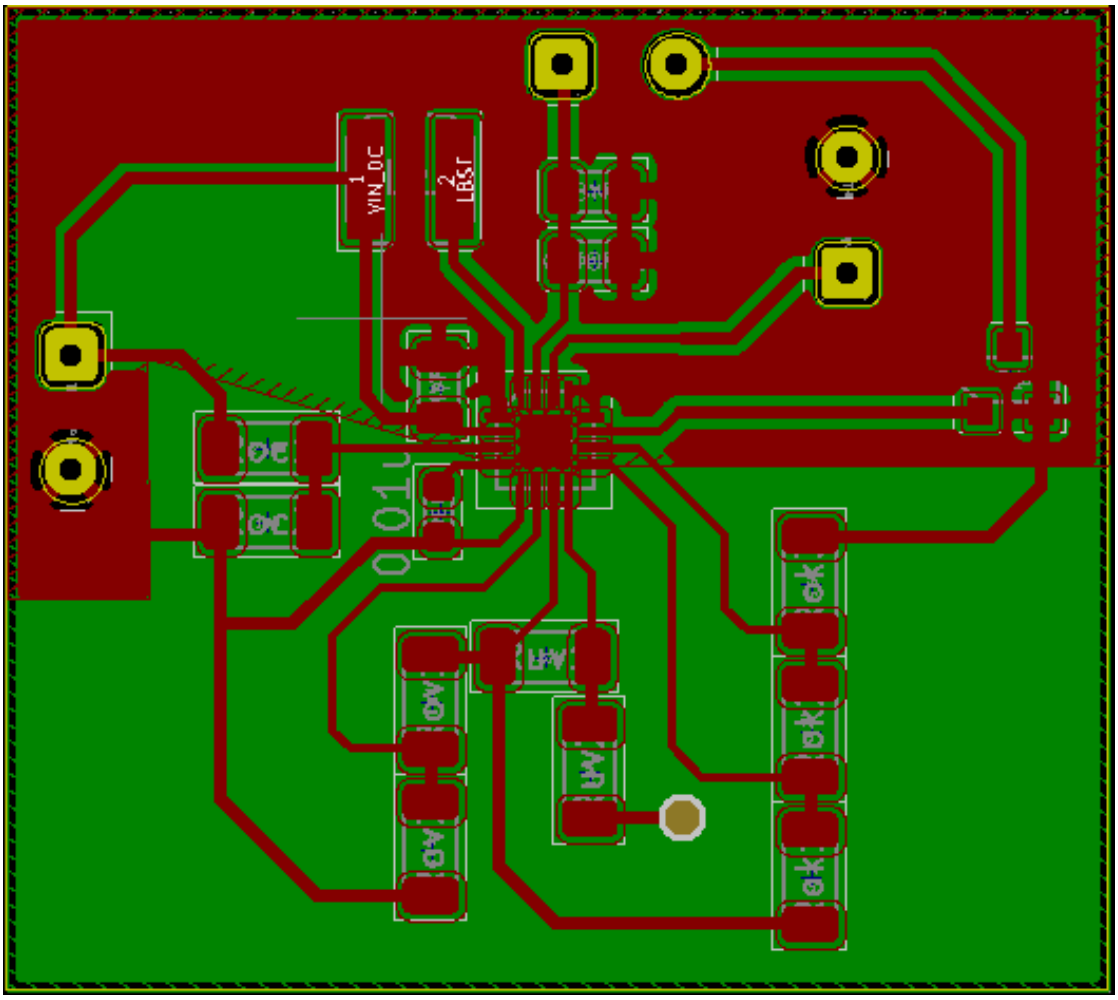

Figure 7.17: Layout of the harvester's power management circuit.

Reference	Quantity	Value	Footprint	MFR	MFR Code
CHVR1 CBYP1	2	4.7uF	0805_2012Metric	Samsung Electro-Mechanics	CL21A475KPFNNNE
CREF1	1	0.01u	0603_1608Metric		
CSTORE1	1	0.1uF	0805_2012Metric	Wurth Elektronik	885012207098
L1	1	22uH	Taiyo-Yuden_NR-40xx	Laird Performance Materials	TYA4012220M-10
Q1	1	ZXMN3B14F	SOT-23	Diodes Incorporated	ZXMN3B14FTA
Roc1	1	2.55M	1206_3216Metric	Vishay / Dale	CRCW12062M55FKEA
Roc2	1	18M	1206_3216Metric	KOA Speer	RK73B2BTTD186J
Rok1	1	40.2k	1206_3216Metric	Bourns	CR1206-FX-4022ELF
Rov1	1	3.3M	1206_3216Metric	Bourns	CR1206-JW-335ELF
Rov2	1	6.65M	1206_3216Metric	KOA Speer	HV73V2BTTD6654F
Ruv1 Rok2	2	4.32M	1206_3216Metric	Vishay / Dale	CRCW12064M32FKEA
Ruv2 Rok3	2	5.6M	1206_3216Metric	Bourns	CR1206-JW-565ELF
U1	1	BQ25504	VQFN-16-1EP_3x3mm_P0.5mm_EP1.6x1.6mm	Texas	BQ25504RGTT

Figure 7.18: Bill of materials of the harvester's power management circuit.

Bibliography

[1] *Detectors*, Tscm. [Online]. Available: http://www.tscm.com/detector.pdf

[2] A. P. Sample, D. J. Yeager, P. S. Powledge, and J. R. Smith, "Design of a passively-powered, programmable sensing platform for uhf rfid systems," in *2007 IEEE International Conference on RFID*, 2007, pp. 149–156.

[3] *HSMS-285x Series Surface Mount Zero Bias Schottky Detector Diodes IC, Data Sheet*, Avago Technologies. [Online]. Available: http://www.farnell.com/datasheets/47810.pdf

[4] V. Liu, A. Parks, V. Talla, S. Gollakota, D. Wetherall, and J. R. Smith, "Ambient backscatter: Wireless communication out of thin air," in *Proc. ACM SIGCOMM*, Hong Kong, China, 2013, pp. 39–50.

[5] *UG309: Thunderboard Sense 2 User's Guide, Technical Document*, Silicon Labs, 2020. [Online]. Available: https://www.silabs.com/documents/public/user-guides/ug309-sltb004a-user-guide.pdf

[6] V. Papageorgiou, A. Nichoritis, P. Vasilakopoulos, G. Vougioukas, and A. Bletsas, "Towards Ambiently Powered Inference on Wireless Sensor Networks: Asynchrony is the Key!" in *5th IEEE International Workshop on Wireless Communications and Networking in Extreme Environments*, Jul. 2021.

[7] "What is the iot? everything you need to know about the internet of things right now," 2020. [Online]. Available: https://www.zdnet.com/article/what-is-the-internet-of-things-everything-you-need-to-know-about-the-iot-right-now/

[8] G. Vougioukas, "Extended Range Scatter Radio Links with Embedded Radio," School of ECE, Technical Univ. of Crete, 2016.

[9] "Explain the Square Law Demodulation and Envelope Demodulation of AM Wave," 2015. [Online]. Available: https://electronicspost.com/explain-the-square-law-demodulation-and-envelope-demodulation-of-am-wave/

[10] *RF and Microwave Power Detection with Schottky Diodes, White Paper*, Infineon. [Online]. Available: https://www.infineon.com/dgdl/Infineon-AN_1807_PL32_1808_132434_RF%20and%20microwave%20power%20detection%20-AN-v01_00-EN.pdf?fileId=5546d46265f064ff0166440727be1055

[11] *Schottky Barrier Diode Video Detectors, White Paper*, Agilent Tchologies, 1999. [Online]. Available: https://g3ynh.info/circuits/diode_data/AN923.pdf

[12] *Surface Mount Mixer and Detector Schottky Diodes, Data Sheet*, Skyworks. [Online]. Available: https://gr.mouser.com/datasheet/2/472/skyworks_surface_mount_schottky_diodes_200041w-1213983.pdf

[13] B. Razavi, *RF Microelectronics*. New Jersey: Prentice-Hall, 1998.

[14] *RF Impedance Matching Calculator*, Analog Devices. [Online]. Available: https://www.analog.com/en/design-center/interactive-design-tools/rf-impedance-matching-calculator.html

[15] K. C. Adel S.Sedra, *Microelectronics Circuits*. Oxford University Press, 2020.

[16] *NCS2200, NCS2200A,NCS2202, NCS2202A, Data Sheet*, On Semiconductors, 2018. [Online]. Available: https://gr.mouser.com/datasheet/2/308/1/NCS2200_D-2317441.pdf

[17] G. Vougioukas, S. N. Daskalakis, and A. Bletsas, "Could battery-less scatter radio tags achieve 270-meter range?" in *2016 IEEE Wireless Power Transfer Conference (WPTC)*, Aveiro, Portugal, May 2016, pp. 1–3.

[18] J. Kimionis, A. Bletsas, and J. N. Sahalos, "Increased range bistatic scatter radio," *IEEE Trans. Commun.*, vol. 62, no. 3, pp. 1091–1104, Mar. 2014.

[19] *Wideband* 4 *GHz,* 43 *dB Isolation at* 1 *GHz, CMOS* 1.65 V *to* 2.75V*,* 2 : 1 *Mux/SPDT, Data Sheet*, Analog Devices, 2003–2016. [Online].

Available: https://www.analog.com/media/en/technical-documentation/data-sheets/ADG918_919.pdf

[20] *C8051F93x-C8051F92x, Data Sheet*, Silicon Labs, 2017. [Online]. Available: https://www.silabs.com/documents/public/data-sheets/C8051F93x-92x.pdf

[21] *BQ25504 Ultra Low-Power Boost Converter With Battery Management For Energy Harvester Applications, Data Sheet*, Texas Instruments, 2019. [Online]. Available: https://www.ti.com/lit/ds/symlink/bq25504.pdf?ts=1627043482746&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FBQ25504%253FkeyMatch%253DBQ25504%2526tisearch%253Dsearch-everything%2526usecase%253DGPN

[22] S.-N. Daskalakis, S. D. Assimonis, E. Kampianakis, and A. Bletsas, "Soil Moisture Scatter Radio Networking With Low Power," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 7, pp. 2338–2346, 2016.

[23] T. Nichoritis, "Design and Implementation of a Solar Powered Wireless Sensor Network for Autonomous Inference," School of ECE, Technical Univ. of Crete, 2021.