"Design of a high switching frequency FPGA-based SPWM generator for DC/AC inverters"

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Abstract

With the increasing concern about global environmental protection, the need to produce electric energy using pollution-free methods, such as solar energy, has been drawing increasing interest. In an effort to utilize the solar energy effectively, a great deal of research has been performed on the grid-connected PhotoVoltaic (PV) generation systems. The key element of grid-connected PV systems is the DC/AC inverter, which is used to interface the energy generated by the PV source into the electric grid. The power section of the DC/AC inverter is controlled by a control unit according to the Sinusoidal Pulse Width Modulation (SPWM) principle. The digital SPWM generation unit implementations have dominated over their counterparts based on analog circuits.

In this thesis, an FPGA-based SWPM generator is presented, which is capable to operate at switching frequencies up to 1MHz (requiring FPGA operation at 100-160MHz), thus it is capable to support the high switching frequency requirements of modern power electronic DC/AC converters. The proposed design exhibits architectural flexibility features, enabling the change of the SPWM switching frequency and modulation index either internally, or externally. The proposed SPWM unit has been implemented in a single chip in order to enable the reduction of the DC/AC converter control unit complexity, cost and development time. Thus, the main contribution of this work is a system which is more than an order of magnitude faster in switching frequency vs. previously proposed ones and it has a more flexible architecture which can be tuned to a variety of PV energy production applications. Additionally, compared to the past-proposed designs, the proposed SPWM generation system exhibits less deviation of the generated SPWM output voltage from its theoretical value and consumes less power during operation.

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CHAPTER 1

1. Introduction

The first chapter of this Master thesis provides some introductory information about the operation of DC/AC converters (inverters), the various control schemes typically applied in order to adjust the magnitude and frequency of the ac output voltage. The motivation for conducting research in digital controllers is described and the application on real systems as well as the scientific contribution of this work is summarized. Finally describes the structure of this thesis.

1.1 Motivation

With the increasing concern about global environmental protection, the need to produce energy using pollution-free methods, such as solar energy, has been drawing increasing interest as an alternative source of energy for the future since solar energy is clean, pollution-free and inexhaustible. In an effort to utilize the solar energy effectively, a great deal of research has been done on the grid-connected photovoltaic generation systems.

There is renewed focus on the power electronic converter interface for dc energy sources. A specific example of such dc energy sources that has a role in distributed generation and sustainable energy systems is the photovoltaic (PV) module. The combination of a PV module and an inverter forms an AC module and this is generally called PV-MIPS (Photovoltaic Module with Integrated Power Conversion System). The general objectives of the PV-MIPS idea are the development of low cost photovoltaic modules with integrated inverters that can feed directly into the grid. The photovoltaic AC-modules have become a future trend in PV system technology [1, 2, 3].

Photovoltaic power supplied to the utility grid is gaining more and more visibility, while the world's power demand is increasing. Many PV-systems have so far been interconnected with the grid due to the continuously decreasing cost. The price of the PV modules was in the past the major contribution to the cost of these systems. A downward tendency is now observed in the price of the modules and for this reason the cost of the single-phase grid-connected inverters is becoming more visible in the total cost.

A PV system generates the highest power output when each PV module is continuously operated at its maximum power point. This can be achieved by using module-integrated inverters. In this case, every PV module has its own controller. Module integrated inverters lead to higher yields with PV systems that are partially shaded or aligned with different angles. The unique conditions of the PV-MIPS concept are:

- Ease of installation
- No DC cabling
- Higher output in case of shading
- Flexibility in system size

Inverter topologies can basically be divided into two main types: Voltage Source Inverters (VSI) and Current Source Inverters (CSI) [4]. The VSI is principally a step down converter and needs at least about 700V for a proper and accurate sinusoidal current feed-in into a 3 phase, 400 V grid. In contrast to that, the CSI has a step up characteristic and there is an upper limit for the input voltage in order to ensure a proper inverter operation, which is about 540 V for a 400 V 3-phase system.

A VSI in combination with a high voltage PV-module would require an MPP voltage of at least 700 V. The idling module easily would exceed a voltage of 1 kV. Discussions with PV-module manufactures revealed, that this would cause a lot of problems. Modules typically are tested and certified up to 1 kV. Thus a boosting configuration, e. g. as in Fig. 1, would be required. The high number of parts, which affects the reliability performances and costs and the poor estimated efficiency motivated to look for another topology.

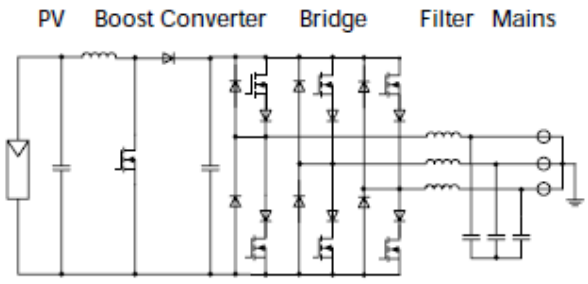

Fig. 1. Topology of Module Integrated Converte r (MIC) with boost stage and voltage source inverter with external diodes for improved switching.

The CSI is more promising than the VSI. As mentioned above its inherent characteristic is boosting and thus allows an MPP-voltage far below 1 kV. By using the CSI it is possible to implement a 1-stage inverter (Fig. 2). This topology has a low number of parts and the critical electrolytic capacitors are replaced by a choke. This choice is striking as the CSI is known from high power drives. Lately, it was used for fuel cell inverters in the kW-range. The application in a 200 W PV-inverter is a novelty.

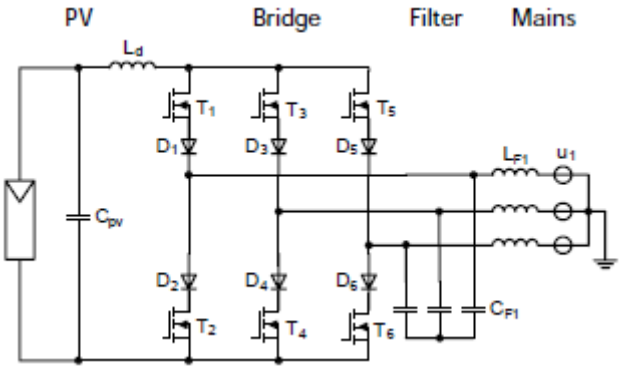

Fig. 2. Topology of Module Integrated Converter (MIC) based on a Current Source Iinverter with a choke in the DC-link and the required series-diodes in each leg.

The first generation of grid connected photovoltaic systems was composed of several strings of panels associated in parallel and connected to a single inverter. Such centralized approach had as disadvantages the necessity of string diodes (with their inherent power losses) and high voltage DC cabling. Furthermore, since operation was limited to only one maximum power point (MPP) for the whole array, mismatch losses reduced the system efficiency. Finally, due to the high power level of the inverter, there was little flexibility on system expansion.

At present, most of the systems at low and medium power levels are composed of a single or multiple strings of modules connected to an inverter, the so-called string and multi-string inverters, respectively. This way, in contrast with their predecessors, losses due to maximum power point tracking (MPPT) mismatch were reduced, but not totally eliminated and string diodes are not necessary anymore.

The next expected evolution on grid connected photovoltaic systems is considered as the integration of the converter in the module and is usually named AC Module or Module Integrated Converter (MIC), since the output of the panel can now be directly connected to the mains. A

major highlight of such an approach is the elimination of MPPT mismatches, allowing optimal coupling between panel and inverter and therefore increasing the generated power per module. In addition, the small level of power and modularity allows flexibility in system expansion and low purchase investment, being considered as the best option for end-user applications. Since the output of the panels can be directly connected to the grid, DC cabling and installation expertise are not necessary, allowing considerable reduction in installation expenses. Though, a higher production cost per produced Watt is expected for this approach, the mass production of such small units may in the end increase competitiveness due to economy of scale. A disadvantage of the module integrated solution is the strict requirement of a design with long lifetime under harsh ambient conditions that needs to be tackled by a highly robust power electronic design, since maintenance is much more complex than the ones of traditional string inverters [5].

Generally, the photovoltaic module integrated converter system consists of a step-up DC/DC converter connected to a single-phase full-bridge inverter. Since the PV module supplies low dc voltage to the MIC, a step-up DC/DC converter must boost the PV voltage to a level that can be converted to the ac grid voltage. Meanwhile, the grid connected full-bridge inverter generates ripple current at twice the grid-frequency in the PV module, which decreases the average power generation from the PV module. Thus, large electrolyte capacitor is usually utilized to reduce the ripple current. However, it has a large volume and a relatively short lifespan. Active compensation methods using an active power filter, a dc power smoothing circuit and an external bidirectional dc-dc converter were proposed for low frequency ripple current elimination. However, additional circuits are necessary, which increase the overall cost and decrease the entire system efficiency. Fig. 3 and 4 show the diagrams of alternative Module Integrated Converter (MIC) topologies [6].

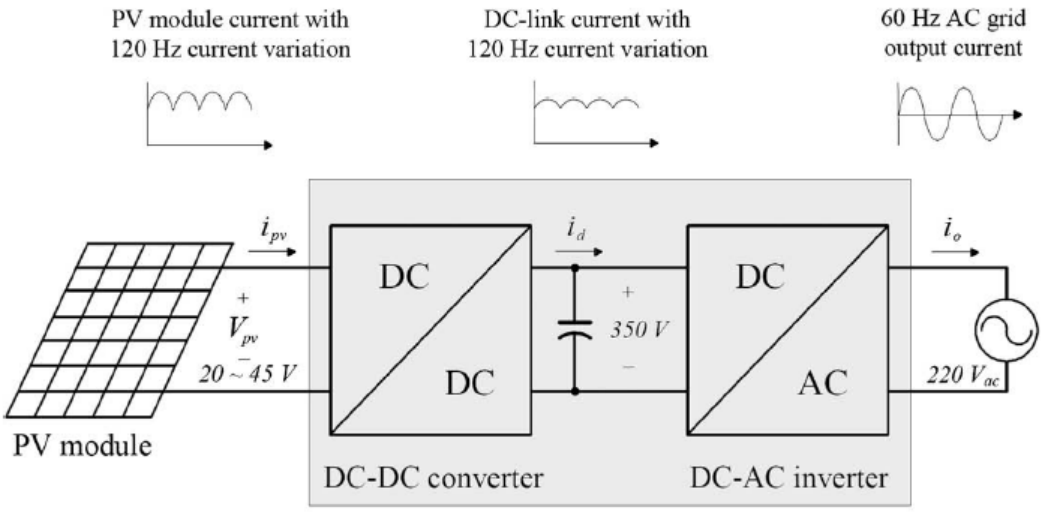

Fig. 3. Block diagram of a single-phase grid-connected PV MIC system.

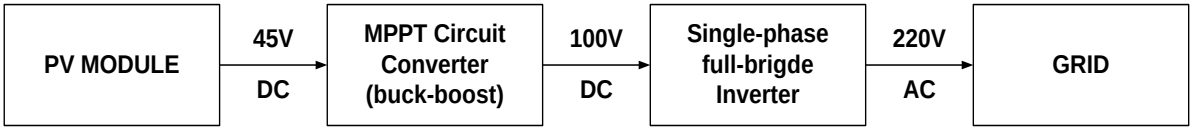

Fig. 4. Block diagram of a MIC system employing a buck-boost converter.

The trinity efficiency, cost and lifetime gives in general the orientation on the topology choice and on most of the project development. It is mainly affected by the amount and rating of components in such a way that simple topologies are preferable with the condition that components are not under severe current or voltage stress. Cost itself has been mainly one of the critical obstacles for the further expansion of module integrated solutions. Aside from the specification of the components, it is also strongly influenced by the fact that the lower the power rating is, the higher is the cost per produced kWh. In order to reduce such disparity, mass production is a mandatory condition and may only be achieved by flexible solutions capable of operating with most of the available panels in the market. That leads to the necessity of high voltage gain capability as PV panels usually have output voltages around 30 and 50V. The alternative PV inverter topologies are illustrated in Fig. 5 [7, 8, 9, 10].

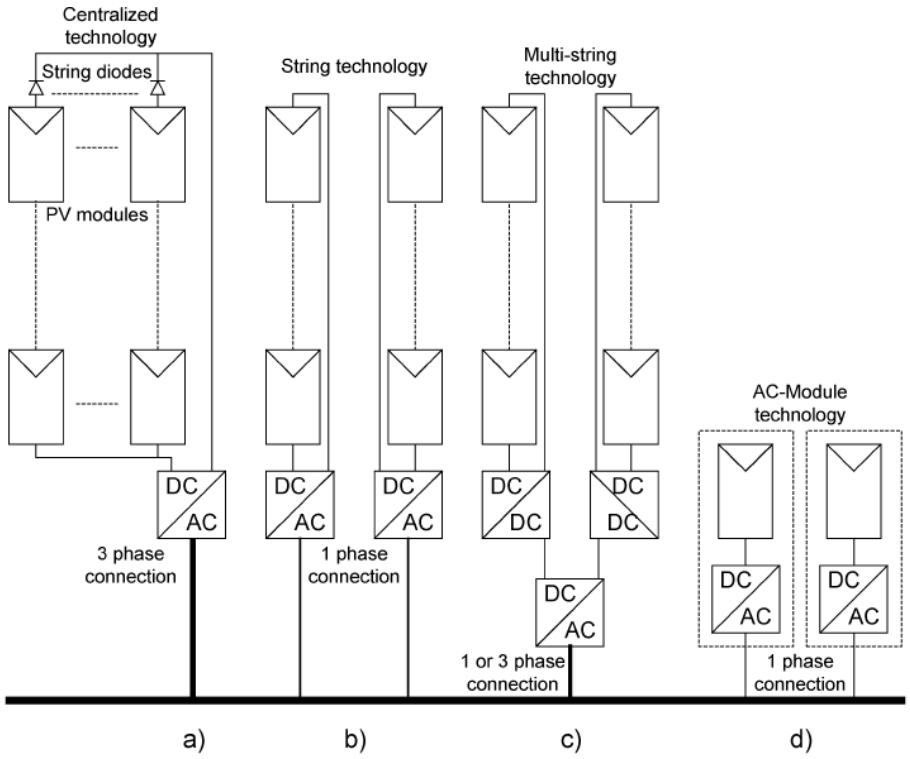

Fig. 5. Historical overview of PV inverters. (a) Centralized technology. (b) String technology. (c) Multi-string topology. (d) Future AC-module topology.

A. Centralized inverters

The centralized inverters (Fig. 6) are interfaced to a high number of modules. The modules are normally connected in both series, called a string and parallel in order to reach a high voltage and power level. This results in some limitations, such as the necessity of high voltage DC cables between the modules and the inverter, power losses due to a centralized MPP Tracking (MPPT), mismatch between the modules and the requirement to use string diodes. If one of the modules in a string becomes shadowed, then it will operate as a load with lower power generation of the PV array as a consequence. On the other hand, if the modules are connected in parallel, the shadowed module is still generating power, but the input voltage to the inverter is inevitable lower due to the parallel connection.

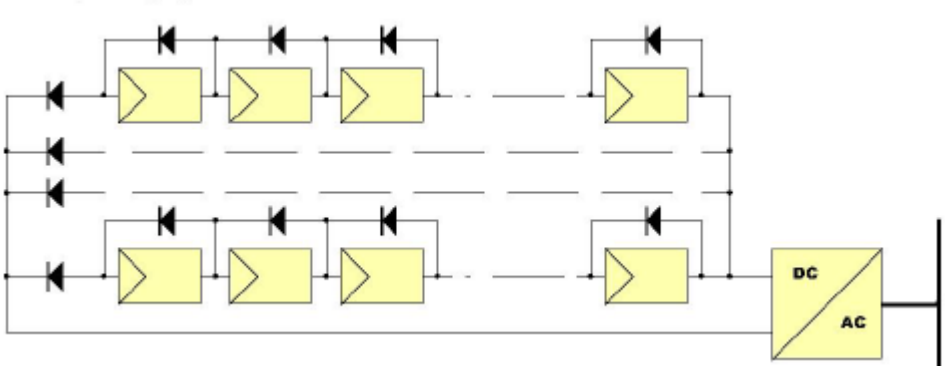

Fig. 6. The PV aaray configuration in the centralized inverter topology.

B. String inverters and AC-modules

String-inverters (Fig. 7) use a single string of modules to obtain a high input voltage to the inverter. However, the high DC voltage requires an examined electrician to perform the interconnections between the modules and the inverter. On the other hand, there are no losses generated by the string diodes and an individual MPPT can be applied for each string. Yet, the risk of a hot-spot inside the string still remains.

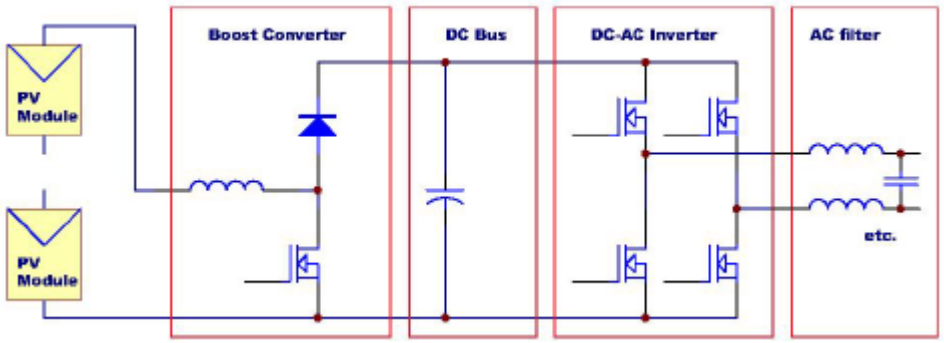

Fig. 7. String-inverter topology.

The AC-Module (Fig. 8), where the inverter is an integrated part of the PV-module, is an interesting solution since it avoids the losses due to mismatch between modules and inverter. Moreover, the hot-spot risk is removed and a better efficiency may be achieved. It also includes the possibility of an easy enlarging of the system due to the modular structure. The opportunity to

become a ‘plug and play’ device, which can be used by persons without any education in electrical installations, is also an inherent feature.

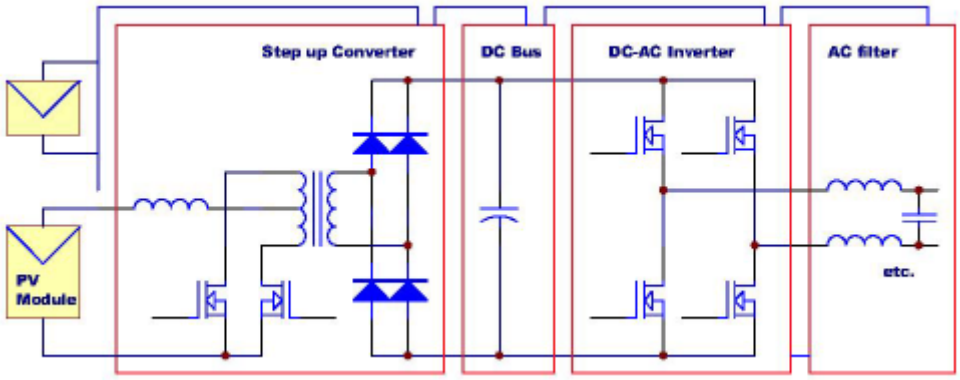

Fig. 8. Main circuit configuraion of the Module Integrated Converter (MIC) topology.

C. The future: AC-cells

A solution for the future could be the AC-cell, which is the integration of one PV-cell and the inverter. The main challenge for the inverter is to amplify the cell’s inherent very low voltage up to an appropriate level for the grid-connected inverter and at the same time to reach a high efficiency. For the same reason, entirely new converter technologies are requested.

In grid-connected photovoltaic power generation systems, a DC/AC inverter is employed to transfer the DC energy into the electric grid, as already mentioned. Usually the inverter is controlled so as to generate the output current in phase with the grid voltage (i.e. unity power factor) in order to achieve the maximum active output power injection and the minimization of the reactive output power. There are various control strategies to control the factor power and fundamental current waveform. The overall efficiency of grid-connected photovoltaic power generation systems depends on the efficiency of the DC/AC conversion process. Therefore, a key consideration in the design and operation of inverters is how to achieve high power conversion efficiency [11].

The use of DC/ AC inverters is required for two reasons: i) the low DC voltage generated by the photovoltaic (PV) modules must be amplified to a higher AC level in the grid and ii), the power

produced by PV the modules is very sensitive to the point of operation and the inverter should therefore incorporate a function for tracking the Maximum Power Point (MPP).

Switch-mode DC/AC inverters are also used in AC-motor drives and uninterruptible AC power supplies where the objective is to produce a sinusoidal AC output voltage whose magnitude and frequency can both be controllable. The switch-mode inverter is a converter through which he power flow is reversible. However, most of the time the power flow is from the dc side to the motor on the ac side, requiring an inverter mode of operation. Therefore, these switch-mode converters are often referred to as switch-mode inverters. A simplified block diagram of a DC/AC power converter is depicted in Fig. 9.

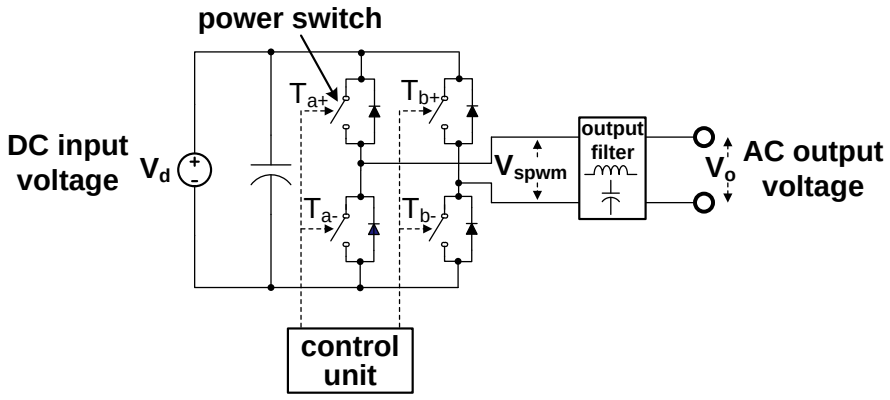

Fig. 9. DC/AC power converter (inverter) block diagram.

Pulse width modulation (PWM) is a widely used technique for controlling the output of static power converters. By using PWM techniques, the frequency spectrum of the input waveforms can be changed such that major non-fundamental components are at relatively high frequency. As to the software aspects, there are many different PWM techniques proposed in the existing literature such as Sinusoidal PWM (SPWM), space-vector PWM, selected harmonic elimination PWM. Among these techniques, SPWM scheme is the most popular one in both practical applications and literature introductions.

The vast development in industrial power conditioning equipment over the past two decades has resulted in the development process from research side demanded by the automation industry. Also, this period was outstanding due to the revolution of technological possibilities in the field

of digital electronic control by microcontroller, digital signal processor (DSP), complex programmable logic devices (CPLD), field programmable gate array (FPGA) and application specific integrated circuit (ASIC) technologies. Among all these possibilities, the FPGA is a good candidate having the advantage of the flexibility of a programming solution, the efficiency of a specific architecture with a high-integration density and high speed. In the field of digital control in electrical systems, advanced microprocessors and programmable logic devices are playing a critical role. Though FPGAs have been used for two decades in electrical and control engineering applications, now they are used in other domains as well. These include the use of hardware description languages (HDLs. Due to the high gate densities, availability of hardware/software resources and low cost, the FPGAs can target a large market of application specific standard products [12].

With the development of microprocessors and their peripheral circuits, some of the problems existing in digital control technology have been greatly improved and gradually replace the analog control technology to achieve the traditional control functions. PWM technology is a very important part of the power electronic technologies. It has huge function to enhance the performance of power electronic devices and promote the development of power electronic technologies.

Sinusoidal Pulse Width Modulation (SPWM) changes the pulse-width modulation of full-bridge DC/AC inverters based on PWM technique. The pulse width time duty ratio is arranged according to the sine rule, so that the output waveform to be sinusoidal whose magnitude and frequency should both be controllable. Traditional SPWM is mainly composed by analog circuits, whereas the triangular and the sine-wave are composed by discrete devices. These waves are then synthesized to get the SPWM waveform by comparator, thus SPWM to obtain a higher accuracy. The disadvantage is lack of control flexibility, fact that does not facilitate to compose closed-loop control system with the microcomputer system. With the continuous development of digital communications technologies and integrated circuits, direct digital synthesis (DDS) and programmable logic gate array (FPGA) have been widely used. DDS as a new type of frequency synthesizer technology has many characteristics such as high frequency resolution, fast frequency conversion speed and the output phase-continuous when the frequency changes and easy to implement a variety of modulation functions. [13].

In the field of digital control in electrical systems, advanced microprocessors and Programmable Logic Devices (PLDs) are playing a critical role. Due to the higher gate densities and lower cost, FPGAs can target a large market of Application Specific Standard Products (ASSPs). Field Programmable Gate Array (FPGA) vendors are offering the software and hardware resources and Computer Aided Design (CAD) tools for their devices. SPWM algorithms can be developed using HDL and the detailed tutorial of Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL). This method is as flexible as any software solution. Another important advantage of VHDL is that it is technology independent.

The real time implementation of a PWM control scheme requires high performance digital controllers such as Digital Signal Processors (DSPs), FPGAs and combination of them. During 1980s, the low performance microprocessors were used [14]. In late 1990s, the DSPs were used for Power Electronics (PE) converter control [15]. DSPs provide the sequentially executable software solution and FPGA provide the concurrently executable hardware solution. Each device is having specific merits and demerits in terms of speed, input/output (I/O) capabilities and memory space/chip resources to store the application software and data size in signal processing. Since, FPGAs are executing the control statements concurrently they offer the high speed computation in real time. Therefore, FPGA has been extensively used in many Power Electronics Converter (PEC) control like DC/DC converters, matrix converters, resonant converters, converters for power factor correction applications and AC/DC converters.

FPGA technology allows developing specific hardware architectures within a flexible programmable environment. This specific feature of FPGAs gives designers a new degree of freedom compared to microprocessor implementations, since the hardware architecture of the control system is not imposed *a priori*. However, in many cases, the development of this architecture is rather intuitive and not adapted to the implementation of more and more complex algorithms. Thus, in order to benefit from the advantages of the FPGAs and their powerful CAD tools, the designer has to follow an efficient design methodology. Such a methodology rests on three main principles: the control algorithm refinement, the modularity and the best suitability between the algorithm to implement and the chosen hardware architecture.

1.2 Scientific contribution

In past years, power conversion systems have been implemented using very precise analog IC's with complex control methodology in order to achieve the required performances. Due to analog nature, these systems are difficult to upgrade and modify. Recently, there has been a growing interest in digital controllers, due to their low power consumption and high immunity to noise (temperature changes, components aging, etc.). Moreover digital systems are the most suitable ones to implement sophisticated control schemes composed by simply interfacing circuits. Among the various advantages of digital approach, design flexibility is the most valuable one, as well as accurate time delay compensation. Digital control methods are now offering good alternatives to analog approaches. Due to the advance of digital technology, the implementation of digital controllers has become feasible, which vary from the use of DSP, microprocessors and FPGA, to software-programmable mixed-signal integrated circuits. Compared to analog circuit, digital controllers offer a number of salient advantages [16].

(1) **Enabling the implementation of advanced control algorithms:** it is much easier to implement advanced control techniques into a digital control system, some of which are considered impractical for analog realization. Advanced control schemes may help in improving the performances of power converters in terms of dynamic performance, efficiency, stability, etc.

(2) **Flexibility and programmability:** the use of software or programmable memory to change the controller functionality makes a system based on a digital controller very flexible. The design can be easily adapted or modified to meet new requirements. It is also very easy to implement power management algorithms in digital controllers, which is increasingly becoming a standard requirement.

(3) **Less susceptible to component and ambient variations:** analog controllers suffer from component tolerance variation and drift due to ambient conditions and aging. A digital controller can precisely position the poles and zeros and requires fewer components. Thus, the digital control system is less susceptible to these variations.

FPGA is a Programmable Logic Device (PLD) developed by Xilinx comprising thousands of logic gates. Some of them are combined to form a Configurable Logic Block (CLB). A CLB simplifies higher-level circuit design. Interconnections between logic gates using software are defined through SRAM or ROM, which will provide flexibility in modifying the designed circuit without altering the hardware. Concurrent operation, less hardware, easy and fast circuit

modification, comparatively lower cost for complex circuitry and rapid prototyping make it the favorite choice for prototyping an Application Specific Integrated Circuit (ASIC). The advent of FPGA technology has enabled rapid prototyping of digital systems. So, today, electronic industries and researchers try to develop digital control schemes for power conversion systems.

The digital SPWM generation unit implementations have dominated over their counterparts based on analog circuits, since they offer higher noise immunity and less susceptibility to voltage and temperature variations [17]. Typically, microcontrollers, Digital Signal Processors (DSPs) or Field Programmable Gate Arrays (FPGAs) are used for the implementation of the SPWM generation unit and the execution of DC/AC inverter control algorithms (e.g. fuzzy logic, motor speed control etc.) [18]. FPGAs have the advantage of flexibility in case of changes and they enable the reduction of the execution time of the DC/AC inverter control algorithm due to their capability to integrate digital hardware with high-speed and parallel processing features. Frequently, a microcontroller, DSP or FPGA-based unit is used to execute the DC/AC inverter control algorithm and output the results to a separate analog or digital SPWM generator, which produces the control signals of the DC/AC inverter power switches. The integration of both the control and SPWM units in the same chip has the advantage of reducing the design complexity and total system cost [19].

In this thesis, an FPGA-based SWPM generator is presented, which is capable to operate at switching frequencies up to 1MHz (requiring FPGA operation at 100-160MHz), thus it is capable to support the high switching frequency requirements of modern power electronic DC/AC converters [20-22]. The proposed design exhibits architectural flexibility features, enabling the change of the SPWM switching frequency and modulation index either internally, or externally. The proposed SPWM unit has been implemented in a single chip in order to enable the reduction of the DC/AC converter control unit complexity, cost and development time. Thus, the main contribution of this work is a system which is more than an order of magnitude faster in switching frequency vs. previously proposed ones and it has a more flexible architecture which can be tuned to a variety of applications. Fig. 10 depicts the block diagram of a PV power production system with the FPGA-based control unit which implements the SPWM algorithm developed in this thesis.

In order to assure that the proposed architecture can reach high operating switching frequencies compared to previously proposed designs, five more architectures where studied and

implemented on the same target device. As it will be demonstrated in the experimental results Section, their maximum operating switching frequency does not exceed 250 kHz.

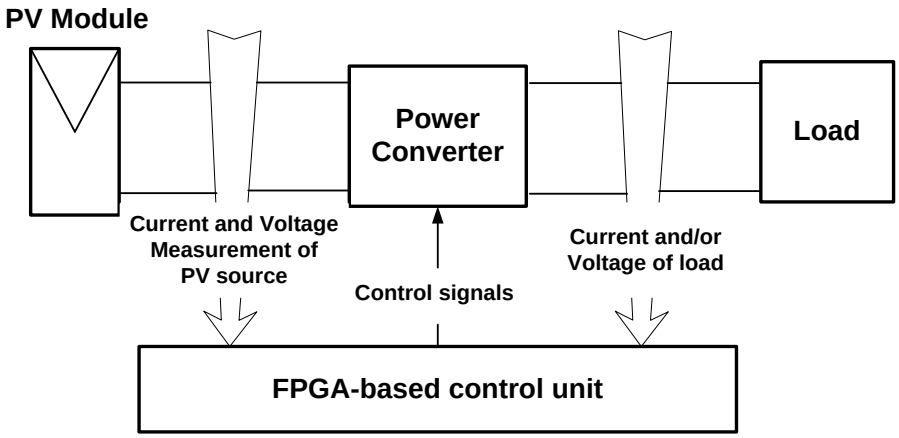

Fig. 10. Block diagram of a PV power production system with an FPGA-based control unit.

1.3 Structure of the thesis

The remainder of this thesis is organized as follows:

- **Chapter 2** presents relevant research which focuses on digital implementation of SPWM, describing the field of interest of other works.

- **Chapter 3** describes the way that the past-proposed architectures generated the SPWM pattern in different low operating switching frequencies.

- **Chapter 4** proposes the new SPWM hardware architecture, capable to operate at switching frequencies up to 1MHz and describes in detail the design and implementation of this new architecture. It also highlights the differentiations made on the previously proposed architectures in order to produce a unipolar SPWM waveform for a single-phase inverter and thus be fully compatible with the newly proposed architecture.

- **Chapter 5** demonstrates the successful operation of the newly introduced SPWM architecture with post place-and-route simulation and experimental results for design verification and actual runs on hardware for design validation and proof-of-concept.

- **Chapter 6** shows the comparison of the proposed SPWM generator with other methods and analyzes the reasons that this implementation has more efficient performance vs. the previously described architectures.

- **Chapter 7** presents the SMART project, ARTEMIS joint undertaking and suggests a possible contribution of the present thesis to this project.

- **Chapter 8** provides the conclusions made by this thesis and it also presents the future work for an integrated control unit that implements more algorithms.

CHAPTER 2

2. Theoretical Background and Relevant Research

This chapter introduces the theoretical background of the SPWM principle, the different SPWM types and how the SPWM algorithm works. Moreover, some other interesting works that have implemented a digital SPWM controller in low operating switching frequency are presented.

2.1 Theoretical background

Generally, two classes of PWM techniques can be identified: (i) optimal PWM (ii) carrier PWM [23]. The optimal PWM technique for producing switching patterns is based on the optimization of specific performance criteria. In this case, the converter switching patterns are calculated a priori for given operating conditions and are then stored in memory (look-up tables) for use in real time. Reduction in converter effective switching frequency is achieved and higher gain due to over-modulation is possible when compared with the conventional PWM scheme. However, the considerable computational effort of solving nonlinear equations to derive the switching angles, the large memory required to store the information for various modulation indexes and the relatively sophisticated control to allow smooth transient pattern changes, are considered to be serious practical difficulties.

The other class is based on comparing a certain low-frequency reference or modulating waveform with a high frequency carrier waveform. This technique is known as carrier PWM technique. The Sinusoidal Pulse Width Modulation (SPWM) technique is the most common one and it is based on the principle of comparing a triangular carrier signal with a sinusoidal reference waveform.

The SPWM principle is widely used in power electronic DC/AC converters (inverters) in energy conversion and motor control applications, in order to control the DC/AC inverter output voltage amplitude to the desired value. The SPWM waveform is a series of constant amplitude and different width rectangular pulse waveform equivalent to sine-wave.

2.1.1 SPWM types

There are two types of SPWM: the bipolar voltage switching pattern and the unipolar one. Regarding to the first type, the diagonally opposite switches (T_{a+}, T_{b-}) and (T_{a-}, T_{b+}) from the two legs of the power bridge depicted in Fig. 11 are switched as switch-pairs 1 and 2, respectively. With this type of PWM switching, the output voltage waveform of the first leg of the inverter is determined by comparison of υ_s and υ_c in Fig. 12. The output of the inverter second leg is the complementary of the first leg output.

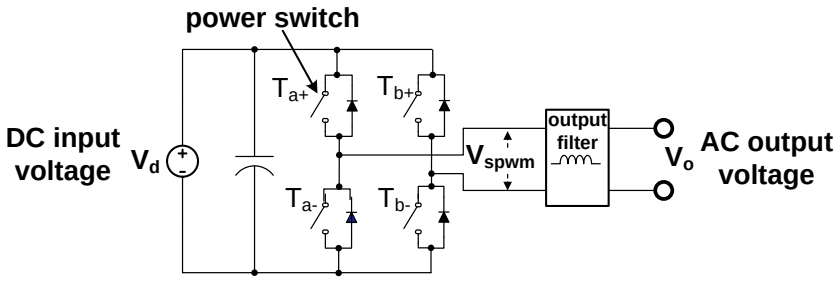

Fig. 11. Single-phase full-bridge inverter.

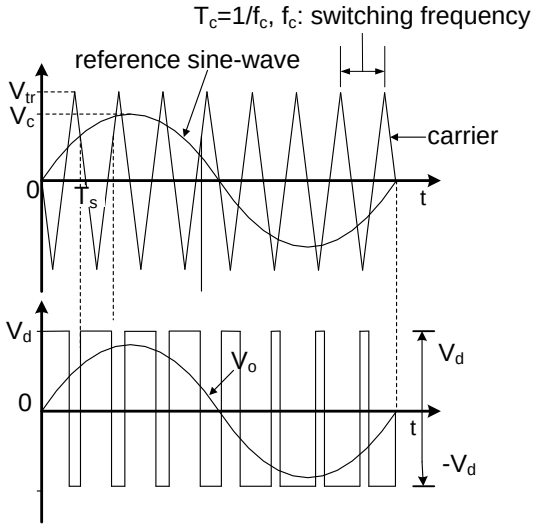

Fig. 12. Bipolar sinusoidal pulse width modulation.

In the second type of SPWM scheme, the unipolar one and on which this thesis is focused, the switches in the two legs of the full-bridge inverter of Fig. 11 are not switched simultaneously, as in the previous type. Here, the legs of the inverter are controlled separately. In this type of PWM scheme, when a switching occurs, the output voltage changes between 0 and $+V_d$ or between 0 and $-V_d$ voltage levels, as opposed to the PWM with bipolar (between $+V_d$ and $-V_d$) voltage switching scheme described earlier.

The power converter switches (e.g. MOSFETs, IGBTs etc.) are set ON or OFF according to the result of the comparison between a high-frequency, constant-amplitude triangular wave (carrier) with two low-frequency (e.g. 50 Hz) reference sine-waves of adjustable amplitude (Fig. 13) [24]. The intersection point determines the switching waveform.

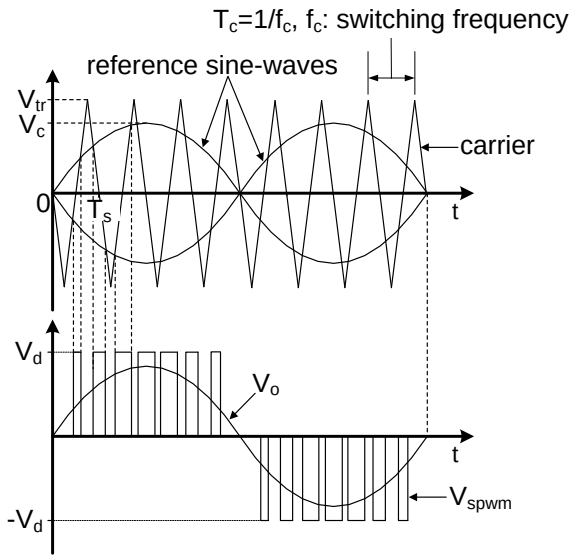

Fig. 13. Unipolar sinusoidal pulse width modulation.

The high-frequency harmonics of the generated SPWM signal, V_{spwm}, are then filtered using a low-pass LC- or LCL-type filter, thus producing the high-power and low-frequency sinusoidal waveform, V_o, at the DC/AC inverter output terminals. The amplitude of V_o is calculated as follows:

$$V_o = M \cdot V_d = \frac{V_c}{V_{tr}} \cdot V_d \quad (1)$$

where V_d (V) is the DC/AC inverter DC input voltage, V_c (V) and V_{tr} (V) are the reference sine-wave and carrier amplitudes, respectively and M is the modulation index which ranges from [0,1]. Increasing the triangular wave switching frequency, f_c, results in a reduction of the DC/AC inverter output filter size and cost. Depending on their nominal power rating, the DC/AC inverters typically operate at switching frequencies in the range of 1 kHz - 100 kHz [20, 25]. A further increase is expected in the near future [21] due to the development of Silicon Carbide (SiC) JFETs which are capable to operate at switching frequencies up to 3 MHz with low power losses [22].

2.1.2 SPWM techniques

Several techniques there have been developed in order to produce a regular sampled Sinusoidal Pulse Width Modulation by significantly reducing the number of calculations required and thereby allowing higher switching frequency SPWM to be generated with the minimum deterioration in performance [26]:

- **Symmetric modulation:** The modulating frequency f_m, carrier frequency f_c and sampling frequency f_s are in general independent and therefore any desired relationship between them can be defined. The sampling frequency f_s refers to the time instants that both sine and triangular wave are simultaneously sampled. The simplest relationship is to set $f_s = f_c$ and therefore to sample the modulating wave at the carrier frequency. This results in only one sample being taken every carrier cycle and therefore the sampled modulating wave is kept constant throughout the carrier period, resulting in each edge of the PWM pulse being modulated equally.

- **Asymmetric modulation:** Alternatively, $f_s = 2f_c$ can be used such that two samples of the modulating wave are taken in each carrier cycle. The first sample taken at the start of the carrier cycle is used to modulate the leading edge of the pulse and the second sample, taken at the middle of the carrier cycle, used to modulate the trailing edge. Since more samples of the modulating wave are used to produce asymmetric PWM, the harmonic spectrum is superior to that of symmetric PWM.

- **$f_s < f_c$:** Another possible relationship is to make $f_s < f_c$, that is to use less than one sample per carrier cycle. Thus, the number of samples of the modulating wave would be reduced and consequently the number of calculations is also reduced, allowing higher switching frequencies to be generated.

2.2 Related work

As already mentioned in the first chapter, the development of high performance microprocessors has encouraged work on digital PWM control. Implementation using microprocessors was introduced in order to provide a more flexible method of designing the system. The system offers a simple circuitry, software control and flexibility in adaptation to various applications.

In the FPGA-based SPWM generation units presented in [27-32], the triangular wave is implemented in the form of an up-down counter. Depending on the implementation, the reference sine-wave is sampled at the time instants corresponding either only to the nadirs [Fig. 14(a)] or both at the nadirs and the peaks [Fig. 14(b)] of the carrier wave. The corresponding samples are stored in digital format in a lookup table (LUT) implemented in the FPGA internal memory. The SPWM control signals are produced by comparing the corresponding values of the sinusoidal and carrier digital signals. Using these techniques, switching frequencies in the range of 1.157 kHz - 20 kHz have been achieved. The same design method has been applied in [19] for the development of an SPWM signal generation SoC based on the OpenRISC1200 32-bit RISC processor core.

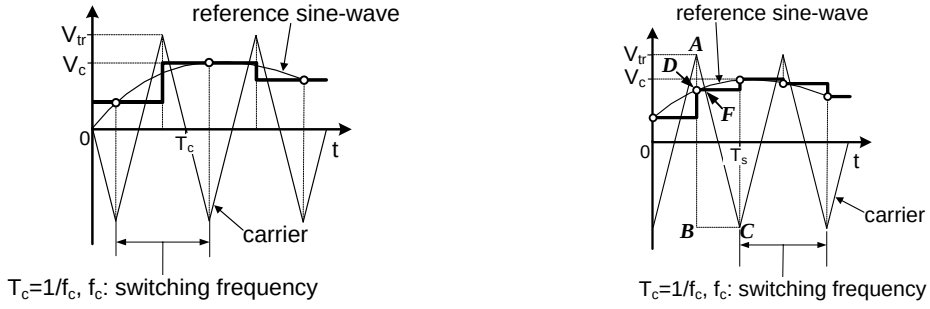

Fig. 14. The reference sine-wave digital representation in past-proposed SPWM generator design methods.

Targeting at the reduction of the SPWM generator memory requirements, the sinusoidal wave is produced in [33] using an FPGA-based implementation of the Coordinate Rotation Digital Computer (CORDIC) algorithm. A 5 kHz switching frequency has been achieved in this case. Although this implementation does not require the use of a hardware multiplier, it is characterized by a slower speed compared to the LUT-based SPWM units. CORDIC algorithm is a simple and efficient iterative technique to calculate basic trigonometric and hyperbolic functions such as cosine, sine, cosh, sinh. It is developed by Jack Volder and Andraka has explored several CORDIC's architectures and the implementation of the algorithm in FPGA. It is famous for its simplicity of implementing it in hardware because the CORDIC algorithm is merely just the repetition of addition/subtraction, bit-shifting and table lookup operations. It is commonly used when no hardware multiplier is available or when to minimize the number of gates required. However, when hardware multiplier is available, Digital Signal Processing (DSP) microprocessor, table lookup methods and power series are generally faster than CORDIC. CORDIC algorithm has many applications. One of them is to generate a digital sinusoidal (sine or cosine) wave. The digital wave generated by the CORDIC algorithm can then be used in various applications such as wireless/mobile and Software Defined Radio (SDR) systems.

An alternative approach has been proposed in [34, 35]. A lookup table is used to store the reference sine-wave digital values corresponding to the time instants of the triangular wave peaks and nadirs. The width of each pulse is calculated using an equation based on the similarity of the triangles ABC and ADF depicted in Fig. 14. This design method has been validated in case of a 1 kHz switching frequency.

In [3], the SPWM pulse-train is produced by comparing the sinusoidal and triangular signals generated according to the Direct Digital Synthesis (DDS) technique. The comparison is performed using a high-speed analog comparator. The DDS approach is also used in [36] for the development of a digital SPWM generator chip with 0.35μm CMOS technology. The maximum clock frequency of this chip is 50 MHz. DDS is a digital frequency synthesizer. By controlling the phase this directly produces a variety of different frequency and amplitude signals. DDS provides a higher frequency resolution, can fast realize frequency switching and maintain a constant phase when frequency changes. It is easy to realize a numerically controlled modulation of frequency, phase and amplitude. A DDS system is mainly composed by the phase accumulator, sine ROM look-up table and D/A converters.

In [37] the SPWM unit is composed of a DSP chip, accomplishing the calculation of the widths of the individual pulses comprising the SPWM wave, which communicates through a parallel port with an FPGA-based unit producing the SPWM control signals.

A common disadvantage of the previously proposed SPWM generators, described above, is that they have been designed to operate at low switching frequencies (i.e. 1kHz - 20 kHz), while their operation at higher switching frequencies has not been explored.

CHAPTER 3

3. Architecture Analysis of Previously Published SPWM Implementations

This chapter analyzes the architectures proposed by previously mentioned related works. The past proposed SPWM generators that are going to be compared with the newly introduced SPWM in this thesis are those that implement the triangular wave in the form of an up-down counter and the sampled reference sinusoidal wave is stored in digital format in a lookup table (LUT) implemented in the FPGA internal memory. The reference sine-wave is sampled at the time instants corresponding to nadirs, peaks, both at the nadirs and the peaks of the carrier wave or less than one sample per carrier cycle.

Another approach that has been proposed is the one that although it uses a lookup table to store the reference sine-wave corresponding to the time instants of the triangular wave peaks and nadir, there is no comparison between the sine and the triangular wave and the width of each pulse is derived by the calculation of an equation based on the similarity of two triangles, ABC and ADF that are formed between the two basic waves, as shown in Fig.15.

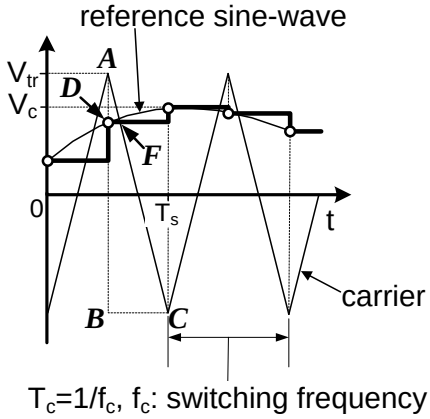

Fig. 15. The triangles ABC and ADF formed between the carrier and sinusoidal waveforms.

3.1 M. S. N. Romli, Z. Idris, A. Saparon, M. K. Hamzah

This architecture implements an SPWM generator by sampling the sine-wave at the nadir times of the carrier wave [29]. The output of SPWM is illustrated in Fig. 16. This specific architecture was implemented on a Xilinx FPGA device, XC4000XL with switching frequency 5 kHz.

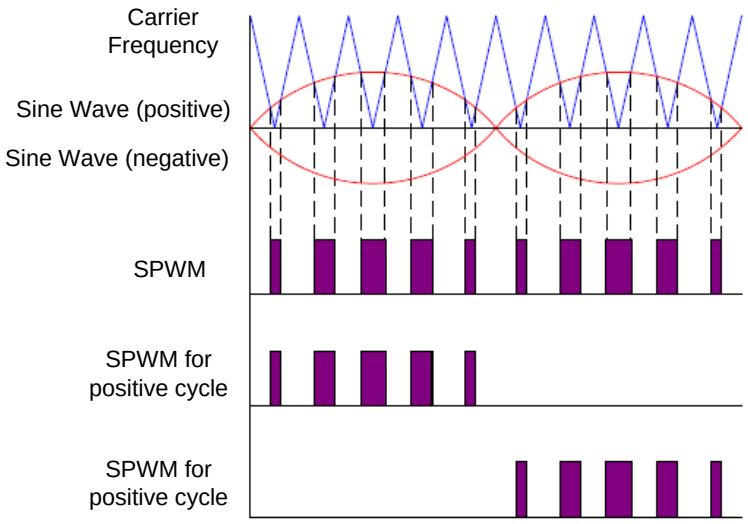

Fig. 16. SPWM formation.

The sine-wave used as a reference to generate the SPWM output is divided into 4 symmetrical Sections A, B, C & D as it can be shown in Fig. 17. B can represent a mirror of A. C & D can mirror the positive cycle of A & B, respectively. Hence by using section A, the other parts of the sine-wave B, C & D can be developed to generate respective representations. This approach reduces representations to 25% of the total required data to produce the reference. In this way, the sine-wave is produced by a quarter of a cycle.

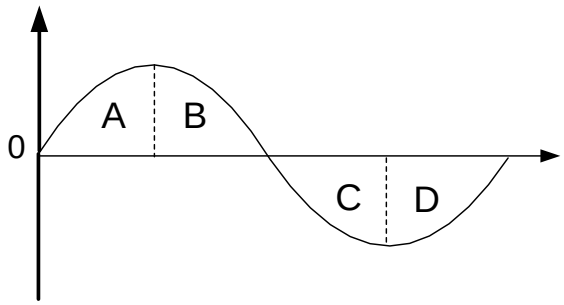

Fig. 17. Optimization concept.

Fig. 18 shows the flowchart of producing a sine-wave by a quarter of cycle. The first stage is the initialization for the block. Reset is used to reset the block and if reset is equal to 1 the system will detect the clock either it is rising or not. The system will only be active when the clock is rising. Then, the system will detect the count where it is equal to 0 or 24. If count equals to 0 then the DIR will equal to 1 (up) and if count equals to 24 then the DIR will equal to 0 (down). DIR stands for direction. When the direction is up, the count will count up and when the direction is down the count will count down.

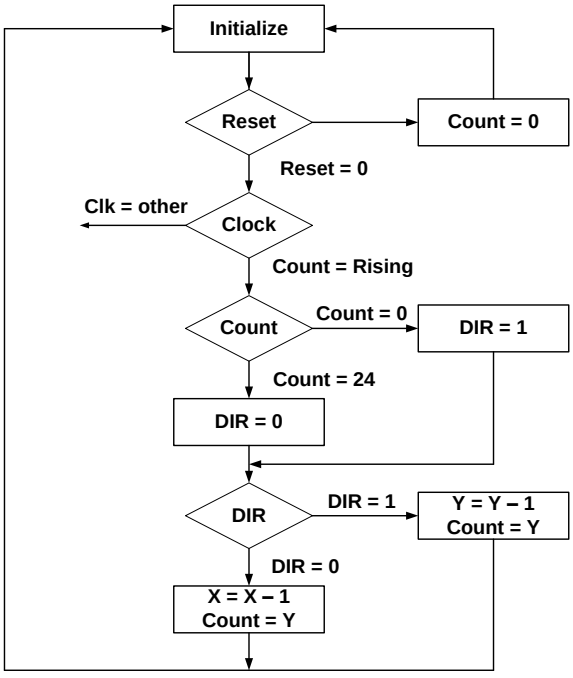

Fig. 18. The flowchart of the algorithm which produces sine-wave by a quarter of a cycle .

Fig. 19 shows the sampling process of the reference sine-wave in the nadir instants of the carrier wave. The inputs for Xilinx FPGA are the “Phase Detector”, “Main Clock” and “Modulation Index” signals. A phase detector is used to generate SPWM for the positive and negative cycles as shown in Fig. 20.

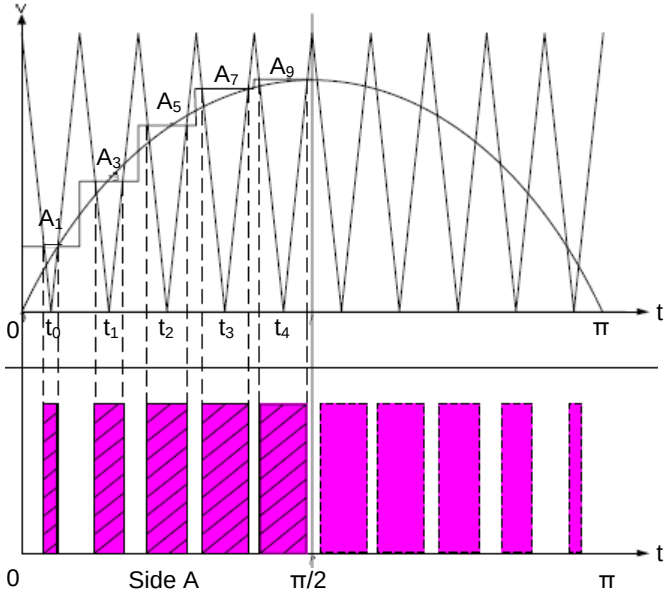

Fig. 19. Digital implementation of SPWM.

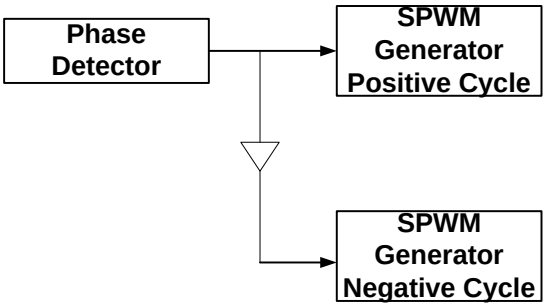

Fig. 20. Basic block diagram to generate SPWM in both cycles.

The overall block diagram of the SPWM generator is shown in Fig. 21 and the description of each component is presented in the following paragraphs.

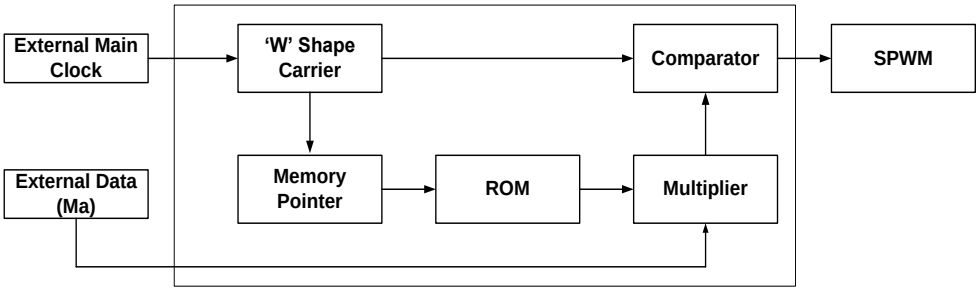

Fig. 21. Block diagram of SPWM.

The circuit consists of an up-down counter that generates an 'M' shape triangular waveform, produced by an eight-bit counter. This digitally increments the counter value from 0 to 255 and then subsequently decrements it back to 0 again over a period of time. This 'M' shape carrier signal is transformed to 'W' shape using an inverter and is then compared with the output of the multiplier obtained from multiplication of the modulating signal from the look-up table (ROM) with an external modulation index input.

Good accuracy requires high bit number. For optimization, an eight bit counter with a clock speed of 2.55 MHz was determined based on the following equation.

$$f_{clk} = f_c \times ((2^{n-1} - 1) \times 2) \quad (2)$$

where f_c is the carrier frequency (5 kHz), f_{clock} is the external main clock frequency and n = 8 is the bits for the up-down counter.

For a carrier of 5 kHz the use of sixteen bit counter is not possible due to the very high clock frequency (655.35 MHz) requirements. XC4005XL on the other hand has a maximum clock speed 80 MHz. It has been further shown that an 8-bit counter provides acceptable accuracies, resulting with a range of 0 to 255. The 'W' shape carrier waveform is designed using 8 bit up-down counter range from 0 to 255. The external clock is used as input to generate the 5 kHz carrier signal.

To facilitate variations in modulation index of 0 to 1 in steps of 0.1, the maximum value is divided by 10; i.e. 25.5. It uses 4 bit to multiply with the digital sample sinusoidal waveform in order to vary the amplitude of the reference signal. The memory pointer is then used to select the data in ROM and it uses the up counter to address the data. The carrier provides information in terms of clock pulse to other units. The pulse train is generated at every zero point of 'W' shape. The sample data of sinusoidal waveform which was calculated will stored in the Look-up Table (LUT). The samples data is calculated by using the following equation:

$$f_{clk} = \frac{(2^n - 1)}{10}\left\{\sin(2\pi fr \times (2k+1) \times \frac{Tc}{2}\right\} \quad (3)$$

where f_r is the reference frequency, f_c is the carrier frequency and k is the carrier pulse position. The multiplier is used to multiply the data from ROM with the external data (M_a). Actually, it is used to amplify the sample data (sinusoidal waveform) from ROM. The comparator is used to compare output data from the 'W' shape carrier signal with the output data from the multiplier. The SPWM pattern is generated from the output of comparator. The output of comparator is equal to one when the output of multiplier is greater than or equal to the carrier signal.

3.2 R. K. Pongiannan, P. Selvabharathi, N. Yadaiah

The second architecture implements a three-phase FPGA-based SPWM generator by sampling the sine-wave both at the nadir and the peak instants of the carrier wave with maximum switching frequency 20 kHz [32]. The SPWM IP core is designed using VHDL and a single FPGA device (SPARTAN XC3S400PQ208). The block diagram of this architecture is shown in Fig. 22.

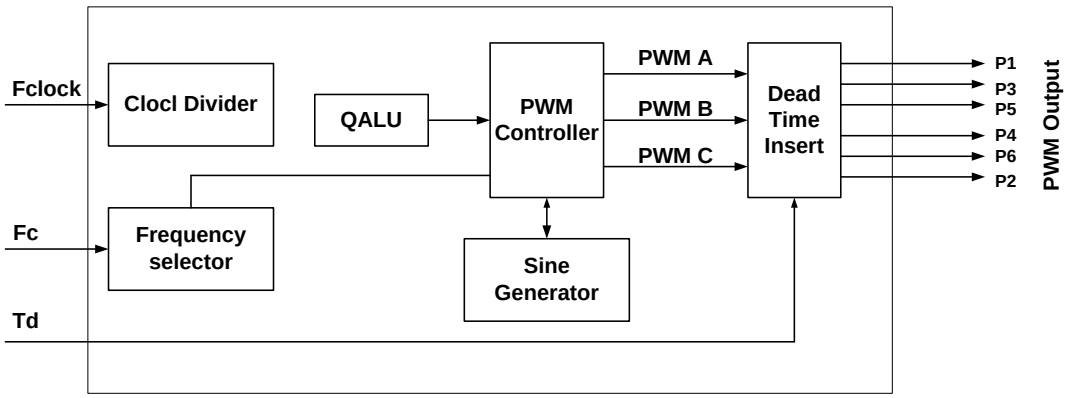

Fig. 22. Block diagram of the SPWM generator proposed in [32].

The reference sine-wave is generated by a sine generator module. The sine table is designed as a look-up table which contains the sine values for 180° of the sine-wave. The SPWM pulses are generated by comparing the sinusoidal reference and triangular carrier signals. The relation for the vertex sampling point t_1 and the nadir sampling point t_2 are evaluated using the following relations:

$$t_1 = \frac{T_c}{2} \times k \qquad (\text{when } k = 0, 2, 4, 6, ...) \tag{4}$$

$$t_2 = \frac{T_c}{2} \times k \qquad (\text{when } k = 1, 3, 5, 7, ...) \tag{5}$$

The frequency relation between the reference and carrier signals should satisfy the Nyquist theorem. One comparator and a counter are used to generate the PWM pulses. The frequency f_c can be varied by changing the f_{clk} and by adjusting the clock divider**.**

The authors suggest a QALU design that performs the data representation, arithmetic and logic operations in the SPWM algorithm using Q-Format. The QALU in FPGA is implemented as generic library function. The VHDL code for QALU arithmetic operations like addition and multiplication has been developed. This ALU can be used as core for designing FPGA based dedicated processors for inverter and motor control applications.

3.3 S. R. Bowes, D. Holliday

The authors of this work suggest an implementation that combines the two last SPWM techniques mentioned in Section 2.1.2 [26, 38]. The important features of this process is the relationship $f_s = 2f_c$ producing two different samples per carrier cycle, such that each consecutive pulse edge is modulated by a different amount, requiring a calculation to produce each switching edge. To reduce the number of calculations required, whilst still maintaining the same switching frequency, the $f_s < f_c$ condition is used in the first condition to produce the modulation process shown in Fig. 23.

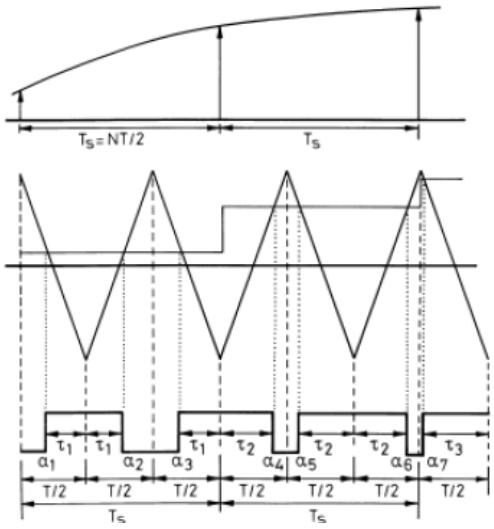

Fig. 23. High switching frequncy, low sampling frequency SPWM generation method. Sampling frequncy = f_s, sampling period = T_s, carrier frequency = f_c, carrier period = T, $f_s = 2fc/N$, $T_s = NT/2$.

In this figure the sampling frequency is reduced by *N* to give a sampling frequency relationship $f_s = 2f_c/N$, resulting in only one sample being taken every *N-samples* of the conventional asymmetric case. Thus, the number of calculations required to produce the complete PWM waveform is *N* times less than the conventional case. This is a substantial saving in calculation time which allows significantly higher switching frequencies to be used for the same number of calculations. The example used in Fig. 23 is for *N* = 3and as illustrated, one sample value of the modulating wave is used over three half carrier cycles, where $T_s = 3T/2$. This results in the degree of modulation being calculated once and this is then used on three consecutive switching edges before a new sample is used to calculate the next three consecutive switching edges. Thus, the

new low sampling frequency regular sampling process shown in Fig. 23 can be viewed as incorporating both symmetric and asymmetric PWM characteristics. As illustrated in Fig. 23 those pulses produced with the same sample value are symmetric and the pulses centered on a new sample value are asymmetric for odd *N*. Note that all pulses will be symmetric for even *N*.

3.4 L. Jiaz, Y. Xianggen, Z. Zhe, X. Qing

The last architecture proposes a different digital implementation of the SPWM generator on a single FPGA chip (LFEC10 from LATTICE Inc.) with operating switching frequency 1 kHz [34, 35]. The asymmetrical regular sampling strategy is illustrated in Fig. 24, which displays the sinusoidal modulation signal against the triangle carrier signal for a three-phase inverter.

Fig. 24(a) shows an operation of the PWM duty cycle generation process in the double update mode. In Fig. 24(b) the reference sine-wave value is greater than zero. Under this circumstance the control signal S2 will hold the high level and S4 will hold the zero level. The on-times and off-times control switch of S1 and S3 can be defined as:

$$S1\_ON = (t4 - t2) - (1/2) \times PWM\_DT \tag{6}$$

$$S1\_OFF = PWM\_TM - S1\_ON - PWM\_DT \tag{7}$$

$$S3\_ON = (t2 - t0) - (1/2) \times PWM\_DT \tag{8}$$

$$S3\_OFF = PWM\_TM - S3\_ON - PWM\_DT \tag{9}$$

where *S*1_ *ON* , *S*3 _*ON* are the on-times switch and *S*1_ *OFF*, *S*3 _ *OFF* are the off-times.

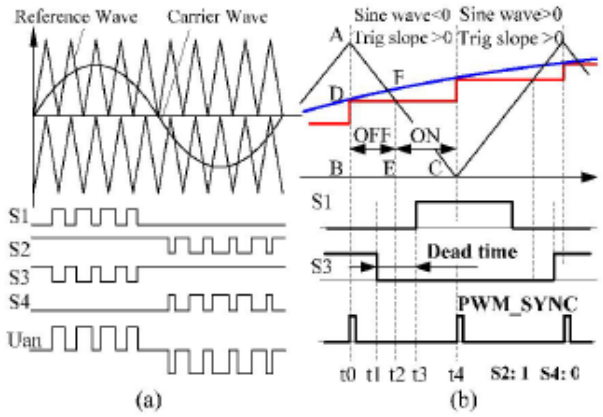

Fig. 24. SPWM generator implemented for a three-level NPC inverter.

In Fig. 25 the reference sine-wave value is less than zero. Under this circumstance, the control signal S3 will hold the high level and S1 will hold the zero level. The on-times and off-times which control switches S2 and S4 can be defined as:

$$S2\_ON = (t4' - t2') - (1/2) \times PWM\_DT \tag{10}$$

$$S2\_OFF = PWM\_TM - S2\_ON - PWM\_DT \tag{11}$$

$$S4\_ON = (t2' - t0') - (1/2) \times PWM\_DT \tag{12}$$

$$S4\_OFF = PWM\_TM - S4\_ON - PWM\_DT \tag{13}$$

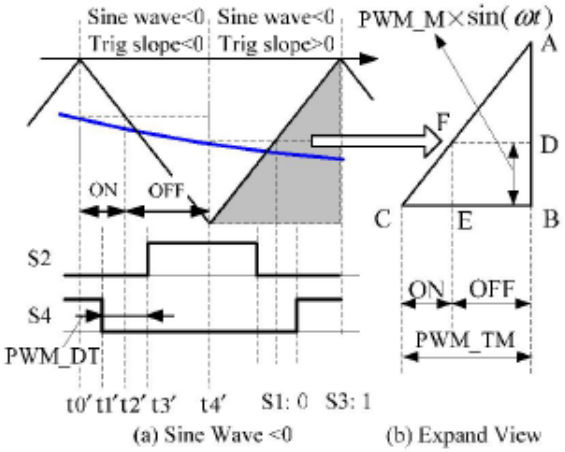

Fig. 25. Calculation of PWM duty cycle.

It can be seen that the two triangles $\triangle ABC$ and $\triangle ADF$ are similar triangles. From this relationship, it is possible to state that the corresponding lengths of the two triangles satisfy the relation:

$$\left|\frac{DF}{BC}\right| = \left|\frac{AD}{AB}\right| \tag{14}$$

So that:

$$\frac{PWM\_TM - CE}{PWM\_TM} = \frac{1 - PWM\_TM \times \sin(\omega t)}{1} \tag{15}$$

This expression can be solved for *CE* to yield:

$$CE = PWM\_TM \times PWM\_M \times \sin(\omega t) \tag{16}$$

When the value of the sine-wave is less than zero:

$$CE = t2' - t0' \tag{17}$$

$$t4' - t2' = PWM\_TM - CE \tag{18}$$

When the value of the sine-wave is greater than zero:

$$CE = t4 - t2 \tag{19}$$

$$t2 - t0 = PWM\_TM - CE \tag{20}$$

The expression for *CE* is the core mathematical formula of the PWM duty cycle calculation. Fig. 26 shows the block diagram of the digital controller developed.

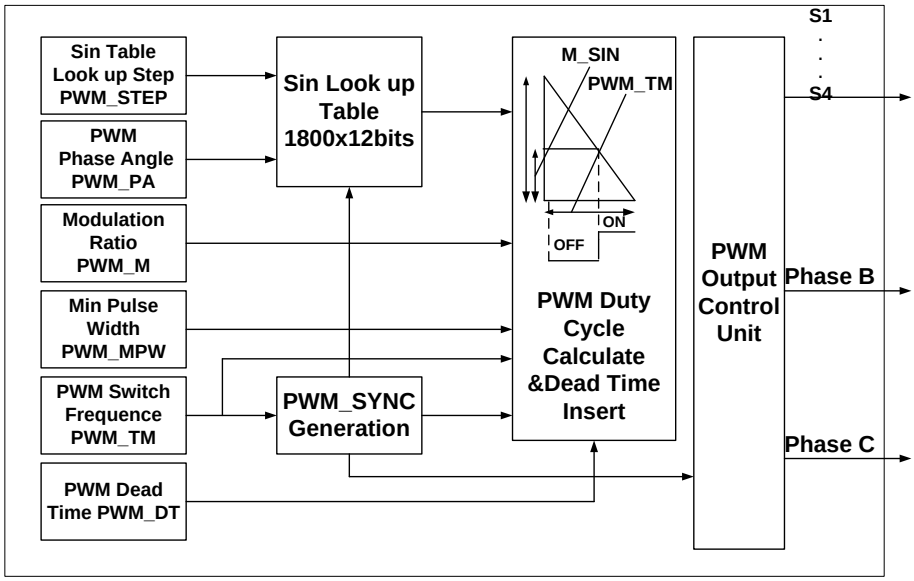

Fig. 26. Block diagram of digital SPWM generatiom unit.

In this pattern the switching frequency of the PWM is directly commanded from the PWM_TM module which value is directly determined from the desired switch frequency, f_{pwm} and the FPGA clock rate, f_{clk} ,

$$\text{PWM\_TM} = \frac{\text{f}_{\text{clk}}}{2 \times \text{f}_{\text{PWM}}} \tag{21}$$

In the FPGA program there is a specific PWM timer clocked at the FPGA clock rate. During every half cycle the PWM timer decrements from PWM_TM to 0. At the vertex time and the nadir time of the triangular carrier wave the value of PWM timer is zero. At these points, the PWM_SYNC pulse is generated. The PWM duty cycle calculation and PWM output control will be achieved at the rising edge of the PWM_SYNC signal.

In this system, the look-up table has been used. The table is stored in the embedded ROM block of the FPGA device. The ROM configurations are as follows: 1) ROM address depth is 1800, 2) ROM data width is 12 bits, 3) Look-up range is 0º~90º, 4) Look-up step is 0.05º. The FPGA program samples the sine-wave both at the vertex and the nadir time of the triangular wave. The increasing address value Δsin_address of the sine look-up table can be expressed as:

$$\text{sin\_address} = \text{sin\_address} + \Delta\text{sin\_address} \tag{22}$$

where $\Delta sin\_address$ = 180.

CHAPTER 4

4. Architecture and Implementation

In this Section, the architecture of the proposed SPWM generator algorithm, which is mapped on reconfigurable logic, is presented. The description of the modified architectures also follows. All the designs were fully implemented on a Virtex 5 Xilinx FPGA device. The Xilinx ISE Design Suite 10.1 tool was used for the design of the reconfigurable architectures.

4.1 The proposed architecture of the SPWM generator

The architecture of the proposed SPWM generation unit is presented in Fig. 27. It consists of five main subsystems that implement the SPWM algorithm. The input of the system is the modulation index in single precision floating point arithmetic, while the system architecture is based on 8-bit fixed-point arithmetic. The following equations have been derived under the assumption that the sine-wave [-1, 1] in this fixed point architecture is represented by the equivalent range [1, 255] with the zero point corresponding to the discrete value 128.

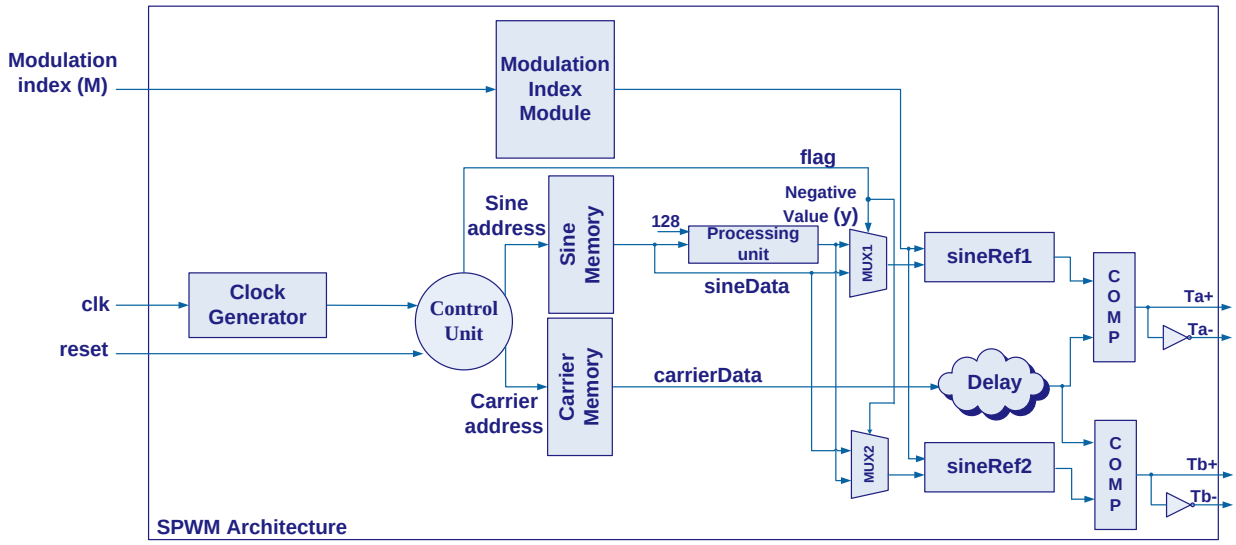

Fig. 27. The proposed SPWM generation unit architecture.

4.1.1 Clock generator subsystem

The first subsystem, the clock generator, takes as input the FPGA's clock and produces a new one that allows the whole system to operate in the desired switching frequency. This clock generator consists of a Digital Clock Manager (DCM) and a two-state Finite State Machine (FSM). In order this module to be flexible in many different operating switching frequencies, the FSM is used to set the initial system's frequency, f_{clk}, to $f_{clk}/2$ and the DCM plays the role of exactly adapting the external clock to the desired switching frequency by either increasing, or decreasing the corresponding FPGA clock frequency. By keeping the FSM for every different switching frequency constant and changing the DCM CLKFX_MULTIPLY and CLKFX_DIVIDE parameters respectively, the SPWM generator can produce the desired switching waveform output. As an example, a VHDL code of this module is quoted:

```
clkgen: DCM

Generic Map (
              CLKFX_MULTIPLY => 2,
              CLKFX_DIVIDE    => 1
)

PORT MAP (
            clkin => clk,
            clkfb =>sysclkfb,
            rst    =>'0',
            clk0  => sysclk,
            clkfx =>sysclkx2
);

buf : BUFG port map (
                      I  =>sysclk,
                      O =>sysclkfb
);

FSM_label:  FSM port map (
                           clk      => sysclkx2,
                           output => new_clock
);
```

4.1.2 Modulation index subsystem

The second subsystem, as shown in Fig. 28, takes as input the modulation index, which ranges from 0 to 1. As mentioned above, this value has to be converted to fixed-point arithmetic. Assuming there is an n-bit wide architecture, the equation to convert a floating point value to a given fixed-point architecture is the following:

$$y = M \times (2^{n-1} - 1) + 2^{n-1} \tag{23}$$

where *M* is the modulation index and *n* is the digital word length (*n*=8 in the proposed architecture). This conversion is achieved by multiplying the modulation index floating point input value with 127 and adding 128, respectively. The floating point value produced is then converted into a fixed value ranging from 0 to 255, via a float-to-fixed point conversion unit and outputs the index variable.

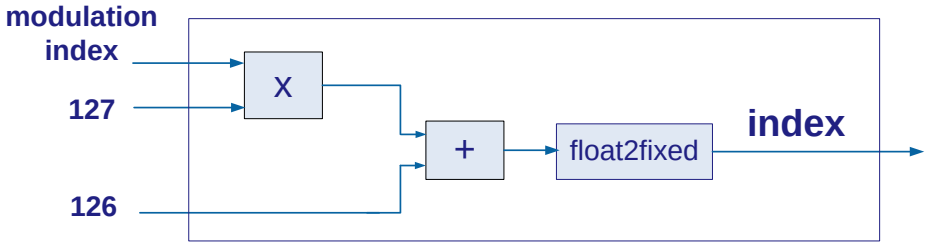

Fig. 28. Modulation index subsystem.

4.1.3 Sine-Carrier subsystem

The third subsystem, illustrated in Fig. 29, consists of the control unit, two BRAMs, which contain the sinusoidal and the triangular values, respectively and two multiplexers which produce the two reference sine-waves either on a positive, or a negative cycle.

In order to minimize the FPGA resource utilization, the memories were organized as follows; both the sinusoidal and the triangular pulses were sampled and quantized using MATLAB tools with the same sampling frequency, f_s (4 MHz, 8 MHz, 16 MHz, 32 MHz, 64 MHz), in order to

produce the discrete values used for the BRAMs initialization over the corresponding sampling period. The sinusoidal memory contains the values of the first quarter of the sine-wave period [0, $\pi/2$). The values of the sine-wave in the other three quarters are calculated by mirroring and inverting the values of the first quarter. The carrier memory contains the values of one period of the triangular wave. In this way, both the sine-wave and the carrier BRAMs operate as lookup tables (LUTs).

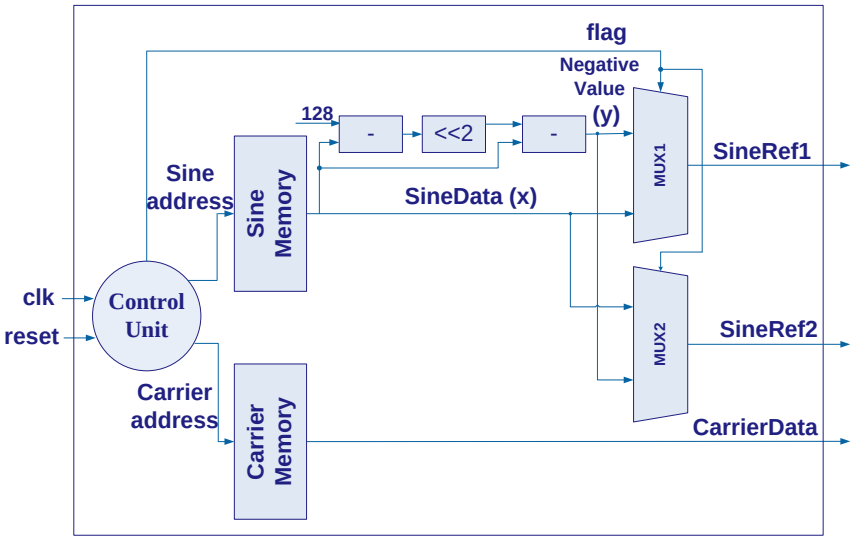

Fig. 29. Sine-Carrier subsystem.

Consecutive addresses of both memories ("Sine address" and "Carrier address", respectively, in Fig. 29) are generated in every clock cycle through the control unit. The control unit also produces a flag signal, which is responsible for the retrieval of the sine-wave values on a negative cycle. The sinusoidal-wave memory is scanned up and down four times, since this memory contains only the first quarter of a sinusoidal period, as described above. Memory up/down counting determines the value of the flag signal. Fig. 30 describes the FSM that, taking into consideration all the possible conditional statements, generates the correct addresses for both the sinusoidal and the carrier memory. The first state of this FSM (state 0) contains all the different possible cases that may occur to the memory address pointers and these are listed as a pseudocode in Fig. 31 and correspond to the numbered conditions of the FSM.

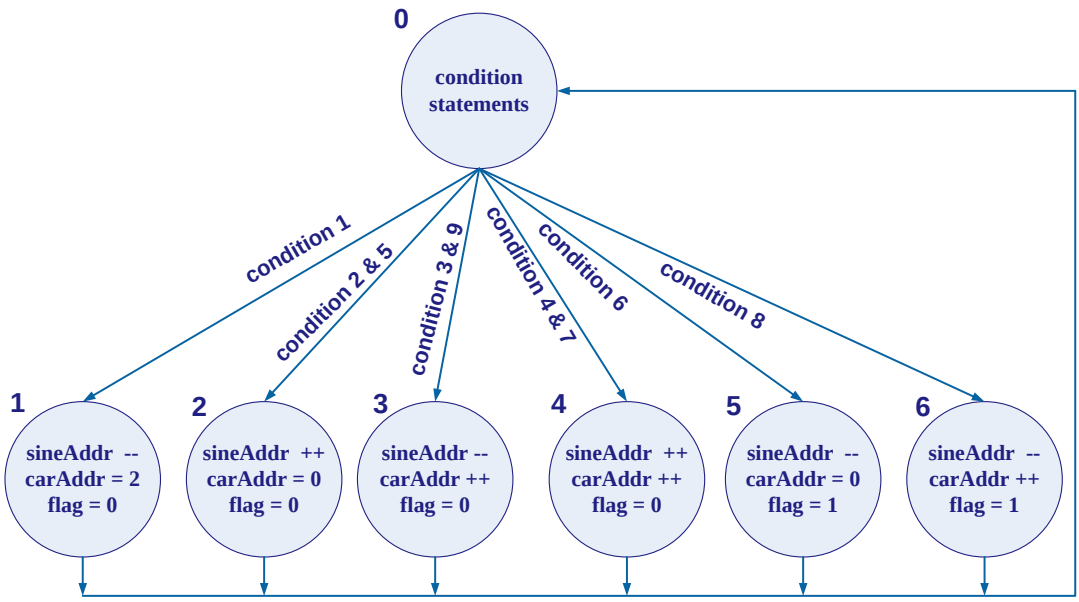

Fig. 30. SPWM control unit

```
1: if carAddr = end && sineAddr = end
       goto 1
2: elsif  carAddr = end && sineAddr != end
       goto 2
3: elsif  carAddr != end && sineAddr = end
       goto 3
4: elsif  carAddr != end && sineAddr != end
       goto 4
5: elsif  carAddr = end && sineAddr = start
       goto 2
6: elsif  carAddr = end && sineAddr = 1
       goto 5
7: elsif carAddr != end && sineAddr = start
       goto 4
8: elsif carAddr = !end && sineAddr = 1
       goto 6
9: else
       goto  3
```

Fig. 31. Pseudocode of the conditional statements.

While flag is set to 0, the multiplexer outputs the data read from the sinusoidal memory ("SineData" in Fig. 29). Otherwise, the multiplexer outputs the sinusoidal values on the negative

cycle that correspond to the values read from the memory after processing ["Negative Value (y)" in Fig. 29]. The conversion of the positive values stored in the sinusoidal memory to the corresponding negative values is performed according to the following equation:

$$y = x - [(x - 2^{n-1}) \times 2] \tag{24}$$

where *x* is the positive value stored and *n* is the digital word length (*n*=8 in the proposed architecture).

The second multiplexer is used for the production of the second reference sine-wave operating exactly on the opposite mode from the one analyzed above. Consequently, this subsystem outputs the two reference sinusoidal and triangular values ("SineRef1", "SineRef2" and "CarrierData", in Fig.29), respectively, synchronized in every clock cycle over a sinusoidal sampling period.

4.1.4 Adjustable amplitude sinusoidal subsystem

The adjustable amplitude sine subsystem, presented in Fig. 32, takes as input the reference sinusoidal values ["SineRef (y)", in Fig. 32] produced by the subsystems described above and generates a sinusoidal digital signal ["sineAdjustable (x)" in Fig. 32], with amplitude adjustable according to the modulation index value, which is also input of this subsystem. The adjustable-amplitude, sine-wave digital signal, which is 8-bit wide and takes values in the range 0-255, follows the equation:

$$x = \frac{(y - 2^{n-1}) \times (index - 2^{n-1})}{(2^{n-1} - 1)} + 2^{n-1} \tag{25}$$

where *y* is the reference sine-wave value and *index* is the output of the Modulation Index Subsystem presented in paragraph 4.1.2. The "f2fl" block in Fig. 32 is used to perform a fixed-to-floating point conversion, while the "fl2f" block performs the reverse operation.

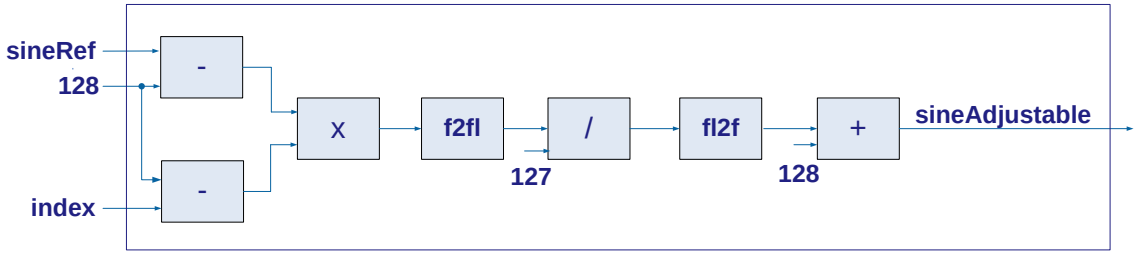

Fig. 32. Adjustable amplitude sinusoidal subsystem.

4.1.5 Comparison subsystem

The comparison subsystems (COMP in Fig. 27) implement the comparison between the high-frequency, constant-amplitude triangular wave (carrier) with the two low-frequency reference sine-waves of adjustable amplitude, using a simple comparator. The control signals T_{a+} and T_{b+} of the DC/AC inverter power switches depicted in Fig. 1, comprising the SPWM pattern, are generated from the outputs of the corresponding comparators (Fig. 27). The output of each comparator is equal to one when the output of the corresponding adjustable amplitude sine subsystem (Fig. 18) is equal to or greater than the digital value of the carrier signal. Moreover, the inverted SPWM pulses are generated in order control the DC/AC inverter power switches T_{a-} and T_{b-} (Fig. 1).

4.2 Differentiations on the past-proposed architectures

This Section highlights the main differentiations made on the original architectures (as described in Section 3) in order to produce a unipolar sinusoidal pulse width modulation for a single-phase inverter at the maximum possible switching frequency that every previously proposed implementation can operate on. At this point it should be noted that all other architectures were implemented as close as possible in the way suggested by the respective paper. Moreover, some additional changes were made so as to operate at switching frequencies higher than the proposed ones and close to those that the target board can offer.

4.2.1 Sampling at nadir time instants

This sampling technique is implemented by the architecture analyzed in Section 3.1. It was mentioned that the sine-wave is produced by a quarter of a cycle and the sine memory contains discrete values ranging in the interval [1, 25] as it holds the 25% of the representations of the total required data. In order to produce a unipolar SPWM wave and keep the same range of values in the sine memory, this scaling had to be converted according to the following equation:

$$y = 128 + [(x - 13) \times index] \tag{26}$$

where *x* is the initial sine value, *y* is the new sine value, converted from range [1-25] to range [0-255] and *index* is the integer value of the modulation index ranging from 1 to 10. Fig. 33 shows the respective block diagram.

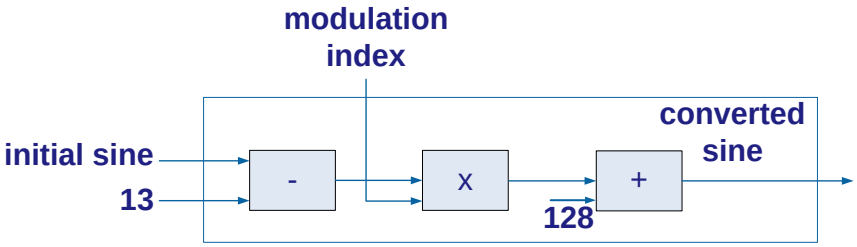

Fig. 33. Sine conversion subsystem.

After this conversion, another one has to be done. This is the conversion to the corresponding negative values of the sine-wave according to the following equation.

$$y = x - [(x - 128) \times 2] \tag{27}$$

where *x* is the converted sine value resulting from the previous subsystem and *y* is the corresponding negative sine value. The multiplication can be achieved by a left. Fig. 34 depicts the corresponding block diagram.

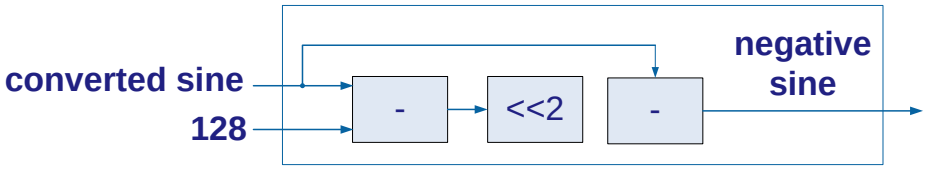

Fig. 34. Negative sine subsystem.

The positive quarter sine memory now contains discrete values in the range [13, 25] while the values [1, 12] correspond to the quarter time period of the second negative reference sine-wave. The block diagram of this architecture is illustrated in Fig. 35. The conversion of the initial sine memory values to the new ones, multiplied by the integer modulation index [1, 10], and to the corresponding negative values, are indicated by the brown and the green bracket, respectively. The clock generator module operates in exactly the same way as the one described in the Section 4.1.1.

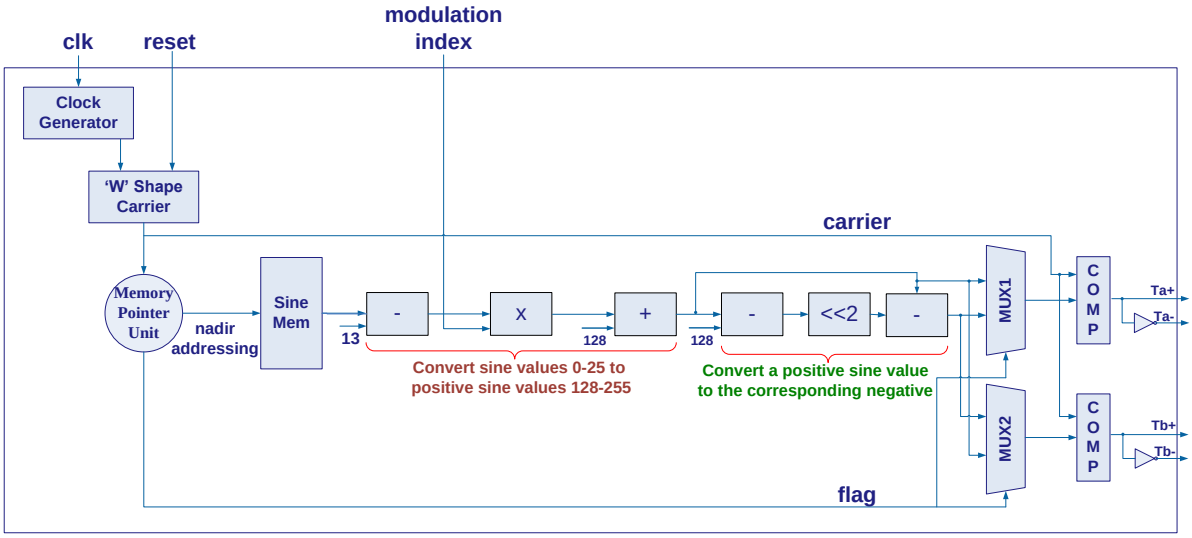

Fig. 35. Nadir sampling architecture.

The control unit generates a new sine address at every zero point of the triangular wave as it can be seen in Fig. 36. It is implemented by a two-state FSM which counts 510 clock cycles and then increases the memory address pointer. If this pointer reaches the final address of the sine

memory, it starts decreasing as the sine memory contains the sine values for a quarter of a sine period. After every up/down memory scanning, a flag signal is produced to indicate the negative cycle of the sine period. This flag is used as a control signal by the multiplexers, which operate in reverse way and generate the correct sine values for both the reference sine-waves.

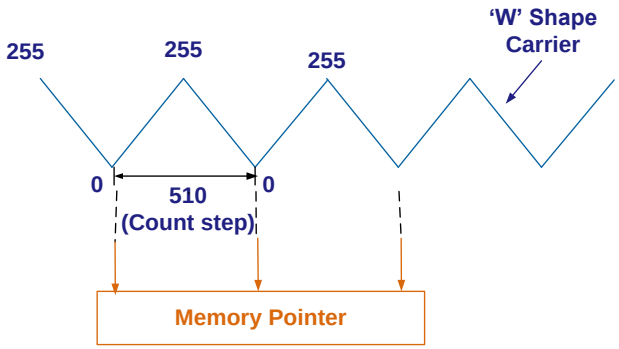

Fig. 36. Sampling at nadir time instants.

4.2.2 Sampling at peak, peak/nadir and N-samples time instants

The architecture of generating the SPWM when the sinusoidal wave is sampled at the time instants corresponding to peak, both at the nadirs and the peaks and to N-samples of the carrier wave follows the idea presented in the Section 3.2, where the sine table is designed as a look-up table which contains the sine values for 180° of the sine-wave. The modulation index keeps floating point values in the range [0, 1]. The differently colored modules in Fig. 37, "Modulation Index Module", "Processing Unit", "SineRef1" and " SineRef2" implement the equations (21), (22) and (23), presented in the Section 4.1. Thus, a unipolar SPWM is produced and all the calculated values (positive sine, negative sine and sine multiplied with the modulation index) are normalized in the range of the 8-bit fixed-point arithmetic architecture (i.e. 0-255). Fig. 37 shows the block diagram of this architecture.

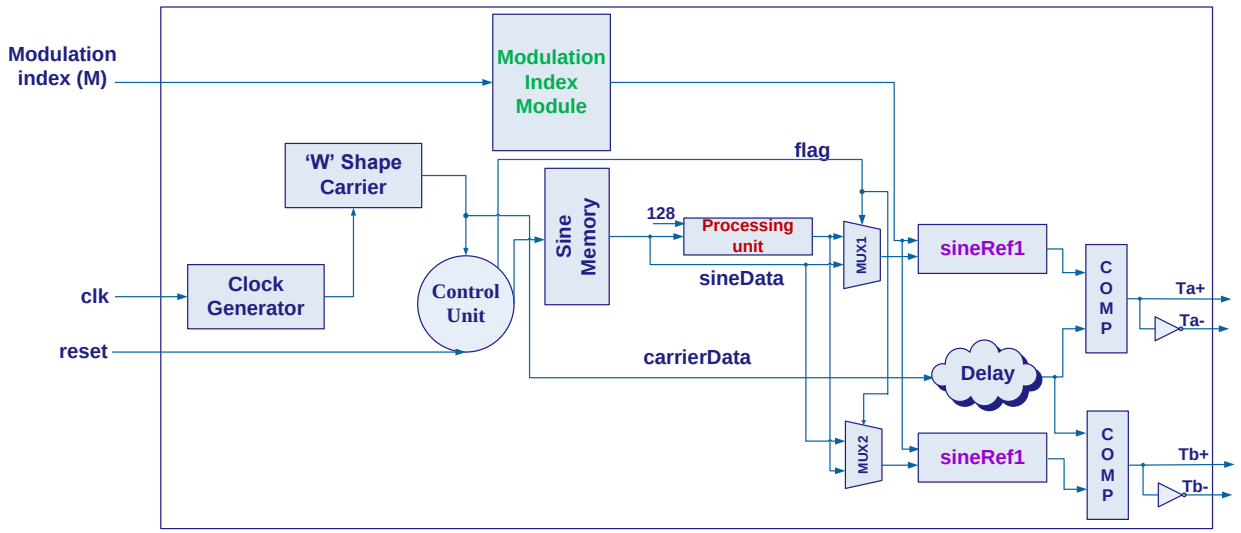

Fig. 37. The peak, peak/nadir and N-sampling architectures.

The main differences between these three techniques, implemented using the same architecture, have to do with the way the sinusoidal memory is sampled. Figs. 38-40, depict the respective time instants that the control unit generates a new address to the sine LUT. This control unit is a two-state FSM producing a counter that actually 'follows' the carrier wave. When the counter equals to the corresponding time instance (peak, peak/nadir or NT/2 of the carrier wave), the memory address pointer is increased by one.

The sine memory of this architecture contains values of the half-sine period. Once scanned, the memory pointer starts decreasing in order to retrieve the negative values of the other half-sine period and the flag signal gets the opposite value (0 to 1 or 1 to 0, respectively).

Another difference among these sampling techniques is the number of sine values in the sine memory. For the same switching frequency, when sampling at both the peaks and the nadirs of the carrier wave the resulting values are double than those obtained when sampling only at the peaks of the triangular wave, since in the first case there are two samples over a triangular period while in the second case there is only one. When the sampling is realized every *N-samples*, the number of different sine values, as well as the sampling time instants, depends either on the switching frequency, or the number *N* which corresponds to less than one sample per carrier cycle.

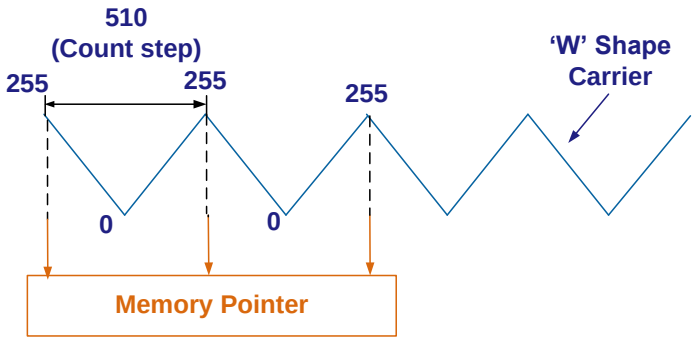

Fig. 38. Sampling at peak time instants.

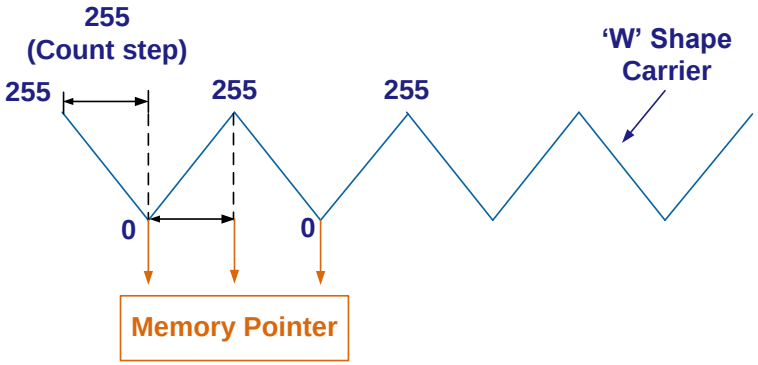

Fig. 39. Sampling at peak/nadr time instants.

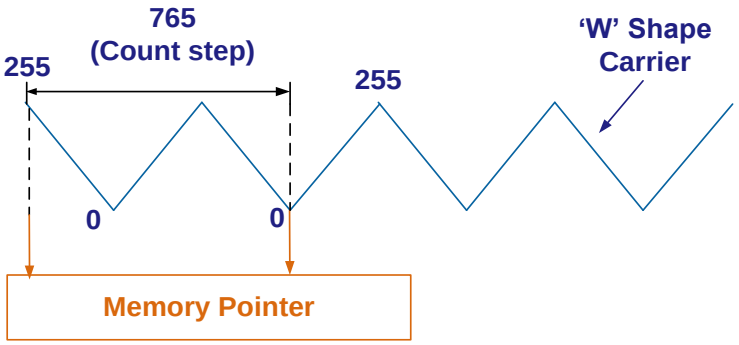

Fig. 40. Sampling at NxT/2 time instants.

4.2.3 Sampling at peak/nadir time instants and triangles similarity

The basic idea of this sampling approach was described in Section 3.4. In order to generate a unipolar SPWM for a full-bridge single-phase inverter, the architecture proposed by L. Jian et al. was converted in a way to produce the desired SPWM wave. The general block diagram of this architecture is presented in Fig. 41.

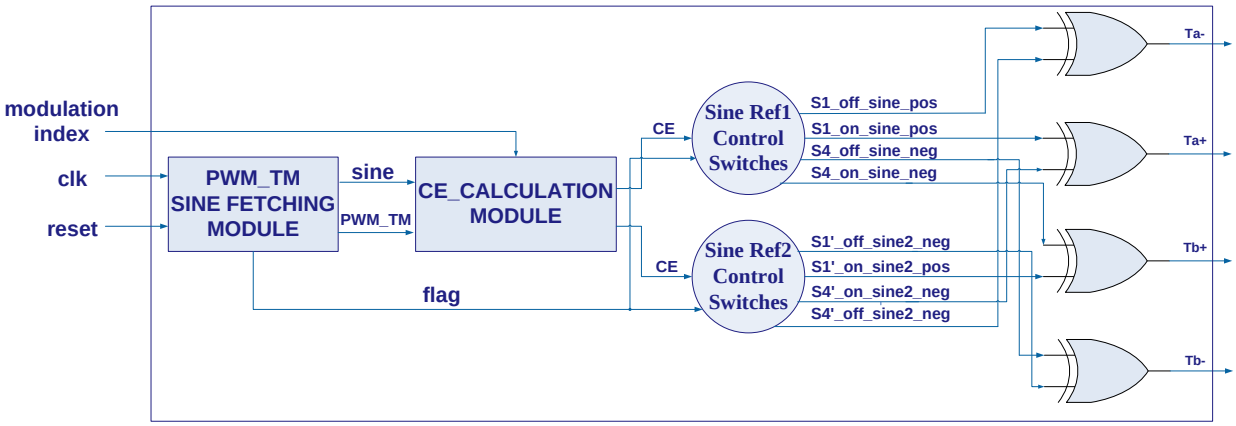

Fig. 41. Genaral block diagram of triangles similarity architecture.

The first module, shown in Fig. 42, is responsible for the data fetching according to the authors' suggested configuration. The look-up step is 0.05º within the range 0º-90º while the sine values are expanded 2^{12} times. Every sampled sine value deviates from the previous one by 9º. Hence, the memory should be accessed by a new address every 180 (= 9º/0.05º) memory locations. This new address must be synchronized with PWM_TM value, which was mentioned to be the desired switching frequency given by eq. (21).

The PWM_TM is implemented as a simple counter and when it reaches its maximum value that defines the desired switching frequency, the PWM_SYNC pulse is generated. PWM_TM's value depends on both the switching frequency and the system clock frequency. It plays the same role as that played by the clock generator in the rest architectures. The new sine-data fetching is performed at the rising edge of the PWM_SYNC signal. This module also outputs a flag signal which determines the positive or negative, respectively, sine period.

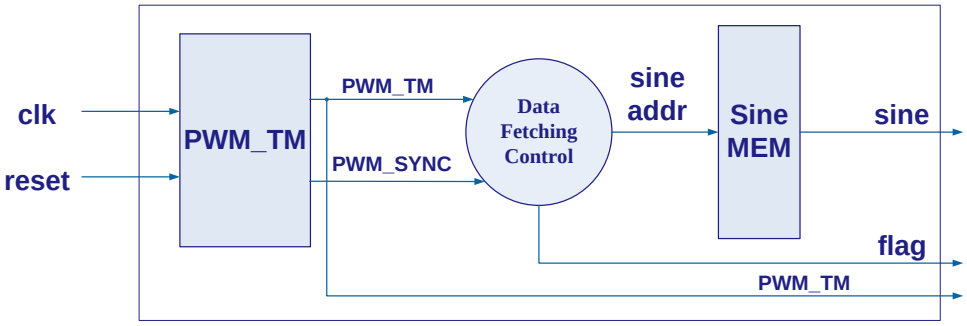

Fig. 42. Sine data module.

The module which is responsible for the CE calculation is shown in Fig. 43 and it implements the eq. (16).

The modulation index is in the same range (i.e. 0-1) as in the other architectures presented. For this reason, the sine data, as well as the PWM_TM value, have to be converted accordingly via a fixed2float unit. After the multiplications, the final result has to be divided with the number 4096 in order to be right-shifted 12 positions, since the initial sine-values are expanded by 2^{12} times. As was previously described in this thesis, the CE parameter defines the ON and OFF duration of the inverter switches that form the SPWM pattern. So, it is also converted to an integer value via a float2fixed unit.

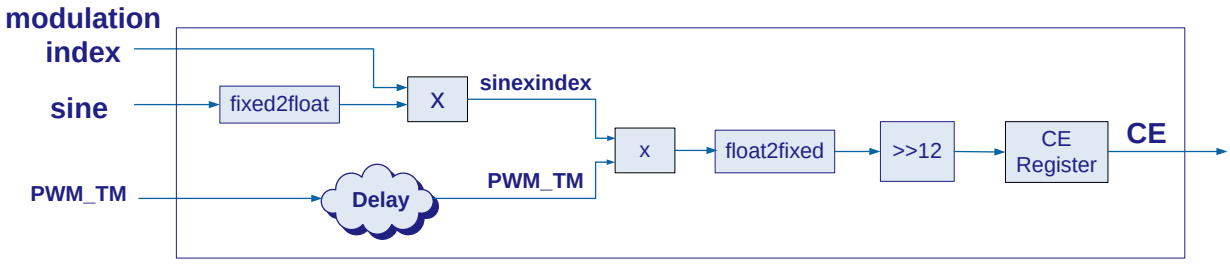

Fig. 43. CE calculation module.

The equations determining high or zero level of the switches were presented in Section 3.4. These equations are based on the similarity of the triangles that are formed. Here is another difference of

this architecture compared to the previously described ones: the control signals hold their duty cycle values during the complete sinusoidal period.

In this architecture, when the reference sinusoidal wave is greater than zero, S1_ON gives the ON duration with duty cycle equal to the CE that was computed previously. The S4_ON in this case holds the zero level. When the reference sinusoidal wave is less than zero, S4_ON holds the ON duration, while the S1_ON holds the zero level. The control signals S1_OFF and S4_OFF operate in the opposite mode. For the second reference sine-wave, the control signals operate in the opposite way than the first sine-wave. The S1_ON signal becomes S4'_ON and so on. Fig. 44 illustrates this operation either on the positive sinusoidal period (flag = 0), or on the negative sinusoidal period (flag = 1).

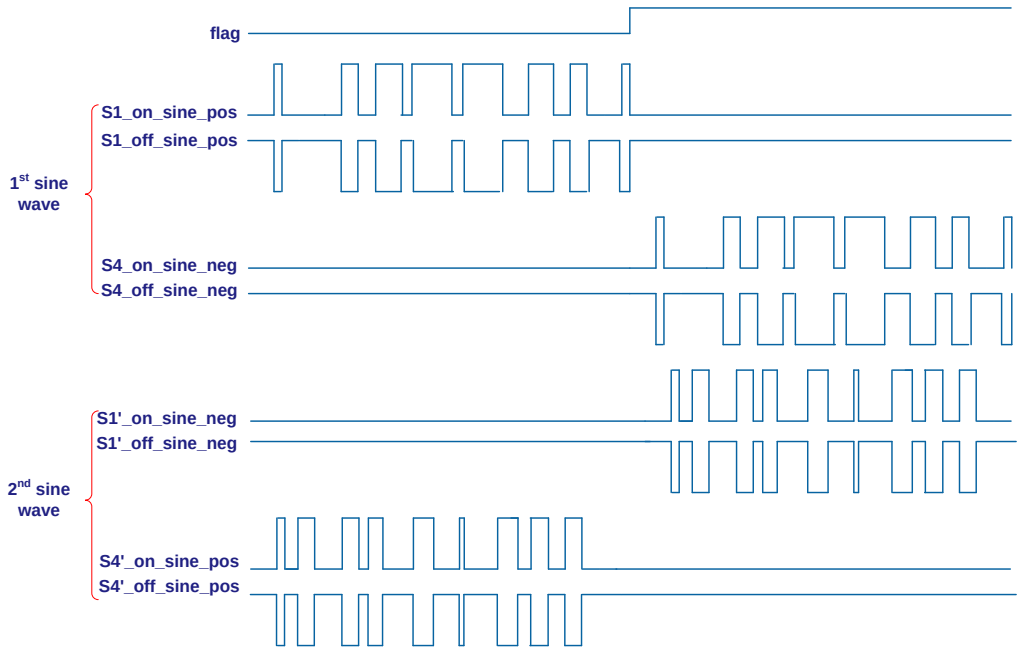

Fig. 44. Switch operation for a sinusoidal period.

The last modules of this architecture are the control units, which are responsible for the switches ON/OFF state; these units implement two FSMs that generate the ON/OFF pulses proportionally to the pre-computed CE value. The first control unit operates for the first sine reference wave, while the other for the reverse sine-wave. The period of the pulse is given by the PWM_TM

value. During this period the two FSMs adjust the switches ON-state to be equal to the CE parameter, whilst the rest are set OFF. These pulses are finally cross – XOR, as shown in Fig. 45, in order to produce a unipolar SPWM generator. The control units implement the following equations for the first sine reference wave:

$$S1\_ON = CE \tag{28}$$

$$S1\_OFF = PWM\_TM - CE \tag{29}$$

$$S4\_ON = 0 \tag{30}$$

$$S4\_OFF = 1 \tag{31}$$

For the second sine reference wave, the following equations are implemented:

$$S4'\_ON = CE \tag{32}$$

$$S4'\_OFF = PWM\_TM - CE \tag{33}$$

$$S1'\_ON = 0 \tag{34}$$

$$S1'\_OFF = 1 \tag{35}$$

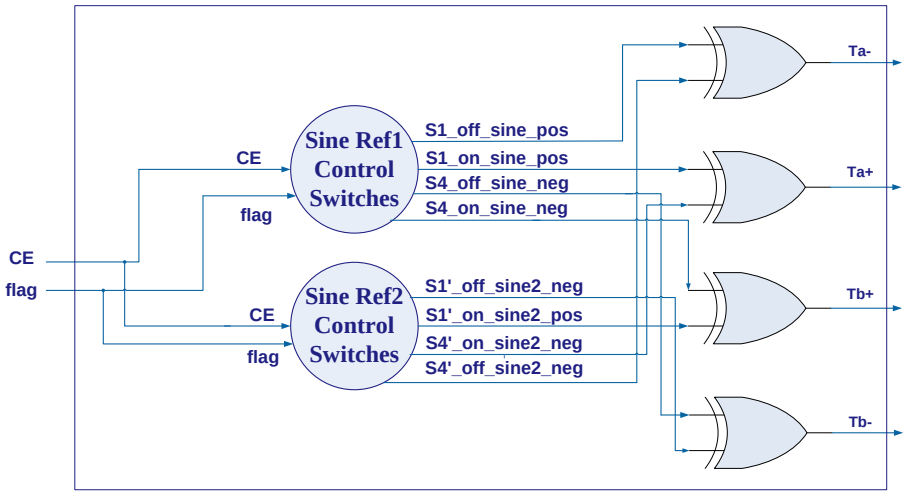

Fig. 45. Control units for the unipolar SPWM generator.

CHAPTER 5

5. Validation and Performance Evaluation

In this Section, the performance of the implemented SPWM generation system is presented. The proposed system performance has been evaluated on the actual design, which has been fully implemented and downloaded to an FPGA board. The system was evaluated based on four major metrics: sampling frequency, switching frequency, modulation index and power consumption both with simulation and experimental results. Several tests took places in order to assure the correct operation of the new SPWM generator and its capacity to operate over a wide range of switching frequencies (1kHz-1MHz) and modulation index values (0-1). All possible combinations of the previously mentioned metrics were taken into consideration during testing designs. Oscilloscope results as well as Fast Fourier Transform (FFT) of the generated signal verify the successful implementation of the SPWM generator. The FPGA resources utilized by this design are also presented analytically in this Section.

5.1 System validation by simulation

The architecture presented in the previous Section has been synthesized using the VHDL language and its correct operation has been verified using the ModelSim 6.3f simulator. The major internal signals of the proposed system and the SPWM outputs in case that f_c = 1 kHz, f_s = 4 MHz and modulation index (M) = 0.5 are plotted in Fig. 46. A low carrier frequency has been used in this example only for demonstration purposes, since it enables the easy discrimination of all SPWM pulses produced within a period of the reference sine-wave and the observation of their width. As analyzed in Section 2, the SPWM output is generated at the intersection of the sinusoidal and triangular waveforms at certain sampling instants. When the value of each sine-wave is higher than the triangular wave value, the output pulse is set to logical “1”, else it is set to logical “0”.

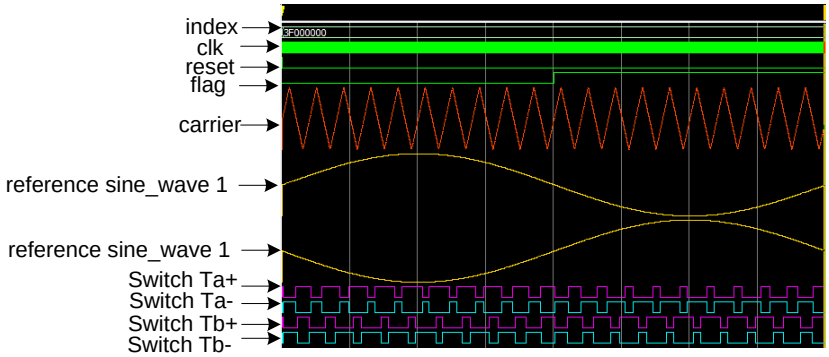

Fig. 46. The major internal signals of the proposed system and the SPWM outputs in case that f_c = 1 kHz, f_s = 4 MHz and M = 0.5.

5.2 Oscilloscope results

The oscilloscope measurement of the SPWM waveform which is generated in case that the implemented SPWM design is downloaded in the XC5VLX110T FPGA board, for f_c = 500 Hz, f_s = 4 MHz and M = 0.9 is illustrated in Fig. 47. This waveform emulates the V_{spwm} signal depicted in Fig. 1 and it is produced by subtracting the T_{a+} and T_{b+} control signals generated by the proposed system. As it can be observed the frequency of the SPWM waveform corresponds to the 50Hz basic sinusoidal frequency. Fig. 48 shows zoom-in view of the SPWM signal such that the individual pulses are displayed and that is the reason that a so low switching frequency is demonstrated in this case. For this case of switching frequency and the sinusoidal frequency equal to 50Hz, the number of the resulting pulses is equal to 500Hz/50Hz = 10 and in case of unipolar SPWM this number should appear in the half period of the SPWM signal, something that is confirmed in Fig. 48.

Fig. 47. Oscilloscope measurement of the SPWM waveform for f_c = 500 Hz, f_s = 4 MHz and M = 0.9.

Fig. 48. Zoom-in oscilloscope measurement of the SPWM waveform for f_c = 500 Hz, f_s = 4 MHz and M = 0.9.

In order to investigate the harmonic content of the SPWM signal, the SPWM waveform needs to be converted to the frequency domain using the Fast Fourier Transform (FFT). As shown in Fig. 49, the unipolar PWM scheme has the advantage of "effectively" doubling the switching frequency as far as the harmonics are concerned. The advantage of "effectively" doubling the switching frequency appears in the harmonic spectrum of the output voltage waveform, where the harmonics appear as sidebands at multiplies of twice the switching frequency. Fig. 49 shows that with switching frequency f_c = 500 Hz the lowest order harmonics appear at double the switching frequency (i.e. 1 kHz).

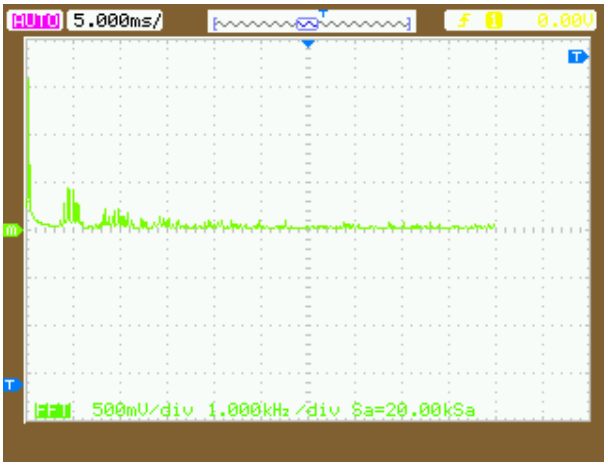

Fig. 49. The FFT of the SPWM signal presented in Figs. 47 & 48.

Figs. 50-52 refer to M = 0.9 and M = 0.1, respectively and show the different pattern of FFT generated by modifying the modulation index. The modulation index also determines the duty cycle of every single pulse of the generated SPWM signal.

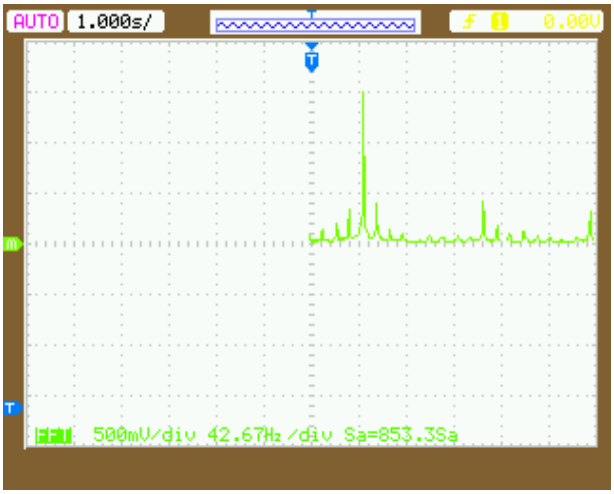

Fig. 50. FFT of the SPWM signal in case that M = 0.9 and f_c = 500 Hz.

Fig. 51. FFT of the SPWM signal in case that M = 0.1 and f_c = 500 Hz.

Fig. 52. SPWM for M = 0.1 and f_c = 500 Hz.

The generated control signal T_{a+} (T_{b+} is similarly produced) for f_c = 1 kHz and M = 0.5 is illustrated in Fig. 53. It is observed that the frequency of every single pulse is equal to the switching frequency. Fig. 54 depicts the FFT of the SPWM wave in case that f_c = 1 kHz and M = 0.5. The first band of harmonics is positioned at twice the switching frequency (i.e. 2 kHz).

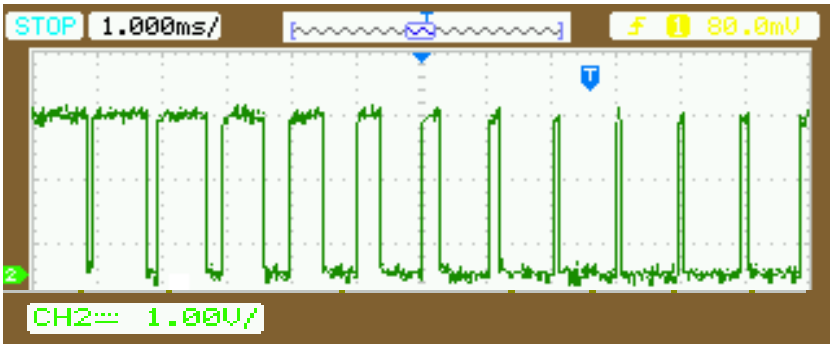

Fig. 53. The control signal T_{a+} (T_{b+} is produced similarly) in case that f_c = 1 kHz and M = 0.5.

Fig. 54. The FFT of the SPWM signal in case that M = 0.5 and f_c = 1 kHz.

Similarly, Figs. 55-57 show the oscilloscope measurement of the FFT patterns, for f_c = 10 kHz, 100 kHz, 1 MHz and M = 0.5, respectively, confirming the correct operation of the proposed SPWM generator at high switching frequencies. The sampling frequency is kept constant at 4 MHz.

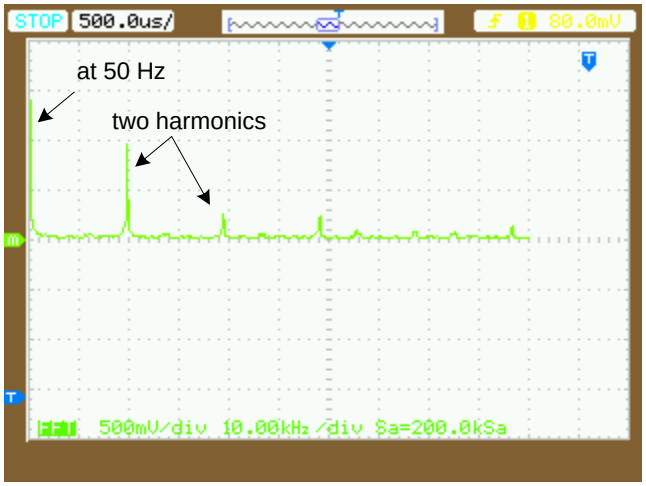

Fig. 55. FFT pattern in case that M = 0.5 and f_c = 10 kHz.

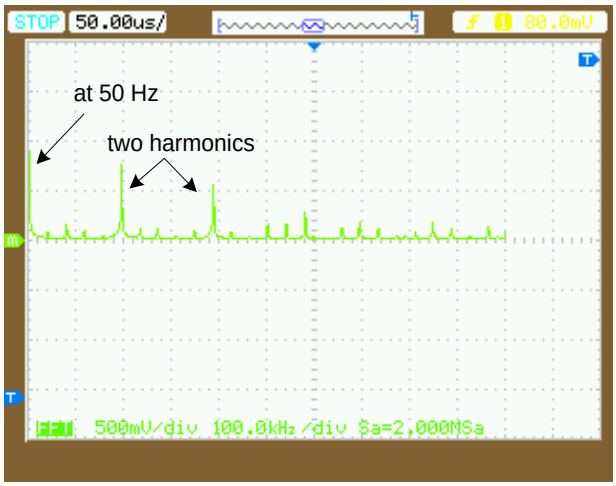

Fig. 56. FFT pattern in case that M = 0.5 and f_c = 100 kHz.

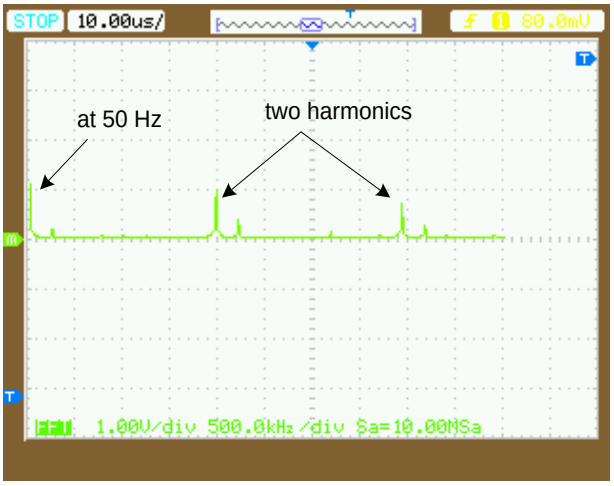

Fig. 57. FFT pattern in case that M = 0.5 and f_c = 1 MHz.

At this point, the method that each one of the different switching frequences could be achieved with respect to the system clock frequncy will be analyzed. As described in Section 4, every architecture has a clock generator module, consisting of a DCM and a two-state FSM which in the first state counts the corresponding system clock cycles and produces the positive edge of the desired switching cycle and in the second state does the same to produce the negative edge. The DCM plays the role of adjusting the system clock frequncy to the desired switching frequency. For low swiching frequncies the DCM module was not necessary as only the FSM could generate the desired switching frequency.

As far as the high switching frequency is concerned, (e.g. f_c = 1 MHz) by varying the sampling frequncy (e.g. f_s = 4 MHz, 16 MHz, 32 MHz, 64 MHz), the FSM decreases to half the system clock frequency and the DCM parameters change according to the desired switching frequency, thus producing a simplified clock generator for sampling frequencies gretater than 4 MHz. The measurements of all clock periods in case of switching frequency 1 MHz are quoted below:

- **f_c = 1 MHz, f_s = 4 MHz, f_{clock} = 149 MHz** => 12 clock cycles for positive edge of the desired clock cycle and 12 clock cycles for the negative one and DCM = 2/2. The DCM does not offer any essential impact to the new clock period and the system clock frequency has to be approximately decreased to the samling frequncy, since the former is the maximum achieved clock frequncy of the target FPGA and the later determines the memory accessing for the real system.

- **f_c = 1 MHz, f_s = 16 MHz, f_{clock} = 131 MHz** => the FSM decreases to half the system clock frequncy and the DCM parameters are 2/6, respectively.

- **f_c = 1 MHz, f_s = 32 MHz, f_{clock} = 105 MHz** => the FSM decreases to half the system clock frequncy and the DCM parameters are 5/8, respectively.

- **f_c = 1 MHz, f_s = 64 MHz, f_{clock} = 96 MHz** => the FSM decreases to half the system clock frequncy and the DCM parameters are 4/3, respectively.

The control signals T_{a+} and T_{b+} are connected via a User Constraints File (UCF) to the FPGA's output pins in order to get the final SPWM signal through the oscilloscope. Considering that the output voltage of the FPGA pins is 2.5V, the theoretical root mean square voltage (V_{rms}) is calculated as follows:

$$y = \frac{(2.5 \times M)}{\sqrt{2}} \tag{36}$$

Figs. 58-60 depict the experimental output voltage for switching frequency f_c = 100 kHz and M = 0.1, 0.5 and 0.9, respectively. Figs. 61 shows the experimental and theoretical SPWM output voltage at 50 Hz for f_c = 10 kHz and M = 0.1 -1 with a 0.1 step. Figs 62-63 show the experimental graphs of the 50 Hz output voltage of the proposed SPWM generator and the corresponding theoretical output voltage for f_c = 100 kHz and 1 MHz and M = 0.1, 0.5 and 0.9, respectively.

The output voltage of the fundamental frequency (50 Hz), V_o, in case of f_c = 100 kHz, as it can also be observed in the following figures, is the following:

- M = 0.1: experimental V_o = 0.19 V vs. theoretical V_o = 0.18 V.
- M = 0.5: experimental V_o = 0.89 V vs. theoretical V_o = 0.88 V.
- M = 0.9: experimental V_o = 1.50 V vs. theoretical V_o = 1.59 V.

The deviation, d (%) of the output voltage is calculated as follows:

$$d = \left|[(\text{theoretical} - \text{exprerimental}) / \text{theoretical}]\right| \times 100 \qquad (37)$$

For the above measurements, the deviation of the experimental output voltage from the corresponding theoretical value is 5.6 %, 1.1% and 5.7%, respectively.

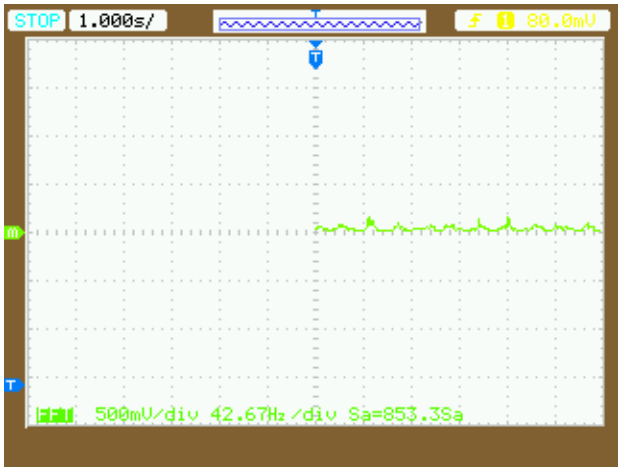

Fig. 58. FFT of the SPWM signal in case that M = 0.1 and f_c = 100 kHz.

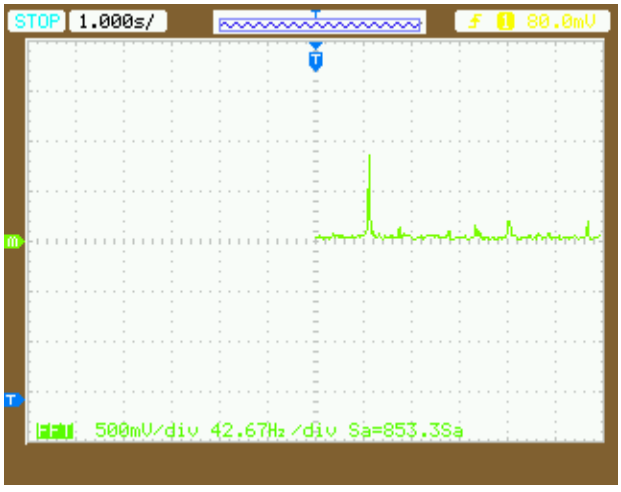

Fig. 59. FFT of the SPWM signal in case that M = 0.5 and f_c = 100 kHz.

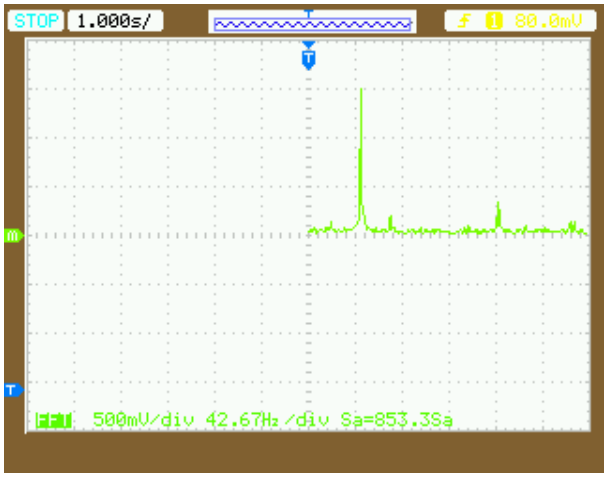

Fig. 60. FFT of the SPWM signal in case that M = 0.9 and f_c = 100 kHz.

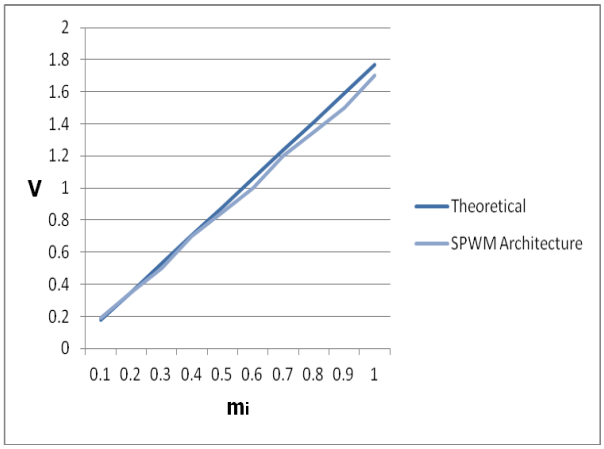

Fig.61. Experimental and theoretical output voltage at 50 Hz for M = 0.1-1 and f_c = 10 kHz (d ranges from 0-5.6%).

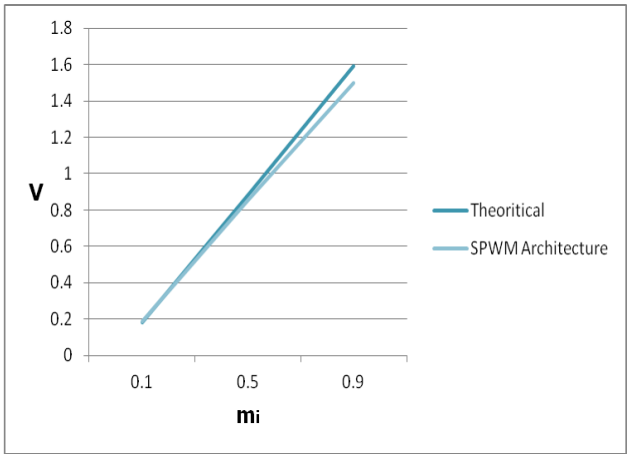

Fig.62. Experimental and theoretical output voltage at 50 Hz for M = 0.1, 0.5, 0.9 and f_c = 100 kHz (d = 5.6%, 1.1% and 5.6%, respectively).

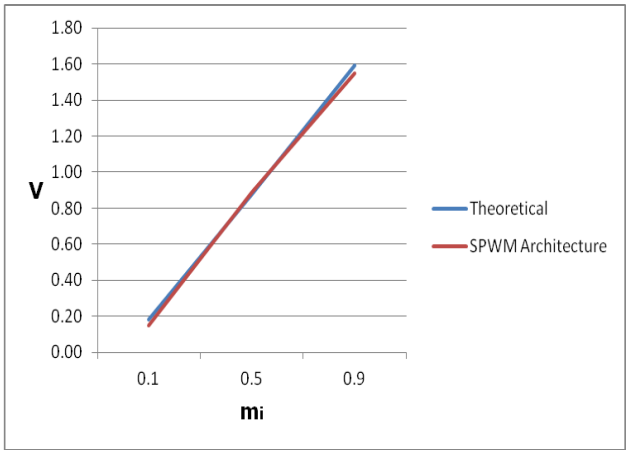

Fig. 63. Experimental and theoretical output voltage at 50 Hz for M = 0.1, 0.5, 0.9 and f_c = 1 MHz (d = 16.7%, 13.13% and 2.5%, respectively).

At this point, it is necessary to mention that the proposed architecture was moreover tested for switching frequencies greater than 1 MHz and these were 2 MHz and 4 MHz respectively. For switching frequency 2 MHz the proposed architecture operates properly as it can be seen in Fig. 64, where the FFT pattern for f_c = 2MHz and M = 0.5 is depicted. For f_c = 4MHz and M = 0.5 the system starts to limp (Fig. 65), something that is not necessarily an architectural disadvantage as the modern power electronic DC/AC converters do not require maximum operating switching frequency approximately greater than 1.5 MHz.

In these two last cases the corresponding switching frequencies were achieved as follows:

- **f_c = 2 MHz, f_s = 8 MHz, f_{clock} = 143 MHz** => 5 clock cycles for positive edge of the desired clock cycle and 12 clock cycles for the negative one and DCM = 25/26.
- **f_c = 2 MHz, f_s = 16 MHz, f_{clock} = 132 MHz** => FSM decreases to half the system clock frequency and DCM = 2/6.
- **f_c = 2 MHz, f_s = 32 MHz, f_{clock} = 119 MHz** => FSM decreases to half the system clock frequency and DCM = 2/3.
- **f_c = 2 MHz, f_s = 64 MHz, f_{clock} = 94 MHz** => FSM decreases to half the system clock frequency and DCM 4/3.

- **f_c = 4 MHz, f_s = 8 MHz, f_{clock} = 140 MHz** => 5 clock cycles for positive edge of the desired clock cycle and 12 clock cycles for the negative one and DCM = 25/26.

- **f_c = 4 MHz, f_s = 16 MHz, f_{clock} = 126 MHz** => FSM decreases to half the system clock frequncy and DCM = 2/6.

- **f_c = 4 MHz, f_s = 32 MHz, f_{clock} = 105 MHz =>** FSM decreases to half the system clock frequncy and DCM = 5/8.

The reason that for high switching frequncies (i.e. f_c > 1 MHz), the sampling frequency also increases is to obtain more samples in the carrier BRAM and to result in a more accurate calculation of the individual SPWM pulses widths, as the higher the number of samples, the more comparisons between the reference sinusoidal waves and the carrier will occur.

Fig. 64. FFT pattern in case that M = 0.5 and f_c = 2 MHz.

Fig. 65. FFT pattern in case that M = 0.5 and f_c = 4 MHz..

5.3 System resources

The proposed FPGA-based SPWM system was implemented on a Virtex-5 FPGA (XC5VLX110T). Several tests took place on the implemented system using different clock rates either on the carrier (1 kHz, 100 kHz, 500 kHz, 1 MHz), or the sampling frequency of the sine-wave values stored in the LUT (4 MHz, 8 MHz, 16 MHz, 32 MHz, 64 MHz), f_c and f_s respectively. Taking into consideration all possible combinations, all the designs were tested and their proper operation was confirmed.

A post place-and-route analysis of the implemented system has been performed using the XILINX ISE Design Suite 10.1 software. The resources required for the implementation of the full system are presented in Table 1 for all the possible combinations mentioned above; the last row in this table shows the corresponding maximum clock frequency. It is observed that the proposed design is capable to operate at switching frequency values up to 1 MHz, thus covering the requirements of modern power electronic DC/AC converters. Also, a low percentage of the FPGA device logic and memory blocks are occupied by the proposed SPWM generation architecture enabling the implementation of additional DC/AC inverter control algorithms in the same FPGA IC. Increasing the sampling frequency, f_s, results in a more accurate calculation of the individual SPWM pulses widths, but the LUT memory requirements are also increased. Thus, the Block RAMs are the critical resource that restricts further increase of the sampling frequency (e.g. to 128 MHz, 256 MHz etc.).

Table 1. FPGA resources and system frequency for various SPWM designs.

f_c/f_s	*1kHz/ 4MHz*	*1MHz/ 4MHz*	*500kHz / 4MHz*	*100kHz /4MHz*	*1MHz/ 16MHz*	*500kHz/ 16MHz*	*100kHz/ 16MHz*	*1MHz/ 64MHz*	*500kHz/ 64MHz*	*100kHz/ 64MHz*
DSPs	6 / 64 (9%)	6 / 64 (9%)	6 / 64 (9%)	6 / 64 (9%)	6 / 64 (9%)	6 / 64 (9%)	6 / 64 (9%)	6 /64 (9%)	6 / 64 (9%)	6 / 64 (9%)
Slice Registers	3447 / 69120 (4%)	3437 / 69120 (4%)	3438 / 69120 (4%)	3441 / 69120 (4%)	3441 / 69120 (4%)	3442 / 69120 (4%)	3445 / 69120 (4%)	3450 / 69120 (4%)	3451 / 69120 (4%)	3454 / 69120 (4%)
Slice LUTs	2860 / 69120 (4%)	2840 / 69120 (4%)	2838 / 69120 (4%)	2843 / 69120 (4%)	2846 / 69120 (4%)	2846 / 69120 (4%)	2852 / 69120 (4%)	2893 / 69120 (4%)	2893 / 69120 (4%)	2901 / 69120 (4%)
BRAMs	6 / 148 (4%)	6 / 148 (4%)	6 / 148 (4%)	6 / 148 (4%)	21 / 148 (14%)	21 / 148 (14%)	21 / 148 (14%)	79 / 148 (52%)	79 / 148 (52%)	79 / 148 (52%)
max clock frequ.	**158MHz**	**149MHz**	**144MHz**	**155MHz**	**131MHz**	**138MHz**	**126MHz**	**99MHz**	**97MHz**	**96MHz**

5.4 Power consumption

Quiescent power (also called static power) is the power drawn by the device when it is powered up, configured with user logic and there is no switching activity. In XPower Analyzer, the value reported for **Total Quiescent Power** is composed of these quiescent power components:

- **Device static power** – This represents power consumed by the device when it is powered up without programming the user logic. The main contributor to this number is the junction temperature. Any change affecting the device operating environment will affect this power.
- **Design static power** – This represents the power consumed by the user logic when the device is programmed and without any switching activity. For instance, depending on the device family and resource configuration, some blocks used in a design (such as clock management, I/Os and Multi-Gigabit Transceivers) will consume a set amount of power regardless of activity.

XPower Analyzer determines the device quiescent power based on environmental settings and the logic configuration in each design. The power consumed when there is switching activity (e.g the SPWM algorithm is running on the board) is dynamic power.

This Section quotes the power consumed by each SPWM design presented in the previous sections of this chapter, measured using XPower Analyzer. From Table 2 that is presented below, it is observed that the power consumption of the proposed design is less than one Watt (W), which is considered to be relatively low power consumption.

Table 2. FPGA Power Consumption for all possible SPWM designs in case of the XC5VLX110T FPGA board.

f_c/f_s	***10kHz/ 4MHz***	***100kHz/ 4MHz***	***1MHz/ 4MHz***	***1MHz/ 16MHz***	***1MHz/ 32MHz***	***1MHz/ 64MHz***	***2MHz/ 8MHz***	***2MHz/ 16MHz***	***2MHz/ 32MHz***	***2MHz/ 64MHz***
Total Quiescent Power (W)	0.875	0.875	0.875	0.916	0.916	0.917	0.916	0.916	0.917	0.916
Total Dynamic Power (W)	0.015	0.019	0.014	0.024	0.019	0.028	0.018	0.024	0.033	0.023
Total Power (W)	0.891	0.895	0.889	0.941	0.935	0.945	0.934	0.941	0.950	0.939

CHAPTER 6

6. Comparison with the Past-Proposed SPWM Generators

This Section presents the performance results achieved by the past-proposed SPWM generator architectures after they have been modified in order to produce a unipolar SPWM for single-phase full-bridge inverters and be fully compatible with the newly introduced SPWM generator in this thesis. They were also implemented on the same target device Virtex-5 FPGA (XC5VLX110T). Many tests took place so as to find the maximum operate switching frequencies of all past-proposed architectures. The corresponding results are presented in the following sections.

6.1 Operating switching frequencies

After many tests for several switching frequencies and modulation indexes, the maximum achieved operating switching frequency, concerning any previous architecture and how the clock generator was managed is shown below (√ stands for operating switching frequencies, x stands for non operating switching frequencies).

- **Nadir architecture @ 136 MHz:**
  - **f_c = 50 kHz, $f_{desired\_clock}$ = 34 MHz** => 1 clock cycle for positive edge of the desired clock cycle and 1 clock cycle for the negative one and DCM = 2/2. √
  - **f_c = 100 kHz, $f_{desired\_clock}$ = 68 MHz** => FSM decreases to half the system clock frequency and DCM = 2/2. √
  - **f_c = 112 kHz, $f_{desired\_clock}$ = 78 MHz** => FSM decreases to half the system clock frequency and DCM = 8/7. x
  - **f_c = 200 kHz, $f_{desired\_clock}$ = 136 MHz** => FSM decreases to half the system clock frequency and DCM = 2/1. x

- **Peak architecture @ 117 MHz:**

  - **f_c = 100 kHz, $f_{desired\_clock}$ = 58 MHz** => FSM decreases to half the system clock frequency and DCM = 2/2. √

  - **f_c = 112 kHz, $f_{desired\_clock}$ = 66 MHz** => FSM decreases to half the system clock frequency. DCM = 28/25. √

  - **f_c = 200 kHz, $f_{desired\_clock}$ = 119 MHz** => FSM decreases to half the system clock frequency and DCM = 2/1. √

  - **f_c = 250 KHz, $f_{desired\_clock}$ = 146 MHz** => FSM decreases to half the system clock frequncy and DCM = 5/2. √

  - **f_c = 300 KHz, $f_{desired\_clock}$ = 175 MHz** => FSM decreases to half the system clock frequncy and DCM = 3/1. x

- **Peak/Nadir architecture @ 119 MHz:**

  - **f_c = 100 kHz, $F_{desired\_clock}$ = 62 MHz** => FSM decreases to half the system clock frequency and DCM = 2/2. √

  - **f_c = 112 kHz, $F_{desired\_clock}$ = 68 MHz** => FSM decreases to half the system clock frequency and DCM = 28/25. √

  - **f_c = 200 kHz, $F_{desired\_clock}$ = 123 MHz** => FSM decreases to half the system clock frequncy and DCM = 2/1. √

  - **f_c = 250 kHz, $F_{desired\_clock}$ = 153 MHz** => FSM decreases to half the system clock frequncy and DCM = 5/2. √

  - **f_c = 300 kHz, Fdesired_clock = 184 MHz** => FSM decreases to half the system clock frequncy and DCM = 3/1. x

- **N-samples architecture @ 113 MHz:**

  - **F_c = 100 KHz, $F_{desired\_clock}$ = 57MHz** => FSM decreases to half the system's clock frequency and DCM = 2/2. √

- **F_c = 200 KHz, $F_{desired\_clock}$ = 113MHz** => FSM decreases to half the system's clock frequency and DCM = 2/1. √

- **F_c = 250 KHz, $F_{desired\_clock}$ = 141MHz** => FSM decreases to half the system's clock frequency and DCM = 5/2. √

- **F_c = 300 KHz, $F_{desired\_clock}$ = 169MHz** => FSM decreases to half the system's clock frequency and DCM = 3/1. x

➢ **Triangles Similarity @ 151 MHz:**

This architecture determines slightly differently the desired system clock frequency and consequently the desired switching frequency. As it was described in the previous chapter and Section 4.2.3 the PWM_TM counter is equivalent to the clock generator in any other architecture. The values of the corresponding frequencies are calculated according to the eq. 21.

It is also necessary to be reminded that this architecture generates the SPWM signal by producing the ON and OF state of the inverter's switches which is calculated by the CE parameter which is calculated according to the eq. 16.

Applying the eq. 16 for the CE calculation with system clock frequency 151 MHz and e.g. f_c = 100 kHz, then the PWM_TM is equal to 750. But its actual value was reduced to 500 when it was measured with the oscilloscope in order to achieve the desired switching frequency.

Assuming the modulation index takes its minimum value which is 0.1 and the sine value takes the same value, according to eq. 16, the resulting values of CE parameter results as following:

- **f_C = 1 kHz, PWM_TM = 50.000, M = 0.1, sine value = 0.1** => CE = 500

- **f_C = 10 kHz, PWM_TM = 5.000, M = 0.1, sine value = 0.1** => CE = 50

- **f_C = 20 kHz, PWM_TM = 2.500, M = 0.1, sine value = 0.1** => CE = 25

- **f_C = 100 kHz, PWM_TM = 500, M = 0.1, sine value = 0.1** => CE = 5

Although the spectrum of this architecture seems to operate at high switching frequencies up to 1MHz, the quality of the produced SPWM signal is inadequate and this is explained as follows: the CE parameter needs 30 clock cycles to be calculated; as it can be observed by the previous CE calculations for switching frequencies greater than 10 kHz (e.g. 20 kHz, 50 kHz and 100 kHz the

CE value is less than 30 cycles, which are required for its calculation. Thus, for switching frequencies greater than 10 kHz and modulation indexes less than 0.5, the SPWM output signal does not correspond to the expected one as presented in Fig. 30.

Figs. 66-70 illustrate the FFT pattern of past-proposed architectures in their maximum operating switching frequencies. Figs 71-86 show the graph of the experimental and theoretical output voltage at 50 Hz of all the previously proposed architectures for f_c = 10 kHz and M = 0.1-1, f_c = 100 kHz and M = 0.1, 0.5 and 0.9, respectively and the maximum f_c achieved by each design and M = 0.1, 0.5 and 0.9 respectively. All architectures including the proposed SPWM in this thesis except the architecture that calculates the ON/OFF duration of the SPWM pulses seem to operate very close to the theoretical output voltage. All these implementations operate by multiplying the values of the sinusoidal wave with the modulation index and this result is compared to the corresponding value of the triangular wave and where the result is equal or greater than zero, the output pulse is set to logical "1", otherwise it is set to logical "0". In the case of the last described architecture, it has been mentioned that it does not apply this logic in order to produce the SPWM pulses. It has already pre-computed the time intervals where the sine value is greater than the carrier and thus it sets the pulse ON during this pre-computed comparison. When the sine value is less than the carrier the respective operation is performed and the pulse is set OFF. This is the reason that the experimental output voltage has a large deviation from the theoretical output voltage at 50 Hz.

Fig. 66. FFT pattern for the nadir architecture (f_c max = 100 kHz, M = 0.5).

Fig. 67. FFT pattern for the peak architecture (f_c max = 250 kHz, M = 0.5).

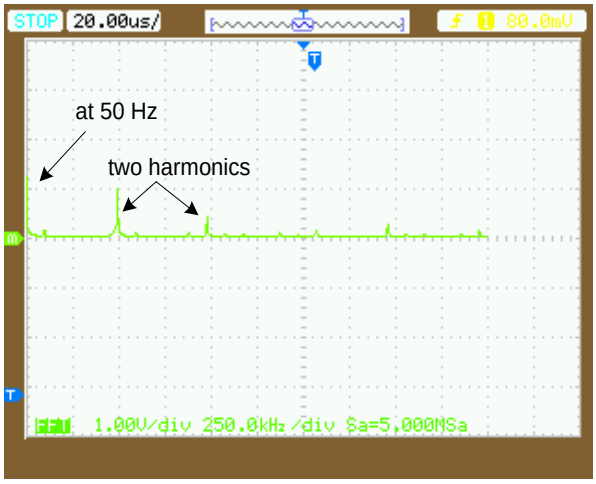

Fig. 68. FFT pattern for the peak/nadir architecture, (f_c max = 250 kHz, M = 0.5).

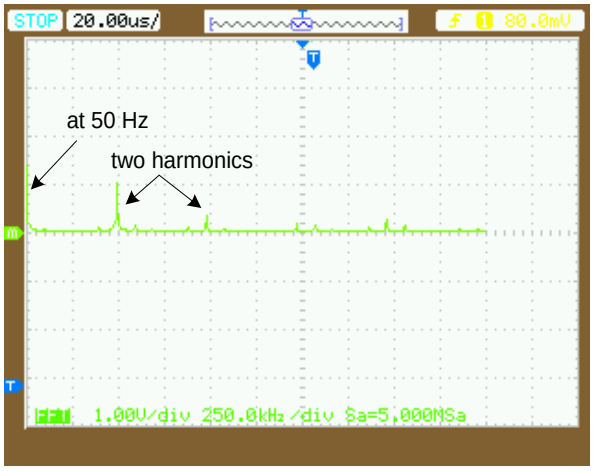

Fig. 69. FFT pattern for the N-samples architecture (f_c max = 250 kHz, M = 0.5).

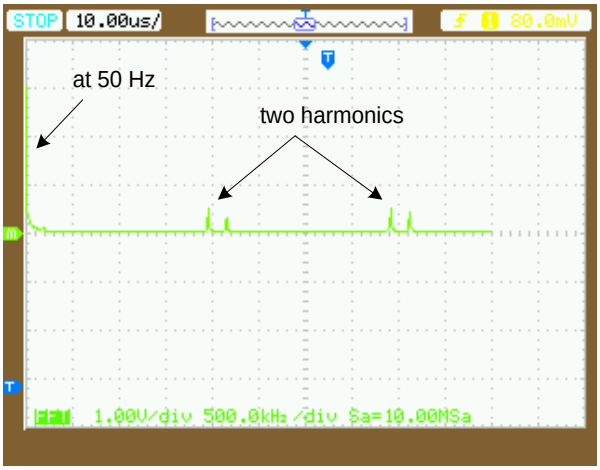

Fig. 70. FFT pattern for the triangles architecture (f_c max = 1 MHz, M = 0.5).

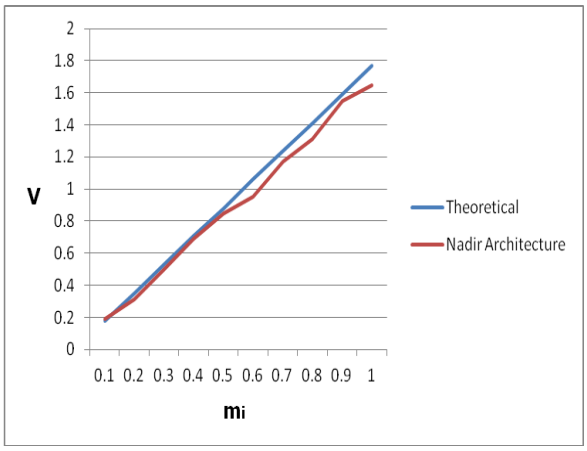

Fig.71. Experimental and theoretical output voltage at 50 Hz for the nadir architecture in case that M = 0.1-1 and f_c = 10 kHz (d ranges from 2.5-11.4%).

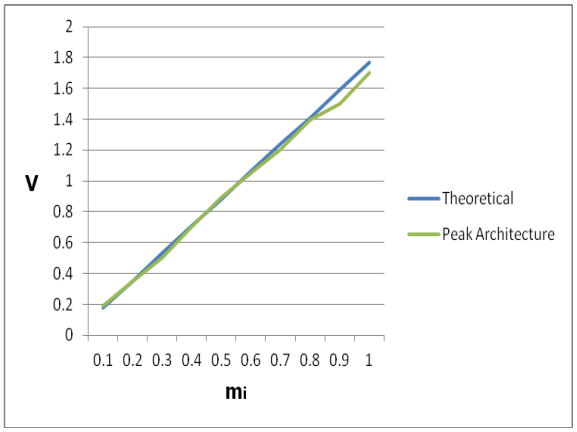

Fig.72. Experimental and theoretical output voltage at 50 Hz for the peak architecture in case that M = 0.1-1 and f_c = 10 kHz (d ranges from 0-5.7%).

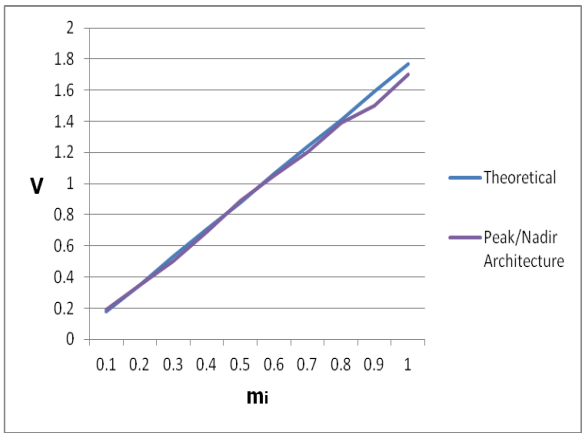

Fig. 73. Experimental and theoretical output voltage at 50 Hz for the peak/nadir architecture in case that M = 0.1-1 and f_c = 10 kHz (d ranges from 0-5.7%).

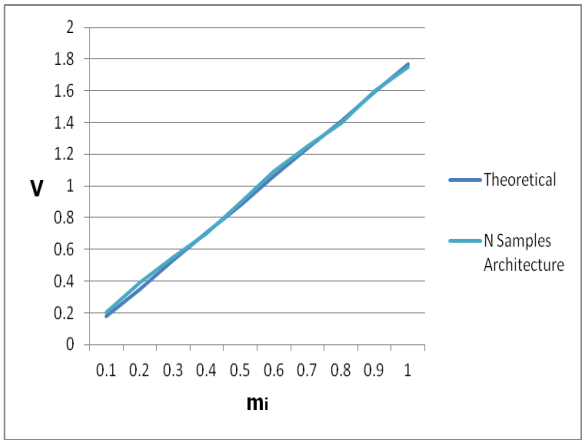

Fig.74. Experimental and theoretical output voltage at 50 Hz for the n samples architecture in case that M = 0.1-1 and f_c = 10 kHz (d ranges from 0-11.4%).

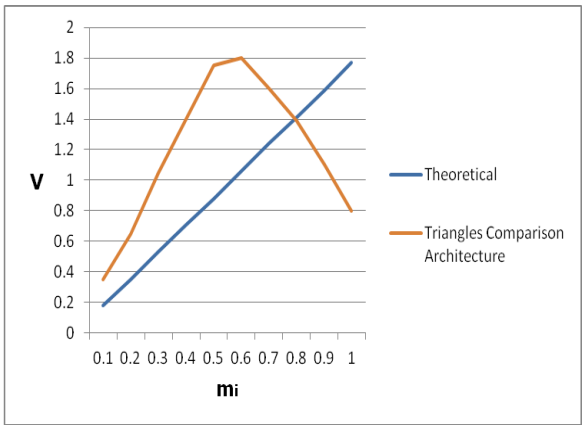

Fig.75. Experimental and theoretical output voltage at 50 Hz for the triangles architecture in case that M = 0.1-1 and f_c = 10 kHz (d ranges from 1.4-98.9%).

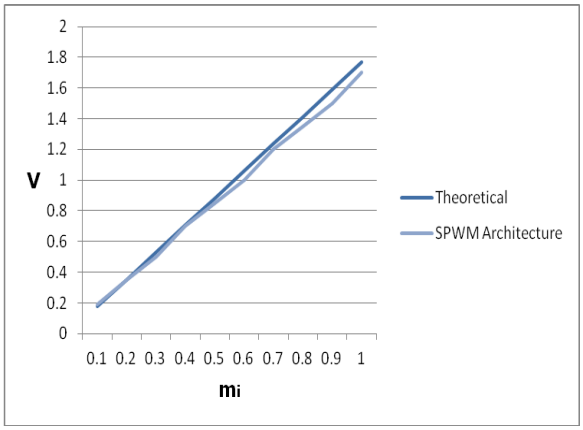

Fig.76. Experimental and theoretical output voltage at 50 Hz for the newly proposed architecture in case that M = 0.1-1 and f_c = 10 kHz (d ranges from 0-5.6%).

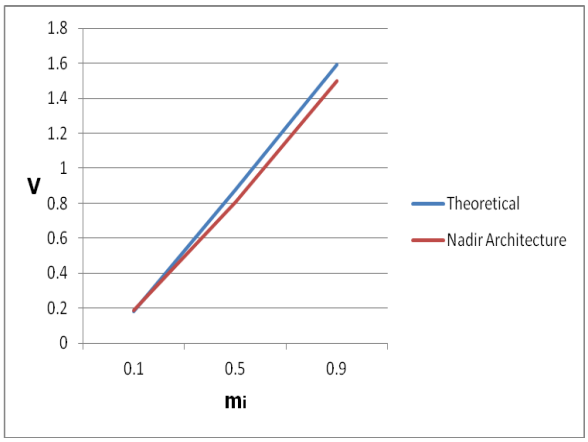

Fig.77. Experimental and theoretical output voltage at 50 Hz for the nadir architecture in case that M = 0.1, 0.5 and 0.9, respectively and f_c = 100 kHz (d = 5.6%, 8% and 5.7%, respectively).

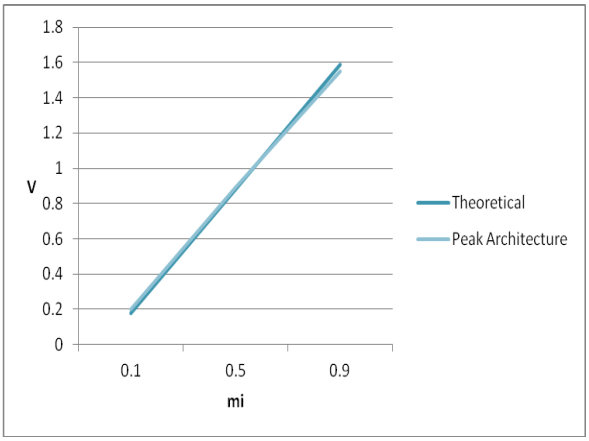

Fig.78. Experimental and theoretical output voltage at 50 Hz for the peak architecture in case that M = 0.1, 0.5 and 0.9, respectively and f_c = 100 kHz (d = 11.1%, 1.1% and 2.5%, respectively).

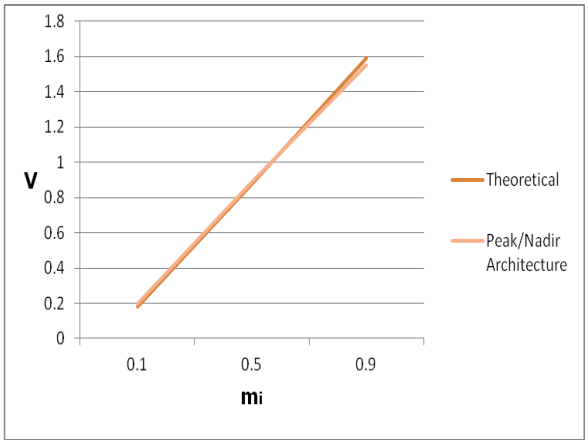

Fig.79. Experimental and theoretical output voltage at 50 Hz for the newly proposed architecture in case that M = 0.1, 0.5 and 0.9, respectively and f_c = 100 kHz (d = 5.6%, 8% and 5.7%, respectively).

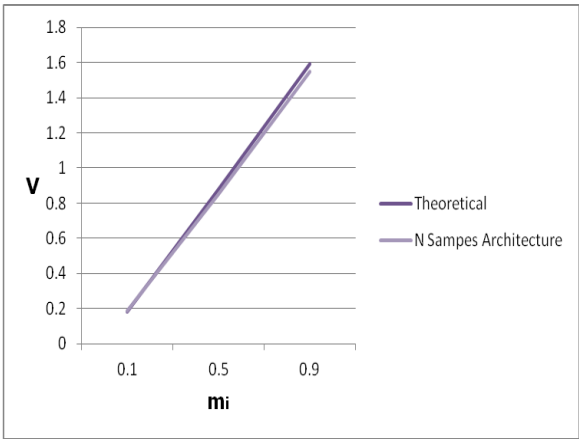

Fig.80. Experimental and theoretical output voltage at 50 Hz for the n samples architecture in case that M = 0.1, 0.5 and 0.9, respectively and f_c = 100 kHz (d = 5.6%, 3.4% and 2.5%, respectively).

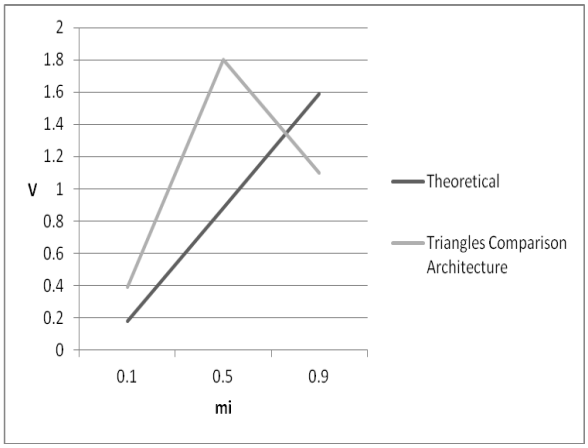

Fig.81. Experimental and theoretical output voltage at 50 Hz for the triangles architecture in case that M = 0.1, 0.5 and 0.9, respectively and f_c = 100 kHz (d = 116.7%, 104.8% and 30.8%, respectively).

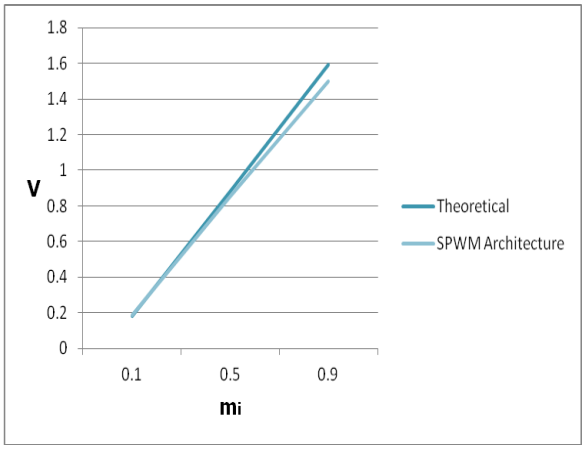

Fig.82. Experimental and theoretical output voltage at 50 Hz for the newly proposed architecture in case that M = 0.1, 0.5 and 0.9, respectively and f_c = 100 kHz (d = 5.6%, 3.4% and 5.7%, respectively).

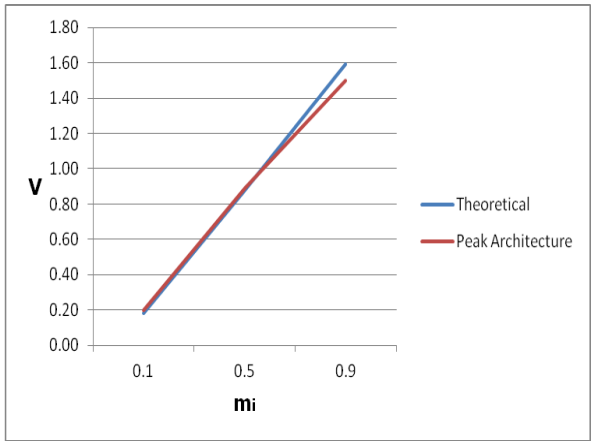

Fig.83. Experimental and theoretical output voltage at 50 Hz for the peak architecture in case that M = 0.1, 0.5 and 0.9, respectively and f_c = 250 kHz (d = 11.1%, 1.1% and 5.7%, respectively).

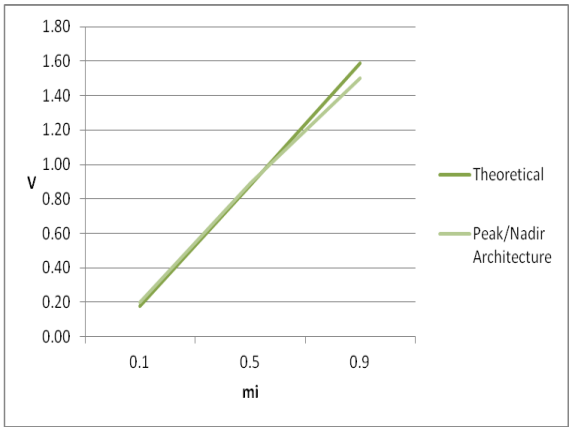

Fig.84. Experimental and theoretical output voltage at 50 Hz for the peak/nadir architecture in case that M = 0.1, 0.5 and 0.9, respectively and f_c = 250 kHz. (d = 11.1%, 1.1% and 5.7%, respectively).

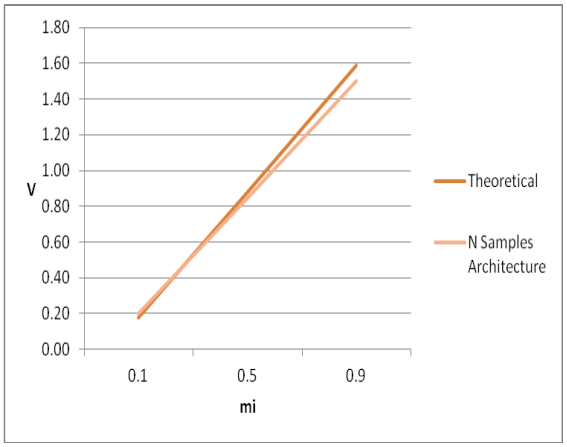

Fig.85. Experimental and theoretical output voltage at 50 Hz for the N-samples architecture in case that M = 0.1, 0.5 and 0.9, respectively and f_c = 250 kHz (d = 11.1%, 3.4% and 5.7%, respectively).

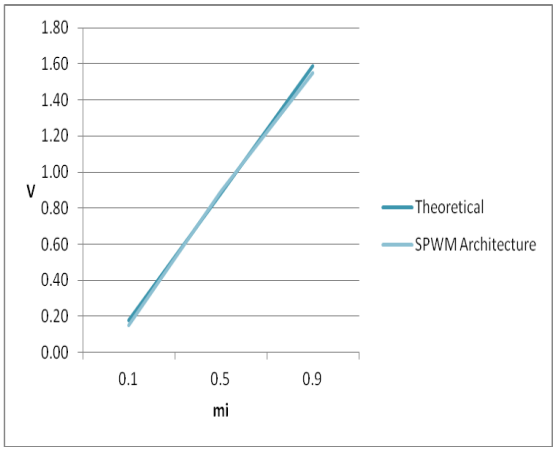

Fig.86. Experimental and theoretical output voltage at 50 Hz for the newly proposed architecture in case that M = 0.1, 0.5 and 0.9, respectively and f_c = 250 kHz (d = 11.1%, 1.1% and 2.5%, respectively).

6.2 Past-proposed systems resources

In this Section, by the FPGA resources utilized by the past-proposed SPWM generator designs, are presented. The resources required by the fully implemented systems are presented in Tables 3-7 for all the possible switching frequencies that the previous architectures can operate at; the last row in those tables shows the corresponding maximum clock frequency. These tables show that the utilized resources are only few and none of them is the critical one to prevent further development in the implementation of the corresponding design, in contrast to the newly proposed architecture, where the Block RAMs were the critical resource that restricts further increase of the sampling frequency.

The critical path for nadir, peak, peak/nadir and N-samples architectures resides at the hardware performing the access of the sinusoidal memory and consequently this was the bottleneck for achieving higher operating switching frequencies, since the system clock frequency determined the maximum allowed switching frequency.

In the architecture that computed the ON/OFF signal duration the critical path was at the control units that were responsible for the ON and OFF pulses production. Taking into consideration that i) the sine-wave may hold a small value (e.g. 0.1) , ii) the modulation index may hold its minimum value, which is the same as the sine and iii) the CE parameter, that defines the ON and OFF duration, needs 30 clock cycles to be calculated then this scenario constitutes a bottleneck for high switching frequencies. The higher the switching frequency is, the smaller the PWM_TM counter is and this results to a small value of the CE parameter, even smaller than 30. This last CE value corresponds to the prerequisite clock cycles in order the CE value to be computed. The ON and OF duration are determined by this last calculation.

Table 3. FPGA resources and system frequency for nadir architecture at all possible switching frequencies.

f_c	***10kHz***	***100kHz***
DSPs	1/64 (6%)	1/64 (6%)
Slice Registers	54 /69120 (5%)	53 /69120 (5%)
Slice LUTs	172/69120 (4%)	165/69120 (4%)
BRAMs	1/148 (1%)	1/148 (1%)
Max clk frequency	136MHz	139MHz

Table 4. FPGA resources and system frequency for peak architecture at all possible switching frequencies.

f_c	***10kHz***	***100kHz***	***250kHz***
DSPs	4/64 (6%)	4/64 (6%)	4/64 (6%)
Slice Registers	3615 /69120 (5%)	3610 /69120 (5%)	3612 /69120 (5%)
Slice LUTs	3021/69120 (4%)	3021/69120 (4%)	3023/69120 (4%)
BRAMs	1/148 (1%)	1/148 (1%)	1/148 (1%)
Max clk frequency	114MHz	116MHz	112MHz

Table 5. FPGA resources and system frequency for peak/nadir architecture at all possible switching frequencies.

f_c	***10kHz***	***100kHz***	***250kHz***
DSPs	4/64 (6%)	4/64 (6%)	4/64 (6%)
Slice Registers	3615 /69120 (5%)	3610 /69120 (5%)	3614 /69120 (5%)
Slice LUTs	3013/69120 (4%)	3009/69120 (4%)	3028/69120 (4%)
BRAMs	1/148 (1%)	1/148 (1%)	1/148 (1%)
Max clk frequency	117MHz	123MHz	120MHz

Table 6. FPGA resources and system frequency for N-samples architecture at all possible switching frequencies.

f_c	***10kHz***	***100kHz***	***250kHz***
DSPs	4/64 (6%)	4/64 (6%)	4/64 (6%)
Slice Registers	3616 /69120 (5%)	3611 /69120 (5%)	3612 /69120 (5%)
Slice LUTs	3021/69120 (4%)	3014/69120 (4%)	3015/69120 (4%)
BRAMs	1/148 (1%)	1/148 (1%)	1/148 (1%)
Max clk frequency	111MHz	113MHz	109MHz

Table 7. FPGA resources and system frequency for triangles architecture at all possible switching frequencies.

f_c	***10kHz***	***100kHz***	***1MHz***
DSPs	4/64 (6%)	4/64 (6%)	4/64 (6%)
Slice Registers	3616 /69120 (5%)	3611 /69120 (5%)	3612 /69120 (5%)
Slice LUTs	3021/69120 (4%)	3014/69120 (4%)	3015/69120 (4%)
BRAMs	1/148 (1%)	1/148 (1%)	1/148 (1%)
Max clk frequency	111MHz	113MHz	109MHz

6.3 Past-proposed systems power resources

In this Section the power consumed by all of the past-proposed SPWM generator designs for different switching frequencies is presented. Tables 8-12 show the power consumption measurements for all the other implementations and switching frequency is equal to 10 kHz, 100 kHz and the maximum operating frequency, respectively. As it can be observed, all of the measurements do not exceed 1Watt (W) limit, something that constitutes either the newly proposed SPWM generator, or the previously proposed architectures ideal for the calculation of the SPWM pattern in the PV inverter applications considered in this thesis.

Table 8. FPGA power consumption for nadir architecture at all possible switching frequencies.

f_c	***10kHz***	***100kHz***
Total Quiescent Power (W)	0.847	0.915
Total Dynamic Power (W)	0.003	0.004
Total Power (W)	0.877	0.919

Table 9. FPGA power consumption for peak architecture at all possible switching frequencies.

f_c	***10kHz***	***100kHz***	***250kHz***
Total Quiescent Power (W)	0.876	0.875	0.916
Total Dynamic Power (W)	0.022	0.018	0.020
Total Power (W)	0.898	0.893	0.937

Table 10. FPGA power consumption for peak/nadir architecture at all possible switching frequencies.

f_c	***10kHz***	***100kHz***	***250kHz***
Total Quiescent Power (W)	0.875	0.876	0.916
Total Dynamic Power (W)	0.020	0.022	0.017
Total Power (W)	0.895	0.898	0.932

Table 11. FPGA power consumption for N-samples architecture at all possible switching frequencies.

f_c	***10kHz***	***100kHz***	***250kHz***
Total Quiescent Power (W)	0.876	0.876	0.916
Total Dynamic Power (W)	0.021	0.020	0.014
Total Power (W)	0.897	0.896	0.930

Table 12. FPGA power consumption for triangles architecture at all possible switching frequencies.

f_c	***10kHz***	***100kHz***	***1MHz***
Total Quiescent Power (W)	0.875	0.875	0.875
Total Dynamic Power (W)	0.012	0.011	0.013
Total Power (W)	0.887	0.886	0.887

6.4 Total Harmonic Distortion (THD)

In this Section presents the Total Harmonic Distortion (THD) among of the implemented SPWM generation architectures vs. the theoretical. THD is defined as the RMS value of the SPWM waveform remaining when the fundamental (i.e. at 50 Hz) is removed. Harmonic distortion is caused by the introduction of waveforms at frequencies in multiplies of the fundamental, i.e.: 3rd harmonic is located 3x the fundamental frequency = 150Hz.

Initially, the distortion factor, d, was measured using the HAMEG HM8027 distortion meter. Then the corresponding THD values were calculated using the following equation:

$$\mathrm{THD} = \frac{d}{\sqrt{1 - d^2}} \tag{38}$$

where *d* is the distortion factor indicating the share of harmonics in the total signal (fundamental harmonics). Fig. 87 shows the THD (%) measurement of all SPWM generation architectures compared with the corresponding theoretical THD value for f_c = 1 kHz and M = 0.9.

It is observed that the THD (%) for the newly proposed SPWM generator abstains less than the other architectures from the theoretical THD value. The past-proposed architectures exhibit a small deviation, excluding the triangle architecture which tends to exceed the theoretical value significantly.

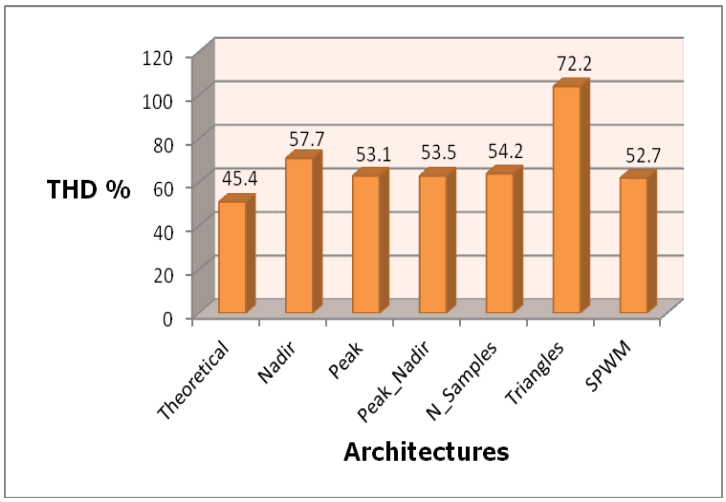

Fig. 87. THD for all SPWM generation architectures for f_c = 1 kHz and M = 0.9.

CHAPTER 7

7. SMART Project: ARTEMIS Joint Undertaking

This chapter presents the European project SMART (Secure, Mobile visual sensor networks ARchiTecture) which aims to the design, development and implementation of a sophisticated Wireless Sensor Network (WSN) node, based on a low-power miniaturized reconfigurable device and describes the way that the present thesis can contribute to this project.

7.1 Concept and objectives

Wireless Sensor Networks (WSNs) are expected to have widespread application in the coming decades, ranging from monitoring and control (in industrial environments) to emergency response to habitat and environmental monitoring. WSNs have been identified as one of the most important technologies for the 21st century and according to current market estimations, more than half a billion nodes had been shipped for wireless sensor applications in 2010. These networks must be capable of adapting to changing environments and requirements. A WSN application may need to alter its behavior to manage limited resources more efficiently, recover from broken network links, or change its functional behavior in response to commands issued by an operator or even implied by the environment itself.

A WSN is a collection of nodes organized into a "cooperative" network. Each node consists of a processing unit, may contain multiple types of memory, an RF transceiver (usually with a single omni-directional antenna), a power source (e.g. batteries, solar cells etc.) and may accommodate various sensors and/or actuators. The nodes communicate wirelessly and often self-organize after being deployed in an ad-hoc fashion. Systems of thousands or even tens of thousands nodes are anticipated. Such systems can revolutionize the way we live and work.

Currently, WSNs are beginning to be deployed at an accelerated pace. It is not unreasonable to expect that in 10-15 years the world will be covered with WNSs. This technology is exciting and has tremendous potential for numerous application areas including environmental, medical, military, transportation, entertainment, crisis management, homeland security, defense and smart spaces. The vast majority of the existing sensor nodes are software based, which provides the flexibility necessary for adaptation. A variety of programs can be stored in a node's local

memory, or a base station can wirelessly distribute programs for necessary adaptations. Even if a processor executing software is far less efficient (in terms of energy consumption, manufacturing cost per unit and performance) than a fixed-logic ASIC executing the same function, an ASIC does not have the flexibility for node-level adaptation and therefore it is not used in WSN environments.

Since sensor nodes are typically run on batteries, one of the most important factors in determining the success of a certain distributed sensor network (if not the most important one) is how well it manages energy. Hence, the SMART (Secure, Mobile visual sensor networks ARchiTecture) project focuses on allowing WSNs to adapt their energy consumption in real time based upon the rapidly changing environmental conditions [39]. This has been enabled through the use of data-compression and a technique that has been employed for the first time in a WSN environment: Real-Time Dynamic hardware reconfigurability.

Another critical factor for the WSN infrastructure is the provided security level. The security aspect is extremely important, since WSNs very frequently transmit and process sensitive data; in parallel, the isolated and distributed nature of the infrastructure, together with the requested low power consumption, make the provision of high levels of security in WSNs a very difficult task. SMART tackles the open-research topic of WSN security by adopting an innovative approach.

Additionally, the network bandwidth in WSNs is very often limited and therefore it is hard to support real-time video streaming over it. Moreover, current video encoding technologies rely upon motion estimation and compensation techniques and thus they require high computation power, which sensor nodes are not usually equipped with. SMART provides an innovative WSN infrastructure, moving towards the new era of Wireless Visual Sensor Nodes (WVSN) that supports high-quality real-time video streaming over relatively low-bandwidth links. Within SMART, WVSN is defined as networks of miniaturized, light-weight, low-cost, battery powered sensing devices, able to capture images and video streams utilizing embedded micro-cameras, to pre-process the content and to transmit it efficiently over a mobile ad-hoc network.

In general, for numerous application domains, there are certain specific and very important features of WSNs, such as high-security levels, low power consumption, video-capabilities, auto-configuration and self-organization, that are not efficiently addressed by today's offerings; SMART aims at providing an infrastructure that will support all those features efficiently and inexpensively. It should be noted that every WSN node consists of the sensing and actuation unit

(single element or array), the processing/communication unit and some kind of power supply. The SMART project focuses on the processing/communication element, while it offers the flexibility to anyone to plug his/her own sensor/actuator unit(s) and take advantage of the SMARTs very low power and sophisticated processing. The SMART approach is general enough so any kind of sensor/actuator can be plugged to the SMART node such as radio-wave frequency sensors, optical, electro-optical and infrared sensors, radars, lasers, location/navigation sensors, seismic and pressure-wave sensors, environmental parameter sensors (e.g., wind, humidity, temperature), as well as biochemical, nuclear and other national security–oriented sensors; as a result, numerous and diverse application domains can take advantage of the relevant features and efficiency of the SMART basic infrastructure.

SMART proposes a new architecture for such sensor nodes, which would be based on reconfigurable hardware devices. This is due to the substantial boost in sensor network node flexibility, features, performance, security and low power-consumption provided by such hardware resources. Even though the reconfigurable hardware resources are often considered, for certain processing tasks, more power hungry than the ultra-low-power micro-controllers, they allow for extremely higher performance and power-efficient processing when implementing encryption/decryption/authentication algorithms as well as data/video/image compression tasks, while they can be reconfigured in real-time. Based upon real-world measurements, recently announced tiny FPGAs consume less than $1/100^{th}$ of the power consumed by a low-power Mcro-controller executing the exact same such algorithms. The reconfigurable devices are also more power efficient than the corresponding micro-controllers and DSPs when executing certain digital signal processing tasks. Moreover, the use of reconfigurable systems can heavily increase the resistance of the distributed and thus highly vulnerable to attacks, sensor nodes, to the so-called "side attacks", such as simple power attacks (SPAs) and differential power attacks (DPAs).

Last but certainly not least, based upon those reconfigurable devices, highly flexible nodes can be built. Those nodes will take advantage of the real-time reconfiguration feature of the state-of-the-art reconfigurable devices and will be able to alter their processing tasks to allow for power-efficient communication under the rapidly changing sensor environment. For example, the proposed highly flexible sensor nodes can use a certain communication protocol for a low-noise environment, that can be altered remotely (or even autonomously), in run-time, when the noise increases over a specific threshold; in another case it can increase the security aspects of both the transmitted data and the sensor node itself when it senses any kind of a security attack. In order to

change the communication/encryption/compression processing tasks, implemented in the state-of-the-art, real-time- reconfigurable systems, a two-step process is utilized: 1) certain parts of the systems are fixed, namely those destined to receive the configuration bit-stream (according to a certain very low-power and low-bandwidth wireless communication protocol) which are used for configuration purposes, 2) when the configuration information is received it is used to re-program the Reconfigurable Device (or maybe just part of it) for example to execute a different communication/compression/encryption protocol.

In order to address all those issues, the proposed processing node mainly consists of a low-power Reconfigurable Device and a low-power processor, either embedded in a single chip or in two different ones. The Reconfigurable resources execute the tasks that are more efficiently executed by dedicated hardware modules (e.g. data and video compression, encryption, authentication), while the rest of the processing tasks are executed by an ultra-low-power CPU.

The research problems which are addressed in order to implement the innovative SMART infrastructure are among three very challenging areas: a) Reconfigurable Sensor Devices, b) Secure Wireless Ad-hoc Networking and c) Audio/Visual Processing and Networking. In more details:

a) **Powerful nodes:** The SMART node is able to execute certain encryption, authentication and compression algorithms that cannot be executed by today's offering due to their need for high processing power (and thus high power consumption). In SMART, the available encryption, authentication and compression schemes are investigated and, based on a number of criteria (including the associated power consumption and the actual needs of the WSN environments), a certain group of new such schemes are introduced and implemented in the reconfigurable nodes. Since the reconfigurable devices consume much less power when executing such algorithms, the SMART framework will be able to provide much more features than the existing solutions at the same power-budget. Moreover, a certain reconfigurable silicon device has been implemented that and optimized for the execution of all those schemes; this device consumes up to an order of magnitude less power when compared to an off-the-shelf reconfigurable device, when implementing the developed data manipulation techniques.

b) **Low-Power infrastructure:** If we reduce the data transmitted over a WSN, we reduce also the power consumption. Moreover, the network bandwidth in WSN is, very often, limited. Therefore, it is highly desirable to compress the data transmitted. However, in order to reduce the overall

power-budget, the data compression task should consume less power than that saved in data transmission. However, existing compression algorithms, when executed in microcontroller-based sensor nodes, consume marginally less power than that saved by the reduced data transmission. Since the SMART nodes consume significantly less power than the microcontroller-based nodes (as low as $1/100^{th}$) when executing the compressing tasks and the compression ratio these algorithms can achieve when applied to real-world (network) data can be up to 60%, the overall power budget of the SMART framework is significantly reduced when compared to the existing solutions. In order to reach an optimal solution, the various data compression algorithms have been investigated and a group of innovative ones has been introduced and implemented in the SMART reconfigurable devices.

c) **Highly secure nodes:** The nodes in a sensor network are by nature distributed and thus, in the vast majority of the cases, they are vulnerable to side attacks. Those attacks are performed by measuring certain characteristics of the processing activity on a node such as power consumption, electromagnetic emission, timing, etc. By analyzing those measurements, the attacker can recover the secret information stored in the node (e.g. the key used in the majority of the security algorithms). The most efficient way of defending against those attacks is the use of special-purpose hardware blocks that are designed in specific ways; however, those implementation techniques increase the overall power consumption of the security module. SMART provides hardware architecture for the nodes that consumes relatively low power while providing extremely high-levels of protection against such side attacks.

d) **Real-time reconfigurable nodes:** The SMART nodes are capable of being (re)configured in real-time. In order to exploit this advantage in an optimal manner, there would be a mechanism sensing the environment and informing either the node itself or a centralized management system of the need to perform a node reconfiguration. This is obviously an open and very interesting research problem. Two examples demonstrating the advantages of real-time reconfiguration are the following: a) the WSN can operate in a low-secure, low-power mode until the detection mechanism realizes that a certain security threat appears; then a group of nodes will be reconfigured so as to support a much better (and more power-hungry) encryption protocol and, obviously, when the threat disappears the nodes will switch back to the low-power mode; b) the WSN can have a low-noise, low-power mode in which the Forward Error Correction (FEC) code used (such as the Viterbi code) will employ a short constrain length (this length heavily impacts the error-rate as well as the processing power-consumption); when the sensing mechanism

realizes that the noise increases, the constrain length used by a group of nodes will be increased so as to allow the node to accommodate higher error-rates at the cost of higher power consumption.

e) **Video-capable WSN:** Since the network bandwidth in WSNs is very often limited, it is hard to support real-time video streaming over it. Moreover, the current video encoders use complex algorithms (i.e. they require a lot of CPU and/or hardware resources) in order to achieve high compression ratio and a good quality; as a result, they require high computation power that sensor nodes are not usually equipped with. The re-configurable device of the SMART node executes video compression tasks in a more efficient manner than the currently available micro-controller based nodes. Video compression algorithms have been investigated, from very simple one like JPEG (DCT based) up to the last standardized algorithms such as JPEG2000 or H.264 / MPEG4-Part10and the most appropriate, for the SMART reconfigurable infrastructure, has been selected and altered so as to satisfy the specific WSN requirements.

f) **Flexible middleware:** In order to seamlessly take advantage of the various features of the implemented device, an abstract yet powerful programming environment is definitely needed. Within SMART has been designed and implemented a flexible, context-dependent and modular middleware, providing the needed programming abstractions to build SMART environments independently of the implementation peculiarities of the underlying sensors and tags dynamically discovered in the deployment environment.

g) **User-friendly configuration, commissioning and self-organization tools:** In order to be able to easily adopt the SMART infrastructure in various WSN environments, both the initial configuration and the real-time re-configuration of the SMART nodes are done in a user-friendly and fully automated way by a specially developed toolset which takes advantage of the developed middleware. As a result, the end-user and/or the manager of the system do not need to be at all aware of the fact that the SMART sensor nodes contain Reconfigurable Devices. The commissioning aspects of the network have also been studied in detail to allow easy and transparent re-configuration of both the hardware and the software. Special attention has been paid to debug and maintenance aspects.

7.2 TSI contribution

SMART partners represent 5 European countries (Greece, Germany, Italy, Spain and Netherlands). More particularly they are: Hellenic Aerospace Industry (HAI), Thales (Thales), Philips Consumer Lifetime (Philips), Innovations of High Performance microelectronics (IHP), Telecommunications Systems Institute (TSI), TEI Halkidas (TEIHal), Metodos y Tecnologia (MTP), Universidad Politecnica de Madrid (UPM), Lippert (LIP), TU Carolo-WilhelMna zu Braunschweig (TUBS), Nanosens (NSEN).

TSI's contribution to SMART project was to implement in the Reconfigurable Devices adaptations of existing innovative data compression, encryption and authentication schemes addressing the WSNs' requirements. No hardware-based compression encryption schemes exist for WSNs' environments. Therefore, TSI developed and implemented in the nodes' reconfigurable device a number of novel such schemes that will compress efficiently the WSN's data (therefore reducing the power consumption for transmission), consume small amounts of energy, while also being more secure than the existing software-based solutions. Those schemes are based on variations of well known compression (Huffman and Lempel-Ziv), encryption (Blowfish and AES) and authentication algorithms (MD5, SHA1) and are implemented in a very innovative way so as to significantly reduce the power consumption.

After the implementation of the compression, enctryption and authentication schemes was completed, TSI contributed in the definition of the details of the testing equipment and the complete environment in which the validation of SMART took place by specifying the test cases, test and validation plan and demo scenarios for the SMART platform. The test and validation cases target heterogeneous traffic, rapidly changing situations in the WSN environment and certain side-attacks and propose actions to those situations. TSI also participated at the dissemination effort of the project. A detailed dissemination plan has been specified in the form of a database where relevant events (exhibitions, conferences, workshops, journal's/magazine's CFPs) pursued during the lifetime of the project will be stored.

7.3 SMART grid application

Implementing network security requires significant computational time and energy and becomes particularly challenging in a WSN battery-powered situation. For example, asymmetric cryptographic algorithms are not applicable in typical WSNs due to the limited computation and power resources available on a microcontroller-based sensor node. WSNs are expected to be widely deployed in a vast variety of environments for commercial, civil and military applications including surveillance, vehicle tracking, climate and habitat monitoring, intelligence, medical and acoustic data gathering. Although many of these application areas require a high level of information security, security has been the issue less addressed so far by researchers which have concentrated on the other problems that also needed to be solved in WSNs environments, such as routing, localization and reliability considerations.

The encryption schemes proposed by SMART can be applied to “SMART grid” applications, where the newly proposed SPWM generator in this thesis consists part of them. Firstly, a short definition of what encryption means is necessary to be given and then to be proposed how encryption methods can be exploited in a photovoltaic system.

Data encryption refers to mathematical calculations and algorithmic schemes that transform plaintext into cyphertext, a form that is non-readable to unauthorized parties. The recipient of an encrypted message uses a key which triggers the algorithm mechanism to decrypt the data, transforming it to the original plaintext version.

Photovoltaic systems need to be monitored to detect breakdown and optimize their operation. The application of the WSN technology can provide quick, easy and cost-effective data analysis. This enables accurate assessments of profitability and optimizing the technical performance of the entire PV system – keeping it cost effective also in the long term. Monitoring can measure production only, retrieve all the data from the inverter or retrieve all of the data from the communicating equipment (sensors, meters, etc.). Monitoring tools can be dedicated to supervision only or offer additional functions. Individual inverters may include monitoring using manufacturer specific protocols and software. Energy metering of an inverter may be of limited accuracy and not suitable for revenue metering purposes. A third-party data encryption-acquisition system can monitor multiple inverters, using the inverter manufacturer's protocols and also acquire weather-related information. Independent smart meters may measure the total energy production of a PV plant. Encrypted data collected from a monitoring system can be displayed

remotely over the World Wide Web. Some companies offer analysis software to analyze system performance.

Monitoring photovoltaic systems can provide useful information about their operation and what should be done to improve performance, but if the data are not reported properly, the effort is wasted. To be helpful, a monitoring report must provide information on the relevant aspects of the operation in terms that are easily understood by a third party. Appropriate performance parameters need to be selected and their values consistently updated with each new issue of the report. In some cases it may be beneficial to monitor the performance of individual components in order to refine and improve system performance, or be alerted to loss of performance in time for preventative actions. For example, monitoring battery charge/discharge profiles will signal when replacement is due before downtime because of system failure is experienced.

Encryption schemes proposed by SMART project can collect the information provided by a PV system or a solar park and the control unit that handles the encryption algorithms can verify, or not, the correct operation and the performance of any photovoltaic power station.

CHAPTER 8

8. Conclusions and Future Work

This chapter presents the conclusions derived by the implementation of a unipolar SPWM generator for a single-phase full-bridge inverter, using a Virtex 5 FPGA (XC5VLX110T). It also suggests some additional implementations of other algorithms that can complete the control unit that controls the power converter which is responsible for the AC power supply into the electric grid.

8.1 Conclusions

The Sinusoidal Pulse Width Modulation (SPWM) principle is widely used in power electronic DC/AC converters (inverters) in energy conversion and motor control applications. The previously proposed SPWM generators have been designed to operate at low switching frequencies (i.e. 1kHz - 20 kHz), while their operation at higher switching frequencies has not been explored.

Using the FPGA to implement the control unit of a DC/AC power converter, the realization of a reconfigurable digital system is achieved, exploiting its provision for high operating speed and low power consumption.

In this thesis, an FPGA-based SWPM generator has been presented, which is capable to operate at switching frequencies up to 1 MHz, thus it is capable to support the high switching frequency requirements of modern power electronic DC/AC converters. The design occupies a small fraction of a medium-sized FPGA and thus can be incorporated in larger designs. The successful operation of the proposed SWPM generator at high switching frequencies has been demonstrated not only with post place-and-route simulation results for design verification, but also with experimental results on actual hardware, thus validating the design.

As it had been analyzed in Chapters 5 and 6, the system clock frequency played an important role in the corresponding switching frequency, since in order to be able to achieve high switching frequencies up to 1 MHz requires FPGA operation at 100-160 MHz.

Another factor that could increase the maximum operating switching frequencies in the previously proposed systems would be to shorten the clock period of the counter that implements the triangular wave. This could be achieved by decreasing the number of bits that constitute the carrier counter (i.e. 128 bits instead of 256 used in all of the implemented architectures) and this would lead to the increase of the carrier switching frequency. But changing the counter bits will also reduce the resolution and thereby lowering the quality of the produced SPWM signal.

All the above conclusions, derived by the comparison between the past-proposed SPWM generator architectures and the one presented in this thesis, are summarized below in terms of: i) maximum switching frequency, ii) modulation index deviation from the theoretical value, iii) FPGA resources, iv) power consumption and v) THD value.

- **Maximum switching frequency:** the newly proposed SPWM generator architecture is capable to operate at switching frequencies up to 1 MHz in contrast with the nadir architecture having a maximum switching frequency 100 kHz, the peak, peak/ nadir and N-samples architectures having a maximum switching frequency 250 kHz and the triangles architecture having a maximum switching frequency 10 kHz, respectively.

- **Deviation of output voltage at 50Hz from the theoretical value:** taking into consideration the case that f_c = 10 kHz and M = 0.1-1 with a 0.1 step, the deviation, d (%), from the theoretical value of the newly proposed SPWM generator architecture is 0-5.6% the nadir architecture is 2.5-11.4%, the peak and peak/nadir architectures is 0-5.7%, the N-samples architecture is 0-11.4% and the triangles architecture is 1.4-98.9%, respectively.

- **Power consumption:** the power consumption of all the SPWM generator architectures at their maximum operating switching frequency is 0.889 W for the newly presented architecture with f_{cmax} = 1 MHz, 0.919 W for the nadir architecture with f_{cmax} = 100 kHz, 0.937 W for the nadir architecture with f_{cmax} = 250 kHz, 0.932 W for the peak/nadir architecture with f_{cmax} = 250 kHz, 0.930 W for the N-samples architecture with f_{cmax} = 250 kHz and 0.887 W for the triangles architecture with f_{cmax} = 10 kHz, respectively. It is observed that the SPWM generator architecture presented in this thesis consumes less power than almost all the past-proposed implementations operating in much higher switching frequency.

- **THD:** in case that f_c = 1 kHz and M = 0.9, the THD (%) measurements of the newly proposed SPWM generator architecture deviates 7.3 % from the theoretical THD value, whilst the nadir architecture deviates 12.3%, the peak architectures deviates 7.7%, the peak/nadir architecture deviates 8.1%, the N-samples architecture deviates 8.8% and the triangles architecture deviates 26.8 % from the theoretical THD value, respectively.

- **FPGA resources:** as far as the FPGA resources are concerned all the architecture designs occupy a small fraction of a medium-sized FPGA (XC5VLX110T). Excluding the BRAMs which are the critical resource that restricts further increase of the sampling frequency of the newly proposed SPWM generator architecture and which are the main difference of the past-proposed architectures, the next critical resource is the DSPs that occupy 3% more space in the FPGA device.

8.2 Future work

In stand-alone PV energy production application for interfacing the DC output voltage of the PV array at the operating voltage level of the fed load, a power converter which is controlled by a control unit is used. Depending on the type and standards of operation, the load can be powered either by DC operating voltage (e.g., batteries, DC motors, etc.) or by AC voltage (e.g. household appliances, AC motors, the electric grid in case of supplying the PV generated electricity to it etc.). A part of the AC voltage case has been implemented in this thesis.

In case of DC loads:

- The power converter is of DC / DC type (e.g. Buck, Boost, Cúk etc.).

- The control unit of the DC / DC converter generates appropriate control signals to the converter (usually according to Pulse Width Modulation) in order to regulate the output voltage of the converter to the desired value.

- The control unit of the DC / DC converter executes an algorithm to maximize the energy produced by the PV array (Maximum Power Point Tracking, MPPT).

- The control unit of the converter DC / DC executes an algorithm for management of the energy produced (e.g. regulating battery charging process).

In case of AC loads:

- The power converter is of DC / AC type.
- The control unit of the DC / AC inverter generates appropriate control signals to the converter (usually according to Sinusoidal Pulse Width Modulation, SPWM) in order to regulate the output voltage of the converter to the desired value.
- The control unit of the DC / AC inverter executes an algorithm to maximize the energy produced by the PV array (Maximum Power Point Tracking, MPPT).
- The control unit of the DC / AC inverter algorithm executes an algorithm for the management of the energy produced (e.g. stopping the diversion of part of the energy to the grid during specified time periods).

The topologies of DC / DC and DC / AC power converters are different; the circuit of a DC / DC power converter cannot be used to implement a DC / AC inverter and vice versa. So, depending on the type of the load that will be powered and its operating specifications (depending on the application) it should be:

1. Construct a specialized circuit of a power converter (DC / DC or DC / AC, respectively)
2. The individual functions of the control unit should be tailored to the specifications of the particular power converter that has been developed and the requirements of the application.

Thus, a Reconfigurable Power Conditioner can be developed consisting of:

1. A power converter circuit which is reconfigurable so it can function either as a controlled DC / DC converter, or as a controlled DC / DC inverter, depending on the type of load that will be power-supplied.
2. A controller based on FPGA, which will run the control algorithms of the power converter, in order to maximize the power produced by the PV modules and perform the

management of energy produced. The architecture of the digital circuits implemented in the control unit will re-arrange itself to fit the operational requirements of the:

- Reconfigurable power converter
- PV array used
- The fed load (all three can be different in each application).

The programming function of the Reconfigurable Power Regulator will be made by the user through the power lines of the PV array (power line carrier communication) using an appropriate communication interface which will be developed.

This idea can be extended to cover even the wind systems. In these systems, controlled power inverters of both AC / DC and AC / AC types are used depending on the type of load (DC or AC). The general operations of the control unit of the power circuit are the same as above (control of the power converter, maximize the output power and power management).

With this proposed solution:

1. The user of an electrical power production PV system is provided with flexibility to alter the function depending on the application as if the type of the powered load (DC ↔ AC) is changed, this does not require the purchase of new, specialized equipment. Moreover, it helps reduce the cost of installation of PV systems that re-use existing equipment.

2. Flexible / "Smart" systems for PV energy management can be developed that e.g. during time intervals that the power provision for charging batteries (DC load) is not required (e.g. when they are fully charged), then the PV power system itself is rearranged and alters its operation in order to provide the excess energy into the electric grid (AC load).

3. Industrial manufacturers of power converters for PV applications acquire flexibility to construct only one type of power converter (any power converter consists of the power circuit and control unit), which with proper programming can be used throughout the possible range of PV applications. This results in reduction of manufacturing costs and increase of the economic benefits resulting from the commercialization of these converters.

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