Technical University of Crete
Department of Electronic & Computer Engineering

Master Thesis

"Ultra-Low Voltage Analog Design Techniques"

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To my family, my friends and myself

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Table of Contents

List of Figures

List of Tables

Abstract

The purpose of this work is the design of a fully differential gate-input operational transconductance amplifier in two low supply voltages, 1V and 0.5V. The design procedure is based on specific low-voltage techniques such as Drain-Bulk and Grounded-Gate MOSFET connection. For these configurations, real measurements have been performed in order to analyze and investigate their behavior in designing analog circuits. Another interesting technique, which is used in the designs of this work, is the body forward bias of the MOS devices in order to lower the threshold voltage. This technique results in a larger gate effective voltage V_{EFF}, which is important for biasing current mirrors in the onset of strong inversion.

Moreover, the basic characteristics of NMOS and PMOS drain-bulk connected transistors for ultra-low voltage applications are demonstrated in this work. On-wafer measurements as well as TCAD simulations have been performed for 180nm and 45nm technology nodes. The charge-based explicit MOS transistor model is used to provide an analysis in weak-moderate inversion, showing that output characteristics are well-controlled and dominated by the substrate effect. Furthermore, simulations with the EKV3 MOSFET compact model following a parameter extraction are performed, with the simulation results being very close to real measurements and TCAD simulated data.

The amplifiers that are proposed in this work have been designed for two low supply voltages, 1V and 0.5V. These amplifiers are used to design and implement an ultra-low voltage 5^{th}-order low-pass elliptic filter.

The analog circuits have been simulated in Cadence Tool using Spectre simulator. The design kit that used for amplifiers and filters design has been developed by the team in our lab at 0.18 CMOS process based on the EKV2.6 MOSFET model. This model has been extracted and developed in our lab as well. Finally, it must be pointed out that the wafer that used for measuring the devices has been provided by EM Microelectronic Marin.

CHAPTER 1: MOS Devices – Characterization and Modeling

This chapter briefly presents the basic theory of the MOS devices and describes the EKV model that has been used in designing many types of analog building blocks such as current mirrors, differential pairs and more complicated analog circuits like Operational Transconductance Amplifiers. Furthermore, in this chapter, two different configurations of MOS transistors (Drain-Bulk and Grounded-Gate MOS) are presented and discussed.

1.1 The MOSFET device

Nowadays, transistors are the basic elements of integrated circuits (ICs). The major difference between transistor and passive elements (resistors, capacitors, inductors and diodes) is that the transistor's current and voltage characteristics depend on the voltage (or current) on a control terminal. There are two types of transistors with different physical principles: the bipolar transistors and field effect transistors (FETs). One type of bipolar transistor exists and specifically the bipolar junction transistor (BJT), and two types of FET transistors-the junction field effect transistor (JFET) and the metal oxide semiconductor field effect transistor (MOSFET). Today the BJT transistors are used in specific digital technologies and more generally in analog circuits, the JFETs have specific application and are not used in digital applications but MOSFETS appear in more than 90% percent of digital ICs application.

MOSFETs have three signal terminals: gate (G), source (S) and drain (D), plus a bulk terminal (B) to which the gate, drain and source voltages are referenced. Fig. 1.1 (a) shows a three dimensional representation with its four terminals and its insulator (with thickness T_{ox}) between gate and bulk and Fig. 1.1 (b) shows the commonly used symbols for MOSFETs, where the bulk terminal (B) is either labeled or implied. There are two types of MOSFET transistor, the NMOS and PMOS, depending on the polarity of the carries responsible for conduction.

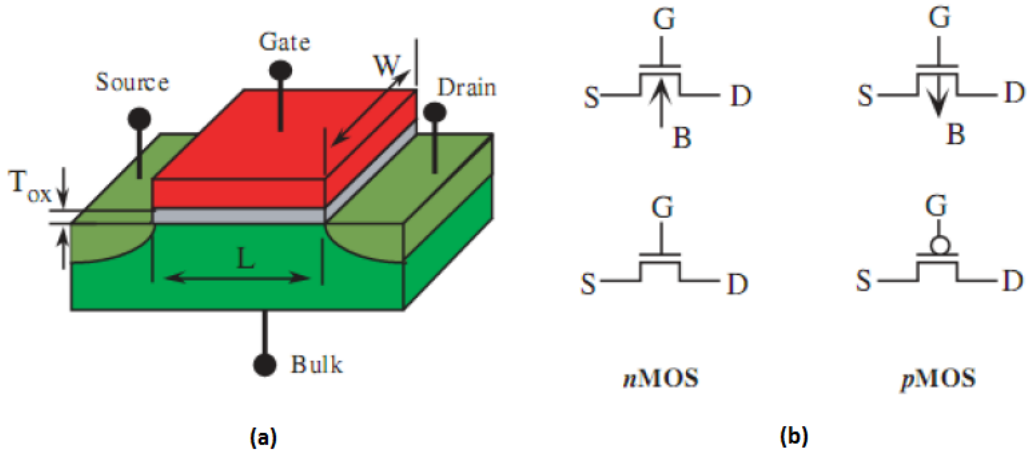


Fig. 1.1: (a) MOS structure (b) Symbols used at the circuit level

1.1.1 Physical Structure of MOSFET

The MOSFET transistors are made from a crystalline semiconductor that forms the host structure called the substrate or bulk of the device. The thin oxide of the transistor electrically isolates the gate from the

semiconductor crystalline structures underneath. Drain and source regions are made from crystalline silicon by implanting a dopant with polarity opposite to that of the substrate.

The region between the drain and source is called the channel and the distance from the drain to the source is a geometrical parameter called channel length (L) of the device. There is also the transistor channel width (W). These two parameters are defined by the circuit designer and are shown in Figure 1.1(a). However some other parameters, such as the transistor oxide thickness, threshold voltage, and doping levels, depend on the fabrication process, and cannot be changed in the design level-they are technology parameters.

The gate is the control terminal, and the source provides electron or hole carriers that are collected by the drain. Often, the bulk terminals of all transistors are connected to the ground or power rail that is often the source and, therefore, not explicitly drawn in most schematics. The gate is electrically isolated from the drain, source, and channel by the gate oxide insulator.

Figure 1.2 shows NMOS and PMOS transistor structures. The NMOS transistor has a p-type silicon substrate with opposite doping for the drain and source. PMOS transistors have a complementary structure with an n-type silicon bulk and p-type doped drain and source regions. Since drain and source dopants are opposite in polarity to the substrate (bulk), they form p-n junction diodes (Fig. 1.2) that in normal operation are reverse-biased.

Fig. 1.2: Relative doping and equivalent electrical connections between device terminals for (a) NMOS and (b) PMOS transistors

1.1.2 MOSFET's operation

Transistor terminals must have proper voltage polarity so as the device can operate correctly. The bulk or substrate of an NMOS transistor (PMOS) must always be connected to the lower (higher) voltage. It is assumed that the bulk and source terminals are connected in order to simplify the description. (Fig. 1.3)

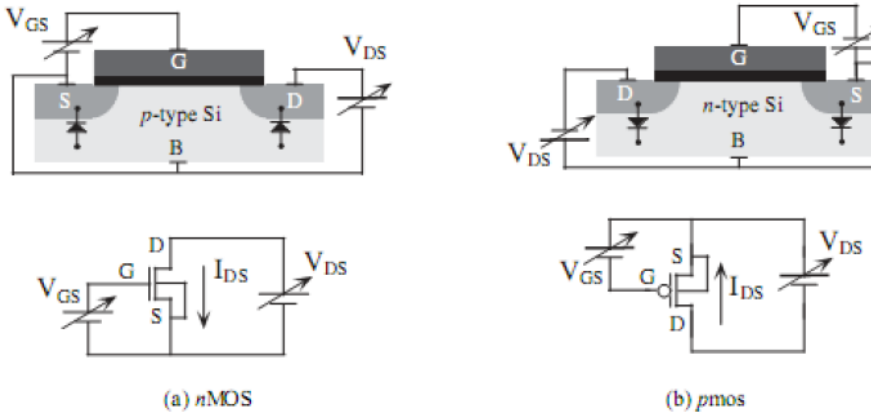
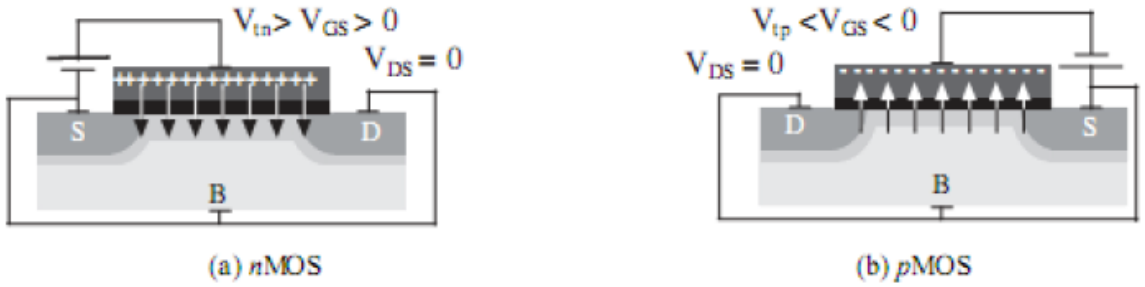


Fig. 1.3: Normal transistor biasing (a) NMOS and (b) PMOS

The positive convention current in an NMOS (PMOS) device is from the drain (source) to the source (drain), and is referred to as I_{DS} or just I_D (drain and source current are equal). When a positive (negative) voltage is applied to the drain terminal, the drain current depends on the voltage applied to the gate control terminal (for PMOS transistors, V_{GS}, V_{DS}, and I_{DS} are negative). If V_{GS} is zero, then an applied drain voltage reverse-biases the drain–bulk diode (Fig. 1.3), and there are no free charges between the drain and source. As a result, there is no current when V_{GS}= 0 for NMOS devices (the same hold for PMOS devices). This is the off, or non-conducting, state of the transistor.

At first the transistor operation when the source and substrate are at the same voltage is analyzed. When the voltage at the gate terminal an NMOS (PMOS) device is slightly increased (decreased), a vertical electric field starts to exist between the gate and the substrate across the oxide. In NMOS (PMOS) transistors, the holes (electrons) of the p-type (n-type) substrate close to the silicon–oxide interface initially "feel" this electrical field, and move away from the interface. As a result, a depletion region forms beneath the oxide interface or this small gate voltage (Fig. 1.4). The depletion region contains no mobile carriers, so the application of a drain voltage provides no drain current, since free carriers still do not exist in the channel.



(a) *n*MOS (b) *p*MOS

Fig. 1.4: (a) Depleting the NMOS channel of holes with small positive values of gate–source voltage, and (b) depleting the PMOS channel of electrons with small negative values of gate–source voltage

If the gate voltage of the NMOS (PMOS) device is further increased (decreased), then the vertical electric field is strong enough to attract minority carriers (electrons in the MOS device and holes in the PMOS device) from the bulk toward the gate. These carriers are attracted to the gate, but the silicon dioxide insulator stops them, and the electrons (holes) accumulate at the silicon– oxide interface. They form a conducting plate of mobile carriers (electrons in the p-type bulk of the NMOS device, and holes in the n-type bulk of the p-MOS device). These carriers form the inversion region or conducting channel, which can be viewed as a "short circuit" to the drain/source-bulk diodes. This connection is shown in Fig. 1.5.

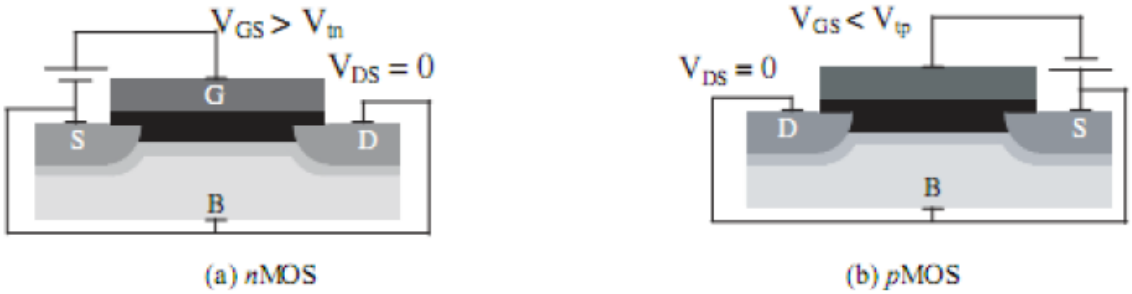


Fig. 1.5: Creating conducting channel for (a) NMOS and (b) PMOS transistors.

Since the drain and source are at the same voltage, the channel carrier distribution is uniform along the device. The gate voltage for which the conducting channels respond is an intrinsic parameter of the transistor called the threshold voltage, referred to as V_{th}. As an approximation, V_{th} can be considered constant for a given technology. The threshold voltage of a NMOS transistor is positive, while for a PMOS transistor it is negative. Since NMOS and PMOS transistors have different threshold voltages, Vthn refers to the NMOS transistor threshold voltage and V_{thp} to the PMOS transistor. An NMOS (PMOS) transistor has a conducting channel when the gate–source voltage is greater than (less than) the threshold voltage, i.e., $V_{GS} > V_{thn}$ ($V_{GS} < V_{thp}$). When the channel forms in the NMOS (PMOS) transistor, a positive (negative) drain voltage with respect to the source creates a horizontal electric field, moving the channel carriers toward the drain and forming a positive (negative) drain current. If the horizontal electric field is of the same order or smaller than the vertical one, the inversion channel remains almost uniform along the device length. This happens when:

$$V_{DS} < (V_{GS} - V_{Tn}) \quad NMOS\ transistor$$
$$V_{DS} > (V_{GS} - V_{Tp}) \quad PMOS\ transistor$$

The above conditions state that the vertical electric field dominates the horizontal one. The transistor is in its linear region, also called the ohmic or non-saturated region. If the drain voltage increases beyond the limit of Equation (1.1), the horizontal electric field becomes stronger than the vertical field at the drain end, creating an asymmetry of the channel carrier inversion distribution. The drain electric field is strong enough so that carrier inversion is not supported in this local drain region. The conducting channel retracts from the drain, and no longer “touches” this terminal. When this happens, the inversion channel is said to be “pinched off” and the device is in the saturation region. The pinch-off point is the location that separates the channel inversion region from the drain depletion region. It varies with changes in bias voltages. The channel distribution in this bias is shown in Fig. 1.6.

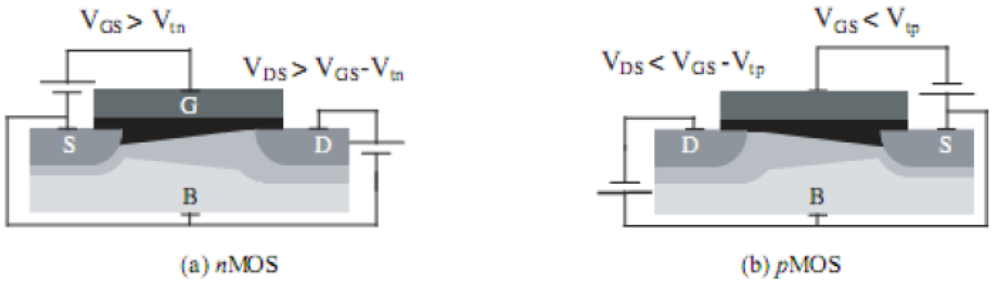


Fig. 1.6: Channel pinch-off for (a) NMOS and (b) PMOS transistor devices.

Although there are no inversion charges at the drain end of the channel, the drain region is still electrically active. Carriers depart from the source and move under the effect of the horizontal field. Once they arrive at the pinch-off point of the channel, they travel from that point to the drain, driven by the high electric field of the depletion region. CMOS ICs use all three states described here: off-state, saturated state, and the linear state.

1.2 MOSFET Modeling

Nowadays, with the explosive growth of the IC industry and modern large-scale integrated circuits, the modeling of MOSFETs has raised in a big issue among the scientific and industry communities.

The models are used widely by the IC designers, who rely on simulations of their design before building a prototype and thus the models' role, which provide a mathematical description of the element behavior in the circuit, becomes very important. Specifically, the accuracy of the results which come from the simulations depends on the quality of the element models, which means that the integrated circuit will behave as the designed ones.

For non critical digital circuits, this model may in principle be very simple. It would be sufficient to model each transistor as an on-off switch in order to design purely logic circuits. However, there are critical races among transitions, so the model must be extended to describe the dynamic behavior of the device, in order to obtain the rise and fall time of these transitions. This dynamic behavior is also needed when the frequency of operation approaches its maximum limit.

Analog circuits may contain a smaller number of transistors than digital ones, but they are more dependent on the exact behavior of each transistor. The design of high-performance analog circuits requires a very detailed model of the transistor. This model must include a precise description of the voltage-current relationships, including the effect of the source that is often not grounded, and of the dynamic behavior of the device. Its behavior with respect to noise and to temperature variations must also be accounted for.

At this point, the two categories of device models should be differentiated, namely the numerical device simulation models and compact models. Numerical device simulators are used to study the device physics and to predict the electrical, optical, and thermal behavior of the device. Numerical device simulators solve a set of (partial differential) equations associated with the physics involved in device operation but their requirements of intensive computation and huge amount of memory prevent them from being used for circuit simulations.

On the other hand, compact models describe the terminal properties of the device by means of simplified set of equations or by an equivalent circuit model.

From the above it can be concluded that the conditions for a model to be regarded as good is how correct and accurate can predict the behavior if a MOSFET and how demanding can it become, in the simulation level. A good model must be accurate and fast.

1.2.1 Compact Modeling

The purpose of a compact model is to obtain simple, fast and accurate representations of the device behavior. Compact transistor models are needed to evaluate the performance of integrated circuits containing a large quantity of transistors. MOSFET compact models fall into three categories: (a) Physical Models, based on device physics, (b) Table Lookup Models, in the form of tables containing device data for different bias points and (c) Empirical Models, which represent the device characteristics through equations that fit data. Physical models take considerable time to develop but once they become mature, their advantages are significant: parameters have physical meaning, effects of device geometry, technological parameters, and temperature can be accounted for, statistical modeling can be applied to

predict ranges of expected performance and, in many cases, the model can be applied to different generation technologies by simply changing parameters.

1.3 EKV3 Model

1.3.1 A charge-based model

The requirements for good MOS analog simulation models such as accuracy and continuity of the large and small signal characteristics are well established. The EKV3 MOSFET model has been designed in order to have computational efficiency, ease of parameter extraction and the designer's need for insight into the device behavior.

The EKV3 is a charged-based model which first calculates the dependency of the density Q_i of induced mobile charge on the voltages applied to the transistor. Then, it relies on Q_i, and on its particular values Q_{iS} and Q_{iD} at the source and drain ends of the channel, to calculate the drain current and to model all aspects of the device behavior. Below an analysis without going into much detail follows.

For zero electric field at the silicon surface, the source to drain structure of Fig. 1.7 corresponds to two back-to-back diodes connected in series; thus, no current other than the junction leakage current can flow as long as V_S and V_D are positive. The situation remains qualitatively the same when more holes are attracted at the surface by applying a negative gate voltage V_G.

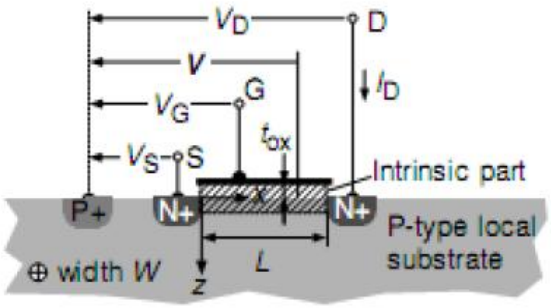


Fig. 1.7: Cross section of a MOS transistor

On the contrary, if a positive voltage is applied to the gate, the holes are forced away from the surface, leaving the negatively charged P-doping atoms. As shown schematically in Fig. 1.8, this corresponds to a negative charge of density Q_b per unit area. This charge is fixed and therefore cannot carry any current. By further increasing V_G, negative electrons are attracted to the surface thereby forming an N-type channel. It is this negative mobile inversion charge, of density Q_i per unit area, which will carry the drain-to-source current by a combination of drift and diffusion mechanisms of electrons. For the N-channel device, this current ID will be defined positive if it enters the drain terminal.

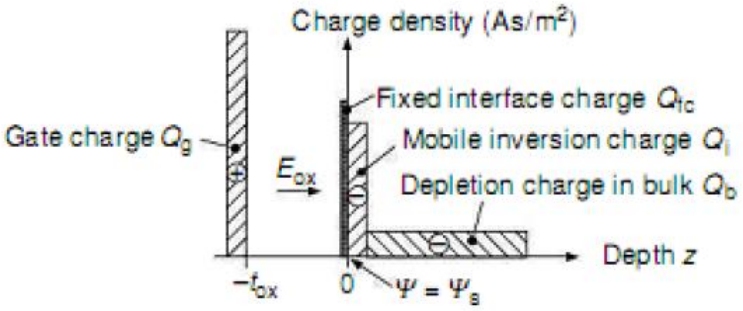


Fig. 1.8: Representation of various local charge densities

1.3.2 Surface Potential and Inversion Charge Modeling

The total channel density $Q_C^{'}$ in an infinitesimal piece of the channel is found by applying Gauss' law,

$$Q_C^{'} = -C_{OX}^{'} \cdot (V_G - V_{FB} - \Psi_S) \quad (1.1)$$

where Ψ_S is the surface potential, $C_{OX}^{'} = \varepsilon_{OX} / T_{OX}$ the oxide capacitance per unit area, and V_{FB} the flat-band voltage. The bulk depletion charge $Q_B^{'}$ is given by,

$$Q_B^{'} = -\sqrt{2q\varepsilon_{si} N_{sub} \Psi_S} \quad (1.2)$$

and ε_{OX} and ε_{si} are the permittivities of silicon and silicon dioxide, respectively. The gate oxide thickness T_{OX} and the substrate doping concentration N_{sub}, together with V_{FB} are the main actual physical parameters describing the NMOS technology.

Inversion charge is then expressed as,

$$Q_I^{'} = Q_C^{'} - Q_B^{'} = -C_{OX}^{'} \cdot \left(V_G - V_{FB} - \Psi_S - \gamma \sqrt{\Psi_S} \right) \quad (1.3)$$

where $\gamma = \sqrt{2q\varepsilon_{si} N_{sub}} / C_{OX}^{'}$ is the substrate effect parameter. Linearizing the inversion charge versus surface potential provides the inversion charge linearization factor n_q,

$$n_q \equiv \frac{\partial \left(Q_I^{'} / C_{OX}^{'} \right)}{\partial \Psi_S} = 1 + \frac{\gamma}{2\sqrt{\Psi_S}} \quad (1.4)$$

Neglecting, on the other hand, inversion charge density in (1.3) provides the pinch-off surface potential Ψ_P [3, 4, 14, 15],

$$\Psi_P = \Psi_S\big|_{Q_I^{'}=0} = V_G - V_{FB} + \gamma\left[\frac{\gamma}{2} - \sqrt{\frac{\gamma^2}{4} + V_G - V_{FB}}\right] \quad (1.5)$$

We can therefore express the inversion charge as,

$$Q_I^{'} \cong n_q \cdot C_{OX}^{'} \cdot \left(\Psi_S - \Psi_P\right) \quad (1.6)$$

We then define the pinch-off voltage V_P as [14],

$V_P \cong \Psi_P - \Psi_0$, where $\Psi_0 \cong 2\Phi_F = 2U_T \ln\left(\frac{n_i}{N_{sub}}\right)$ (1.7)

where Φ_F is the quasi-Fermi potential and n_i the intrinsic carrier concentration.

A convenient approximation of the pinch-off voltage is [3],

$$V_P \cong \frac{V_G - V_{TO}}{n} \quad \text{where } V_{TO} = V_{FB} + \Psi_0 + \gamma\sqrt{\Psi_0} \quad (1.8)$$

where n is the slope factor, $n \equiv \left[\frac{\partial \Psi_P}{\partial V_G}\right]^{-1} = 1 + \frac{\gamma}{2\sqrt{\Psi_P}}$ (1.9)

1.3.3 Drain Current

The MOS transistor drain current in the context of the EKV model is expressed as [3],

$$I_D = I_F - I_R = I_{SPEC} \cdot \left(i_f - i_r\right) (1.10)$$

where the specific current is the normalization current given by,

$$I_{SPEC} = 2 \cdot n \cdot \beta \cdot U_T^2 (1.11)$$

where $\beta = \mu C_{ox}^{'} W/L$ is the gain factor, and W and L the device width and length respectively. i_f and i_r are the symmetric forward and reverse normalized currents. Each of these currents is related to inversion charge densities q_s and q_d at source and drain [4],

$$i_{f(r)} = q_{s(d)}^2 + q_{s(d)} (1.12)$$

which in turn relate to the terminal voltages [4],

$$v_p - v_{s(d)} = 2 \cdot q_{s(d)} + \ln(q_{s(d)}) \quad (1.13)$$

Terminal voltages are normalized to the thermodynamic potential $U_T = kT/q$,

$$v_p = V_P / U_T \qquad v_{s(d)} = V_{S(D)} / U_T$$

where the pinch-off voltage V_P and slope factor n are function of the gate voltage [3],

$$V_P \cong \frac{V_G - V_{TO}}{n} \qquad n \equiv \frac{dV_G}{dV_P} = 1 + \frac{\gamma}{2 \cdot \sqrt{V_P + \phi}}$$

In the above, V_{TO} is the threshold voltage, γ the substrate factor and Φ amounts to twice the Fermi potential.

1.3.4 Transconductances

The relationship among transconductance and inversion charge densities at source and drain is immediate [3, 4],

$$g_{ms} = Y_{spec} \cdot q_s$$
$$g_{md} = Y_{spec} \cdot q_d$$

where $Y_{spec} = 2n\beta U_T$.

Noting the relationships among normalized current and charge, the important relationship among transconductance and normalized current is established [16],

$$\frac{g_{ms} U_T}{I_D} = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + i_f}} \qquad \frac{g_{md} U_T}{I_D} = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + i_r}}$$

This work aims to demonstrate the basic characteristics of NMOS and PMOS drain-bulk connected transistors for ultra-low voltage applications. On-wafer measurements as well as TCAD simulations have been performed for 180nm and 45nm technology nodes. The charge-based explicit MOS transistor model is used to provide an analysis in weak-moderate inversion, showing that output characteristics are well-controlled and dominated by the substrate effect. Furthermore, simulations with the EKV3

MOSFET compact model following a parameter extraction are performed, with the simulation results being very close to real measurements and TCAD simulated data.

The MOS transistor, with its tremendous improvements in downscaling and hence in functionality and speed performance, constitutes the main driving force of modern consumer electronics. The regions of weak and moderate inversion that, with a few brilliant exceptions, were previously ignored or even unknown, are now becoming the much desired ones for MOS transistor. Using the inversion coefficient permits design in all regions of MOS operation, including moderate inversion. Moderate inversion [1], a transitional region spanning nearly two decades of drain current between weak and strong inversion, as described in Section II below, has become increasingly important in modern design. This is because it offers a compromise of high transconductance (high transconductance efficiency), low drain-source saturation voltage, minimal velocity saturation degradation of transconductance, and moderate bandwidth necessary for power-efficient, low-voltage design.

Several ultra-low voltage design techniques, such as forward biasing of the body-source junction, have been proposed [2] for low voltage digital circuits and have been applied to lower the threshold voltage V_T of the transistors. In the context of low voltage operation, such as 0.5 V or below, the risk of forward biasing of the junctions is minimized since parasitic bipolar devices cannot be activated even when the full power supply is used as forward bias. These techniques are discussed in Chapters 2 and 3.

1.4 Low-Voltage MOSFET configurations

1.4.1 Source-Bulk and Drain-Bulk Connected MOS transistors

As shown in Fig. 1.9, either NMOS or PMOS transistors may be used with the somewhat unusual drain-bulk connection, instead of the conventional source-bulk connection (where 'bulk' may stand for the local substrate or well). For the NMOS transistors, a triple-well technology would be presupposed.

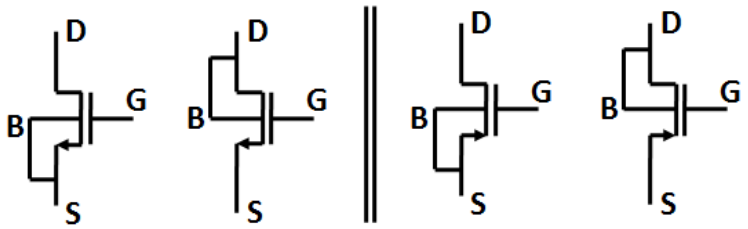


Fig. 1.9: NMOS (left) and PMOS (right) transistors, with their local substrate (or well) connected to either source or drain.

The drain current of the NMOS transistors biased in weak inversion is given by the EKV model [7] – [9] as:

$$I_{DS} = I_{SPEC} \cdot e^{\frac{V_{GB}-V_{TO}}{nU_T}} \cdot \left[e^{\frac{V_{SB}}{U_T}} - e^{\frac{V_{DB}}{U_T}} \right] (1.14)$$

For the conventional device where V_{BS}=0, the relation (1.14) becomes:

$$I_{DS} = I_{SPEC} \cdot e^{\frac{V_{GB}-V_{TO}}{nU_T}} \cdot \left[1 - e^{\frac{V_{DB}}{U_T}} \right]$$

$$\Leftrightarrow I_{DS} = I_{SPEC} \cdot e^{\frac{V_{GS}-V_{TO}}{nU_T}} \cdot \left[1 - e^{\frac{V_{DS}}{U_T}} \right] (1.15)$$

On the contrary, for the drain-bulk connected device, where $V_{DB} = 0\ V$, the relation (1.14) becomes:

$$I_{DS} = I_{SPEC} \cdot e^{\frac{V_{GB}-V_{TO}}{nU_T}} \cdot \left[e^{\frac{V_{SB}}{U_T}} - 1 \right]$$

$$\Leftrightarrow I_{DS} = I_{SPEC} \cdot e^{\frac{V_{GS}-V_{TO}}{nU_T}} \cdot \left[e^{\frac{-V_{DS}}{U_T} \cdot \frac{n-1}{n}} - e^{\frac{V_{DS}}{nU_T}} \right] (1.16)$$

The output small signal conductance g_{SD} and resistance r_{SD} are defined as:

$$g_{DS} = \frac{\partial I_{DS}}{\partial V_{DS}},\ r_{DS} = \frac{1}{g_{DS}} = \left[\frac{\partial I_{DS}}{\partial V_{DS}} \right]^{-1}$$

Assuming long-channel behavior, i.e. neglecting drain voltage dependence of the threshold voltage, slope factor and I_{SPEC}, $\delta V_{TO}/\delta V_{SD}$=0, $\delta n/\delta V_{SD}$=0, $\delta I_{SPEC}/\delta V_{SD}$=0, we have for the conventional device:

$$g_{DS,S=B} = \frac{I_{SPEC}}{U_T} e^{\frac{V_{GS}-V_{TO}}{nU_T}} \cdot \left[e^{\frac{V_{DS}}{U_T}} \right] (1.17)$$

whereas for the drain-bulk connected device,

$$g_{DS,D=B} = \frac{I_{SPEC}}{U_T} e^{\frac{V_{GS}-V_{TO}}{nU_T}} \cdot \left[\frac{n-1}{n} \cdot e^{\frac{-V_{DS}}{U_T} \cdot \frac{n-1}{n}} + \frac{1}{n} \cdot e^{\frac{V_{DS}}{nU_T}} \right] (1.18)$$

Furthermore, we define Early voltage V_A as a quantity equal to the ratio of the drain current I_{DS} divided by the output conductance g_{DS}. We note from (1.16) and (1.18) that for the saturated drain-bulk connected NMOS transistor,

$$V_A = \frac{I_{DS}}{g_{DS,D=B}} \cong U_T \cdot \frac{n}{n-1} (1.19)$$

which means that V_A in this operating region is well-known, since n does not strongly depend on bias, and is not a strong function of channel length. The output resistance is given by the reverse of the output conductance, and therefore, we have, $r_{DS} = V_A/I_{DS}$. On the other hand, the intrinsic gain of the transistor is defined as $A_V = g_m/g_{DS}$,

$$A_V = \frac{g_m}{g_{DS}} \cong \frac{V_A}{U_T} \cdot \frac{g_m U_T}{I_D} = \frac{G(IC)}{n-1} (1.20)$$

where *G(IC)* is the well-known normalized transconductance [4] – [6].

Measurements have been made on a 180 nm wafer through IC-CAP, using a Cascade Microtech SUMMIT 10600 prober and an HP4145A Semiconductor Parameter Analyzer, in order to demonstrate the advantages of using the drain-bulk connected PMOS transistors. The drain-bulk connected PMOS have been measured with the source-drain voltage V_{SD} ranging from 0 V to 280 mV with a step size of 10 mV, and the source-gate voltage V_{SG} ranging from 250 mV to 350 mV with a step size of 25 mV. Simulations with the analytical charge-based EKV model of Equation (1.13) on the real data have been made, after extracting different sets of parameters for V_{T0}, γ and Φ, with the charge-based model simulation results being very close to real measurements. The following figures depict the output characteristics I_{SD} and g_{SD} vs. V_{SD} for two different geometries:

W/L=10um/0.18um (wide/short)

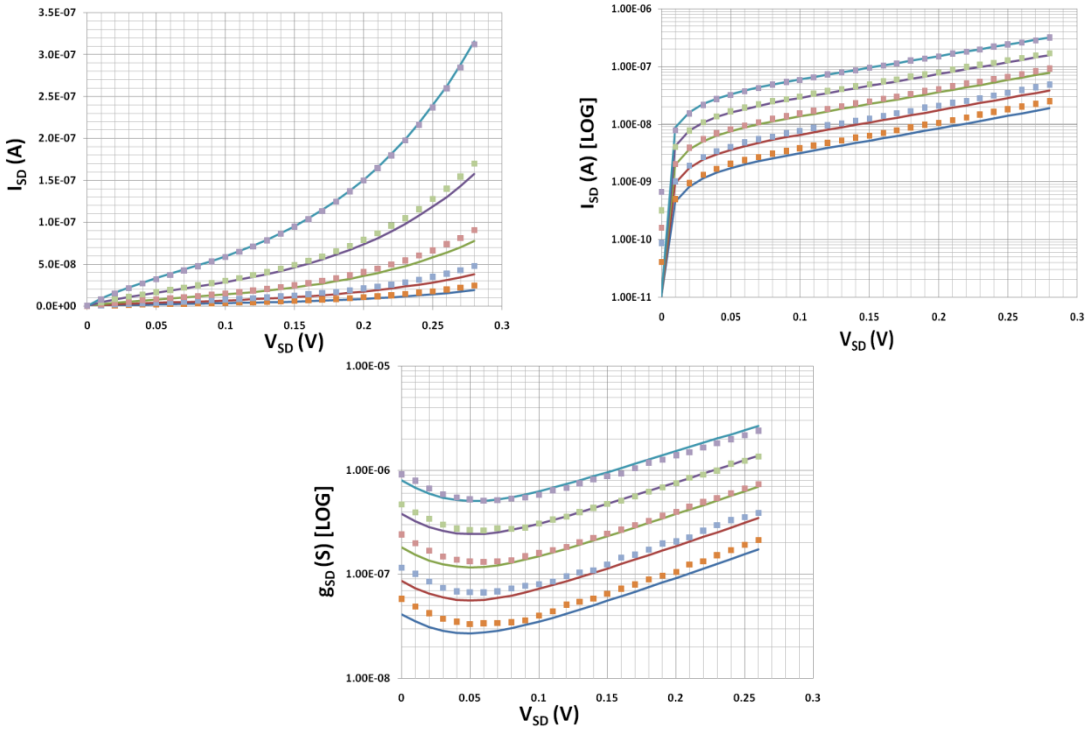


Fig. 1.10: Drain-bulk connected PMOS transistor, with respective output characteristics, W/L=10um/180nm. I_{SD}, g_{SD} vs. V_{SD} are shown for various values of V_{SG} (markers: measurements, lines: analytical charge-based model).

Fig. 1.10 illustrates that the I_{SD} vs. V_{SD} behavior and thus the output conductance g_{SD}, are dominated by the substrate effect. Drain Induced Barrier Lowering (DIBL) effect which is the usually dominant effect for output conductance in short transistors in weak inversion, is actually dominated by the substrate effect.

Fig. 1.11 below shows the Early Voltage V_A, the slope factor n extracted from Equation (1.19) and the intrinsic gain A_V of the measured drain-bulk connected PMOS device:

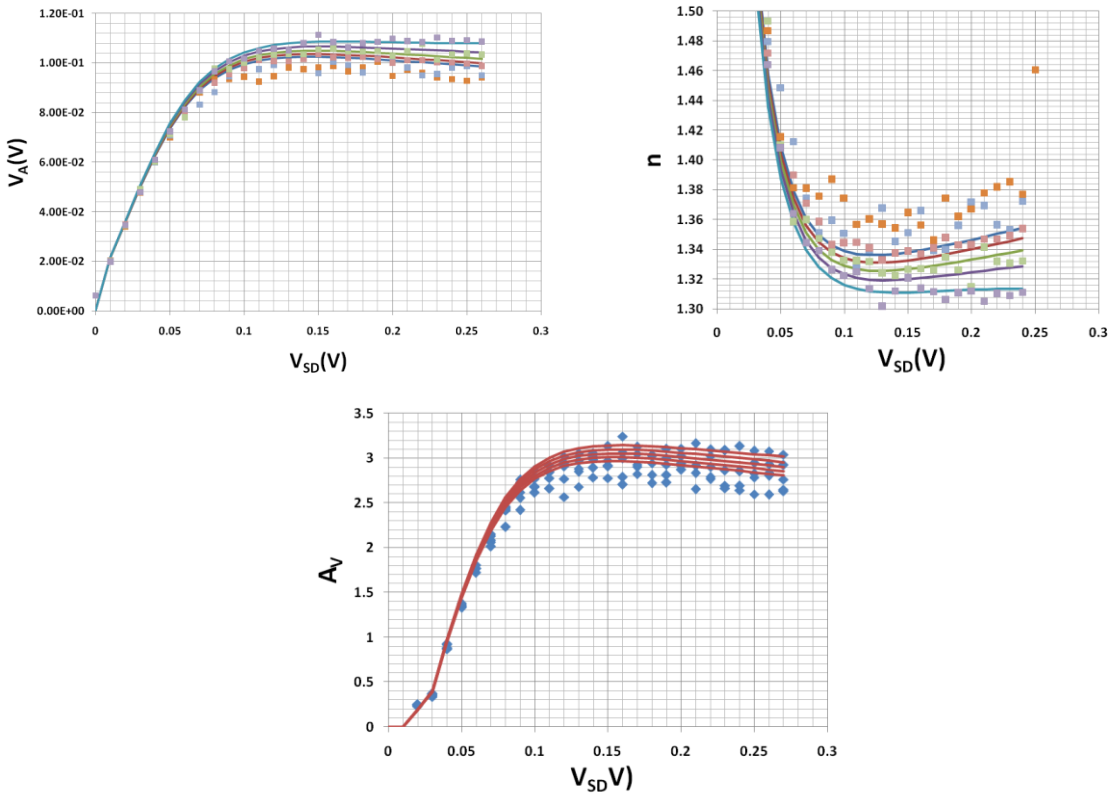


Fig. 1.11: Early Voltage V_A, Slope Factor n extracted from Equation (1.19) and Intrinsic Gain A_V of drain-bulk connected PMOS devices (markers: measured data, lines: analytical model).

As seen in Fig. 1.11 above, for any geometry we use, the Early voltage is nearly constant and independent of V_{SG}. the same result arrives for the case of the slope factor n, which is extracted from V_A using Equation (1.19) in weak inversion and saturation region. Additionally, the behavior of the intrinsic gain g_m/g_{SD} vs. $V_{SD,}$ is independent of the V_{SG} bias point and begins to remain almost constant for a low V_{SD} voltage nearly equal to 100 mV.

W/L=10um/10um (wide/long)

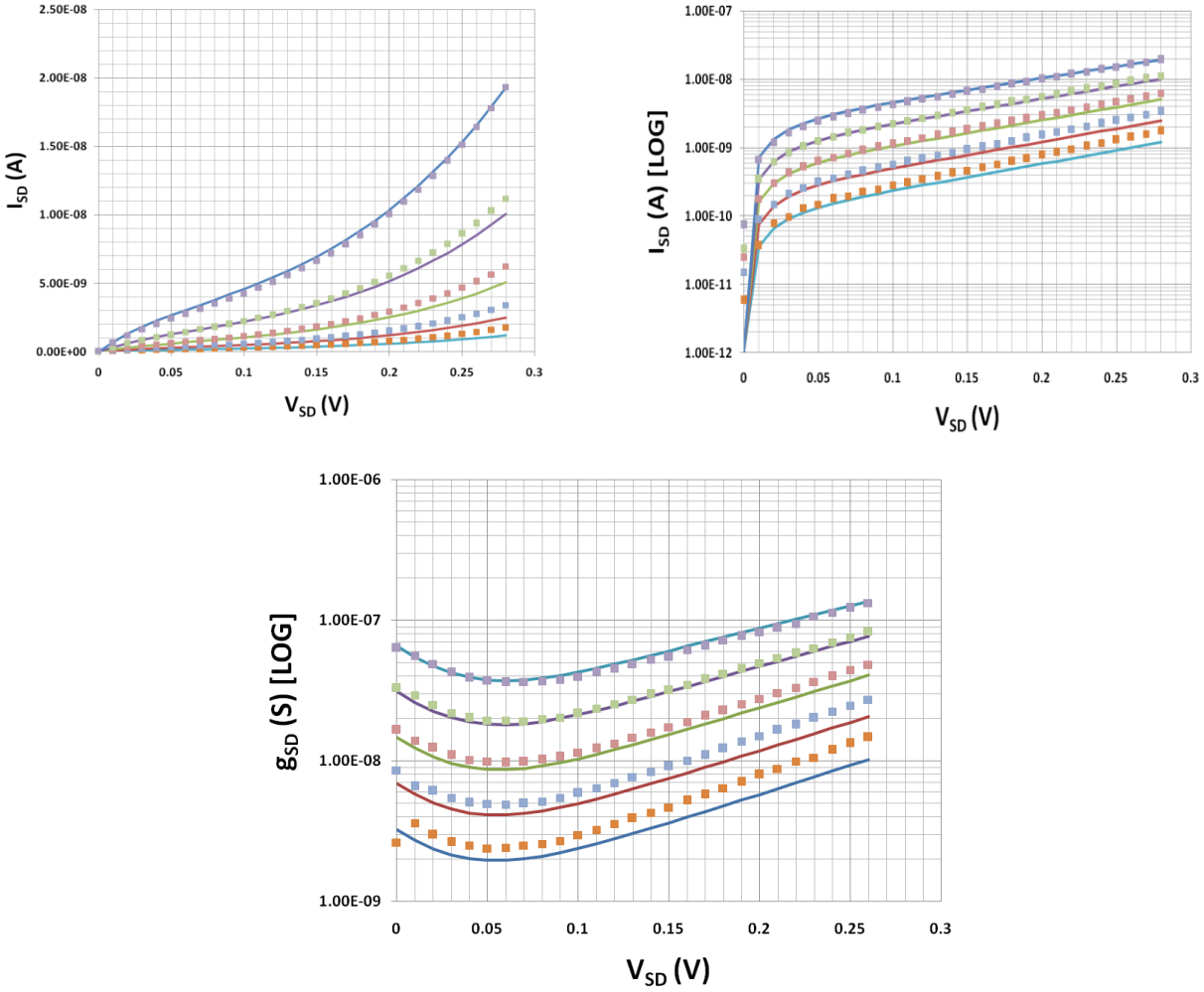


Fig. 1.12: Drain-bulk connected PMOS transistor, with respective output characteristics, W/L=10um/10um. I_{SD}, g_{SD} vs. V_{SD} are shown for various values of V_{SG} (markers: measurements, lines: analytical charge-based model)

Fig. 1.13 below shows the Early Voltage V_A, the slope factor n extracted from Equation (1.19) and the intrinsic gain A_V of the measured drain-bulk connected PMOS device:

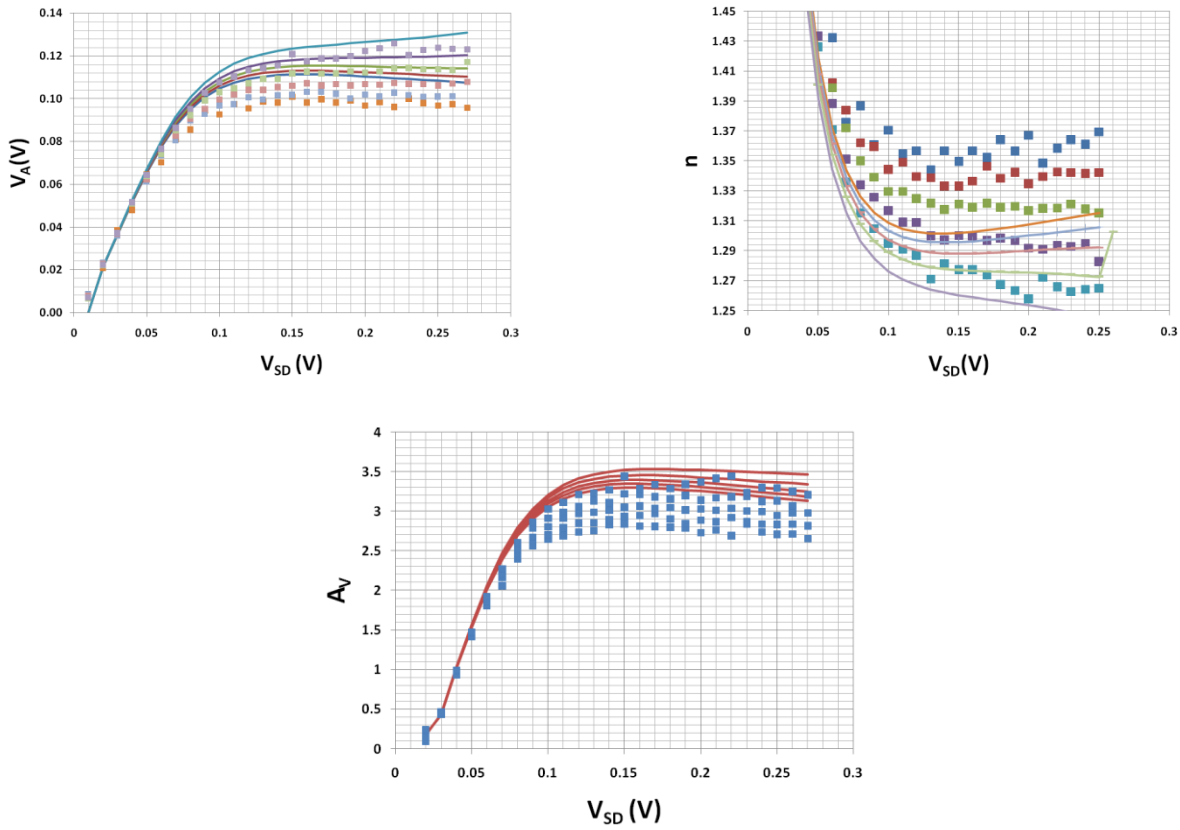


Fig. 1.13: Early Voltage V_A, Slope Factor n extracted from Equation (1.19) and Intrinsic Gain A_V of drain-bulk connected PMOS devices (markers: measured data, lines: analytical model).

At this point, the difference between long and short channel effects must be noted. For long channel devices, a one-dimensional analysis is used using the gradual channel approximation [17]. On the other hand, effects appearing when reducing the length of the transistor to dimensions that get close to the depletion width are discussed here in this section. In such a situation, the one-dimensional approach is no longer valid and two-dimensional analysis is required. Drain Induced Barrier Lowering (DIBL), Charge Sharing and Reverse Short Channel Effect (RSCE) are the main effects dominating weak inversion operation.

When the device length gets small, the surface potential in the channel region is no longer defined uniquely by the vertical field, but becomes influenced by the drain (source) voltage. This effect is called DIBL, which has important impacts in Drain-Bulk connected transistors as well as the conventional configuration.

The DIBL effect is governed by a characteristic length, L_0,

$$L_0 = n_D \cdot \sqrt{\frac{\varepsilon_{si} \cdot \gamma}{q \cdot N_{sub}}} \sqrt{\Psi_0} \quad (1.21)$$

where $n_D \cong 1$ is the main parameter for DIBL. Note the other implicit dependences of L_0 on N_{sub} and C'_{ox}, as well as temperature through the surface potential Ψ_0.

In weak inversion, the surface potential for a long channel is constant. At both ends of the channel, this potential drops from $\Phi_B + V_{S,D}$ to $\Psi_P=\Psi_0+V_P$ within a distance characterized by λ. λ is given by the ratio of channel length divided by the characteristic length L_0 of Equation (1.21),

$$\lambda = \frac{L}{L_0}$$

Φ_B, Ψ_P are the potential barrier of source and drain junctions at equilibrium and the pinch-off surface potential respectively. $V_{S,D}$, V_P are the source (drain) voltage and pinch-off voltage respectively.

For a long channel $\left(L >> L_0\right)$, this distance is negligible, and the surface potential is equal to Ψ_P over most of the channel length. On the contrary, for a short channel, the surface potential never reaches Ψ_P; the barrier for the current carriers is lowered and the current is increased. Furthermore, the amount of lowering depends on the drain voltage. Therefore, even the device is saturated, the drain current keeps increasing with the drain voltage.

For the case of Drain-Bulk connected transistors, DIBL is the main short channel effect that affects the output characteristics of the devices and therefore the performance of analog circuits. For both NMOS and PMOS transistors, the I_{DS} vs. V_{DS} behavior and thus the output conductance g_{DS}, are dominated by the substrate effect. DIBL effect which is the usually dominant effect for output conductance in short transistors in weak inversion, is actually dominated by the substrate effect.

The combination of DIBL, charge sharing and reverse short channel effect gives good results for threshold voltage modeling over channel lengths, as can be seen in Fig. 1.14 below,

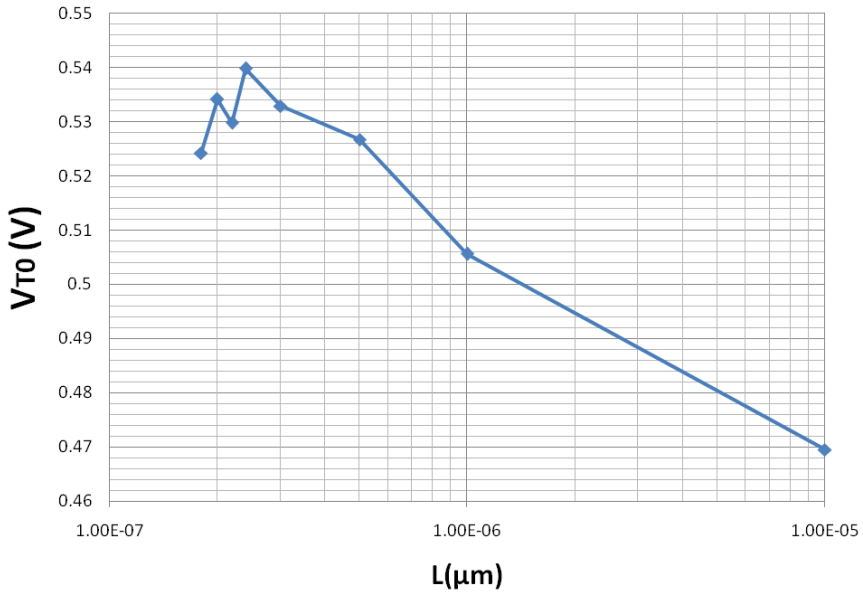


Fig. 1.14: Threshold Voltage vs. Channel Length

The previous figures show the output characteristics of Drain-Bulk connected PMOS transistors that have been measured on-wafer of 180nm CMOS technology. Simulations with the analytical charge-based EKV model have been made, after extracting different sets of parameters for V_{T0}, γ and Φ, with the charge-based model simulation results being very close to real measurements. On the other hand, the analytical charge-based model does not cover significantly all the regions of MOS operation from weak to strong inversion and therefore, the full EKV3 compact model is needed in order to cover all the effects that appear in MOS operation and affect their performance. Simulations both on Source-Bulk

and Drain-Bulk connected MOS transistors with the EKV3 MOSFET compact model following a parameter extraction are performed, with the simulation results being very close to real measurements as shown in the following figures.

Source-Bulk PMOS W/L=10um/0.18um (wide/short)

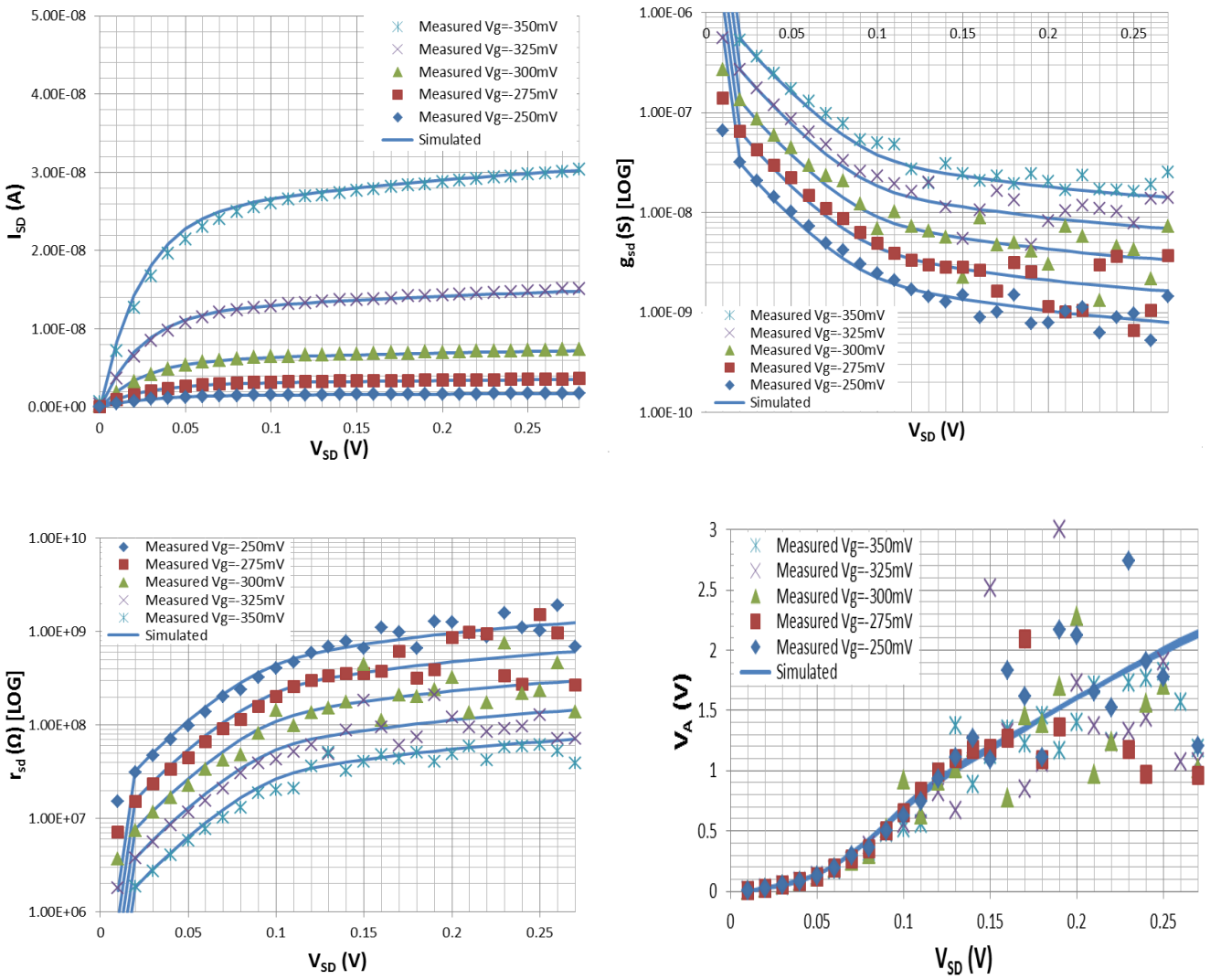


Fig. 1.15: Source-Bulk Connected PMOS W/L=10um/0.18um

As shown in Fig. 1.15, I_{SD} is almost independent of V_{SD} in saturation region, whereas the linear region of the I_{SD}-V_{SD} characteristic is restricted to the triode region of operation. Furthermore, it must be pointed out that the output resistance is almost infinite and uncontrollable even for submicron devices, whereas the Early voltage V_A is strongly dependent on V_{SD}.

Drain-Bulk PMOS W/L=10um/0.18um (wide/short)

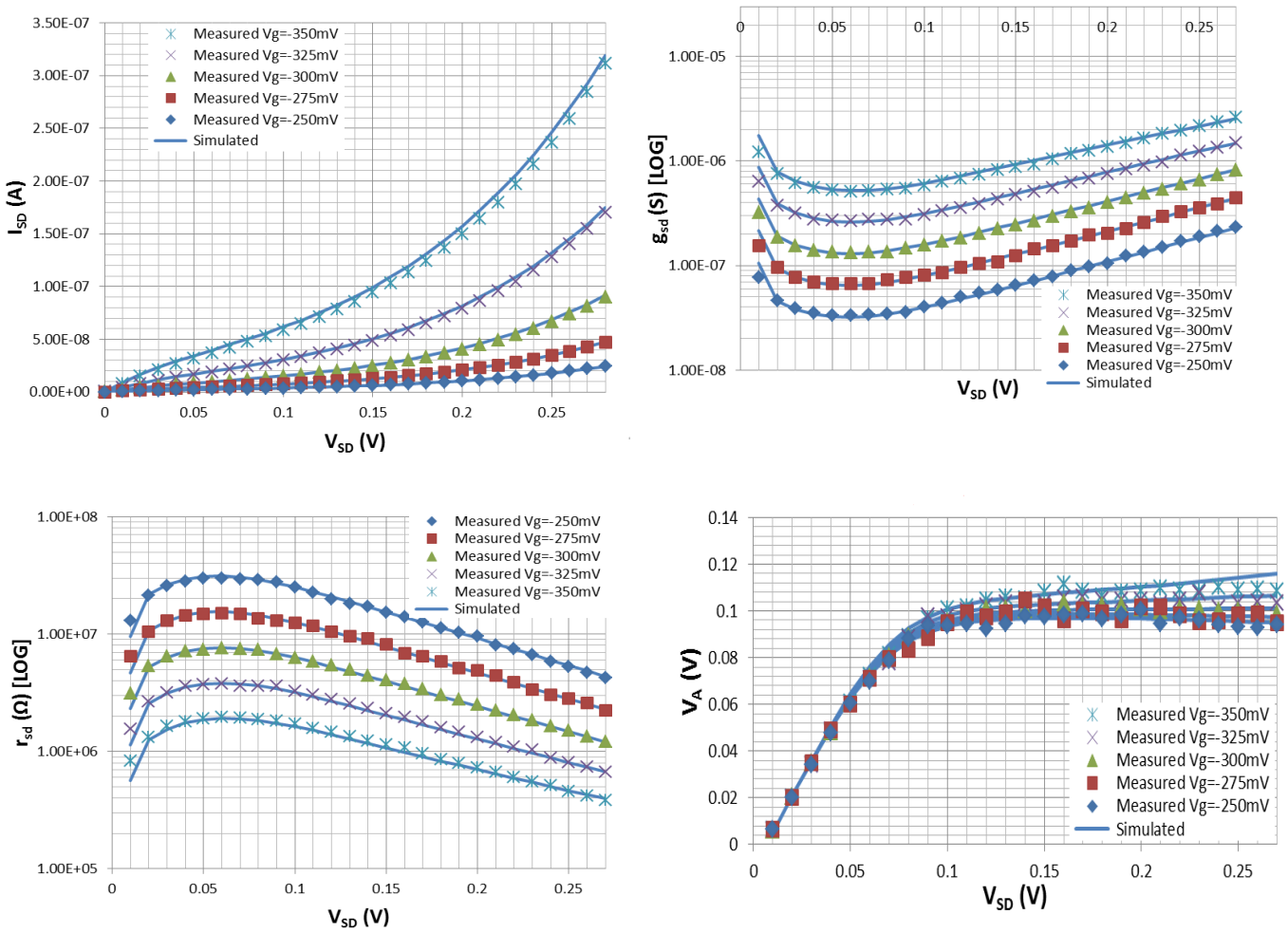


Fig. 1.16: Drain-Bulk Connected PMOS (W/L=10um/0.18um)

As depicted in Fig. 1.16, I_{SD} depends on V_{SD} in saturation region, whereas, the linear region extends to the saturation region which begins at $V_{SD}>4.U_T=104mV$. Additionally, the output resistance is finite and easily controllable and can take high values. This means that it is possible to implement a very high resistivity load device using a single minimum size PMOS.

Source-Bulk PMOS W/L=10um/10um (wide/long)

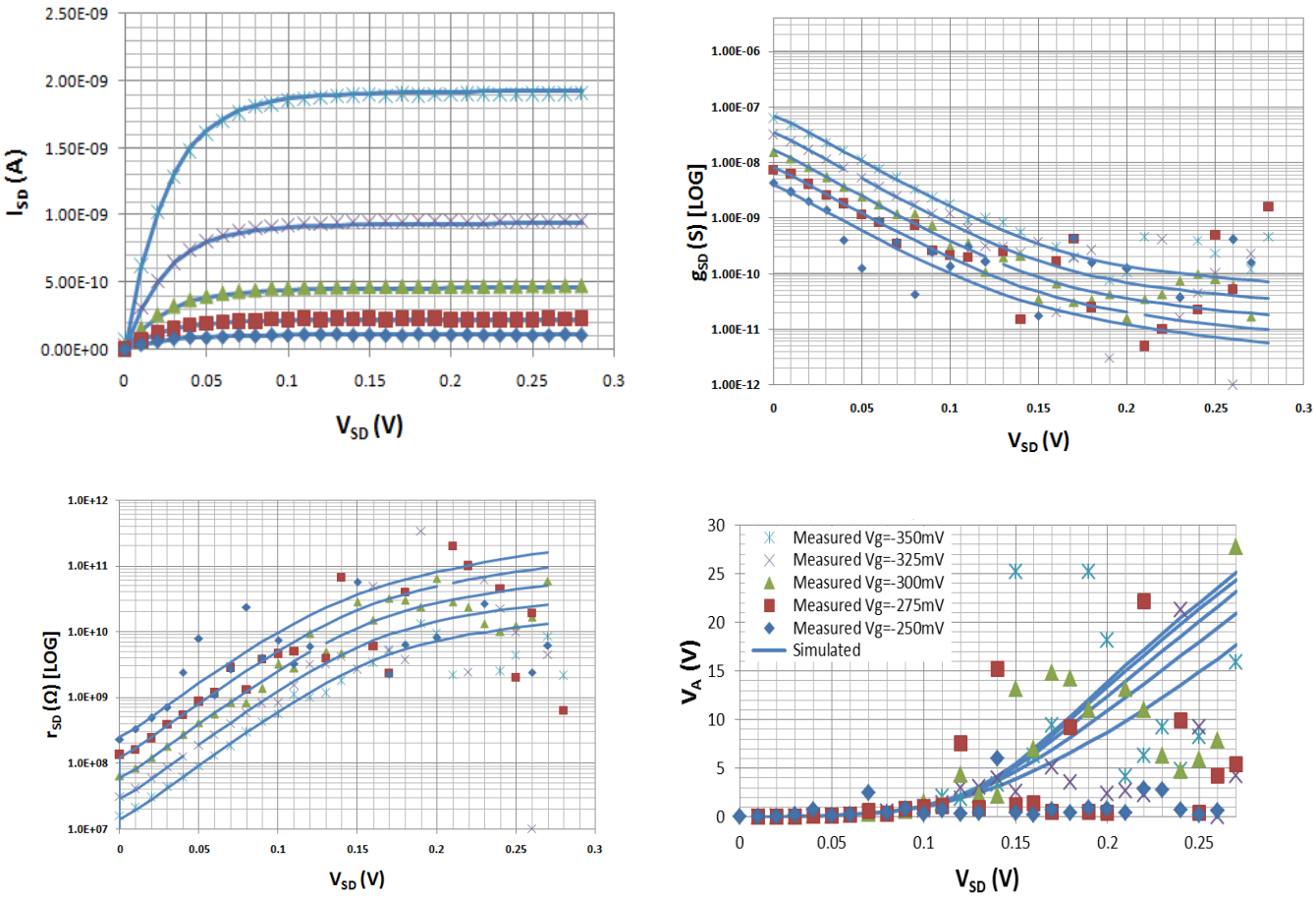


Fig. 1.17: Source-Bulk Connected PMOS W/L=10um/10um

Drain-Bulk PMOS W/L=10um/10um (wide/long)

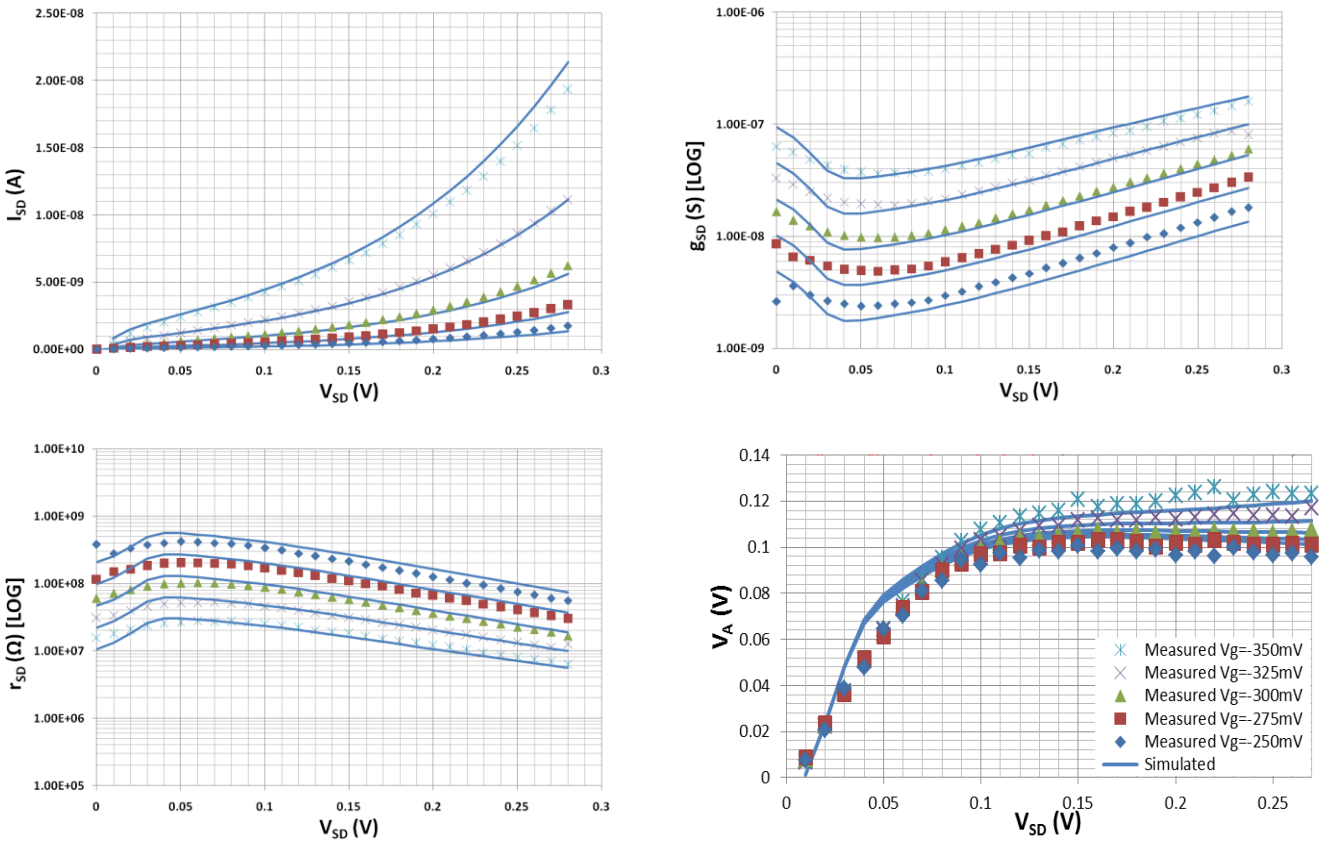


Fig. 1.18: Drain-Bulk Connected PMOS W/L=10um/10um

In addition to above measurements, simulations have been made through with the ATLAS TCAD tool for conventional and drain-bulk connected NMOS and PMOS transistors of lengths 10 μm and 180 nm and of width 1 μm. All the TCAD simulations assume a uniformly doped channel. Simulations with the analytical charge-based EKV model of Equation (1.13) on simulated TCAD results have been made, after extracting different sets of parameters for V_{T0}, γ and Φ, with the charge-based model simulation results being very close to TCAD simulated data. Furthermore, TCAD data have been imported into IC-CAP, where simulations with the EKV model version 301.02 [10] have been performed, after extracting the parameters of the model for the 180nm technology, with the simulation results being very close to TCAD simulated data. The parameter extraction was based on the procedure proposed by [11], [12]. Next sections demonstrate the output characteristics Source-Bulk and Drain-Bulk connected NMOS and PMOS devices of a 180nm technology which have been simulated through the ATLAS TCAD tool.

1.4.2 Source-Bulk and Drain-Bulk connected NMOS simulations

Fig. 1.19 below depicts the output characteristics I_{DS} vs. V_{GS} and g_m vs. V_{GS} of the conventional NMOS transistor for linear and saturation region of operation. The aspect ratio is equal to W/L=1um/10um.

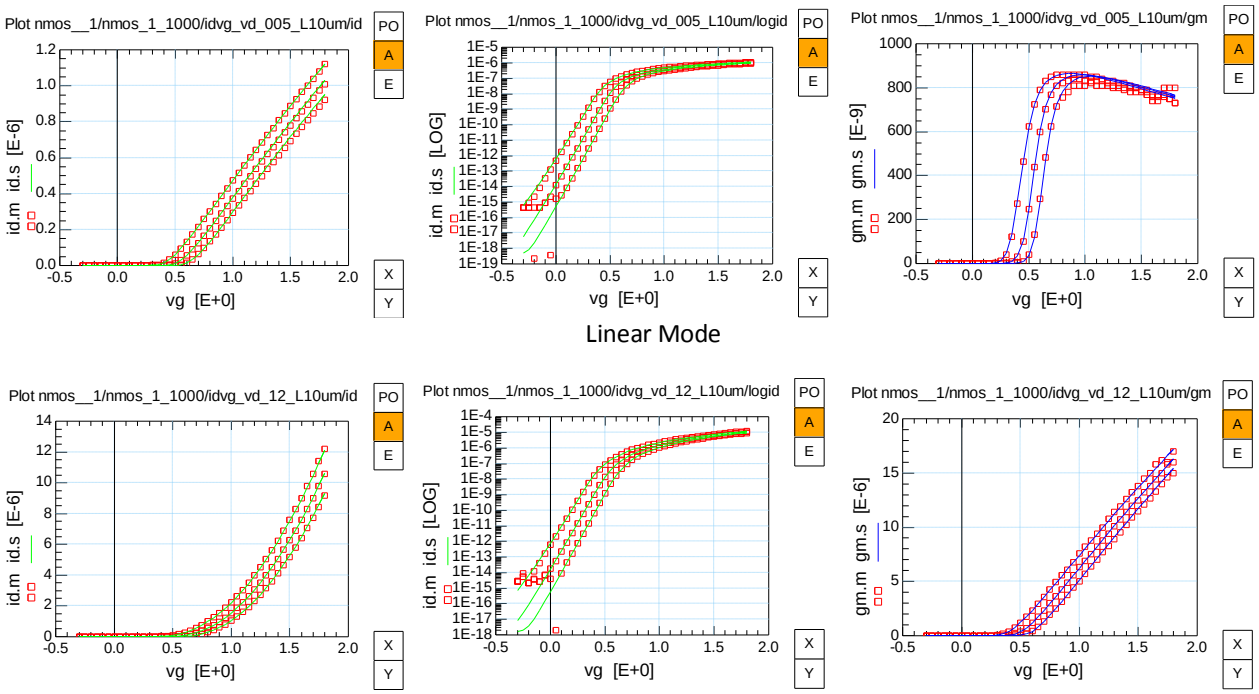


Fig. 1.19: NMOS Source-Bulk output characteristics I_{DS}, g_m vs. V_{GS} (W/L=1um/10um), linear region (up) and saturation region (down)

Additionally, Fig. 1.20 below shows the output characteristics I_{DS} vs. V_{DS} and g_{DS} vs. V_{DS} for the same configuration as mentioned above.

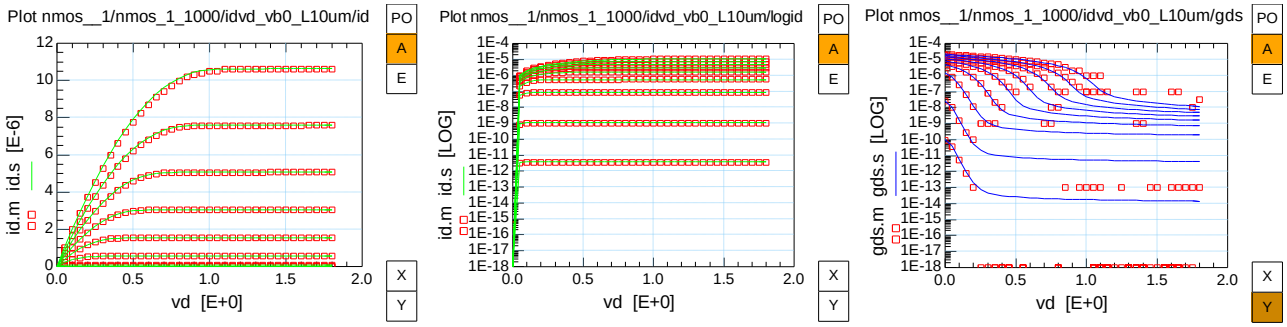


Fig. 1.20: NMOS Source-Bulk output characteristics I_{DS}, g_{DS} vs. V_{DS} (W/L=1um/10um)

On the other hand, for the drain-bulk connected NMOS topology, the output characteristics are shown in Fig. 1.21,

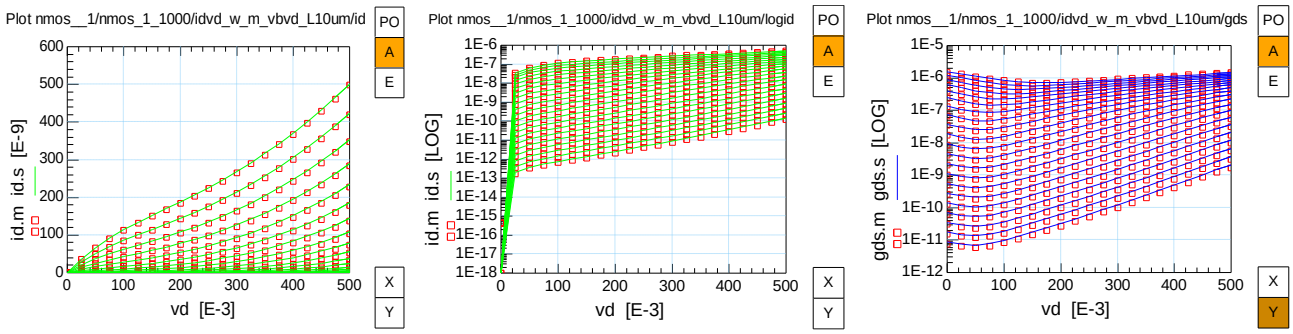


Fig. 1.21: NMOS Drain-Bulk output characteristics I_{DS}, g_{DS} vs. V_{DS} (W/L=1um/10um)

Fig. 1.22 shows the V_A, and *n* vs. V_{DS} characteristics for the Drain-Bulk connected NMOS device. The slope factor is extracted from Early voltage V_A and Equation ().

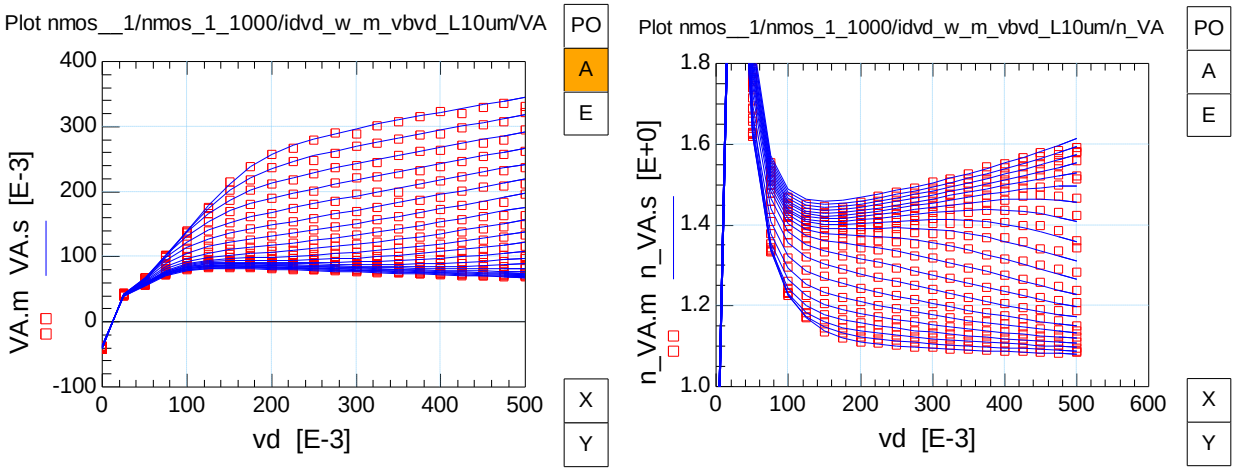


Fig. 1.22: V_A, and *n* vs. V_{DS} characteristics for the Drain-Bulk connected NMOS device (W/L=1um/10um)

In addition to the above, the same characteristics for Source-Bulk and Drain-Bulk configurations of aspect ratio equal to W/L=1um/180nm are followed:

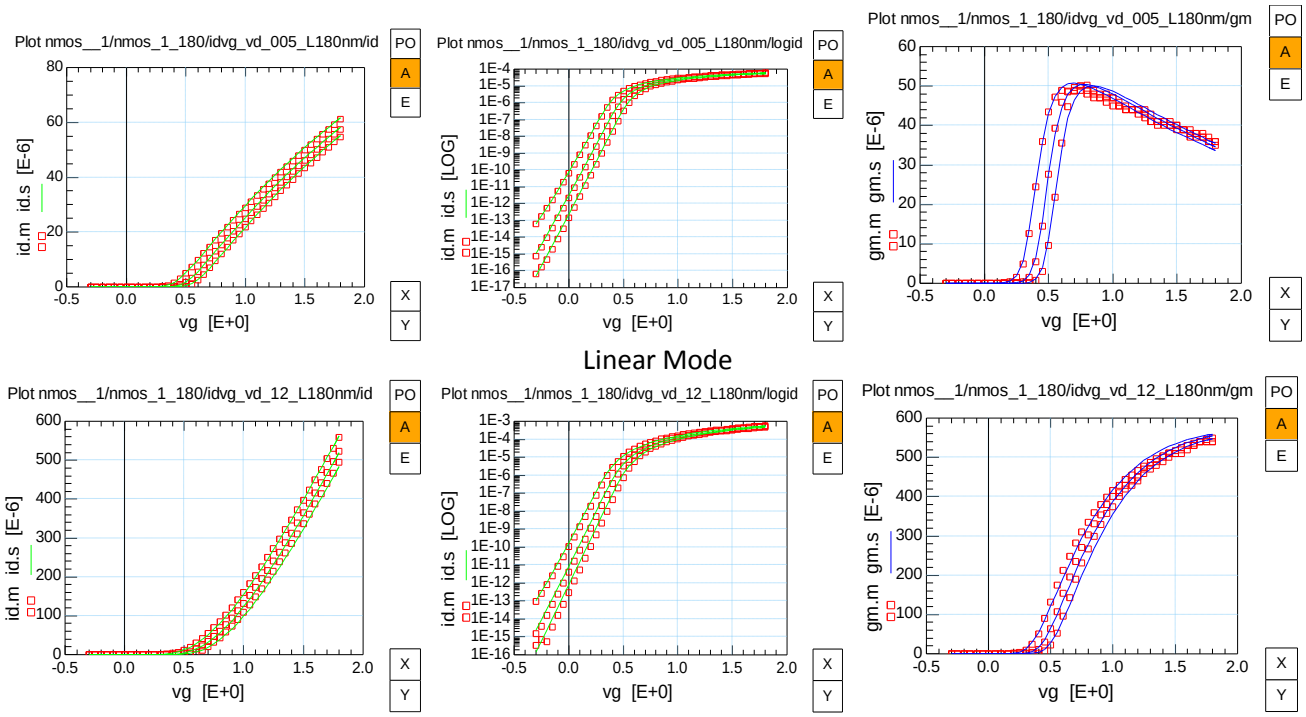


Fig. 1.23: NMOS Source-Bulk output characteristics I_{DS}, g_m vs. V_{GS} (W/L=1um/180nm), linear region (up) and saturation region (down)

Additionally, Fig. 1.24 below shows the output characteristics I_{DS} vs. V_{DS} and g_{DS} vs. V_{DS} for the same configuration as mentioned above,

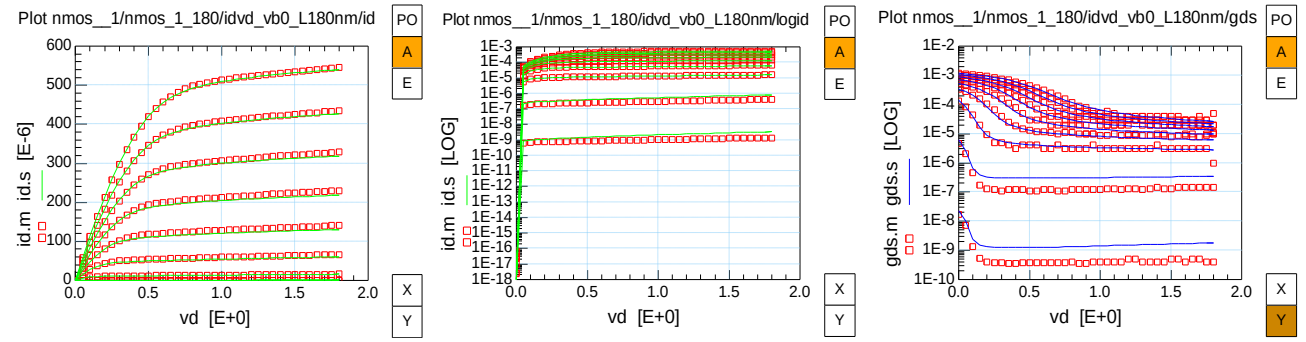


Fig. 1.24: NMOS Source-Bulk output characteristics I_{DS}, g_{DS} vs. V_{DS} (W/L=1um/180nm)

On the contrary, for the drain-bulk connected NMOS topology, the output characteristics are shown in Fig. 1.25,

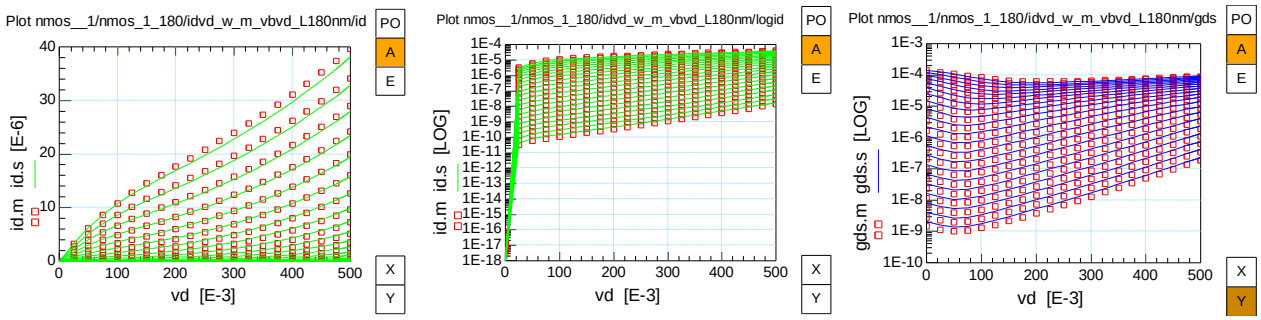


Fig. 1.25: NMOS Drain-Bulk output characteristics I_{DS}, g_{DS} vs. V_{DS} (W/L=1um/180nm)

Fig. 1.26 shows the V_A, and n vs. V_{DS} characteristics for the Drain-Bulk connected NMOS device. The slope factor is extracted from Early voltage V_A and Equation (1.19).

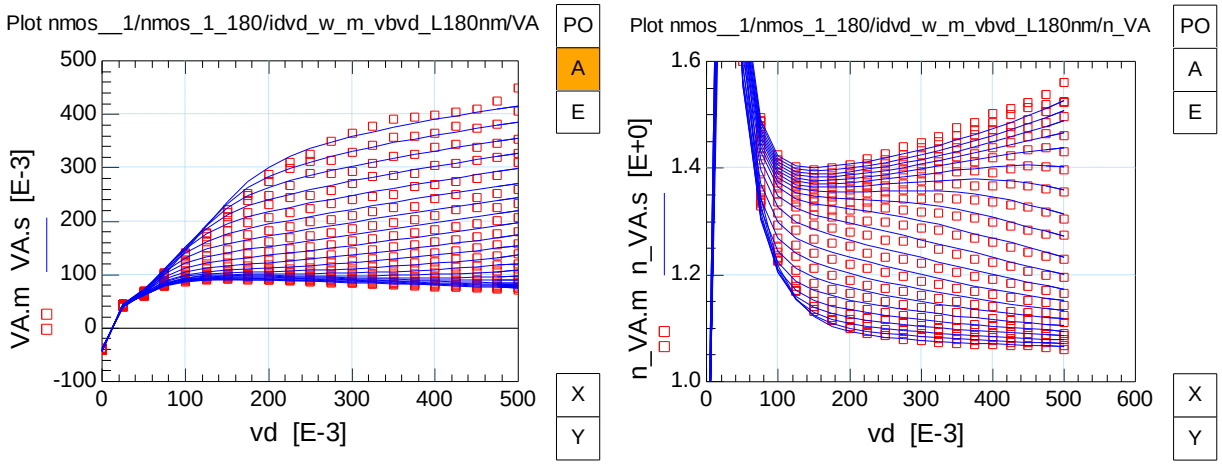


Fig. 1.26: V_A, and n vs. V_{DS} characteristics for the Drain-Bulk connected NMOS device (W/L=1um/180nm)

1.4.3 Source-Bulk and Drain-Bulk connected PMOS simulations

The following figures summarize and demonstrate the output characteristics of Source-Bulk and Drain-Bulk connected PMOS transistors similar to these of the NMOS devices that are shown above. Two different dimensions have been simulated, W/L=1um/10um and W/L=1um/180nm.

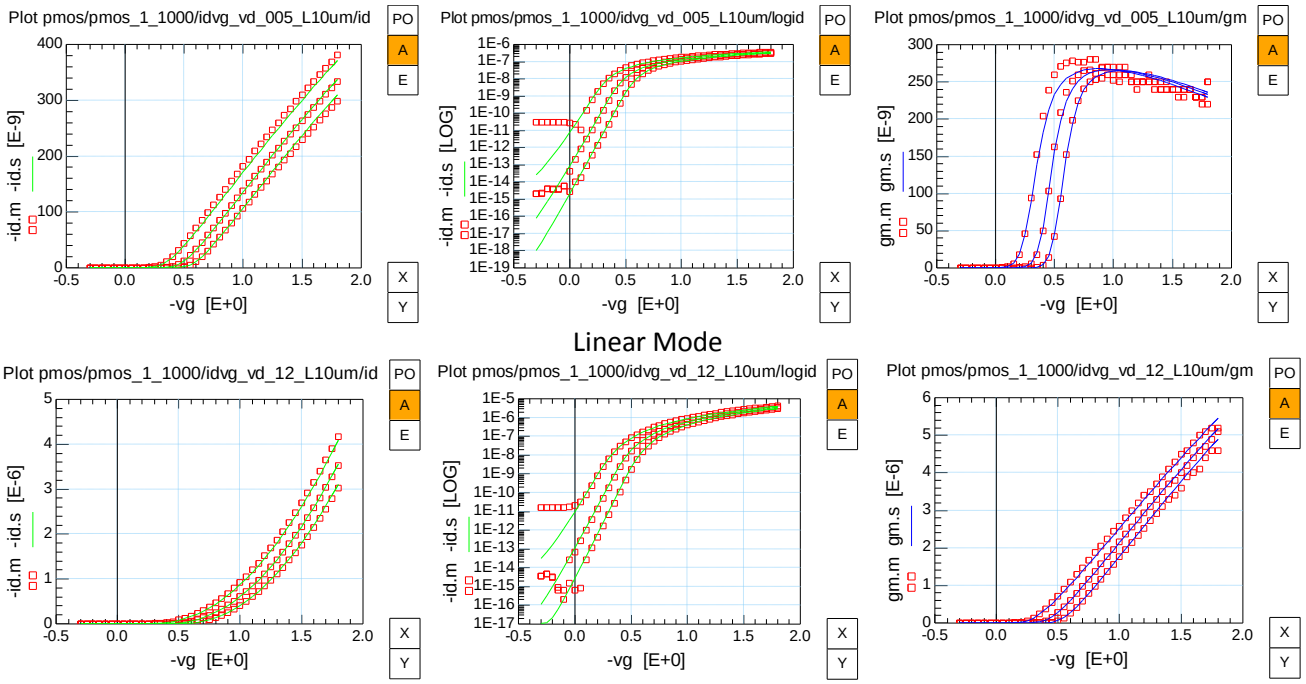


Fig. 1.27: PMOS Source-Bulk output characteristics I_{DS}, g_m vs. V_{GS} (W/L=1um/10um), linear region (up) and saturation region (down)

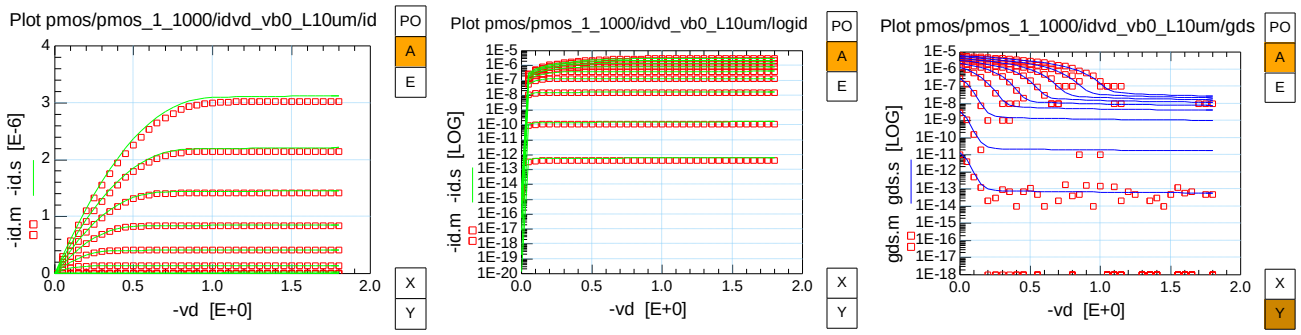


Fig. 1.28: PMOS Source-Bulk output characteristics I_{DS}, g_{DS} vs. V_{DS} (W/L=1um/10um)

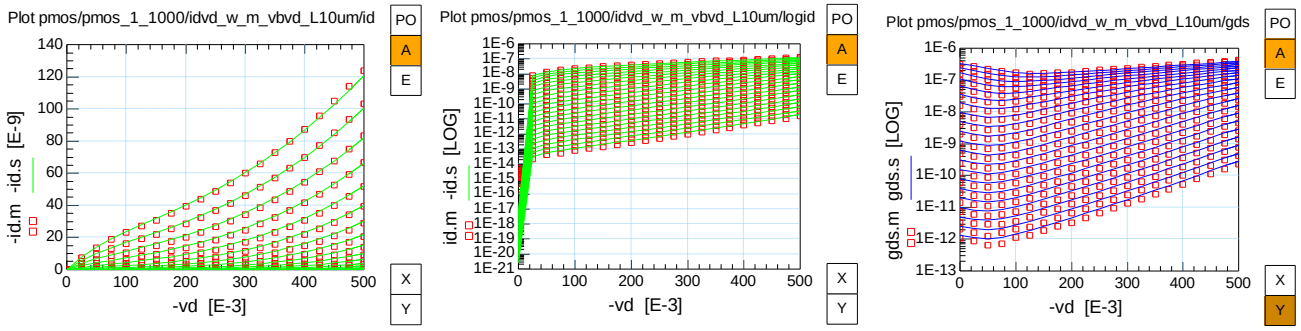


Fig. 1.29: PMOS Drain-Bulk output characteristics I_{DS}, g_{DS} vs. V_{DS} (W/L=1um/10um)

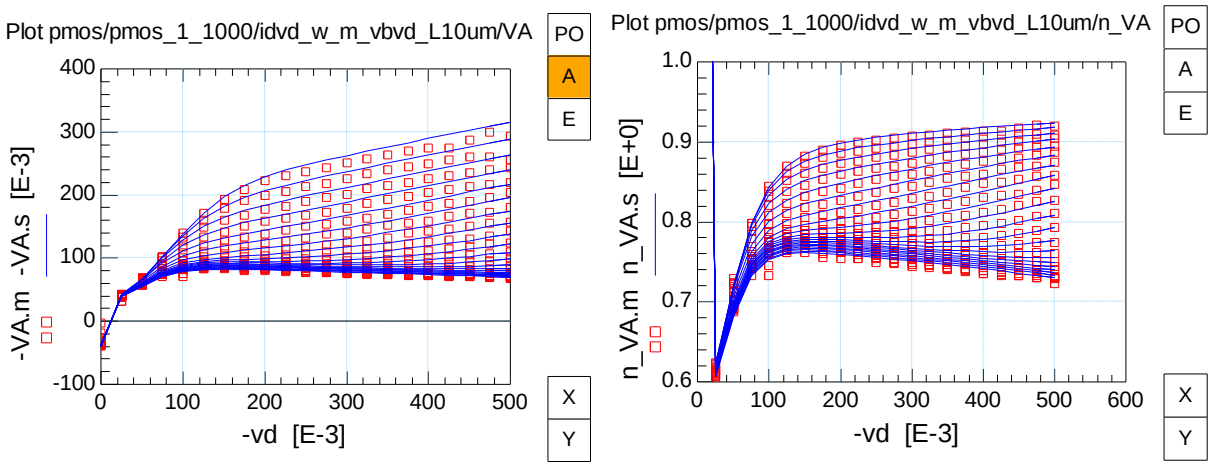


Fig. 1.30: V_A, and *n* vs. V_{DS} characteristics for the Drain-Bulk connected PMOS device (W/L=1um/10um)

The figures for the aspect ratio equal to W/L=1um/180nm follow:

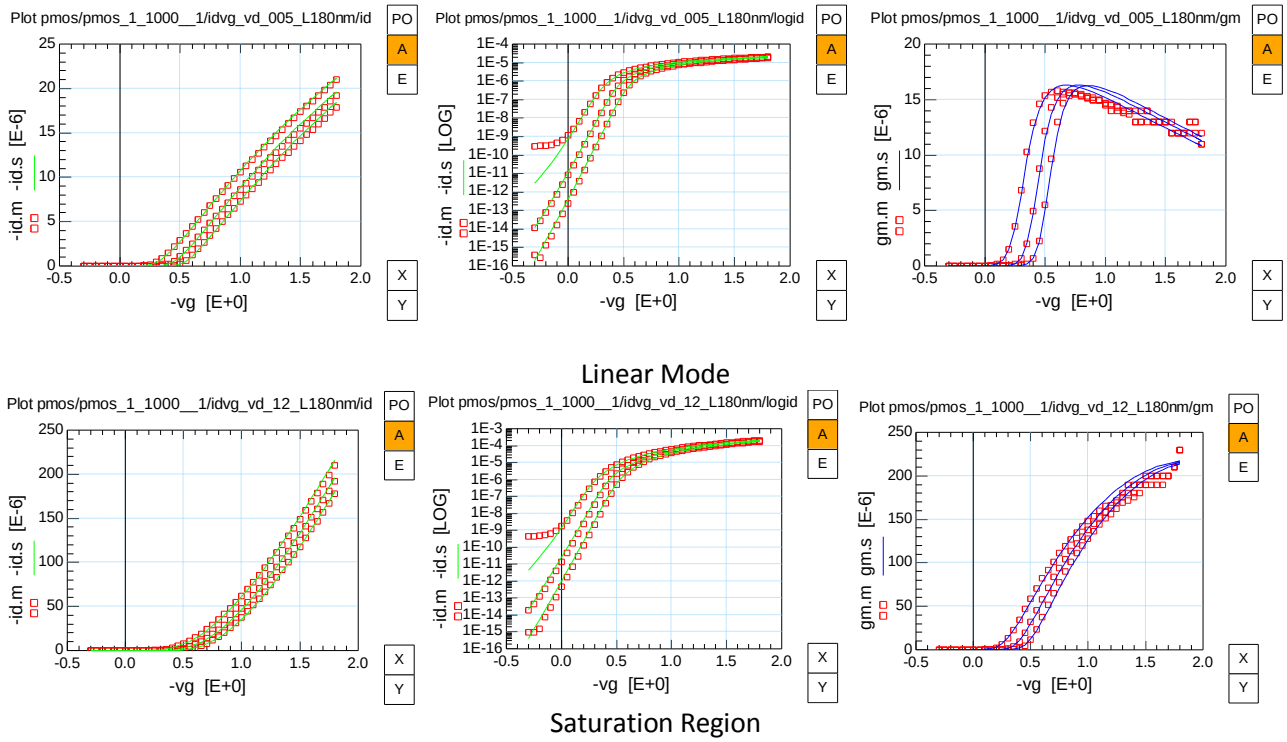


Fig. 1.31: PMOS Source-Bulk output characteristics I_{DS}, g_m vs. V_{GS} (W/L=1um/180nm)

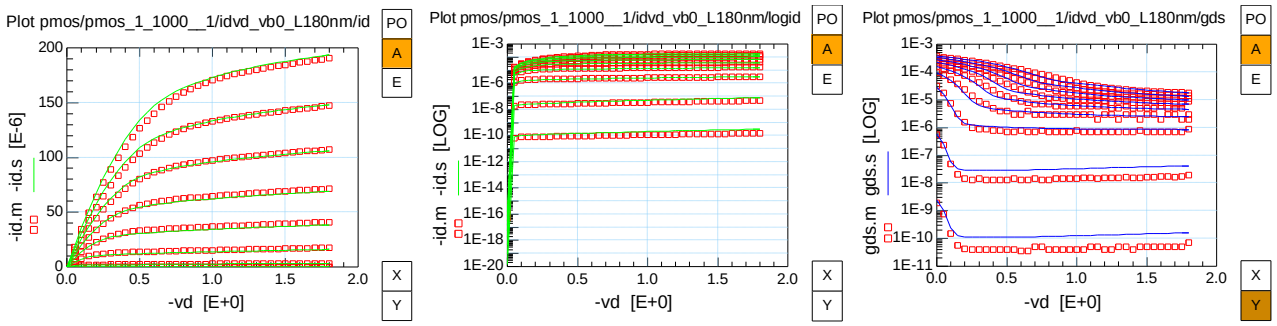


Fig. 1.32: PMOS Source-Bulk output characteristics I_{DS}, g_{DS} vs. V_{DS} (W/L=1um/180nm)

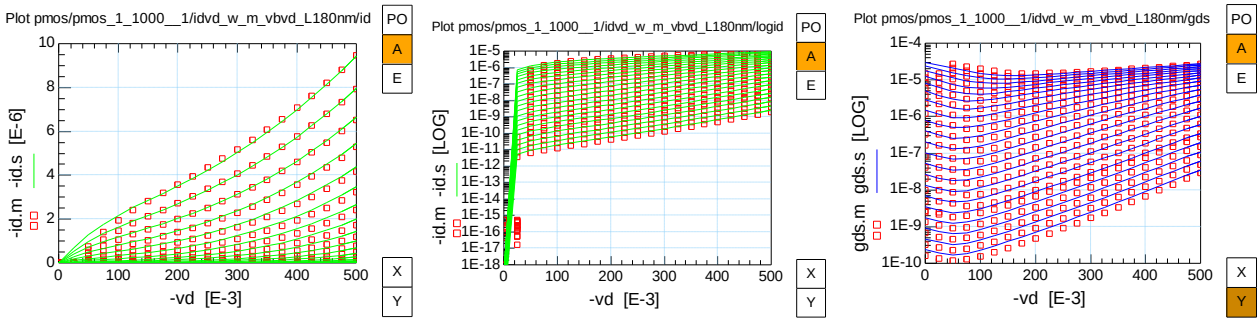


Fig. 1.33: PMOS Drain-Bulk output characteristics I_{DS}, g_{DS} vs. V_{DS} (W/L=1um/180nm)

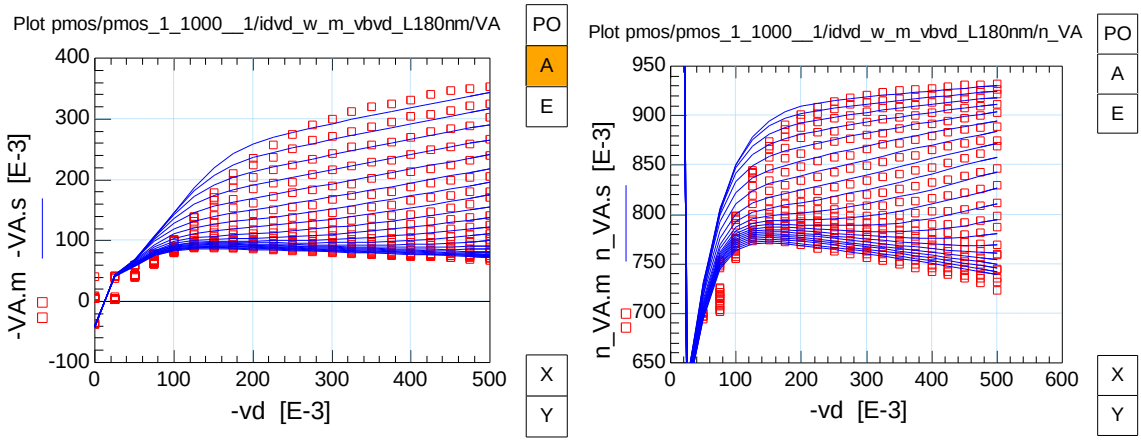
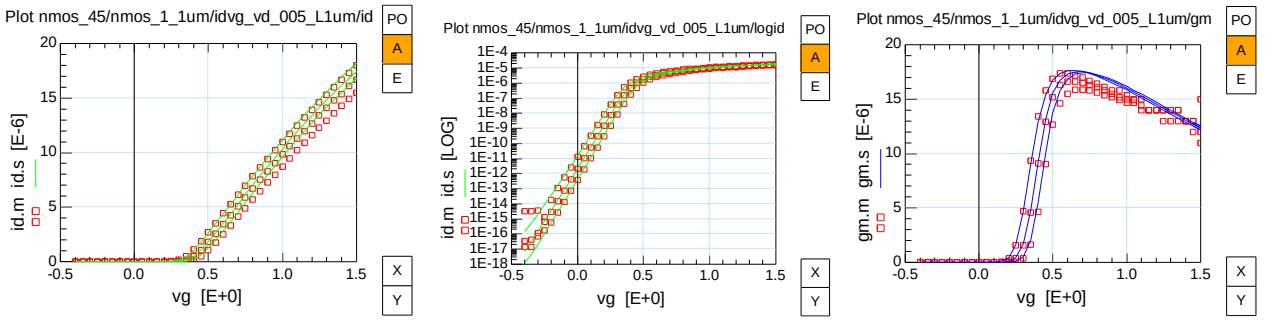


Fig. 1.34: V_A, and *n* vs. V_{DS} characteristics for the Drain-Bulk connected PMOS device (W/L=1um/180nm)

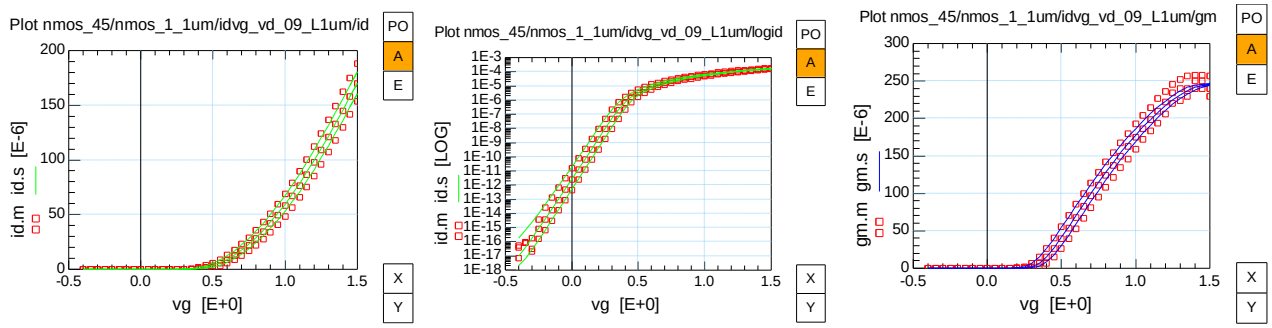
1.4.4 Source-Bulk and Drain-Bulk Connected MOS transistors of 45nm CMOS Technology Node

Additionally to the above, TCAD simulations have been made on a technology of 45nm. The simulated data have been imported into IC-CAP, where simulations with the EKV model version 301.02 have been performed, after extracting the parameters of the model for the 45nm technology used.

Fig. 1.35 below depicts the output characteristics I_{DS} vs. V_{GS} and g_m vs. V_{GS} of the conventional NMOS transistor for linear and saturation region of operation. The aspect ratio is equal to W/L=1um/1um:



Linear Mode



Saturation Region

Fig. 1.35: NMOS Source-Bulk output characteristics I_{DS}, g_m vs. V_{GS} (W/L=1um/1um)

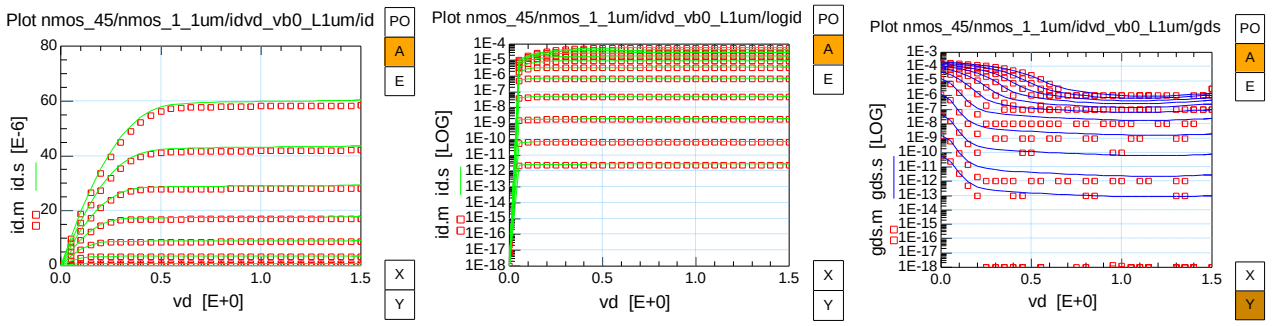


Fig. 1.36: NMOS Source-Bulk output characteristics I_{DS}, g_{DS} vs. V_{DS} (W/L=1um/1um)

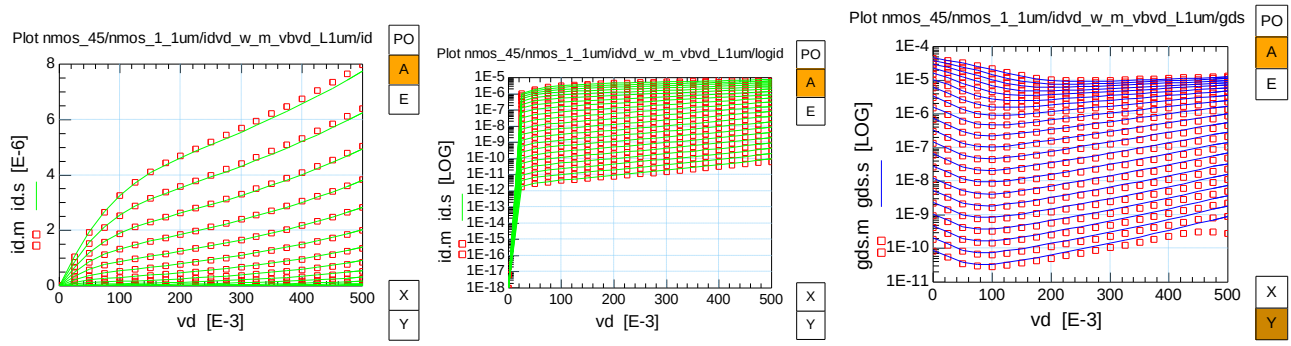


Fig. 1.37: NMOS Drain-Bulk output characteristics I_{DS}, g_{DS} vs. V_{DS} (W/L=1um/1um)

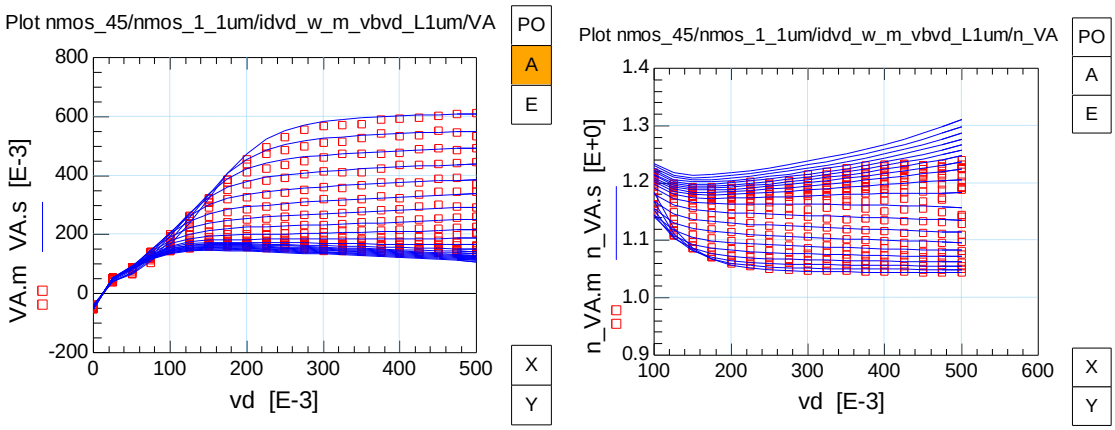
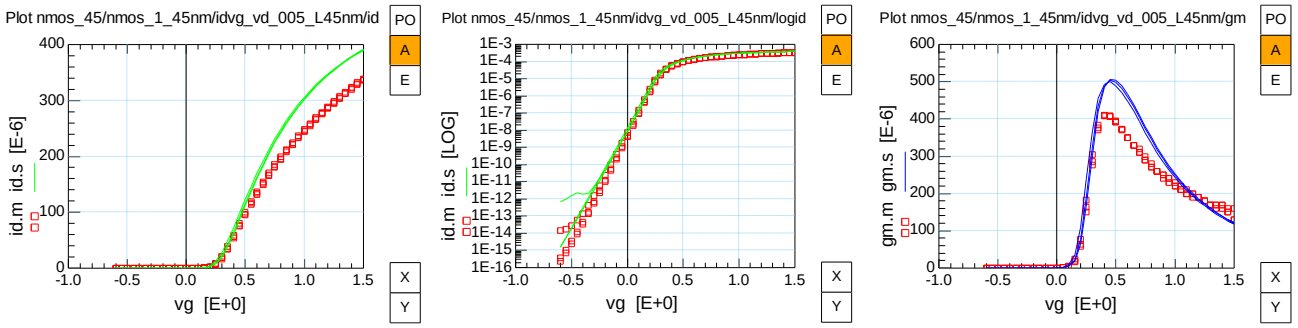
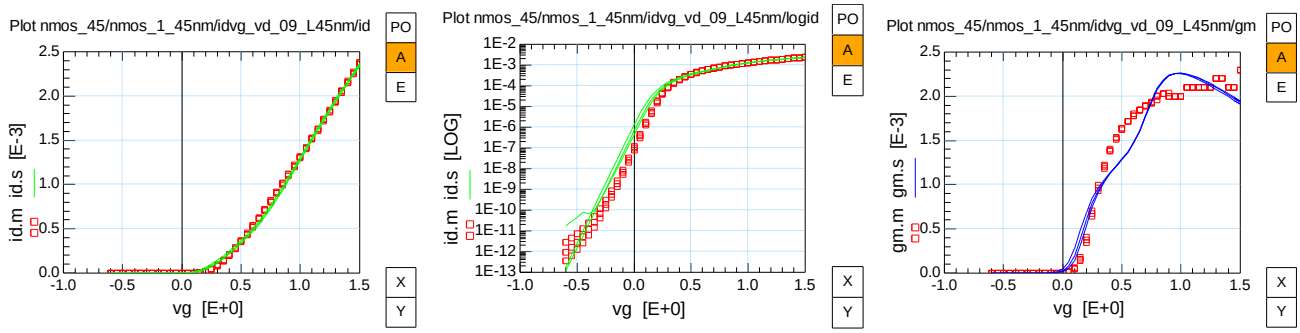


Fig. 1.38: V_A, and *n* vs. V_{DS} characteristics for the Drain-Bulk connected NMOS device (W/L=1um/1um)

In addition to the above, the following figures present the output characteristics for Source-Bulk and Drain-Bulk configurations of aspect ratio equal to W/L=1um/45nm:



Linear Mode



Saturation Region

Fig. 1.39: NMOS Source-Bulk output characteristics I_{DS}, g_m vs. V_{GS} (W/L=1um/45nm)

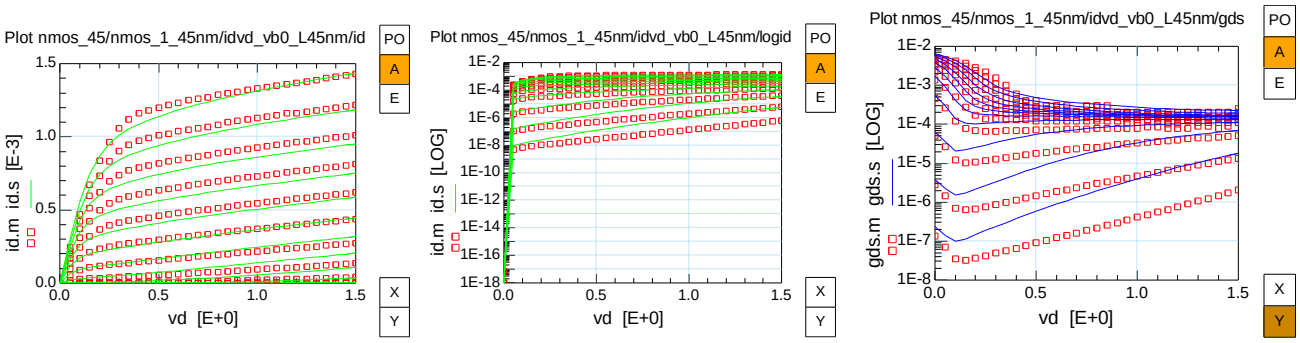


Fig. 1.40: NMOS Source-Bulk output characteristics I_{DS}, g_{DS} vs. V_{DS} (W/L=1um/45nm)

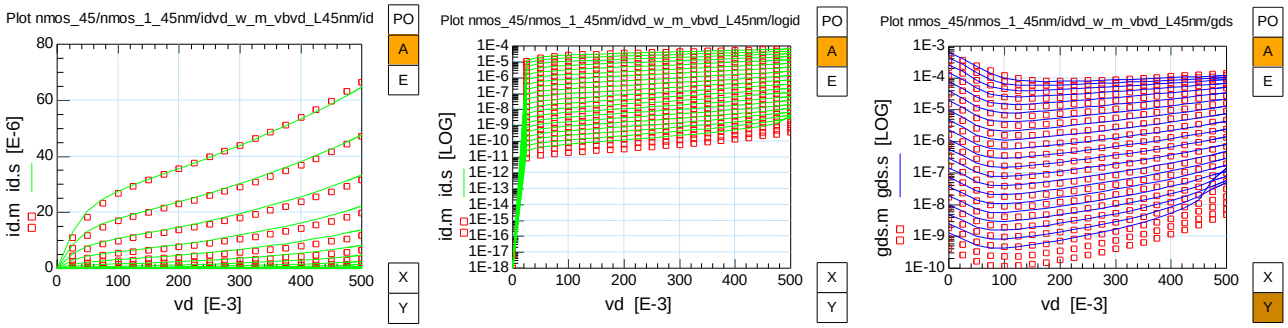


Fig. 1.41: NMOS Drain-Bulk output characteristics I_{DS}, g_{DS} vs. V_{DS} (W/L=1um/45nm)

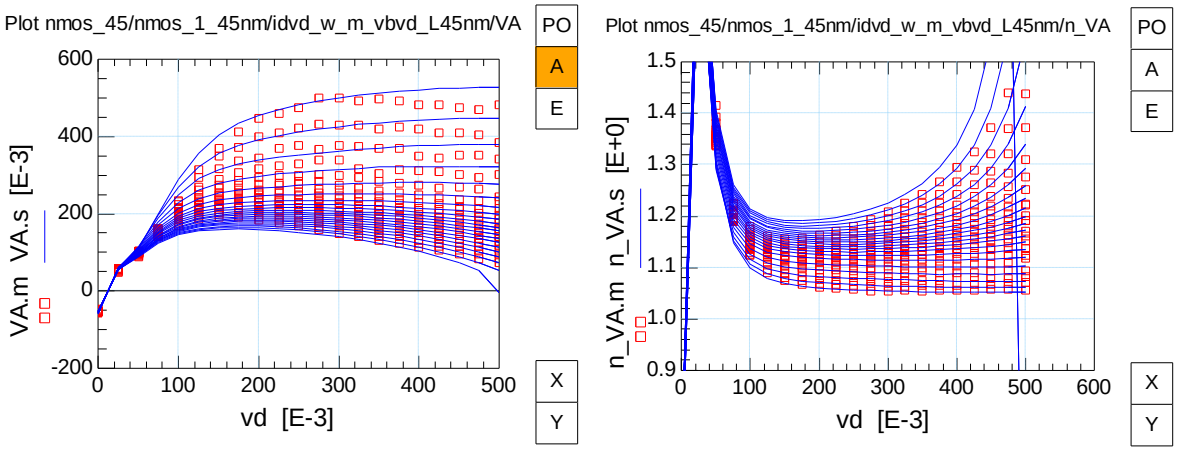


Fig. 1.42: V_A, and n vs. V_{DS} characteristics for the Drain-Bulk connected NMOS device (W/L=1um/45nm)

1.4.5 Summary of Source-Bulk and Drain-Bulk Connected MOS Devices

This work has shown the invariability of Early voltage and intrinsic gain of drain-bulk connected NMOS and PMOS transistors operated in weak-moderate inversion. Both quantities are governed essentially by the substrate effect - or slope factor n – and hence have a very low dependence on short-channel and biasing effects, once the V_{DS} value attains voltages as low as about $4U_T$. This can be easily exploited in applications where insensitivity of gain or Early voltage w.r.t. bias and channel length is favored.

The measured and simulated I_{DS} vs. V_{DS} and g_{DS} vs. V_{DS} characteristics of the drain-bulk connected NMOS devices are shown in the left side of Fig. 1.43. The same characteristics of the drain-bulk PMOS are depicted in the right side of Fig. 1.43. In the first case, we have TCAD data versus the EKV301.02

simulations, whereas, in the second case, we have real measurements versus the analytical charge-based model of Equation (1.13). The NMOS devices are biased with a gate voltage ranging from 100 mV to 600 mV with a step of 25 mV. On the other hand, the PMOS devices, measured on the 180nm wafer, are biased with a gate voltage ranging from 250mV to 350mV with a step size of 25mV.

The Fig. 1.43 illustrates that for both NMOS and PMOS transistors, the I_{DS} vs. V_{DS} behavior and thus the output conductance g_{DS}, are dominated by the substrate effect. Drain Induced Barrier Lowering (DIBL) effect which is the usually dominant effect for output conductance in short transistors in weak inversion, is actually dominated by the substrate effect.

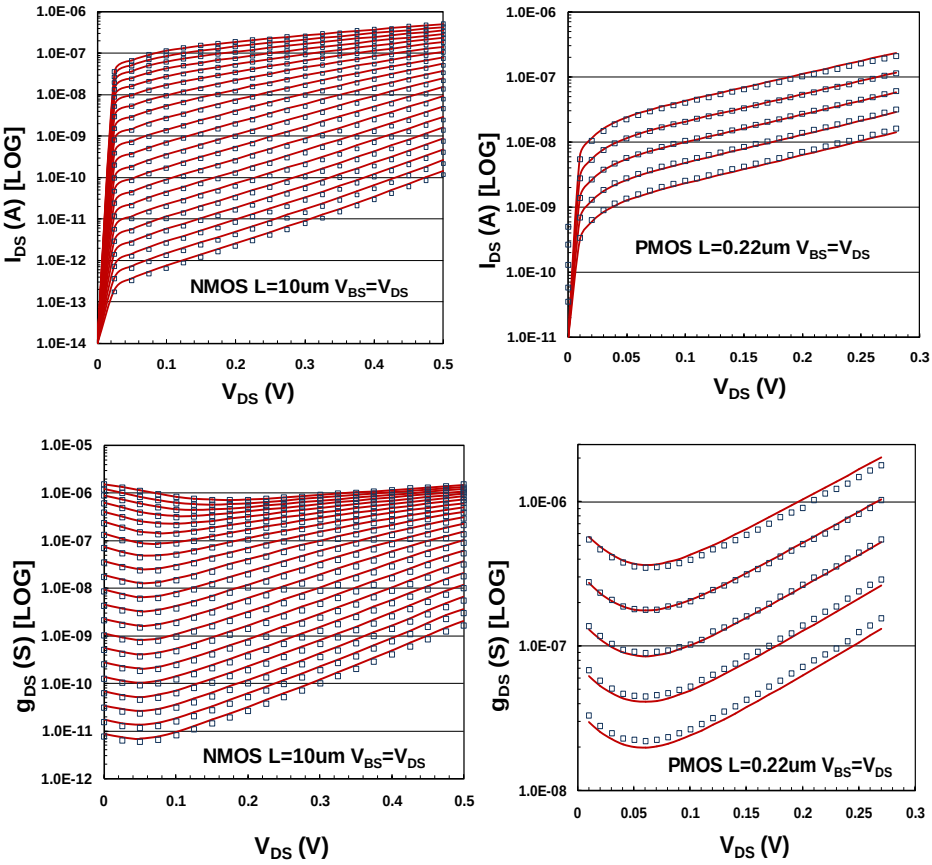


Fig. 1.43: Drain-bulk connected NMOS (left) and PMOS (right) transistor, with respective output characteristics, W/L=1µm/10µm (left) and W/L=10µm/0.22µm. I_{DS}, g_{DS} vs. V_{DS} are shown for various values of V_{GS} (markers: TCAD simulation data(left), measurements (right), lines: EKV3 model (left), analytical charge-based model (right)).

Fig. 1.44 shows the V_A, n and A_V vs. V_{DS} characteristics for the drain-bulk connected NMOS and PMOS devices. In the left case, we have the TCAD vs. EKV301.02 simulations, whereas in the right case, we have the comparisons between real measurements and analytical charge-based model of Equation (1.13). In the case of drain-bulk connected NMOS configuration, the devices are biased with a gate voltage ranging from 100 mV to 600 mV with a step of 25 mV. On the other hand, the PMOS devices, measured on the 180 nm wafer, are biased with a gate voltage ranging from 250 mV to 350 mV with a step size of 25 mV.

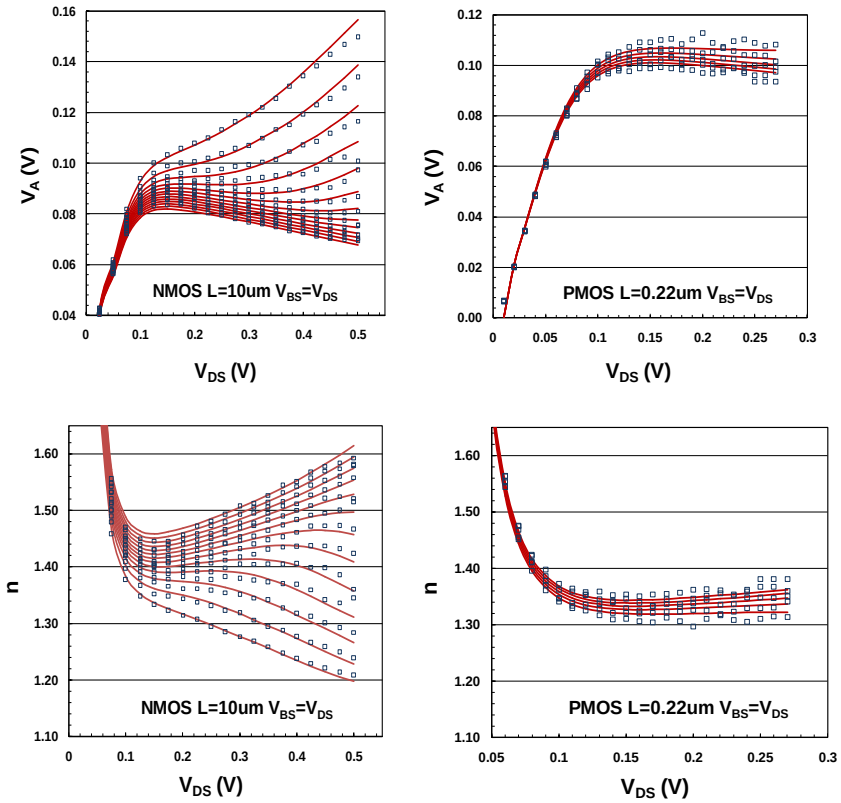


Fig. 1.44: Early Voltage V_A and slope Factor n extracted from Equation (1.19) of drain-bulk connected NMOS (left) and PMOS (right) devices (markers: TCAD/measured data, lines: EKV3/analytical model).

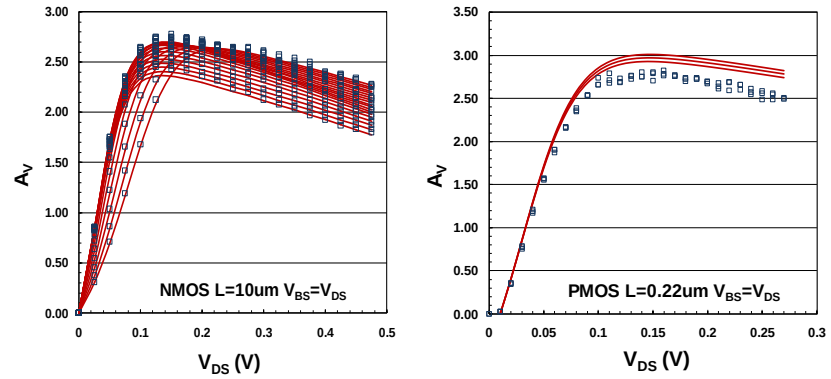


Fig. 1.45: Intrinsic Gain A_V of drain-bulk connected NMOS (left) and PMOS (right) devices (markers: TCAD/measured data, lines: EKV3/analytical model).

The behavior of V_A vs. V_{DS} for drain-bulk connected NMOS and PMOS transistors, for W/L = 1 µm / 10 µm and W/L = 10 µm / 0.22 µm is given in the left and right side of Fig. 1.44, respectively.

In the case of the V_A characteristics, the same figure shows that for any geometry we use, the Early voltage in nearly constant and independent of V_{GS} both for NMOS (TCAD vs. EKV301.02) and PMOS (real measurements vs. analytical charge based model).

The same result arrives for the case of the slope factor n, which is extracted from V_A using Equation (1.19) in weak inversion and saturation region. Additionally, Fig. 1.45 depicts the behavior of the intrinsic gain g_m/g_{DS} vs. $V_{DS,}$ which is independent of the V_{GS} bias point and begins to remain almost constant for a low V_{DS} voltage nearly equal to 100 mV.

As again seen in Fig. 1.45, the drain-bulk connected topology is characterized in weak and moderate inversion saturation by a V_A almost independent of V_{DS}. The Early voltage is also independent of inversion coefficient *IC* and channel length *L* as reported in [13] and consequently, V_A is approximately constant and independent of bias voltages and channel length.

Additionally to the above, TCAD simulations have been made on a technology of 45nm. The simulated data have been imported into IC-CAP, where simulations with the EKV model version 301.02 have been performed, after extracting the parameters of the model for the 45nm technology used. Fig. 1.46 depicts the simulated drain-bulk connected NMOS transistor, with respective output characteristics of I_{DS}, g_{DS} vs. V_{DS} for two geometries, W/L = 1 µm / 1 µm (left side) and W/L = 1 µm / 45 nm (right side) and confirm the aforementioned I_{DS} vs. V_{DS} and g_{DS} vs. V_{DS} behavior similar to the 180 nm technology node.

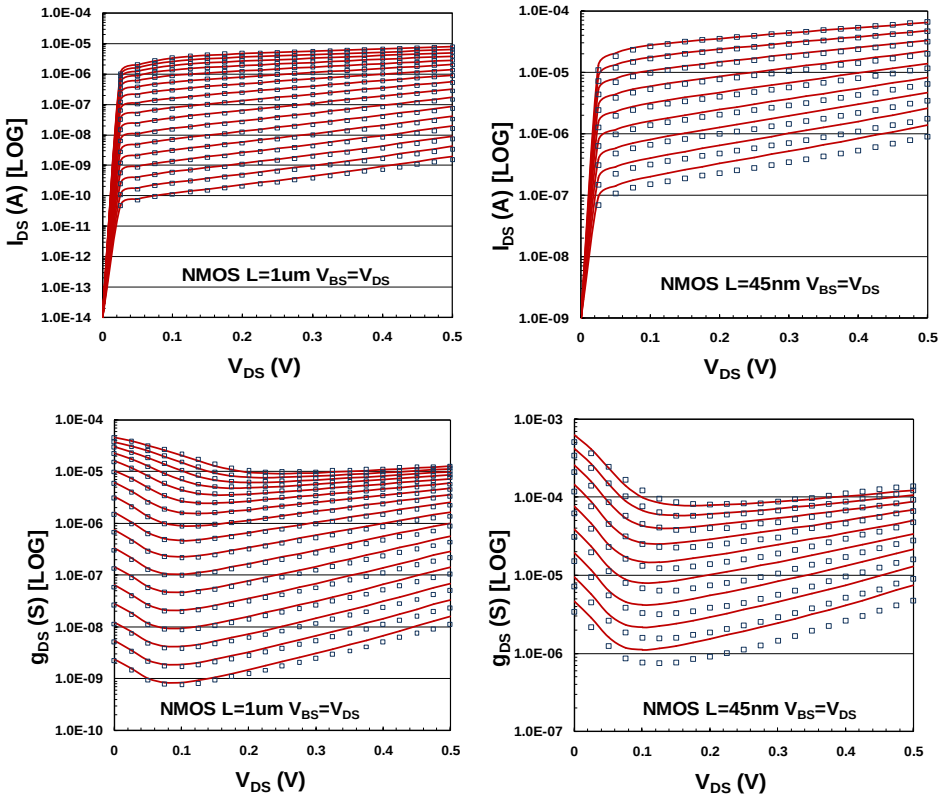


Fig. 1.46: Drain-bulk connected NMOS transistor, with respective output characteristics, W/L=1µm/1µm (left) and , W/L=1µm/45nm. I_{DS}, g_{DS} vs. V_{DS} are shown for various values of V_{GS} (markers: TCAD simulation data, lines: EKV3 model).

1.4.6 Grounded-Gate MOS Transistors

Another interesting configuration of MOS transistors that have been used in circuit design (see Chapter 5), is the grounded-gate, where the terminals of gate and bulk are shorted. The following figure shows this topology,

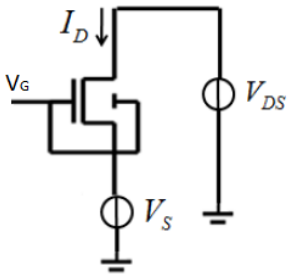


Fig. 1.47: Grounded-Gate MOSFET

As mentioned above, the drain current of the MOS device is given by,

$$I_D = I_F - I_R = I_{Spec}\left(i_f - i_r\right)$$

where

$$i_f = q_s^2 + q_s, \; i_r = q_d^2 + q_d$$

are the normalized forward and reverse currents of the channel.

Let us assume a threshold voltage of V_T=500mV, a drain voltage of V_D=700mV and a source voltage V_S that ranges from -0.3V to 0.3V. For a given slope factor n=1.4 and a technology current of I_{Spec}=500nA, we have:

$$V_P = \frac{V_{GB} - V_T}{n} \Rightarrow V_P = -400mV$$ (notice that V_G=V_B)

The pinch-off voltage remains constant across the channel and is smaller than all values of the source voltages V_S and drain voltage V_D. Therefore, the device operates in weak inversion at both source and drain terminals. In order to calculate the inversion charges under the source and drain terminals, we use the voltage-charge relations,

$$u_p - u_s = \ln\left(q_s\right)$$

$$u_p - u_d = \ln\left(q_d\right)$$

For a given source voltage of V_S=-300mV, we have,

$$u_p - u_s = \ln\left(q_s\right) \Rightarrow q_s = \exp\left(u_p - u_s\right) \Rightarrow q_s = \exp\left(\frac{V_P - V_S}{U_T}\right) \Rightarrow q_s = 0.01$$

$$u_p - u_d = \ln\left(q_d\right) \Rightarrow q_d = \exp\left(u_p - u_d\right) \Rightarrow q_s = \exp\left(\frac{V_P - V_D}{U_T}\right) \Rightarrow q_s = 3.2 \cdot 10^{-19}$$

As we can see, the value of inversion charge at the source terminal is much larger than this at the drain terminal. Therefore, the MOS channel is biased in weak inversion and operates in saturation region. The total current of the device is given by,

$$I_D = I_F - I_R \cong I_F \cong I_{Spec} \cdot i_f \Rightarrow I_{Spec} \cdot q_s \Rightarrow \exp\left(u_p - u_s\right)$$

where

$$i_f = q_s^2 + q_s \cong q_s$$

NMOS W/L=10um/10um (wide/long)

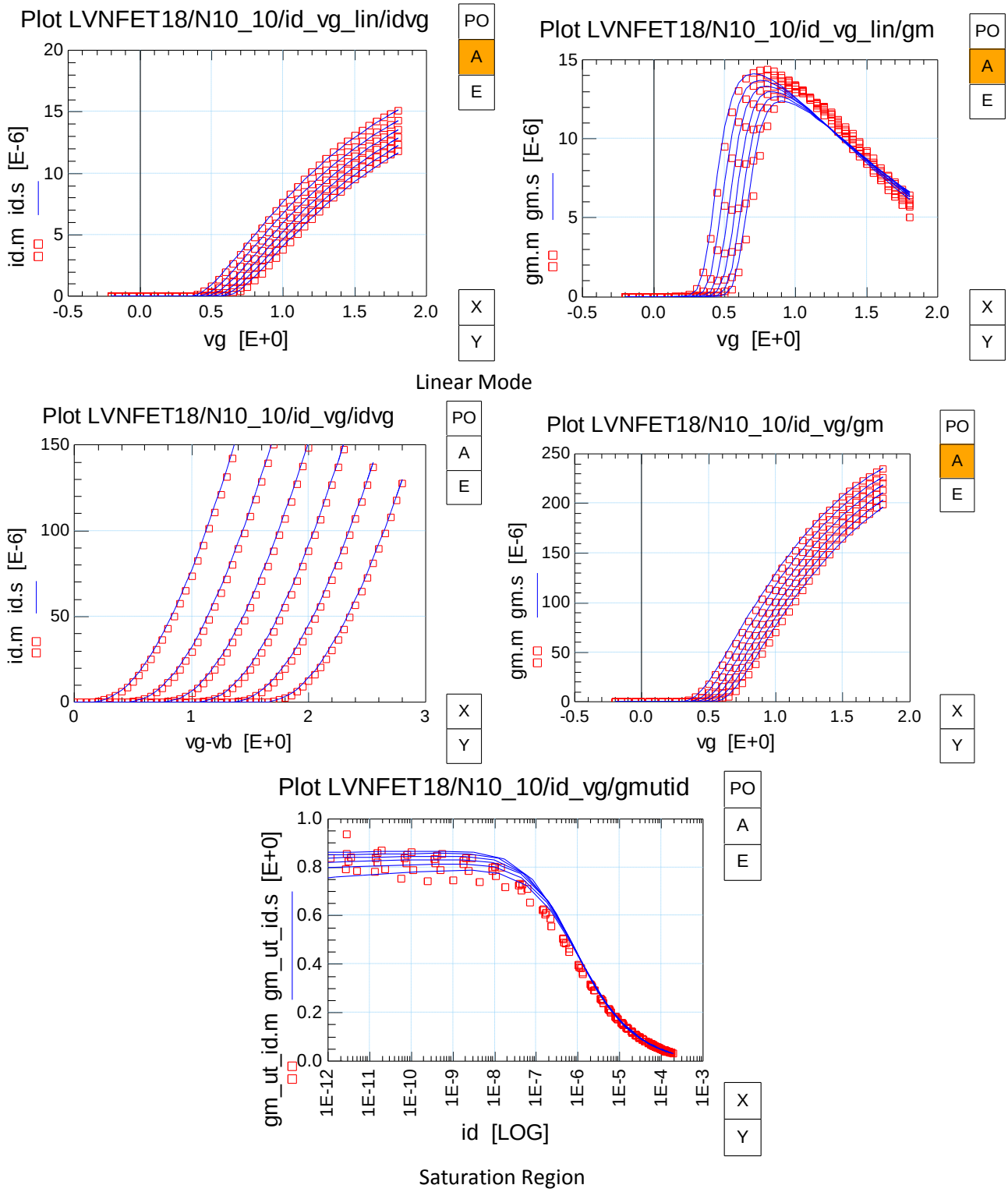


Fig. 1.48: Output Characteristics I_{DS}-V_{GS}, g_m-V_{GS}, g_m/I_{DS} (NMOS W/L=10um/10um)

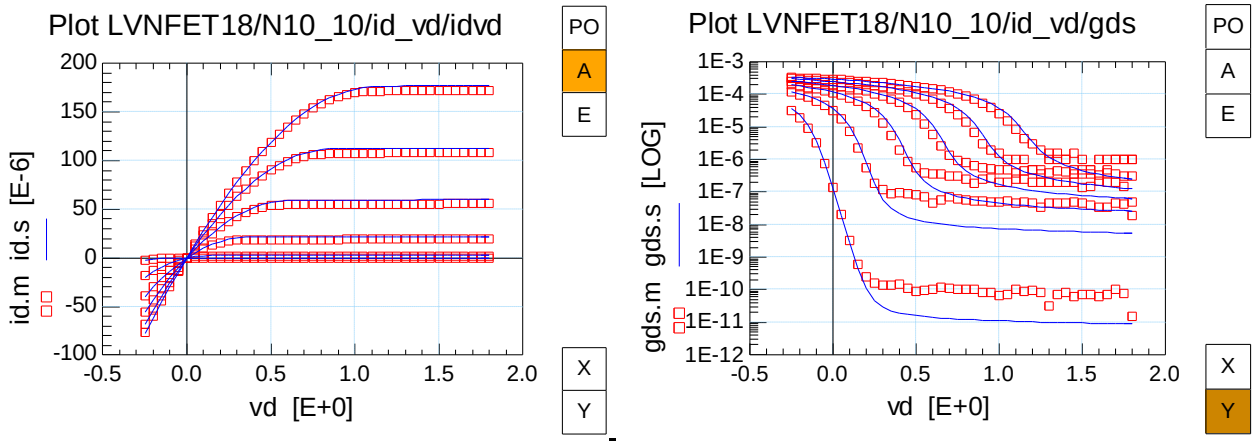


Fig. 1.49: Output Characteristics I_{DS}-V_{DS}, g_{DS}-V_{DS} (NMOS W/L=10um/10um)

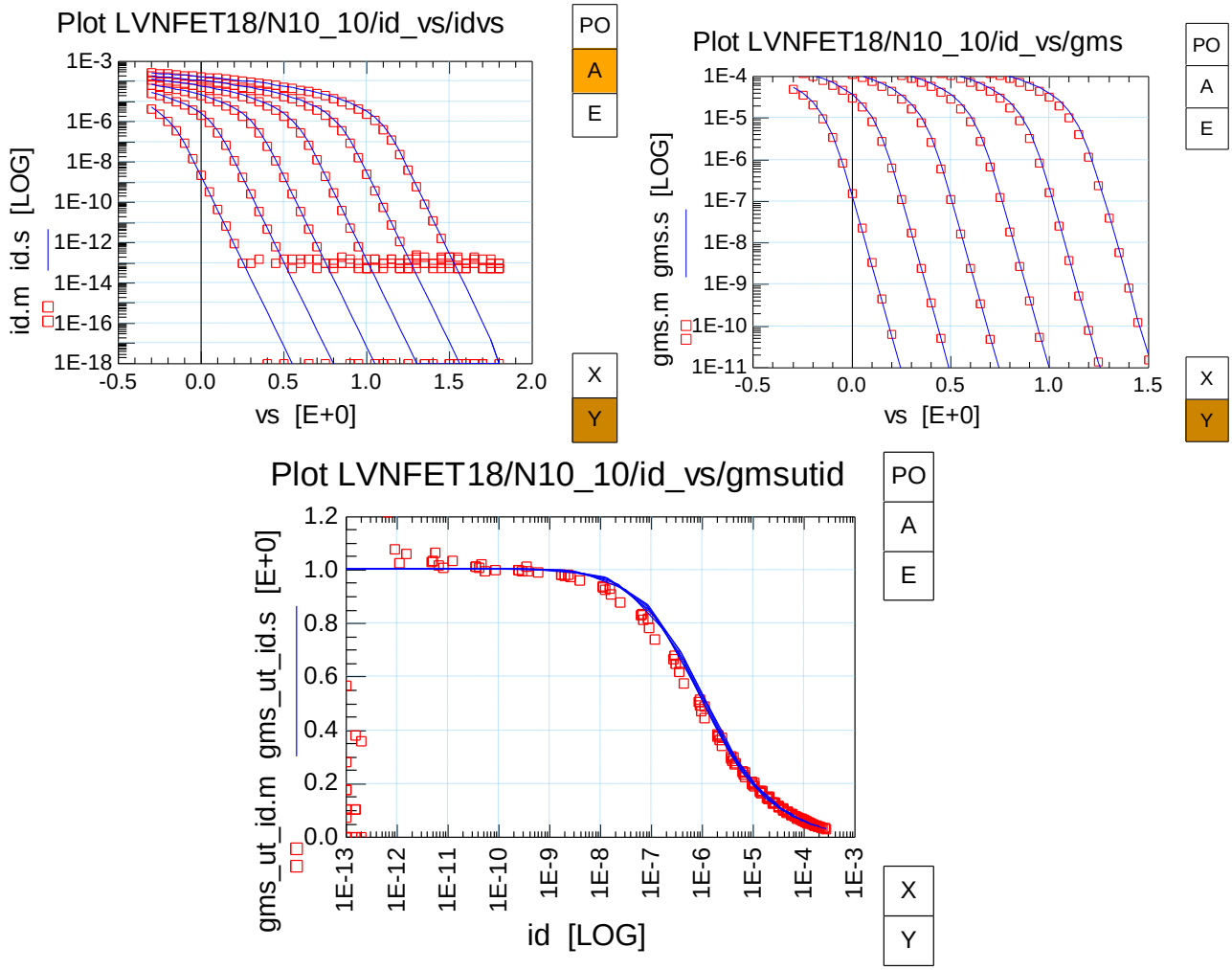


Fig. 1.50: Output Characteristics I_{DS}-V_S, g_{ms}-V_S, g_{ms}/I_{DS} (NMOS W/L=10um/10um)

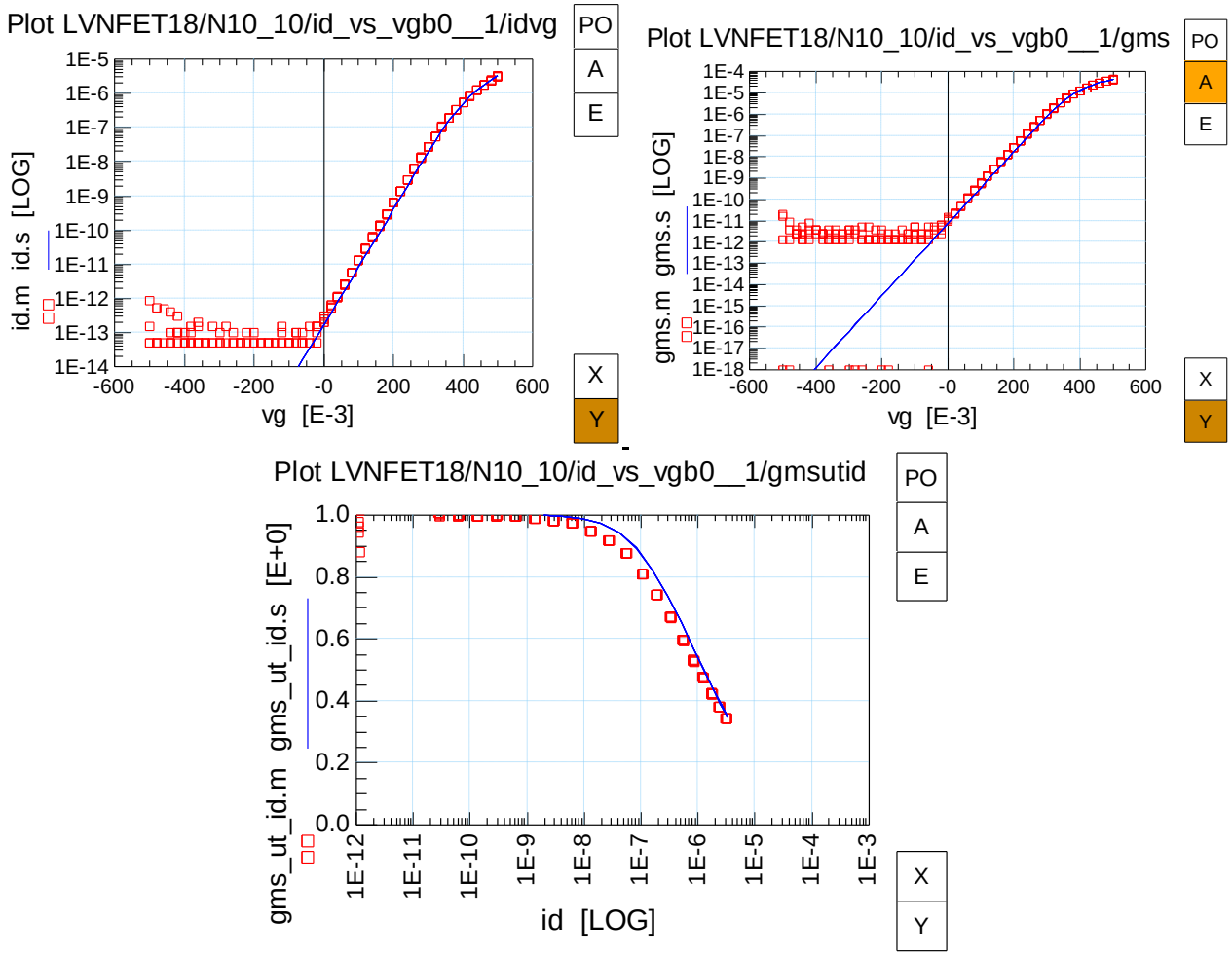


Fig. 1.51: Output Characteristics I_{DS}-V_{GS}, g_m-V_{GS}, g_{ms}/I_{DS} V_G=V_B (NMOS W/L=10um/10um)

NMOS W/L=10um/0.18um (wide/short)

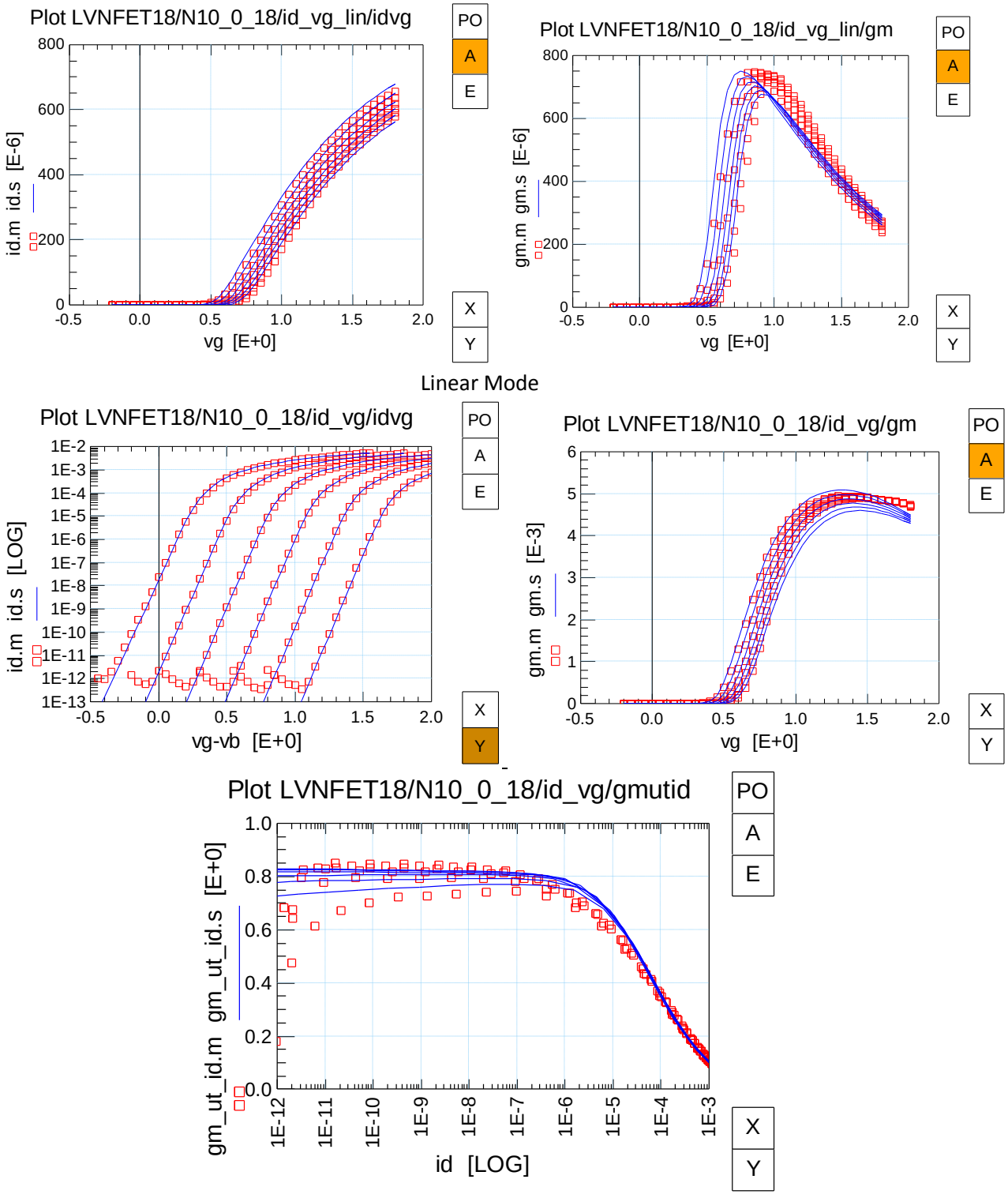


Fig. 1.52: Output Characteristics I_{DS}-V_{GS}, g_m-V_{GS}, g_m/I_{DS} (NMOS W/L=10um/0.18um)

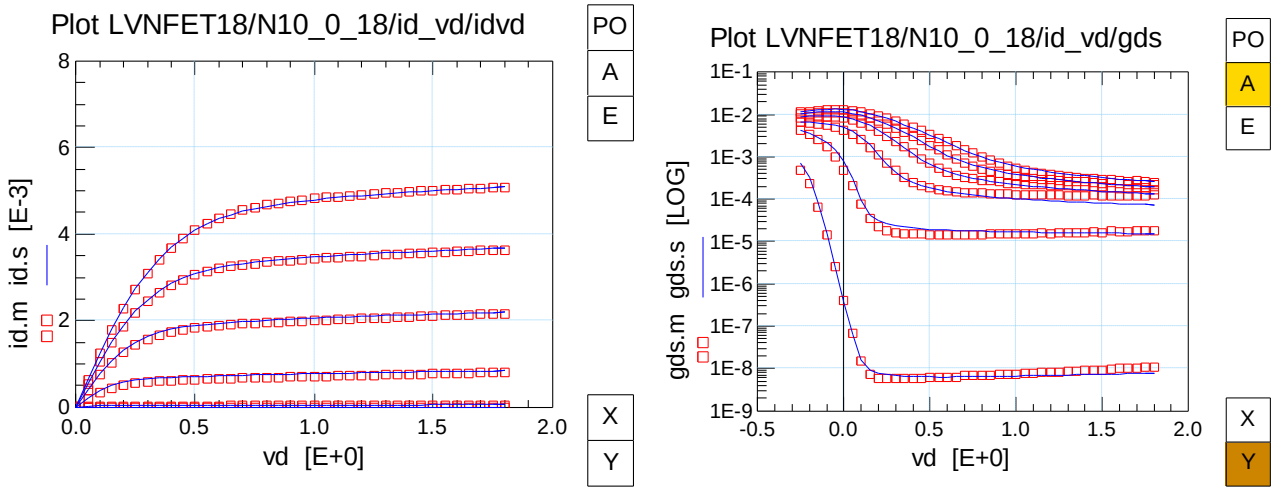


Fig. 1.53: Output Characteristics I_{DS}-V_{DS}, g_{DS}-V_{DS} (NMOS W/L=10um/0.18um)

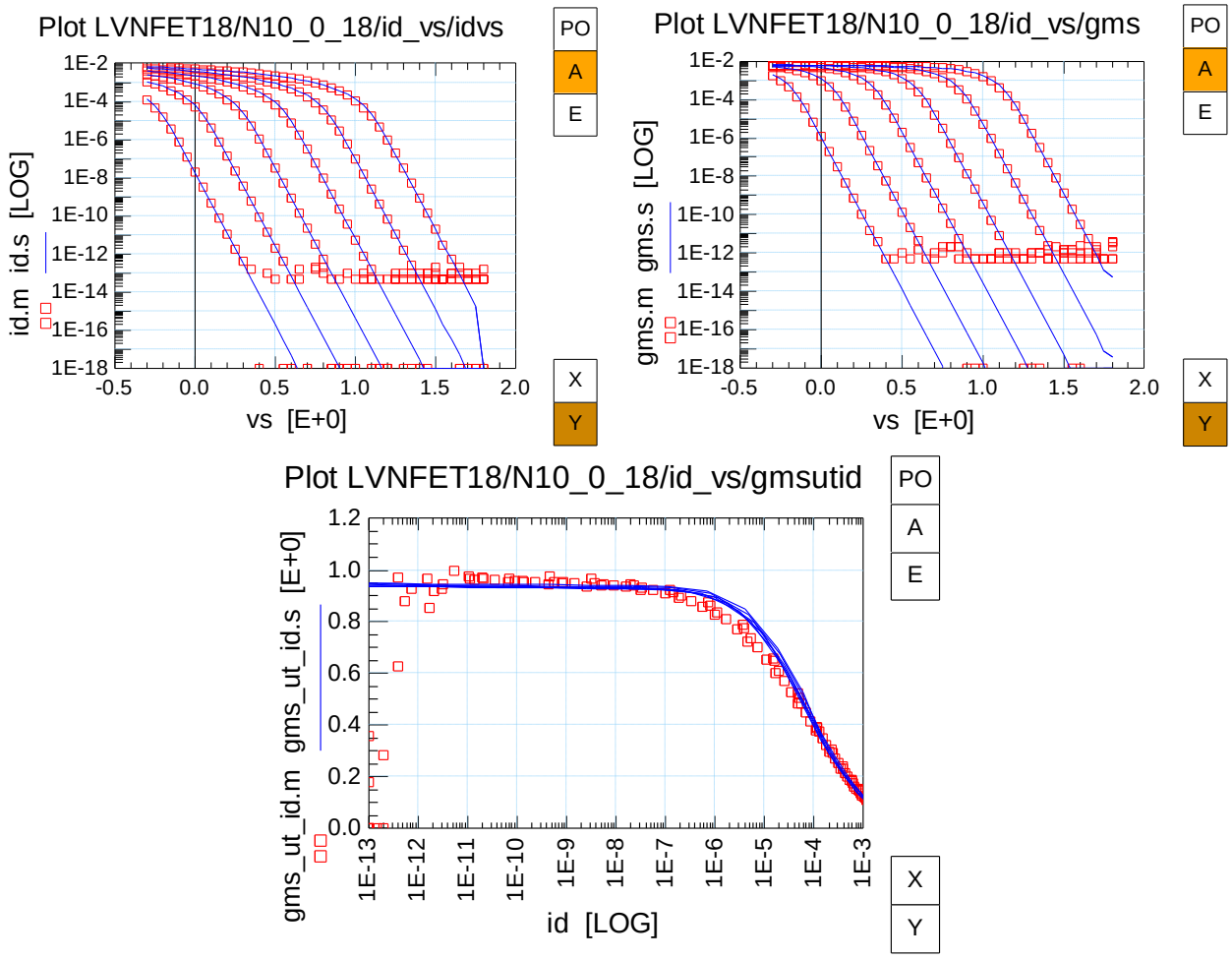


Fig. 1.54: Output Characteristics I_{DS}-V_S, g_{ms}-V_S, g_{ms}/I_{DS} (NMOS W/L=10um/0.18um)

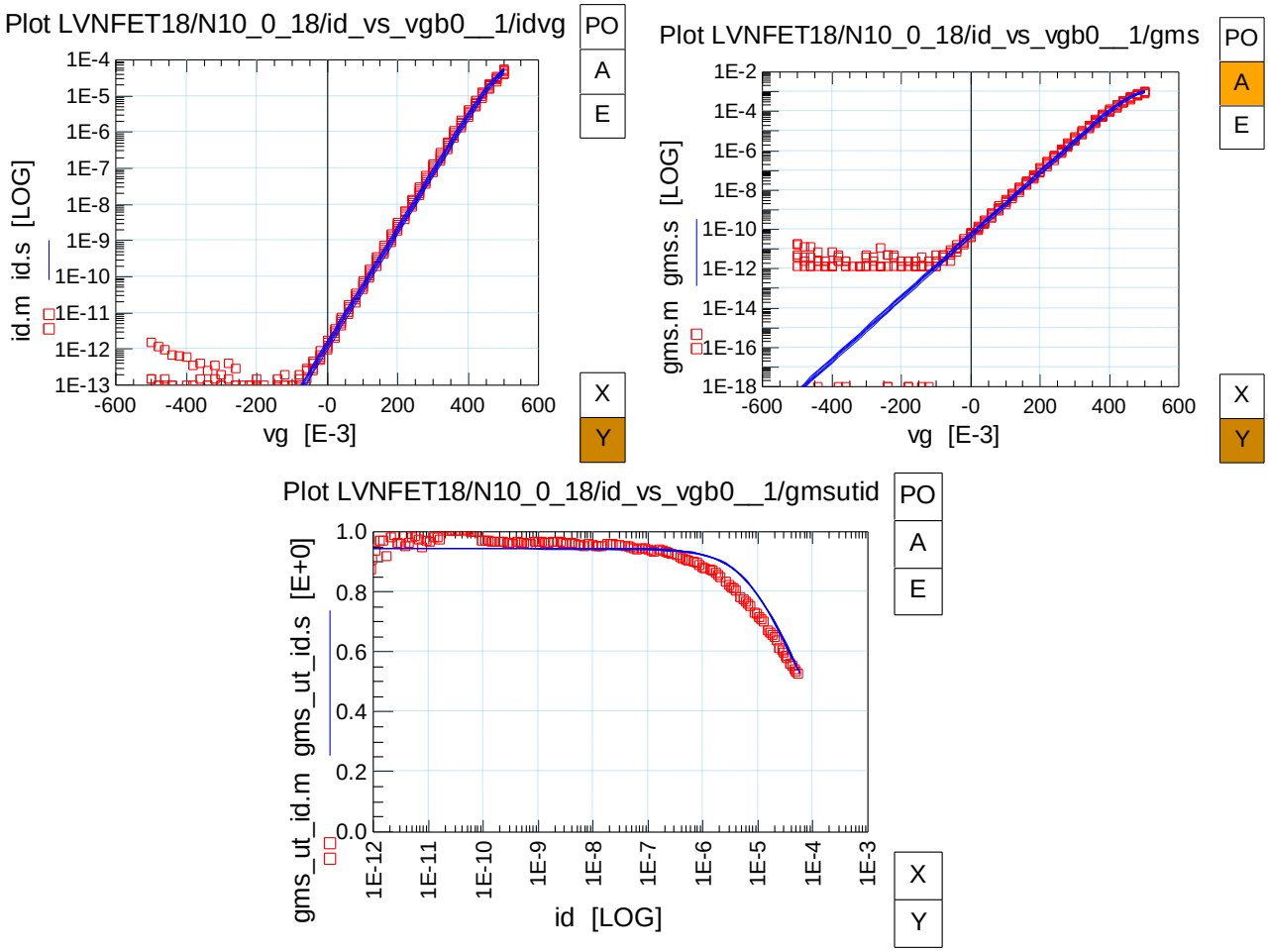


Fig. 1.55: Output Characteristics I_{DS}-V_S, g_{ms}-V_S, g_{ms}/I_{DS} V_G=V_B (NMOS W/L=10um/0.18um)

PMOS W/L=10um/10um (wide/long)

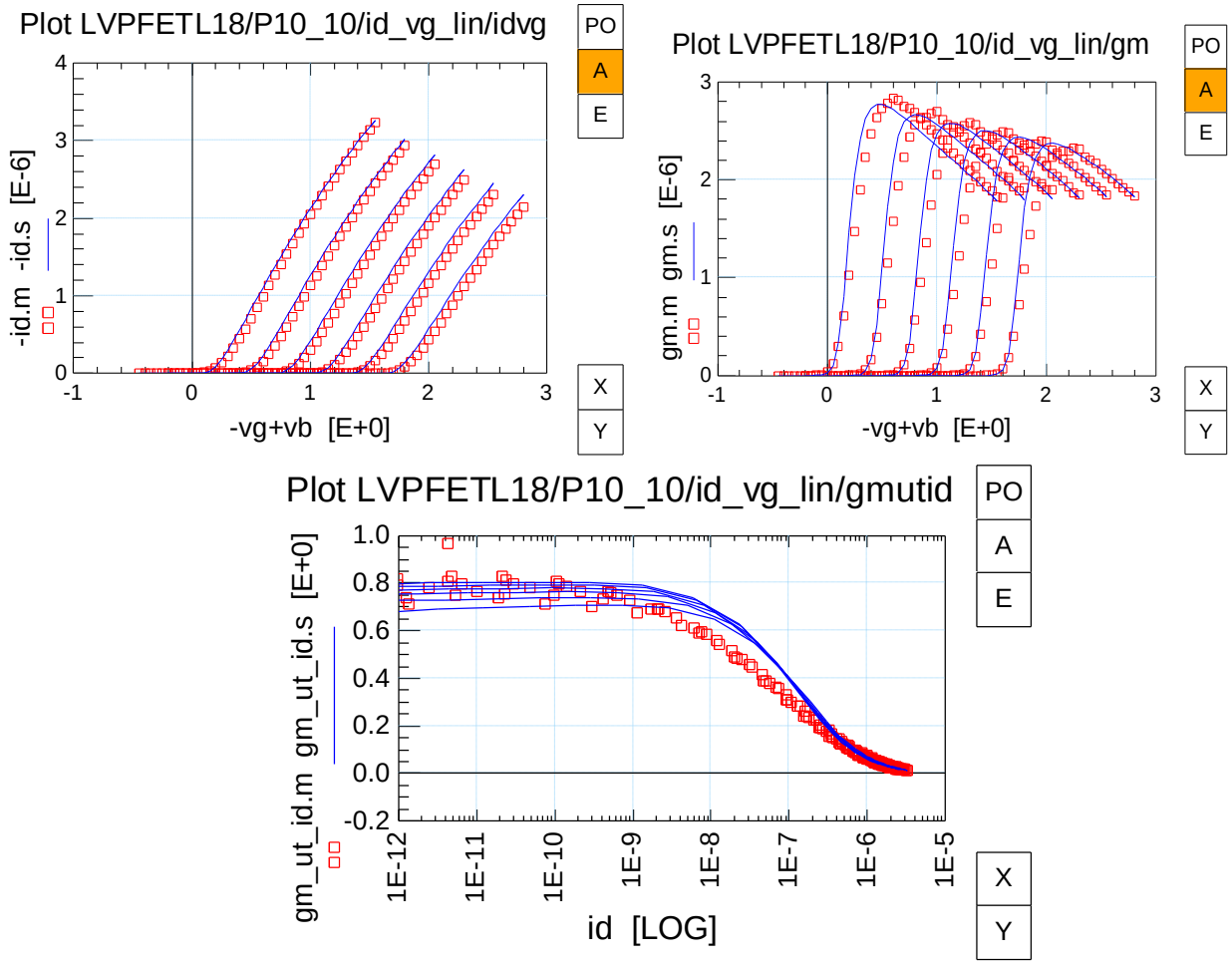
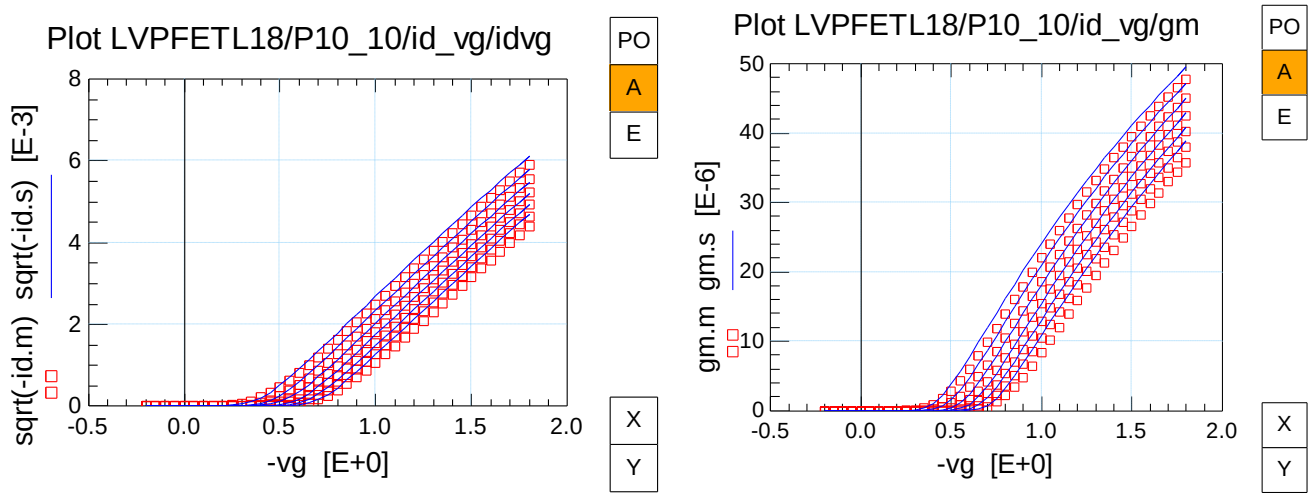


Fig. 1.56: Output Characteristics I_{DS}-V_{GS} g_m-$V_{GS,}$ g_m/I_{DS} Linear Mode(PMOS W/L=10um/10um)



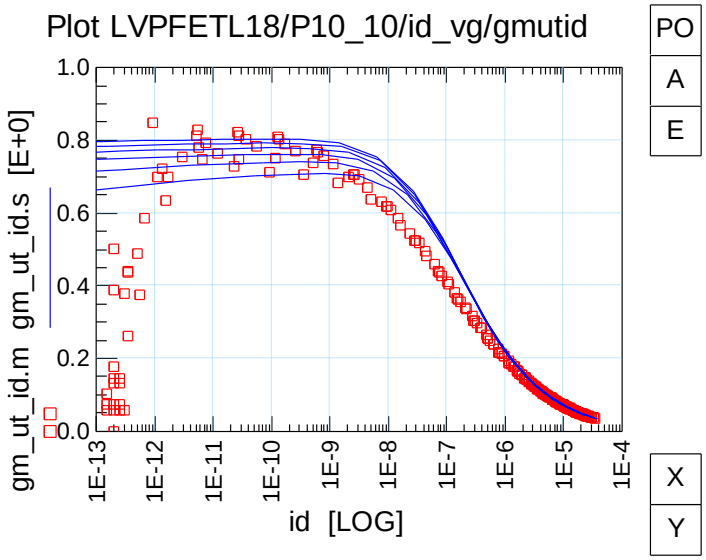


Fig. 1.57: Output Characteristics I_{DS}-V_{GS} g_m-V_{GS}, g_m/I_{DS} Saturation Region(PMOS W/L=10um/10um)

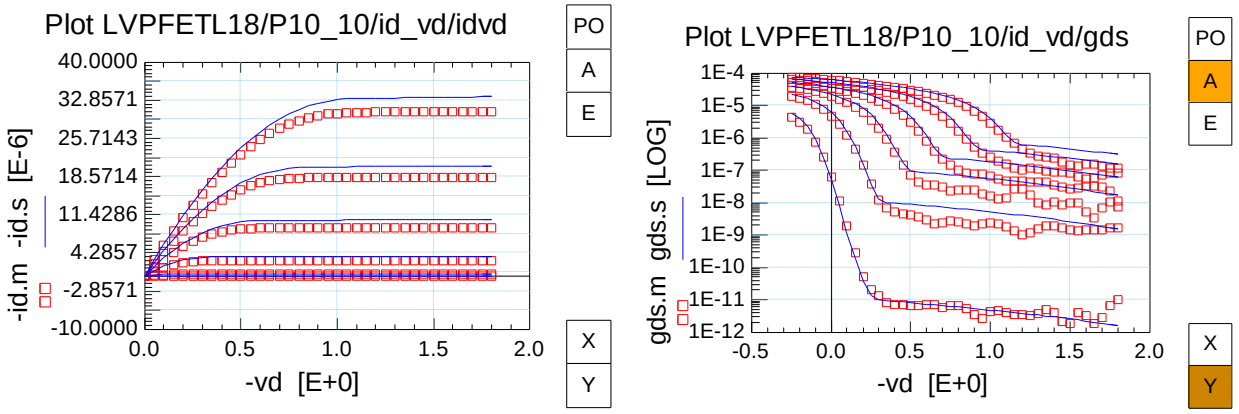
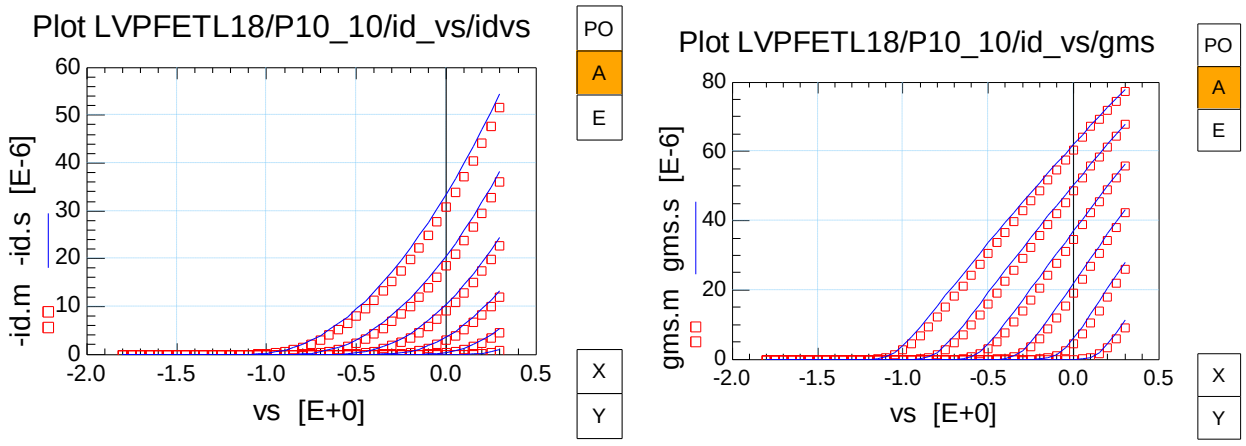


Fig. 1.58: Output Characteristics I_{DS}-V_{DS} g_{DS}-V_{DS} (PMOS W/L=10um/10um)



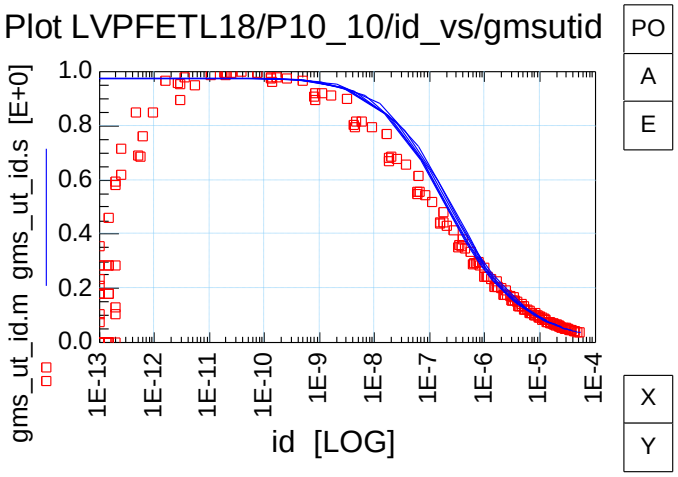


Fig. 1.59: Output Characteristics I_{DS}-V_S g_{ms}-V_S, g_{ms}/I_{DS} (PMOS W/L=10um/10um)

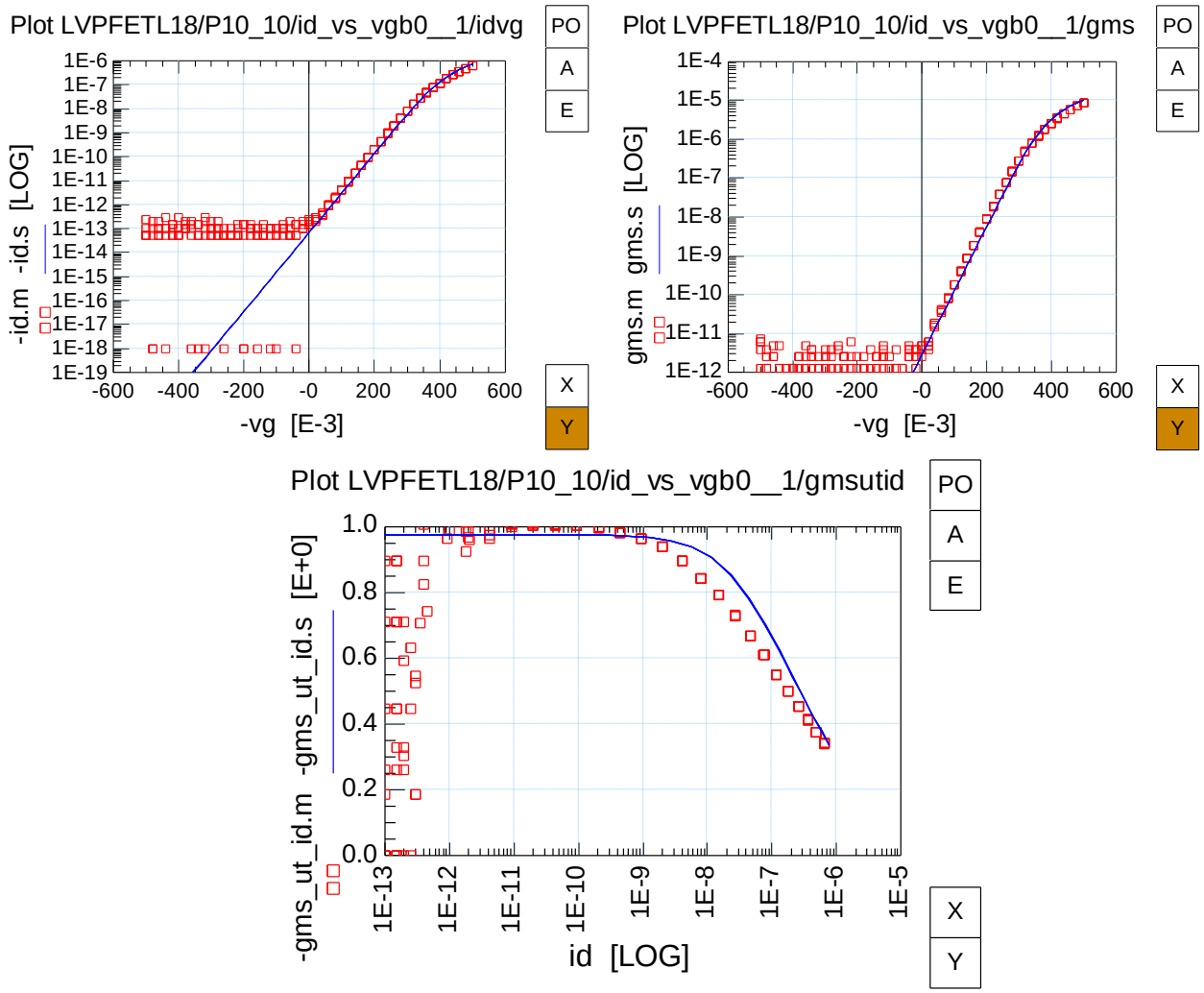


Fig. 1.59: Output Characteristics I_{DS}-V_S g_{ms}-V_S, g_{ms}/I_{DS} V_G=V_B (PMOS W/L=10um/10um)

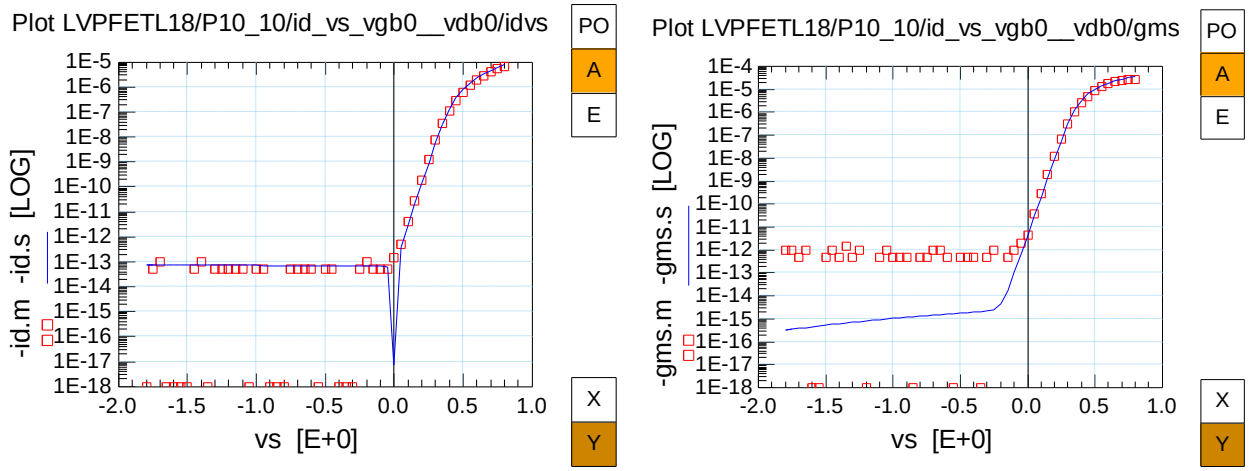


Fig. 1.60: Output Characteristics I_{DS}-V_S g_{ms}-V_S, V_G=V_B= V_D (PMOS W/L=10um/10um)

PMOS W/L=10um/0.18um (wide/short)

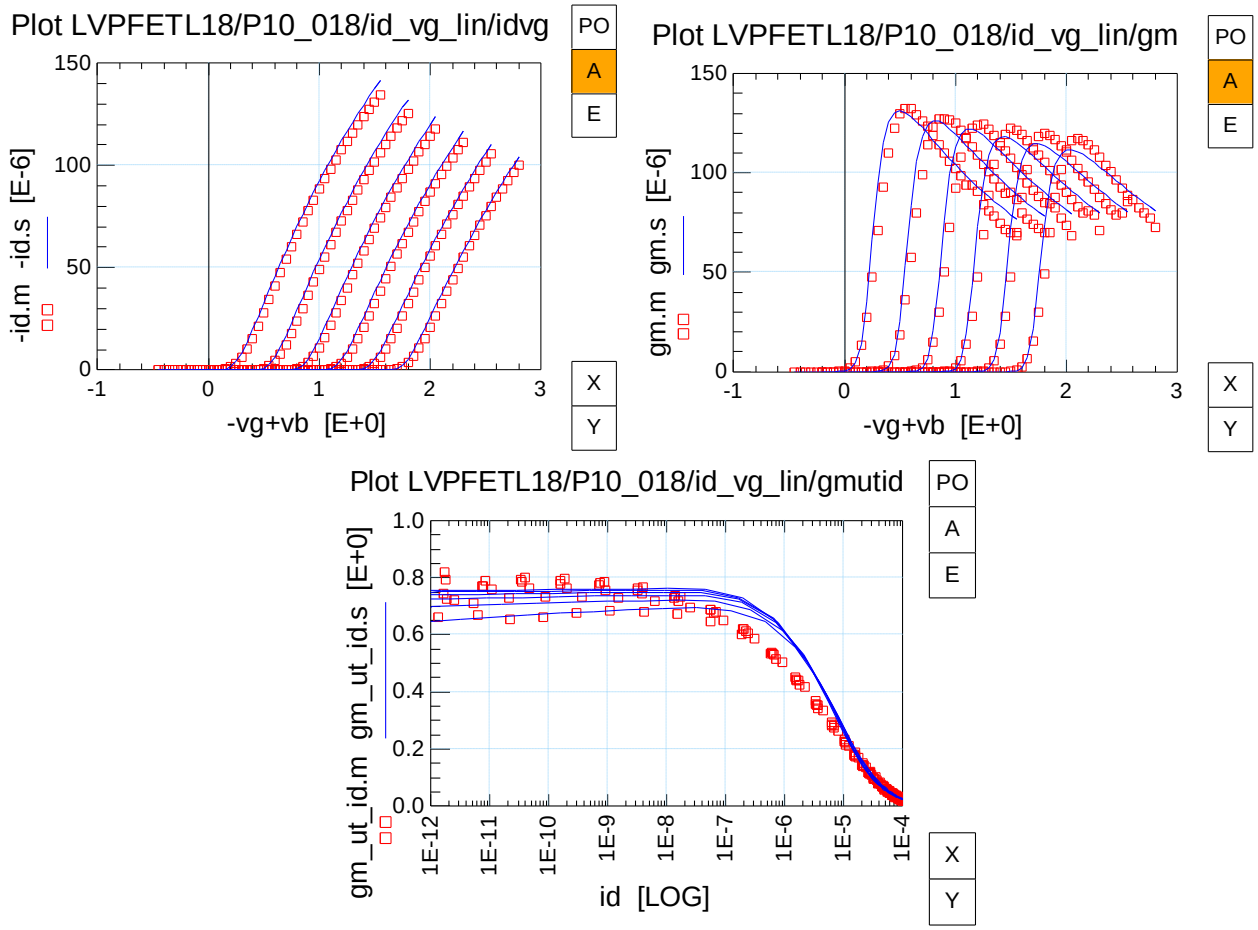


Fig. 1.61: Output Characteristics I_{DS}-V_{GS} g_m-V_{GS}, g_m/I_{DS} Linear Mode (PMOS W/L=10um/0.18um)

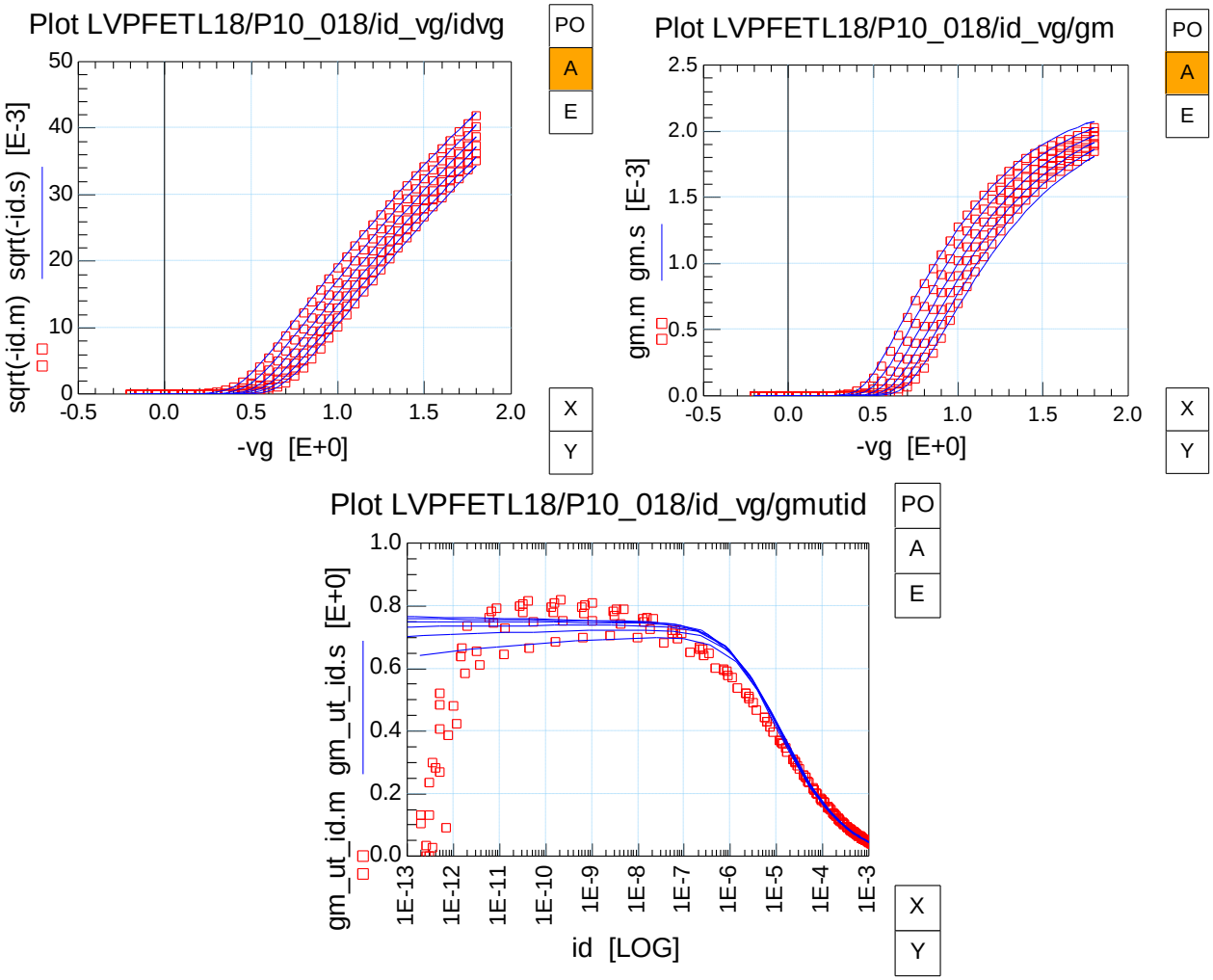


Fig. 1.62: Output Characteristics I_{DS}-V_{GS} g_m-V_{GS}, g_m/I_{DS} , Saturation Region (PMOS W/L=10um/0.18um)

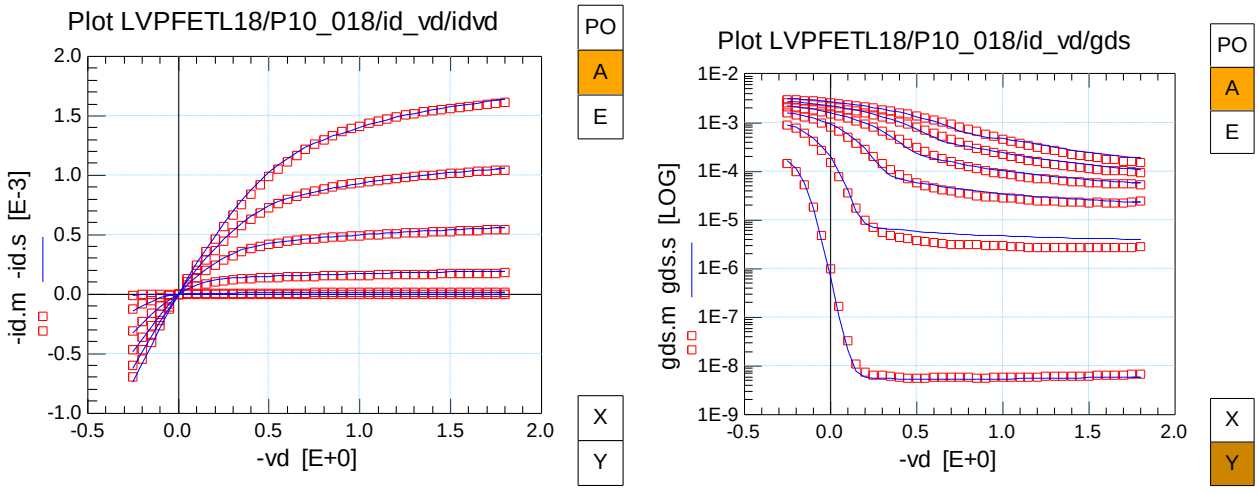


Fig. 1.63: Output Characteristics I_{DS}-V_{DS} g_{DS}-V_{DS} (PMOS W/L=10um/0.18um)

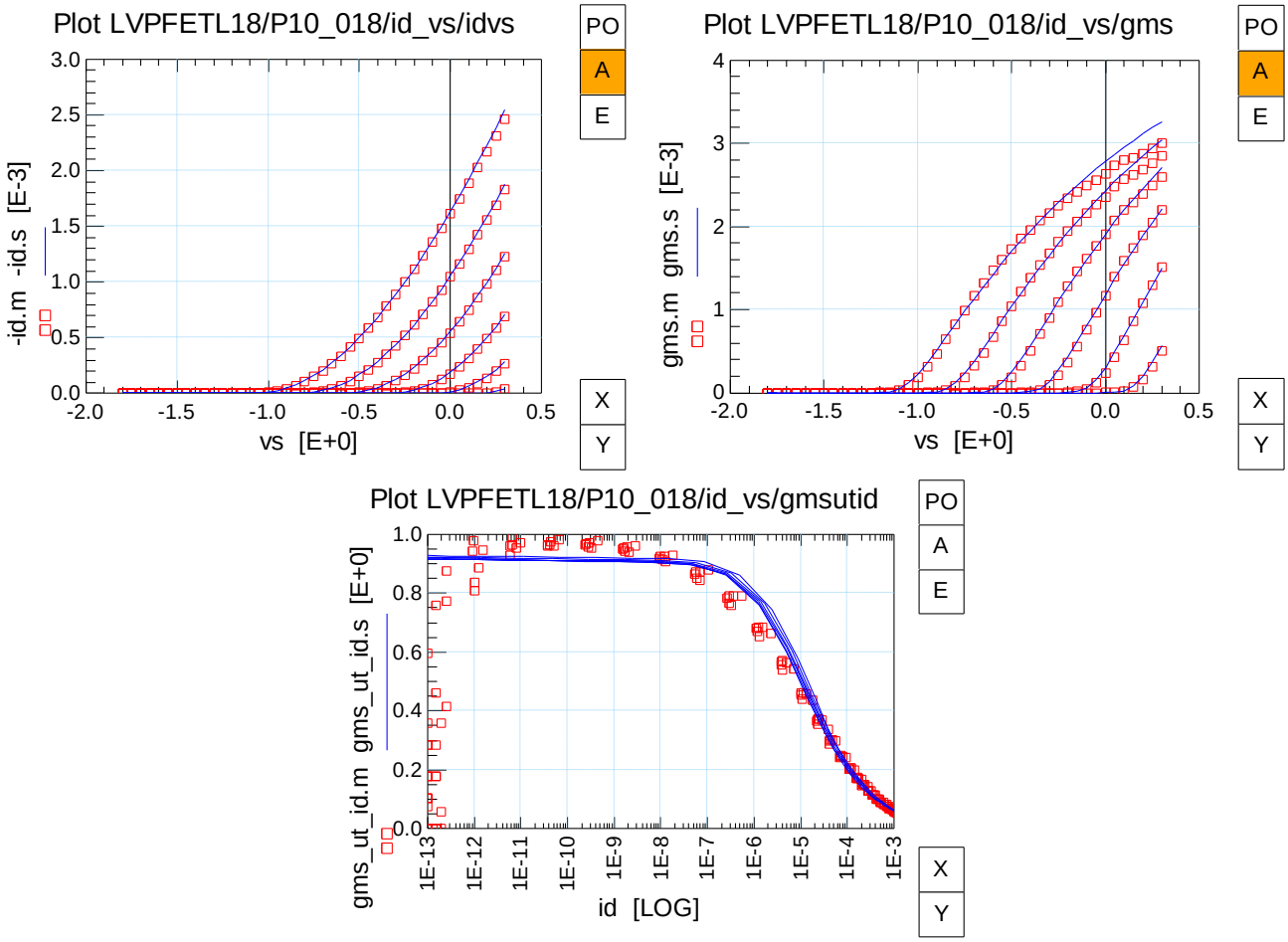
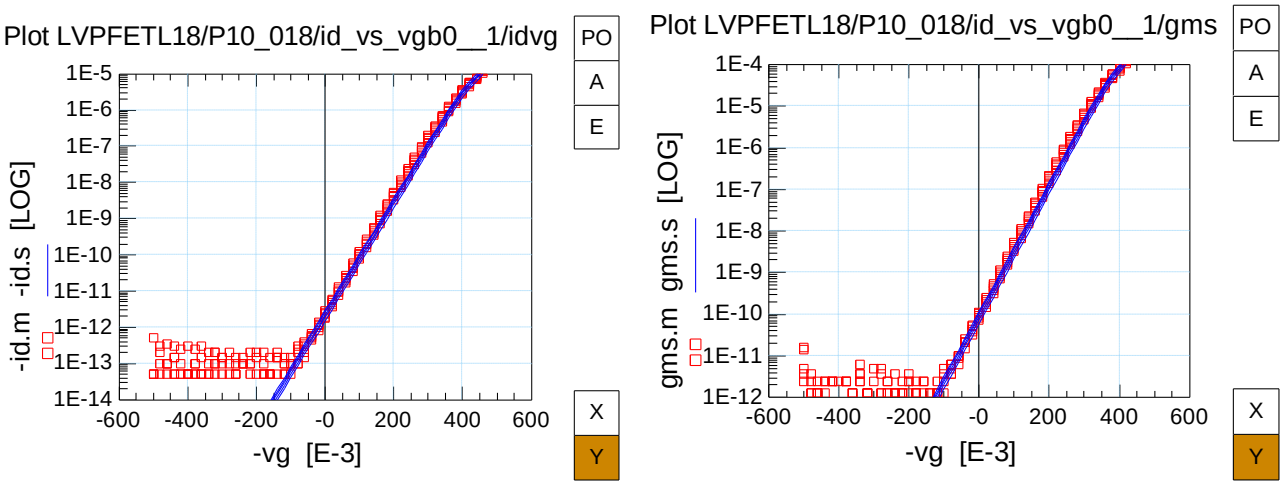


Fig. 1.63: Output Characteristics I_{DS}-V_S g_{ms}-V_{DS}, g_{ms}/I_{DS} (PMOS W/L=10um/0.18um)



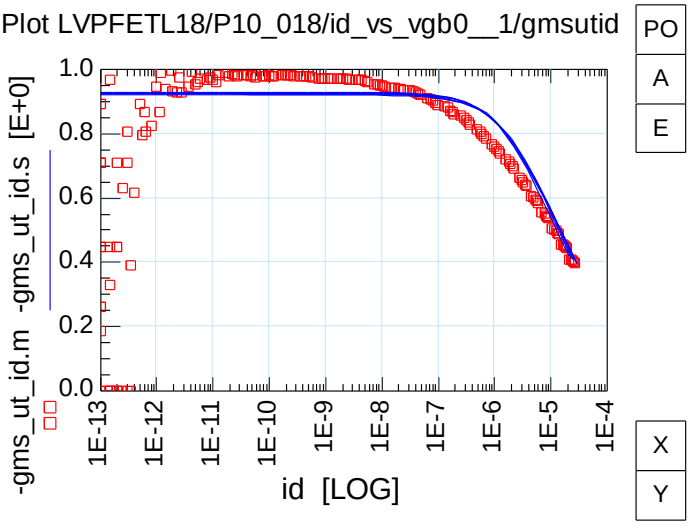


Fig. 1.64: Output Characteristics I_{DS}-V_S g_{ms}-V_{DS}, g_{ms}/I_{DS} V_G=V_B (PMOS W/L=10um/0.18um)

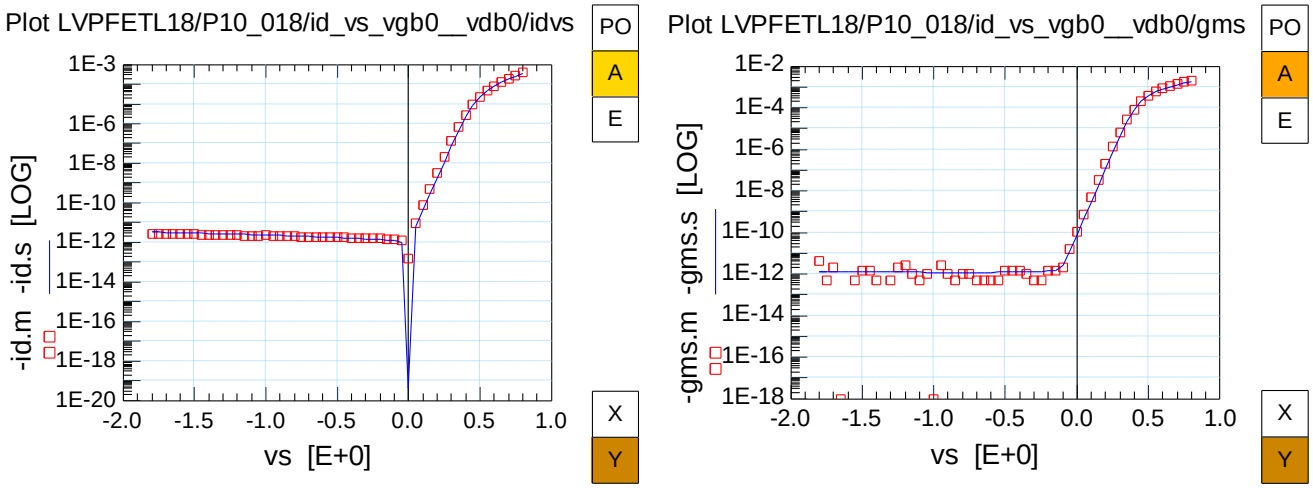


Fig. 1.64: Output Characteristics I_{DS}-V_S g_{ms}-V_{DS}, V_G=V_B=V_D (PMOS W/L=10um/0.18um)

1.4.7 EKV301.02 Parameter Extraction Methodology

The parameter extraction procedure that was followed in order to extract the set of parameters of 180nm and 45nm technology nodes for both topologies source-bulk and drain-bulk connected MOS transistors, include specific and accurate steps. This procedure is depicted in Fig. 1.69 below:

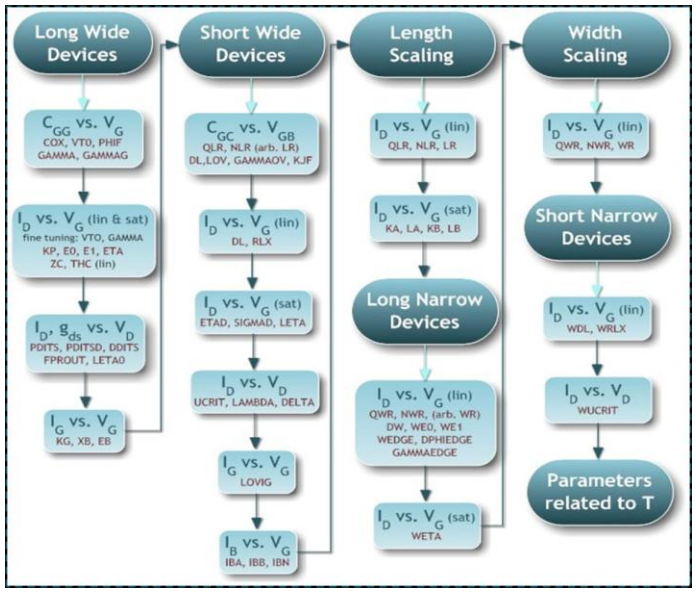


Fig. 1.69: DC parameter extraction basic scheme

The parameter extraction was based on the procedure proposed by [11], [12]. The following table shows the parameter extraction procedure in detail:

	1. $W = W_{MAX}$ $L = L_{MAX}$	2. $W = W_{MAX}$ $L = L_{MIN}$	3. $W = W_{MAX}$ $vs.\ L$
$C_{GG}\ vs.\ V_G$	COX, VTO, PHIF, GAMMA, GAMMAG	DL, LOV, GAMMAOV, KJF, CJF	
$I_D\ vs.\ V_G$ (lin)	KP, E0, E1, ETA, THC, ZC	DL, RLX	QLR, NLR, LR
$I_D\ vs.\ V_G$ (sat)	KP, E0, E1, ETA	ETAD, SIGMAD, LETA	KA, LA, KB, LB
$I_D\ vs.\ V_D$		UCRIT, LAMBDA, DELTA	
$I_G\ vs.\ V_G$	KG, XB, EB	LOVIG	
$I_B\ vs.\ V_D$		IBA, IBB, IBN	

	4. $W = W_{MIN}$ $L = L_{MAX}$	5. $vs.\ W$ $L = L_{MAX}$	6. $W = W_{MIN}$ $L = L_{MIN}$
$I_D\ vs.\ V_G$ (lin)	DW, WE0, WE1	QWR, NWR, WR	WDL, WRLX
$I_D\ vs.\ V_G$ (sat)	WETA		
$I_D\ vs.\ V_D$			WUCRIT

	7.1. $W = W_{MAX}$ $L = L_{MAX}$ $vs.\ T$	7.2. $W = W_{MAX}$ $L = L_{MIN}$ $vs.\ T$
$I_D\ vs.\ V_G$ (lin)	TCV, BEX, TE0EX, TE1EX	TCVL, TR
$I_D\ vs.\ V_G$ (sat)	BEX, TE0EX, TE1EX	
$I_D\ vs.\ V_D$		UCEX

Table 1.1: EKV301.02 Parameter Extraction Methodology. The table is parsed first by columns and then by rows.

CHAPTER 2:Ultra-Low Voltage Analog Design, Challenges and Opportunities

2.1 Introduction

"Analog" is analogous to real life. In real life, most things are continuous with respect to time. Analog circuits provide the connection between the physical world and the digital computing signal-processing systems. As such the true power of digital signal and information processing can only be exploited if analog interfaces with corresponding performance are available.

The low power supply voltages and the relatively large device threshold voltages are an obstacle to high performance analog circuit design. Smaller supply voltages result in smaller available signal swing. To reduce circuit errors from thermal noise or offset voltages, often circuit power consumption has to be increased [18–21]. In addition, devices used in high speed linear circuits need to be biased in moderate or strong inversion with a minimum voltage over-drive, ($V_{GS} - V_T$) of about 0.2 V, resulting in a $V_{DS.sat}$ requirement of about 0.15 V. Typical analog circuits require a supply voltage that is several $V_{DS.sat}$ plus the signal swing, or a V_T plus several $V_{DS.sat}$ plus the signal swing. At supply voltages below 1 V, the design of analog circuits becomes very challenging since the traditional circuit techniques do not have sufficient voltage headroom [20–25].

These challenges can be addressed with technology modifications or with circuit design solutions. A straightforward technology solution is to add thick oxide devices that are less aggressively scaled; these are slower but can operate, without breakdown, with larger supply voltages. The other technology modification is to include low-V_T [26] or native, zero-V_T devices. These devices will offer some extra headroom in circuits [27], but as reported in [50], the main design challenge of enabling circuit operation with reasonable voltage swing, remains unaddressed with low-VT or native zero-VT devices.

Low-V_T devices require an extra mask and extra semiconductor processing steps, resulting in an increase in cost and turn-around time. This cannot be justified when the analog interfaces occupy only 5-30% of the die area on large system-on-chip (SoC) circuits. Native zero-V_T devices do not require any extra mask or processing steps, but are typically less characterized and modeled and sometimes have less reproducible characteristics.

On the other hand, there are several circuit techniques that have been proposed allowing circuit design at low voltages, without using floating-gate devices, special low V_T devices, or native zero-V_T devices. Back-gate or body driven circuits have been proposed in [28–30]. [31] demonstrates input level-shifting techniques, allowing for ultra-low power supply voltages. Rail-to-rail input stages [32, 33], and multi-stage amplifiers with nested Miller compensation [32, 34, 35] have been proposed for low voltage circuits. Analog circuit blocks and amplifiers have been designed, operating at 1 V [30, 36, 37] and down to 0.9 V [38].

In this work low voltage circuit design techniques at a power supply voltage as low as 0.5 V, in standard CMOS technologies, have been developed and demonstrated. Voltages at all nodes in the circuit are within the power supply rails at all times. In Section 2.2, we will take a close look at the circuit design challenges at ultra-low power supply voltages. This will be followed by a discussion, in Section 2.3, on the various design opportunities that open up at ultra-low power supplies.

2.2 Low-voltage analog circuit design challenges

With a supply voltage of 0.5 V and a V_T of at least 0.2 V, devices in practical circuits can be expected to have a maximum $|V_{GS}|-|V_T|$ of 0.2 V, i.e, the devices will be at the edge of strong inversion.

For applications requiring high bandwidths or high clock and sampling rates, the MOS devices in the circuit are biased in the strong inversion region, i.e, for an NMOS device, $V_{GS}-V_T \geq 0.2V$ [39]. As long as $V_{DS} \geq V_{DS,sat}$ where $V_{DS,sat} = 2U_T\sqrt{IC+1/4}+3U_T$, the device is in saturation, or in other words, acts as a voltage controlled current source.

At the edge of strong inversion, a good estimate of $V_{DS,sat}$ is about 0.15 V. The devices can also be operated in weak inversion, with a reduced V_{GS}, i.e, for an NMOS device, $V_{GS} - V_T \leq 0$ V. Weak inversion operation results in a much higher transconductance/current (g_m/I_D) efficiency and is useful for low power applications [40]. However the bandwidth offered by the use of a device in weak inversion is considerably less.

The gate-source bias of the device, V_{GS}, on the other hand, directly controls the inversion of the device and the bias current through the device. To bias a device in a given region of inversion with a given bias current, the required V_{GS} depends on the V_T.

The simplest arrangement to get amplification from a MOS device is the common source configuration with a single-device active load, as shown in Fig. 2.1 (a). For a V_{DD} of 0.5 V, and a $V_{DS,sat}$ of 0.15 V, at the optimal output (drain) bias voltage of $V_{DD}/2$ or 0.25 V, the maximum peak-peak output swing, $V_{out,pp}$, is $V_{DD}-2V_{DS,sat}$ or 0.2 V. The signal swing allowed at the input (gate) depends on the V_T of the device, and is likely to be small. However, as long as there is a large gain between input and output, this is not a strong limitation.

With a 0.5 V supply, in a common drain configuration as shown in Fig. 2.1(b), the output can swing sufficiently. However, because there is no gain from the input to the output, and because of stacking of the output bias and V_{GS} bias, the DC bias voltage at the gate is very high. This limits the available swing at the gate.

In a common gate configuration the input signal, as shown in Fig. 2.1(c), output signal and $3V_{DS,sat}$ are stacked. Even if we assume a large voltage gain for the stage, the available output swing is too small for most applications. A common gate stage (or folded cascode) can be embedded in an amplifier if followed by sufficient gain so that no significant swings are needed at the common gate output. Similarly, cascode topologies with all devices in saturation are excluded at 0.5 V since they require a stack of the output swing and $4V_{DS,sat}$ (about 0.6 V).

Of the basic transistor configurations only the common source configuration has the potential to operate at supply voltages of 0.5 V. It is again important to remark that this limitation stems from the required $V_{DS,sat}$ of about 0.15 V and is independent of the value of V_T.

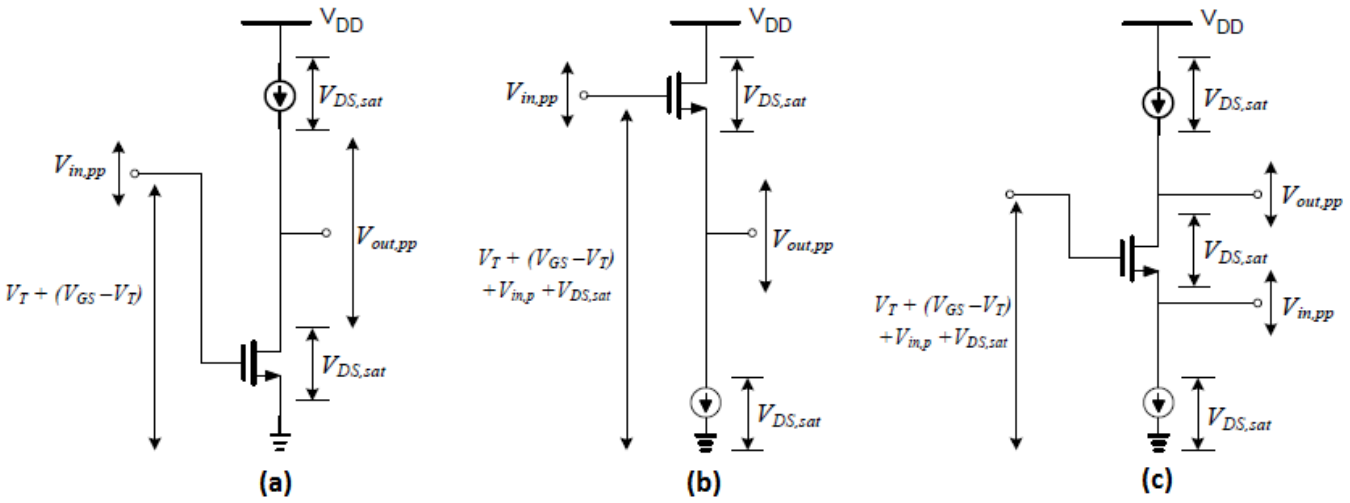


Fig. 2.1: Single-stage Amplifiers

The two major challenges in designing an amplifier at a power supply voltage of 0.5 V are therefore:

- A minimum drain-source voltage of $4U_T$ to $5U_T$ is required to maintain the device in saturation. Given the low power supply voltage, this limits the voltage swing at the drain of the device.
- $V_{GS} - V_T$ sets the inversion level of the device. For high speed applications, the device has to be maintained in strong inversion. However, the gate-source voltage is limited by the power supply.

Fully differential circuits are widely used in contemporary analog integrated circuits [41–43] due to their larger signal swing and better supply and substrate interference immunity. At 0.5 V, we have to rely on those properties and fully differential topologies are essential. The correct operation of fully differential topologies relies on the availability of good common-mode rejection. Not only does the differential gain need to be significantly larger than the common-mode gain, the common-mode gain also needs to be sufficiently less than 1, due to the possible presence of positive feedback loops in the common-mode signal paths.

2.3 Opportunities at low voltages

In addition to the gate, the channel of a MOS device can also be controlled from the body. However, this is usually not done, due to concerns of latch-up when a forward bias voltage is applied across the body-source junction.

The phenomenon of latch-up is explained in [43] (pp. 118-120). A typical CMOS circuit consists of NMOS and PMOS transistors, all located close together on the die. A simplified cross section showing one PMOS and one NMOS is shown in Fig. 2.2(a). Parasitic NPN and PNP transistors are also depicted in the same figure. A rearrangement of the way these parasitic bipolar transistors are viewed shows a positive feedback structure in Fig. 2.2(b). If Q_2 is triggered on, with current injected into its base, it switches on Q_1. The emitter-base junction of Q_1 requires about 0.7 V to turn the device on. Q_1 being on, causes further current to flow into the base of Q_2. The p-substrate, thus, latches close to the positive supply rail, while the n-well latches close to the ground potential.

At a supply voltage of 0.5V, even with current injected into the base of Q_2, without the voltage headroom, Q_1 will not be triggered on. As a result, the mechanism of latch-up will fail. However, there still exists a possibility of latch-up in the presence of power-supply transients.

The diminished risk of latch-up enables the use of forward biasing of the body-source junction, and in general, the use of the body terminal of any device as a fourth, controllable terminal. Forward biasing the body-source junction of a device reduces the threshold voltage as reported in [44–47].

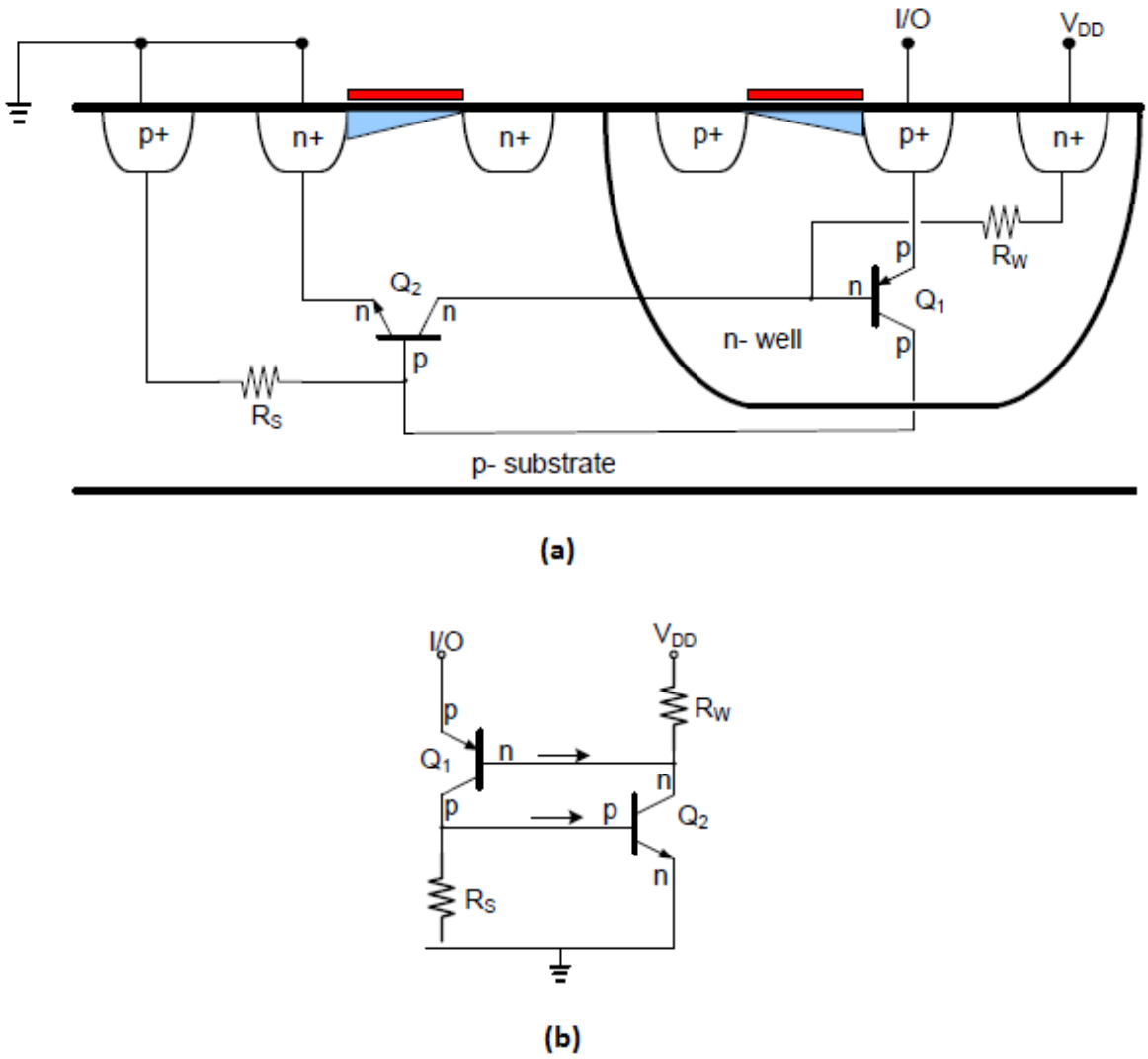


Fig. 2.2: Mechanism of latch-up: (a) Cross-section of simple CMOS circuit with one NMOS and one PMOS (b) Re-arrangement of parasitic bipolars shows a positive feed-back structure

Traditionally only the body terminal of PMOS devices could be accessed in n-well processes, but modern CMOS processes offer the availability of NMOS devices in a separate well or with buried deep n-well layers, so that their body terminal can be accessed independently, as shown in Fig. 2.3. Isolated NMOS devices in a deep n-well process (Fig. 2.3(a)) track their un-isolated counterparts in the same

process, because of similar doping profiles. On the other hand, in a triple-well process (Fig. 2.3(b)), the isolated NMOS device is different in characteristic from its un-isolated counterpart, where the doping profile is markedly different. In both cases, access to the body node of a device has an area penalty. This area penalty is of little concern if the design is limited by other larger components, such as capacitors or inductors. Also, several NMOS devices which are connected to the same body potential can be grouped together in the same well to reduce the total area use. In any case, the area increase is small in comparison to the area of the digital circuits.

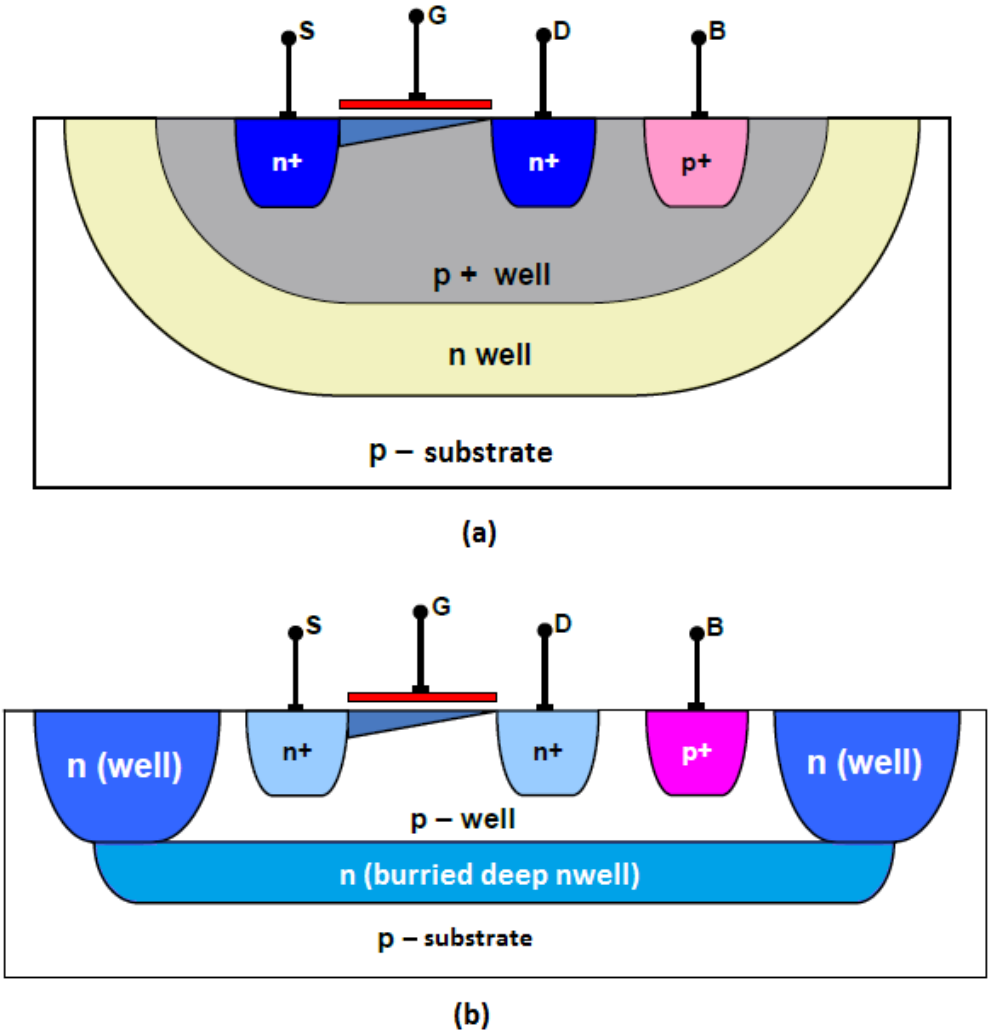


Fig. 2.3: Conceptual cross-sectional view of isolated NMOS devices: (a) with a buried deep n-well layer, (b) in a triple-well CMOS process

2.4 Body Effect

As reported in [48], in semiconductors physics, the threshold voltage V_T of an NFET is usually defined as the gate voltage for which the interface is "as much n-type as the substrate is p-type". It can be proved [49] that,

$$V_T = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{OX}} (2.1)$$

where Φ_{MS} is the difference between the work functions of the poly-silicon gate and the silicon substrate [48].

The body effect appears when the bulk voltage of an NFET drops below the source voltage (see Fig. 2.4). Since the S and D junctions remain reverse-biased, we surmise that the device continues to operate properly but certain characteristics may change. To understand the effect, suppose $V_S = V_D = 0$ and V_G is somewhat less than V_T so that a depletion region is formed under the gate but no inversion layer exists. As V_B becomes more negative, more holes are attracted to the substrate connection, leaving a larger negative charge behind, as shown in Fig.2.5, the depletion region becomes wider. Now recall from Equation (2.1) that the threshold voltage is a function of the total charge in the depletion region because the gate charge must mirror Q_d before an inversion layer is formed. Thus, as V_B drops and Q_d increases, V_T also increases. This is called the "body effect" or the "back-gate effect".

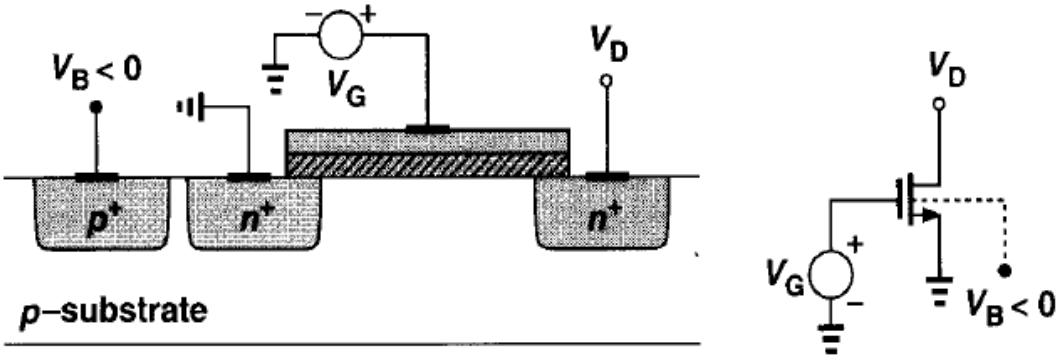


Fig. 2.4: NMOS device with negative bulk voltage

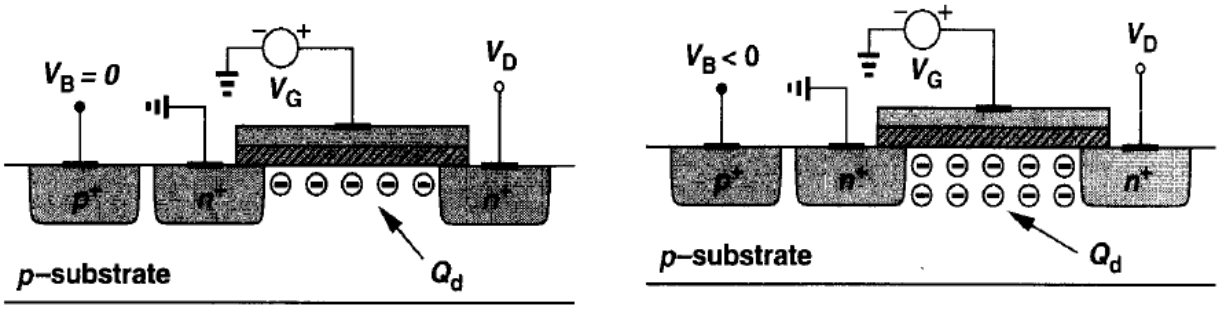


Fig. 2.5: Variation of depletion region charge with bulk voltage

It can be proved that with the body effect:

$$V_T = V_{T0} + \gamma\left(\sqrt{\varphi_0 + V_{SB}} - \sqrt{\varphi_0}\right) (2.2)$$

where V_T is the threshold voltage [48], $\gamma = \sqrt{2q\varepsilon_{si}}/C_{ox}$ denotes the body effect coefficient, and V_{SB} is the source-bulk potential difference [48].

Furthermore, the effect of the body on the device V_T is also explained [39] (pp. 101-103) with the help of Fig. 2.6. When the body and source are at the same potential (Fig. 2.6(a)), there is a depletion region between the n+ source and the p-substrate. The same depletion region continues, when in strong inversion, beneath the channel, where there is an abundance of free electrons. For the same V_{GS} in strong inversion, the charge on the gate, which is the positive plate of the capacitor, remains constant. This charge has to be equal in magnitude to the total negative charge, which is the sum of the free charge in the channel and the fixed charge in the depletion region, assuming negligible interface charge. In Fig. 2.6(b), a positive body-source bias voltage decreases the depth of the depletion region. As a result, for the same V_{GS}, the charge in the channel increases, and the threshold voltage, V_T, decreases.

As mentioned above, he V_T of an MOS device has been classically developed [39, 51] for $V_{SB} > 0$:

$$V_T = V_{T0} + \gamma\left(\sqrt{\varphi_0 + V_{SB}} - \sqrt{\varphi_0}\right) (2.3)$$

where, V_{T0} is the value of V_T for a body-source bias of zero, γ is the body-effect coefficient for a given technology, φ_0 is given by:

$$\varphi_0 = 2\varphi_F + \Delta\varphi (2.4)$$

where φ_F is the Fermi-potential and $\Delta\varphi$ is about 6kT/q, i.e about 150 mV at room temperature. Equation (2.3) shows that when V_{SB} on a device is positive and is increased, V_T of the device increases. Equation (2.3) has been rearranged and extended for $V_{SB} < 0$ (or positive V_{BS}), with the help of experimental evidence [53–55].

$$V_T = V_{T0} - \gamma\left(\sqrt{\varphi_0} - \sqrt{\varphi_0 - V_{BS}}\right) (2.5)$$

Equation (2.5) shows that increasing the body-source junction forward-bias decreases the V_T of the device.

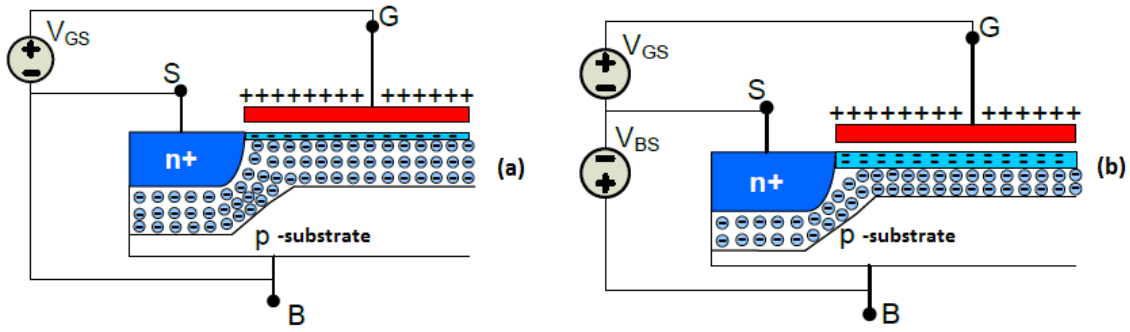


Fig. 2.6: Effect of forward-biasing the body-source junction in a weakly-inverted NMOS device: (a) Depletion and channel charges shown for a given V_{GS} and no body-source forward bias. (b) Depletion and channel charges shown for the same V_{GS} and small body-source forward bias.

A NMOS device of length $1um$ and width $1um$ has been simulated in Advanced Design System using the SGB25 design kit of IHP Microelectronics, which is based on a $0.25um$ CMOS process technology. This device was simulated for fixed gate-source and drain-source voltage but different body-sourced voltages. The extracted threshold voltage of this NMOS device, V_T, is plotted in Fig. 2.7 for different body-source junction voltages ranging from 0V to 500mV with a step size of 10mV. V_T decreases as V_{BS} increases. In [52-54], it is typically used a forward bias which results in a reduction of the threshold voltage V_T.

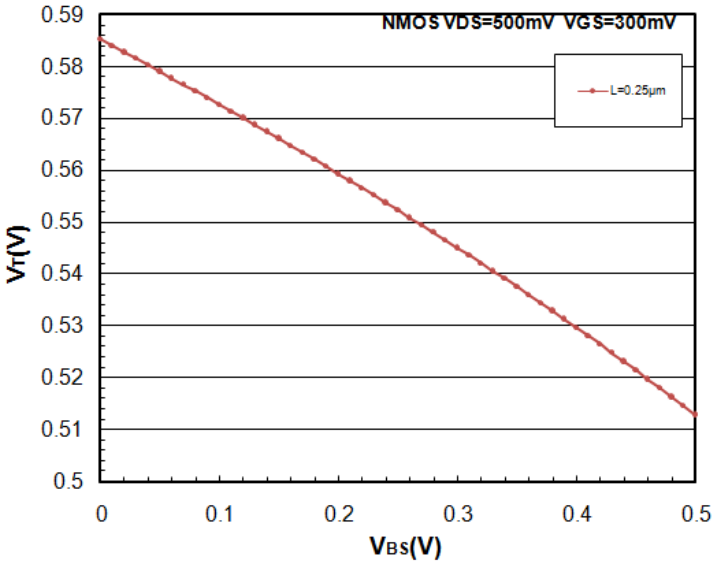


Fig. 2.7: Simulated device V_T as a function of V_{BS}

Fig. 2.8 depicts simulations of device threshold voltage, V_T, as a function of V_{BS} for different technology nodes. Four NMOS devices have been simulated for $0.25um$, $0.18um$, $0.11um$ and $45nm$ CMOS technologies. These four devices of length $1um$ and width $1um$, operate in saturation region and are biased in weak inversion. The relative simple circuits have been simulated in Advanced Design

System for $0.25um$, $0.18um$ technologies, Cadence, Spectre simulator for the $0.18um$ technology and TCAD for the $45nm$ process.

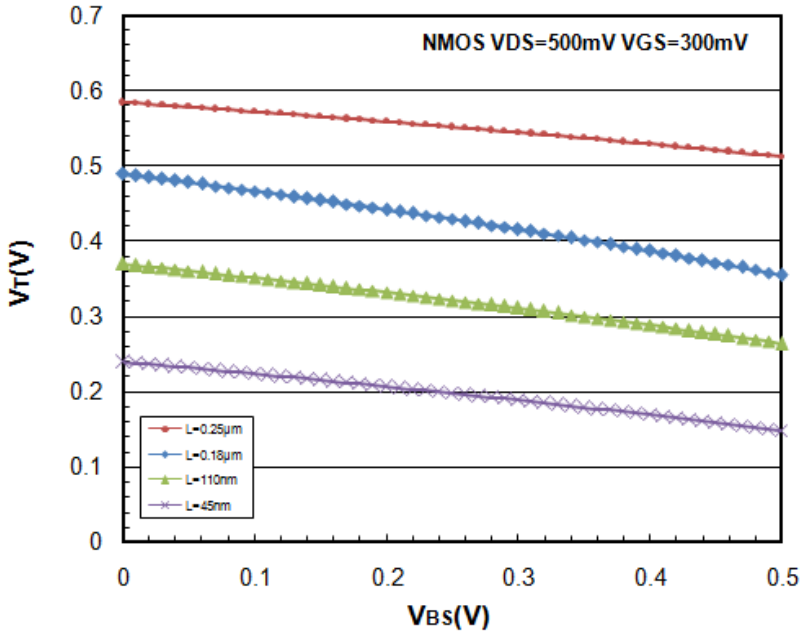


Fig. 2.8: Simulations of device V_T as a function of V_{BS} for advanced technology generations.

The process parameters of each technology are shown in the Table 2.1 below:

CMOS Technology	$0.25um$	$0.18um$	$0.11um$	$45nm$
$V_{TO}(V)$	0.58	0.49	0.38	0.24
$gamma(\sqrt{V})$	0.23	0.42	0.42	0.3
$phi(V)$*	0.95	0.89	0.5	0.94

*The parameter phi is equal to $2\varphi_F$, where φ_F is the quasi-Fermi potential.

Table 2.1: CMOS process parameters used for the device V_T simulations

Forward body bias has been used in digital applications to tune the V_T so that a more consistent circuit performance over process and temperature and thus a higher yield is obtained. These issues are reported in [44,45,55,56]. The availability of the body terminal offers two opportunities. The signal can be applied to the body (back-gate) of the device [28-30,52], whereas the gate is used to bias the device; or, when we apply the signal to the gate, we can use the body (back-gate) to control the bias of the device [53].

CHAPTER 3: Fully Differential Operational Transconductance Amplifiers (OTAs)

3.1 Introduction

An amplifier is one of the most fundamental building blocks of an analog circuit. Fully differential circuits are widely used due to their large available signal swing, and superior supply and substrate interference immunity. In this chapter we will analyze and develop the design of fully differential amplifiers at a 0.5 V supply voltage. The realization of low output impedance is required for the implementation of an operational amplifier. The unavailability of the common-drain stage makes this difficult, and hence we will only discuss the implementation of operational transconductance amplifiers (OTAs).

Forward biasing of the body-source junction, as discussed above, has been applied in these low voltage analog circuits (Fully differential Transconductance amplifiers) and it is applied to lower the V_T of the transistors. In the context of 0.5V operation, the risk of forward biasing the junctions is minimized since parasitic bipolar devices cannot be activated even when the full power supply is used as forward bias, provided that supply transient over-voltages are adequately kept under control.

3.2 Basic Analog Building Blocks

3.2.1 Current Mirrors

One of the basic building blocks in an OTA is a current mirror which acts as a current source. The design of these current sources in analog circuits is based on "copying" currents from a reference, with the assumption that one precisely-defined current source is already available.

For a MOSFET, if $I_D = f(V_{GS})$, where $f(\cdot)$ denotes the functionality of I_D versus V_{GS}, then $V_{GS} = f^{-1}(I_D)$. That is, if a transistor is biased at I_{REF}, then it produces $V_{GS} = f^{-1}(I_{REF})$, as depicted in Fig. 3.1. Thus, if this voltage is applied to the gate and source terminals of a second MOSFET, the resulting current is $I_{out} = ff^{-1}(I_{REF}) = I_{REF}$. From another point of view, two identical MOS devices that have equal gate-source voltages and operate in saturation carry equal currents, neglecting the channel-length modulation.

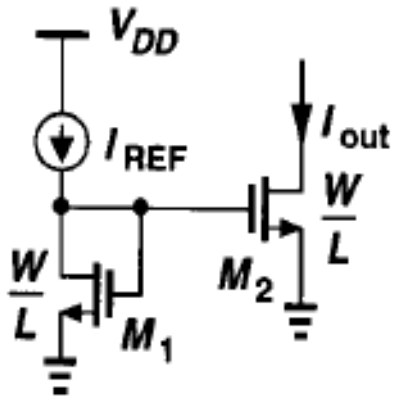


Fig. 3.1: Simple current mirror

The structure consisting of M_1 and M_2 in the Fig. 3.1 above is called, as mentioned before, a "current mirror". In the general case, the devices need to be identical. Neglecting channel-length modulation and assuming that the devices are in saturation region, we can write:

$$I_{REF} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_1 \left(V_{GS} - V_{TO}\right)^2$$

$$I_{out} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_2 \left(V_{GS} - V_{TO}\right)^2$$

obtaining

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

The key property of this topology is that it allows precise copying of the current with no dependence on process or temperature. The ratio of I_{out} and I_{REF} is given by the ratio of device dimensions, a quantity that can be controlled with reasonable accuracy.

3.2.2 Gate-Input OTA

The OTA developed in this work uses gate inputs with the body terminal for adaptive biasing. The forward biasing of the body terminals is applied only in the context of 0.5V operation.

In the basic differential amplifier, as shown in Fig. 3.2, the input differential pair, M_{1A} and M_{1B} and the active loads M_{2A} and M_{2B} amplify the differential input voltage. The resistors R1A, R1B, provide common-mode feedback through the active load. A level-shifting current I_L develops a 200mV drop across R_{1A} and R_{1B} to maintain V_X around 250mV so that M_{2A} and M_{2B} operate in moderate inversion or in lower. The bodies of M_{2A} and M_{2B} are connected to the gates to further reduce their threshold voltage V_T. In addition, to lower the V_T, the body of the input devices M_{1A} and M_{1B} is forward biased.

The ratio of the transconductance of M_{1A} and M_{1B} to the total transconductance of M_{2A} and M_{2B} sets the common-mode gain. In the process used, the PMOS transconductance is not sufficiently large compared to the NMOS transconductance to obtain a low common-mode gain. Therefore a common-mode feed-forward cancellation path [57], [58] is added, as shown in Fig. 3.4, through M_{5A} M_{5B} , M_6 and M_{3A} , M_{3A} . In M_{3A} , M_{3B} and M_6 , the gate and the body are connected to each other to obtain a forward bias across the body-source junctions; this pushes these devices towards moderate and weak inversion.

The small-signal equivalent circuit of a gain stage of the OTA of Fig. 3.4 is shown in Fig. 3.6. The overall DC small-signal differential gain is:

$$A_{diff} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{ds4} + 1/R - g_{m4}} \quad (3.1)$$

The common-mode small-signal gain is given by:

$$A_{CM} = \frac{g_{m1} - 2g_{m5}\dfrac{g_{m3}+g_{mb3}}{g_{m6}+g_{mb6}}}{g_{m4}+g_{m2}+g_{mb2}} \quad (3.2)$$

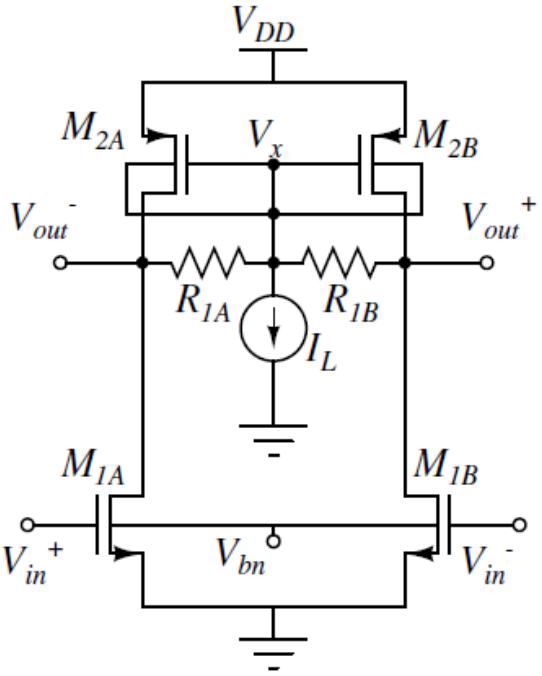


Fig. 3.2: Basic configuration of gate-input OTA

As depicted in Fig. 3.2, the simple OTA circuit consists of a pseudo-differential input pair $M_{1A} - M_{1B}$, where a tail current does not exist. This configuration is similar with the circuit that is shown in Fig. 3.3 (a) below. The question is what happens if V_{in1} and V_{in2} experience a large common-mode disturbance or simply do not have a well-defined common-mode dc level when a tail current does not exist at the same time? As the input CM level, $V_{in,CM}$, changes, so do the bias currents of M_1 and M_2, thus varying both the transconductance of the devices and the output CM level. The variation of the transconductance in turn leads to a change in the small-signal gain while the departure of the output CM level from its ideal value lowers the maximum allowable output swings. For example, as shown in Fig. 3.3(b), if the input CM level is excessively low, the minimum values of V_{in1} and V_{in2} may in fact turn off M_1 and M_2, leading to severe clipping at the output. Thus, it is important that the bias currents of the devices have minimal dependence on the input CM level.

A simple modification can resolve the above issue. The differential pair can employ a current source I_{SS} to make $I_{D1} + I_{D2}$ independent of $V_{in,CM}$. This current source is connected at the common source

terminals of the devices. Thus, if $V_{in1} = V_{in2}$, the bias current of each transistor equals $I_{SS}/2$ and the output common-mode level is $V_{DD} - R_D I_{SS}/2$.

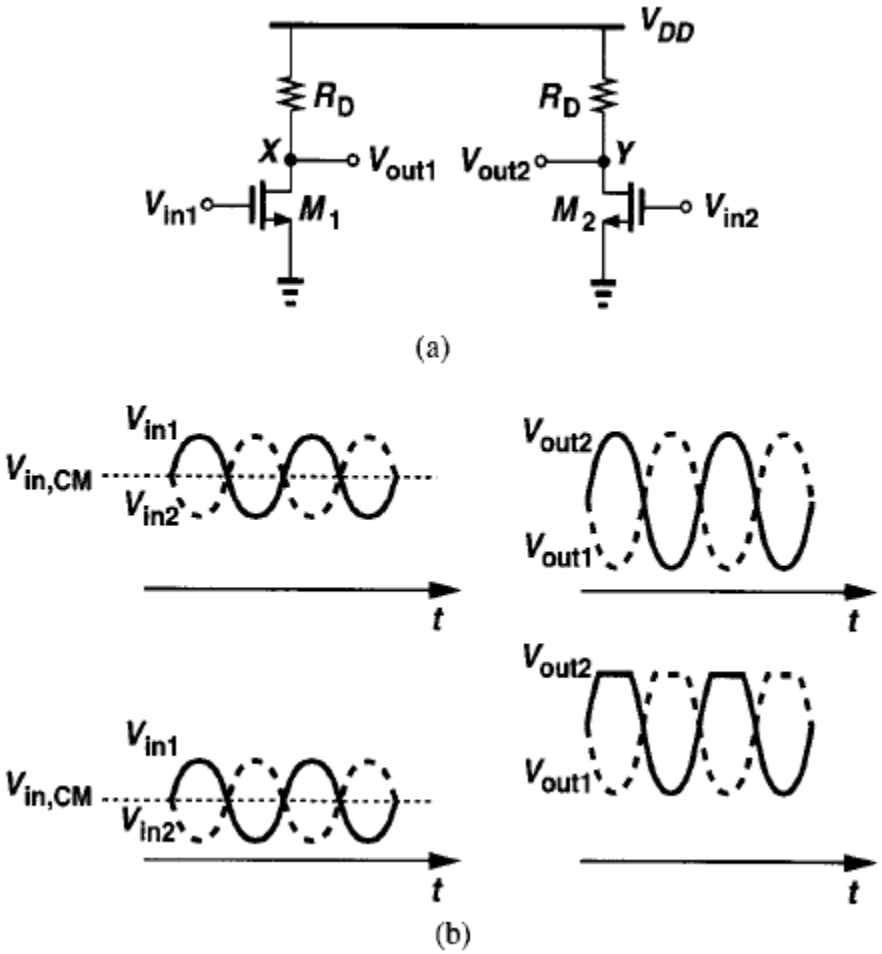


Fig. 3.3: (a) Simple differential circuit, (b) illustration of sensitivity to the input common-mode level

On the other hand, the use of the tail current creates "stacked" devices which in turn limit the available output signal swing. This result is not useful for low voltage design. Therefore, and as mentioned above, a common-mode feed-forward cancellation path is added, as shown in Fig. 3.4, through M_{5A} M_{5B} , M_6 and M_{3A}, M_{3A}.

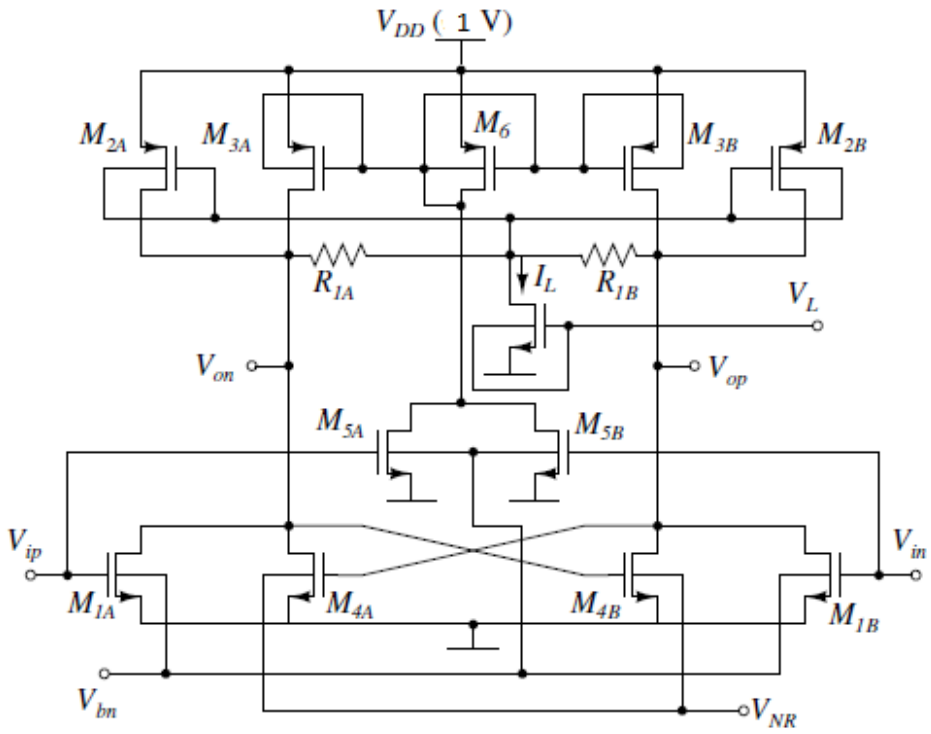


Fig. 3.4: Schematic of the one stage gate-input OTA

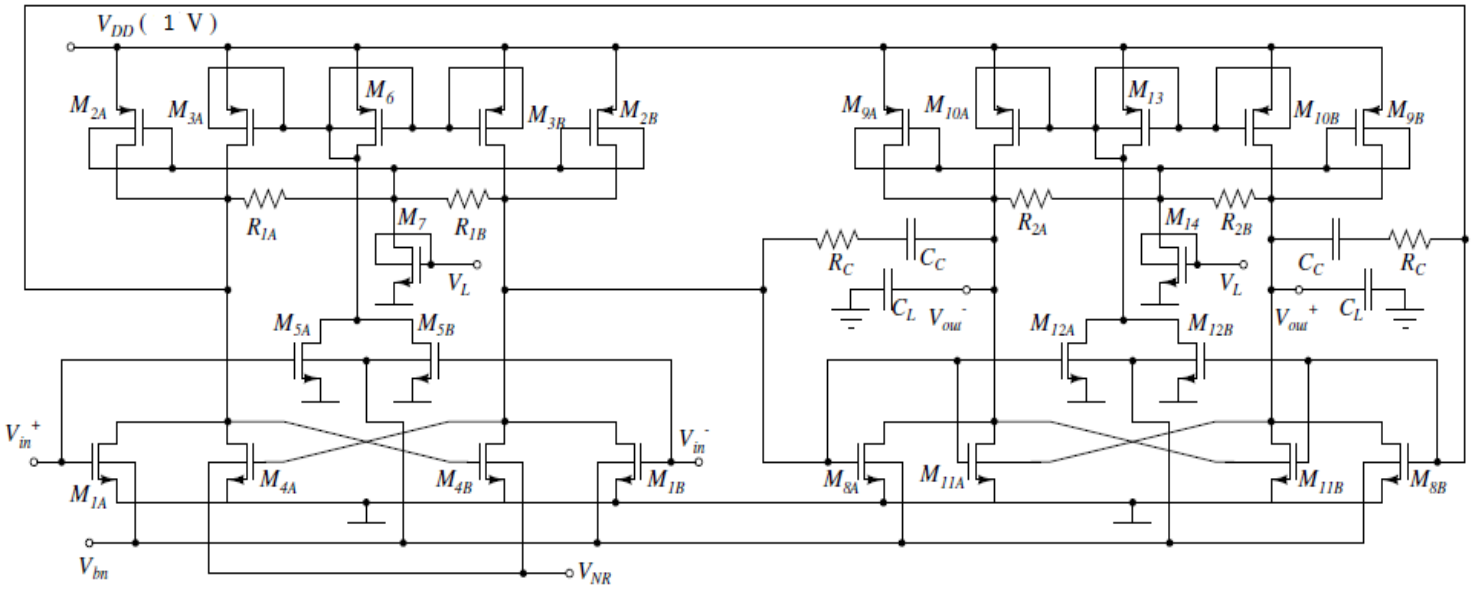


Fig. 3.5: Two stage, fully differential, gate-input OTA, with Miller compensation

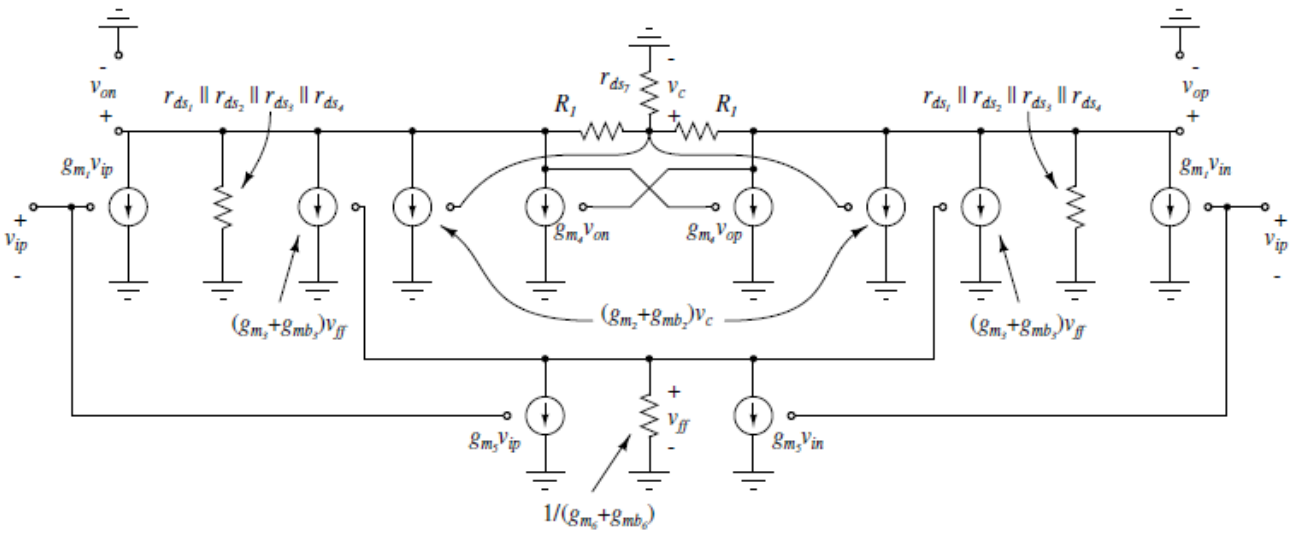


Fig. 3.6: Small-signal equivalent circuit of a single gain stage of the gate-input OTA.

If the aspect ratios W/L of M_1, M_3, M_5, M_6 are such that $M_1/M_5 = M_3/M_6$, the common-mode gain will be zero. In this design, it has been selected that $\frac{M_3}{M_6} = 0.25\frac{M_1}{M_5}$ [50].

The input-referred white noise spectral density is given by:

$$8kT \cdot \frac{2}{3} \cdot \frac{1}{g_{m1}} \cdot \left(1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{m3}}{g_{m1}} + \frac{g_{m4}}{g_{m1}}\right) + \frac{2 \cdot 4kT}{g_{m1}^2 R} \quad (3.3)$$

To obtain a large enough DC gain, two gain stages are cascaded to form a two-stage operational transconductance amplifier. The complete schematic of the two-stage fully differential gate-input OTA is shown in Fig. 3.5. The differential gain is further enhanced with a cross-coupled pair, M_{4A}, M_{4B}, in the first stage which acts as a negative conductance and decreases the output conductance. As an added benefit, the common-mode gain is also further reduced. The body of this cross-coupled pair is set through an on chip automatically controlled bias voltage, V_{NR}. The V_{NR} adapted bias is not discussed in this section and it is out of the purpose of this work. A similar pair, M_{11A} and M_{11B}, is added in the second stage, only its body terminal can operate from the low common voltage at the output and its body transconductance is used to provide a negative conductance; its gate transconductance is in parallel with the input transconductance.

The OTA is stabilized through the Miller capacitors C_C across the second stage. The gain bandwidth product is approximately $g_{m1}/2\pi C_C$ and the second pole frequency of the amplifier is approximately at $g_{m8}/2\pi C_L$ where C_L is the single-ended load capacitance. The series resistor R_C moves the zero

introduced by C_C from the right half plane to the left half plane. This technique is called "Miller Compensation" which is explained in next section.

3.2.3 Negative resistance topology

The negative resistance topology [73] that used in the circuits of this work is depicted in Fig. 3.7(a). Transistors $M_{1p} - M_{1n}$ define a differential pair, where the gate terminals are cross-coupled. In this network, transistor M_{1p} is bias with the current $I_B + i_p$, whereas transistor M_{1n} is biased with the current $I_B + i_n$. Actually, these two devices create a positive feedback loop. Fig. 3.7(b) shows the small signal equivalent of this topology, where G_{1p}, G_{1n} are the gate terminals. Assuming that the transistors have the same dimensions and the output resistance of M_{1p}, M_{1n} is quite high, we have:

$$i_p = -i_n \quad (3.4)$$

$$i_p = g_{m1} v_n \Rightarrow v_n = \frac{i_p}{g_{m1}} \quad (3.5)$$

$$i_n = g_{m1} v_p \Rightarrow v_p = \frac{i_n}{g_{m1}} \quad (3.6)$$

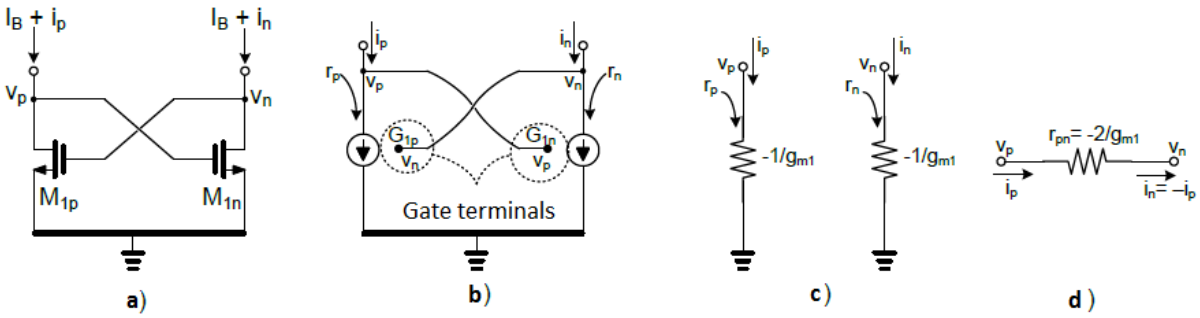


Fig. 3.7: Negative resistance topology

where g_{m1} is the transconductance of M_{1p}, M_{1n}, and v_p, v_n the output voltages. i_p, i_n are the small signal currents of the devices. Therefore, for fully differential currents and for simplicity, it is arrived that:

$$v_p = -v_n \quad (3.7)$$

The resistance that can be "seen" between the v_p, v_n nodes is given by the Equations (3.5) and (3.6) respectively:

$$r_p = \frac{v_p}{i_p} = \frac{-\frac{i_p}{g_{m1}}}{i_p} = -\frac{1}{g_{m1}} \quad (3.8)$$

$$r_n = \frac{v_n}{i_n} = \frac{-\frac{i_n}{g_{m1}}}{i_n} = -\frac{1}{g_{m1}} \quad (3.9)$$

The passive equivalent of these two resistances is shown in Fig. 3.7(c). The small signal resistance that exists between the v_p, v_n nodes has negative value and it is equal to $-1/g_{m1}$. Finally, the differential resistance between the v_p, v_n nodes (the passive equivalent of this resistance is depicted in Fig. 3.7(d)) is given by the Equation (3.10) below:

$$r_{pn} = \frac{v_p - v_n}{i_p} = \frac{-\frac{i_p}{g_{m1}} - \frac{i_p}{g_{m1}}}{i_p} = -\frac{2}{g_{m1}} \quad (3.10)$$

3.3 Frequency Compensation

Nowadays, multistage amplifiers are an essential part when designing in modern technologies, as the single-stage amplifiers cannot live up to the expectations of low-voltage design. Furthermore, short-channel effect of the sub-micron CMOS transistor degrades output impedance and as a result the gain of the amplifier is reduced at a large scale. That makes frequency compensation at multistage amplifiers an essential sector and many frequency-compensation topologies have been reported based on pole-splitting and pole-zero cancelation techniques. These techniques will be explained later on having as an example a 2-stage amplifier. However, in order to reach the optimum results not only provided stability criteria but also trial and error procedure is required. At the same time, it should be noticed that the provided stability criteria find difficulties from theory to practice since any extra stage consumes more power, requires more complicated circuit structure and may reduce the bandwidth dramatically. In order to understand the more complex frequency compensation topologies, it is highly recommended to start examining the frequency response of a single-stage amplifier.

3.3.1 Single-stage amplifier review

Single-stage amplifier's frequency behavior is quite stable since the amplifier has only one left-half-plane (LHP) pole, as it can be noticed from its transfer function.

$$A_{v\sin gle}(s) = \frac{g_{mL} R_L}{1 + sC_L R_L} \quad (3.11)$$

where g_{mL} is the output stage transconductance, R_L is the loading resistance and C_L the loading capacitance, which is in fact the compensation capacitor of the amplifier. The GBW of the amplifier is

obtained by the Equation (3.12).

$$GBW = \frac{g_{mL}}{C_L} (3.12)$$

and the phase margin PM of the amplifier is 90°, because of the single pole. From Equation (3.12) it can be deducted that GBW can be increased, by increasing the g_{mL} factor or decreasing the loading capacitance. However, the existence of many parasitic poles and zeros (p_{par} and z_{par}) should not be neglected as they affect the stability of the amplifier. The transistor's dimensions and the bias current determine the position of the parasitic poles and zeros, frequency of which, as a rule of thumb, should be at least the double of the GBW. In other words, there is a maximum g_{mL} and a minimum C_L for the single-stage amplifier at which min(p_{par}andz_{par})>2GBW.Nevertheless, the dc gain of the single-stage amplifier is relatively small and to deal with this drawback gain-boosting topologies are employed on the initial circuit. However, these topologies require a larger supply voltage, a more complicated circuit design and at the same time limit the maximum output voltage swing. It should be noticed though, that the bandwidth of the amplifier is not affected due to its independence of R_L.

3.3.2 Two-stage amplifier with Simple Miller Compensation (SMC)

As mentioned above single-stage amplifier has excellent frequency response, however cascode configuration maybe be needed in order to increase the gain. Nevertheless, cascode configuration cannot live up to the expectations of the modern demanding low-voltage design. To face this problem two-stage SMC amplifier [59] is commonly used (see Fig. 3.8).

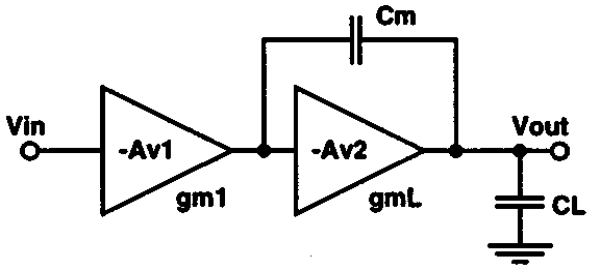


Fig.3.8: SMC amplifier

The transfer function of the above structure is given by:

$$A_{V(SMC)}(s) = \frac{g_{m1} g_{mL} R_{o1} R_L (1 - s\frac{C_m}{g_{mL}})}{(1 + sC_m g_{mL} R_{o1} R_L)(1 + s\frac{C_m}{g_{mL}})} (3.13)$$

It can be noticed that there are two LHP poles and one right-half-plane (RHP) zero. The dominant pole is $p_{-3dB}=1/C_m\, g_{mL}\, R_{o1}R_L$, the non-dominant pole is $p_2= g_{mL}/C_L$ while the RHP zero is $z_1=- g_{mL}/C_m$, where C_m is the compensation capacitor. It is a rule that both p_2 and z_1 should be at frequencies higher than the unity-gain frequency in order to ensure circuit's stability. How can this condition be achieved? An easy solution is to use a relatively large capacitor C_m in order to move the dominant pole to a lower frequency. However by doing this, the GBW is linearly reduced since $GBW=g_{m1}/C_m$.As a result it is suggested that GBW is set to be at the half of the frequency of p_2 in order to obtain a good phase margin and bandwidth at the same time.

$$C_L = \frac{1}{2}\frac{g_{mL}}{g_{m1}} C_m \quad (3.14)$$

If g_{m1} / g_{mL} has a large value then C_m is quite large compared to C_L according to Equation (3.14). In this case, z_1 is at a frequency before or close to the one of p_2, as shown in Fig. 3.9. On the other case where p_2 is before z_1 we receive a small gain and the amplifier shows a quite unstable behavior if there are parasitic poles and zeros. However if z_1 is after p_2 we may have low gain but the phase margin achieves quite good values. In other words the position of the RHP zero sets the tradeoff between gain and the phase margin.

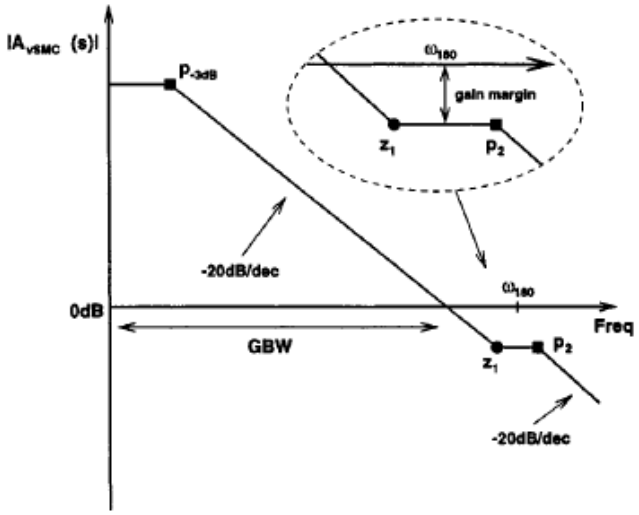


Fig. 3.9: Frequency response of a SMC amplifier

Using Equations (3.13) and (3.14), the GBW product is given by

$$GBW = \frac{g_{m1}}{C_m} = \frac{1}{2}(\frac{g_{mL}}{C_L})(3.15)$$

which compared to the single-stage amplifier has the half value. The GBW of a two-stage SMC amplifier cannot be increased by increasing g_{m1}.This happens because the required C_m is increased proportionally with g_{m1} so the g_{m1}/C_m has a constant value. One way of improving GBW is increasing the output transconductance g_{mL} and decreasing the loading capacitance C_L at the same time. Then the PM is evaluated by the following expression:

$$PM = 180° - \tan^{-1}(\frac{GBW}{p_{-3dB}}) - \tan^{-1}(\frac{GBW}{p_2}) - \tan^{-1}(\frac{GBW}{|z_1|})$$

$$\approx 63° - \tan^{-1}(\frac{g_{m1}}{g_{mL}})(3.16) \quad .$$

By noticing the Equation (3.15) it can be concluded that the PM is highly affected by the g_{m1}/g_{mL} ratio, which in fact reveals the RHP zero effect on the PM. The RHP zero is created by the feed-forward small-signal current that flows through the compensation capacitor C_m to the output. The first way to increase the g_{m1}/g_{mL} ratio is to search for a large g_{mL} .If the g_{mL} is large, then the small-signal output current is larger than the feed-forward current and the effect of the RHP zero appears at very high frequencies. At this work we care about very high frequencies so the problem still exists. As a consequence choosing a smaller g_{m1} is preferable. However there are some limitations when choosing the g_{m1} such as the bias current, which is related to the slew rate, and the size of the input differential pair. Moreover, if the size of the differential pair is relatively small, then there is the danger of having increased offset voltage at the output. All in all, a small g_{m1} cannot be obtained easily. In conclusion, according to the previous analysis, the RHP zero creates serious concerns regarding the stability of the amplifier. To deal with this problem, several methods can be employed such as the addition of a voltage buffer or a nulling resistor to the circuit. The presence of the nulling resistor at the circuit is a technique that will be studied later at this work.

3.3.3 Two-stage amplifier with Simple Miller Compensation with Nulling Resistor (SMCNR)

As mentioned above the feed-forward small-signal current creates the RHP zero. One way to eliminate this zero is to increase the impedance seen at the capacitance path, and this can be done by inserting a resistor to the circuit. The resistor, called nulling resistor, is inserted next to the compensation capacitor as shown in Fig. 3.10.

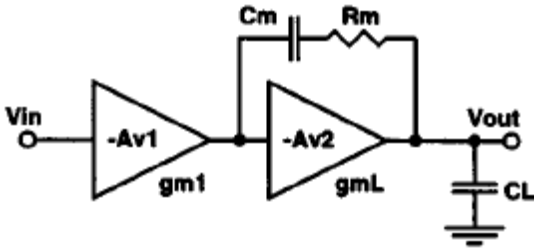


Fig. 3.10: SMCNR amplifier

It is significant to notice that the addition of the resistor affects not only the frequency position of the RHP zero but also the position of the poles. Theoretically speaking, when the value of the nulling resistor reaches infinity, the compensation network is open-circuit and as a result no **pole-splitting** takes place. Pole-splitting will be explained afterwards in this chapter. In other words there are limits regarding both the minimum and the maximum value of the nulling resistor.

The transfer function of the SMNCR (R_m) amplifier is given by:

$$A_{v(SMCNR)}(s) = \frac{g_{m1}g_{mL}R_{o1}R_L[1+sC_m(R_m - \frac{1}{g_{mL}})]}{[1+sC_m(R_m + g_{mL}R_{o1}R_L)][1+s\frac{C_L(R_{o1}+R_m)R_L}{R_m + g_{mL}R_{o1}R_L}]} \quad (3.17)$$

The dominant pole is $p_{-3dB}=1/C_m$ $(R_m+g_{mL}R_{o1}R_L)$, the non-dominant pole is $p_2= (R_m+g_{mL}R_{o1}R_L)/C_L (R_{o1}+ R_{m)\ RL}$ and the zero is $z_1=1/C_m$ $(R_m – 1/g_{mL})$.Later on, it will be proved that when $R_m=1/g_{mL}$ the RHP zero is completely eliminated. In that case, the circuit is in practice a SMC amplifier and the C_m and GBW are given by the Equations (3.14) and (3.15) respectively. Moreover, as proven before, the value of the phase margin is about 63° because of the absence of the zero. However, when using a nulling resistor in design it is preferable to choose a value larger than $1/g_{mL}$ in order to transfer the zero to the left plane and in that way, increases the phase margin. Indeed, observing the transfer function (3.17), when the value of R_m is increased the position of the poles change as they move to lower frequencies. However we should be careful not to overpass the suggested value of R_m because there will be no pole-splitting effect. In other words, it is suggested that the value of R_m lies between $1/g_{mL}$ and $(1/10)R_{o1}$. The upper limit is set by the assumption that the value of R_m is negligible when determining the frequencies of p_{-3dB} and p_2 at the transfer function.

3.3.4 Pole-splitting and zero-cancellation

As mentioned before two important methods in order to utilize the frequency compensation are the pole-splitting and zero-cancellation methods. Studying an example will make it easier to understand not only the significance of the methods but also the way they work. Considering the circuit depicted in Fig. 3.11, three poles p_x, p_E, p_A are identified at nodes X, E and A respectively.

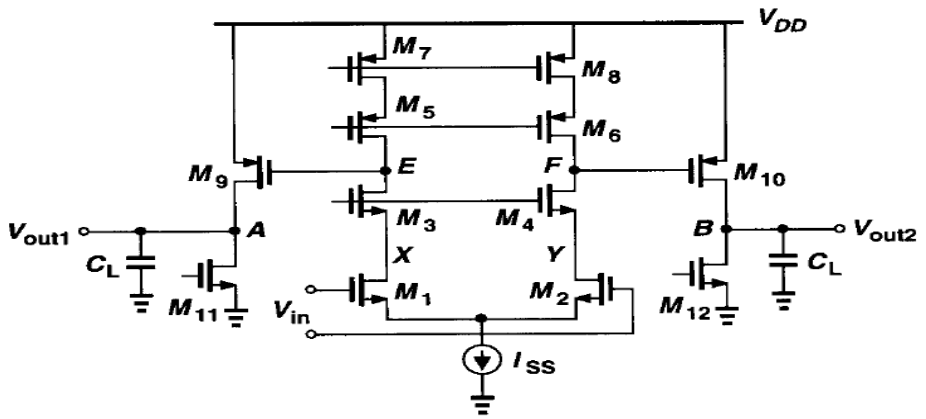


Fig. 3.11: Two-stage op-amp.

Nodes X and Y are the nodes at the sources of the differential pair transistors, so it is known [48] that their frequencies are relatively high. However, examining the rest two poles it will point out that both their frequencies lay near the origin pole. First of all, regarding the p_E this happens because the small-signal resistance seen at E is quite high, which means that M_3, M5 and M_9 are capable of creating a pole close to the origin one. On the other hand, the loading capacitance C_L is quite high at node A and this brings the same result. As a result there are two dominant poles. Assuming that p_E is more dominant than p_A the magnitude and phase plots are constructed as shown below in Fig. 3.12.

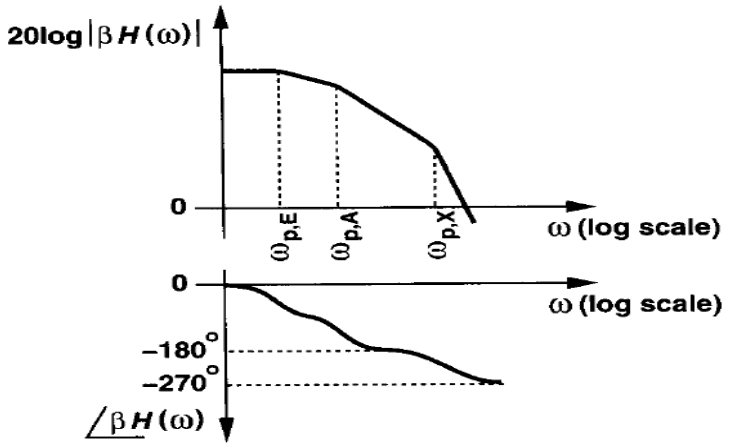


Fig. 3.12: Bode plots of loop gain of two-stage op amp.

It can easily be observed that due to the existence of two dominant poles near the origin, the phase starts to drop quite rapidly after the second pole and before reaching the third. The question is what kind of frequency compensation should be applied to this case.

In Fig. 3.12, one of the dominant poles must be moved toward the origin so as to place the gain crossover well below the phase crossover.However, it is a rule that, the unity-gain bandwidth cannot exceed the frequency of the second dominant pole [48].In case we decide to reduce the magnitude of

p_E ,automatically we limit the bandwidth near the frequency of p_A, which is a small value, not to mention the fact that in order to achieve that we need a large capacitor, which means consuming odd space at the circuit's design.

An effective way to save a considerable amount of chip area is to use the Miller compensation technique. Shown in Fig. 3.13 the initial circuit is a two-stage amplifier, which assumable the first stage exhibits high output impedance and the second adds a moderate gain, conditions which make the employment of the Miller theorem feasible.

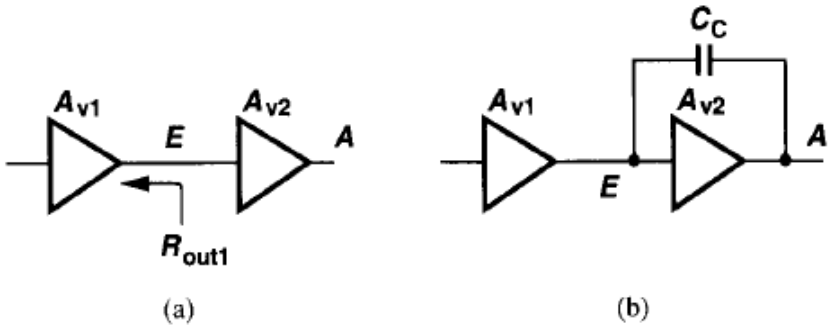


Fig. 3.13: Miller compensation of a two-stage op amp

The goal is to create a large capacitance at node E, but using on the same time a capacitor of moderate size in order to save chip area. The capacitance that is created because of the Miller effect is $C_C\left(1+A_{v2}\right)$ and the total capacitance at node E, which denotes the frequency of the respective pole, is $R_{out}^{-1}\left[C_E+\left(1+A_{v2}\right)C_C\right]^{-1}$ where R_{out1} is the output resistance of the first stage and C_e the capacitance at node E before the addition of C_c. Besides improving the minimum chip area needed the Miller compensation moves the output pole away from the origin. This phenomenon shown in Fig. 3.14 is called **pole-splitting.**

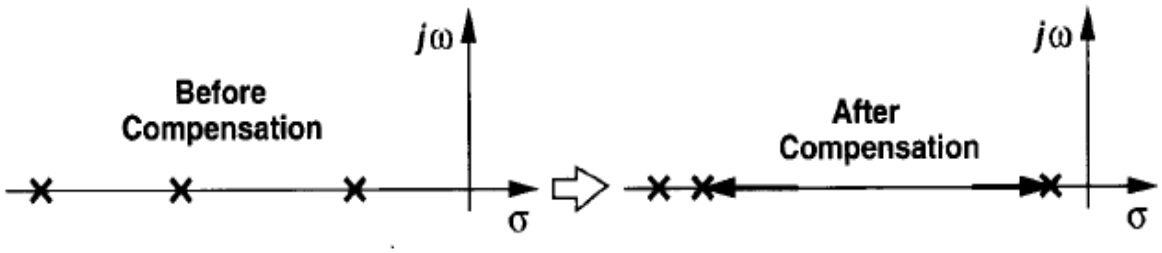


Fig. 3.14: Pole splitting as a result of Miller compensation.

In simple words, the addition of the Miller capacitor moves the inter-stage pole towards the origin and the output pole in the different direction. This results in a far greater bandwidth compared to the occasion that a capacitance is interposed between a node and the ground.

However, during the previous analyses a serious fact was omitted: the presence of zeros in the

transfer function. Whenever Miller compensation is applied, a RHP zero is created, as by doing that a parasitic path is formed from the input to the output. For instance, assuming that the frequency of the zero is ω_z, this is expressed at the numerator of the transfer function as (1-s/ ω_z), producing a phase of $-\tan^{-1}(\omega/\omega_z)$. This is a negative value since ω_z is positive. In that way, like LHP poles, zeros increase the phase shift and move the phase crossover toward the origin. At the same time, a presence of a RHP zero slows down the magnitude curve positioning the gain crossover away from the origin. Combining the last two effects, it is easy to notice that the zero reduces the system's stability.

Fig. 3.15 shows a simplified circuit of a two-stage opamp, and the RHP zero frequency ω_z is given by $g_m/(C_C + C_{GD})$ [48], where C_C is the Miller capacitance. Usually g_m has a small value so ω_z is affected at a large percent by the C_C, which occasionally has a relatively high value, in order to set the dominant pole properly.

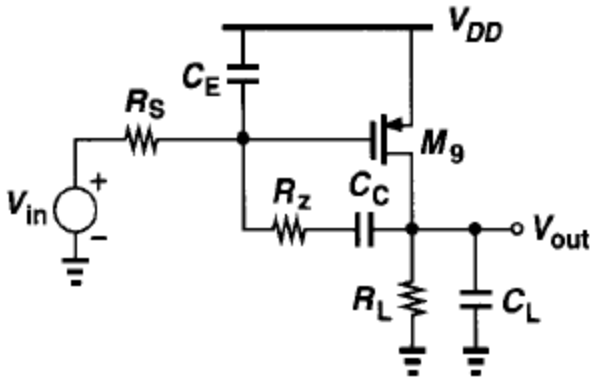


Fig. 3.15: Simplified circuit of two-stage opamp, with the addition of R_z

In order to eliminate the zero R_z resistor is added in series with the compensation capacitor. This happens because the altered ω_z is calculated as

$$\omega_Z \approx \frac{1}{C_C(g_{m9}^{-1} - R_z)} \quad (3.18)$$

One simple way to eliminate the zero would be to set $\omega_z = 1/g_{m9}$. However, it is a design trend to set a R_z so that $\omega_z < 0$. A good reason to move the zero to the left half plane as a way to neutralize the first non-dominant pole, whose frequency is:

$$\omega_{p2} = \frac{-g_{m9}}{C_L + C_E} \quad (3.19)$$

Combining Equations (3.18) and (3.19) and taking into consideration that C_E has typically a much smaller value than C_C, C_L:

$$R_Z \approx \frac{C_L + C_C}{g_{m9} C_C} \quad (3.20)$$

Although canceling the first non-dominant pole is a quite attractive prospect, this method has two disadvantages. First of all, it is not easy to find the exact suitable value for $R_{z,}$ according to Equation (3.20), as C_L in most cases has a variable value since the output of the op-amp for example may be an input to a higher level circuit. As a result, the load capacitance changes. Moreover since R_z a significant value, in order to save space, is substituted by a transistor working in triode region. A random voltage swing may upset the frequency of the zero and in that way preventing it from canceling the non-dominant pole.

CHAPTER 4: Design Optimization

4.1 Inversion Coefficient-Performance Trade-offs

In this work, the design of the OTA circuits is based on selecting the drain current, the inversion coefficient and the channel length of each MOSFET. The level of MOS inversion is considered here using the inversion coefficient, *IC* which is a numerical measure of MOS inversion where unity corresponds to the center of moderate inversion [61]. The inversion coefficient can be found by the drain current, I_D, divided by the product of the specific current I_{Spec}:

$$IC = \frac{I_D}{I_{Spec}} = \frac{I_D}{2nU_T^2\mu_0 C_{OX}\left(\frac{W}{L}\right)} \quad (4.1)$$

Inversion coefficient values less than 0.1 correspond to weak inversion, values between 0.1 and 10 correspond to moderate inversion, and values above 10 correspond to strong inversion. The choice of MOS IC strongly influences transconductance efficiency, g_m/I_D, whereas channel length strongly influences the Early voltage, V_A, or normalized drain–source resistance, where $r_{ds} = V_A/I_D$. Additionally, the inversion coefficient and channel length strongly influence intrinsic voltage gain, capacitances, intrinsic bandwidth, thermal and flicker noise, DC voltage and current mismatch, and other aspects of analog circuit performance.

Selecting drain current, inversion coefficient, and channel length as the three independent degrees of design freedom represents a conceptual shift from the traditional selections of drain current, channel width, and channel length. Selecting the inversion coefficient permits a conscious choice of the region and level of MOS inversion, which is not directly known when making the traditional selections of drain current, channel width, and channel length.

When selecting drain current, inversion coefficient, and channel length as the independent degrees of MOS design freedom, the question arises, "What happens if drain current is changed for a device having a fixed channel width and length?" As observed from $IC = I_D/\left[I_0\left(W/L\right)\right]$, if drain current is increased for a device having fixed channel width and length, *both* the drain current and inversion coefficient increase simultaneously. As a result, g_m/I_D decreases due to the increase in inversion level, represented by the inversion coefficient, while overall $g_m = \left(g_m/I_D\right)\cdot I_D$ usually increases because the increase in drain current usually exceeds the decrease in gm/ID. This obscures optimization choices compared to separately exploring drain current, inversion coefficient, and channel length, which are independent, non-interacting degrees of design freedom. When drain current, inversion coefficient, and channel length are explored separately, MOS channel width must be adjusted to maintain the selected inversion coefficient at the selected drain current and channel length.

When exploring drain current, inversion coefficient, and channel length separately, selecting an initial drain current permits a separate optimization of inversion coefficient and channel length. Holding drain current constant also permits a "fair" optimization where power consumption remains constant. As a result, in this book drain current will normally be selected first and held constant, followed by exploration of the inversion coefficient and channel length. Of course, drain current can also be explored, especially for thermal noise and other parameters that depend strongly on the drain current.

4.2 Simple Predictions of Performance and Trends

For the three independent degrees of MOS design freedom – drain current, inversion coefficient, and channel length – used here, the effective gate–source voltage, $V_{EFF} = V_{GS} - V_T$, could replace the inversion coefficient as the design choice governing the level of MOS inversion. However, MOS drain current, channel width, and gate area are non-linearly linked to the effective gate–source voltage, compared to the simple linkage provided by the inversion coefficient as observed in the expression $IC = I_D/(I_{spec0}*W/L)$. The linkage of selected drain current, inversion coefficient, and channel length to MOS channel width and gate area is described in detail in Section 3.6 of [61]. This simple linkage permits the development of performance predictions that implicitly consider the impact of channel width and gate area on capacitances, intrinsic bandwidth, flicker noise, and DC mismatch. These expressions provide simple predictions and trends of MOS device and circuit performance, continuously valid from weak through strong inversion.

The relation between the drain current and the associated effective gate–source voltage, $V_{EFF} = V_{GS} - V_T$ is given by,

$$I_D = 2 \cdot n \cdot \mu_0 \cdot C_{ox}^{'} \cdot U_T^2 \cdot \left(\frac{W}{L}\right) \cdot \left[\ln\left(1 + e^{\frac{V_{GS}-V_T}{2 \cdot n \cdot U_T}}\right)\right]^2 \quad (4.2)$$

where n is the slope factor, μ_0 the channel mobility and $C_{ox}^{'}$ the gate oxide capacitance.

Furthermore, the drain current of MOS transistors, in saturation region, is given by,

$$I_D = 2 \cdot n \cdot \mu_0 \cdot C_{ox}^{'} \cdot U_T^2 \cdot \left(\frac{W}{L}\right) \cdot IC \quad (4.3)$$

Setting Equations (4.2) and (4.3) equal, we have,

$$2 \cdot n \cdot \mu_0 \cdot C_{ox}^{'} \cdot U_T^2 \cdot \left(\frac{W}{L}\right) \cdot \left[\ln\left(1 + e^{\frac{V_{GS}-V_T}{2 \cdot n \cdot U_T}}\right)\right]^2 = 2 \cdot n \cdot \mu_0 \cdot C_{ox}^{'} \cdot U_T^2 \cdot \left(\frac{W}{L}\right) \cdot IC$$

$$\Rightarrow \ln\left(1 + e^{\frac{V_{GS}-V_T}{2 \cdot n \cdot U_T}}\right)^2 = IC$$

$$\Rightarrow \ln\left(1 + e^{\frac{V_{GS}-V_T}{2 \cdot n \cdot U_T}}\right) = \sqrt{IC}$$

$$\Rightarrow 1 + e^{\frac{V_{GS}-V_T}{2 \cdot n \cdot U_T}} = e^{\sqrt{IC}}$$

$$\Rightarrow e^{\frac{V_{GS}-V_T}{2 \cdot n \cdot U_T}} = e^{\sqrt{IC}} - 1$$

$$\Rightarrow \ln\left(e^{\frac{V_{GS}-V_T}{2\cdot n\cdot U_T}}\right) = \ln\left(e^{\sqrt{IC}}-1\right)$$

$$\Rightarrow \frac{V_{GS}-V_T}{2\cdot n\cdot U_T} = \ln\left(e^{\sqrt{IC}}-1\right)$$

$$\Rightarrow V_{GS}-V_T = 2\cdot n\cdot U_T\cdot \ln\left(e^{\sqrt{IC}}-1\right)$$

$$\Rightarrow V_{EFF} = 2\cdot n\cdot U_T\cdot \ln\left(e^{\sqrt{IC}}-1\right) \quad (4.4)$$

4.3 Observing Performance Tradeoffs – The *MOSFET Operating Plane*

In addition to permitting the prediction of device and circuit performance for all regions of MOS operation, the selection of drain current, inversion coefficient, and channel length permits the observation of performance tradeoffs. Performance tradeoffs are available through the selection of drain current, inversion coefficient, and channel length for individual MOSFETs or related MOSFETs, for example differential pairs and current mirrors, in an analog circuit.

Fig. 4.1 introduces the *MOSFET Operating Plane*, which illustrates performance tradeoffs versus the selected inversion coefficient and channel length for a fixed drain current [62–69]. Each MOSFET or related group of MOSFETs operates at a selected inversion coefficient and channel length, corresponding to a point on the operating plane. Operation at low inversion coefficients in weak or moderate inversion (the left side of the plane) maximizes transconductance efficiency and transconductance, minimizes gate-referred thermal-noise voltage, maximizes drain-referred thermal noise current, maximizes intrinsic voltage gain, and minimizes the effective gate–source bias and drain–source saturation voltages. Since shape factors (S = W/L), channel widths, gate areas, and capacitances are large at low inversion coefficients, intrinsic bandwidth, gate-referred flicker-noise voltage, drain-referred flicker-noise current, and DC gate–source voltage and drain current mismatch are minimized. Conversely, operation at high inversion coefficients in strong inversion (the right side of the plane) minimizes transconductance efficiency and transconductance, maximizes gate-referred thermal-noise voltage, minimizes drain-referred thermal-noise current, minimizes intrinsic voltage gain, and maximizes the effective gate–source bias and drain–source saturation voltages. Since shape factors, channel widths, gate areas, and capacitances are small at high inversion coefficients, intrinsic bandwidth, gate-referred flicker-noise voltage, drain-referred flicker-noise current, and DC gate–source voltage and drain current mismatch are maximized.

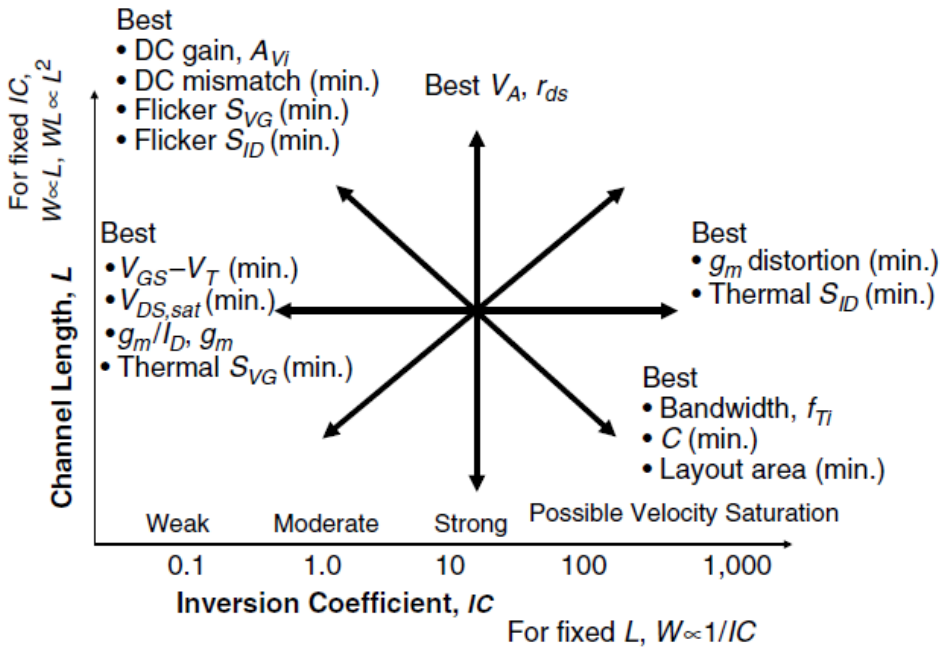


Fig. 4.1: *MOSFET Operating Plane* illustrating MOS analog performance tradeoffs versus selected inversion coefficient and channel length for a fixed drain current. Each MOSFET in an analog circuit operates at some inversion coefficient and channel length defining a point on the operating plane

Operation at short channel lengths (the bottom side of the plane) minimizes drain–source resistance, Early voltage, and intrinsic voltage gain. Since channel width, gate area, and capacitances must decrease with length to maintain the required shape factor, these are small at short channel lengths, maximizing intrinsic bandwidth, gate-referred flicker-noise voltage, drain-referred flicker-noise current, and DC gate–source voltage and drain current mismatch. Conversely, operation at long channel lengths (the top side of the plane) maximizes drain–source resistance, Early voltage, and intrinsic voltage gain. Since channel width, gate area, and capacitances must increase with length to maintain the required shape factor, these are large at long channel lengths, minimizing intrinsic bandwidth, gate-referred flicker-noise voltage, drain-referred flicker-noise current, and DC gate–source voltage and drain current mismatch.

The combination of low inversion coefficients and long channel lengths (the upper left side of the plane) further maximizes intrinsic voltage gain, maximizes gate area and capacitances, minimizes intrinsic bandwidth, and minimizes gate-referred flicker-noise voltage, drain-referred flicker-noise current, and DC gate–source voltage and drain current mismatch. Conversely, the combination of high inversion coefficients and short channel lengths (the lower right side of the plane) further minimizes intrinsic voltage gain, minimizes gate area and capacitances, maximizes intrinsic bandwidth, and maximizes gate-referred flicker-noise voltage, drain-referred flicker-noise current, and DC gate–source voltage and drain current mismatch. These and other performance tradeoffs will become clear during the course of this chapter. Additionally, performance tradeoffs are discussed in detail in Chapter 4 of [61].

Modern, low-voltage analog CMOS design requires lower levels of inversion to keep the drain–source saturation and effective gate–source voltages to sufficiently low values. Thus, design choices are increasing required in weak (IC < 0.1), moderate (0.1<IC<10), and at the onset of strong inversion (IC = 10). As a result, design is increasingly shifting to the left side of the *MOSFET Operating Plane* where inversion coefficient values are less than 10. Since operation in weak inversion at IC < 0.1 provides little

increase in transconductance efficiency but requires larger shape factors, channel widths, and gate areas giving high capacitances and low intrinsic bandwidth, there is little reason to operate in weak inversion compared to the weak inversion side of moderate inversion. This further illustrates the importance of the moderate-inversion region.

Different transistors or transistor groups may be optimized differently, as denoted by different locations on the *MOSFET Operating Plane*. For example, transistors in the signal path may be optimized for tradeoffs in gain, bandwidth, and noise while transistors in DC bias and control paths may be optimized solely for low DC mismatch. The optimization of different transistors in an analog circuit is reported in [61] for cascoded, operational transconductance amplifiers (OTAs) optimized for low thermal noise. Here, input devices are operated at low inversion coefficients for high transconductance efficiency and high transconductance, giving low gate-referred thermal-noise voltage. Conversely, non-input devices are operated at high inversion coefficients for low transconductance efficiency and transconductance, giving low drain-referred thermal-noise current contributions such that input devices dominate the thermal noise. In addition to different inversion coefficient choices, different channel lengths are selected for input and non-input devices for the micro-power, low-noise preamplifier design examples [61]. Here, input devices dominate both thermal and flicker noise. In all cases, visualizing or even marking the location of MOSFET inversion coefficient and channel length selections on the *MOSFET Operating Plane* provides design guidance and intuition that can lead towards optimum design.

The performance tradeoffs shown in the *MOSFET Operating Plane* of Fig. 4.1 assume negligible gate leakage current. However, for gate-oxide thickness around 2 nm and below, gate–source conductance, gate shot- and flicker-noise current, and mismatch due to gate leakage current can affect performance tradeoffs. As a result, operating at arbitrarily long channel lengths where gate area is large may not maximize intrinsic voltage gain and minimize flicker noise and DC mismatch because the large gate area increases gate leakage current and deteriorates performance. A smaller channel length and resulting gate area may be required to balance the traditional improvements in intrinsic voltage gain, flicker noise, and DC mismatch with the deterioration of these associated with gate leakage current.

4.4 Regions and sub-regions of inversion

As mentioned above, the inversion coefficient describes the region and level of MOS inversion from weak through strong inversion as illustrated in Fig. 4.2. The primary regions are weak inversion for $IC < 0.1$, moderate inversion for $0.1 < IC < 10$, and strong inversion for $IC > 10$.

We will define sub-regions of inversion to facilitate discussion of MOS inversion-level choices. The sub-regions are defined in terms of the inversion coefficient and the associated effective gate–source voltage, $V_{EFF} = V_{GS} - V_T$. V_{EFF} can be used to describe the level of MOS inversion, but it is non-linearly linked to drain current and the MOS shape factor, $S = W/L$. The effective gate-source voltage, V_{EFF}, however, is included here since it provides insight and connection to traditional analog CMOS design methods.

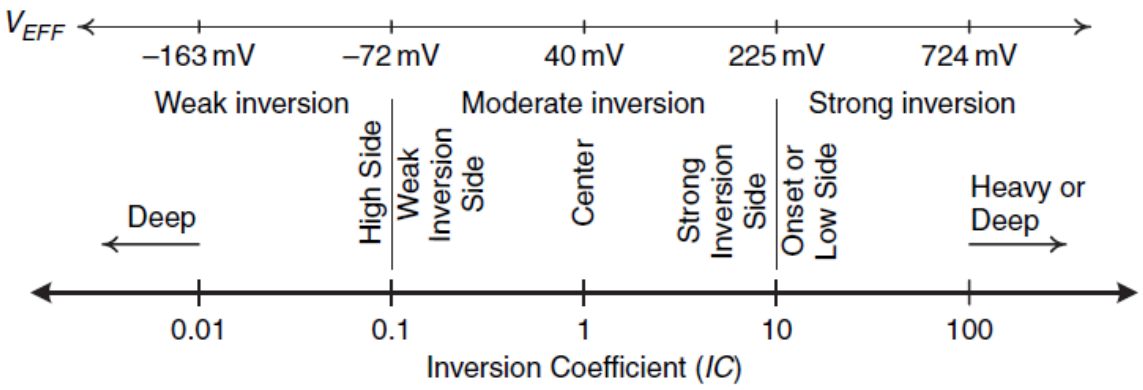


Fig. 4.2: The inversion coefficient presented as a number line showing the regions and sub-regions of MOS inversion with corresponding effective gate–source voltage, $V_{EFF} = V_{GS} - V_T$. The effective gate–source voltage is for room temperature (T = 300K) and an average substrate factor of n = 1.4. It is higher than values shown for short-channel devices operating in strong inversion due to velocity saturation. Moderate inversion is increasingly important in modern, low-voltage processes because of lower allowable effective gate–source and drain–source saturation voltages

The value of V_{EFF} associated with a given *IC*, described in Section 4.2, is approximately −4.5, −2, 1.08, 6.24, and $20nU_T$ for IC = 0.01, 0.1, 1, 10, and 100, respectively. Values given assume U_T = 25.9mV (T = 300K) and a constant value of n at 1.4. Values given exclude the increase associated with velocity saturation present for short-channel devices at high levels of inversion.

The sub-regions of inversion are described below in terms of *IC* and the associated V_{EFF} . Additionally, a few comments about MOS transconductance efficiency, g_m/I_D, effective gate–source voltage, V_{EFF}, drain–source saturation voltage, $V_{DS,sat}$, intrinsic voltage gain, and intrinsic bandwidth are included. These aspects of MOS performance are developed in Sections 3.8.2, 3.7.2, 3.7.3, 3.8.5, and 3.9.6 of reference [61].

The sub-regions of MOS inversion shown in Figure 4.2 are:

- **Deep weak inversion *(IC* < 0.01, V_{EFF} < −163mV).** Because the large device shape factor, channel width, and gate area required results in high gate capacitances, very low bandwidth, and potentially high DC leakage, operation here is not desirable. There is little increase in g_m/I_D or decrease in $V_{DS,sat}$ here compared to the *high side of weak inversion*. Operation may be required here for very low drain currents.
- **High side of weak inversion *(IC* =0.1, V_{EFF} =−72mV).** This occurs at the boundary of moderate inversion. Operation here provides nearly the full g_m/I_D of *deep weak inversion*, low V_{EFF} and $V_{DS,sat}$, high gain, and low bandwidth, although improved bandwidth compared to *deep weak inversion*.
- **Weak-inversion side of moderate inversion** (0.1 < *IC* < 1, −72mV < V_{EFF} < 40mV). This occurs between the boundary of weak inversion and the center of moderate inversion, with IC = 0.3 corresponding to the geometric center between weak and moderate inversion. Operation here provides high g_m/I_D, low V_{EFF} and $V_{DS,sat}$, high gain, and improved bandwidth compared to the *weak-inversion side of moderate inversion*.
- **Center of moderate inversion** (*IC* = 1, V_{EFF} = 40mV). Operation in the center of moderate inversion provides good g_m/I_D, low V_{EFF} and $V_{DS,sat}$, good gain, and modest bandwidth.

- **Strong-inversion side of moderate inversion** (**1 < *IC* < 10, 40mV < V_{EFF} < 225mV**). This occurs between the center of moderate inversion and the boundary or onset of strong inversion, with IC =3 corresponding to the geometric center between moderate and strong inversion. Operation here provides modest g_m/I_D, modestly increasing V_{EFF} and $V_{DS,sat}$, modest gain, and good bandwidth.
- **Onset of strong inversion** (***IC*** = **10, V_{EFF}** = **225mV**)**.** Operation at the onset of strong inversion provides low g_m/I_D, high V_{EFF} and $V_{DS,sat}$, low gain, and very good bandwidth.
- **Low side of strong inversion** (**10 < *IC* < 100, 225mV < V_{EFF} < 724mV**)**.** Operation here provides low and declining g_m/I_D, high and increasing V_{EFF} and $V_{DS,sat}$, low and declining gain, and excellent bandwidth. Because of high V_{EFF} and $V_{DS,sat}$, operation here may not be feasible in low-voltage processes. Additionally, significant velocity saturation reduction in g_m/I_D and increases in V_{EFF} are likely for short-channel NMOS devices. This can also result in saturation or leveling off of bandwidth.
- **Heavy or deep strong inversion (*IC* > 100, V_{EFF} > 724mV)**. Because of the small device shape factor and channel width required, it is increasingly difficult to size devices here. Operation here is generally not useful in modern, low-voltage processes because of the very high V_{EFF} and $V_{DS,sat}$, g_m/I_D and voltage gain are very low, and the velocity saturation effects described for the *low side of strong inversion* are generally severe for short-channel NMOS devices.

It must be noted that moderate inversion is advantageous because V_{EFF} and $V_{DS,sat}$ are moderate (only slightly above their weak-inversion values), permitting low-voltage design. Additionally, g_m/I_D and voltage gain are high, bandwidth is moderate, and velocity saturation reductions in g_m/I_D and increases in V_{EFF} are generally small, even for short-channel devices.

CHAPTER 5: Gate-Input OTA Simulation-Results

5.1 Design Flow

In this chapter, we present the steps that should be followed during the gate-input OTA design. Firstly, the design kit that was used is presented and transistors' characteristics are shown. Also, the next sections present the low-voltage techniques that have been used in order to design and simulate the gate-input OTA at two supply voltages, 1V and 0.5 V following some basic specifications such as Power Dissipation, DC gain, GBW product, Slew Rate, Phase Margin, Input Referred Noise and Common-Mode Rejection Ratio.

5.2 Design Kit

The design kit that used for amplifiers and filters design has been developed by the team in our lab at 0.18 CMOS process based on the EKV2.6 MOSFET model. This model has been extracted and developed in our lab as well**.** EM Microelectronic Marin has provided the wafers that used for MOS devices measuring. For NMOS transistors, the short channel voltage threshold is about 0.49 V, while for PMOS transistors it is -0.463 V. Other useful parameters that have been extracted are given in Table 5.1,

Parameter	NMOS	PMOS
V_{T0}	$0.49V$	$-0.46V$
γ	$0.42\sqrt{V}$	$0.63V$
Φ	$0.89V$	$1.05V$
K_P	$400\,\mu A/V^2$	$65.63\,\mu A/V^2$
$I_{spec0}=2n(U_T)^2K_P$	$646nA$	$114nA$

Table 5.1: Design kit parameters

5.3 Conventional and Drain-Bulk Connected MOSFETS Simulation

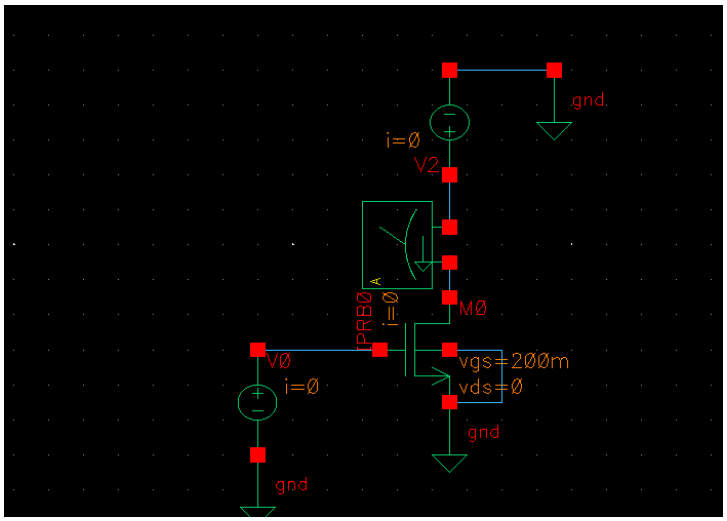


Fig. 5.1: Conventional NMOS simulation setup

Fig. 5.1 shows the setup that has been used in order to simulate a conventional NMOS device in Cadence Tool for two aspects ratios, W/L=10µm/10µm and W/L=10µm/280nm (wide/long and wide/short respectively). This device is biased with a gate voltage that sweeps from 0.2V to 1V and a drain voltage that sweeps from 0V to 1V. The I-V characteristics are depicted in Fig. 5.2 and Fig. 5.3,

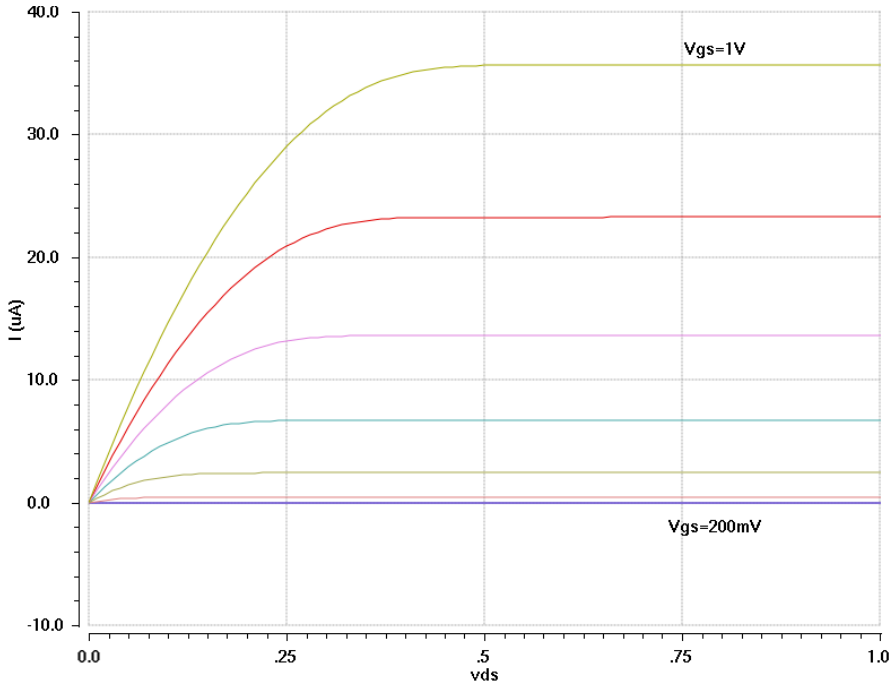


Fig. 5.2: I_{DS}-V_{DS}, Conventional NMOS (W/L=10µm/10µm)

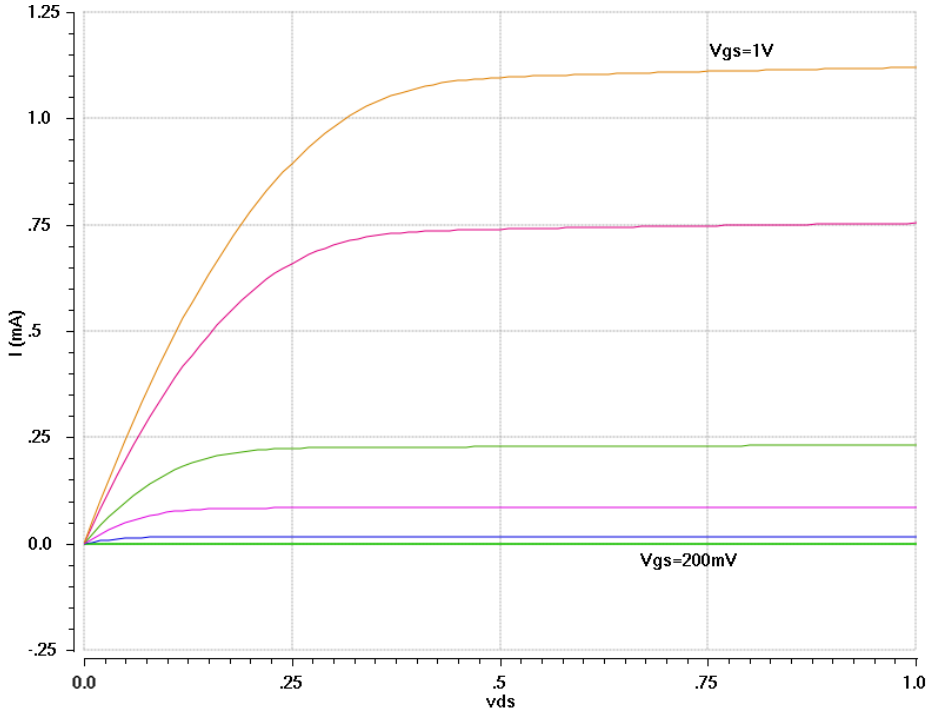


Fig. 5.3: I_{DS}-V_{DS}, Conventional NMOS (W/L=10µm/280nm)

On the other hand, the **Drain-Bulk** configuration setup is presented in Fig. 5.4 below,

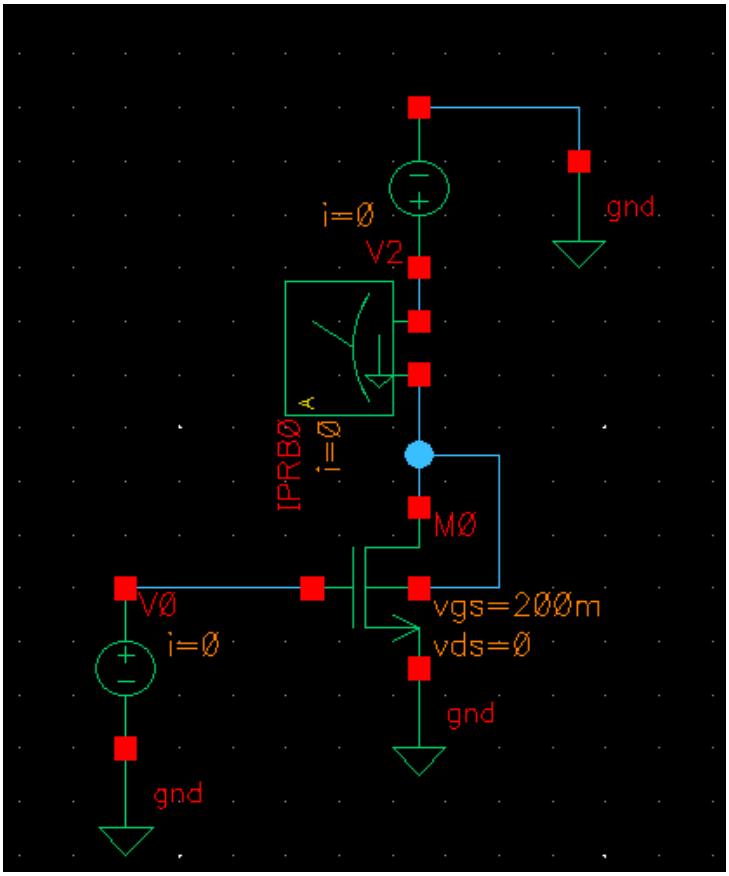


Fig. 5.4: Drain-Bulk NMOS simulation setup

The I-V characteristics of the Drain-Bulk connected NMOS device is depicted in Fig. 5.5,

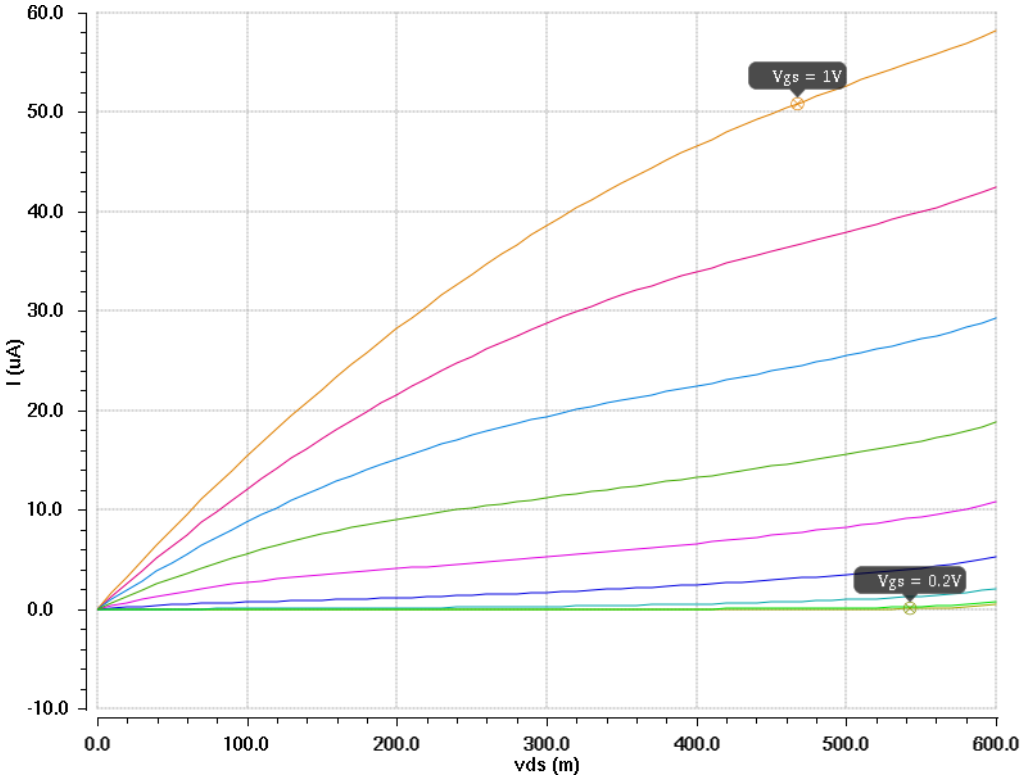


Fig. 5.5: I_{DS}-V_{DS}, Drain-Bulk connected NMOS (W/L=10µm/10µm)

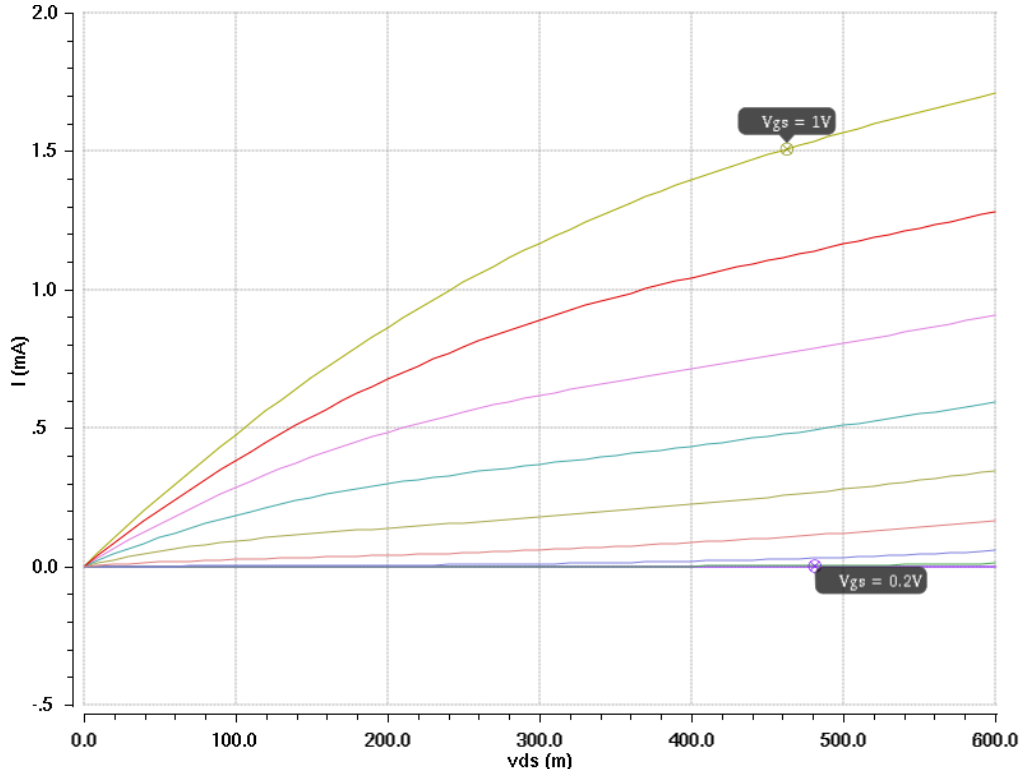


Fig. 5.6: I_{DS}-V_{DS}, Drain-Bulk connected NMOS (W/L=10µm/280nm)

5.4 Grounded-Gate NMOS Current Mirror Simulation

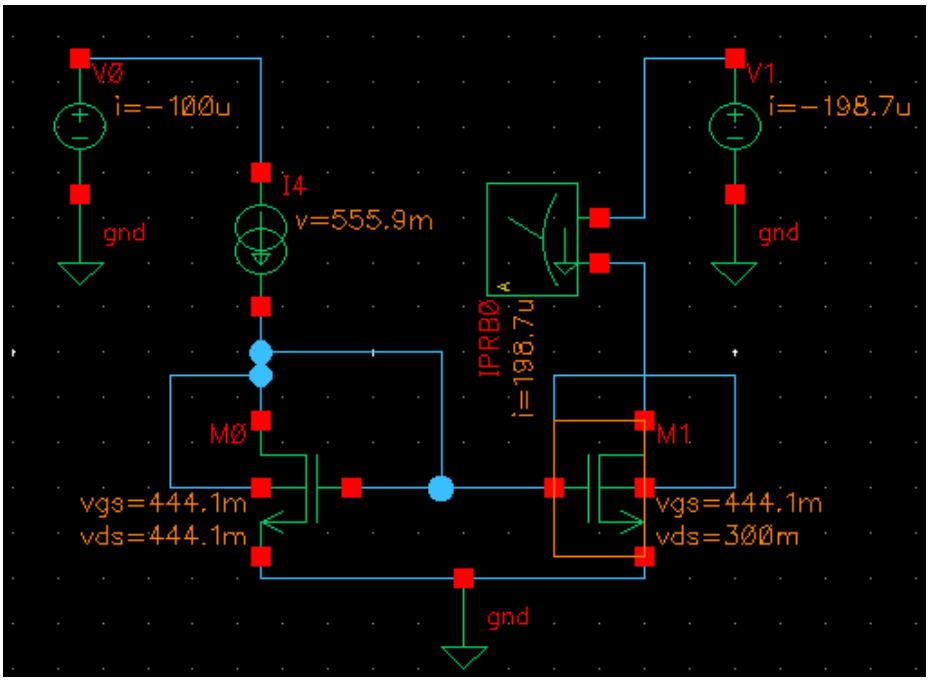


Fig. 5.7: Grounded-Gate NMOS current mirror

Fig. 5.7 shows the setup that has been used in order to simulate a grounded-gate NMOS current mirror. The ratio of I_{DS1} and I_{DS0} is given by the ratio of the device dimensions as mentioned in Section 3.2.1. For this design, W_0/L=20µm/280nm and W_1/L=40µm/280nm, and therefore, the drain current of M_1 is equal to $I_{DS1}=2*I_{DS0}$. The I-V characteristics are depicted in Fig. 5.8,

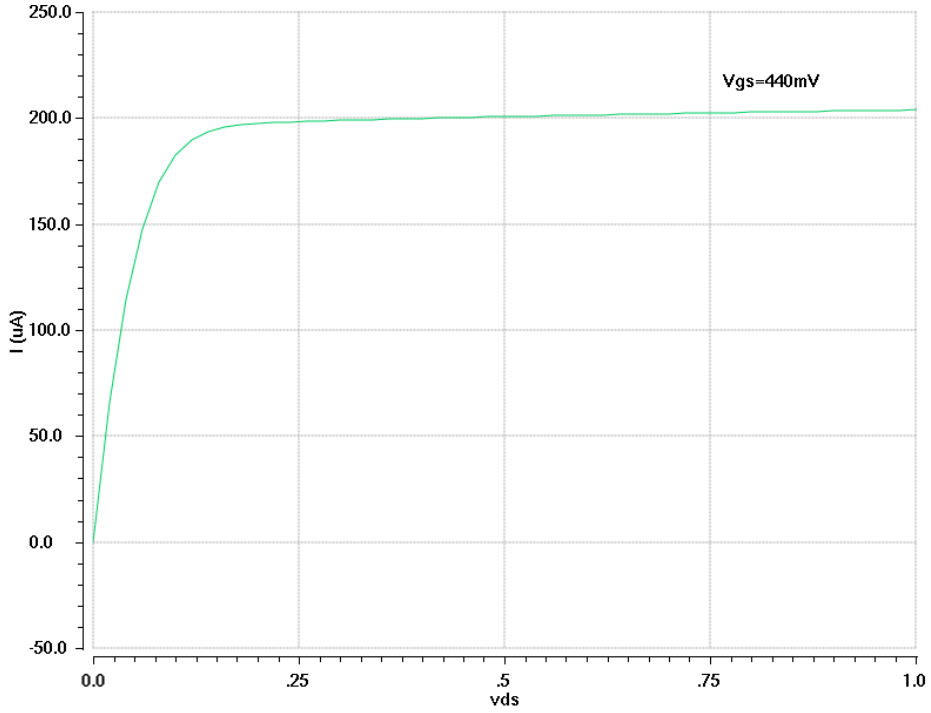


Fig. 5.8: I-V characteristics of grounded-gate NMOS current mirror

5.5 Fully Differential Gate-Input OTA Design at 1V

The basic configuration of the fully differential gate input OTA designed in this section is shown in Fig.5.9 below. This circuit consists of a pseudo-differential pair M_{1A}, M_{1B} and a simple current mirror M_{2A}, M_{2B}. The resistors R_{1A}, R_{1B} provide local common-mode feedback. The level-shifting current I_L develops a 437mV voltage drop across R_{1A}, R_{1B} to maintain V_x around 440mV so that M_{2A} and M_{2B} operate in moderate inversion. The bodies of M_{2A} and M_{2B} are connected to the gates to further reduce their threshold voltage V_T. To obtain the same result for input transistors M_{1A}, M_{1B}, the body of these devices is forward biased.

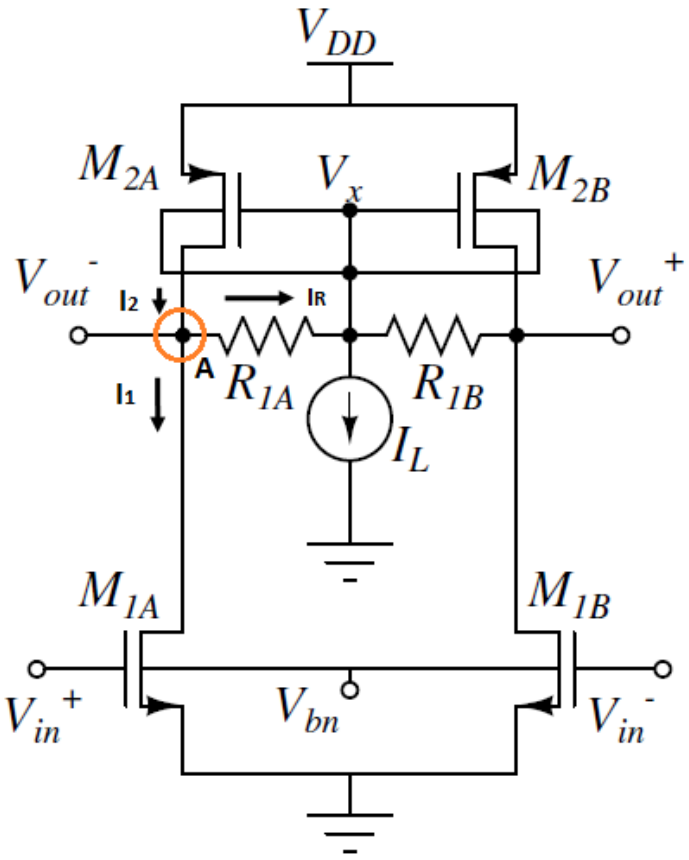


Fig. 5.9: Basic configuration of gate-input OTA

Applying the Kirchhoff's Current Law (KCL) at node A, we have:

$$I_2 = I_1 + I_R (5.1)$$

Furthermore, the total current of the circuit is generated by the supply voltage V_{DD}. Assuming that transistors M_{2A}, M_{2B} have the same dimensions, the total current is given by the Equation (5.2) below:

$$I_{DD} = I_{2A} + I_{2B} \Rightarrow I_{DD} = 2 \cdot I_{2A} (5.2)$$

The design procedure starts by selecting the drain currents and the desired values of inversion coefficients of input and output devices. For a static power dissipation of $100\mu W$ and a supply voltage of 1V, the total current is equal to $100\mu A$. Using Equation (5.2), the drain current of transistors M_{2A}, M_{2B} has a value of $50\mu A$. The level-shifting current I_L has been set equal to $1\mu A$, therefore, using Equation (5.1), input transistor M_{1A} is biased with a current:

$$I_1 = I_2 - I_R \Rightarrow I_1 = 49.5\mu A$$

The next step of the design procedure is to select the inversion coefficients of input and output devices. Input devices, such as differential pairs, must operate in weak inversion, in order to achieve higher transconductance efficiency g_m/I_D , higher DC gain, higher DC input offset voltage matching and lower input-referred thermal noise at the gates of these devices. On the other hand, output devices and current mirrors must operate in strong inversion, in order to obtain lower transconductance efficiency, higher current matching and lower thermal noise at the drain of these devices.

Based on the selected drain currents and inversion coefficients of each transistor, we set the Open-Loop Gain and Gain-Bandwidth specifications of the amplifier.

The following table summarizes and demonstrates the basic design specifications that have been set:

Specifications	**Value**
Nominal supply voltage (V)	1
Total Current (μA)	100
Power Dissipation (μW)	100
Open-Loop Gain (dB)	30
GBW (MHz)	100
C_L (pF)	1

Table 5.2: Design specifications of gate-input basic configuration

The small signal analysis of the circuit gives the expressions of the dominant pole, which is the GBW product, and the Open-Loop Gain of the circuit. The GBW is given by,

$$GBW = \frac{g_{m1}}{2\pi C_L} (5.3)$$

where g_{m1} and C_L are the gate transconductance of M_1 and C_L the output load capacitance of the amplifier respectively.

The Open-Loop Gain is given by,

$$A_{diff} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + 1/R_A} (5.4)$$

where g_{ds1} and g_{ds2} are the output conductances of transistors M_1 and M_2 respectively.

For a given value of the output capacitance and selected specification of the GBW product, the gate transconductance g_{m1} can be calculated from Equation (5.3). If C_L=1pF and GBW=100MHz, g_{m1} is equal to $g_{m1} = 628\mu S$. In order to select the inversion coefficient of input transistor M_1, we can use the g_m over I_D ratio that is given by,

$$\frac{g_m}{I_D} = \frac{1}{nU_T} \cdot \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + IC}}$$

$$\Rightarrow IC = \left(\frac{1}{nU_T \left(\frac{g_m}{I_D} \right) - 0.5} \right)^2 - 0.25(5.5)$$

Using the above equation, the selected IC of transistor M_1 is equal to $IC_1 = 3.8$. The relation between the inversion coefficient and effective input voltage is given by the Equation (4.4). The input gate voltage needed to bias the device in $IC_1 = 3.8$, is equal to V_{GS}=602.8mV.

Finally, using the Equation (4.1) that gives the inversion coefficient, the width of transistors M_1 and M_2 are equal to,

$$W_1 = \frac{L_1 I_{D1}}{I_{Spec0N} \cdot IC_1} \text{ and } W_2 = \frac{L_2 I_{D2}}{I_{Spec0P} \cdot IC_2} \text{ respectively,}$$

where I_{D1}, I_{D2} (I_{D1}= I_1, I_{D2}=I_2 from the schematic of Fig. 5.9) are the selected drain currents, L_1, L_2 the channel lengths and IC_1, IC_2 the selected inversion coefficients of M_1 and M_2 respectively. I_{Spec0N} and I_{Spec0P} are the technology currents for NMOS and PMOS transistors respectively. It must be noted that in this work, we assume the same channel lengths for all devices. For channel length equal to $L = 280nm$ and $IC_2 = 3$, the channel widths of transistors of M_1 and M_2 are equal to $W_1 = 5.6\mu m$ and $W_2 = 41.1\mu m$. Tables 5.3, 5.4 below summarize the DC design specifications and the DC analysis results,

Design Parameters	Specification	Simulation Results
$I_{DD}(\mu A)$	100	100.3
$I_{D1}(\mu A)$	49.5	49.6
$I_{D2}(\mu A)$	50	49.6
$I_R(nA)$	500	486.5
IC_1	3.8	3.9
IC_2	3	2.3
$g_{m1}(\mu S)$	628	606

Table 5.3: DC currents specifications of gate-input basic configuration

According to the above analysis, Table (5.4) below shows the components sizes and values for the simple configuration of the gate-input operational transconductance amplifier,

Transistors	$W(\mu m)$	$L(\mu m)$
M_{1A}, M_{1B}	5.6	$280nm$
M_{2A}, M_{2B}	41.1	$280nm$
Resistors and Capacitors		
R_{1A}, R_{1B}	$100k\Omega$	
C_L	$1pF$	

Table 5.4: Component sizes and values for the gate-input operational transconductance amplifier

5.5.1 DC Transfer Characteristics

In order to simulate the DC transfer characteristics of the amplifier, we use the following setup, where the negative input is tied to the ground whereas the positive input is tied to a voltage source that sweeps from 0V to 1V.

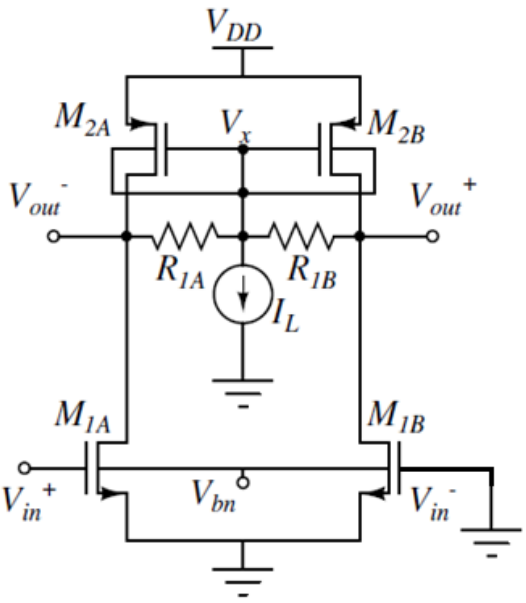


Fig. 5.10: DC transfer characteristics simulation setup

The following figure shows the transfer characteristics of the sub-circuit that consists of transistors M_{1A} and M_{2A}. This sub-circuit defines a simple common source amplification stage where M_{2A} acts like an active load of the input device.

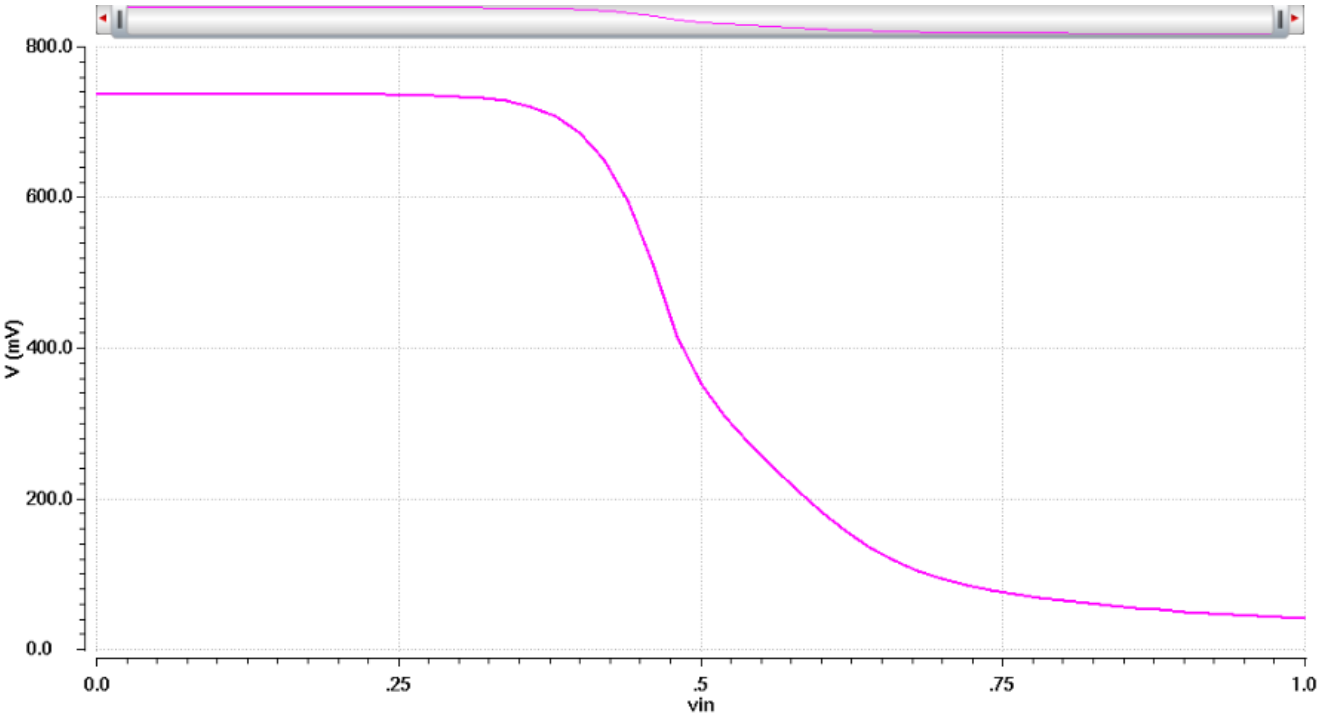


Fig. 5.11: DC transfer characteristics (Negative output-Positive input)

On the other hand, Fig.5.12 below depicts the DC transfer characteristics of the whole circuit:

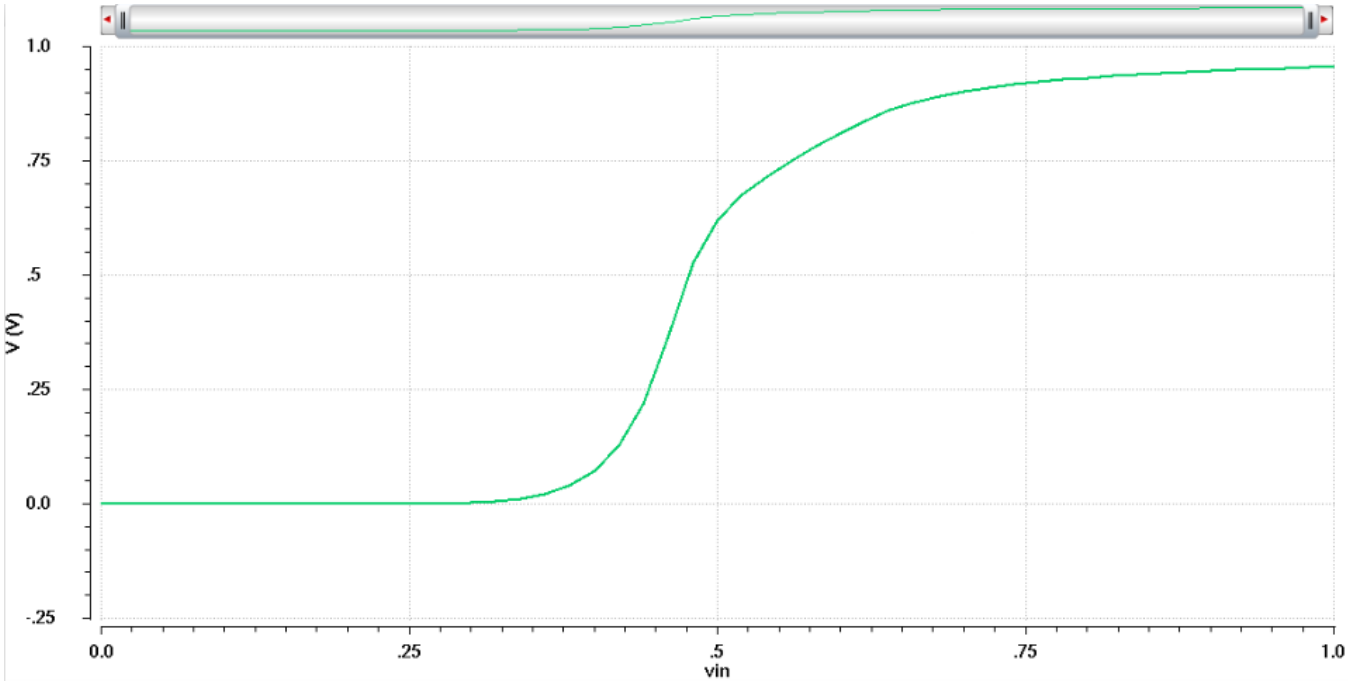


Fig. 5.12: DC transfer characteristics (Differential output-Positive input)

5.5.2 Frequency Response Figures

As mentioned before, the small signal analysis of the gate-input amplifier gives the differential gain and GBW product,

$$A_{diff} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + 1/R_A}$$

$$GBW = \frac{g_{m1}}{2\pi C_L}$$

Fig. 5.13 shows the frequency response of the circuit,

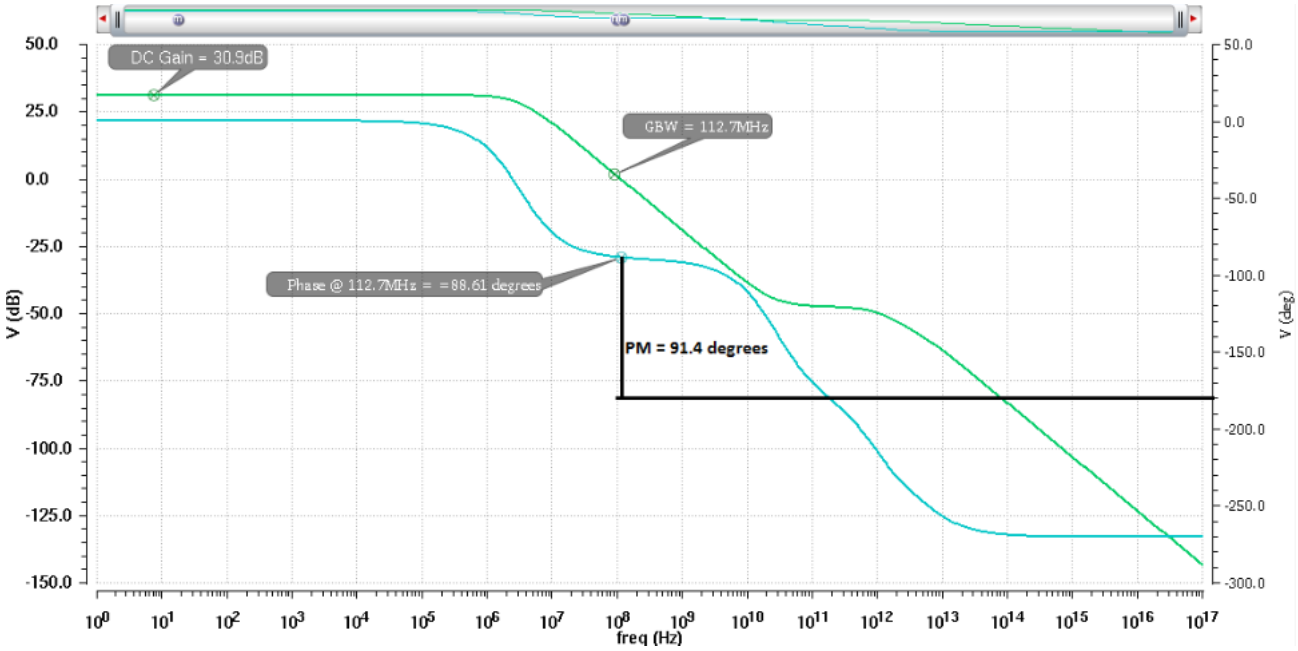


Fig. 5.13: AC response of gate-input operational transconductance amplifier

As shown in Fig. 5.13 above, the operational amplifier is a dc amplifier which has a low-pass response. Table 5.5 summarizes the AC performance of the circuit,

Parameter	Value
$DC\ Gain(dB)$	30.9
$GBW(MHz)$	112.7
Phase Margin (Degrees)	91.4

Table 5.5: Gate-input basic configuration performance

The DC gain of the amplifier is given by the Equation (5.4). The DC analysis that performed gave the values of input and output transconductances g_{m1}, g_{ds1}, g_{ds2}. Using these values, it is easy to estimate the DC gain of the circuit which is equal to:

$$A_{diff} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + 1/R_A} = \frac{606\mu S}{1.9\mu S + 8.7\mu S + 10\mu S} \cong 29.4V/V$$

The differential gain of the amplifier, expressed in dB, is equal to:

$$A_{diff\,(dB)} = 20\log(29.4) = 29.4dB$$

This value is very close to the initial design specification of the differential gain as seen in Table 5.2 above.

Furthermore, the simulated GBW product of the circuit is equal to:

$$GBW = \frac{g_{m1}}{2\pi C_L} = \frac{606\mu S}{2\pi \cdot 10^{-12}} \cong 96.5MHz$$

This value is very close both the initial specification and the simulation of the AC analysis that is shown in Fig. 5.13 above.

Finally, the Phase Margin of the amplifier is given by the expression:

$$PM = -180 - (phase@GBW) \quad (5.6)$$

Equation (5.6) denotes that the Phase Margin of the simple gate-input amplifier is the difference between the phase, measured in degrees, of an amplifier's output signal (relative to its input) and 180°, as a function of frequency. For this design, PM=91.4^o. As shown in Fig. 5.13, the phase of the circuit starts from 0^o, which means that the amplifier is non-inverting.

5.5.3 Transient Analysis Figures

For transient simulation, two voltage sources were applied to the inputs of the circuit having a phase difference of 180^o. Fig. 5.14 below shows the input characteristics,

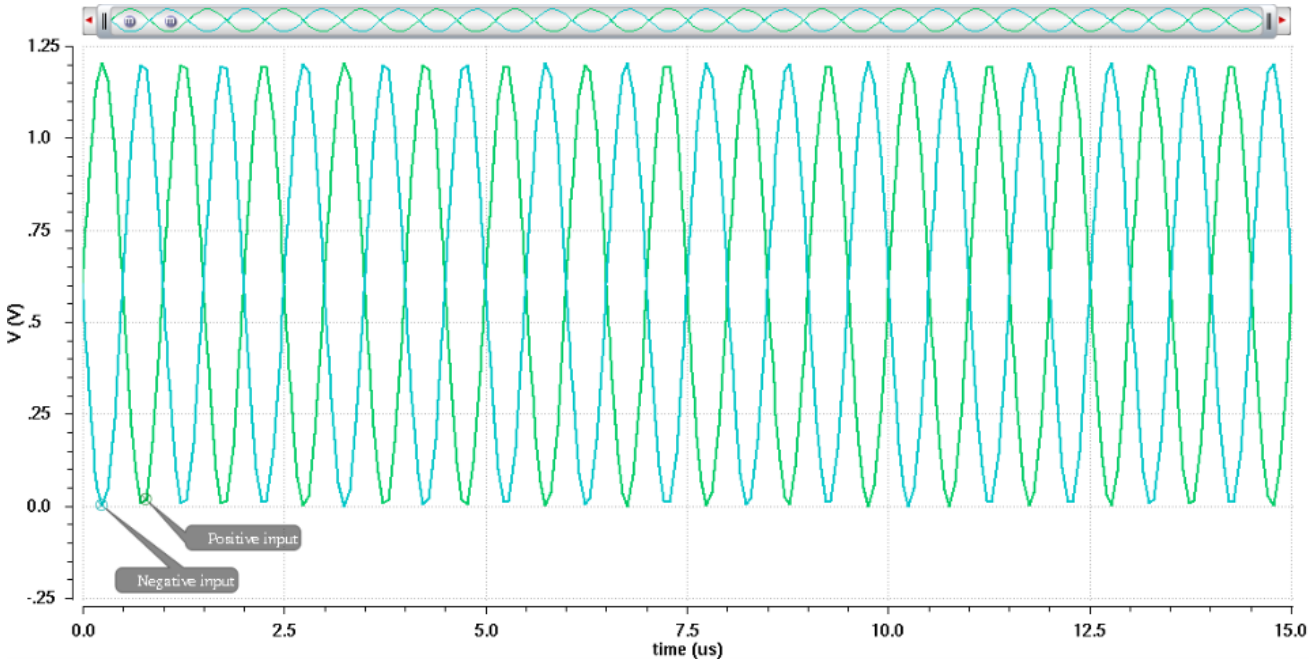


Fig. 5.14: Input signals in time domain

The following figure shows the transient response of the amplifier,

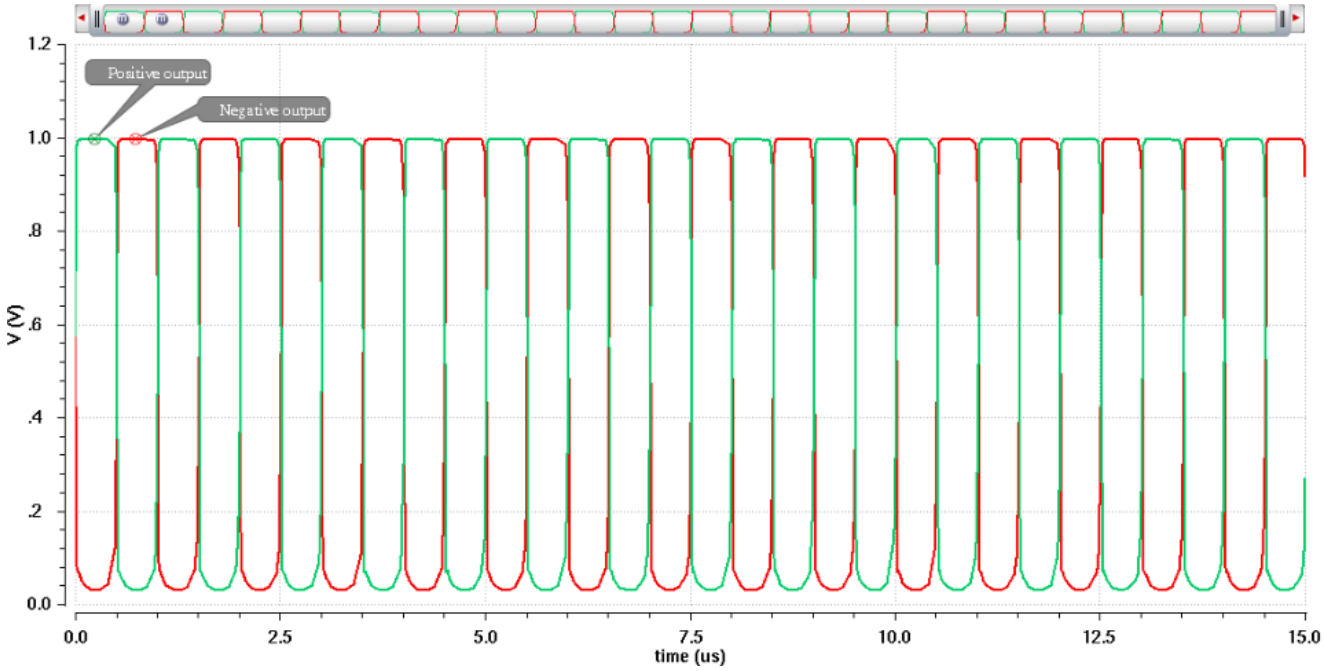


Fig. 5.15: Output signals in time domain

Fig. 5.15 shows that the output of the amplifier is differential, but on the other hand the clipping that can be observed is caused by the fact that as the input CM level, $V_{in,CM}$, changes, so do the bias currents of M_{1A} and M_{1B} , thus varying both the transconductance of the devices and the output CM level. The variation of the transconductance in turn leads to a change in the small-signal gain while the departure

of the output CM level from its ideal value lowers the maximum allowable output swings. For example, as shown in Fig. 3.3 (b), if the input CM level is excessively low, the minimum values of V_{in1} and V_{in2} may in fact turn off M_{1A} and M_{1B}, leading to severe clipping at the output. Thus, it is important that the bias currents of the devices have minimal dependence on the input CM level. A solution to this problem is to add common-mode feedback cancelation paths as reported in [50] and also mentioned in this work.

Additionally, in order to simulate the Slew Rate of the amplifier, we use the following setup:

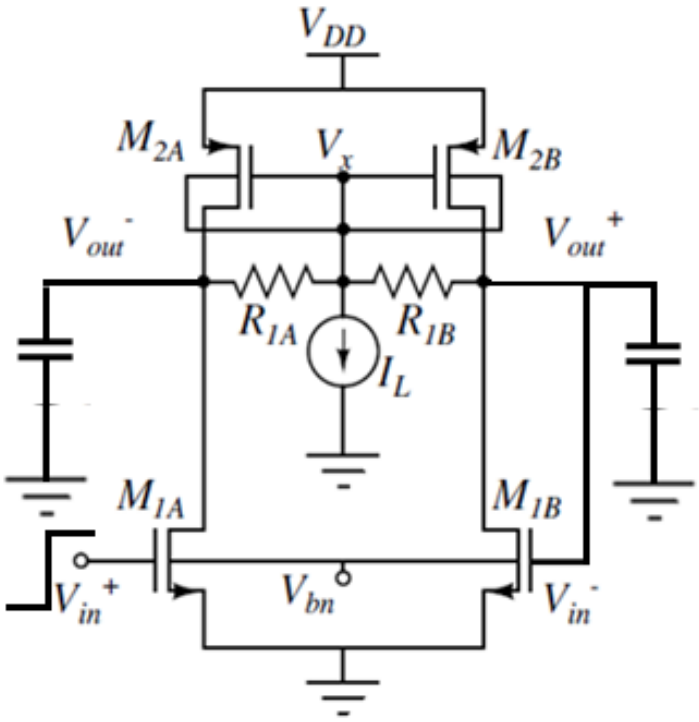


Fig. 5.16: Slew Rate simulation setup

The negative input is tied to the positive output, generating a feedback loop. The positive input is biased with a pulse voltage source that has minimum and maximum values of 0V and 2V respectively, a period equal to 10nsec and a delay time of 10nsec. The following figures depict the input and output characteristics,

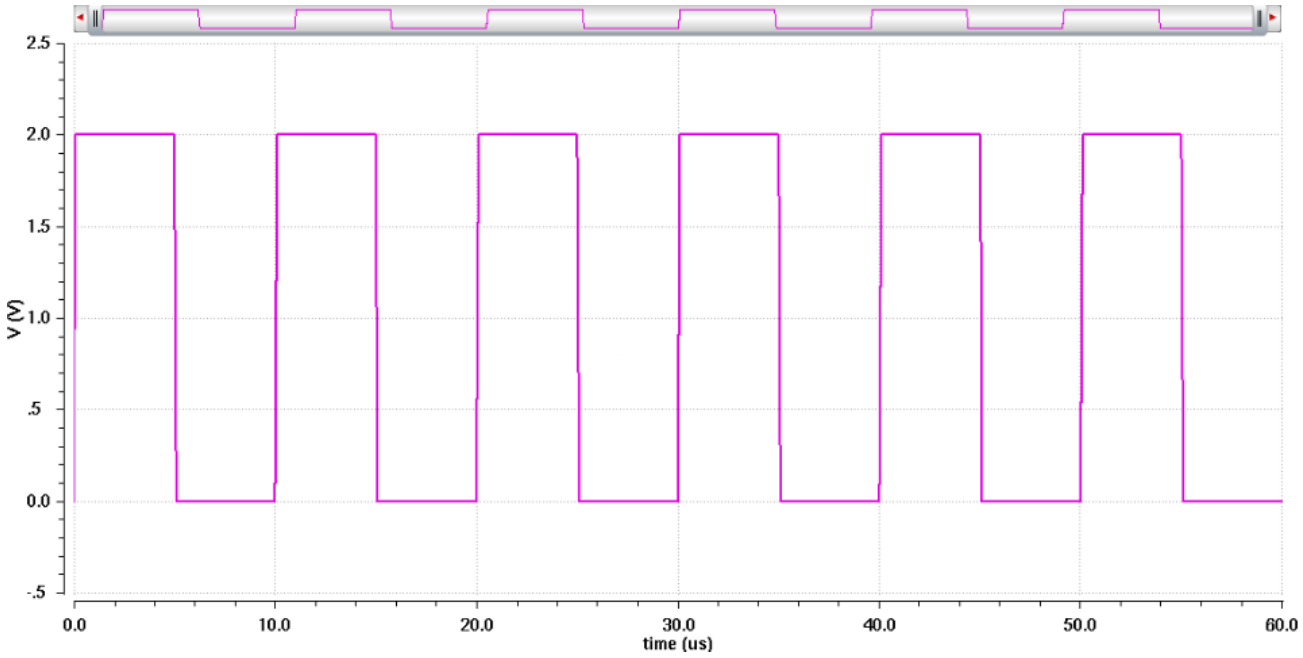


Fig. 5.17: Input signal for Slew Rate simulation

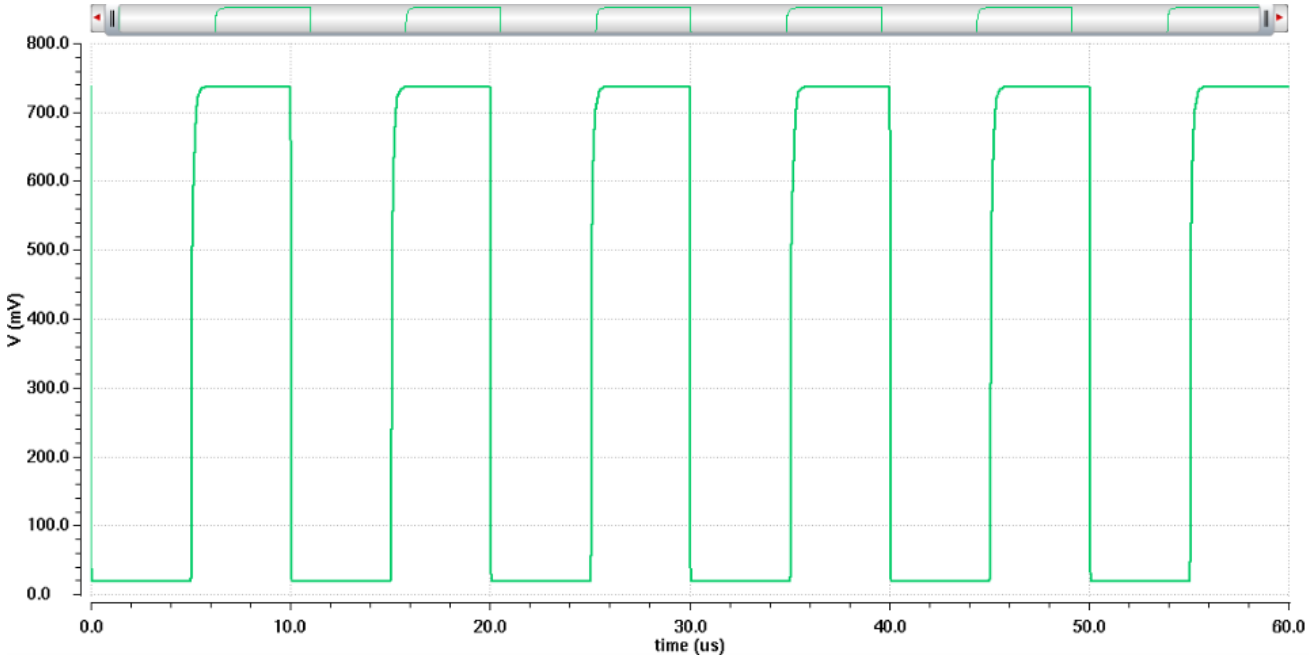


Fig. 5.18: Output signal for simulating Slew Rate

The Slew Rate is defined as the maximum rate of change of the output voltage. Slew rate is usually expressed in units of V/µsec.

$$SR = \left| \frac{dVout}{dt} \right|_{\max}$$

In order to estimate the Slew Rate of the amplifier, we use the **Calculator Tool** of Cadence. First, we apply the *Deriv* function to the output of the circuit and then we find the maximum value of this result. The simulated Slew Rate is equal to $SR = 19V/\mu\text{sec}$.

5.6 One-stage gate-input OTA design

5.6.1. DC Analysis

The following figure shows the schematic of one stage of the gate-input OTA, where seven transistors have been added.

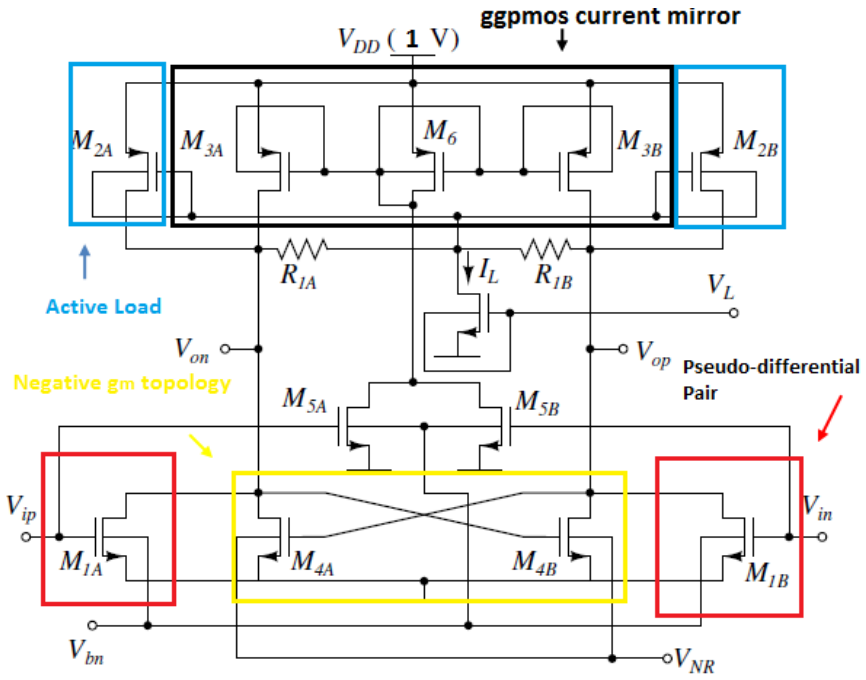


Fig. 5.19: Schematic of one stage of the gate-input OTA

As mentioned before, in the basic differential amplifier, as shown in Fig. 5.19, the input differential pair, M_{1A} and M_{1B} and the active loads M_{2A} and M_{2B} amplify the differential input voltage. The resistors R1A, R1B, provide common-mode feedback through the active load. A level-shifting current I_L develops a 437mV drop across R_{1A} and R_{1B} to maintain V_X around 430mV so that M_{2A} and M_{2B} operate in moderate inversion or in lower. The voltage V_X is the voltage that biases the gate terminals of transistors M_{2A}, M_{2B}. The bodies of M_{2A} and M_{2B} are connected to the gates to further reduce their threshold voltage. In addition, to lower the V_T, the body of the input devices M_{1A} and M_{1B} is forward biased. It must be pointed out that the level-shifting current I_L can be replaced by a grounded-gate NMOS transistor as depicted in Fig. 1.47.

The ratio of the transconductance of M_{1A} and M_{1B} to the total transconductance of M_{2A} and M_{2B} sets the common-mode gain. In the process used, the PMOS transconductance is not sufficiently large compared to the NMOS transconductance to obtain a low common-mode gain. Therefore a common-mode feed-forward cancellation path is added, as shown in Fig. 5.19, through M_{5A} M_{5B} , M_6 and M_{3A},

M_{3A}. In M_{3A}, M_{3B} and M_6, the gate and the body are connected to each other to obtain a forward bias across the body-source junctions; this pushes these devices towards moderate and weak inversion. The differential gain is further enhanced with the cross-coupled M_{4A}, M_{4B}, which acts as a negative conductance and decreases the output conductance. As an added benefit, the common-mode gain is also further reduced. Table 5.6 gives the design specifications of the one stage of the gate-input OTA,

Specifications	Value
Nominal supply voltage (V)	1
Total Current (μA)	100
Power Dissipation (μW)	100
Open-Loop Gain (dB)	≥ 20
GBW (MHz)	13
C_L (pF)	10

Table 5.6: Design specifications of one stage gate-input OTA

Applying the Kirchhoff's Current Law (KCL) at node B (see Fig. 5.20 below), we have:

$$I_{out} + I_{R1A} = I_{2A} + I_{3A} (5.7)$$

Furthermore, the total current of the circuit is generated by the supply voltage V_{DD}. This total current is given by the Equation (5.8) below:

$$I_{DD} = I_{2A} + I_{2B} + I_{3A} + I_{3B} + I_6$$
$$\Rightarrow I_{DD} = 2 \cdot I_{2A} + 2 \cdot I_{3A} + I_6 (5.8)$$

It must be noticed that transistors M_3 and M_6 define a grounded-gate PMOS current mirror. We select that M_3 has a width equal to $W_3 = 2W_6$ (keeping the length the same as M_6), so that the drain current of M_3 is equal to $I_3 = 2I_6$. As a result, Equation (5.8) gives,

$$I_{2A} = \frac{I_{DD} - 5 \cdot I_6}{2} (5.9)$$

In addition, we have:

$$I_{out} = I_{1A} + I_{4A} (5.10)$$

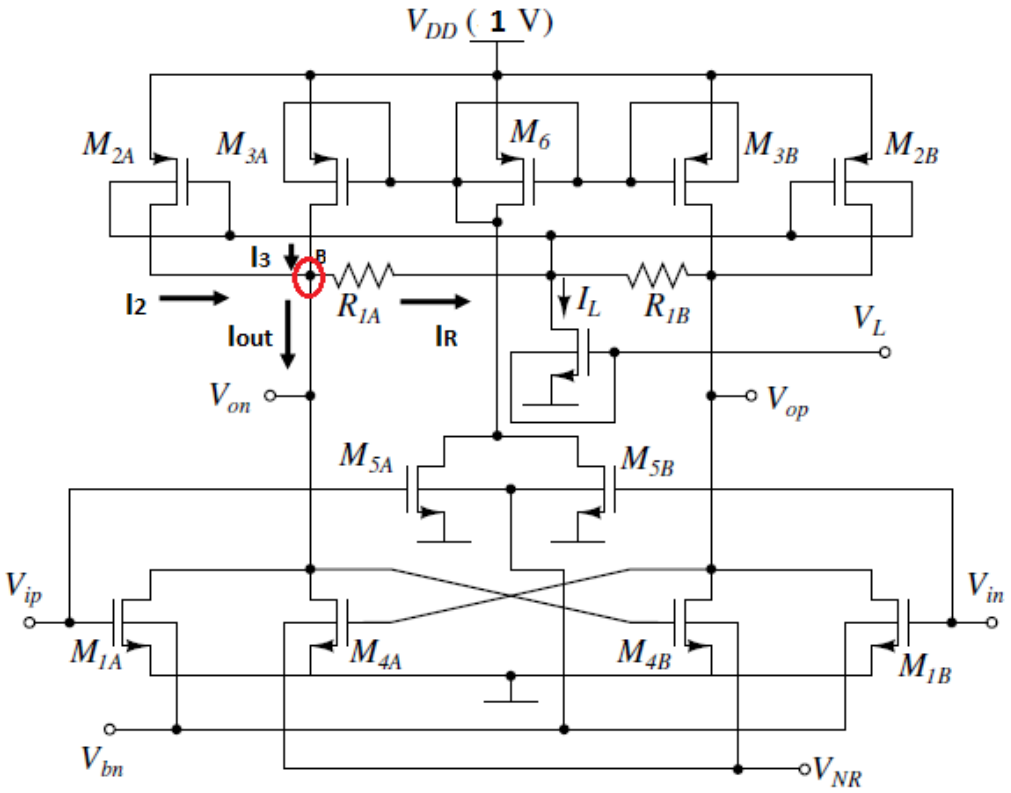


Fig. 5.20: DC Analysis of Gate-input OTA

Based on the known currents I_{2A}, I_{1RA} and I_{3A}, it is easy for us to compute the currents I_{out} and I_{4A} from Equations (5.7) and (5.10) respectively after selecting the drain current I_{1A} of transistor M_{1A} and I_{1RA}. Table 5.7 below summarizes the specified DC currents,

Branch Currents	Value
$I_{DD}(\mu A)$	**100**
$I_{1A}(\mu A)$	**50**
$I_{2A}(\mu A)$	**50**
$I_{3A}(\mu A)$	**10**
$I_{4A}(\mu A)$	**9.5**
$I_{5A}(\mu A)$	**2.5**
$I_{6A}(\mu A)$	**5**
$I_7(\mu A)$	**1**
$I_{R1A}(\mu A)$	**0.5**
$I_{out}(\mu A)$	**59.5**

Table 5.7: DC currents specifications of one stage gate-input OTA

As reported in [50], if the W/L ratios of M_1, M_3, M_5, M_6 are such that $M_1/M_5 = M_3/M_6$, then the common-mode gain will be zero. In this design, it is assumed to have M1/M5 = 0.25*(M3/M6). Furthermore, the ratio of the grounded-gate PMOS current mirror has been selected to be equal to $M_3/M_6 = 2$, so that the ratio $M_1/M_5 = 8$. Based on the aforementioned assumption and by selecting the drain currents (as a function of the power dissipation specification), we can size the MOS devices of the amplifier properly.

The next step of the design procedure is to select the inversion coefficients of the devices and based on the selected currents depicted in Table 5.8, we can size all the transistors using the equation that gives the IC in saturation region.

Table 5.8 below shows the selected inversion coefficients,

Transistor	**IC**
M_1	1.86
M_2	1.5
M_3	5
M_4	2.93
M_5	1.86
M_6	5

Table 5.8: IC selection for the one stage gate-input OTA

In order to specify the IC of transistor M_1, we use the Equation (4.4) that relates the effective gate voltage with the inversion coefficient. In addition, the IC of transistor M_4 is specified using the known output voltage and Equation (4.4) as well.

Table 5.9 depicts the component sizes and values for the gate-input OTA,

Transistors	$W(\mu m)$	$L(\mu m)$
M_{1A}, M_{1B}	11.5	0.28
M_{2A}, M_{2B}	41.1	0.28
M_{3A}, M_{3A}	9.8	0.28
M_{4A}, M_{4A}	1.5	0.28
M_{5A}, M_{5A}	0.57	0.28
M_6	4.9	0.28
M_7	1	0.28
Resistors and Capacitors		
R_{1A}, R_{1B}	$100k\Omega$	
C_L*	$10pF$	

With C_L, we denote the load capacitance of the first stage that is seen at the input of the second stage as described below.

Table 5.9: Component sizes and values for the one stage gate-input OTA

For a specified GBW product of 13MHz and a load capacitance of 10pF, the gate transconductance has been estimated at g_{m1} = 816μS. Based on Equation (5.5), the inversion coefficient is equal to IC_1 = 1.86. The effective gate voltage is equal to V_{EFF} = 67.1mV and for a threshold voltage of 490mV, the input gate-source voltage of transistor M_1 equals to V_{GS1} = 554mV.

The DC simulation results are shown in Table 5.10 below,

Transistor/Branch	Current (μA)	IC	g_m (μS)	g_{ds} (μS)
M_1	49.6	1.87	792	1.78
M_2	50.4	1.3	-	9.75
M_3	9.72	4	132.3	1.57
M_4	10.02	2.74	117	0.372
M_5	2.43	1.87	-	-
M_6	4.86	4.2	-	-
Output Branch	59.62	-	-	-
Total Level-Shifting Current Source I_L	1.05	-	-	-

Table 5.10: DC Simulation Results of one stage gate-input OTA

In order to estimate the overall DC gain of the amplifier, we use the g_m, g_{ds} values from Table 5.10 and Equation (3.1). The DC gain (expressed in dB) has been simulated and estimated at $A_{diff\,(dB)} = 19.5dB$.

5.6.2 Frequency Response Figures

The following figures (Fig. 5.21, Fig. 5.22) shows the frequency response of the gate-input OTA for Gain and Phase respectively,

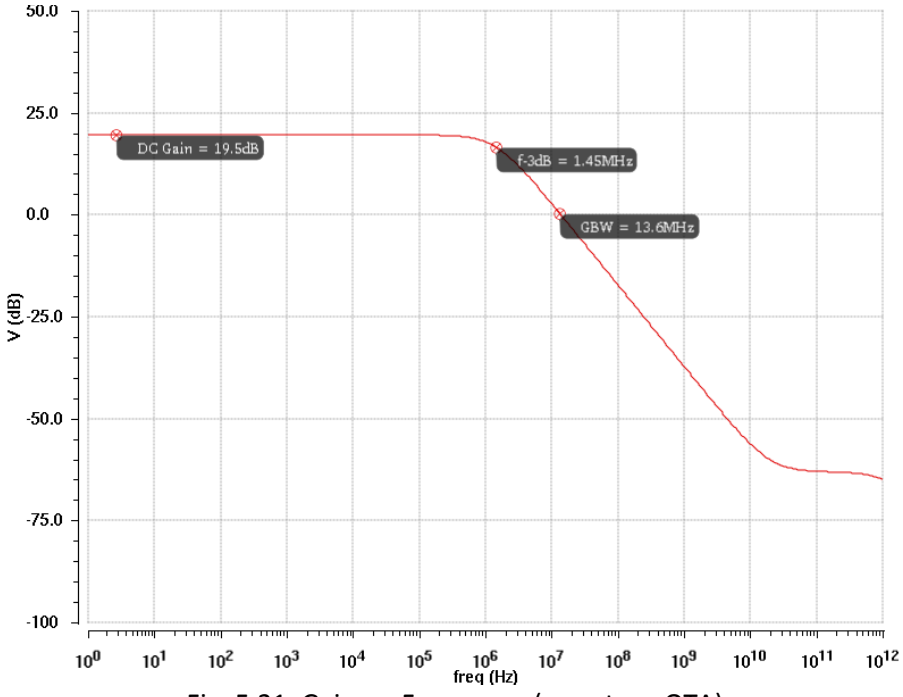


Fig. 5.21: Gain vs. Frequency (one stage OTA)

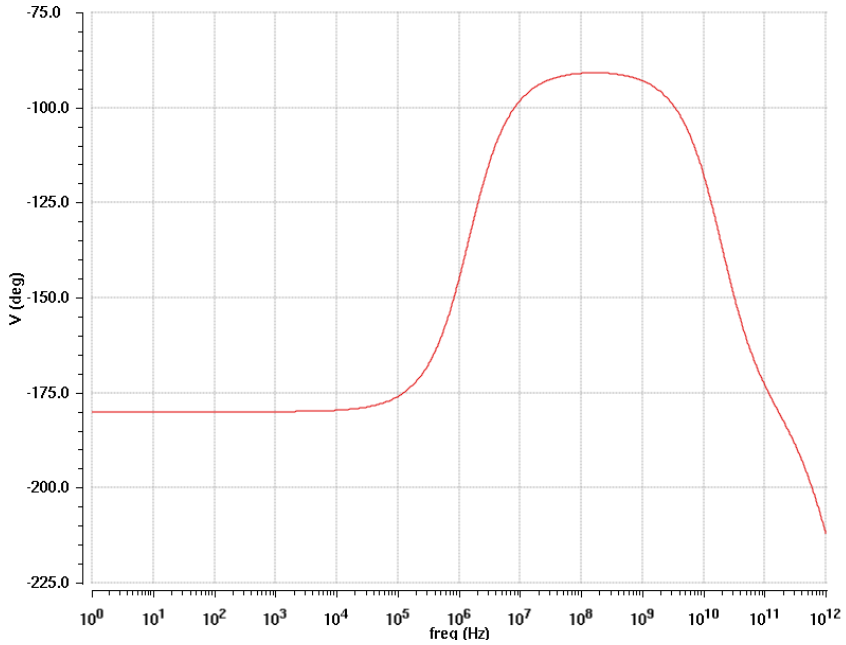


Fig. 5.22: Phase vs. Frequency (one stage OTA)

5.6.3 Transient Analysis Figures

The following figures depict the analysis of the OTA in the time domain. Fig. 5.23 shows the output of the circuit, where the inputs are biased with a sine wave. On the other hand, Fig. 5.24 shows the output that used in order to measure the Slew Rate of the amplifier based on the simulation setup of Fig. 5.16.

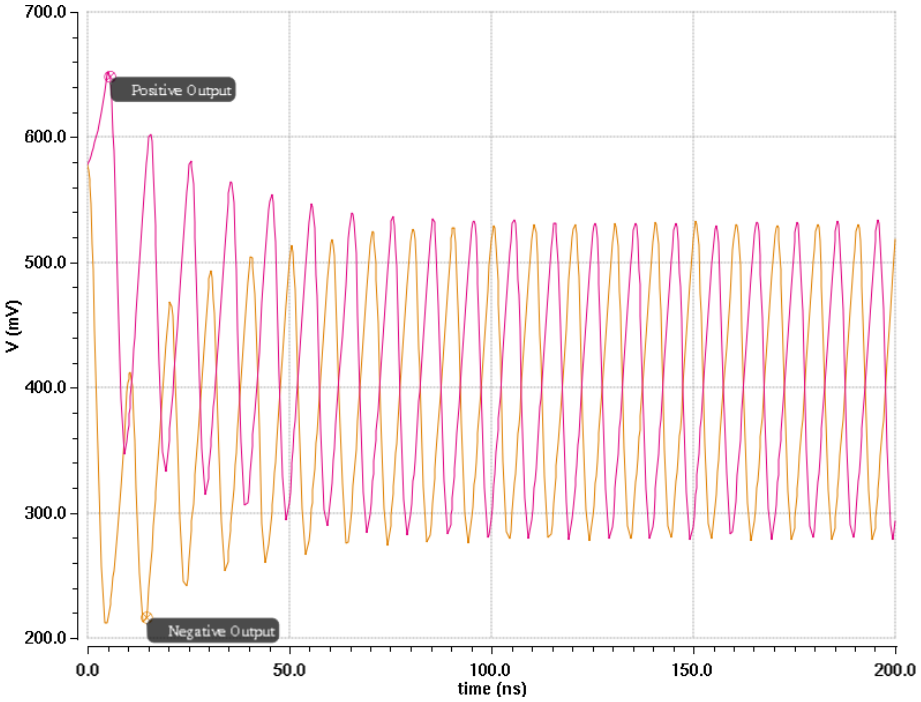


Fig. 5.23: Output signals in time domain (one stage OTA)

As we can see, there is no clipping of the output signals, which means that the amplifier gives a very low common-mode gain.

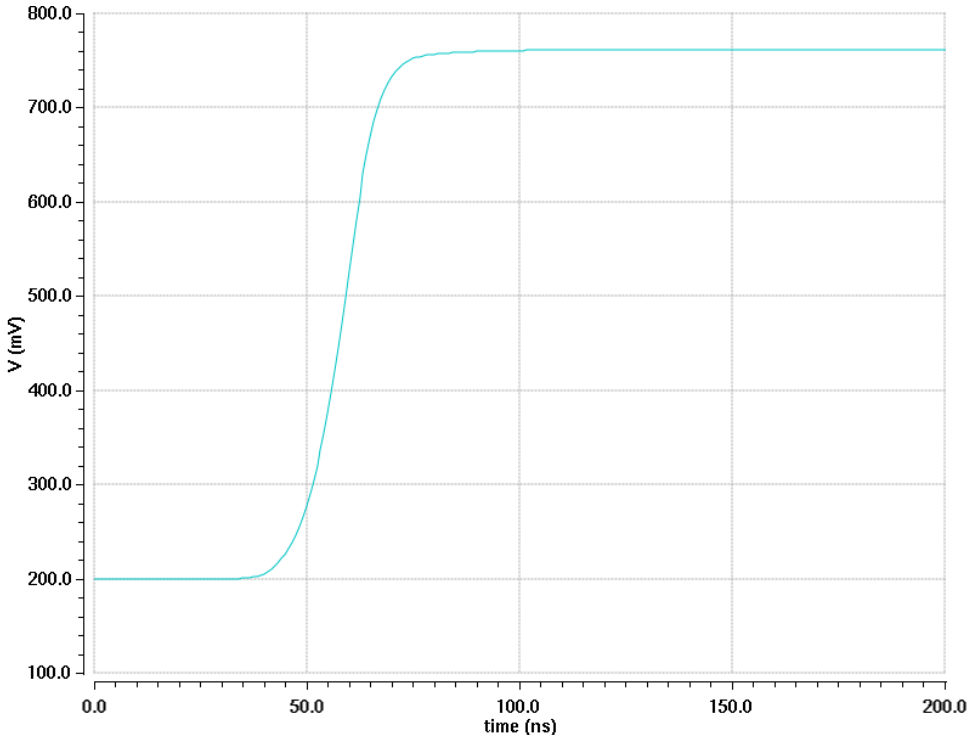


Fig. 5.24: Transient Output for simulating the Slew Rate

The following table summarizes the performance of the one-stage gate-input OTA,

Parameter	Value
Supply Voltage (V)	1
Power Dissipation (µW)	99.8
DC Gain (dB)	19.5
GBW (MHz)	13.6
f_{-3dB} (MHz)	1.45
CMRR (dB)	37.8
Slew Rate (V/µsec)	33.1
Load Capacitance (pF)	10
Phase Margin (Degrees)	91.4

Table 5.11: One-stage gate-input OTA performance

5.7 Two-stage gate-input OTA design

To obtain a DC gain greater than 50dB, two gain stages are cascaded to form a two-stage operational transconductance amplifier. The complete schematic of the two-stage fully differential operational transconductance amplifier is shown in Fig. 5.25 below,

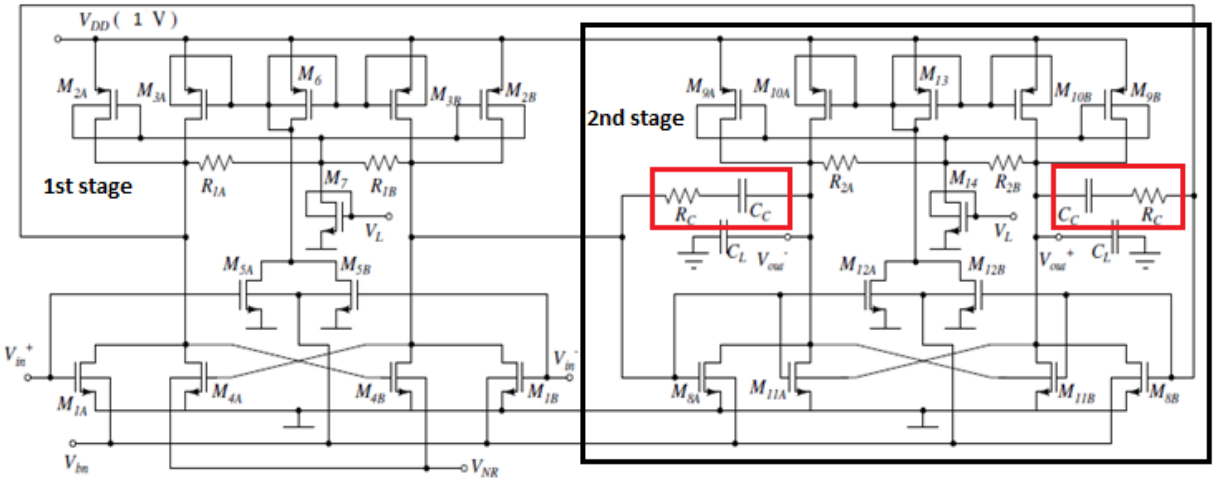


Fig. 5.25: Two-stage, fully differential, gate-input OTA, with Miller compensation.

The input of the second stage is biased by the output of the first stage, as seen in Fig. 5.25. The OTA is stabilized through the Miller capacitors C_C across the second stage. The gain-bandwidth product is approximately $g_{m1}/(2\pi C_C)$ and the second pole frequency of the amplifier is approximately at $g_{m8}/(2\pi C_L)$, where CL is the single-ended load capacitance. The series resistor RC moves the zero introduced by CC from the right half plane to the left half plane.

Table 5.12 shows the design specifications of the two-stage gate-input OTA,

Specifications	Value
Nominal supply voltage (V)	1
Total Current (µA)	200
Power Dissipation (µW)	200
Open-Loop Gain (dB)	≥ 60
GBW (MHz)	13
C_L (pF)	10

Table 5.12: Design specifications of two stage gate-input OTA

5.7.1 DC Analysis

The DC analysis of the complete gate-input OTA is based on the total current that generated by the supply voltage. Equation (5.11) gives the total current of the first stage and including the devices of the second stage, we have:

$$I_{DD} = I_{2A} + I_{2B} + I_{3A} + I_{3B} + I_6 + I_{9A} + I_{9B} + I_{10A} + I_{10B} + I_{13} (5.11)$$

Furthermore,

$$I_{out2} + I_{R2A} = I_{9A} + I_{10A} (5.12)$$

and

$$I_{out2} = I_{8A} + I_{11A} (5.13)$$

where I_{out2} is the current that flows through the output branch of the second stage and I_{R2A} is the current that flows through the resistor R_{2A}. Using the Equation (4.4), it Is easy for us to estimate the IC of input devices M_8, based on the simulated output of the first stage V_{out1}, which is actually the gate-source voltage that biases the input of the second stage.

The drain current I_8 of M_8 is selected to have the half value of I_1, whereas the drain currents of M_{10}, M_{11}, M_{12} and M_{13} have the same value of M_3, M_4, M_5 and M_6 respectively. The procedure of current selection is similar to this that has been followed in designing the first stage. Table 5.13 and Table 5.14 summarize the selected drain currents and inversion coefficients respectively,

Branch Currents	Value
$I_{DD}(\mu A)$	**200**
$I_{8A}(\mu A)$	**25**
$I_{9A}(\mu A)$	**25**
$I_{10A}(\mu A)$	**10**
$I_{11A}(\mu A)$	**9.5**
$I_{12A}(\mu A)$	**2.5**
$I_{13A}(\mu A)$	**5**
$I_{R2A}(\mu A)$	**0.5**
$I_{out2}(\mu A)$	**34.5**

Table 5.13: DC current specifications of two stage gate-input OTA

Transistor	IC
M_8	4.5
M_9	1.5
M_{10}	5
M_{11}	7.93
M_{12}	4.5
M_{13}	5

Table 5.14: IC selection for two stage gate-input OTA

Following the design procedure that described above, Table 5.15 shows the component sizes for the two-stage gate-input operational transconductance amplifier of Fig. 5.25,

Transistors (Second Stage)	$W(\mu m)$	$L(\mu m)$
M_{8A}, M_{8B}	2.3	0.28
M_{9A}, M_{9B}	2.5	0.28
M_{10A}, M_{10A}	4.93	0.28
M_{11A}, M_{11A}	0.413	0.28
M_{12A}, M_{12A}	0.276	0.28
M_{13}	2.46	0.28
M_{14}	1	0.28
Resistors and Capacitors		
R_{2A}, R_{2B}	$100k\Omega$	
C_L	$10pF$	
R_C	$5k\Omega$	
C_C	$10pF$	

Table 5.15: Component sizes and values for the two stage gate-input OTA

The DC simulation results are shown in Table 5.16 below,

Transistor/Branch	Current (μA)	IC	g_m (μS)	g_{ds} (μS)
M_8	22.54	4.4	263.6	1.1
M_9	21.4	1.6	118.7	2.8
M_{10}	10.62	4.1	110.3	1.6
M_{11}	9.35	9.9	74.6	0.474
M_{12}	2.66	4.4	31	0.111
M_{13}	5.31	4.2	54.5	0.831
Output Branch	31.89	-	-	-
Total Level-Shifting Current Source I_L	1.05	-	-	-

Table 5.16: DC Simulation Results of two stage gate-input OTA

The following figure depicts the DC transfer characteristics of the two-stage gate-input OTA,

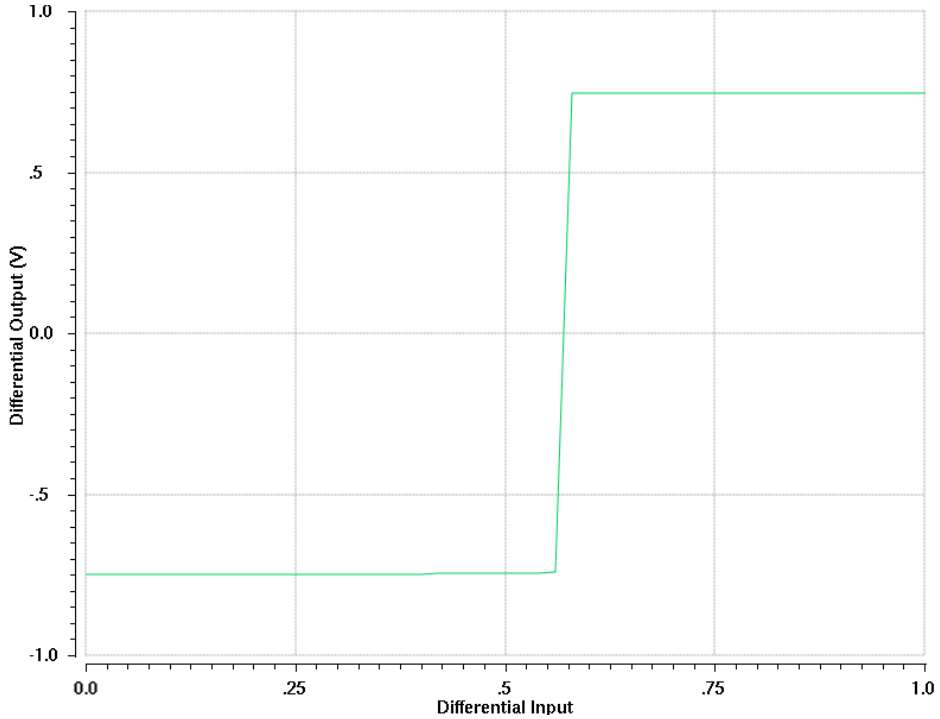


Fig. 5.26: DC input-output transfer characteristics of two stage OTA

5.7.2 Frequency Response Figures

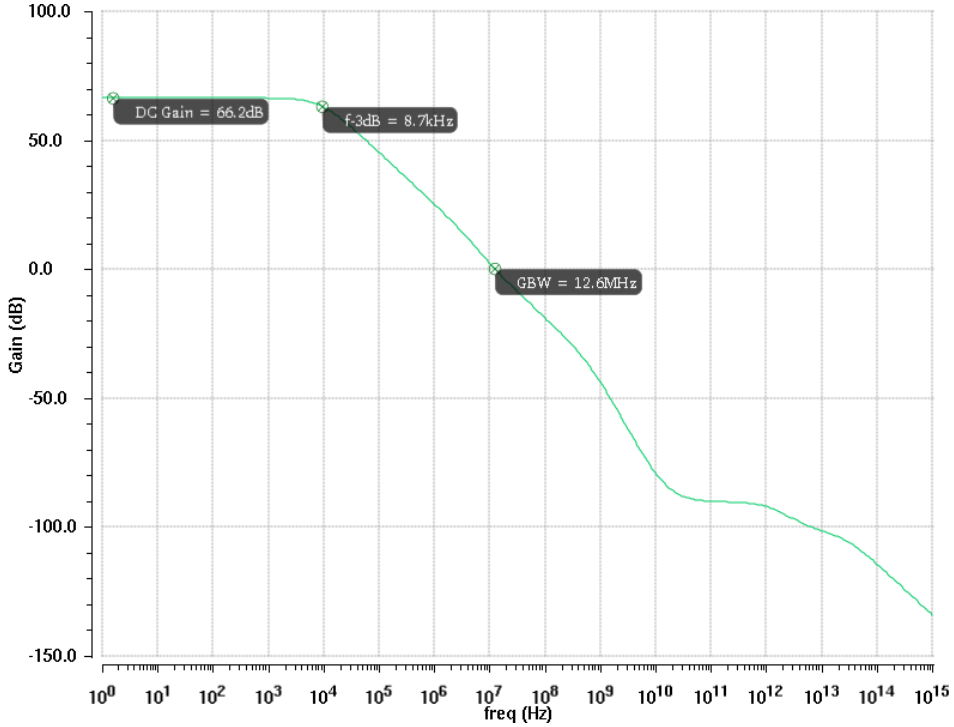


Fig. 5.27: Gain vs. frequency (two stage OTA)

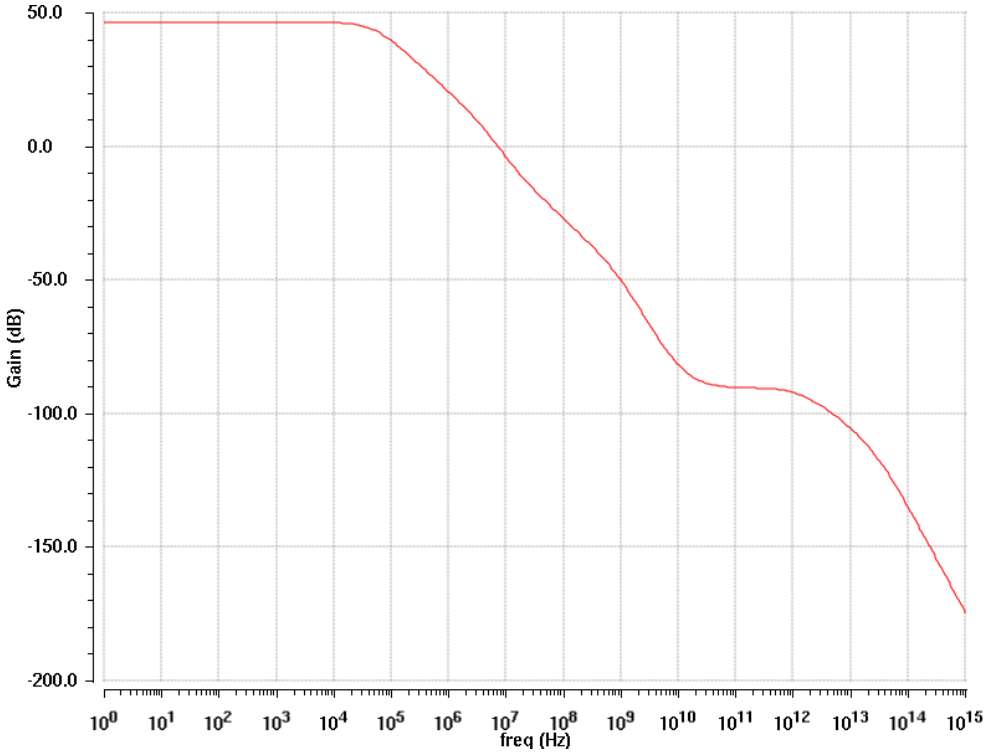


Fig. 5.28: Frequency Response with the gain enhancement disabled

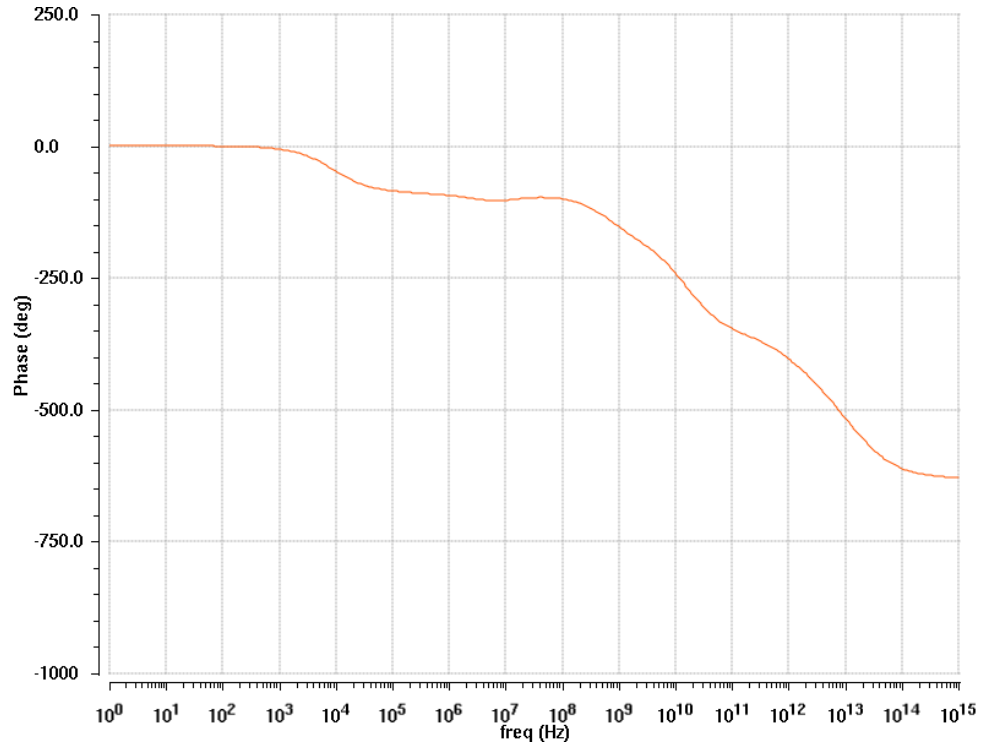


Fig. 5.29: Phase vs. frequency (two-stage OTA)

The frequency response of the Common-Mode gain is shown in Fig. 5.30 below,

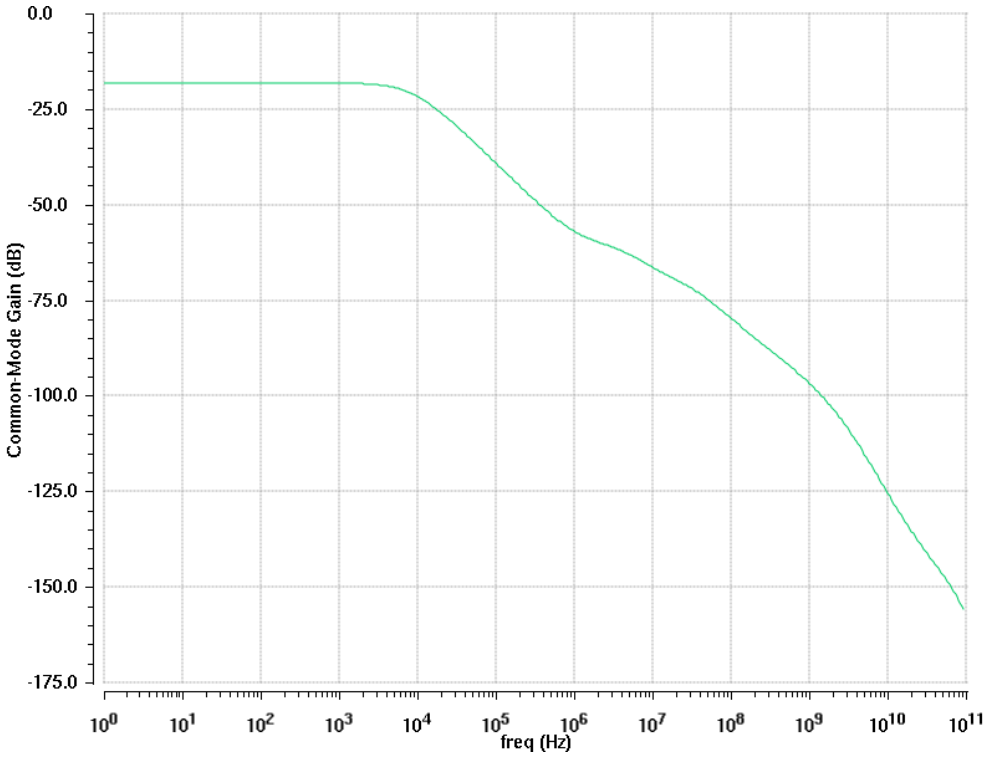


Fig. 5.30: Common-Mode gain response of two stage OTA

In order to measure of how well the amplifier rejects the signals common to both input leads, we use the CMRR (Common-Mode Rejection Ratio), which is defined as,

$$CMRR = 20\log\left(\frac{A_{diff}}{|A_{cm}|}\right),$$

where A_{diff} and A_{cm} are the differential and common-mode gain respectively. A high CMRR is important in applications where the signal of interest is represented by a small voltage fluctuation superimposed on a (possibly large) voltage offset, or when relevant information is contained in the voltage difference between two signals.

Moreover, as other analog circuits, op amps are often supplied from noisy lines and must therefore "reject" the noise adequately. For this reason, it is important to understand how noise on the supply manifests itself at the output of an op amp. Analytical analysis for the PSRR is reported in [42]. Fig. 5.31 depicts the PSRR response of the gate-input OTA. The Power Supply Rejection Ratio is defined as the gain from the input to the output divided by the gain from the supply to the output,

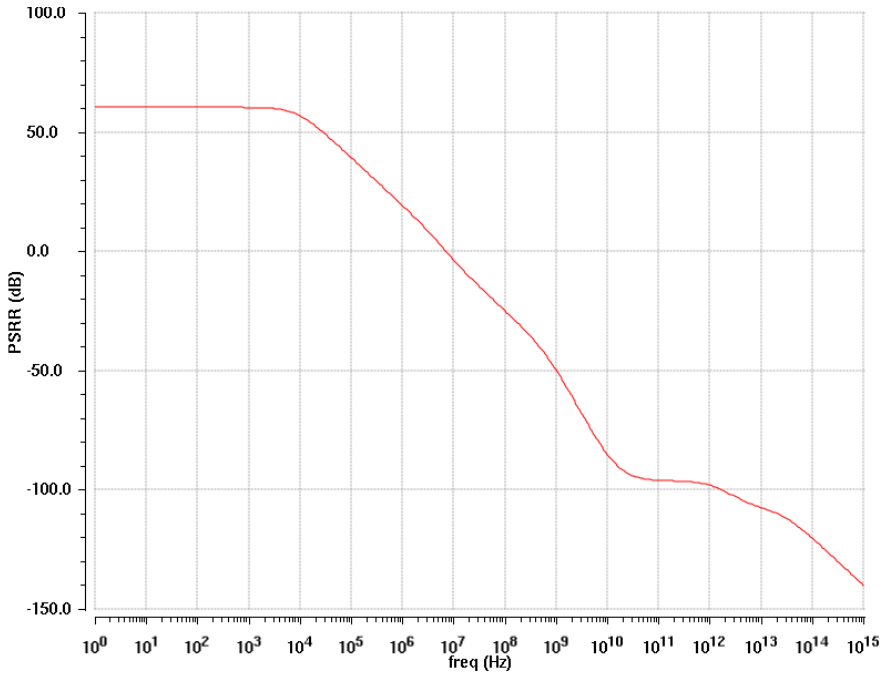


Fig. 5.31: PSRR response of two stage OTA

5.7.3 Transient Analysis Figures

The following figure shows the positive (red color) and negative (yellow color) output signals in the time domain

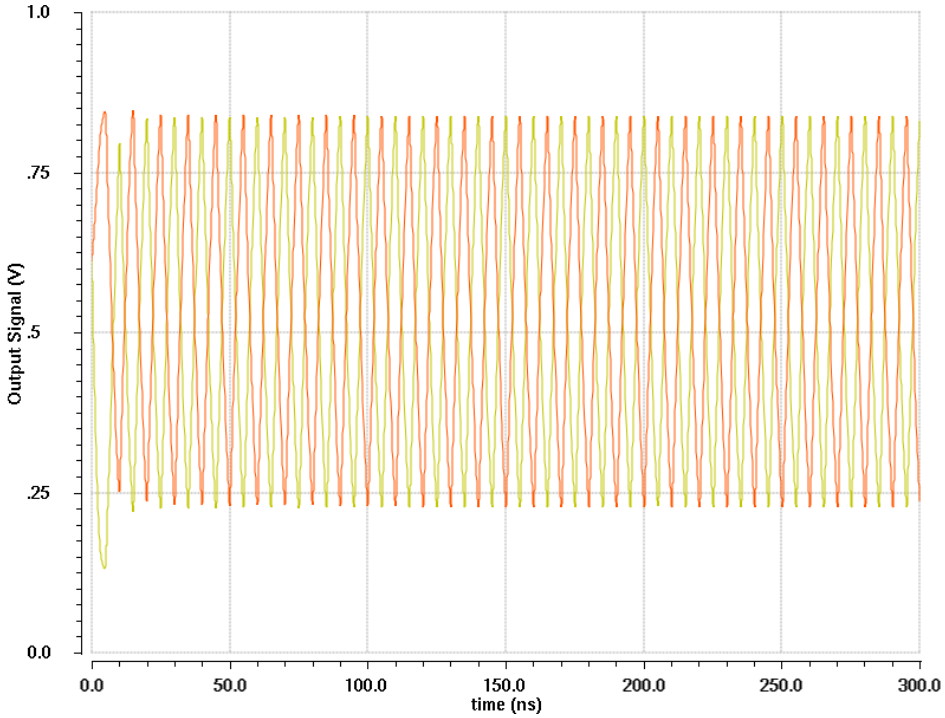


Fig. 5.32: Output Signals in time domain of two-stage OTA

As we can see, there is no clipping at the output signals because of the high Common-Mode Rejection Ratio of the amplifier. The Common-Mode gain is further reduced using the feed-forward cancellation path through transistors M_{10}, M_{12} and M_{13}.

Fig. 5.33 depicts the output signal of the circuit when the input devices are biased with a step function in order to simulate the Slew Rate of the amplifier.

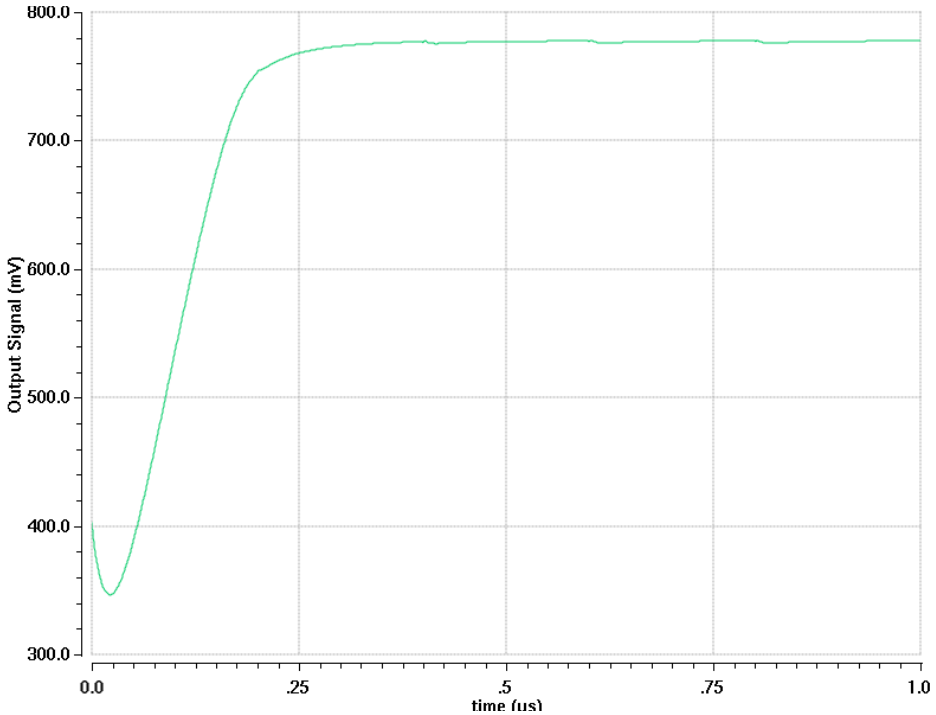


Fig. 5.33: Output Signal for Slew Rate simulation (two-stage OTA)

5.7.4 Noise Analysis Figures

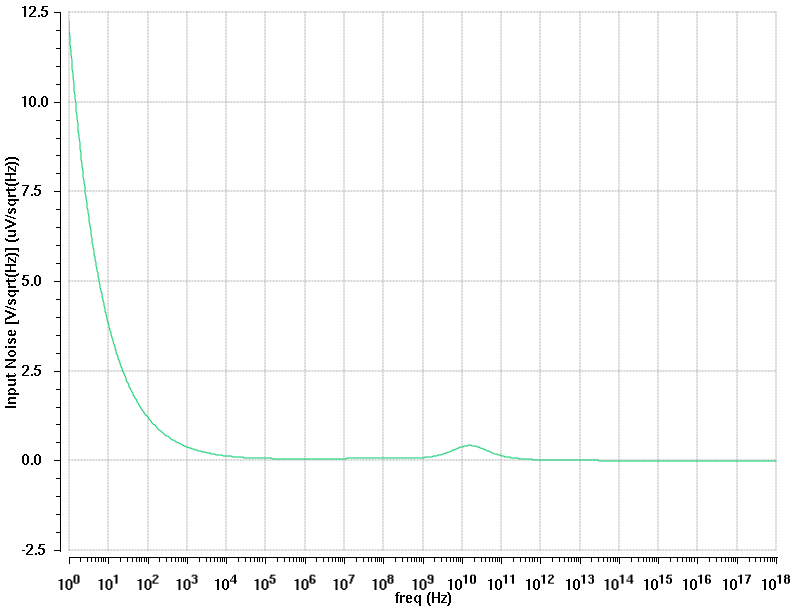


Fig. : Input – referred white noise spectral density

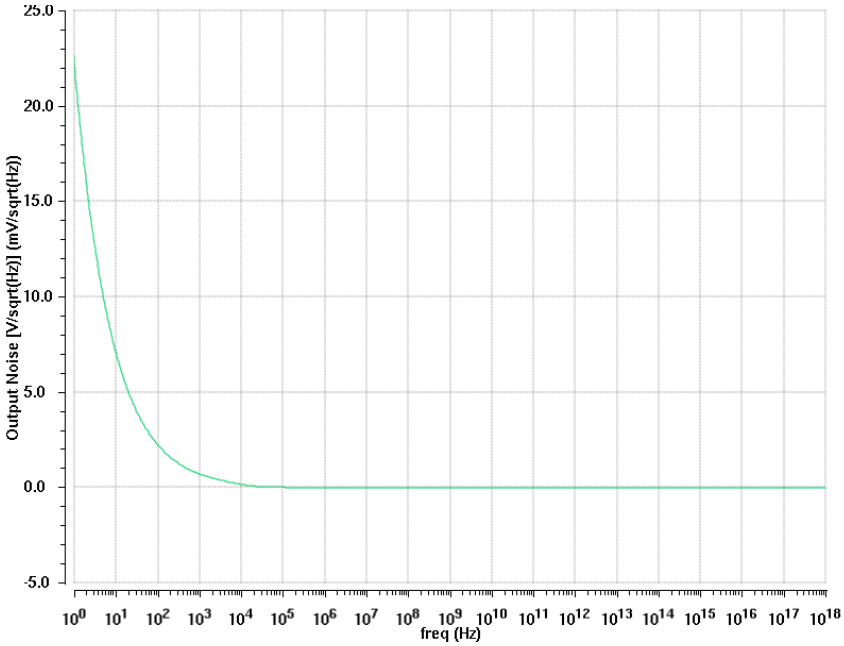


Fig. : Output – referred white noise spectral density

The following table shows the overall performance of the gate-input OTA,

Parameter	Value
Supply Voltage (V)	1
Power Dissipation (µW)	201
DC Gain (dB)	66.2 48*
GBW (MHz)	12.6
f_{-3dB} (kHz)	8.7
CMRR (dB)	84.5
PSRR (dB)	60
Slew Rate (V/µsec)	3.1
Load Capacitance (pF)	10
Phase Margin (Degrees)	79
Input ref. noise @ 10kHz $\left(nV/\sqrt{Hz}\right)$ (diff.)	132
Input ref. noise @ 1MHz $\left(nV/\sqrt{Hz}\right)$ (diff.)	53
100n**	630

*With the gain enhancement disabled

$$**n = \frac{GBW \cdot C_L}{I_{DD}}$$

Table 5.17: Two stage gate-input OTA performance

5.8 Fully Differential Gate-Input OTA Design at 0.5V

This section demonstrates the simulation results of a fully differential gate-input OTA design at a voltage supply of 0.5V. The design procedure is the same as described for the 1V OTA before. The only difference is that the forward body-biasing technique of the input devices is used in order to lower the threshold voltage and decrease the voltage headroom of the design. This allows designers to bias specific analog blocks (for example current mirrors) in moderate inversion, even in the onset of the strong inversion region.

The forward bias technique has been described in Section (2.4). The body effect is modeled by the following equation,

$$V_T = V_{T0} - \gamma\left(\sqrt{\varphi_0} - \sqrt{\varphi_0 + V_{BS}}\right)$$

where V_{BS} is the body-source voltage and ϕ_0 is equal to $2\Phi_F$ (Φ_F is the Fermi potential). Using this equation, it is easy to estimate the new threshold voltage and therefore the effective voltage V_{EFF}. As a result, the V_{GS} voltage can be calculated as well as the inversion coefficient of input devices. The following table presents the design specifications of the gate-input OTA,

Specifications	Value
Nominal supply voltage (V)	0.5
Total Current (μA)	120
Power Dissipation (μW)	60
Open-Loop Gain (dB)	≥ 50
GBW (MHz)	6.5
C_L (pF)	4

Table 5.18: Design specifications of 0.5V gate-input OTA

5.8.1 DC Analysis

The following table depicts the DC currents specifications of the amplifier,

Branch Currents	Value
$I_{DD}(\mu A)$	**120**
$I_{1A}(\mu A)$	**20**
$I_{2A}(\mu A)$	**20**
$I_{3A}(\mu A)$	**8**
$I_{4A}(\mu A)$	**7.5**
$I_{5A}(\mu A)$	**2**
$I_{6}(\mu A)$	**4**
$I_{R1A}(\mu A)$	**0.5**
$I_{out1}(\mu A)$	**27.5**
$I_{8A}(\mu A)$	**10**
$I_{9A}(\mu A)$	**10**
$I_{10A}(\mu A)$	**8**
$I_{11A}(\mu A)$	**7.5**
$I_{12A}(\mu A)$	**2**
$I_{13}(\mu A)$	**4**
$I_{R2A}(\mu A)$	**0.5**
$I_{out2}(\mu A)$	**17.5**

Table 5.19: DC currents specifications of 0.5V gate-input OTA

Table 5.20 depicts the selected inversion coefficients of the devices,

Transistor	IC
M_1	2.85
M_2	1.5
M_3	5
M_4	0.01
M_5	2.85
M_6	5
M_8	0.01
M_9	1.5
M_{10}	5
M_{11}	0.01
M_{12}	0.01
M_{13}	5

Table 5.20: IC selection for the 0.5V gate-input OTA

After the drain current and inversion coefficient selection, the MOS devices have been sized properly according to the procedure that has been described above. Table 5.21 summarizes the component sizes and values for the gate-input OTA,

	First Stage			Second Stage	
Transistors	$W(\mu m)$	$L(\mu m)$	**Transistors**	$W(\mu m)$	$L(\mu m)$
M_{1A}, M_{1B}	3.04	0.28	M_{8A}, M_{8B}	800	0.28
M_{2A}, M_{2B}	32.9	0.28	M_{9A}, M_{9B}	16.4	0.28
M_{3A}, M_{3A}	3.94	0.28	M_{10A}, M_{3A}	4	0.28
M_{4A}, M_{4A}	700	0.28	M_{11A}, M_{11A}	700	0.28
M_{5A}, M_{5A}	10	0.28	M_{12A}, M_{12A}	600	0.28
M_6	2.46	0.28	M_{13}	2	0.28
M_7	1	0.28	M_{14}	1	0.28
Resistors/Capacitors			**Resistors/Capacitors**		
R_{1A}, R_{1B}	$100k\Omega$		R_{2A}, R_{2B}	$100k\Omega$	
			C_L	$4pF$	
			R_C	$10k\Omega$	
			C_C	$1pF$	

Table 5.21: Component sizes and values for the 0.5V gate-input OTA

The DC simulation results are summarized in Table 5.22,

Transistor/Branch	Current (μA)	IC	Transistor/Branch	Current (μA)	IC
M_1	20.5	2.7	M_8	10.5	0.01
M_2	20.1	1.2	M_9	10.9	1.3
M_3	9.8	4.8	M_{10}	8.5	4.9
M_4	8	0.009	M_{11}	8.3	0.01
M_5	1.96	2.5	M_{12}	1.85	0.01
M_6	3.9	4.8	M_{13}	3.8	4.9
M_7	1.05	-	M_{14}	1.05	-
Output Branch	28.4	-	Output Branch	18.8	
Total Level-Shifting Current Source I_L	1.05	-	Total Level-Shifting Current Source I_L	1.05	

Table 5.22: DC Simulation Results of the 0.5V gate-input OTA

The following figure depicts the DC transfer characteristics of the gate-input OTA,

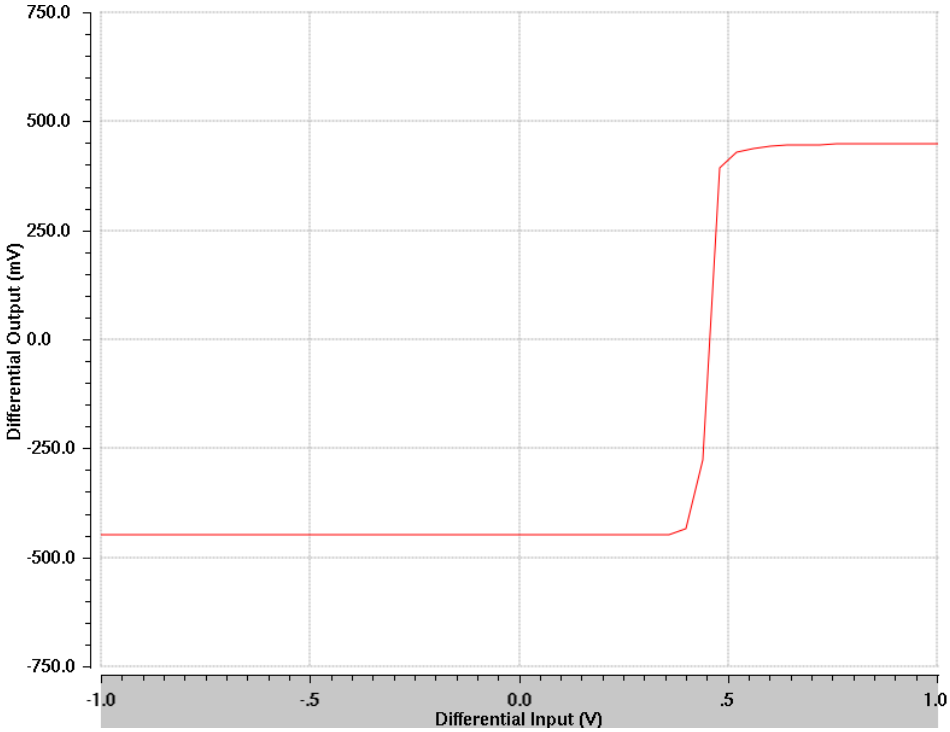


Fig. 5.34: DC input-output characteristics of 0.5V gate-input OTA

5.8.2 Frequency Response Figures

The following figures shows the frequency response of the gate-input OTA, Gain vs. frequency and Phase vs. frequency respectively,

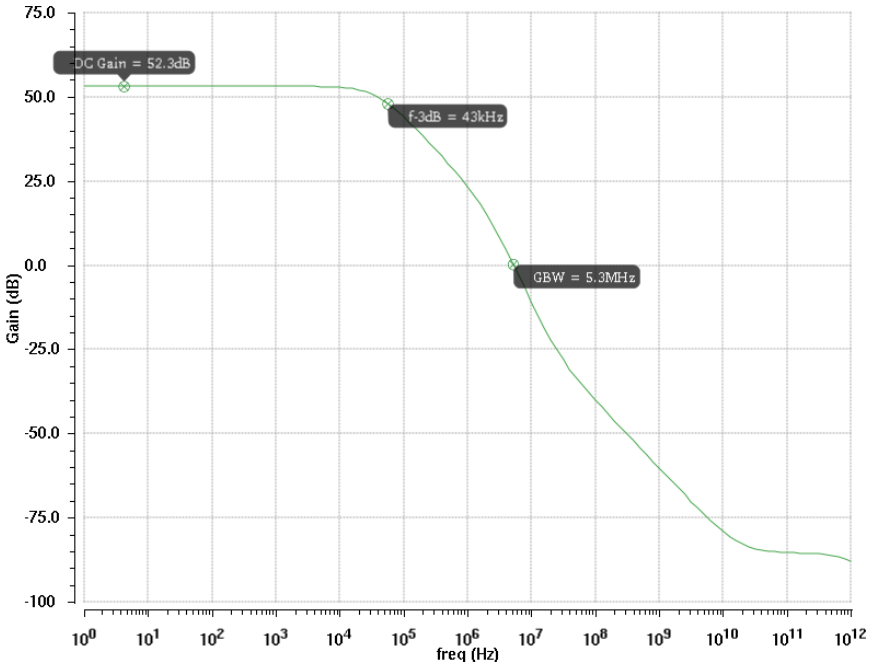


Fig. 5.35: Gain vs. frequency (0.5V OTA)

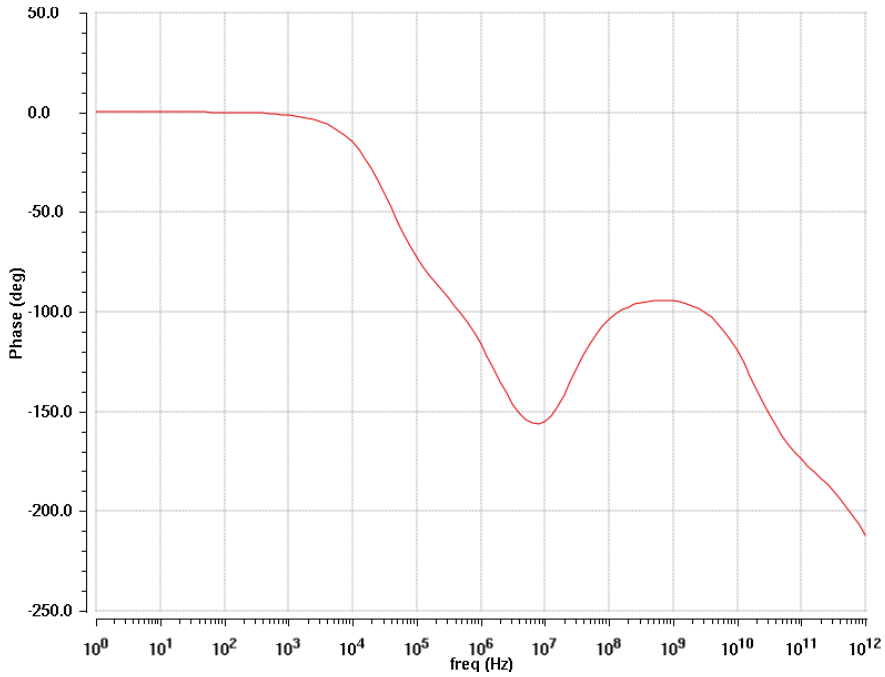


Fig. 5.36: Phase vs. frequency (0.5V OTA)

On the other hand, the DC gain of the amplifier is lower when the negative topology that consists of transistors M_4 (in the first stage) and M_{11} (in the second stage) are disabled. Fig. 5.37 shows the frequency response of the circuit,

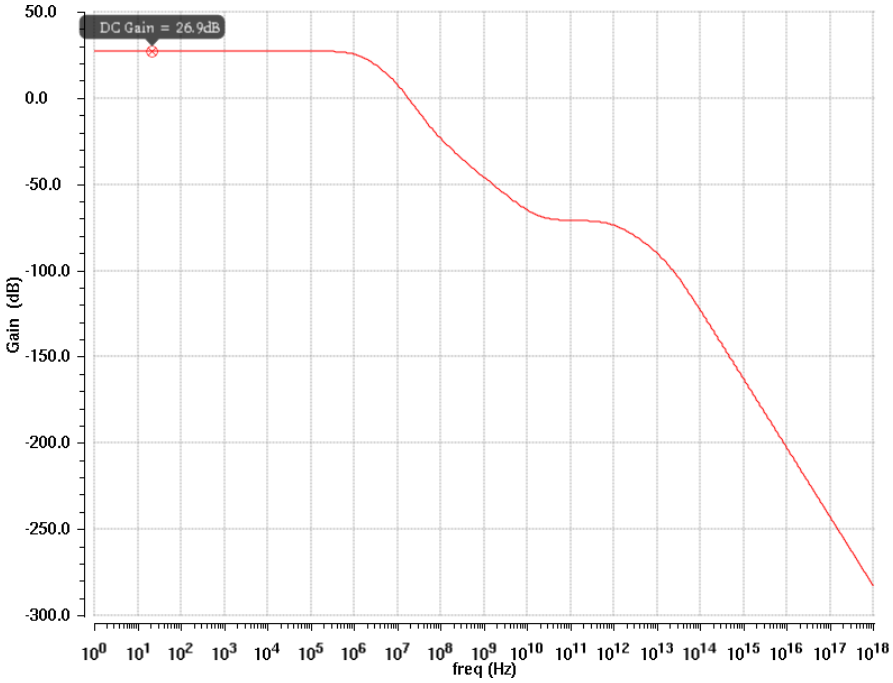


Fig. 5.37: Frequency Response without the gain enhancement disabled

The Common-Mode gain of the amplifier is presented in Fig. 5.38 below,

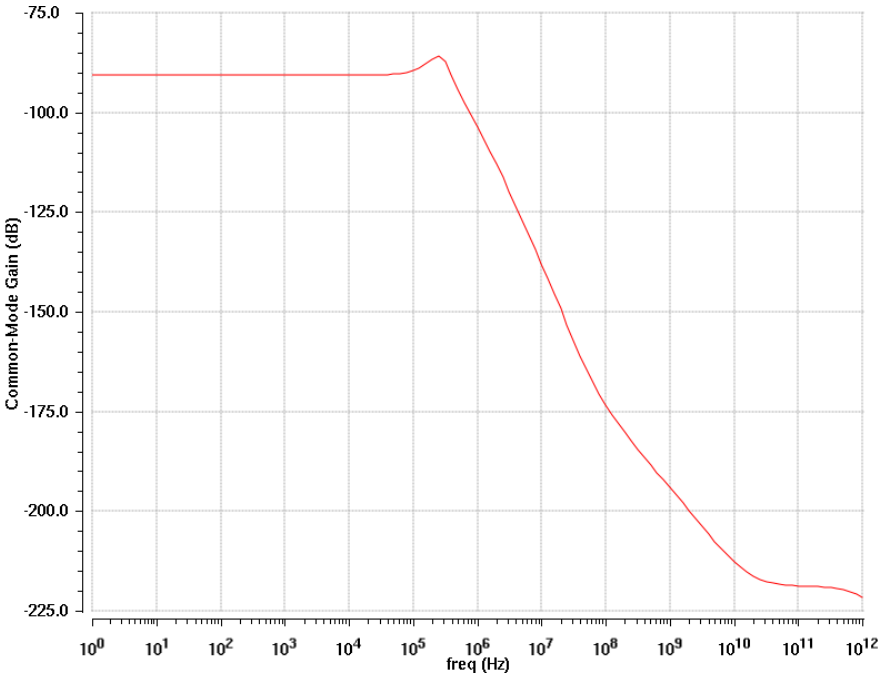


Fig. 5.38: Common-Mode gain response (0.5V OTA)

It must be pointed out that not only does the differential gain need to be significantly larger than the common-mode gain, the common-mode gain also needs to be sufficiently less than 1, due to the possible presence of positive feedback loops in the common-mode signal paths.

Additionally, Fig. 5.39 shows the PSRR (Power Supply Rejection Ratio) of the amplifier,

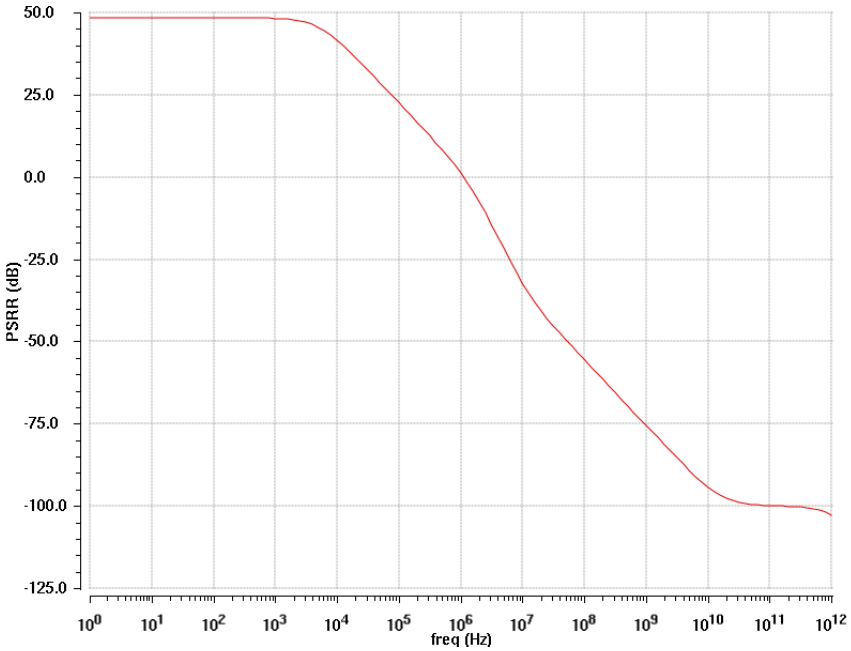


Fig. 5.39: PSRR response (0.5V OTA)

5.8.3 Transient Analysis Figures

The following figure shows the positive (red color) and negative (yellow color) output signals in the time domain

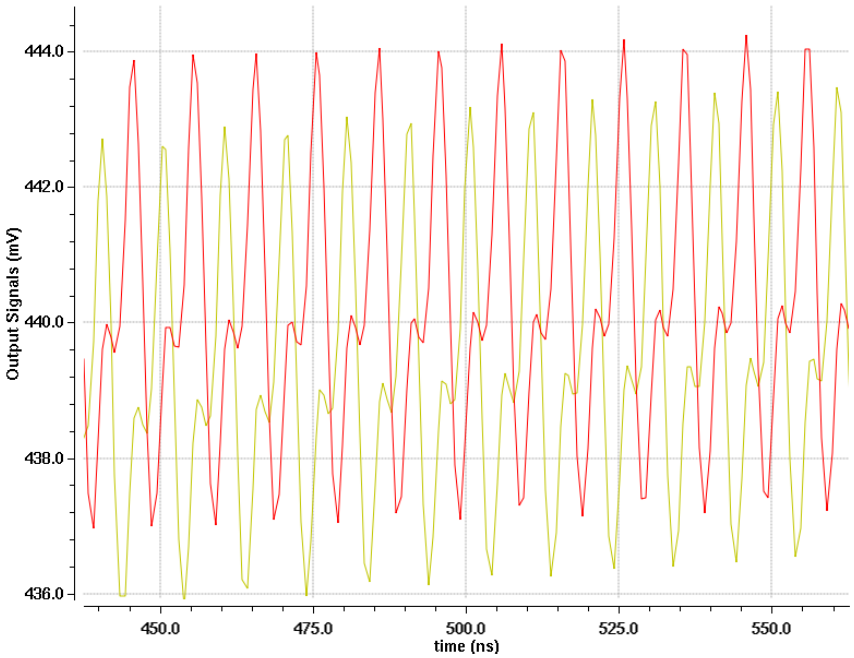


Fig. 5.40: Output signals in time domain (0.5V OTA)

Additionally, Fig. 5.41 depicts the output signal of the circuit when the input devices are biased with a step function in order to simulate the Slew Rate of the amplifier.

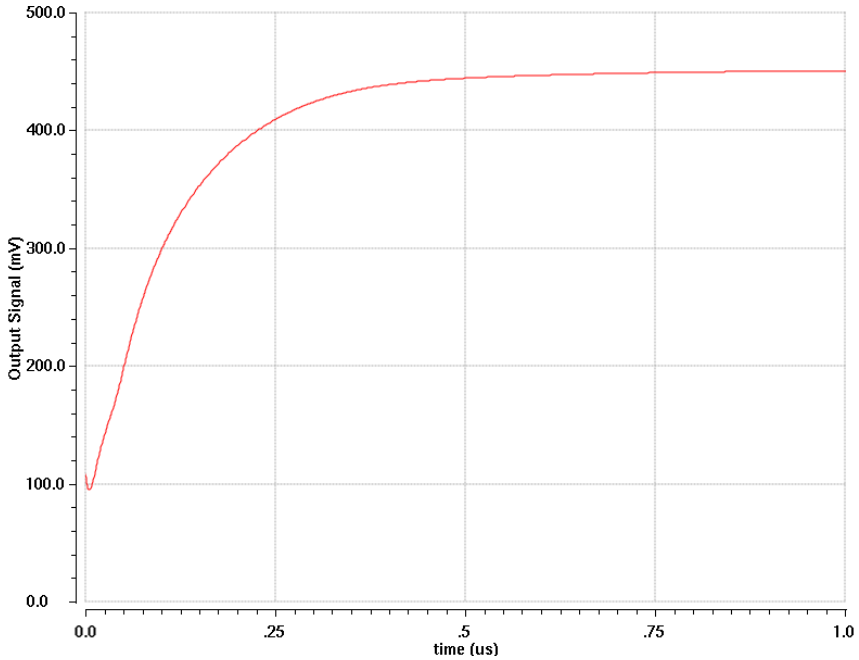


Fig. 5.41: Output Signal for Slew Rate simulation (0.5V OTA)

5.8.4 Noise Analysis Figures

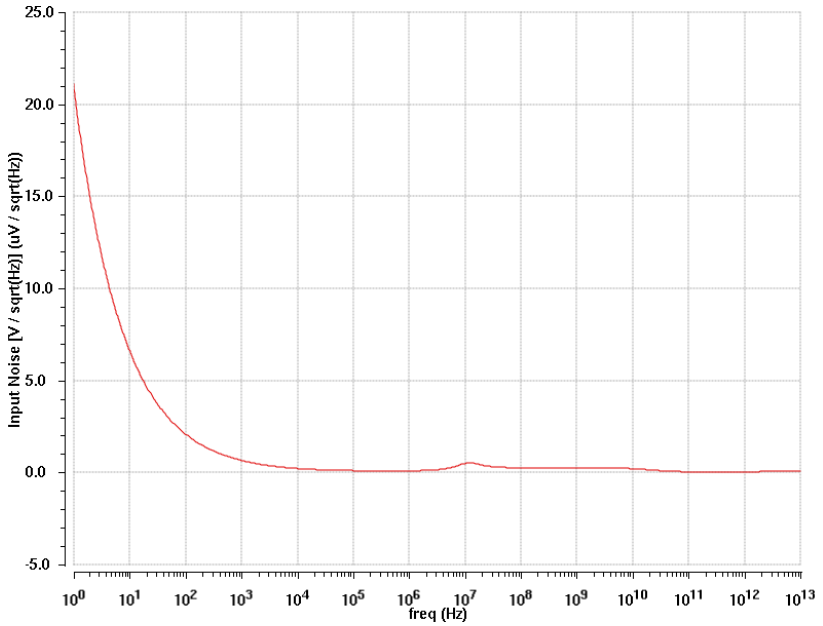


Fig. : Input – referred white noise spectral density

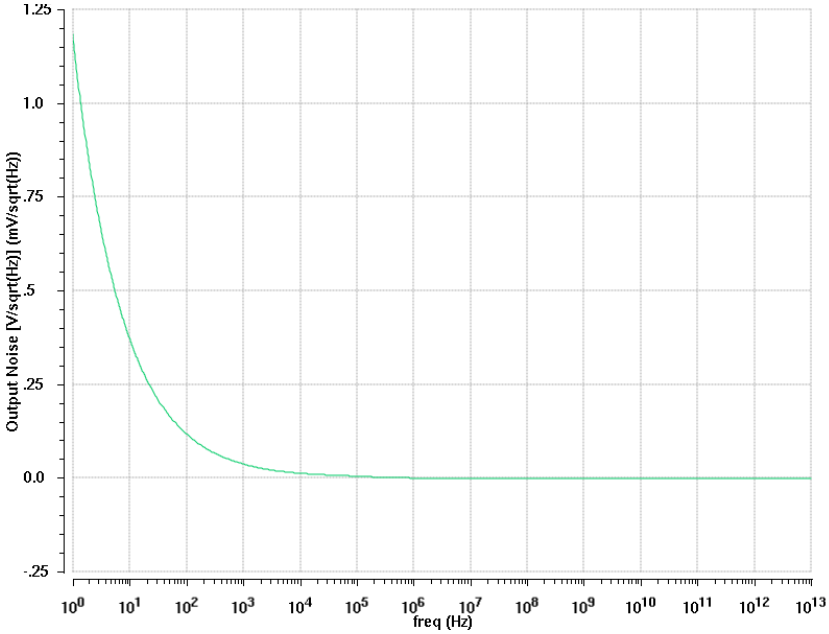


Fig. : Output – referred white noise spectral density

The following table shows the overall performance of the gate-input OTA,

Parameter	Value
Supply Voltage (V)	0.5
Power Dissipation (µW)	53.7
DC Gain (dB)	52.3 26.9*
GBW (MHz)	5.3
f_{-3dB} (kHz)	43
CMRR (dB)	142.3
PSRR (dB)	48.9
Slew Rate (V/µsec)	2.9
Load Capacitance (pF)	4
Phase Margin (Degrees)	30
Input ref. noise @ 10kHz $\left(nV/\sqrt{Hz}\right)$	234
Input ref. noise @ 1MHz $\left(nV/\sqrt{Hz}\right)$	109
100n (1/V)**	198

*With the gain enhancement biasing disabled

$$**n = \frac{GBW \cdot C_L}{I_{DD}}$$

Table 5.23: 0.5V gate-input OTA performance

CHAPTER 6:Ultra-Low Voltage 5th-Order Low-Pass Elliptic Filter

This chapter demonstrates the capabilities and synergy of the proposed ultra-low voltage designs in Chapters 2 and 3. A 5th-order low-pass elliptic filter with a 12.5 kHz cut-off frequency has been designed.

6.1 Elliptic Filter Theory

The frequency response of an Nth-elliptic filter has a ripple in both pass-band and stop-band. The magnitude squared frequency response of a normalized low-pass elliptic filter of order n is defined by,

$$\left|H_N\left(j\omega\right)\right|^2 = \frac{1}{1+\varepsilon^2 R_N^2\left(\omega\right)} \quad (6.1)$$

where $R_N\left(\omega\right)$ is a Chebyshev rational function of ω determined from the specific ripple characteristics.

For a given order n, an elliptic filter is the only type of filters that has the fastest transition between pass-band and stop-band (this is called the transition band between ω_p and ω_s, as shown in Fig. 6.1). A parameter ω_r, representing the sharpness of the transition region is defined as,

$$\omega_r = \frac{\omega_s}{\omega_p} \quad (6.2)$$

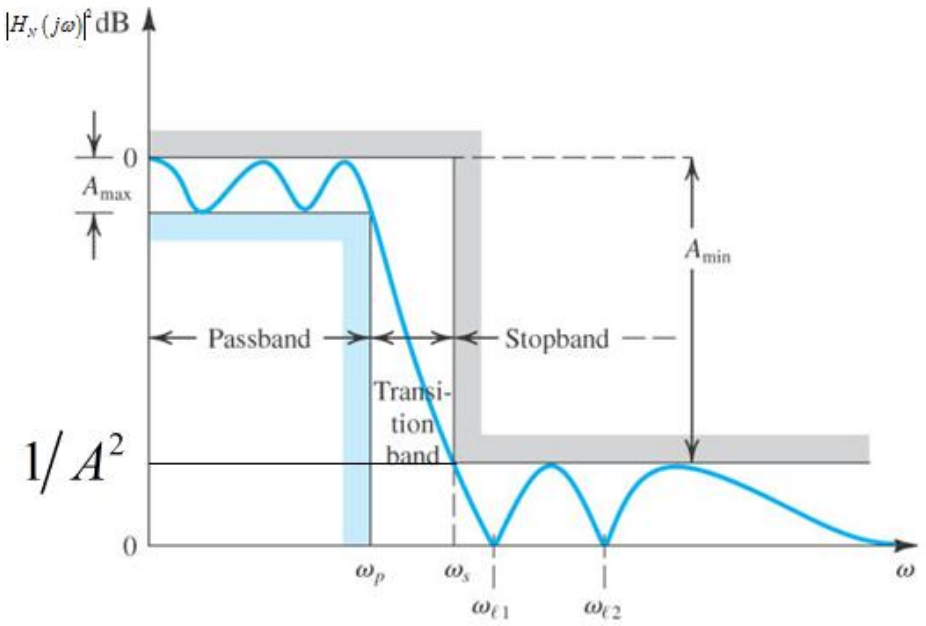


Fig. 6.1: Frequency response of a low-pass filter

A large value of ω_r indicates a large transition band, while a small value of ω_r indicates a small transition band.

The amount of ripple in each band is independently adjustable, and no other filter of equal order can have a faster transition in gain between the pass-band and the stop-band, for the given values of ripple (whether the ripple is equalized or not). As the ripple in the stop-band approaches zero, the filter

becomes a type **I Chebyshev** filter. As the ripple in the pass-band approaches zero, the filter becomes a type **II Chebyshev** filter and finally, as both ripple values approach zero, the filter becomes a **Butterworth** filter.

The general transfer function $H_n(s)$, for the normalized low-pass elliptic filter is given from odd and even n by,

$$H_n(s) = \frac{H_0}{(s+s_0)} \prod_{i=1}^{\frac{N-1}{2}} \frac{s^2 + A_{0i}}{s^2 + B_{1is} + B_{0i}} \text{, for odd N (6.3)}$$

$$H_n(s) = H_0 \prod_{i=1}^{\frac{N}{2}} \frac{s^2 + A_{0i}}{s^2 + B_{1is} + B_{0i}} \text{, for even N (6.4)}$$

In order to design an elliptic low-pass filter, the design parameters N, H_0, A_{0i}, B_{1i} and B_{0i}, have to be determined from the design specifications,

1. ε
2. A
3. ω_r

or equivalently G_1, G_2 and ω_r, where,

$$G_1 = 20\log\left[\frac{1}{(1+\varepsilon^2)}\right] = 20\log\left|H_n(j\omega_p)\right| (6.5)$$

$$G_2 = 20\log\left[\frac{1}{A^2}\right] = 20\log\left|H_n(j\omega_s)\right| (6.6)$$

By finding the G_1 and G_2, the ω_r requirement will not be satisfied exactly; however, an ω_r can be selected that exceeds the requirements.

In conclusion, the transition of a low-pass filter is determined by the following parameters:

1. The pass-band frequency ω_p.
2. The maximum variation in pass-band region A_{max}.
3. The stop-band frequency ω_s.
4. The minimum attenuation in stop-band region A_{min}.

6.2 1V 5th-Order Low-Pass Elliptic Filter

The following figure presents the schematic of the filter that has been designed in Cadence. The filter consists of integrators and gate-input OTAs. The sizing of the individual gate-input OTA is scaled depending on the loading requirements, by connecting multiple units in parallel, with all internal nodes of the OTAs connected to each other. This allows comparable phase and distortion performance for all five stages. As a result, the first integrator stage of the filter uses two OTA units in parallel, the second uses two OTA units, the third uses four OTA units, the fourth uses one OTA unit, and the fifth uses two OTA units in parallel.

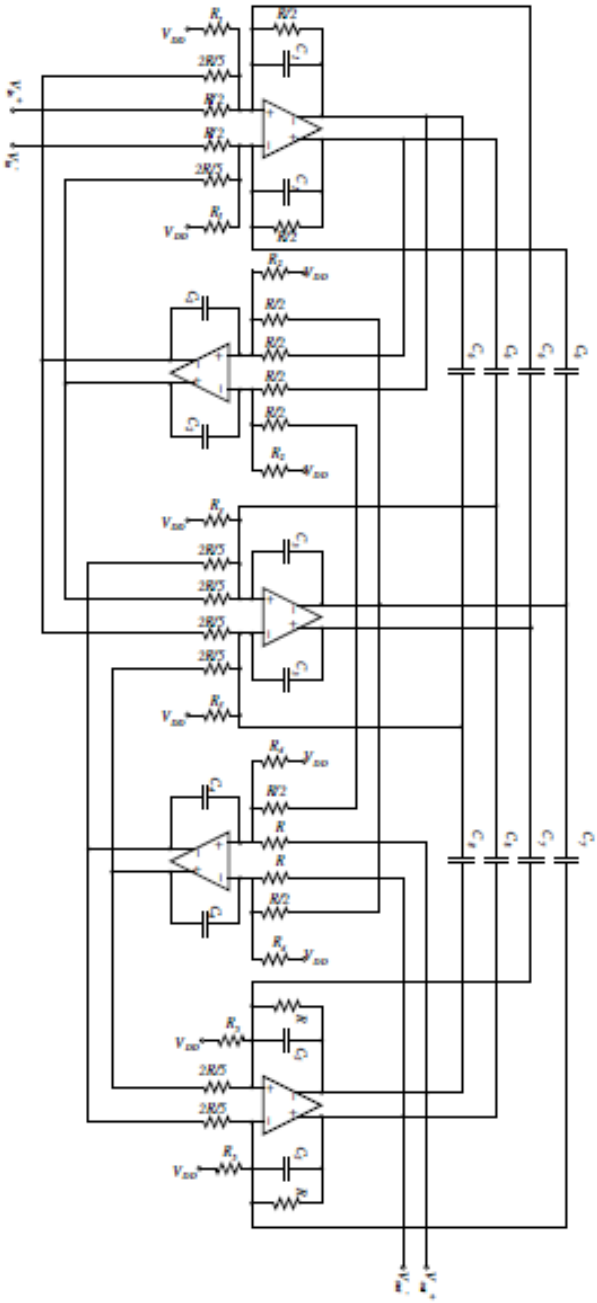


Fig. 6.2: 5th-order Low-pass elliptic filter

The filter characteristics has a pass-band ripple of 0.01dB, a stop-band rejection of at least 53dB, and two zeros in the stop-band – at 42.5 kHz and at 89.1 kHz. To obtain an accurate transfer characteristic, the OTA should have substantial open-loop gain all the way to 89.1 kHz, the second zero of the filter. The proposed amplifier has a worst-case gain of 45dB at 89.1 kHz, which is sufficient.

The filter resistors and capacitors are shown in Table 6.1,

Capacitor	Value	Resistor	Value
C_1	10pF	R	365kΩ
C_2	10pF	R_1	30kΩ
C_3	10pF	R_2	50kΩ
C_4	10pF	R_3	40kΩ
C_5	10pF	R_4	66.7kΩ
C_6	1.8pF	R_5	57.2kΩ
C_7	5.7pF		
C_8	2.9pF		

Table 6.1: Filter resistors and capacitors values

The following figure depicts the frequency response of the elliptic filter,

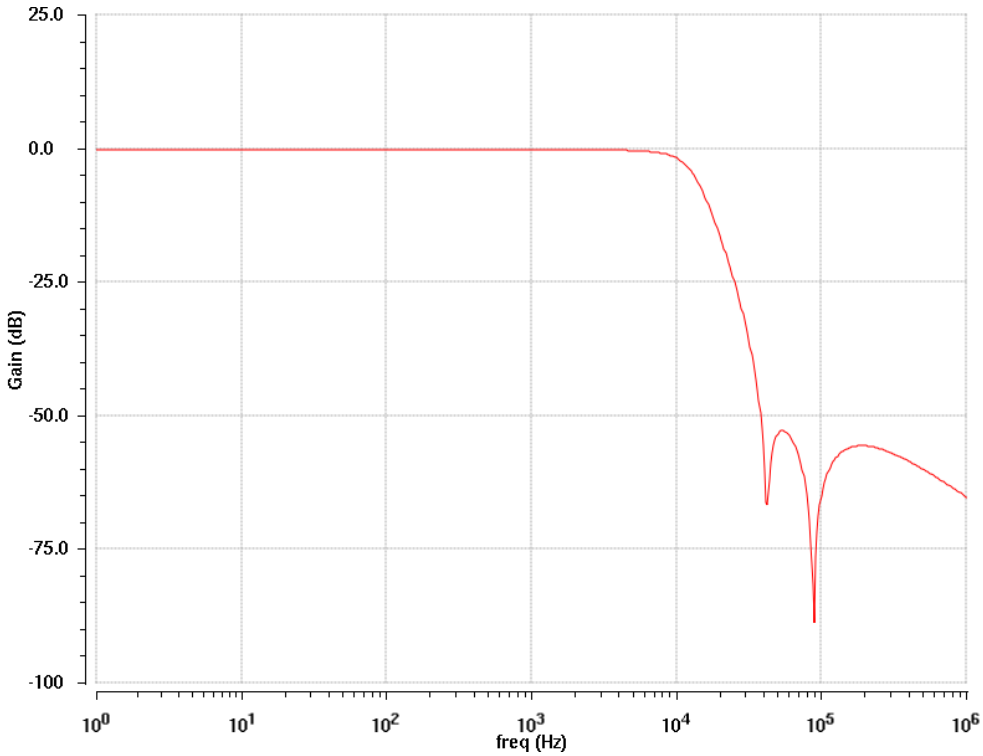


Fig. 6.3: Simulated filter characteristics, Gain vs. frequency (V_{DD}=1V)

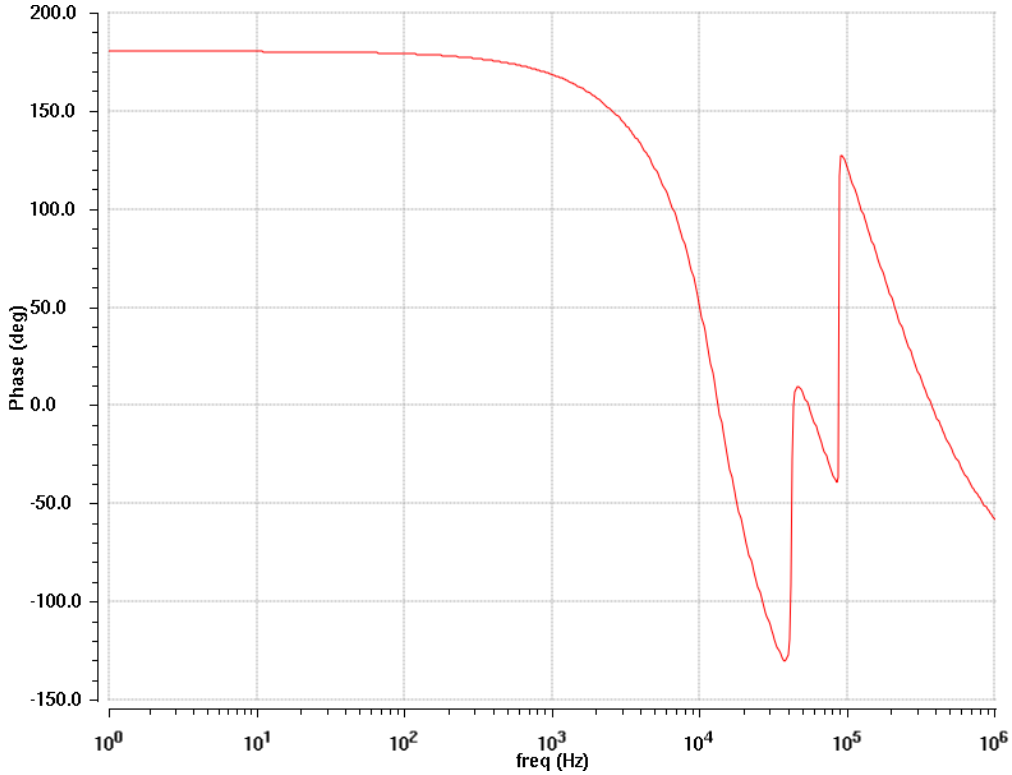


Fig. 6.4: Simulated filter characteristics, Phase vs. frequency (V_{DD}=1V)

Table 6.2 summarizes the 5th-order low-pass elliptic filter performance,

Parameter	Value
Supply voltage(V)	1
-3dB cut-off frequency (kHz)	12.5
Power Dissipation (mW)	2.2
Zero frequency 1 (kHz)	42.5
Zero frequency 2 (kHz)	89.1
Pass-band ripple (dB)	0.01
Stop-band ripple (dB)	-53

Table 6.2: 1V 5th-order low-pass elliptic filter performance

6.2 0.5V 5th-Order Low-Pass Elliptic Filter

Additionally to the design of the 1V low-pass, elliptic filter, the same system has been simulated for a lower supply voltage of 0.5V. The following figure presents the frequency response (Gain vs. frequency) of the 0.5V elliptic filter,

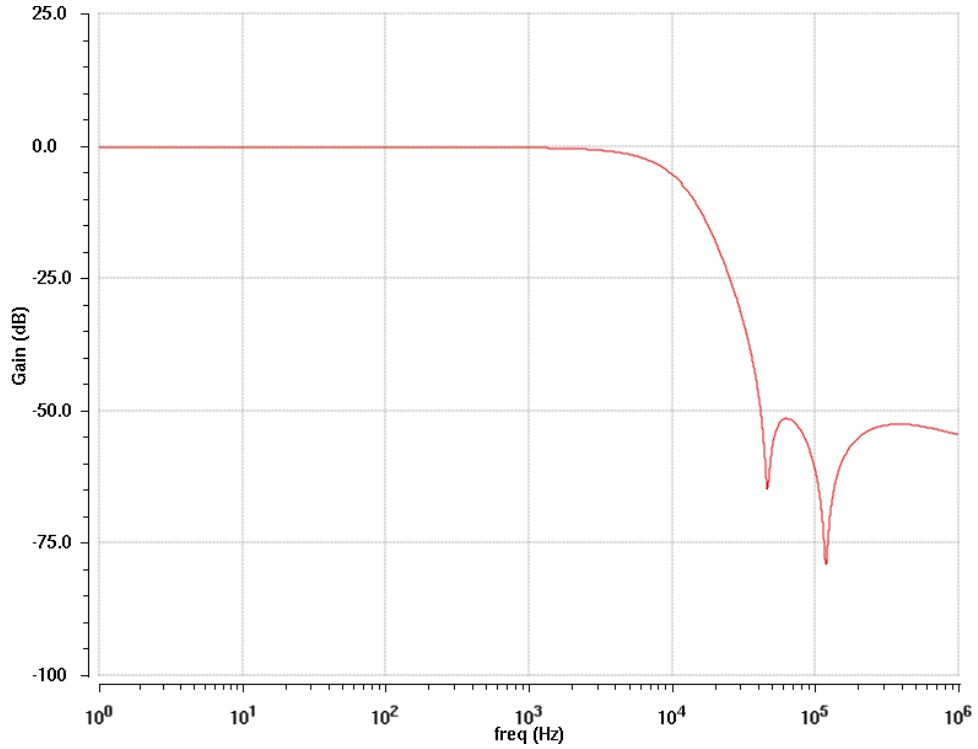


Fig. 6.5: Gain vs. frequency of the 0.5V low-pass elliptic filter

Fig. 6.6 shows the phase of the filter as a function of frequency,

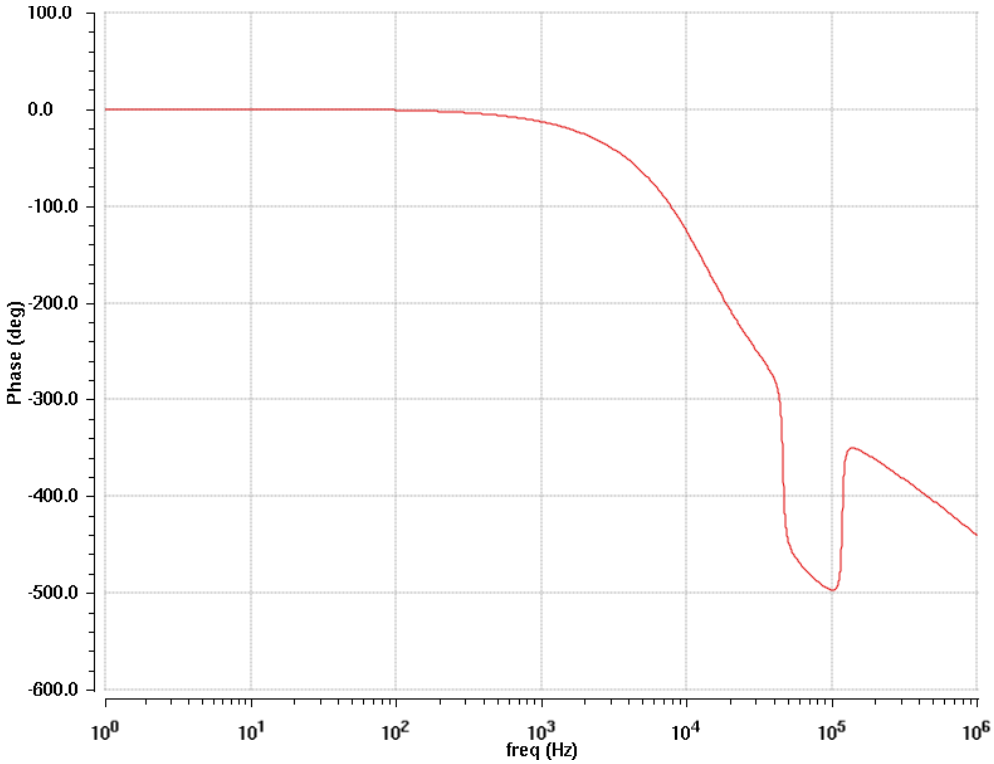


Fig. 6.6: Phase vs. frequency of the 0.5V low-pass elliptic filter

The filter has a cut-off frequency of 10kHz, a pass-band ripple of 0.01dB, a stop-band rejection of -50dB and two zeros – at 46kHz and at 110kHz.The proposed gate-input OTA has a worst-case gain of 48dB at 110kHz, which is sufficient. Table 6.3 summarizes the overall performance of the 0.5V low-pass elliptic filter,

Parameter	Value
Supply voltage(V)	0.5
-3dB cut-off frequency (kHz)	12.1
Power Dissipation (μW)	591
Zero frequency 1 (kHz)	46
Zero frequency 2 (kHz)	110
Pass-band ripple (dB)	0.01
Stop-band ripple (dB)	-50

Table 6.3: 0.5V 5^{th}-order low-pass elliptic filter performance

As again seen in Fig. 6.5, the pass-band ripple approaches the zero value and therefore the circuit acts as a type **I Chebyshev filter**. Frequencies ω_p and ω_s are equal to 10kHz and 39KHz respectively. As a result, the sharpness of the transition region is almost equal to ω_r=3.9, which is a large value for the design of an elliptic filter. On the other hand, for the same order, this filter has faster transition in gain between pass-band and stop-band than the other known types of filter (Butterworth, Chebyshev type I and II).

CHAPTER 7: Conclusion – Future Work

7.1 Conclusion

The purpose of this work was the design of a fully differential gate-input operational transconductance amplifier in two low supply voltages, 1V and 0.5V. The design procedure was based on specific low-voltage techniques such as Drain-Bulk and Grounded-Gate MOSFET connection. For these configurations, real measurements have been performed in order to analyze and investigate their behavior in designing analog circuits. Another interesting technique that used in design of this work was the body forward bias of the MOS devices in order to lower the threshold voltage. This technique resulted in a larger gate effective voltage V_{EFF}, which is important for biasing current mirrors in the onset of strong inversion.

In the context of 1V supply voltage, the proposed gate-input amplifier has an open-loop gain of 66.2dB, a GBW product of 12.6MHz, a power dissipation of 200μW and a slew rate of 3.1V/μsec. On the contrary, in the context of 0.5V supply voltage, the proposed amplifier has an open-loop gain of 53dB, a GBW product of 5.5MHz, a power dissipation of 54μW and a slew rate of 2.9V/μsec. Table 6.4 presents a comparison with other low voltage OTA designs,

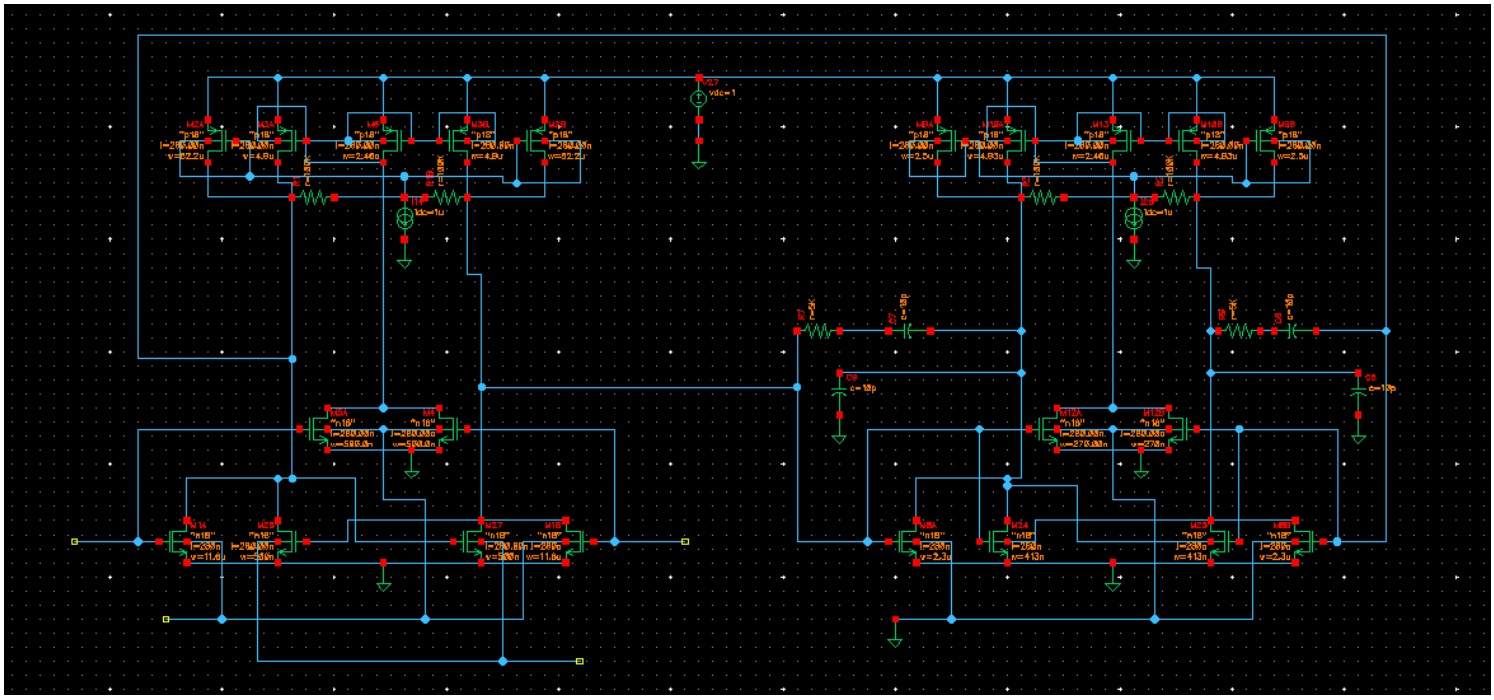
Parameter	[30]	[36]	[37]	[38]	[71]	[72]	**[50]**	**This work**	**This work**
Supply (V)	1	1	0.8	0.9	1.3	0.9	0.5	1	0.5
DC Gain (dB)	49	70	53	70	84	59	62	66.2	52.3
GBW (MHz)	1.3	0.2	1.3	6kHz	1.3	4	10	12.6	5.3
Power (μW)	300	5	-	0.5	460	-	75	201	53.7
CMRR (dB)	-	-	-	-	-	-	85	84.5	142
PSRR (dB)	-	-	-	-	-	-	-	60	48.9
Slew Rate (μV/sec)	-	-	-	-	-	-	2.7	3.1	2.9
Input ref. noise @ 10kHz $\left(nV/\sqrt{Hz}\right)$	-	-	-	-	-	-	120	132	234
Input ref. noise @ 1MHz $\left(nV/\sqrt{Hz}\right)$	-	-	-	-	-	-	100	53	109
C_L (pF)	22	7	20	12	-	14	20	10	4
Technology(μm)	2	0.35	0.5	2.5	0.7	0.5	0.18	0.18	0.18
100n (1/V)	9.5	28	-	13	-	-	133.4	630	198

Table 6.4: Comparison with other low voltage OTA designs

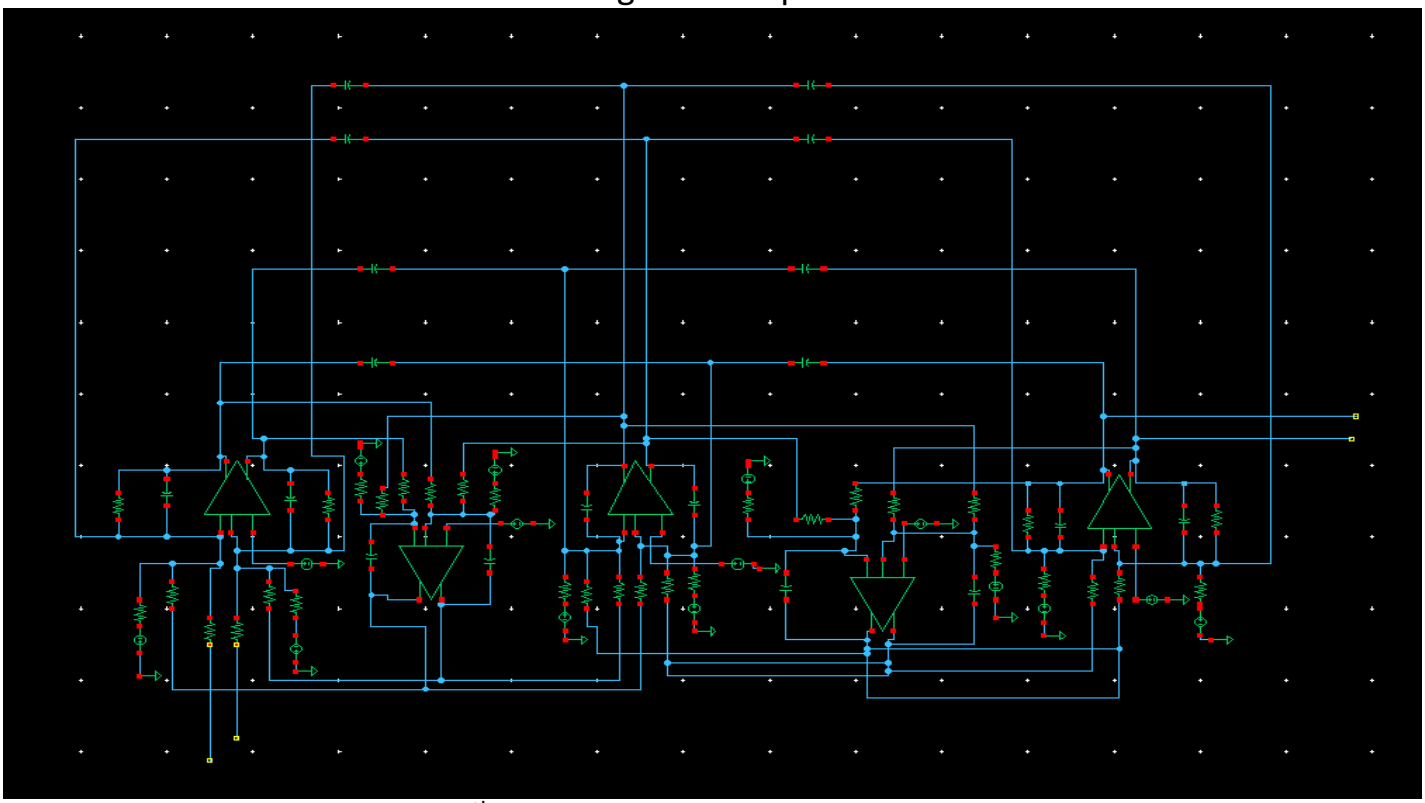
7.2 Future Work

Further work would be dedicated to implementing the basic configuration of the gate-input OTA using zero-V_T MOS devices without accessing the body terminal. Also, capacitors would be replaced by weak inversion MOS varactors in order to use them in designing the 5^{th}-order low-pass elliptic filter. Moreover, future work would include investigation of the impact of mismatch (current mismatch in current mirrors and/or voltage mismatch in input differential pairs) on the DC and AC performance of the gate-input OTA. The mismatch could be simulated using Monte Carlo analysis that is provided by Cadence Tools. Furthermore, on-chip biasing circuits could be designed in order to forward bias the body-source junctions of the input stage (M_{1A}-M_{1B}) and negative conductance topologies (M_{4A}-M_{4B}). Finally, grounded-gate MOS connected devices would be under more detailed investigation in order to find out more advantages of using them in designing amplifiers, filters and other basic analog building blocks.

Appendix



Two-stage Gate-Input OTA



5th-order Low-Pass Elliptic Filter

References

[1]Y. Tsividis, “Moderate inversion in MOS devices,” *Solid-State Electronics*,vol.25,pp.1099–1104,Nov.1982.

[2]Shouri Chatterjee, K.P.Pun, Nebojsa Stanic, Yannis Tsividis, Peter Kinget, “Analog Circuit Design Techniques at 0.5V”, Springer.

[3]C. Enz, F. Krummenacher, E. Vittoz, “An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low- Voltage and Low-Current Applications”, Analog Integrated Cicruits and Signal Processing, Vol. 8, pp. 83-114, 1995. J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp. 68–73.

[4]M. Bucher, “Analytical MOS Transistor Modelling for Analog Circuit Simulation”, *Ph. D. Thesis N° 2114 (1999)*, Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland, 2000.

[5]D. M. Binkley, C. E. Hopper, S. D. Tucker, B. C. Moss, J. M. Rochelle, D. P. Foty, “A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design”, *IEEE Trans. Computer-Aided Design of Int. Circ. & Syst.,* pp. 225-237, Vol. 22, N° 2, February 2003. R. Nicole, “Title of paper with only first word capitalized,” J. Name Stand. Abbrev., in press.

[6]M.Bucher, D. Kazasis, F. Krummenacher, D. Binkley, D. Foty, Y. Papananos, “Analysis of Transconductances at All Levels of Inversion in Deep Submicron CMOS”, 9th *IEEE Conf. on Electronics, Circ & Syst. (ICECS 2002)*, Vol. III, pp. 1183-1186, Dubrovnik, Croatia, September 15-18, 2002.

[7]A. Tajalli, E. Brauer, Y. Leblebici, E. Vittoz, “Subthreshold Source- Coupled Logic Circuits for Ultra-Low-Power Applications”, IEEE J. of Solid-State Circuits, Vol. 43, No.7, pp.1699-1710, July 2008.

[8]A. Tajalli, E. Vittoz, Y. Leblebici, “Ultra-Low Power Subthreshold MOS Current Mode Logic Circuits Using a Novel Load Device Concept”, Proc. 33rd European Solid State Circuits Conference (ESSCIRC),pp.304-307,Sept.2007.

[9]A. Tajalli, Y. Leblebici, “Extreme Low-Power Mixed Signal IC Design”,Springer,2010.

[10]A. Bazigos, M. Bucher, F. Krummenacher, J.-M. Sallese, A.-S. Roy, C. Enz, “EKV3 Compact MOSFET Model Documentation, Model Version 301.02“, Technical Report, Technical University of Crete, Greece,June2008.

[11]A. Bazigos, “Modeling of the MOS Transistor in High Frequencies”, Ph.D. Thesis, National Technical University of Athens, Greece, 2008.

[12]M.-A. Chalkiadaki, “Small and Large Signal Modeling of MOSFEs at High Frequencies”, Diploma Thesis, Technical University of Crete, Greece,2008.

[13]I. Chlis, M. Bucher, “PMOS Drain-Bulk Connected Loads for Subthreshold Source-Coupled Logic”, 18th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES 2011), pp.107-112,Gliwice, Poland, June 16-18, 2011.

[14]Sallese, J.-M.; Bucher, M.; Krummenacher, F.; Fazan, P. “Inversion charge linearization in MOSFET modeling and rigorous derivation of the EKV compact model”, Solid-State Electron., 2003, 47, 677-683

[15]Sallese, J.-M.; Bucher, M.; Lallement, C. “Improved analytical modeling of polysilicon depletion for CMOS circuit simulation”, Solid-State Electron., June 2000, 44(6), 905-912

[16]Cunha, A.I.A.; Gouveia-Filho, O.; Schneider, M.C.; Galup-Montoro, C. “A current-based model of the MOS transistor”, Proc. IEEE Int. Symp. On Circ. & Syst. (ISCAS ’97), June 1997, 3, 1608-1611.

[17]Christian C. Enz, Eric A. Vittoz, “Charge-based MOS transistor modelin, The EKV model for low-power and RF IC design”, WILEY.
[18]E. Vittoz, “Future of analog in the VLSI environment,” in IEEE International Symposium on Circuits and Systems, May 1990, pp. 1372–1375.
[19]P. R. Kinget, “Device mismatch and tradeoffs in the design of analog circuits,” IEEE Journal of Solid-State Circuits, vol. 40, no. 6, pp. 1212–1224, Jun. 2005.
[20]K. Bult, “Analog design in deep sub-micron CMOS,” in Proc. European Solid State Circuits Conference, Sep. 2000, pp. 11–17.
[21]Q. Huang, “Low voltage and low power aspects of data converter design,” in Proc. European Solid State Circuits Conference, Sep. 2000, pp. 29–35.
[22]B. Hosticka, W. Brockherde, D. Hammerschmidt, and R. Kokozinski, “Low-voltage CMOS analog circuits,” IEEE Transactions on Circuits and Systems I, vol. 42, pp.
[23]M. Steyaert, V. Peluso, J. Bastos, P. Kinget, and W. Sansen, “Custom analog low power design: The problem of low voltage and mismatch,” in Proc. IEEE Custom Integrated Circuits Conference, May 1997, pp. 285–292.
[24]W. Sansen, M. Steyaert, V. Peluso, and E. Peeters, “Toward sub 1V analog integrated circuits in submicron standard CMOS technologies,” in IEEE International Solid State Circuits Conference, Digest of Technical Papers, Feb. 1998, pp. 186–187.
[25]J. W. Fattaruso, “Low-voltage analog CMOS circuit techniques,” in International Symposium on VLSI Technology, Systems and Applications, Jun. 1999, pp. 286–289.
[26] T. Ohguro, H. Naruse, H. Sugaya, E.Morifuji, S. Nakamura, T. Yoshitomi, T.Morimoto, H. Kimijima, S. Momose, Y. Katsumata, and H. Iwai, “An 0.18 μm CMOS for mixed digital and analog applications with zero-volt-Vth epitaxial-channel MOSFETs,” IEEE Transactions on Electron Devices, vol. 46, no. 7, pp. 1378–1383, Jul. 1999.
[27] S. Bazarjani andW. Snelgrove, “Low voltage SC circuit design with low-Vt MOSFETs,” in IEEE International Symposium on Circuits and Systems, 1995, pp. 1021–1024.
[28] A. Guzinski, M. Bialko, and J. Matheau, “Body driven differential amplifier for application in continuous-time active-C filter,” in Proc. (IEEE) European Conference on Circuit Theory and Design (ECCTD’87), 1987, pp. 315–319.
[29] F. Dielacher, J. Houptmann, J. Resinger, R. Steiner, and H. Zojer, “A software programmable CMOS telephone circuit,” IEEE Journal of Solid-State Circuits, vol. 26, no. 7, pp. 1015–1026, Jul. 1991.
[30] B. Blalock, P. Allen, and G. Rincon-Mora, “Designing 1-V op-amps using standard digital CMOS technology,” IEEE Transactions on Circuits and Systems II, vol. 45, pp. 769– 780, Jul. 1998.
[31] S. Karthikeyan, S. Mortezapour, A. Tammineedi, and E. Lee, “Low-voltage analog circuit design based on biased inverting opamp configuration,” IEEE Transactions on Circuits and Systems II, vol. 47, no. 3, pp. 176–184, Mar. 2000.
[32] J. Huijsing and D. Linebarfer, “Low-voltage operational amplifier with rail-to-rail input and output ranges,” IEEE Journal of Solid-State Circuits, vol. SC-20, no. 6, Dec. 1985.
[33] R. Hogervorst, J. P. Tero, R. G. H. Eschauzier, and J. Huijsing, “A compact powerefficient 3V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries,” IEEE Journal of Solid-State Circuits, vol. 29, no. 12, pp. 1505–1513, Dec.1994.
[34] R. G. H. Eschauzier, L. Kerklaan, and J. Huijsing, “A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure,” IEEE Journal of Solid- State Circuits, vol. 27, no. 12, pp. 1709–1717, Dec. 1992.
[35]S. Pernici, G. Nicollini, and R. Castello, “A CMOS low-distortion fully differential power amplifier with double nested miller compensation,” IEEE Journal of Solid-State Circuits, vol. 28, no. 7, pp. 758–763, Jul. 1993.

[36]K. Lasanen, E. Raisanen-Ruotsalainen, and J. Kostamovaara, “A 1-V 5 µW CMOSopamp with bulk-driven input transistors,” in Proc. 43rd IEEE Midwest Symposium on Circuits and Systems, 2000, pp. 1038–1041.
[37]T. Lehmann andM. Cassia, “1-V power supply CMOS cascode amplifier,” IEEE Journal of Solid-State Circuits, vol. 36, pp. 1082–1086, Jul. 2001.
[38]T. Stockstad and H. Yoshizawa, “A 0.9-V 0.5-µA rail-to-rail CMOS operational amplifier,” IEEE Journal of Solid-State Circuits, vol. 37, no. 3, pp. 286–292, 2002.
[39] Y. Tsividis, Operation and Modeling of the MOS transistor, 2nd ed. Oxford University Press, New York, 1999.
[40]E. Vittoz and J. Fellrath, “CMOS analog integrated circuits based on weak inversion operation,” IEEE Journal of Solid-State Circuits, vol. 12, Jun. 1977.
[41]P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of AnalogIntegrated Circuits, 4th ed. John Wiley and Sons, New York, 2001.
[42]B. Razavi, Design of Analog CMOS Integrated Circuits. McGraw Hill, New York,1999.
[43]D. Johns and K. Martin, Analog Integrated Circuit Design. JohnWiley and Sons, New York, 1997.
[44] T. Kobayashi and T. Sakurai, “Self-adjusting threshold-voltage scheme (SATS) for lowvoltage high-speed operation,” in Proc. IEEE Custom Integrated Circuits Conference, May 1994, pp. 271–274.
[45] V. R. Kaenel, M. D. Pardoen, E. Dijkstra, and E. A. Vittoz, “Automatic adjustment of threshold and supply voltages for minimum power consumption in CMOS digital circuits,” in Proc. (IEEE) Symposium on Low Power Electronics, 1994, pp. 78–79.
[46] M.-J. Chen, J.-S. Ho, T.-H. Huang, C.-H. Yang, Y.-N. Jou, and T. Wu, “Back-gate forward bias method for low-voltage CMOS digital circuits,” IEEE Transactions on Electron Devices, vol. 43, no. 6, pp. 904–910, 1996.
[47] A. L. Coban, P. E. Allen, and X. Shi, “Low-voltage analog IC design in CMOS technology,” IEEE Transactions on Circuits and Systems I, vol. 42, no. 11, pp. 955–958, Nov. 1995
[48]Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, McGRAWL-HILL International Edition. 2001
[49]R.S. Muller and T.I. Kamins, “Device Electronics for Integrated Circuits”, Second Ed. New York: Wile, 1986
[50] Shouri Chatterjee, K.P. Pun, Nebojsa Stanic, Yannis Tsividis, Peter Kinget, “Analog Circuit Design Techniques at 0.5V”, Springer, December 2006
[51]K. N. Ratnakumar and J. D. Meindl, “Short-channel MOST threshold voltage model,” IEEE Journal of Solid-State Circuits, vol. SC-17, no. 5, pp. 937–948, Oct. 1982.
[52]S. Chatterjee, Y. Tsividis, and P. Kinget, “A 0.5-V bulk-input fully differential operational transconductance amplifier,” in Proc. European Solid State Circuits Conference, Sep. 2004, pp. 147–150.
[53] ——, “A 0.5 V filter with PLL-based tuning in 0.18 µm CMOS technology,” in IEEE International Solid State Circuits Conference, Digest of Technical Papers, 2005, pp. 506–507.
[54] K. P. Pun, S. Chatterjee, and P. Kinget, “A 0.5 V 74dB SNDR 25kHz CT __ modulator with return-to-openDAC,” in IEEE International Solid State Circuits Conference, Digest of Technical Papers, 2006, pp. 72–73.
[55] J. W. Tschanz, J. T. Kao, S. Narendra, R. Nair, D. Antoniadis, and A. P. Chandrakasan, “Adaptive body bias for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leakage,” IEEE Journal of Solid-State Circuits, vol. 37, no. 11, pp. 1396–1402, Nov. 2002.
[56]J. T. Kao, M. Miyazaki, and A. P. Chandrakasan, “A 175-mV multiply-accumulate unit using an adaptive supply voltage and body bias architecture,” IEEE Journal of Solid- State Circuits, vol. 37, no. 11, pp. 1545–1554, Nov. 2002.
[57]A. Baschirotto, F. Rezzi, and R. Castello, “Low-voltage balanced transconductor with high input common-mode rejection,” Electronics Letters, vol. 30, no. 20, pp. 1669–1671, Sep. 1994.

[58] F. Rezzi, A. Baschirotto, and R. Castello, “A 3 V 12-55 MHz BiCMOS pseudodifferential continuous-time filter,” IEEE Transactions on Circuits and Systems I, vol. 42, no. 11, pp. 896–903, Nov. 1995.
[59]Ka Nang Leung and Philip K. T. Mok,”Analysis of Multistage Amplifier-Frequency Compensation”, IEEE Trans. Circuits and Systems I: Fundamental Theory and Applications, vol. 48, no.9, September 2001.
[61] David M. Binkley, Tradeoffs and Optimization in Analog CMOS Design, John Wiley & Sons, 2008
[62] D. M. Binkley, “A methodology for transistor level analog CMOS design,” Conference tutorial with D. P. Foty, “MOSFET modeling and circuit design: re-establishing a lost connection,” 37th Annual Design Automation Conference (DAC), Los Angeles, June 2000.
[63] D. M. Binkley, “A methodology for analog CMOS design based on the EKV MOS model,” 2000 Fabless Semiconductor Association Design Modeling Workshop: SPICE Modeling, Santa Clara, Oct. 2000.
[6]4 D. M. Binkley, “A methodology for analog CMOS design based on the EKV MOS model,” Conference tutorial with D. P. Foty, “Re-connecting MOS modeling and circuit design: new methods for design quality,” 2001 IEEE 2nd International Symposium on Quality Electronic Design (ISQED), San Jose, Mar. 2001.
[65] D. M. Binkley, “A methodology for analog CMOS design based on the EKV MOS model,” Conference tutorial with D. P. Foty, “MOS modeling as a basis for design methodologies: new techniques for next-generation analog circuit design,” 2001 15th European Conference on Circuit Theory and Design (ECCTD), Helsinki, Aug. 2001.
[66] D. M. Binkley, “A methodology for analog CMOS design based on the EKV MOS model,” Conference tutorial
with D. P. Foty, “MOS modeling as a basis for design methodologies: new techniques for modern analog design,” 2002 IEEE International Symposium on Circuits and Systems (ISCAS), Scottsdale, May 2002.
[67] D. M. Binkley, M. Bucher, and D. Kazazis, “Modern analog CMOS design from weak through strong inversion,” Proceedings of the European Conference on Circuit Theory and Design (ECCTD), pp. I-8–I-13, Krakow, Aug. 2003.
[68] D. M. Binkley, C. E. Hopper, S. D. Tucker, B. C. Moss, J. M. Rochelle, and D. P. Foty, “A CAD methodology for optimizing transistor current and sizing in analog CMOS design,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 22, pp. 225–237, Feb. 2003.
[69] D. M. Binkley, B. J. Blalock, and J. M. Rochelle, “Optimizing drain current, inversion level, and channel length in analog CMOS design,” Analog Integrated Circuits and Signal Processing, vol. 47, pp. 137–163, May 2006.
[70] Athanasios Dimakos, Matthias Bucher, Rupendra Sharma, Ilias Chlis, “Ultra-Low Voltage Drain-Bulk Connected MOS Transistors in Weak and Moderate Inversion”, ICECS 2012
[71] G. Ferri and W. Sansen, “A 1.3V op-amp in standard 0.7μm CMOS with constant gm and rail-to-rail input and output stages,” in IEEE International Solid State Circuits Conference, Digest of Technical Papers, 1996, pp. 382–383, 478.
[72] V. Peluso, P. Vancorenland, A. M. Marques, M. Steyaert, and W. Sansen, “A 900-mV low-power ΔΣ A/D converter with 77-dB dynamic range,” IEEE Journal of Solid-State Circuits, vol. 33, no. 12, pp. 1887–1897, Dec. 1998.
[73] Gewrgios Raikos, “Low Voltage Bulk-Driven Analog Circuits”, PhD Thesis, Patra, Greece, November 2011

Ultra-Low Voltage Drain-Bulk Connected MOS Transistors in Weak and Moderate Inversion

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***Abstract*—This paper aims to demonstrate the basic characteristics of NMOS and PMOS drain-bulk connected transistors for ultra-low voltage applications. On-wafer measurements as well as TCAD simulations have been performed for 180nm and 45nm technology nodes. The charge-based explicit MOS transistor model is used to provide an analysis in weak-moderate inversion, showing that output characteristics are well-controlled and dominated by the substrate effect. Furthermore, simulations with the EKV3 MOSFET compact model following a parameter extraction are perfomred, with the simulation results being very close to real measurements and TCAD simulated data.**

I. INTRODUCTION

The MOS transistor, with its tremendous improvements in downscaling and hence in functionality and speed performance, constitutes the main driving force of modern consumer electronics. The regions of weak and moderate inversion that, with a few brilliant exceptions, were previously ignored or even unknown, are now becoming the very desired ones for MOS transistor. Using the inversion coefficient permits design in all regions of MOS operation, including moderate inversion. Moderate inversion [1], a transitional region spanning nearly two decades of drain current between weak and strong inversion, as described in Section II below, has become increasingly important in modern design. This is because it offers a compromise of high transconductance (high transconductance efficiency), low drain-source saturation voltage, minimal velocity saturation degradation of transconductance, and moderate bandwidth necessary for power-efficient, low-voltage design.

Several ultra-low voltage design techniques, such as forward biasing of the body-source junction, have been proposed [2] for low voltage digital circuits and have been applied to lower the threshold voltage V_T of the transistors. In the context of low voltage operation, such as 0.5 V or below, the risk of forward biasing of the junctions is minimized since parasitic bipolar devices cannot be activated even when the full power supply is used as forward bias.

II. CHARGE-BASED MOS TRANSISTOR MODEL

The MOS transistor drain current in the context of the EKV model is expressed as [3],

$$I_D = I_F - I_R = I_{SPEC} \cdot \left(i_f - i_r \right) \tag{1}$$

where the specific current is the normalization current given by,

$$I_{SPEC} = 2 \cdot n \cdot \beta \cdot U_T^2 \tag{2}$$

where $\beta = \mu\, C'_{ox}\, W/L$ is the gain factor, and W and L the device width and length respectively. i_f and i_r are the symmetric forward and reverse normalized currents. Each of these currents is related to inversion charge densities q_s and q_d at source and drain [4],

$$i_{f(r)} = q_{s(d)}^2 + q_{s(d)} \tag{3}$$

which in turn relate to the terminal voltages [4],

$$v_p - v_{s(d)} = 2 \cdot q_{s(d)} + \ln(q_{s(d)}) \,. \tag{4}$$

Terminal voltages are normalized to the thermodynamic potential $U_T = kT/q$,

$$v_p = V_P / U_T \qquad v_{s(d)} = V_{S(D)} / U_T \tag{5}$$

where the pinch-off voltage V_P and slope factor n are function of the gate voltage [3],

$$V_P \cong \frac{V_G - V_{TO}}{n} \qquad n \equiv \frac{dV_G}{dV_P} = 1 + \frac{\gamma}{2 \cdot \sqrt{V_P + \phi}} \tag{6}$$

In the above, V_{TO} is the threshold voltage, γ the substrate factor and Φ amounts to twice the Fermi potential.

The inversion coefficient (*IC*) in MOS transistors offers a convenient way to relate the drain current to fundamental physics of the device,

$$IC = I_D / I_{SPEC} \tag{7}$$

which, usually, implies saturation operation. Levels of $IC > 10$ correspond to operation in strong inversion, $0.1 < IC < 10$ moderate inversion and $IC < 0.1$ weak inversion [3][5][6].

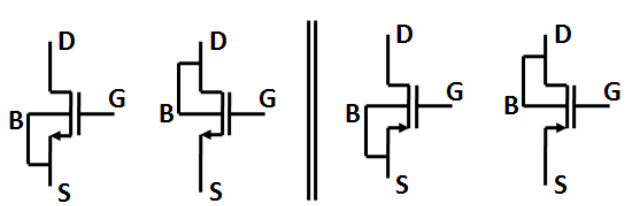

Figure 1: NMOS (left) and PMOS (right) transistors, with their local substrate (or well) connected to either source or drain.

III. DRAIN-BULK CONNECTED MOS TRANSISTORS

As shown in Fig. 1, either NMOS or PMOS transistors may be used with the somewhat unusual drain-bulk connection, instead of the conventional source-bulk connection (where 'bulk' may stand for the local substrate or well). For the NMOS transistors, a triple-well technology would be presupposed.

The drain current of the NMOS transistors biased in weak inversion is given by the EKV model [7] – [9] as:

$$I_{DS} = I_{SPEC} \cdot e^{\frac{V_{GB}-V_{TO}}{nU_T}} \cdot \left[e^{\frac{V_{SB}}{U_T}} - e^{\frac{V_{DB}}{U_T}} \right] \tag{8}$$

For the conventional device where V_{BS}=0, the relation (8) becomes:

$$I_{DS} = I_{SPEC} \cdot e^{\frac{V_{GB}-V_{TO}}{nU_T}} \cdot \left[1 - e^{\frac{V_{DB}}{U_T}} \right]$$

$$\Leftrightarrow I_{DS} = I_{SPEC} \cdot e^{\frac{V_{GS}-V_{TO}}{nU_T}} \cdot \left[1 - e^{\frac{V_{DS}}{U_T}} \right] \tag{9}$$

On the contrary, for the drain-bulk connected device, where $V_{DB} = 0\ V$, the relation (8) becomes:

$$I_{DS} = I_{SPEC} \cdot e^{\frac{V_{GB}-V_{TO}}{nU_T}} \cdot \left[e^{\frac{V_{SB}}{U_T}} - 1 \right]$$

$$\Leftrightarrow I_{DS} = I_{SPEC} \cdot e^{\frac{V_{GS}-V_{TO}}{nU_T}} \cdot \left[e^{\frac{-V_{DS}}{U_T} \cdot \frac{n-1}{n}} - e^{\frac{V_{DS}}{nU_T}} \right] \tag{10}$$

The output small signal conductance g_{SD} and resistance r_{SD} are defined as:

$$g_{DS} = \frac{\partial I_{DS}}{\partial V_{DS}},\ r_{DS} = \frac{1}{g_{DS}} = \left[\frac{\partial I_{DS}}{\partial V_{DS}} \right]^{-1}$$

Assuming long-channel behavior, i.e. neglecting drain voltage dependence of the threshold voltage, slope factor and I_{SPEC}, $\delta V_{TO}/\delta V_{SD}$=0, $\delta n/\delta V_{SD}$=0, $\delta I_{SPEC}/\delta V_{SD}$=0, we have for the conventional device:

$$g_{DS,S=B} = \frac{I_{SPEC}}{U_T} e^{\frac{V_{GS}-V_{TO}}{nU_T}} \cdot \left[e^{\frac{V_{DS}}{U_T}} \right] \tag{11}$$

whereas for the drain-bulk connected device,

$$g_{DS,D=B} = \frac{I_{SPEC}}{U_T} e^{\frac{V_{GS}-V_{TO}}{nU_T}} \cdot \left[\frac{n-1}{n} \cdot e^{\frac{-V_{DS}}{U_T} \cdot \frac{n-1}{n}} + \frac{1}{n} \cdot e^{\frac{V_{DS}}{nU_T}} \right] \tag{12}$$

Measurements have been made on a 180 nm wafer through IC-CAP, using a Cascade Microtech SUMMIT 10600 prober and an HP4145A Semiconductor Parameter Analyzer, in order to demonstrate the advantages of using the drain-bulk connected PMOS transistors. The drain-bulk connected PMOS have been measured with the source-drain voltage V_{SD} ranging from 0 V to 280 mV with a step size of 10 mV, and the source-gate voltage V_{SG} ranging from 250 mV to 350 mV with a step size of 25 mV.

In addition to above measurements, simulations have been made through with the ATLAS TCAD tool for conventional and drain-bulk connected NMOS and PMOS transistors of lengths 10 μm and 180 nm and of width 1 μm. All the TCAD simulations assume a uniformly doped channel. Simulations with the analytical charge-based EKV model of Eq. (4) on simulated TCAD results have been made, after extracting different sets of parameters for V_{T0}, γ and Φ, with the charge-based model simulation results being very close to TCAD simulated data. Furthermore, TCAD data have been imported into IC-CAP, where simulations with the EKV model version 301.02 [10] have been performed, after extracting the parameters of the model for the 180nm technology, with the simulation results being very close to TCAD simulated data. The parameter extraction was based on the procedure proposed by [11], [12].

IV. RESULTS AND DISCUSSION

The measured and simulated I_{SD} vs. V_{SD} and g_{SD} vs. V_{SD} characteristics of the drain-bulk connected NMOS devices are shown in the left side of Fig. 2. The same characteristics of the drain-bulk PMOS are depicted in the right side of Fig. 2. In the first case, we have TCAD data versus the EKV301.02 simulations, whereas, in the second case, we have real measurements versus the analytical charge-based model of Eq. (4). The NMOS devices are biased with a gate voltage ranging from 100 mV to 600 mV with a step of 25 mV. On the other hand, the PMOS devices, measured on the 180nm wafer, are biased with a gate voltage ranging from 250mV to 350mV with a step size of 25mV.

The Fig. 2 illustrates that for both NMOS and PMOS transistors, the I_{DS} vs. V_{DS} behavior and thus the output conductance g_{DS}, are dominated by the substrate effect. Drain Induced Barrier Lowering (DIBL) effect which is the usually dominant effect for output conductance in short transistors in weak inversion, is actually dominated by the substrate effect.

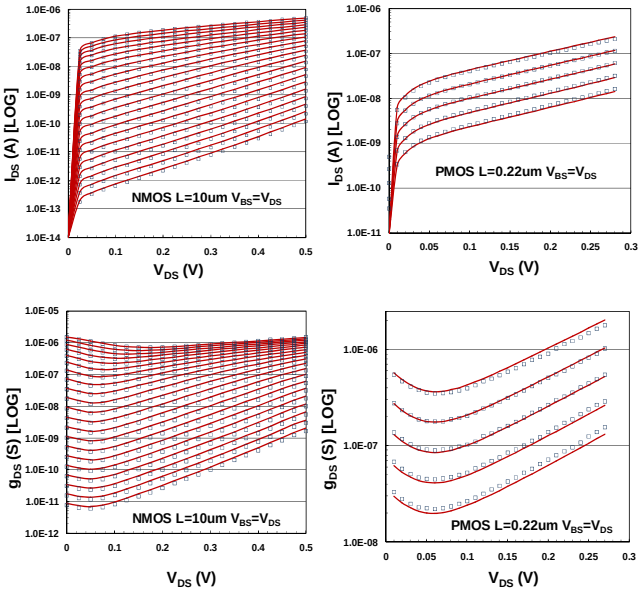

Fig. 2: Drain-bulk connected NMOS (left) and PMOS (right) transistor, with respective output characteristics, W/L=1µm/10µm (left) and W/L=10µm/0.22µm. I_{DS}, g_{DS} vs. V_{DS} are shown for various values of V_{GS} (markers: TCAD simulation data(left), measurements (right), lines: EKV3 model (left), analytical charge-based model (right)).

We define Early voltage V_A as a quantity equal to the ratio of the drain current I_{DS} divided by the output conductance g_{DS}. We note from (10) and (12) that for the saturated drain-bulk connected NMOS transistor,

$$V_A = \frac{I_{DS}}{g_{DS,D=B}} \cong U_T \cdot \frac{n}{n-1} \qquad (13)$$

which means that V_A in this operating region is well-known, since n does not strongly depend on bias, and is not a strong function of channel length. The output resistance is given by the reverse of the output conductance, and therefore, we have, $r_{DS} = V_A/I_{DS}$. On the other hand, the intrinsic gain of the transistor is defined as $A_V = g_m/g_{DS}$,

$$A_V = \frac{g_m}{g_{DS}} \cong \frac{V_A}{U_T} \cdot \frac{g_m U_T}{I_D} = \frac{G(IC)}{n-1} \qquad (14)$$

where $G(IC)$ is the well-known normalized transconductance [4] – [6]. Fig. 3 shows the V_A, n and A_V vs. V_{DS} characteristics for the drain-bulk connected NMOS and PMOS devices. In the left case, we have the TCAD vs. EKV301.02 simulations, whereas in the right case, we have the comparisons between real measurements and analytical charge-based model of Eq. (4). In the case of drain-bulk connected NMOS configuration, the devices are biased with a gate voltage ranging from 100 mV to 600 mV with a step of 25 mV. On the other hand, the PMOS devices, measured on the 180 nm wafer, are biased with a gate voltage ranging from 250 mV to 350 mV with a step size of 25 mV.

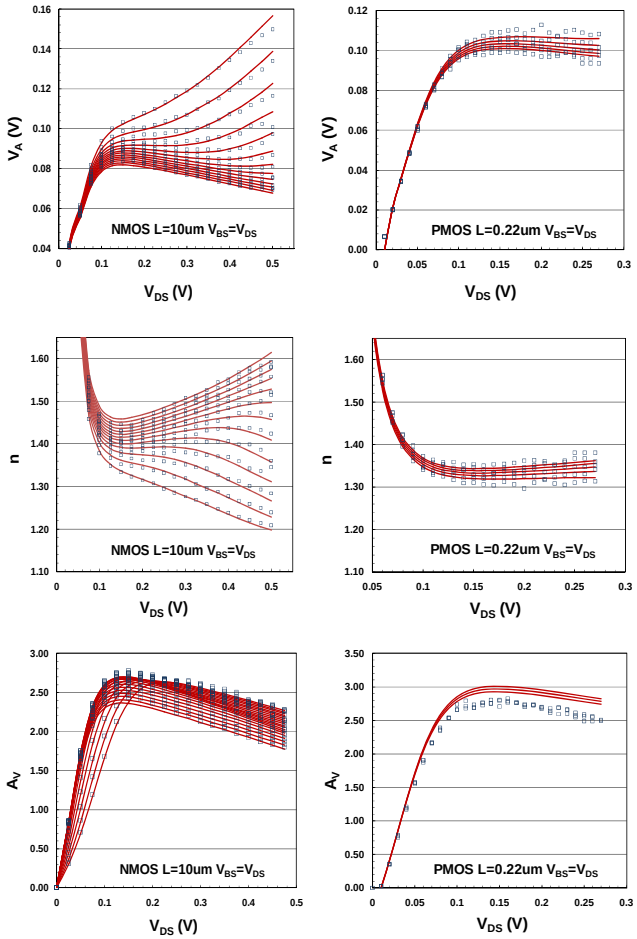

Fig. 3: Early Voltage V_A, Slope Factor n extracted from Equation (13) and Intrinsic Gain A_V of drain-bulk connected NMOS (left) and PMOS (right) devices (markers: TCAD/measured data, lines: EKV3/analytical model).

The behavior of V_A vs. V_{DS} for drain-bulk connected NMOS and PMOS transistors, for W/L = 1 µm / 10 µm and W/L = 10 µm / 0.22 µm is given in the left and right side of Fig. 3, respectively.

In the case of the V_A characteristics, the same figure shows that for any geometry we use, the Early voltage in nearly constant and independent of V_{GS} both for NMOS (TCAD vs. EKV301.02) and PMOS (real measurements vs. analytical charge based model).

The same result arrives for the case of the slope factor n, which is extracted from V_A using Eq. (13) in weak inversion and saturation region. Additionally, Fig. 3 depicts the behavior of the intrinsic gain g_m/g_{DS} vs. $V_{DS,}$ which is independent of the V_{GS} bias point and begins to remain almost constant for a low V_{DS} voltage nearly equal to 100 mV.

As again seen in Fig. 3, the drain-bulk connected topology is characterized in weak and moderate inversion saturation by a V_A almost independent of V_{DS}. The Early voltage is also independent of inversion coefficient IC and channel length L as reported in [13] and consequently, V_A is approximately constant and independent of bias voltages and channel length.

Additionally to the above, TCAD simulations have been made on a technology of 45nm. The simulated data have been imported into IC-CAP, where simulations with the EKV model version 301.02 have been performed, after extracting the parameters of the model for the 45nm technology used. Fig. 5 depicts the simulated drain-bulk connected NMOS transistor, with respective output characteristics of I_{DS}, g_{DS} vs. V_{DS} for two geometries, W/L = 1 µm / 1 µm (left side) and W/L = 1 µm / 45 nm (right side) and confirm the aforementioned I_{DS} vs. V_{DS} and g_{DS} vs. V_{DS} behavior similar to the 180 nm technology node.

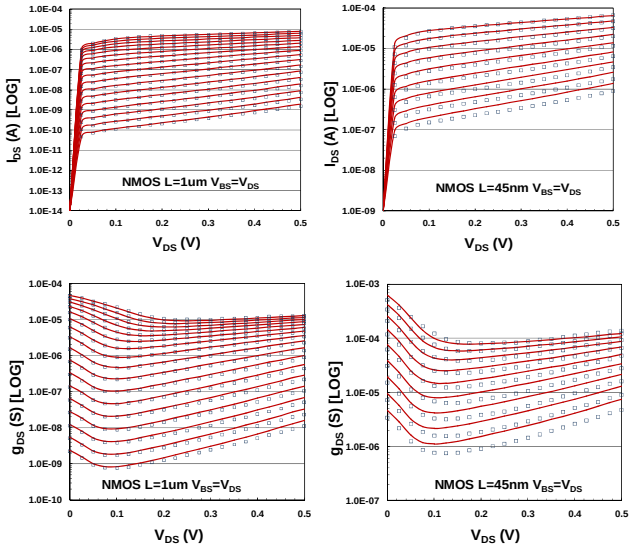

Figure 5: Drain-bulk connected NMOS transistor, with respective output characteristics, W/L=1µm/1µm (left) and , W/L=1µm/45nm. I_{DS}, g_{DS} vs. V_{DS} are shown for various values of V_{GS} (markers: TCAD simulation data, lines: EKV3 model).

V. Conclusion

This paper has shown the invariability of Early voltage and intrinsic gain of drain-bulk connected NMOS and PMOS transistors operated in weak-moderate inversion. Both quantities are governed essentially by the substrate effect – or slope factor n – and hence have a very low dependence on short-channel and biasing effects, once the V_{DS} value attains voltages as low as about 4 U_T. This can be easily exploited in applications where insensitivity of gain or Early voltage w.r.t. bias and channel length is favored.

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References

[1] Y. Tsividis, “Moderate inversion in MOS devices,” *Solid-State Electronics*,vol.25,pp.1099–1104,Nov.1982.

[2] Shouri Chatterjee, K.P.Pun, Nebojsa Stanic, Yannis Tsividis, Peter Kinget, “Analog Circuit Design Techniques at 0.5V”, Springer.

[3] C. Enz, F. Krummenacher, E. Vittoz, “An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications”, Analog Integrated Cicruits and Signal Processing, Vol. 8, pp. 83-114, 1995. J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp. 68–73.

[4] M. Bucher, “Analytical MOS Transistor Modelling for Analog Circuit Simulation”, *Ph. D. Thesis N° 2114 (1999)*, Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland, 2000.

[5] D. M. Binkley, C. E. Hopper, S. D. Tucker, B. C. Moss, J. M. Rochelle, D. P. Foty, “A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design”, *IEEE Trans. Computer-Aided Design of Int. Circ. & Syst.,* pp. 225-237, Vol. 22, N° 2, February 2003. R. Nicole, “Title of paper with only first word capitalized,” J. Name Stand. Abbrev., in press.

[6] M.Bucher, D. Kazasis, F. Krummenacher, D. Binkley, D. Foty, Y. Papananos, “Analysis of Transconductances at All Levels of Inversion in Deep Submicron CMOS”, 9th *IEEE Conf. on Electronics, Circ & Syst. (ICECS 2002)*, Vol. III, pp. 1183-1186, Dubrovnik, Croatia, September 15-18, 2002.

[7] A. Tajalli, E. Brauer, Y. Leblebici, E. Vittoz, “Subthreshold Source-Coupled Logic Circuits for Ultra-Low-Power Applications”, IEEE J. of Solid-State Circuits, Vol. 43, No.7, pp.1699-1710, July 2008.

[8] A. Tajalli, E. Vittoz, Y. Leblebici, “Ultra-Low Power Subthreshold MOS Current Mode Logic Circuits Using a Novel Load Device Concept”, Proc. 33rd European Solid State Circuits Conference (ESSCIRC),pp.304-307,Sept.2007.

[9] A. Tajalli, Y. Leblebici, “Extreme Low-Power Mixed Signal IC Design”,Springer,2010.

[10] A. Bazigos, M. Bucher, F. Krummenacher, J.-M. Sallese, A.-S. Roy, C. Enz, “EKV3 Compact MOSFET Model Documentation, Model Version 301.02“, Technical Report, Technical University of Crete, Greece,June2008.

[11] A. Bazigos, “Modeling of the MOS Transistor in High Frequencies”, Ph.D. Thesis, National Technical University of Athens, Greece, 2008.

[12] M.-A. Chalkiadaki, “Small and Large Signal Modeling of MOSFEs at High Frequencies”, Diploma Thesis, Technical University of Crete, Greece,2008.

[13] I. Chlis, M. Bucher, “PMOS Drain-Bulk Connected Loads for Subthreshold Source-Coupled Logic”, 18th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES 2011), pp.107-112,Gliwice, Poland, June 16-18, 2011.