Statistical Charge-Based Modeling of 1/f Noise in Standard and High-Voltage MOS Transistors

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Abstract

Nowadays, analog and RFIC applications are exclusively been designed by CMOS technology because of many advantages such as the high level of integration, the low cost and low consumption that it offers. The achievement of integration on a single chip (SoC) both for analog and digital systems triggered a great boost in the domination of CMOS especially with the downscaling of MOSFET dimensions. Apart from conventional CMOS, HV-MOS process is also widely used in specific applications such as automotive industry, scientific and medical applications and consumer electronics. The latter kind of power applications created the need of the usage of power devices such as HV-MOSFETs and nowadays in circuit design, high-voltage parts are integrated together with low-voltage modules. Nevertheless, the performance of both CMOS and HV-MOS design can be limited by low frequency noise (LFN) which becomes really significant in state of the art technologies because it is inversely proportional to channel area. Despite the fact that is dominant for lower frequencies below the corner frequency, it can prove to be a significant hurdle even for high-frequency (RF) applications due to its up conversion in phase noise in VCO design for example. Furthermore, in advanced ultradeep nano-scaled transistors, corner frequencies of several MHz can be noticed and thus analog designers can not ignore LFN. As far as HV-MOSFETs are concerned, circuits such as oscillators, analog baseband and bandgap reference can be limited by LFN. In general, it affects any kind of MOS device but it can also be used as an effective way to evaluate the quality and reliability of a MOS transistor.

LFN is distinguished into two kinds; random telegraph signal (RTS) noise and flicker or 1/f noise. RTS noise is created by the generation-recombination process or trapping/detrapping mechanism at the silicon oxide interface. Each such trap can create an RTS in time domain or a Lorentzian-like spectrum in frequency domain. RTS noise prevails in smaller area transistors where the traps are only few. In larger devices, on the other hand, the number of traps is quite large and the superposition of Lorentzian spectra can lead to 1/f behavior and thus it creates 1/f noise. This connection of RTS with 1/f noise is fully described by carrier number fluctuation effect which constitutes one of the main 1/f noise generators in MOS devices. Two other phenomena create 1/f noise and these are mobility fluctuation and series resistance effects. It is experimentally shown that each of these effects is dominant under different operating conditions.

Mean value and variability of LFN are both area- and bias-dependent. Variability increases as device dimensions shrink bearing similarity with the behavior of mean value noise. The same trend can be observed in the bias-dependence of 1/f noise variability. Carrier number fluctuation effect has been proven to increase normalized flicker noise $WL * S_{ID}/I_D^2$ at $1\,Hz$, in moderate and strong inversion and the same is

confirmed for its variability while mobility fluctuation effect is considered responsible for the increase of normalized 1/f noise in weak inversion and its variability also increases there. This bias-dependence of flicker noise variability is of great concern especially since the downscaling of advanced nanotechnologies has led to circuit operation in moderate or even in weak inversion.

Flicker noise in HV-MOSFETs is expected to be generated by the same causes as in conventional MOSFETs since the same operating principles rule both kind of these MOS devices due to the existence of the oxide interface. Thus, it is experimentally shown that in the LV or channel part of the HV-MOSFET, carrier number fluctuation, mobility fluctuation and series resistance effects are the main contributors to 1/f noise. This was already known and the main question was if any similar effect is observed in drift region. Our analysis showed that the extension of gate oxide in the surface of drift region, causes a similar carrier number fluctuation effect which can give rise to 1/f noise. This noise becomes significant under linear region and strong inversion regime of long channel transistors since only under these conditions it reaches a similar level as the noise generated in the channel.

Because of the significant impact of LFN in advanced analog and RF circuit design, the usage of correct, physics-based, compact models both for mean value and statistical behavior of LFN has become essential for noise simulation. Within the context of this Thesis, a charge-based compact model both for the mean-value and the variability of 1/f noise was implemented, validated at an experimental $180\,nm$ CMOS process with measurements in our lab and appended in the charge-based EKV3 compact MOSFET model. The mean value model was also tested at an $90\,nm$ CMOS process provided by the industry while the variability model was also tested at an $140\,nm$ CMOS process. The analytical, charge-based approach for 1/f noise statistics is directly related to the physical effects that generate 1/f noise in MOS devices and this is something proposed for the first time. A similar charge-based 1/f noise compact model is proposed for the first time for HV-MOSFETs after exploring and locating new noise sources that arise from the drift region of the device. An expression for the variability of 1/f noise arising from the channel of HV-MOSFETs is also proposed but is not validated since sufficient statistical data were not available. The mean value model was validated with data from an $350\,nm$ HV-MOS process provided by ams AG. Measurements were performed by us in a new 1/f noise measurement set-up specialized for HV-MOSFETs and provided by AdMOS. Characterization of 1/f noise data in all the above cases confirms the existing theory while the developed 1/f noise models both for CMOS and HV-MOS technologies give qualitively good results over a wide range of area and operating conditions.

Περίληψη

Στις μέρες μας, οι εφαρμογές αναλογικών και ολοκληρωμένων κυκλωμάτων πολύ υψηλών συχνοτήτων (RFIC) σχεδιάζονται αποκλειστικά με τεχνολογία CMOS εξαιτίας των πολλών πλεονεκτημάτων που προσφέρει όπως το υψηλό επίπεδο ολοκλήρωσης, το χαμηλό κόστος και η χαμηλή κατανάλωση. Η επίτευξη της ολοκλήρωσης σε ένα μόνο chip (SoC) τόσο αναλογικών όσο και ψηφιακών συστημάτων, πυροδότησε μία σπουδαία ώϑηση για την κυριαρχία των CMOS τεχνολογιών ειδικότερα με την μειώση των διαστάσεων των MOSFET διατάξεων. Εκτός από τη συμβατική CMOS τεχνολογία, η HV-MOS τεχνολογία χρησιμοποιείται επίσης ευρέως σε συγκεκριμένες εφαρμογές όπως στη βιομηχανία αυτοκινήτων, σε επιστημονικές και ιατρικές εφαρμογές και σε ηλεκτρονικά είδη ευρείας κατανάλωσης. Αυτού του είδους οι εφαρμογές ισχύος δημιούργησαν την ανάγκη της χρήσης διατάξεων ισχύος όπως τα HV-MOSFETs και έτσι στις μέρες μας στη σχεδίαση κυκλωμάτων, τα τμήματα υψηλής τάσης ενός κυκλώματος ολοκληρώνονται μαζί με αυτά χαμηλής τάσης. Παρόλ'αυτά, η απόδοση τόσο της CMOS όσο και της HVMOS σχεδίασης μπορεί να περιοριστεί από το ϑόρυβο χαμηλών συχνοτήτων (LFN) που γίνεται ιδιαίτερα σημαντικός σε σύγχρονες τεχνολογίες μιας και είναι αντιστρόφως ανάλογως με το μήκος του καναλιού. Παρά το γεγονός ότι είναι κυρίαρχος για χαμηλότερες συχνότητες κάτω από την γωνιακή συχνότητα, μπορεί να αποδειχϑεί ότι είναι ένα σημαντικό εμπόδιο ακόμα και για εφαρμογές υψηλής συχνότητας (RF) εξαιτίας της μετατροπής του σε ϑόρυβο φάσης στη σχεδίαση ταλαντωτών τάσης (VCO) για παράδειγμα. Επιπλέον, σε προηγμένα, πολύ μικρού μήκους καναλιού, τρανζίστορ, μπορούν να παρατηρηϑούν γωνιακές συχνότητες αρκετών *MHz* και κατά συνέπεια οι σχεδιαστές αναλογικών κυκλωμάτων δεν μπορούν να αγνοήσουν τον LFN. Όσον αφορά στα HV-MOSFETs, κυκλώματα όπως ταλαντωτές, αναλογικά κυκλώματα μέσης ζώνης και κυκλώματα αναφοράς bandgap μπορούν να επηρεαστούν απο τον LFN. Γενικότερα, επηρεάζει κάϑε είδος MOS διάταξης αλλά επίσης μπορεί να χρησιμοποιηϑεί ως ένας αποτελεσματικός τρόπος για να αξιολογηϑεί η ποιότητα και η αξιοπιστία ενός MOS τρανζίστορ.

Ο ϑόρυβος χαμηλής συχνότητας διαχωρίζεται σε δύο είδη; σε ϑόρυβο τυχαίων τηλεγραφικών σημάτων (RTS) και σε 1/f ή flicker ϑόρυβο. Ο RTS ϑόρυβος προκαλείται από την διεργασία δημιουργίας-ανασυνδιασμού ή μηχανισμό παγίδευσης/ελευϑέρωσης στη διεπαφή του οξιδίου του πυρητίου. Κάϑε τέτοια παγίδα μπορεί να δημιουργήσει ένα RTS σήμα στο πεδίο του χρόνου ή ένα Lorentzian φάσμα στο πεδίο της συχνότητας. Ο RTS ϑόρυβος επικρατεί σε τρανζίστορ μικρότερης επιφάνειας όπου ο αριϑμός των παγίδων είναι αρκετά μικρός. Από την άλλη μεριά, σε διατάξεις μεγαλύτερης επιφάνειας, ο αριϑμός των παγίδων είναι αρκετά μεγάλος και η υπέρϑεση των Lorentzian φασμάτων μπορεί να οδηγήσει σε 1/f συμπεριφορά και έτσι να δημιουργήσει 1/f ϑόρυβο. Αυτή η σύνδεση μεταξύ RTS και 1/f ϑορύβου περιγράφεται πλήρως από το φαινόμενο διακύμανσης του αριϑμού των φορέων το οποίο αποτελεί μία απο τις βασικές πηγές δημιουργίας 1/f ϑορύβου σε MOS διατάξεις. Δύο άλλα φαινόμενα δημιουργούν 1/f ϑόρυβο και αυτά είναι το φαινόμενο της διακύμανσης της κινητικότητας και το φαινόμενο της σειριακής αντίστασης.

Η μέση τιμή και η μεταβλητότητα του ϑορύβου χαμηλών συχνοτήτων είναι εξαρτώμενες τόσο από την επιφάνεια όσο και από τις συνϑήκες πόλωσης του τρανζίστορ. Η μεταβλητότητα αυξάνει όσο οι διαστάσεις της διάταξης μειώνον-

ται ενώ παρόμοια συμπεριφορά παρουσιάζει και η μέση τιμή του θορύβου. Η ίδια τάση μπορεί να παρατηρηθεί όσον αφορά την εξάρτηση της μεταβλητότητας του 1/f θορύβου από την πόλωση. Το φαινόμενο διακύμανσης του αριθμού των φορέων έχει αποδειχθεί ότι αυξάνει τον κανονικοποιημένο 1/f θόρυβο $WL * S_{ID}/I_D^2$ στο $1\,Hz$, στη μεσαία και ισχυρή αντιστροφή ενώ το ίδιο επιβεβαιώνεται και για την μεταβλητότητα του ενώ το φαινόμενο της διακύμανσης της κινητικότητας θεωρείται υπεύθυνο για την αύξηση του κανονικοποιημένου 1/f θορύβου στην ασθενή αντιστροφή και η μεταβλητότητα του επίσης αυξάνει εκεί. Αυτή η εξάρτηση από την πόλωση του flicker θορύβου είναι ιδιαίτερα σημαντική ειδικά αφού η μείωση του μήκους καναλιού σε προηγμένες νανοτεχνολογίες έχει οδηγήσει τη λειτουργία των κυκλωμάτων σε μέτρια ή ακόμα και σε ασθενή αντιστροφή.

Ο flicker θόρυβος στα HV-MOSFETs αναμένεται να δημιουργείται από τις ίδιες αιτίες όπως και στα συμβατικά MOSFETs μιας και οι ίδιες αρχές λειτουργίας διέπουν και τα δύο είδη αυτών των MOS διατάξεων εξαιτίας της ύπαρξης της διεπαφής οξιδίου. Έτσι, δείχνεται πειραματικά ότι στο LV τμήμα ή τμήμα καναλιού του HV-MOSFET, τα φαινόμενα διακύμανσης του αριθμού των φορέων, διακύμανσης της κινητικότητας και της σειριακής αντίστασης είναι οι βασικόι συνεισφέροντες του 1/f θορύβου. Αυτό ήταν ήδη γνωστό και το βασικό ερώτημα ήταν αν κάποιο παρόμοιο φαινόμενο παρατηρείται στην drift περιοχή. Η ανάλυση μας έδειξε ότι η επέκταση του οξιδίου της πύλης στην επιφάνεια της drift περιοχής, προκαλεί ένα παρόμοιο φαινόμενο διακύμανσης του αριθμού των φορέων που μπορεί να προκαλέσει 1/f θόρυβο. Αυτός ο θόρυβος γίνεται σημαντικός σε γραμμική περιοχή λειτουργίας και ισχυρή αντιστροφή σε τρανζίστορ μεγάλου μήκους καναλιού μιας και μόνο υπό αυτές τις συνθήκες γίνεται συγκρίσιμος με τον θόρυβο που προέρχεται από το κανάλι.

Εξαιτίας της σημαντικής επίδρασης του LFN σε προηγμένη σχεδίαση αναλογικών και RF κυκλωμάτων, η χρήση σωστών, βασισμένων στη φυσική, συμπαγών μοντέλων τόσο για τη μέση τιμή όσο και για την στατιστική συμπεριφιρά του LFN έχει γίνει αναγκαία για τις ανάγκες προσομείωσης θορύβου. Στα πλαίσια αυτής της διατριβής, ένα συμπαγές, βασισμένο στα φορτία, μοντέλο τόσο για τη μέση τιμή όσο και για την μεταβλητότητα του 1/f θορύβου αναπτύχθηκε, επικυρώθηκε για μια πειραματική $180\,nm$ CMOS τεχνολογία με μετρήσεις στο εργαστήριο μας και προσαρτήθηκε στο EKV3 συμπαγές μοντέλο για MOSFET. Το μοντέλο μέσης τιμής δοκιμάστηκε επίσης σε μία $90\,nm$ CMOS τεχνολογία που μας έγινε διαθέσιμη απο τη βιομηχανία ενω το μοντέλο μεταβλητότητας δοκιμάστηκε επίσης σε μία $140\,nm$ CMOS τεχνολογία. Η αναλυτική, βασισμένη στα φορτία, προσέγγιση της στατιστικής του 1/f θορύβου συνδέεται άμεσα με τα φυσικά φαινόμενα που δημιουργούν 1/f θόρυβο σε MOS διατάξεις και αυτό είναι κάτι που προτείνεται για πρώτη φορά. Ένα παρόμοιο, βασισμένο στα φορτία, συμπαγές μοντέλο 1/f θορύβου προτείνεται για πρώτη φορά για τα HV-MOSFETs μετά από τη διερεύνηση και τον εντοπισμό νέων πηγών θορύβου που προκύπτουν από την περιοχή drift της διάταξης. Μία έκφραση για τη μεταβλητότητα του 1/f θορύβου, που προέρχεται από το κανάλι των HV-MOSFETs, επίσης προτείνεται αλλά δεν ήταν δυνατό να επικυρωθεί λόγω έλλειψης επαρκούς αριθμού δεδομένων. Το μοντέλο μέσης τιμής επικυρώθηκε για δεδομένα από μία 350 *nm* HV-MOS τεχνολογία που μας παρείχε η εταιρία ams AG. Οι μετρήσεις πραγματοποιήθηκαν από εμάς με ένα καινούριο σύστημα μετρήσεων 1/f θορύβου εξειδικευμένο σε HV-MOSFETS που μας παρείχε η εταιρία AdMOS. Ο χαρακτηρισμός των δεδομένων 1/f θορύβου σε όλες τις παραπάνω περιπτώσεις επιβεβαιώνει την υπάρχουσα θεωρία ενώ τα μοντέλα 1/f θορύβου που αναπτύξαμε τόσο για CMOS όσο και για HV-MOS τεχνολογίες δίνουν πολύ ποιοτικά αποτελέσματα για ένα ευρύ φάσμα επιφανειών και συνθηκών λειτουργίας.

List of Publications

Scientific Journals

1. **N. Mavredakis**, N. Makris, P. Habas, and M. Bucher, “Charge-Based Compact Model for Bias-Dependent Variability of 1/f Noise in MOSFETs,” *IEEE Trans. Electron Devices*, 2016, Submitted.
2. **N. Mavredakis**, W. Pflanzl, E. Seebacher, and M. Bucher, “Methodology for 1/f Noise Parameter Extraction for High Voltage MOSFETs,” *Solid State Electronics*, Vol. 103, pp 202-208, January 2015.
3. **N. Mavredakis**, M. Bucher, R. Friedrich, A. Bazigos, F. Krummenacher, J. M. Sallese, T. Gneiting, W. Pflanzl, and E. Seebacher, “Measurements and Compact Modeling of 1/f Noise in HV-MOSFETs,” *IEEE Trans. Electron Devices*, Vol. 60, No. 2, pp 670-676, February 2013.
4. A. Antonopoulos, M. Bucher, K. Papathanasiou, N. Makris, **N. Mavredakis**, R. K. Sharma, P. Sakalas, M. Schroter, “Modeling of High Frequency Noise of Silicon MOS Transistors for RFIC Design,” *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, special issue on Modeling of high-frequency silicon transistors*, Vol. 27, Issue 506, pp 802-811, 2014.
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International Conferences

1. **N. Mavredakis**, and M. Bucher, “Compact Model for Variability of Low Frequency Noise due to Number Fluctuation Effect” to be presented in *46th Europ. Solid-State Device Res. Conf. (ESSDERC)*, Lausanne, Switzerland, September 12-15, 2016.
2. **N. Mavredakis**, W. Pflanzl, E. Seebacher, T. Gneiting, and M. Bucher, “Analysis of Drain Bias Dependence of 1/f Noise in HV-MOSFETs,” in *23rd Int. Conf. on Noise and Fluctuations (ICNF)*, Xian, China, June 2-6, 2015.

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7. R.K. Sharma, A. Antonopoulos, **N. Mavredakis**, M. Bucher,“Impact of Design Engineering on RF linearity and Noise Performance of Nanoscale DG SOI MOSFETs,” in *14th Int. Conf. on Ultimate Integration of Silicon, (ULIS 2013)*, pp 145-148, Warwick, UK, March 19-21, 2013.

8. R.K. Sharma, A. Antonopoulos, **N. Mavredakis**, M. Bucher,“Analog/RF Figures of Merit of Advanced DG MOSFETs,” in *8th Caribbean Conf. on Devices, Circuits and Systems, (ICCDCS 2012)*, pp 1-4, Mexico, March 14-17, 2012.

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Chapter 1

Introduction

1.1 Noise and its Impact on Microelectronics

Noise in electronics and especially in communications, is defined as any undesirable fluctuation that reduces the information of the signal. Focusing on an individual semiconductor such as MOSFET, drain current noise or gate voltage noise respectively are caused by current or voltage fluctuations. Regardless of what is causing these fluctuations, the result is the variation of the current or voltage value around a median value. The Power Spectral Density (PSD) of noise is defined as the Fast Fourier Transform (FFT) of the fluctuation signals mentioned above.

During the last decades, wireless applications such as mobile phones, wireless LAN, Bluetooth, WiMAX, have been tremendously improved and widely used. A main cause of this boost, was the advanced CMOS technology which permitted the integration of different circuits in the same chip. On the other hand, the replacement of bipolar technology with CMOS, brought some issues in terms of noise. Electronic noise in a communication system defines the lowest limit of a signal that can be detected. Below this limit, background noise prevails. Noise can not be completely eliminated, so it can not be ignored, it is always there to limit the accuracy of measurements and set a lower limit of how small signals can be detected and processed. Analog designers nowadays, constantly struggle with the problem of noise since it trades with power dissipation, speed and linearity [1, 2, 3].

This Thesis mainly focuses on Low Frequency Noise (LFN) of Low- and High-voltage (LV-HV) MOS transistors. This kind of noise has a greater impact on these transistors than bipolar ones. LFN is mainly of two kinds; flicker or 1/f noise for larger area devices and random telegraph signal noise (RTS) for smaller ones. PSD of flicker noise is inversely proportional to frequency thus is dominant at low frequencies below the so-called corner frequency f_c. The LFN is a severe obstacle in analog and RF applications [4]. As an example, LFN is up-converted to undesired phase noise in voltage controlled oscillator (VCO) circuits, which can limit the information capacity of communication systems. Furthermore, LFN increases inversely proportional with device area, as a result it becomes of major concern for analog designers in modern ultradeep submicron devices where corner frequencies of tens of MHzs can be observed.

The downscaling of device dimensions makes RTS noise more and more significant. The main cause of RTS noise is the traps or defects at the silicon-oxide interface and this is assumed to be the origin of flicker noise in MOS transistors [5]. In more detail, the superposition of the RTS noise spectra from individual traps could lead to 1/f spectrum. As mentioned above, LFN can be a limiting factor in modern circuits because of its increase with device area and RTS noise is the main cause for this. On the other hand, LFN measurements and characterization are considered a very effective tool for the quality and reliability of MOS devices. The same conclusions can be extracted for HV-MOSFETs. LFN analysis in these devices is also of great importance for several reasons. Firstly HV-MOS technologies can offer higher levels of integration for system-on-chip (SOC) applications. In such applications, such as hand-held devices, where HV transistors are used as switches, LFN can become significant if it couples to other circuits through the substrate. Furthermore, LFN can especially affect the performance of oscillators, analog baseband and bandgap reference circuits. In addition, HV-MOS transistors have also been increasingly used in other $10-120\ V$ circuits, such as gate drives, voltage converters, LED drivers, and high-voltage operational amplifiers. These circuits used in industrial, scientific and medical applications, consumer electronics and cellular base stations, are sensitive to LFN [6].

Because of the importance of LFN in modern analog and RF circuits, noise simulation becomes of great importance to determine whether the overall noise performance of a circuit or a transistor would be sufficient in order the circuit to function properly. Appropriate physics-based mean value as well as statistical LFN models that can predict accurately the noise behavior over a wide range of operating conditions and device dimensions are essential and this is the main objective of this Thesis.

1.2 Historical Background of Semiconductors Evolution

The starting point of semiconductors evolution is dated back in 1904 when the need for better communications led to the invention of the first vacuum diode [7]. The disadvantages of this device such as the high power consumption, the high cost and the big size constituted for the vacuum tube to be considered inadequate to contribute to technology evolution. Researchers of the time soon concentrated on more energyeconomical structures, such as solid-state devices. Around 20 years after the invention of vacuum tube, in 1926, the first concept of an NPN junction transistor being used as an amplifier was patented by Julius Edgar Lilienfield [8]. Soon enough, it become widely adopted that the interest of scientists needed to turn on solid-state devices. It was in 1936 when Mervin Kelly, at Bell Labs, started a group dedicated on solid-state devices. Important researchers such as Bill Schockley, Russel Ohl, Jack Scaff, and others were convinced to join this group and something really innovative was about to begin. This effort was delayed by a significant obstacle, World War II since during the war research was only focused on army applications such as radars.

In 1947, important inventions at Bell Labs changed the future of microelectronics. First of all the point contact transistor was discovered by Bardeen and Brattain [9] while Shockley published the theory of bipolar junction transistor [10]. In 1950, the well-known bipolar junction transistor was invented by Shockley [11]. This device which behaved according to Shockley's theory, was more reliable, easier and cheaper to construct and gave more consistent results than point-contact devices. For their contribution to semiconductors and microelectronics evolution, John Bardeen, Walter Brattain, and William Shockley were awarded with the Nobel Prize in Physics in 1956. The same year, the first computer made of transistors called TX-O[1] was created at the Massachusetts Institute of Technology. In 1962, Steven Hofstein and Frederik Heiman invented a new family of devices called metal-oxide-semiconductor field-effect transistors (MOSFETs) [12]. Despite the fact that these transistors were somewhat slower tha bipolar ones, they outbalanced in cost, size and power dissipation. Furthermore the fact that these devices could be also used as capacitors or resistors was of great interest. In 1965, a paper was published by Moore which predicted that the number of devices in an integrated circuit would double each year [13]. This prediction became the famous "Moore's Law". Today the density of transistors in a chip has surpassed even the billion mark.

During the late '70s, the emergence of the power applications for the large scale integration is a key point at the history of semiconductors and especially of power or high-voltage devices. It was then when the idea of integration of such devices was born and high-voltage/high power circuit parts started to be designed and developed together with the low-voltage ones. In the beginning, different MOSFET configurations were used to build high-voltage transistors. One of these attempts was the so called U-MOS transistor where the gate contacts were put on the sides of the mesas produced using an isotrophic etch [14, 15]. A better approach which finally led to the first commercialized power device [16, 17, 18, 19], was to use an anisotropic etch to produce a V-shaped groove in the silicon surface. Such devices are the known VMOS transistors where the angle of the groove is determined by the crystal structure of the silicon and the channel length by the relative depths of successive diffusions which are essential for the groove to be etched into the surface. An important drawback of this device which makes its production quite difficult, is the inability to control critical etching sufficiently. A better approach for the power MOSFET was the ver-

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[1] Transistorized Experimental computer

tical double-diffused MOS transistor which combines both the concept of a vertical power structure and the one of lateral double diffusion. A slightly different architecture, still based on the same physical concept is the lateral HV transistor [20]. These transistors are the closest to the conventional LV-MOSFET. Both vertical double-diffused and lateral HV transistors are of great importance since they are the better candidates for high-voltage circuits design and they will be analyzed in detail in next chapter of this Thesis.

1.3 Thesis Motivation and Structure

Flicker Noise in MOSFETs remains a critical issue of research during last decades for reasons described above. A lot of work is published on 1/f noise characterization and modeling and plenty of these models concerning both physical and statistical operation of the devices are already available in industry. Nevertheless, there is no doubt that there is a lack of simple, physical approaches which not only would provide a better understanding of the underlying physical principles but also would make noise simulations more precise and faster. As far as LV-MOSFETs are concerned, such a physical charge-based 1/f noise compact model was developed recently [21, 22, 23, 24] based on EKV3 charge-based compact model [2, 25, 26]. At this point it should be noted that there are cases such as HV-MOSFETs where there are no available 1/f noise models in literature and this was one of the innovative scopes of this Thesis. A new physical charge-based 1/f noise compact model for HV-MOSFETs is proposed [27] based on the recently established EKV3 1/f noise model mentioned above. One of the main aspects of this work was to investigate and reveal, if any, additional 1/f noise sources which are not present at LV-MOS transistors and then model them in a sufficient way.

Physics-based 1/f noise models were the main objective of this Thesis not only as far as mean value but also as far as variability of 1/f noise is concerned. Statistical models are of great importance since under specific bias and area conditions, deviation of noise becomes more crucial than its mean value. A basic goal of our research was to find a connection between bias conditions and LFN deviation, in other words to create physics-based bias-dependent statistical compact models which will be connected with fundamental physical effects that generate 1/f noise in MOSFETs. This task was successfully accomplished and the result is presented in this Thesis [28, 29, 30].

The Thesis is organized as follows:

In Chapter 2, the structure and the fundamental device physics that rules both standard LV- and HV-MOS devices are presented. There is a strong correlation between flicker noise behavior and the basic static DC operation of such devices thus in order to correctly develop and extract 1/f noise models, DC models should have been extracted correctly first. The 1/f noise models presented in this Thesis are based on charge-based modeling both for LV and HV devices. Basic operating principles of

EKV3 charge-based compact model for standard MOSFETs are introduced while for HV-MOSFETs a new charge-based compact model [31, 32] based on EKV3 model has been recently established which is also presented in this chapter.

Chapter 3 gives an introduction to the the background of noise in MOSFETs. Statistical nature of noise is briefly outlined and its basic sources in MOS transistors such as thermal noise, 1/f noise etc are described. Afterwards, a generalized noise modeling methodology for MOSFETs adopted by EKV3 approach is addressed. As expected, the chapter is mostly dedicated to 1/f noise and the main physical phenomena that contribute to it which are presented with detailed description of the role that each of them has. In parallel, a brief enumeration and explanation of existing 1/f noise modeling approaches is cited and afterwards, the recently developed charge-based flicker noise compact model for standard CMOS transistors [24, 33] is presented and tested based on data from both $180\,nm$ and $90\,nm$ experimental CMOS technology nodes. Since measurements at $180\,nm$ node were performed in the lab, the instrumentation and measurement set-up is also briefly described.

Chapter 4 addresses 1/f noise modeling in HV devices. Until recently, all models available for HV-MOSFETs use standard LV models as far as flicker noise is concerned. Since the HV transistor is separated in a channel (LV) part similar to a standard MOSFET and the drift region, there was the assumption that only the LV part of the device contributed to flicker noise. Drift region contribution remained uninvestigated mainly because of the lack of adequate measurement set-ups available to measure up to high-voltage values. This issue was solved in this work since a new LFN measurement set-up was provided by AdMoS[2] that permitted 1/f noise measurements at high-voltage values up to $200\,V$. The main scope of this work was to investigate and model the contribution of drift region in 1/f noise. This goal was accomplished and a new complete charge-based 1/f noise compact model was recently published for the first time [27, 34, 35].

Chapter 5 addresses the analysis of statistical behavior of LFN in MOSFETs. Number of oxide traps decreases as device dimensions shrink and as a result Lorentzian-like spectra prevail at small devices which increase the deviation of LFN in these devices. This was already known and a lot of modeling work was devoted to it previously. In larger area devices though where 1/f behavior prevails over RTS, noise variability is connected to operating conditions. A new physics-based bias-dependent statistical 1/f noise compact model is introduced and tested for first time [28, 30] which reveals a direct bias-dependence of 1/f noise variability with fundamental physical effects that are responsible for 1/f noise existence. Apart from the physics-based compact model addressed in [28, 30], a simpler empirical formula which is derived from the fact that LFN variability follows a ~g_m/I_D~ (transconductance-to-current ratio) shape versus inversion level in the channel, was proposed in [29] and presented in Appendix A.

Finally Chapter 6 draws a conclusion.

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[2] Advanced Modeling Solutions

Chapter 2

Basic MOSFET Device Physics

2.1 Low-Voltage MOSFET

2.1.1 General Considerations

Semiconductors, as their name suggests, let current flow through them better than insulators but not as well as conductors. In modern semiconductor industry, silicon is the material which is the most widely used while the metal-oxide-semiconductor field effect transistor (MOSFET) is the fundamental component for circuit design. In the beginning of this section, a simple preview of the MOS transistor structure is introduced. Afterwards, the basic part of the MOS transistor is presented which is the so called MOS capacitor. This is the two terminal MOS structure the analysis of which is shown to be very helpful to explain the working principles of MOSFET. After that, the complete four terminal MOS structure is addressed while some fundamental MOSFET effects are described [2]. Finally the fundamental functionalities of EKV3 charge-based model are introduced.

2.1.2 MOSFET Structure and Operation

MOSFET operation, as described by its name, is defined by the field effect. More particularly the electric field that appears between two nodes, determines the conductance between the other two nodes. FET devices are considered to be voltage controlled current sources while bipolar devices are current controlled current sources. This basic difference is a big advantage for FET transistors since it leads to lower power consumption circuits.

In more detail, MOSFET is a four terminal 3D device and as all semiconductors, can be built with two complementary ways depending on the polarity of its regions: NMOSFET and PMOSFET. In Figure 2.1, the circuits symbols of both NMOSFET and PMOSFET are shown. The four terminals of a MOSFET are: Gate (G), Source

(S), Body or Bulk (B) and Drain (D). In reality there is an insulator interface between the gate and the rest of the device. The developing field below the gate insulator defines the conductance between the drain and the source nodes.

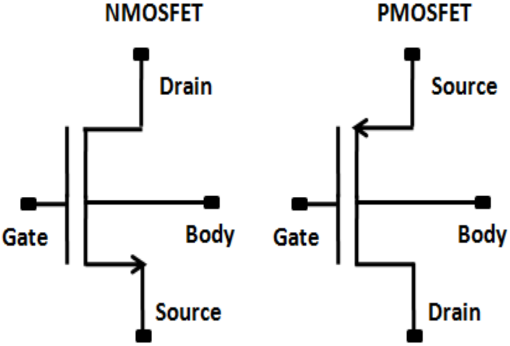


Figure 2.1: NMOS-PMOS circuit symbols

In Figure 2.2, a cross-section of an NMOSFET device is illustrated. Body terminal is considered to extend in whole substrate region which in NMOSFET is usually a p-type semiconductor. Typical doping concentration for the substrate are 10^{16} to $10^{18}\,cm^{-3}$. For the ideal connection of the substrate with the metal terminal, some regions of more intense doping (p+) are used. In older CMOS generations the gate material was aluminum; then many generations used implanted polysilicon gates, while technologies roughly from $45\,nm$ generation use high-k metal gates.The gate consists of an conductive surface which lays upon an insulator layer as mentioned above. The most widely used insulator in this case is silicon dioxide (SiO_2). For the better operation of the device, the gate should have as low a resistance as possible and for this reason, polysilicon gates are usually implanted together with source and drain, which are of opposite type of channel implant. [2, 12, 36, 37, 38, 39]. Consequently two parasitic pn junctions are formed between source and drain and the substrate respectively. For the valid operation of the device, these two diodes should be reverse biased in order to ensure electrical isolation between source, drain and the substrate. This leads to the following equations:

$$\begin{gathered} V_S > V_B \Longleftrightarrow V_S - V_B > 0 \Longleftrightarrow V_{SB} > 0, \ (nMOS) \\ V_D > V_B \Longleftrightarrow V_D - V_B > 0 \Longleftrightarrow V_{DB} > 0 \end{gathered} \tag{2.1}$$

where V_S is the source voltage, V_D is the drain voltage and V_B is the bulk voltage. It is easily noticed by the Figure 2.2, that there is an explicit symmetry between source and drain terminals. It is the biasing of the device that can break this symmetry. In NMOSFETs, source terminal is considered to be in lower voltage than drain.

$$V_D > V_S \Longleftrightarrow V_D - V_S > 0 \Longleftrightarrow V_{DS} > 0, \ (nMOS) \tag{2.2}$$

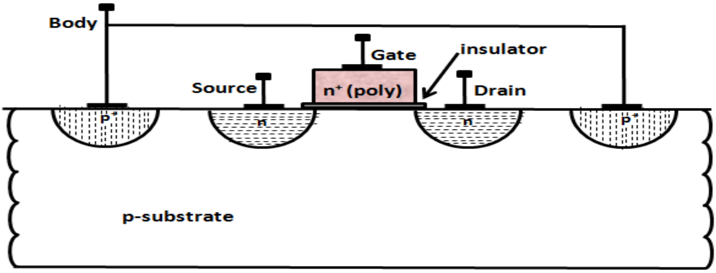


Figure 2.2: Cross-section of an NMOS device

In a first level qualitative analysis of the device, it is observed that there is no electrical connection between source and drain. The p-type semiconductor between them, insulates these two regions. On the other hand as mentioned before, gate voltage, depending on its intensity, may attract carriers of the same type (n in case of NMOS) with source and drain and as a result a new layer of carriers to be created close to the insulator which permits the electrical connection between the two edges, source and drain. This is the so called channel of the device. With the term channel we refer to the region below the gate even if there are no concentrated carriers there. The channel width W and length L can vary greatly depending on circuit design needs. In digital circuits, L is normally kept at the minimum value possible. In fact, the actual values of W, L after fabrication can be different than the drawn values extracted from the layout because of fabrication reasons. Thus:

$$\begin{aligned} W_{EFF} &= W - \Delta W \\ L_{EFF} &= L - \Delta L \end{aligned} \tag{2.3}$$

where W_{EFF} and L_{EFF} are the actual channel length and width respectively while W, L are the corresponding layout or drawn values, and ΔW and ΔL are the corrections that are essential in order to reach true dimensions. Effective length L_{EFF} as well as oxide thickness T_{OX} play an important role in the performance of MOS circuits thus one of the basic reasons of CMOS process evolution is the shrinking of these two dimensions.

The case of PMOS is completely dual with NMOS, a PMOS device has exactly the same structure but different polarities (Figure 2.3). One basic difference is that since PMOS are built in the same substrate with NMOS in CMOS technologies, their construction demands the creation of a large n-type area inside the p-type substrate. This area is named n-well. Equations 2.1 are valid in PMOS by just changing the signs while source terminal is considered to be in higher voltage than drain.

$$V_D < V_S \Longleftrightarrow V_D - V_S < 0 \Longleftrightarrow V_{DS} < 0, \ (pMOS) \tag{2.4}$$

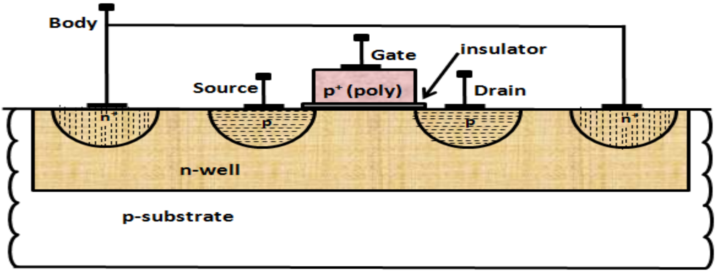


Figure 2.3: Cross-section of a PMOS device

Apart from the conventional, there are different types of CMOS processes such as STI (Shallow Trench Isolation) and SOI (Silicon on Insulator). STI is an advanced process which has been used widely. A "trench" filled with oxide isolate devices from one another and thus permitting the devices to be packed closer to each other without the danger of a latch up immunity. Even better isolation is provided with SOI processes where each device is surrounded by oxide and this results to complete isolation from neighboring devices.

2.1.2.1 The Two Terminal MOS Structure

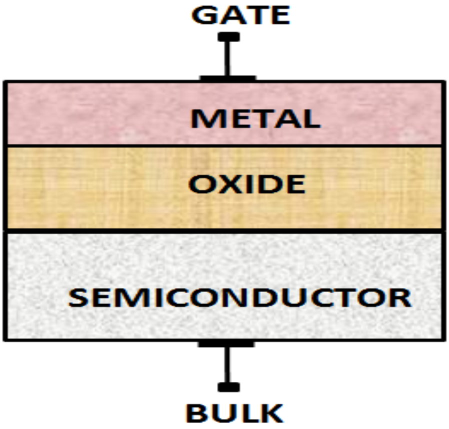


Figure 2.4: Cross-section of a MOS capacitor

In order to understand the working principles of a MOS transistor, it is useful to first understand its basic part; the two terminal MOS structure. This structure is often referred to as MOS capacitor and is shown in Figure 2.4 [2]. In the MOS capacitor, the terminals source and drain are ignored and the analysis is focused on the gate and the area below it, the channel region [39, 40].

In the following analysis (Figure 2.5), a voltage source V_{GB} is applied between the gate and the bulk of the device and the way it is distributed as well as the effects it has, are studied [2, 41, 42]. Below the oxide ($y = 0$), charge Q_{OX} is noticed which refers to trapped charges of the oxide from the substrate side which are created during fabrication. Since Q_{OX} is fixed it does not influence significantly the operation of the device. On the contrary Q_G at $y = -T_{OX}$ and Q_C at $y > 0$ are of great importance since they directly depend on V_{GB} value. In case V_{GB} is positive enough, then such an amount of carriers can be concentrated below the oxide that even they are inside a p-type semiconductor, an area with higher n-type concentration can be created.

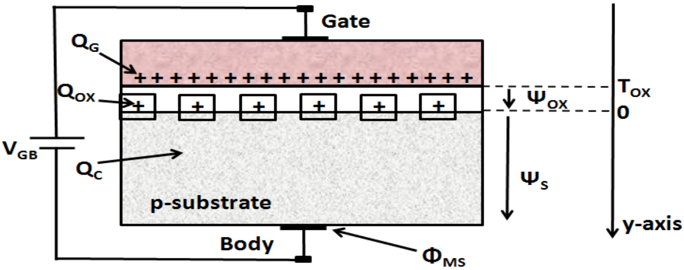


Figure 2.5: MOS capacitor analysis

As far as voltage analysis is concerned, Φ_{MS} is the voltage drop that is created when there is contact between gate and substrate materials. It is called work function and is related with the allowed energy bands of the materials. Its value is around $-1\,V$ for NMOS and $1\,V$ for PMOS [43, 44]. Additionaly, voltages Ψ_{OX} and Ψ_S which are related to the charges Q_G and Q_C respectively, appear. Ψ_S is also known as surface potential. By applying the Kirchhoff voltage law at circuit in Figure 2.5:

$$V_{GB} = \Phi_{MS} + \Psi_{OX} + \Psi_S \tag{2.5}$$

Furthermore from charge preservation law:

$$Q'_G + Q'_{OX} + Q'_C = 0 \tag{2.6}$$

where the charges are expressed per unit area. The relation between Q'_G and Ψ_{OX} is:

$$\Psi_{OX} = \frac{Q'_G}{C'_{OX}} \tag{2.7}$$

where C'_{OX} is the oxide capacitance per unit area and is defined as the ratio of oxide permittivity and oxide thickness:

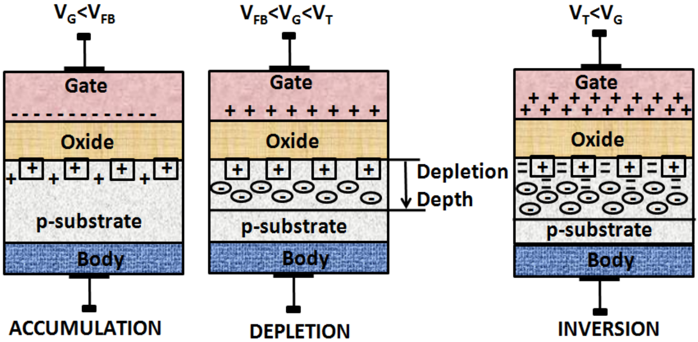
$$C'_{OX} = \frac{\varepsilon_{OX}}{T_{OX}} \tag{2.8}$$

At this point flat-band voltage V_{FB} can be defined. V_{FB} is defined as the V_{GB} value that should be applied so as the $Q_C^{'} = 0$. In this case, from Equations 2.5, 2.6:

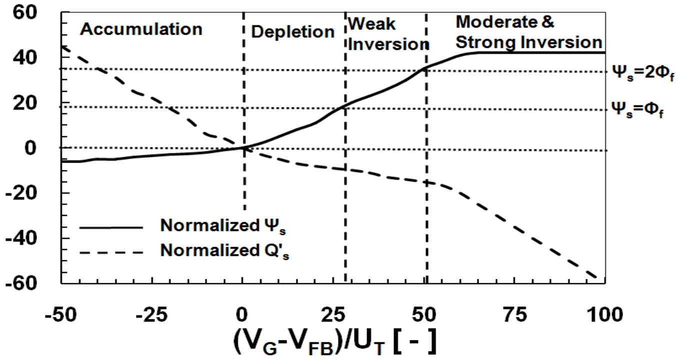
$$V_{FB} = \Phi_{MS} - \frac{Q'_{OX}}{C'_{OX}} \tag{2.9}$$

From Equations 2.6, 2.7, 2.9, Equation 2.5 can be reformed to:

$$V_{GB} = V_{FB} + \Psi_S - \frac{Q'_C}{C'_{OX}} \tag{2.10}$$



(a) Schematic



(b) Normalized Ψ_S, $Q_C^{'}$

Figure 2.6: NMOSFET operation regions

Before the delimitation of operation regions of the structure, the definition of the n-type carriers concentration in the surface can be very useful.

$$n_{surface} = n_i \exp\left(\frac{\Psi_S\text{-}\Phi_F}{U_T}\right) \approx N_A \exp\left(\frac{\Psi_S\text{-}2\Phi_F}{U_T}\right) \tag{2.11}$$

where n_i is the electron concentration in the intrinsic semicoductor or intrinsic carrier concentration, N_A is the doping of the device, U_T is the thermal voltage and Φ_F is the fermi potential [2]. Definition of the V_{FB} (Equation 2.9) was based on the nihilism of substrate charge $Q_C^{'}$. Consequently the operation of the device varies with $V_{GB} - V_{FB}$ variation. As mentioned above, when $V_{FB} = V_{GB}$, then $Q_C^{'}$, $\Psi_S = 0$ and this is called Flat-Band Condition. When the $V_{GB} - V_{FB}$ difference is negative then Ψ_S is negative and $Q_C^{'}$ is positive (Figure 2.6b) and in this case more holes are added in the already existing ones in the semiconductor. This region is called accumulation (Figure 2.6a). While V_{GB} increases, at some point it becomes greater than V_{FB} and thus $V_{GB} - V_{FB}$ as well as Ψ_S become positive while $Q_C^{'}$ becomes negative (Figure 2.6b). This region is named depletion and n-type carriers start to be gathered in the surface (Figure 2.6a). But this concentration is still much smaller than p-type carriers of the substrate (N_A) and also smaller than intrinsic carrier concentration n_i. By increasing V_{GB} more, at the point where the concentration of n-type carriers become larger than n_i, the device starts to operate in the so-called inversion region. At this point $\Psi_S = \Phi_F$ (Figure 2.6).

Inversion region is divided into three subcategories depending on the level of inversion in the channel. Weak inversion is defined the region where n-type concentration is bigger than n_i but smaller than N_A. Next region is called moderate inversion and starts when Ψ_S becomes two times the Φ_F. Both in moderate and in strong inversion which follows, n-type concentration is bigger than N_A. The limit of these two regions is not so clear but generally speaking the width of moderate inversion as far as Ψ_S is concerned, is some U_T [2, 25]. It is crucial here to define inversion Coefficient (IC), which is a numerical measure of MOS inversion level where unity corresponds to the center of moderate inversion [26].

$$IC = \frac{I_D}{I_0(\frac{W}{L})} \tag{2.12}$$

where I_0 is the technology current:

$$I_0 = 2n\mu C_{OX}^{\prime} U_T^2 \tag{2.13}$$

where n is the weak inversion slope factor and μ is the carrier mobility. Values of IC less than 0.1 correspond to weak inversion, values between 0.1 and 10 to moderate inversion and values above 10 to strong inversion. In older CMOS processes moderate inversion was much less important since power supply voltages were quite high. But nowadays, power supply becomes less and less and as a result moderate and even weak inversion can become very important since circuits often have their optimal operation conditions in these regions.

2.1.2.2 The Four Terminal MOS Structure

With the introduction of the other two terminals, source and drain, the four terminal device or complete MOS transistor (NMOSFET in this analysis) is formed

(Figure 2.7). In this structure, the x-axis is introduced with direction from source to drain. With the source and drain terminals connected to some bias supply, the electric contact through the channel is possible. By introducing the two terminals at the edges of the channel and by applying different voltages in each of these terminals, the uniformity along the channel is broken. The concept of V_{CH} is addressed where $V_{CH}(0) = V_{SB}$ and $V_{CH}(L_{EFF}) = V_{DB}$. In each point of the x-axis in the channel a different inversion level can be assumed which can be defined as:

$$\begin{aligned} \Phi_F + V_{CH} < \Psi_S < 2\Phi_F + V_{CH} &\longleftrightarrow \textit{weak inversion} \\ 2\Phi_F + V_{CH} < \Psi_S &\longleftrightarrow \textit{moderate inversion or strong inversion} \end{aligned} \tag{2.14}$$

The inversion level at source is the one to determine the inversion level in the whole device.

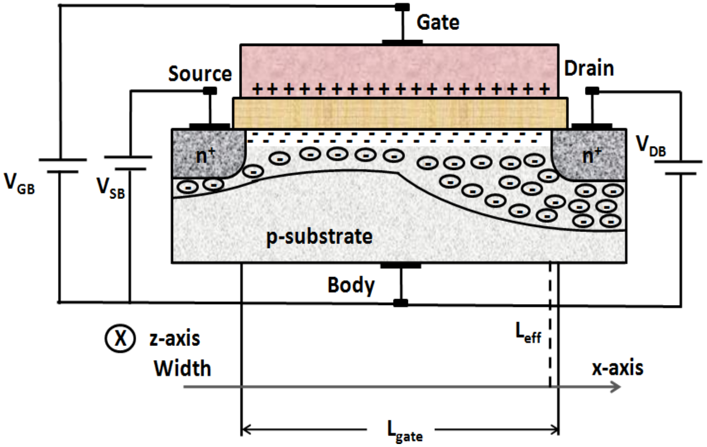


Figure 2.7: Complete four terminal NMOSFET

As mentioned above (Section 2.1.2.1) gate voltage is responsible for the creation of the channel below the oxide. It is also responsible for the determination of the level of the inversion, if it is weak, moderate or strong. In case, V_{GB} is low enough that the device is not inverted, then terminals source and drain are not significant in the operation of the device since they are electrically isolated from the rest semiconductor. Only in inversion region, channel can be created and current can flow through it.

The source and drain form two pn junctions with the body which are reverse-biased. In a pn junction the resulting depletion region extends to both the n and p sides [2]. In the NMOS transistor, the drain potential is more positive than the source potential (Equation 2.2). Consequently, the reverse bias np junction across the drain-body is larger, and the depletion region for that junction is deeper. As a result, there are larger numbers of negatively charged acceptor atoms around the drain than there are near the source which means that fewer electrons are needed near the drain to balance the positive charges on the gate. It is for this reason that the larger electron concentration is found near the source which become larger with the increase of gate potential leading to higher inversion level for the device.

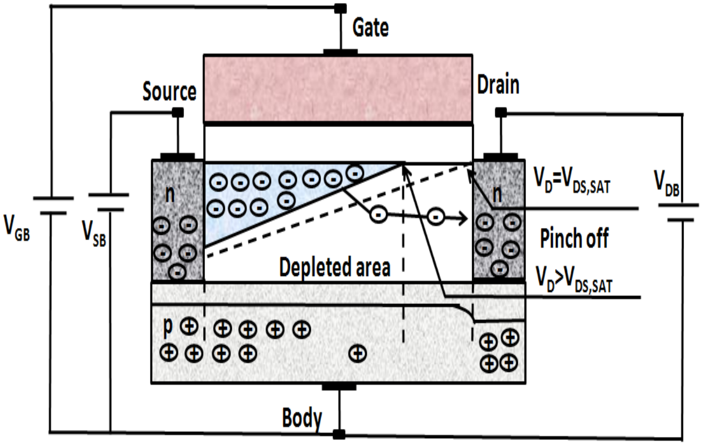
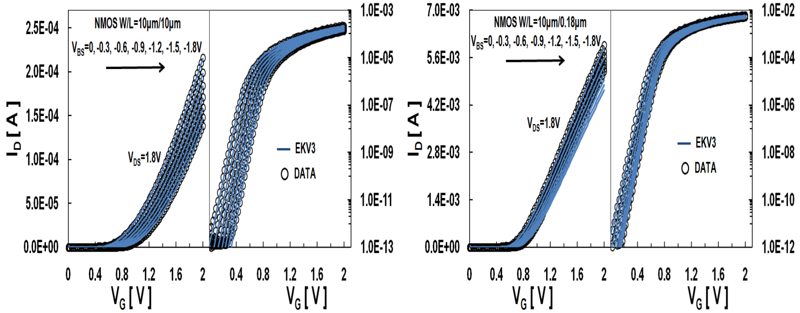


Figure 2.8: NMOS in saturation region

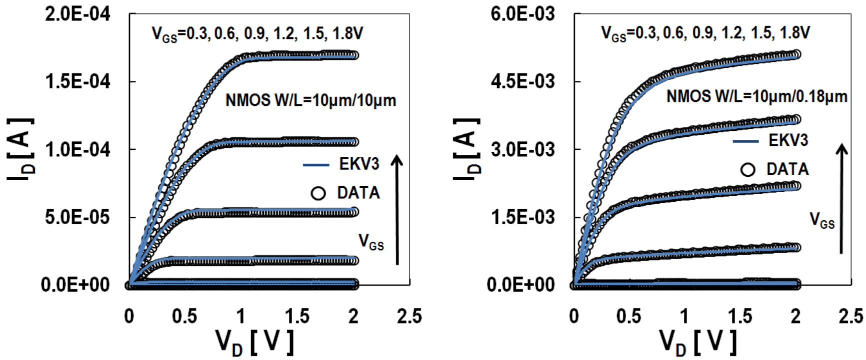
The potential difference V_{DS} is positive and appears accross the inversion layer. It causes electron movement; electrons enter from the source, flow through the channel and are drained by the drain and thus a positive current I_D is formed from the drain to the source. Supposing that V_{DS} starts from zero value and is gradually increased then drain current will also increase. For small values of drain potential, its effect on drain current is large but for quite high drain potential values above the so-called saturation value $V_{DS,Sat}$, the current gets saturated and remains constant. This happens because above this saturation value, the drain voltage is such high that can drain all electrons that can be supplied by the channel and the channel gets pinced-off while drain gets depleted (Figure 2.8). These two regions below and above the $V_{DS,Sat}$ value can be distinguished as linear and saturation regions. $V_{DS,Sat}$ value depends on gate potential and it increases as gate potential increases.

In Figure 2.9, the fundamental drain current characteristics of both long ($W/L = 10\,\mu m/10\,\mu m$) and short ($W/L = 10\,\mu m/0.18\,\mu m$) NMOS transistors from an experimental $180\,nm$ CMOS process are shown. As mentioned above, drain current depends on gate potential since the inversion level is defined by V_G, and on drain potential since the linear or saturation operation is determined by V_{DS}. The plot of I_D versus V_G is named transfer characteristic and it can be shown in a logarithmic or linear I_D axis depending on the level of inversion as in Figures 2.9a, 2.9b. In weak inversion, for lower V_G values where I_D's behavior is exponential, it is shown in logarithmic axis (right subplot) while in strong inversion, for higher V_G values the behavior of I_D is shown in linear axis (left subplot). Different lines represent different V_B values. Figures 2.9c, 2.9d are the so-called output characteristic and show the plot of I_D versus V_D. Different lines represent different V_G values. It can be noticed that for each V_G value there is a unique V_D value above which the drain current is saturated. The higher the V_G value the higher the $V_{D,Sat}$ gets. Finally in Figure 2.9, both measurements (markers) and EKV3 model (line) are shown and the model seem to perfectly fit the experimental data.



(a) Transfer - long channel

(b) Transfer - short channel



(c) Output - long channel

(d) Output - short channel

Figure 2.9: Transfer and output characteristics of NMOS

2.1.3 Basic MOSFET Effects

The fundamental effects that take place during the operation of a MOS transistor are listed and briefly explained in this section. Some of these effects known as "core" effects, exist in any MOSFET regardless its structure or geometry such as threshold voltage, carrier mobility etc, while some others become significant and affect the whole structure operation under certain circuimstances such as the short channel length in short channel effects.

Threshold Voltage

Threshold voltage is defined as the value of V_{GB} where the inversion charge equals to zero. In fact is the point where as V_{GB} increases the channel starts to be created. From [2, 39]:

$$V_{TB} = V_{FB} + \Psi_S + \gamma\sqrt{\Psi_S} \tag{2.15}$$

where γ is the substrate coefficient and will be defined later. The difference between threshold voltage and flat-band voltage is that V_{FB} is the value of gate voltage where the whole semiconductor charge equals to zero. ($Q_C^{'} = 0$) while V_{TB} is the value of gate voltage where the invesion charge equals to zero ($Q_I^{'} = 0$).

Substrate Effect

In Figure 2.8, body or substrate terminal is connected to the ground. Assuming that a voltage source is inserted in such a way that the body potential becomes smaller than the source potential, this will cause the population of electrons in the channel to decrease and as a result drain current will also decrease. This phenomenon is referred to as body or substrate effect. In an NMOS transistor, V_{SB} must be positive for body effect to be activated. This means either V_B to be negative in case V_S is zero or V_S to be positive in case V_B is zero (Figures 2.9a, 2.9b). To make things clearer, the body is a conductive structure, separated from the channel by an “insulating “ region (depletion) in a similar way as the oxide separates the gate and the channel. So, the body behaves as a back gate which means that by applying a negative potential population of electrons will be reduced just as if the gate potential would be negative. Substrate coefficient γ is defined as:

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{OX}'} \tag{2.16}$$

where q is the electron charge and ε_{si} is the silicon permittivity.

Slope Factor

The subthreshold or weak inversion slope of drain current versus gate voltage (Figures 2.9a, 2.9b) is named slope factor. Slope factor is defined as the first derivative of threshold voltage versus surface potential [2, 39]:

$$n = \frac{\vartheta V_{TB}}{\vartheta \Psi_S} = 1 + \frac{\gamma}{2\sqrt{\Psi_S}} \tag{2.17}$$

Slope factor value is always above unity and can go up to 1.5 depending on the process.

Pinchoff Voltage

In Figure 2.8, when $V_{DS} \geqq V_{DS,Sat}$ the drain part is depleted and the device enters saturation region. Under these conditions, the channel is considered to be "pinched-off". Pinchoff terminology comes from the old days when only strong inversion was known and in other cases the inversion layer was assumed to be pinched off which means that the charge was assumed to decrease to zero. In order to define the pinchoff voltage, the pinchoff surface potential should be defined firstly. From Equation 2.15:

$$V_{GB} = V_{FB} + \Psi_P + \gamma\sqrt{\Psi_P} \tag{2.18}$$

where Ψ_P is the surface potential of zero charge or pinchoff surface potential. Pinchoff voltage V_P can be defined as:

$$V_P = \Psi_P - 2\Phi_F = \Psi_P - \Psi_0 \tag{2.19}$$

and is considered to be the channel potential value which would have made inversion charge equal to zero if strong inversion theory was valid even for very arbitrary small $Q_I^{'}$. From threshold voltage definition (2.1.3), it can be assumed that V_P is the channel potential value where applied gate potential is equal to threshold voltage. Based on this, a simple approximation of V_P could also be [2]:

$$V_P = \frac{V_G - V_{TH}}{n} \tag{2.20}$$

Carrier Mobility

In a silicon semiconductor without any dopants under thermal equilibrium and no applied electric field, the mobility equals to:

$$\begin{aligned} \mu_e &\approx 0.143 \left(\frac{T}{300K}\right)^{-2} \frac{m^2}{V.s} \\ \mu_h &\approx 0.046 \left(\frac{T}{300K}\right)^{-2.18} \frac{m^2}{V.s} \end{aligned} \tag{2.21}$$

where μ_e is the electron mobility and μ_h is the hole mobility [45, 46]. T is the kelvin temperature. Real mobility in MOSFET devices is smaller than the values above (Equation 2.21) because of the non uniform inversion charge and the vertical field created by gate potential. Various scattering mechanisms limit the carrier mobility. These mechanisms are:

- Surface scattering [47, 48]
- Coulomb scattering [49]
- Phonon Scattering [50]

Each one of the above mechanisms will give a mobility coefficient such as μ_s, μ_c and μ_{ph} respectively. The active mobility can be calculated from the empirical rule of Mathiessen [51, 52, 53]:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_s} + \frac{1}{\mu_c} + \frac{1}{\mu_{ph}} \tag{2.22}$$

From now on, in any equation that carrier mobility is needed such as in drain current or even in noise equations, μ_{eff} will be used after it is modeled correctly.

Quantum Mechanic Effects

As long as the gate oxide thickness shrinks with CMOS technology evolution, quantum mechanic effects can not be considered negligible any longer. They affect significantly the transistor's operation. The thinner oxide leads to higher electric field in the channel since potentials do not decrease propotionally with T_{OX} [42, 54]. An important effect on transistor's operation is that quantum mecahnic effects' activation influence the oxide capacitance per unit area C'_{OX}. Furthermore they affect the value of Ψ_0 which is defined as the double of fermi potential Φ_F.

Short Channel Effects

The analysis of the effects until now was based on the assumption that device's channel length is quite long so that the effects that take place in the edges of the channel are insignificant. But as it has been mentioned, short channel devices are really important and it is those which are used mainly in circuit design. Consequently the studying of short channel effects is essential. Some of the most important of them which are going to be presented are:

- Velocity saturation
- Channel length modulation
- Drain induced barrier lowering
- Series resistance

Velocity Saturation-Channel Length Modulation Up to now, the dependence of carrier mobility on the vertical field was studied while the dependence on horizontal field was ignored. In the horizontal axis, the field depends proportionally on V_{DS} potential while it inreases as the channel length decreases and the carrier velocity will be proportional to this horizontal field at any channel point. On the other hand, there is a maximum value of the carrier velocity, consequently the linear relationship between horizontal field and carrier velocity is valid only for low fields while for higher fields this velocity is saturated. This effect is called velocity saturation [55, 56]. At presence of velocity saturation, channel can be divided into two parts: the first which is bigger at the source side is the one where the velocity is not saturated yet and the second at the drain side will be crossed by carriers with saturated velocity which can not accelerate more. In other words, only the first part operates like a MOSFET while the current which is created in the first part just flow through the second. As mentioned before, the channel can be divided in a non-velocity saturated part at the source side and a saturated part towards the drain side. All the effects and equations presented so far are valid in the non-velocity saturated part. The channel length of the velocity-saturated part should be calculated and subtracted from the effective channel length: $L' = L_{EFF} - \Delta L_{CLM}$ [57]. This is the channel length modulation effect. Through this active channel, the horizontal field affects the carrier mobility similarly with the vertical field so a new term of mobility is taken into account at Equation 2.22.

Drain Induced Barrier Lowering The potential values at source and drain can affect the surface potential along the channel. Since in NMOS, the drain voltage is higher than source voltage, this effect depends on drain voltage mainly especially in saturation region. This effect is called Drain induced barrier lowering or DIBL effect. Because of this, a significant dependence of threshold voltage on drain voltage is noticed, in fact threshold voltage decreases as drain voltage increases [58].

Series Resistance There is a small resistance which appears inside the active area of source and drain areas. This resistance is insignificant in long transistors but this is not valid in short ones since there a significant voltage drop is developed which can not be ignored in the calculation of drain current. These series resistances are proportional to half of the lenght of active source and drain areas. This length is symbolized as H_{DIF}.

2.1.4 EKV3 Charge-Based Model

2.1.4.1 Introduction

Main scope of MOSFET modeling remains the complete and correct description of the device behavior. Models are used inside a simulator and a good model ensures that a circuit design will meet the specifications defined initialy. Basic criteria of a good MOSFET model are both the accuracy of the prediction of device operation as well as the speed of simulation since circuit complexity becomes higher and higher. But what is a model? It is a set of physical equations written in a programming language such as Verilog-A, which describes the operation of the device. Compact models are usually either empirical, or physics-based. The physical approach is by any means better since it uses less parameters and also is easily adjusted to different CMOS processes. For these reasons, physics-based models are now exclusively used and the demand from the circuit design community for highly consistent and fully featured such models, has increased tremendously. In the present Thesis, the charge-based modeling approach introduced by EKV model is used in LFN modeling both for LV and HV devices. The EKV model [2, 22, 25, 42, 59, 60, 61, 62, 63, 64, 65, 66] is considered to be the first continuous model from weak to strong inversion something really innovative since in modern sub-micron CMOS processes, moderate and weak inversion are of great importance from a design point of view.

The EKV model allows physically consistent and accurate modeling of charges and current without introducing artificial parameters additional to physical parameters. One of the most important characteristics of the model, was the replacement of the current and transconductance interpolation functions between weak and strong inversion firstly proposed in [25], by a more physical one, derived from the linearization of inversion charge versus surface potential [65]. The EKV model is continually being developed to include all the effects that might affect MOSFET operation such as:

- Nonuniform doping [67]
- Non-quasi-static model [68, 69]
- Polysilicon depletion and quantum effects [70, 71]
- Charge/transcapacitances modeling [72, 73]
- Mobility modeling [74]
- Series resistance, overlap capacitance [75, 76]
- High frequency and thermal noise modeling [69, 77, 78, 79, 80, 81, 82]
- Flicker noise modeling[1] [24, 33]
- Transconductance analysis [26, 83]
- Parameter extraction [67, 84, 85]

The latest version of EKV MOST model is the EKV3.0 full-featured compact model which has already been released and included in some of the most known simulators such as spectre [39, 73, 86, 87, 88].

2.1.4.2 Charge Model

As it has been introduced before, inversion is the most important operation regime of a MOSFET since only there channel is activated and current flows along it. In this region, the charge in the semiconductor ($Q_C^{'}$) is the sum of immobile bulk ($Q_B^{'}$) and mobile inversion ($Q_I^{'}$) charge. Inversion charge is accumulated just beneath

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[1] Our work

the oxide while the bulk charge is located in the depletion area of a specific depth. Under charge sheet approximation, $Q_B^{'}$ is given by:

$$Q_B' = -\gamma C_{OX}' \sqrt{U_T} \sqrt{\frac{\Psi_S}{U_T}} \tag{2.23}$$

Inversion charge is then expressed as:

$$Q_I' = Q_C' - Q_B' = -C_{OX}' \cdot \left(V_G - V_{FB} - \Psi_S - \gamma \sqrt{\Psi_S} \right) \tag{2.24}$$

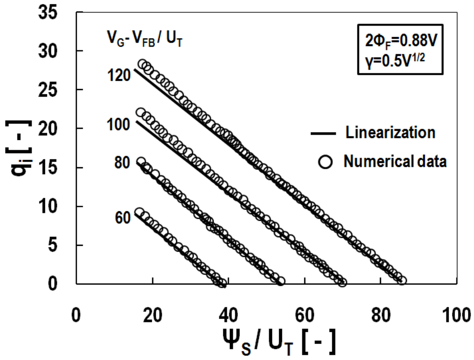


Figure 2.10: Normalized inversion charge vs. surface potential for different gate voltage values

One of the most important considerations in charge-based model, is the linearization between the inversion charge and surface potential as it seems in Figure 2.10, something that is not taken into account in Equation 2.24. For the purposes of this linearization [65], the pinch off surface potential Ψ_P is defined as the surface potential where the inversion charge equals to zero [25, 42, 65, 70] (Section 2.1.3). From Equation 2.24 if $Q_I^{'} = 0$ then:

$$\Psi_P = V_G\text{-}V_{FB}\text{-}\gamma^2 \left(\sqrt{\frac{V_G - V_{FB}}{\gamma^2} + \frac{1}{4}} - \frac{1}{2} \right) \tag{2.25}$$

The extraction of a simple linear equation between inversion charge and surface potential is now possible.

$$Q_I' = nC_{OX}' \left(\Psi_S - \Psi_P \right) \tag{2.26}$$

where n is the slope factor defined in Equation 2.17. Another important consideration in EKV charge model is the normalization of all quantities such as charges, current, potentials etc. Normalized current or inversion coefficient calculation through specific current I_{SPEC} has already been introduced (Equations 2.12, 2.13). All potentials are normalized with thermal voltage U_T while charges are normalized with the quantity

$$Q'_{SPEC} = -2nU_T C'_{OX} \tag{2.27}$$

After taking into account all these considerations, the applying of Poisson equation at the channel leads to the basic charge-voltage relationship of the MOSFET which is:

$$2q_i + lnq_i = u_P - u_{CH} \tag{2.28}$$

where q_i is the normalized inversion charge and u_p, u_{ch} the normalized pinch-off and channel potential respectively. In weak inversion, it holds that $q_i \lll 1$ and the mobile inverted charge can be approximated by:

$$q_i = exp(u_P - u_{CH}) \tag{2.29}$$

while in strong inversion $q_i \ggg 1$ and thus:

$$q_i = \frac{u_P - u_{CH}}{2} \tag{2.30}$$

2.1.4.3 Current-Transconductances Model

The current transport equation in MOSFETs is written:

$$I_D = \mu W \left(-Q'_I \frac{\vartheta \Psi_S}{\vartheta x} + U_T \frac{\vartheta Q'_I}{\vartheta x} \right) \tag{2.31}$$

Using the charge linearization approximation by differentiating Equation 2.26, we can get:

$$\frac{\vartheta \Psi_S}{\vartheta x} \approxeq \frac{1}{n} \frac{\vartheta Q'_I}{\vartheta x} \tag{2.32}$$

which allows us to integrate the channel current from source to drain in terms of source and drain normalized inversion charges q_s and q_d [42, 65]. Thus:

$$I_D = 2nU_T^2 \mu C'_{OX} \frac{W}{L} \left[q_s^2 + q_s - q_d^2 - q_d \right] \tag{2.33}$$

In Equation 2.33 the quantity $2nU_T^2 \mu C'_{OX} \frac{W}{L}$ is the specific current I_{SPEC} which is the denominator of Equation 2.12. The quantity $q_s^2 + q_s - q_d^2 - q_d$ is the normalized current i or the inversion coefficient IC defined in Equation 2.12. The above drain current can be expressed in symmetric forward and reverse normalized currents i_f and i_r [25] (Figure 2.11) as:

$$i = \frac{I_D}{I_{SPEC}} = \left[i_f - i_r \right] \begin{cases} i_f = q_s^2 + q_s \\ i_r = q_d^2 + q_d \end{cases} \tag{2.34}$$

For short channel devices where velocity saturation effect is activated, the equation of normalized current transforms to [22, 23]:

$$i_{dlc} = \frac{q_s^2 + q_s - q_d^2 - q_d}{1 + \lambda_c (q_s - q_d)} \tag{2.35}$$

where :

$$\lambda_c = \frac{2U_T}{E_{CRIT} (L_{EFF} - \Delta L_{CLM})} \tag{2.36}$$

In case of a long channel device where VS is not active, λ_c becomes very low and as a result Equation 2.35 becomes equal to Equation 2.34.

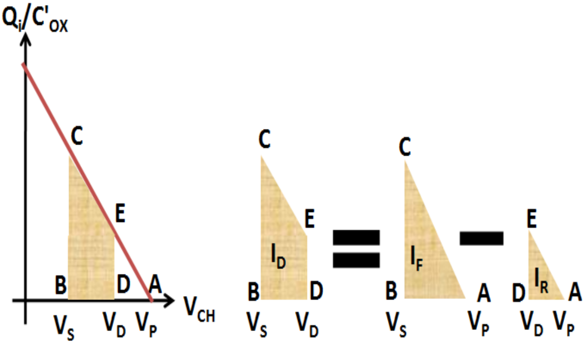


Figure 2.11: Forward and reverse drain current components

Source, gate and drain transconductances (g_{ms}, g_m, g_{md}) respectively, can be defined as:

$$g_{ms} = -\frac{\vartheta I_D}{\vartheta V_S},\; g_m = -\frac{\vartheta I_D}{\vartheta V_G},\; g_{md} = -\frac{\vartheta I_D}{\vartheta V_D} \tag{2.37}$$

Transconductances can be directly related to normalized inversion charges as [42]:

$$g_{ms(d)} = G_{SPEC} q_{s(d)} \tag{2.38}$$

where

$$G_{SPEC} = \frac{I_{SPEC}}{U_T} \tag{2.39}$$

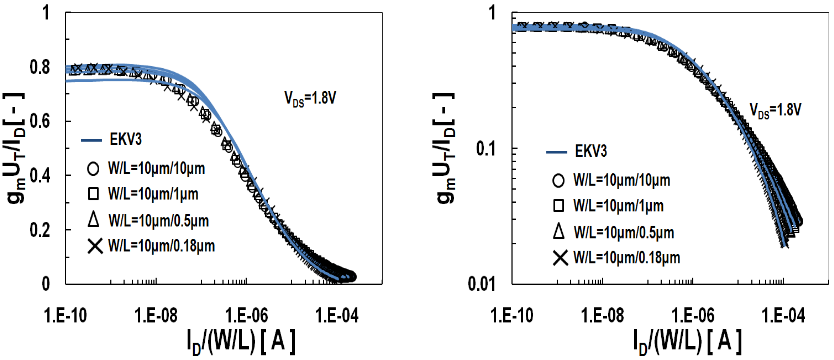
is the specific transconductance and

$$g_m = \frac{g_{ms} - g_{md}}{n} = \frac{G_{SPEC}}{n} (q_s - q_d) \tag{2.40}$$

There is a very important relationship that can be extracted by the above equations, among transconductance and normalized current. This is the transconductance-to-current ratio [63].

$$G(IC) = \frac{g_{ms} U_T}{I_D} = \frac{1}{0.5 + \sqrt{0.25 + i}} \tag{2.41}$$

In Figure 2.12, normalized transconductance-to-current ratio of different area MOSFETs from an experimental 180 nm CMOS process is shown versus normalized with area drain current - $I_D/(W/L)$ - in saturation region. In Figure 2.12a, I_D axis is linear while in Figure 2.12b is logarithmic where the steeper behavior of the short channel device due to VS effect is clear. It is interesting to note that $g_m U_T/I_D$ is independent of any process parameters and thus it is very important from design point of view. Both measurements (markers) and EKV3 model (line) are shown and the fit is really good.



(a) Linear I_D axis

(b) Logarithmic I_D axis

Figure 2.12: Normalized transconductance versus inversion coefficient

2.2 High-Voltage MOSFET

2.2.1 General Considerations

The integration of high-voltage (HV) MOS devices with the low power modules in MOS technology lead to a dramatical increase of interest in these devices [89, 90, 91, 92, 93]. Nowadays, HV-MOS devices are used in a wide range of power applications such as switch-mode power supplies, motor drivers and power amplifiers. In this section the basic architectures of HV-MOSFET and their fundemental operating principles as well as their most important special effects will be introduced. Finally the charge-based modeling in HV devices will be presented and explained.

2.2.2 High-Voltage MOSFET Architectures

Three different types of HV-MOSFETs are, nowadays, used with CMOS technology which are the following:

- Drain Extended MOSFET (DEMOS) [92, 93, 94, 95]
- Lateral double-diffused MOSFET (LDMOS) [96, 97, 98]
- Vertical double-diffused MOSFET(VDMOS) [99, 100]

2.2.2.1 Drain-Extended MOSFET (DEMOS)

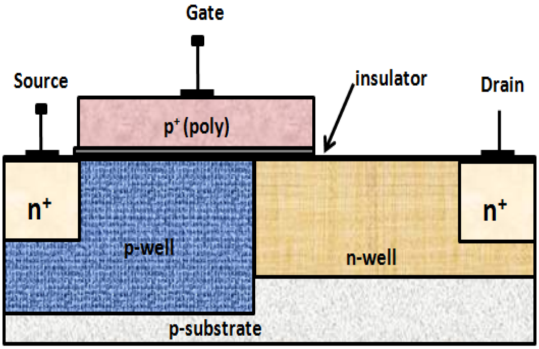


Figure 2.13: Schematic of the DEMOS device

Although modern VLSI circuits are operating under voltage conditions of $1.8\,V$ and below, circuits requirements often call for design and interface with other circuits operating at $3.3/5\,V$ or even higher. Such circuits can be input/output interface circuits with various off-chip system components like power management switches that regulate power from battery or system supplies, analog input circuits conditioning transducer signals, or output analog drive functions for speakers or other actuators. System design demands all of these functions in one monolithic chip so as to reduce system size and increase reliability. The solution to these is to use drain extended (DEMOS) transistors [94, 95] that can operate at high voltages without significant loss of performance and without added process complexity. Furthermore, the use of DEMOS instead of e.g. cascaded circuits or other circuits methods offers significant die size area and less power consumption. The LDD extension used in DEMOS increases the drain breakdown voltage by reducing the electric field under the gate at the drain end of the device. On the other hand, the difficulty here has to do with achieving the goal with a higher than the very thin 4 *nm* oxides can normally withstand, without the luxury of a LOCOS oxide used in conventional DE style devices for the poly to terminate on. Figure 2.13 shows the schematic representation of n-type DEMOS device. These devices are generally used for 5 V operation range especially as in input/output interfaces [101].

2.2.2.2 Lateral double-Diffused MOSFET (LDMOS)

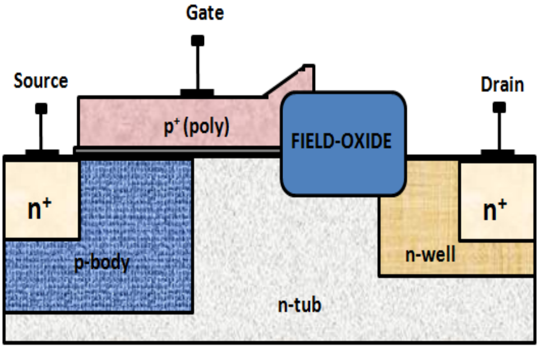


Figure 2.14: Schematic of LDMOS device

In Figure 2.14, the Lateral double-Diffused MOSFET (LDMOS) is introduced. The LDMOS device architecture, which actually originated from DEMOS/LDD-MOS, has much higher breakdown voltage than DEMOS architectures. This kind of devices are useful in high-voltage switching due to their switching speed and relative simplicity in processing [102]. There are many variations of LDMOS devices [96, 97, 98, 103]. The device shown in Figure 2.14 is a reduced surface (RESURF) field LDMOS device and is used for $20 - 100\,V$ applications such as switch-mode power supplies and power amplifiers. The channel in the device is created using double diffused process and thus it has non-uniform doping. The effective gate length is shorter than the physical length of the gate electrode. The maximum drain-source voltage is determined by the breakdown voltage of the pn junction, which is limited by the n-layer doping, thickness and field at the junction edge [101]. The elctric field in the LDMOS near the silicon surface is considerably lower in comparison with conventional MOS or DEMOS. However, the maximum field still remains on the surface and avalanche breakdown may occur here [104]. This field can be remarkably reduced by the use of thick oxide or field plate (bird's beak shaped LOCOS field oxide - FOX) and this is known as Kirk effect. To reduce the on-resistance in LDMOS, the length of the field plate should be as small as possible. The effect of field plate on LDMOS characteristics has been studied thoroughly in literature [105, 106]. The on-resistance can also be decreased by using the ion-implantation in the drift region [107]. The field plate also shields the gate from the drain voltage, thus minimizing the drain to gate capacitance, which improves the RF signal gain. The pn junction and the field plate form a fairly uniform field between the gate and the drain resulting in better breakdown voltage.

2.2.2.3 Vertical double-Diffused MOSFET (VDMOS)

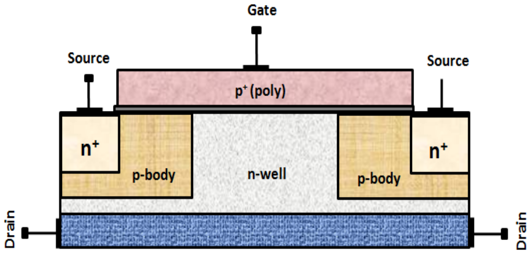


Figure 2.15: Schematic of VDMOS device

A means to reduce the continually increasing chip size is brought by the VDMOS transistor [108]. Figure 2.15 shows the schematic representation of n-type VDMOS device [99, 100]. Since in these devices, the drain is at the back surface, a variety of junction edge termination schemes can be utilized at the perimeter of the die. However, the channel itself remains on the top surface and thus the current flows laterally through the channel and vertically through the lightly doped drift region. The channel in the device is created using double diffused process and thus it has lateral non-uniform doping. The VDMOS device sacrifies speed for lower on-resistance and denser high-voltage layout due to large gate-drift overlap.

2.2.3 HV-MOSFET Operation

The following analysis will focus on the operation of LDMOS device (Figure 2.14) which is the one used for the purposes of this Thesis. The electrical behavior of this device has to be understood and the first way to accomplish this is the segregation of the device in specific parts as in Figure 2.16. The LDMOS device is distinguished into two parts - the intrinsic MOS or Low-Voltage (LV) or channel part and the drift region part. The intrinsic MOS is located between the source and the metallurgical junction or the so-called K-point of the device while the drift region extends from the K-point to the drain of the device. L is the length of LV channel part while L_{OVD} is the gate overlapped length in drift region. Particularly, L_{OVD} is a part of channel that is extended in the drift region part and it plays a significant role in LFN as will be explained later in this Thesis. The seperation described above is not real, it just used for a better understanding of the operation of the transistor [109].

The K point is of great interest from characterization and modeling point of view both for DC and LFN analysis, the potential at this point is defined as V_K. It was recently proved that the LV part of HV-MOSFET behaves like a low-voltage MOS device [110] where the K point becomes the intrinsic drain of the intrinsic MOS transistor. Potentials at K point and gate determine the operating conditions of the "inner" MOS device. It has been shown that V_K remains low no matter how much V_G and V_D are increased (Figure 2.17).

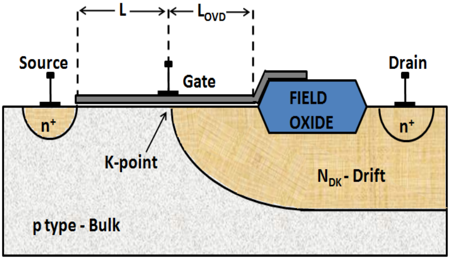
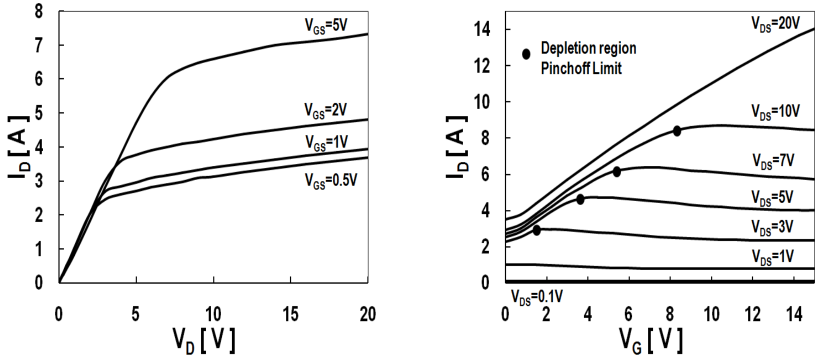


Figure 2.16: Detailed representation of LDMOS device

From Figure 2.17a, it can be shown that the value of V_K remains low even when V_D gets very high. This makes sense since the drift part of the device is designed to sustain the high voltages applied on the drain and thus the voltage drop on the intrinsic MOS is normally limited. From Figure 2.17b, it can be assumed that for constant V_D, V_K potential increases with V_G initially but after reaching a peak it decreases. In more detail, when drain potential is low the current through the device is also low and in this case HV transistor behaves as an LV transistor since drift region is not still activated. Thus, the electron charge is accumulated at the surface of the oxide as the gate voltage increases. Since K point is a surface point, its potential increases with V_G (Section 2.1.2.1). When V_D also increases, a depleted area is created in the drift part. The major part of drain voltage drops on this depleted area, so for constant V_D, V_K increases with the increase of V_G. But, and here is the contribution of drift part, in the same time the increase of gate potential creates an accumulation area at the surface of the thin oxide at the drain size. When this accumulation charge is high enough to counterbalance the depleted part of the drift zone and to create a conductive channel, V_K reaches its maximum value. Once this channel is formed in the drift region, the potential lines redistribute all over the length of the current path from source to drain and as a result this redistribution at constant drain potential leads to the decrease of V_K [109]. The simulations in Figure 2.17, were performed with the recently established charge-based HV model [31, 32].



(a) V_K vs. V_D (b) V_K vs. V_G

Figure 2.17: K point potential behavior

2.2.4 Basic High-Voltage MOSFET Effects

High-voltage devices show some special effects due to high electric field inside the device such as self-heating, quasi-saturation and impact ionization effects. In fact, some of these effects (self-heating and impact ionization) take part also in low-voltage MOSFETs when channel length is significantly decreased and so electric field becomes quite high. As far as saturation is concerned it can be divided into two parts; the one that takes place in the intrinsic MOS and is similar with the standard MOSFET and the quasi-saturation that takes place in the drift region part. Moreover, there is another special effect due to different device processes between HV and standard MOSFET that has to be addressed and this is the lateral non-uniform doping of HV devices.

Quasi-Saturation Effect

The quasi-saturation effect [111] is one of the unique effects observed in HV-MOSFETs. In order to understand this effect, saturation mechanisms in HV-MOS should be discussed firstly[112]. Saturation in output current characteristic can occur because of the following three mechanisms:

1. Pinch-off in the channel: For a fixed gate voltage, if drain voltage is increased, the channel gets depleted and current saturates. This effect is called pinch-off and has already been introduced in standard long channel MOSFETs as the normal saturation mechanism. In HV devices, the channel pinch-off is generally observed at low V_G values (Figure 2.18 $V_G = 2.5\,V$).

2. Velocity saturation in the channel: If the lateral electric field in the channel is more than the limit of the so-called critical field, the velocity of the electrons get saturated and thus there is no further increase in the current even if drain voltage continues to increase. This velocity saturation effect is very common phenomenon in short channel MOSFETs. In HV-MOSFETs, this effect is usually observed for medium to high V_G values (Figure 2.18 $V_G = 2.75..3.5\,V$ at $V_{DS} = 20\,V$). In this case, the output characteristics are equally distanced for equal increase in V_G.

3. Velocity saturation in the drift region or quasi-saturation: Another saturation mechanism may take place because of the saturation in the drift region while intrinsic MOS is still not saturated. In reality current is not saturated in this case. If drift is velocity saturated and intrinsic MOS operates in linear region, the increase in V_G does not increase current level significantly and gate bias has no or little effect (Figure 2.18 $V_G = 3, 3.5, 4\,V$).

All or any two of the above effects may occur simultaneously and thus may not be easily distinguished from each other.

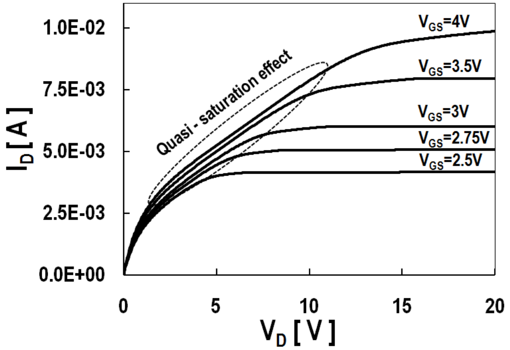


Figure 2.18: Output characteristic of a HV-MOSFET

Self-Heating Effect

The self-heating effect [109, 113, 114, 115, 116, 117, 118] represents the heating of the device due to its internal power dissipation. This effect appears when high levels of power are attained in the device which leads to an increase in the internal temperature of the device and has as a result the current to decrease as shown in Figure 2.19. This decrease is caused by the decrease of mobility due to the high temperature. Generally, this increase of temperature affects the threshold voltage and the velocity saturation effect, apart from mobility.

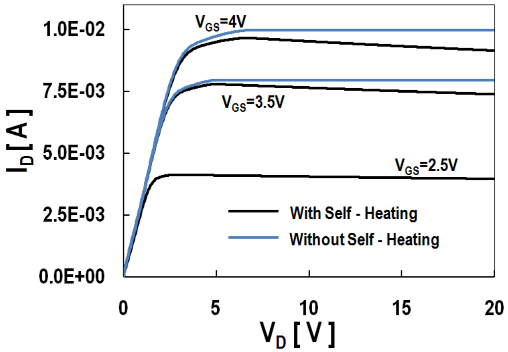


Figure 2.19: self-heating effect

Impact Ionization Effect

Impact ionization effect also takes place in standard LV-MOSFETs [2]. Longituidinal electric field in channel from source to drain is increasing with the increase of V_{DS}. Its peak value is at the drain to channel junction and depends on V_{DS} and L. At this critical value (E_{CRIT}) the velocity of the carriers gets saturated (Velocity Saturation). In fact, the carriers continue to acquire kinetic energy but their velocity is randomized by the excessive collisions such that their velocity along the field direction is not increased, but their kinetic energy does. Depending on the statistics of this scattering, a small fraction of overall carriers acquires a significant amount of energy and become the so-called hot carriers. The higher the field the higher the proportion of hot carriers. In MOSFETs, high fields occur in saturation in the pinchoff region. For such high fields, the cool electrons enter pinchoff region, get heated by the field and some of them (hot carriers) acquire enough energy to create impact ionization with silicon atoms with a result new electrons and holes to be created. The new electrons join channel electrons and move towards drain (I_{DS}) while the holes are pushed by the depletion field to the substrate so impact ionization or substrate current (I_{DB}) is created. This current is proportional to the number of electrons per unit time which in turn is proportional to V_{DS}. For a given V_{DS} when V_{GS} increases, I_{DS} increases as well as I_{DB} since electrons' flow in the channel is higher so hot carriers' proportion is also higher. Further increase of V_{GS} has as a result the increase of pinchoff potential V_P (Equation 2.20) and so, after a point when the device gets out of pinchoff region, the fields get decreased and the I_{DB} becomes negligible.

Impact ionization effect in HV devices is affected by both the channel and the drift region. At low currents where LV part is active, the effect is activated as described above for the standard MOSFETs. At high currents, hot carrierrs are generated near the drain end in the drift region. That is the reason that there is an increase in I_{DB} at higher V_{GS} (Figure 2.20).

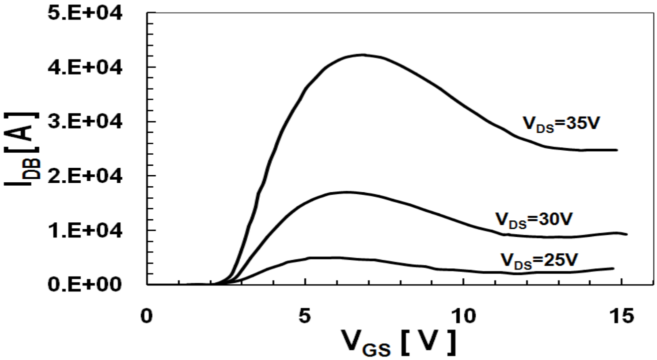


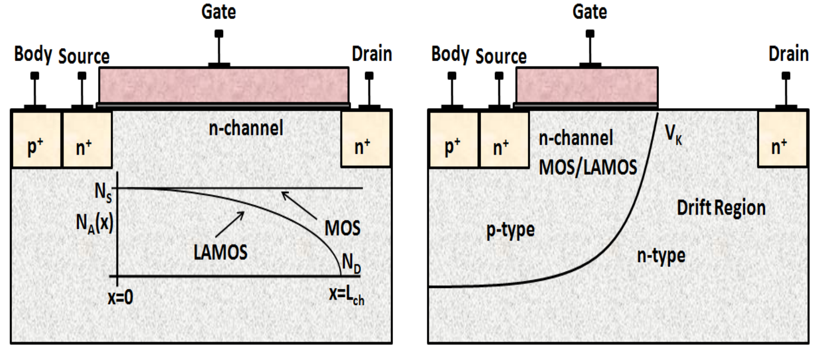
Figure 2.20: Impact ionization effect

Lateral Non-Uniform Doping Effect

As far as AC behavior of HV-MOSFETs is concerned, lateral non-uniform doping in the channel of HV-MOSFET affects the capacitances depending on the bias regime. According to Figure 2.21a, a conventional MOS device could be uniformly doped or lateral non-uniformly doped (LAMOS). In uniform MOS device the doping at source and drain size (N_S, N_D) are equal while in LAMOS there is a decrease of doping towards the drain size. The lateral doping gradient is approximated by the complementary error function [101, 119, 120]:

$$N_A(x) = N_S.erfc\left[k_n(\xi)\right] \tag{2.42}$$

where $\xi = \frac{\chi}{L_{ch}}$ is the normalized position along the channel and k_n is a parameter representing the doping gradient. Higher k_n means sharp decrease in the doping level from source to drain and vice-versa. In Figure 2.21b, a HV device is shown which doping is also determined by the LV channel part which can again be uniform or LAMOS as explained above. Usually and due to fabrication reasons, HV devices have lateral non uniform doping. This technique was first used to SOI MOSFETs since it gives some solutions to short channel effects while it improved device performance by changing doping levels in different length ratios of channel region in lateral direction.



(a) LV-MOSFET with (LAMOS) and without (MOS) lateral non-uniform doping

(b) HV-MOSFET with and without lateral non-uniform doping

Figure 2.21: Lateral non-uniform doping in both LV and HV-MOSFETs

2.2.5 Charge-Based High-Voltage Model

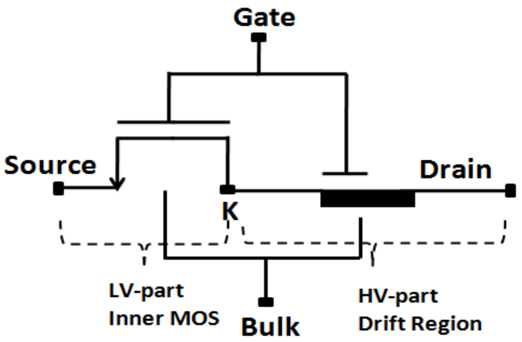


Figure 2.22: Schematic of HV-MOSFET compact model

The accurate compact modeling of HV-MOSFETs has always been a great challenge in the device modeling community from the onset of the development of these devices in the early ’70s. The first modeling approaches were then introduced [121]. In the following decades many attempts have been reported to model the different architectures of HV-MOSFETs, most of which are sub-circuits models [122, 123] and not physical ones. Lately, enough compact models have been proposed but they are not considered to be complete [124, 125, 126, 127]. The first attempt for a charge-based modeling of HV device is found in [101, 128, 129], where the intrinsic part modeling is based on EKV model adjusted properly so as to cover the specific characteristics of the intrinsic MOS such as the lateral non uniform doping [31, 101, 119, 120] while the drift region is modeled as a scalable drift resistance [130, 131]. An important aspect of this model is the scalability as well as the correct modeling of special effects such as quasi-saturation and self-heating. The usage of a bias-dependent resistance to model drift region offers fast convergency but fail to capture the physical phenomena that appear. This was addressed in [32, 132] where a new full charge-based model for drift region of HV-MOSFETs was proposed.

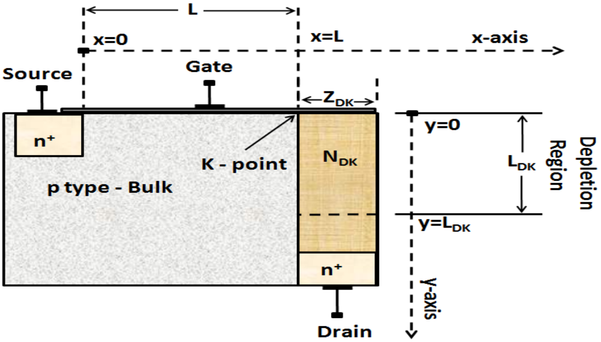


Figure 2.23: Two dimensional approach of a HV-MOSFET

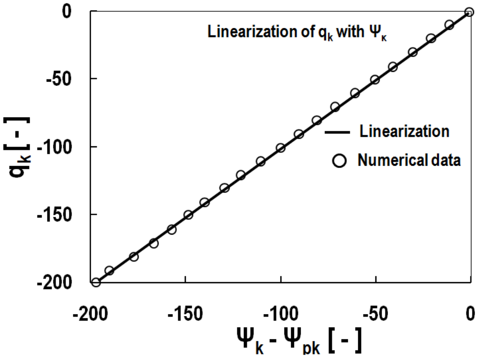


Figure 2.24: Linearization of q_k and ψ_k

As mentioned above, a charge-based approach is applied both in the intrinsic part and the drift region. The, in series combination of the above two charge-based models are shown in a simplified way in Figure 2.22. As far as the LV part of the device, K-point is considered to be the inner drain node and the fundamental equations of this EKV-like model are (Section 2.1.4):

$$2q_{s(k)} + lnq_{s(k)} = u_P - u_{s(k)} \tag{2.43}$$

$$i = \frac{I_{KS}}{I_{SPEC}} = [i_f - i_r] \begin{cases} i_f = q_s^2 + q_s \\ i_r = q_k^2 + q_k \end{cases} \tag{2.44}$$

The physics-based compact model proposed for drift region [32, 132], considers this region as a simple one-dimensional problem, approach similar with charge-based LV model. It applies the charge sheet approximation and proves a linear relation between the charge in drift region and surface potential. The whole approach of the analysis is presented in Figure 2.23, where the x-axis is the inner LV-MOSFET and the y-axis represents the drift region. N_{DK}, L_{DK}, Z_{DK} are the doping, the length of depletion area and the thickness of drift region respectively. Width W is considered to be common in both parts.

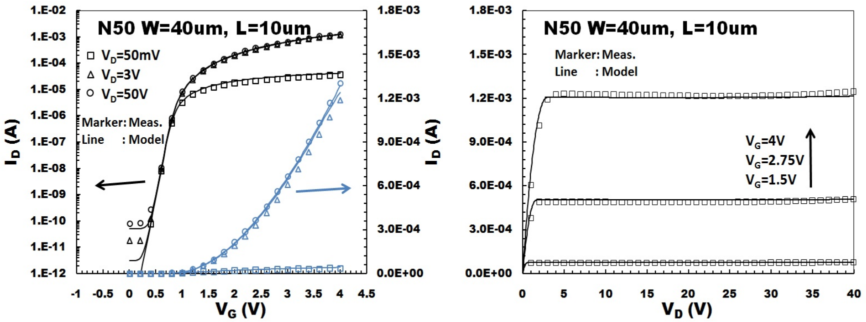
Normalizations of potentials and charges in drift region are defined with the same concept as in EKV model. As it can be observed in Figure 2.24, there is a linear dependence of normalized drift region charge under the K point, q_k and the surface potential ψ_k at the same point:

$$q_k = n_k(\psi_k - \psi_{pk}) \tag{2.45}$$

where as in Equation 2.26, ψ_k, ψ_{pk} are the surface potential and pinchoff surface potential at K-point respectively and n_k is defined as the slope factor in the same point. If Poisson equation is applied in the drift region (y-axis) and due to charge conservation , the basic charge-voltage relationship that results is:

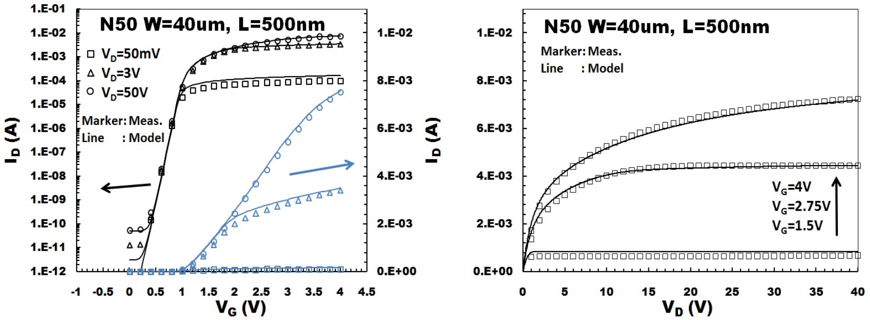
$$2\frac{-q_k}{2n_k} + ln\frac{-q_k}{2n_k} = u_{Pk} - u_k \tag{2.46}$$

which is quite similar with Equation 2.28. In Figures 2.25, 2.26, the IV part of the complete charge-based HV-MOSFET model [31, 32] seems to predict very well the DC behavior of both long and short $50\,V$ transistors from a $0.35\,\mu m$ HV-CMOS process for all regions of operation.



(a) (b)

Figure 2.25: Transfer a) and output characteristics (b) are shown for long 50 V transistors. I_D vs. V_G is shown in linear and logarithmic scale. Measurement (markers), model (lines).



(a) (b)

Figure 2.26: Transfer (a) and output characteristics (b) are shown for short 50 V transistors. I_D vs. V_G is shown in linear and logarithmic scale. Measurement (markers), model (lines).

Chapter 3

Low-Frequency Noise in MOSFETs

3.1 Introduction

Noise is considered a random process and in MOSFETs is associated with current or voltage fluctuations. As mentioned earlier, these fluctuations reduce the signal information, thus are considered undesirable. Due to this random nature, noise is classified as a stochastic signal which is characterized by its average power while the signal to noise ratio (SNR) is considered very important in electronic circuits. This significance of noise, makes the study and understanding of its fundamental characteristics, crucial. In the beginning of this chapter, the stochastic nature of noise will be presented and its main characteristics will be addressed. Following that, the noise sources in a MOSFET device will be introduced with focusing on basic principles of LFN and how it is related to generation-recombination mechanism. The last section of the chapter discusses 1/f noise modeling. A general methodology for noise modeling is first discussed and then the main contributions of this kind of noise such as carrier number fluctuations, mobility fluctuations and series resistance effects are introduced while existing modeling aproaches of these effects are presented and compared. After this, the new charge-based 1/f noise compact model [24, 33] based on the EKV compact model [25, 42] is presented. For the purpose of this Thesis, 1/f noise measurements were performed in our lab and the measurement set-up is described. Finally our new model is evaluated and tested with data from two different CMOS processes.

3.2 Noise as a Stochastic Signal

Figure 3.1 shows the current fluctuation of a resistor. This fluctuation takes place due to thermal effect and creates current noise in the device. Noise is a stochastic, statistical signal which means that its value can not be predicted at any time even if the past values are known. Because of the latter, noise in electronic devices and circuits can only be examined through long term observation of its behavior. Such study could lead to the construction of statistical models that can predict some important properties of noise such as its average power and its Power Spectral Density (PSD) from the frequency point of view [38].

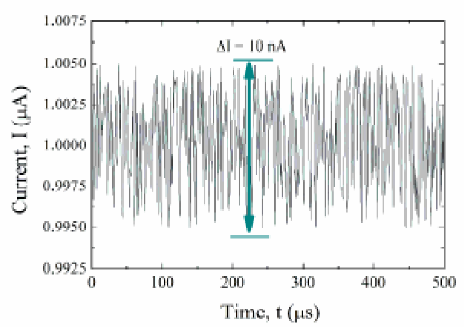


Figure 3.1: Current fluctuation in a resistor

Average power of noise can be defined as:

$$P_{av} = \lim_{T\to\infty} \frac{1}{T} \int_0^T x^2(t)dt \tag{3.1}$$

where $x(t)$ is a stochastic signal, noise in our case and P_{av} is expressed in V^2 rather than W in order to simplify calculations. The actual power delivered to a load can be easily calculated by dividing P_{av} with the resistance of the load. In frequency domain, noise spectrum (PSD) is used to characterize the average power the signal carries at each frequency. An easy way to calculate PSD as it has been mentioned earlier, is using the Fast Fourier Transform of the stochastic signal:

$$S(f) = \lim_{T\to\infty} \frac{|X(f)|^2}{T} \tag{3.2}$$

where $S(f)$ is the PSD of noise and $X(f)$ the FFT.

3.3 Noise Sources in MOSFETs

In this section the fundamental physical noise sources in a MOS device are presented. First of all, thermal noise is introduced the spectrum of which is independent to frequency. Shot noise at the gate of the MOSFET is also mentioned. Low Frequency Noise is dominant at lower frequencies below the corner frequency which is the frequency point where thernal noise and LFN meet, having equal PSDs (Figure 3.2). LFN consists of flicker (1/f) and, especially as device dimensions shrink, of generation-recombination (RTS) noise.

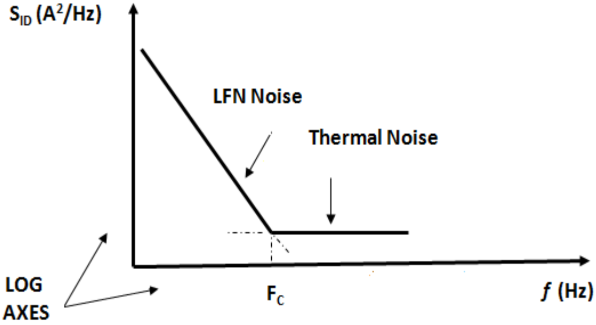


Figure 3.2: Drain current PSD in a MOSFET

3.3.1 Thermal Noise

Figure 3.1 exhibits the thermal noise in a resistor. This kind of noise, also called Nyquist or Johnson noise, is associated with the thermal random motion of charge carriers. MOSFETs also exhibit thermal noise due to local random fluctuations of the carrier velocity. A lot of research has been devoted to compact modeling of thermal noise in MOSFETs [1, 2, 133, 134, 135]. Apart from the long channel approximation, short channel phenomena have great influence on thermal noise such as velocity saturation (VS), channel length modulation (CLM) and carrier heating (CH) effects. In the EKV3 model, the impact of VS and CH on thermal noise is connected with the dimensionless critical field parameter λ_c (Equation 2.36) while as far as CLM is concerned, only the active region contributes to channel thermal noise [22, 23]. The total EKV3 approach of thermal noise is:

$$S_{id} = 4kTg_n\frac{I_{SPEC}}{U_T} \tag{3.3}$$

where K is the Boltzmann's constant, T is the Kelvin temperature and

$$g_n = \frac{2}{(1+\frac{2U_T(q_s-q_d)}{E_cL_{eff}})^2(q_s+q_d+1)} \times \left(\begin{array}{c} \frac{q_s^2+q_sq_d+q_d^2}{3} + \frac{U_T^2i^2}{E_c^2L_{eff}^2} + \frac{(\frac{2U_Ti}{E_cL_{eff}}+1)(q_s-q_d)}{4} + \\ +(\frac{2U_Ti}{E_cL_{eff}}-1)\frac{U_Ti}{2E_cL_{eff}}(q_s+q_d+1)ln\frac{q_s+\frac{1}{2}-\frac{U_Ti}{E_cL_{eff}}}{q_d+\frac{1}{2}-\frac{U_Ti}{E_cL_{eff}}} \end{array} \right) \tag{3.4}$$

Channel thermal noise described above is “white” which means is independent of frequency. But for RF operation, thermal noise in channel is capacitively coupled to the gate of the device leading to the called Induced Gate Noise or Non-Quasi-Static (NQS) noise. Induced gate noise is proportional to the square of frequency.

3.3.2 Shot Noise

Shot noise is another source of noise in MOSFETs which is connected with the gate leakage current [136]. In fact, it is associated to the direct current which flows across a potential barrier like a pn-junction. Shot noise is caused by the random fluctuation of the electric current due to the discrete nature of the electrons and does not depend on frequency. Its value is proportional to gate leakage current I_G and is given by:

$$S_{I_G^2,sh} = 2qI_G \tag{3.5}$$

3.3.3 Generation-Recombination (RTS) Noise

Generation-recombination noise is caused by trapping/detrapping mechanism in the MOSFET oxide. As it is known, drift and diffusion are the fundamental processes for creation of current through free carriers. The generation process involves the creation of free carriers, and the recombination process involves the trapping of these free carriers in defects. Low frequency noise in MOSFETs is strongly correlated with these carrier traps. Due to fabrication reasons, the dielectric oxide of a MOSFET contains local imperfections giving rise to traps. Because of these traps, a free carrier might be trapped and removed from the channel for a short time and then emitted back . In more detail, traps with energy levels significantly lower than quasi-Fermi level (EF) at the surface, are filled with carriers while traps with energy level significantly above EF are considered empty. Those traps with energy level difference of few KT above or below EF are the “crucial” traps. These have the probability of being active by capturing free carriers and then emitting these carriers back to the conduction band. The emission of the free carrier after a short time occurs due to the thermal energy of crystal lattice. This is the trapping/detrapping mechanism which consists of a series of independent discrete events. Each such trapping/detrapping event causes fluctuations in number as well as in mobility of free carriers and as a result channel current is also fluctuated which leads to the creation of generation-recombination noise. Each single trapping/detrapping process leads to a Lorentzian-like PSD or Random Telegraph Noise (RTS) in time domain [1, 137, 138, 139, 140, 141, 142, 143, 144]. In Figure 3.3, a free electron being trapped is shown.

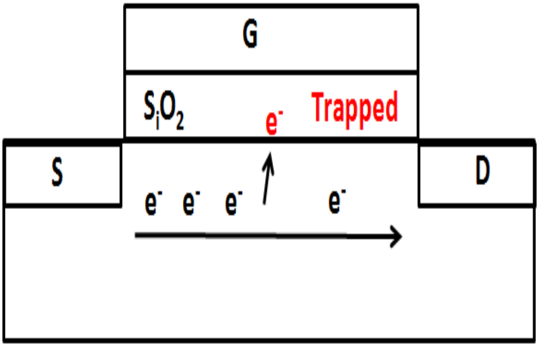


Figure 3.3: An electron being trapped in a MOSFET oxide

3.3.4 Flicker Noise

As it has been stated, flicker noise has a PSD inveresely proportional to frequency and that is the reason it is also called 1/f noise. As it can be seen in Figure 3.2, it dominates at low frequencies below the corner frequency f_c. Because of both higher f_c and dimensions shrinking in modern CMOS technologies, flicker noise which scales inversely proportional to the gate area, becomes really significant. Three are the basic main causes to this kind of noise; carrier number fluctuation effect which connects flicker with RTS noise, mobility fluctuation effect originating from variations of carrier mobility and the series resistance fluctuation effect. A significant amount of modeling approaches of 1/f noise are available in literature but things remain quite ambiguous. Modeling of flicker noise is quite complicated as the rest of this Thesis will prove. Nevertheless, a basic, simple equation describing 1/f noise can be [145]:

$$S_{I_D^2} = K \frac{g_m^{EF}}{C'_{OX} W L f^{AF}} \tag{3.6}$$

where g_m is the device transconductance, EF is a parameter quite close to 2, AF is a parameter determining the slope of the spectrum versus frequency and ideally is 1 but can take values from 0.8 up to 1.2 and K is a constant which depends on device and process. The inversely proportional behavior of flicker noise with gate area (WL) is apparent in Equation 3.6.

3.4 Flicker Noise Modeling in MOSFETs

3.4.1 General Considerations

As it has been stated before, drain current in a MOSFET has noise spectrum that consists of two regions. Flicker noise is dominant below the corner frequency f_c and thermal noise prevails for higher frequencies with a white spectrum independent of frequency. Local random fluctuations of carrier mobility μ or carrier number N can be considered the origin of low frequency noise in MOSFETs. These fluctuations can be caused by statistical perturbation in both μ and N and can be modeled by adding a random current to the local DC current which then propagates to the terminals causing noise through these fluctuations. Any noise source can be described by a local noise source which depends on channel position and its PSD can be calculated by integration of the local noise source across the channel. Compact noise modeling in MOSFETs can be considered as the sum of two parts. Microscopic part which has to do with the definition of a local noise source in an elementary slice of the channel based on the stochastic nature of noise and the macroscopic part which involves the calculation of the total noise in a terminal through the integration process mentioned above. It is important to mention here that local noise sources located in the channel can be considered small as well as uncorrelated and as a result, the whole noise analysis that follows can be considered linear and furthermore the principle of superposition by adding the effects of all local noise sources can be applied under these circumstances [22]. Local noise sources added in device channel can be either current or voltage sources. Generally there are two ways of representing noise, drain current noise $S_{I_D^2}$ or output referred noise and gate voltage noise S_{VG} or input referred noise. Usually, output noise is measured as in this work and input noise is calculated through the simple equation:

$$S_{VG} = \frac{S_{I_D^2}}{g_m^2} \tag{3.7}$$

Figure 3.4 illustrates these two representations of noise. Three methods have been poposed for compact noise modeling:

- Langevin or Klaassen-Prins [135, 146, 147, 148]
- Equivalent small-signal approach [81, 134, 149, 150]
- Impedance field method [151, 152]

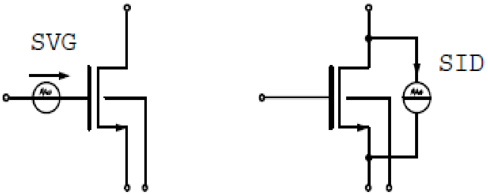


Figure 3.4: Input referred noise voltage source and equivalent output referred noise current source

In long channel approximation, all the above three methods give the same results but this is not the case in short channel where mobility starts to depend on electric field. Generally speaking, this mobility degradation has to be taken into account by noise modeling approaches. Focusing on flicker noise, a thorough analysis and comparison of different approaches which are extracted from the above three general methods, is carried out in the following section before the new 1/f noise model covering all the short channel effects is presented. Carrier number fluctuation effect caused by the fluctuations in carrier density N, mobility fluctuation effect caused by fluctuations in carrier mobility μ and series resistance effect are the main contributors to 1/f noise in a MOSFET. Initially, a general noise modeling methodology which is used in EKV3 model is proposed which can then be applied for the extraction of the new 1/f noise model in the rest of the chapter. As stated above, before the implementation and evaluation of the new model, different contributions of flicker noise are addressed with the various modeling approaches that are available in bibliography so far.

3.4.2 A Generalized Noise Modeling Methodology in MOSFETs - EKV3 Approach

In this section, a general noise analysis will be derived which then can be applied in 1/f noise modeling presented later in this chapter [22]. This analysis can also been applied in thermal noise modeling which is not an objective of this Thesis. Under the assumption that the channel is noiseless apart from an elementary slice between positions x and Δx as it is shown in Figure 3.5, the microscopic noise coming from this slice of the channel can be modeled as a local current noise source δI_n with a PSD $S_{\delta I_n^2}$ which is connected between x and Δx in parallel with the resistance of the slice ΔR (Norton equivalent). The transistor then can be split into two noiseless transistors M1 and M2 on each side of the local current noise source at the source and drain side ends with channel lengths equal to x and $L - x$ respectively. Since the voltage fluctuations on parallel resistance ΔR are small enough compared to thermal voltage U_T, small signal analysis can be used in order to extract a noise model according to which, M1 and M2 can be replaced by conductances G_1 and G_2 equal to $G_1 = G_{md1}$

and $G_2 = G_{ms2}$. The total channel conductance comes from the series connection of G_1 and G_2 as: $\frac{1}{G_{ch}} = \frac{1}{G_1} + \frac{1}{G_2}$.

The fluctuation of the current due to the local current noise source at the drain side δI_{nD} and its corresponding PSD, $S_{\delta I^2_{nD}}$, are given by Equations 3.8, 3.9.

$$\delta I_{nD} = G_{ch} \Delta R \delta I_n \tag{3.8}$$

$$S_{\delta I^2_{nD}}(\omega, x) = G^2_{ch} \Delta R^2 S_{\delta I^2_n}(\omega, x) \tag{3.9}$$

$$S_{\Delta I^2_{nD}}(\omega) = \int_0^L G^2_{ch} \Delta R^2 \frac{S_{\delta I^2_n}(\omega, x)}{\Delta x} dx \tag{3.10}$$

The PSD of the total noise current fluctuation at the drain side $S_{\Delta I^2_{nD}}$ [1] due to all different sections along the channel is obtained by summing their elementary contributions $S_{\delta I^2_{nD}}$ assuming that the contribution of each slice at different positions along the channel remains uncorrelated (Equation 3.10).

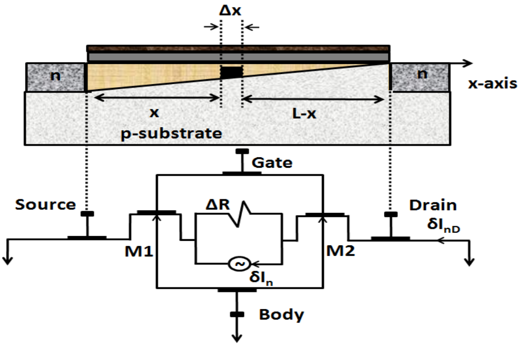


Figure 3.5: MOSFET cross-section with a local current noise source

3.4.3 Carrier Number Fluctuation Effect

3.4.3.1 Basic Physics-Relation with RTS Noise

The carrier number fluctuation theory (ΔN) [153, 154, 155, 156, 157, 158] first proposed by McWhorter [159], is strongly connected with generation-recombination noise and is caused by the random trapping/detrapping of charge carriers into or from traps located into the oxide interface. According to the principles of generation-recombination mechanism presented before, each trapping/detrapping process from a single trap leads to an RTS in time domain which results in Lorentzian-like PSD [1, 137]. How and under what circumstances, the superposition of these spectra can

---

[1] $S_{\Delta I^2_{nD}}$ will be replaced by $S_{I^2_D}$ in A^2/Hz in the rest of this Thesis for simplicity

create 1/f noise will be presented below. It is important to mention here the usage of RTS noise as a characterization tool for the quality or reliability of MOSFETs. More particularly, important information for the oxide quality can be provided by characterising the oxide traps through RTS noise analysis [160, 161, 162, 163, 164].

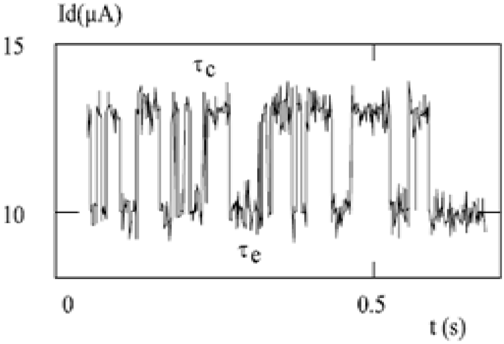


Figure 3.6: Drain current RTS noise in time domain

The trapping/detrapping approach assumes a distribution of trapping times that arise from the transition of electrons from the semiconductor surface to traps located in the oxide [139]. Each trap is characterized by a relaxation time τ determined by the mean time needed for getting captured τ_c and the mean time needed for getting emitted τ_e (Figure 3.6) and claculated as:

$$\tau = \frac{1}{\frac{1}{\tau_c} + \frac{1}{\tau_e}} \tag{3.11}$$

For each trap, the observed current fluctuation would resemble an RTS with two possible states high and low where the two time constants referred above τ_c and τ_e correspond to the mean high and mean low time. A Lorentzian-like PSD is shown in Figure 3.7 and such spectra dominate in today's very small area transistors where the number of traps is quite low and an individual carrier trapping can be observed [162, 165]. The main characteristics of such a PSD are the plateau A below f_c and the $1/f^2$ behavior above f_c. The equation describing this kind of PSD is:

$$S_{I_D^2} = \frac{A}{\left(1 + \frac{f}{f_c}\right)^2} \left(A^2/Hz\right) \tag{3.12}$$

The fundamental principle of generation-recombination noise declares that a trap is an energy state in band gap with an energy level between conduction and valence level [144]. When the energy level of a trap approaches the Fermi level (EF) then $\tau_c = \tau_e$ and the activity of trap becomes maximum meaning that the probability of capturing or releasing an electron becomes maximum. The RTS caused by a single trap can be created by two ways. Firstly, the captured electron takes no further part in the conductance process thus there is a fluctuation in the number of carriers N and secondly the electron capture will make the trap more negatively charged and this modulates the position in the channel. The latter known as Coulomb scattering effect causes a fluctuation in the mobility of the carriers μ and is much more intense than simple carrier number fluctuation effect [144].

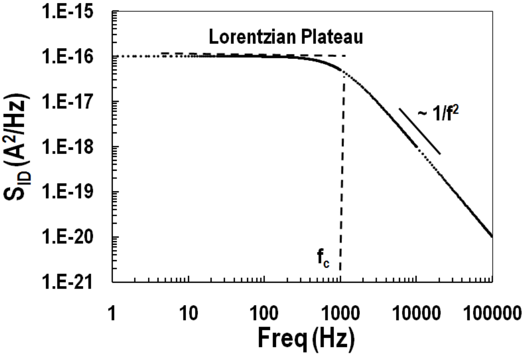


Figure 3.7: Lorentzian PSD

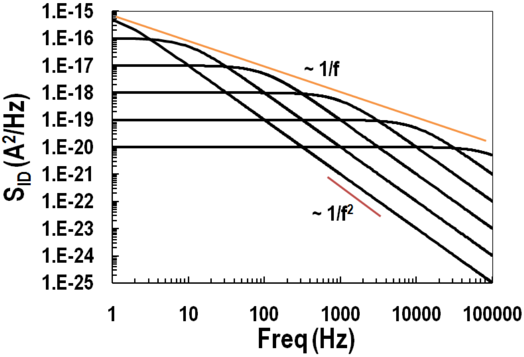


Figure 3.8: Superposition of 5 Lorentzians gives 1/f

While Lorentzian-like PSDs dominate for small area devices, in larger MOSFETs 1/f noise behavior prevails. Since in both cases, the basic principle creating noise is the trapping/detrapping effect, how is this 1/f shape is obtained? The answer is that the superposition of many uniformly positioned Lorentzians, results in 1/f spectrum as it can be observed in Figure 3.8. In order to have uniformly positioned

Lorentzians, the distribution of their time constants should be uniform over an extensive range of frequencies as well. In order to extend this to ten decades, the spread in time constants must cover many orders of magnitude. Tunelling in a MOSFET oxide could account for relaxation times distributed between 10^{-5} to $10^{8}\,sec$. McWhorter [159] proved that a uniform spatial distribution of oxide traps near the interface will give rise to an appropriate distribution of time constants which if they added up, they form an 1/f noise spectrum [154, 157, 166, 167, 168, 169].

The dominant flicker noise source in MOSFETs is the group of traps located at very small distances from the interface (0 to $3\,nm$) [170]. If the density of these traps is uniform then $AF = 1$ which means that there is an ideal 1/f shape in the PSD, but if the added Lorentzians do not have a constant proportion placement, AF varies with frequency. If $AF < 1$ indicates that the trap density is decreasing deeper in the gate oxide while if $AF > 1$ is increasing [171].

3.4.3.2 Existing Approaches

Two main approaches for modeling carrier number fluctuation effect (ΔN) in MOSFETs are available in literature. The Langevin method [170, 172, 173, 174, 175] and the flat band perturbation technique (FBP) [176, 177, 178, 179, 180, 181, 182]. Both of them are derived from McWhorter theory [159] and while for linear region operation the two methods coincide, in saturation region they give different results. FBP technique which is widely used in research labs and industry, is derived with taking into account approximations that are valid only in ohmic region and thus it errors under higher drain voltage operation. The main difference of Langevin and FBP approaches lies on the fluctuations of number of carriers and not in fluctuations of mobility due to Coulomb scatteribng effect as it will be proved analytically below. Even the Langevin method is not reliable for shorter channel lengths where short channel effects such as velocity saturation (VS) and channel length modulation (CLM) affect 1/f noise.

The thorough analysis is presented below starting with the generalized noise modeling approach introduced before for EKV3 (Section 3.4.2). After reaching a general charge-based formulation in order to be compatible with the EKV3 model, both Langevin and FBP methods are analyzed in a charge-based formulation with clarifying their main differences. After that, a complete approach is derived with taking into account the influence of short channel effects such as VS and CLM on ΔN effect and this is the approach which is implemented in our recently established 1/f noise compact model for standard MOSFETs [24, 33]

If we consider a slice of the channel between x and $x+\Delta x$ as in Figure 3.5, and if a number of carriers gets trapped at the position x, then the relative current fluctuation is given by:

$$\frac{\delta I_D(x)}{I_D} = \frac{\delta N}{N} + \frac{\delta \mu}{\mu} \tag{3.13}$$

where $N(x) = -Q'_I(x)/q$ is the number of carriers per unit area with Q'_I the inversion charge per unit area and q the electron charge. The first term of Equation 3.13 $\frac{\delta N}{N}$ refers to carrier fluctuation while the second term $\frac{\delta \mu}{\mu}$ shows the mobility fluctuation which is caused by the influence of trapping/detrapping mechanism on the scattering mechanism. This mobility fluctuation depends on the number of trapped charges per unit area N_t according to [174, 183]:

$$\frac{1}{\mu} = \frac{1}{\mu_0} + \tilde{\alpha}_c N_t = \frac{1}{\mu_0} + \alpha_c |Q'_t| \tag{3.14}$$

where $Q'_t = -qN_t$ is the trapped charge density per unit area, N_t is the trap density in cm^{-2} and $\alpha_c \triangleq \tilde{\alpha}_c/q$ is the Coulomb scattering coefficient which is about 10^4 Vs/C for electrons and 10^5 Vs/sec for holes in silicon [174, 183, 184, 185].

Accounting for Equation 3.14, Equation 3.13 can be transformed as:

$$\frac{\delta I_D(x)}{I_D} = (\frac{1}{N}\frac{dN}{dN_t} + \frac{1}{\mu}\frac{d\mu}{dN_t})\delta N_t = (\frac{1}{N}\frac{dN}{dN_t} - \tilde{\alpha}_c \mu)\delta N_t \tag{3.15}$$

δN, δN_t can be related if the following is taken into account. The fluctuation of the trapped charge $\delta Q_t^{'}$ can cause a variation in the surface potential $\delta \Psi_S$ which is responsible for a change in all charges that depend directly on surface potential such as the inversion, the depletion and the gate charge. Due to charge conservation principle [170]:

$$\delta Q'_G + \delta Q'_B + \delta Q'_I = -\delta Q'_t \tag{3.16}$$

Each of these charge fluctuations of Equation 3.16 can be related to $\delta \Psi_S$ according to [170]:

$$\begin{aligned} \delta Q'_G &= -C_{OX}^{'} \delta \Psi_S \\ \delta Q'_B &= -C'_D \delta \Psi_S \\ \delta Q'_I &= -C'_I \delta \Psi_S \end{aligned} \tag{3.17}$$

It follows that [170]:

$$R \triangleq \frac{\delta N}{\delta N_t} = |\frac{\delta Q'_I}{\delta Q'_t}| = \frac{C'_I}{C'_I + C'_{OX} + C'_D} \tag{3.18}$$

It can be proved [22] that $C_I^{'} = -Q_I^{'}/U_T$ so Equation 3.18 can be rewritten as [174]:

$$R \approxeq= \frac{Q'_I}{Q'_I - (C'_{OX} + C'_D)U_T} = \frac{Q'_I}{Q'_I - C'_{OX}U_T(1 + \frac{C'_D}{C'_{OX}})} \tag{3.19}$$

But from [22], $1 + \frac{C'_D}{C'_{OX}}$ is defined as the slope factor n so Equation 3.19 becomes:

$$R \approxeq= \frac{Q'_I}{Q'_I - nC'_{OX}U_T} \tag{3.20}$$

From the definition of specific charge $Q^{'}_{SPEC}$ (Equation 2.27), $-nC'_{OX}U_T = \frac{Q^{'}_{SPEC}}{2}$ so:

$$R = \frac{\delta N}{\delta N_t} \approx \frac{Q'_I}{Q'_I + \frac{Q^{'}_{SPEC}}{2}} = \frac{q_i}{q_i + 1/2} \tag{3.21}$$

where $q_i = \frac{Q^{'}_I}{Q^{i}_{SPEC}}$ is the normalized inversion charge. Using Equation 3.21 into Equation 3.15:

$$\frac{\delta I_D(x)}{I_D} = \left(\frac{1}{N} \frac{q_i}{q_i + 1/2} + \frac{\alpha \mu}{N_{SPEC}} \right) \delta N_t \tag{3.22}$$

where $N_{SPEC} \triangleq -Q_{SPEC}/q = 2KTnC^{'}_{OX}/q^2$ and $\alpha \triangleq \alpha_c \left(-Q_{SPEC}\right) = \tilde{\alpha}_c N_{SPEC}$ is a coefficient related to Coulomb scattering coefficient. Since

$$N = -\frac{Q_I}{q} \Longleftrightarrow \frac{1}{N} = -\frac{q}{Q_I} = -\frac{q}{q_i Q_{SPEC}} = \frac{1}{q_i N_{SPEC}} \tag{3.23}$$

then Equation 3.22 can become:

$$\frac{\delta I_D(x)}{I_D} = \left(\frac{1}{q_i + 1/2} + \alpha \mu \right) \frac{\delta N_t}{N_{SPEC}} \tag{3.24}$$

The corresponding PSD of the local noise source δI_n normalized to the square of the drain current is given by:

$$\frac{S_{\delta I_n^2}}{I_D^2} |_{\Delta N} = \left(\frac{1}{q_i + 1/2} + \alpha \mu \right)^2 \frac{S_{\delta N_t^2}}{N_{SPEC}^2} \tag{3.25}$$

The PSD of the trap charge density fluctuation $S_{\delta N_t^2}$ depends essentially on the trapping mechanism and is defined by [1, 153, 159]:

$$S_{\delta N_t^2} = \frac{KT \lambda N_T}{W \Delta x f} \tag{3.26}$$

where f is the frequency, λ is the tunneling attenuation distance ($TAD \approx 0.1\, nm$) [153, 184, 185], and

$$N_T = \frac{N_t}{\lambda KT} \tag{3.27}$$

is the oxide volumetric trap density per unit energy in $eV^{-1}cm^{-3}$ evaluated close to the Fermi energy level EF. Typical values of N_T extracted from measurements are from 10^{17} to $10^{16}\, eV^{-1}cm^{-3}$.

According to the generalized noise modeling methodology in EKV3 described above (Section 3.4.2), the fluctuation of the drain current due to an elementary section is given by Equation 3.9:

$$\frac{S_{\delta I_{nD}^2}}{I_D^2}\mid_{\Delta N}= G_{ch}^2\Delta R^2\frac{S_{\delta I_n^2}}{I_D^2}\mid_{\Delta N}=\left(\frac{\Delta x}{L}\right)^2\frac{S_{\delta I_n^2}}{I_D^2}\mid_{\Delta N}= \left(\frac{\Delta x}{L}\right)^2\left(\frac{1}{q_i+1/2}+\alpha\mu\right)^2\frac{S_{\delta N_t^2}}{N_{SPEC}^2} \tag{3.28}$$

where [22]:

$$G_{ch}^2\Delta R^2=\left(\frac{\Delta x}{L}\right)^2 \tag{3.29}$$

Combining Equations 3.10, 3.28, 3.29, the relative PSD of the total fluctuation of the drain current due to ΔN effect can be calculated as:

$$\frac{S_{I_D^2}}{I_D^2}\mid_{\Delta N}=\frac{1}{L^2}\int_0^L \Delta x\frac{S_{\delta I_n^2}}{I_D^2}\mid_{\Delta N} dx= \frac{1}{L^2}\int_0^L \Delta x\left(\frac{1}{q_i+1/2}+\alpha\mu\right)^2\frac{S_{\delta N_t^2}}{N_{SPEC}^2}dx= \frac{1}{L^2}\frac{S_{\delta N_t^2}}{N_{SPEC}^2}\int_0^L \Delta x\left(\frac{1}{q_i+1/2}+\alpha\mu\right)^2 dx \tag{3.30}$$

From Equation 3.26 and N_{SPEC} calculation, Equation 3.30 becomes:

$$\frac{S_{I_D^2}}{I_D^2}\mid_{\Delta N}=S_D\mid_{\Delta N}\frac{1}{4}\int_0^1\left(\frac{1}{q_i+1/2}+\alpha\mu\right)^2 d\xi= S_D\mid_{\Delta N}\frac{1}{4i_d}\int_{q_d}^{q_s}\left(\frac{1}{q_i+1/2}+\alpha\mu\right)^2(2q_i+1)\,dq_i \tag{3.31}$$

where

$$S_D\mid_{\Delta N}=\frac{q^4\lambda N_T}{KTWLn^2C_{OX}^{\prime 2}f} \tag{3.32}$$

and $\xi=\chi/L$, $dq_i/d_\xi=-i_d/(2q_i+1)$ are used for changing variables in the integral, i_d is the normalized current or inversion coefficient. Equation 3.31 gives as a first charge-based evaluation of the total drain current noise PSD normalized with squared drain current for carrier number fluctuation effect. The presence of the integral makes the analytical solution as well as its implementation in a compact model very tedious. The next step would be to solve this integral and the basic difference of Langevin and FBP methods is spotted at this point.

FBP Approach

Inversion charge is considered to be uniform in the channel in linear region operation where V_{DS} is very low. Under these circuimstances, Equation 3.31 becomes:

$$\frac{S_{I_D^2}}{I_D^2}\Big|_{\Delta N}= S_D\Big|_{\Delta N}\left[\left(\frac{q_s-q_d}{i_d}\right)^2+\left(\frac{\alpha\mu}{2}\right)^2+\frac{\alpha\mu}{1+q_s+q_d}\right] \tag{3.33}$$

Equation 3.33 is the charge-based approximation of FBP approach. In literature, FBP approach [177, 184, 186] is usually expressed by the following equation:

$$\frac{S_{I_D^2}}{I_D^2}\Big|_{\Delta N}=\frac{KTq^2N_T\lambda}{WLC'^2_{OX}f}\left(\frac{g_m}{I_D}\right)^2\left(1+\alpha_c\mu C'_{OX}\frac{I_D}{g_m}\right)^2 \tag{3.34}$$

For the validity of our analysis is very crucial to prove the equivalence between Equations 3.33 and 3.34. From the basic principles of the charge-based EKV3 current and transconductance model and from Equations 2.33, 2.34, 2.39, 2.40, it can be proved that:

$$\frac{g_m}{I_D}=\frac{G_{SPEC}}{I_{SPEC}i_d n}(q_s-q_d)=\frac{1}{nU_T}\left(\frac{q_s-q_d}{i_d}\right) \tag{3.35}$$

From Equation 3.34 with considering Equation 3.35 and taking into account that $U_T=KT/q$ and $\alpha=\alpha_c(-Q_{SPEC})$ we can end up in Equation 3.33:

$$\begin{gathered}\frac{S_{I_D^2}}{I_D^2}\Big|_{\Delta N}=\frac{KTq^2N_T\lambda}{WLC'^2_{OX}f}\left(\frac{g_m}{I_D}\right)^2\left(1+\alpha_c^2\mu^2C'^2_{OX}\left(\frac{I_D}{g_m}\right)^2+2\alpha_c\mu C'_{OX}\frac{I_D}{g_m}\right)^2=\\ \frac{KTq^2N_Tq^2(q_s-q_d)^2\lambda}{WLC'^2_{OX}fn^2K^2T^2i_d^2}\\ \left(1+\frac{\alpha^2q^2\mu^2C'^2_{OX}n^2K^2T^2i_d^2}{4n^2K^2T^2C'^2_{OX}q^2(q_s-q_d)^2}+\frac{2\alpha q\mu C'_{OX}nKTi_d}{2nKTC'_{OX}q(q_s-q_d)}\right)=\\ S_D\Big|_{\Delta N}\left[\left(\frac{q_s-q_d}{i_d}\right)^2+\left(\frac{\alpha\mu}{2}\right)^2+\frac{\alpha\mu}{1+q_s+q_d}\right]\end{gathered} \tag{3.36}$$

Langevin Approach

While in linear region FBP approach is considered valid since q_i is considered uniform, this is not the case in saturation and there Langevin approach gives the correct result. Solving the integral in Equation 3.31 gives us the following expression for total drain current noise PSD normalized with squared drain current for carrier number fluctuation effect [21, 22]:

$$\frac{S_{I_D^2}}{I_D^2}\Big|_{\Delta N}= S_D\Big|_{\Delta N}\left[\frac{1}{2i_d}ln\left(\frac{1+2q_s}{1+2q_d}\right)+\left(\frac{\alpha\mu}{2}\right)^2+\frac{\alpha\mu}{1+q_s+q_d}\right] \tag{3.37}$$

Mobility Degradation due to VS-CLM Effect

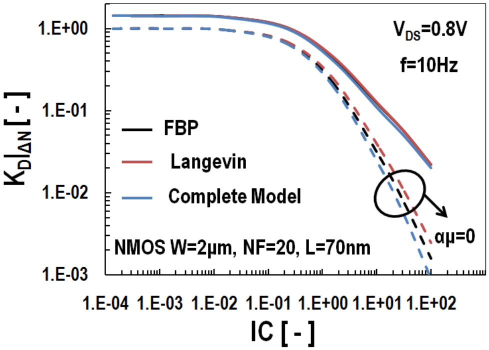
Langevin method presented above gives correct result both for linear and saturation regions but do not take into account the mobility degradation due to the VS and CLM effect. A correct DC model such as EKV3 will give the correct value of mobility μ and channel length L_{EFF} even for short channel devices but in the above Equations (3.33, 3.37), normalized drain current was calculated using Equation 2.34 which is valid in long channel MOSFETs. A correct formulation would use Equation 2.35 which takes into account VS effect. So [23, 33]:

$$\frac{S_{I_D^2}}{I_D^2}\mid_{\Delta N}= S_D\mid_{\Delta N}$$
$$\left[\frac{1}{2i_{d0}^2}\frac{i_{dlc}}{1+\lambda_c\left(q_s-q_d\right)}ln\left(\frac{q_s+0.5-\frac{\lambda_c}{2}i_{dlc}}{q_d+0.5-\frac{\lambda_c}{2}i_{dlc}}\right)+\left(\frac{\alpha\mu}{2}\right)^2+\frac{\alpha\mu}{1+q_s+q_d}\right] \tag{3.38}$$

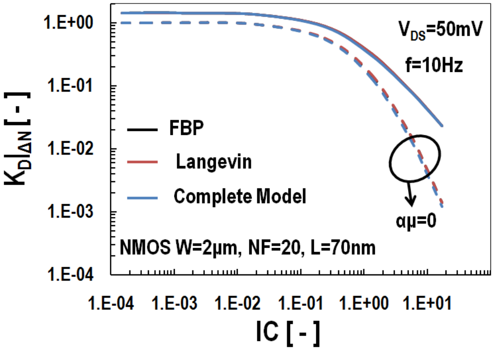
where $i_{d0}=i_d=i_{dlc}|_{\lambda_c=0}$. From Equation 2.35, λ_c equals to zero when critical field E_{CRIT} is very high and there Langevin method (Equation 2.37) is valid. This occurs in longer channel devices. Expression 2.38 provides a complete and detailed description of carrier number fluctuation effect in MOSFETs and it is the one included and applied in our recently established 1/f noise compact model for standard MOSFETs [24, 33] which will be presented later on in this chapter.

Important Conclusions

From the above analysis and introduction of different charge-based approaches for carrier number fluctuation effect for 1/f noise in MOSFETs (Equations 3.33, 3.37, 3.38), very important conclusions can be extracted. The bias independent term $S_D\mid_{\Delta N}$ is the same in all cases while the bias-dependent one which varies depending on the method will now on be symbolized as $K_D\mid_{\Delta N}$ [22]. The first attempts of modeling ΔN effect in MOSFETs either with Langevin or FBP method, had taken place without taking into account mobility fluctuations due to Coulomb scattering effect [170, 176, 177] and there the above equations are valid with product $\alpha\mu=0$. Mobility fluctuation due to Coulomb scattering effect was first studied and correlated with the total ΔN effect by [168, 173] and was then included extensively in modeling approaches [179, 182, 184, 185, 186, 187]. As mentioned before and is clear from the Equations 3.33, 3.37, 3.38, FBP and Langevin differences are spotted in the first term of $K_D\mid_{\Delta N}$ related with fluctuation of number of carriers in all three cases (FBP: $\left(\frac{q_s-q_d}{i_d}\right)^2$, Langevin: $\frac{1}{2i_d}ln\left(\frac{1+2q_s}{1+2q_d}\right)$, Complete model including VS-CLM effect on mobility: $\frac{1}{2i_{d0}^2}\frac{i_{dlc}}{1+\lambda_c(q_s-q_d)}ln\left(\frac{q_s+0.5-\frac{\lambda_c}{2}i_{dlc}}{q_d+0.5-\frac{\lambda_c}{2}i_{dlc}}\right)$), while the second and third term ($\left(\frac{\alpha\mu}{2}\right)^2+\frac{\alpha\mu}{1+q_s+q_d}$) related with mobility fluctuation due to Coulomb scattering is the same in all approaches. $K_D\mid_{\Delta N}$ shows an increase in strong inversion due to Coulomb scattering effect while in moderate inversion $\alpha\mu$ influence is nearly negligible [22, 184, 186].



(a)



(b)

Figure 3.9: $K_D\,|_{\Delta N}$ vs. IC for an NMOS with $W = 2\,\mu m$, $NF = 40$, $L = 70\,nm$ in a) saturation and b) linear region. FBP stands for Equation 3.33, Langevin for 3.37 and Complete Model for 3.38.

The behavior of $K_D\,|_{\Delta N}$ versus inversion coefficient IC is shown in Figure 3.9 for an NMOS device from $90\,nm$ CMOS technology node with $W = 2\,\mu m$, NF (number of fingers) $= 40$ and $L = 70\,nm$ at $f = 10\,Hz$ [24]. All the three approaches analysed before are shown for both saturation (Figure 3.9a) and linear (Figure 3.9b) region. It is clear that while FBP and Langevin method coincide for $V_{DS} = 50\,mV$, FBP underestimates 1/f noise for $V_{DS} = 0.8\,V$ confirming basic theory [23]. Moreover the complete model, taking into account short channel effects shows that especially in saturation region where VS and CLM are intense, $K_D\,|_{\Delta N}$ is significantly decreased. Furtermore the dependence of $K_D\,|_{\Delta N}$ on Coulomb scattering effect is also confirmed since it increases in higher current region when $\alpha\mu$ product is not equal to zero. It is easily understood that the two fundamental parameters of ΔN effect, N_T, α_c, can be easily extracted. In moderate inversion N_T can be extracted since there $\alpha\mu$ is negligible and then in strong inversion α_c can be extracted [186]. Results in Figure 3.9 were produced by implementing all three Equations 3.33, 3.37, 3.38 in Verilog-A and making the simulations with EKV3 model after the DC model was correctly extracted. The detailed procedure of extracting the values of the 1/f noise parameters N_T, α_c for the specific 90 nm technology node will be presented later on this chapter.

3.4.4 Mobility Fluctuation Effect

The mobility fluctuation effect ($\Delta\mu$) was first proposed by Hooge [188] and expanded for semiconductor devices and especially MOSFETs by [189, 190]. It relates 1/f noise with fluctuation of the mobility of the inverted carriers of the transistor. In this approach, output noise is generated by the fluctuations of the carrier mobility and the PSD of the local noise current source of an elementary section is given by [1, 22]:

$$\frac{S_{\delta I_n^2}}{I_D^2}\Big|_{\Delta\mu} = \frac{a_{\mathrm{H}} q}{W \Delta x \left(-Q_i\right) f} \tag{3.39}$$

where a_H is the unitless Hooge parameter ranges from about 10^{-4} to 10^{-6} . According to the generalized noise modeling methodology in EKV3 described above (Section 3.4.2), the fluctuation of the drain current due to an elementary section for $\Delta\mu$ effect is given by Equation 3.9:

$$\frac{S_{\delta I_{nD}^2}}{I_D^2}\Big|_{\Delta\mu} = \left(\frac{\Delta x}{L}\right)^2 \frac{S_{\delta I_n^2}}{I_D^2}\Big|_{\Delta\mu} = \frac{\Delta x a_{\mathrm{H}} q}{W L^2 \left(-Q_i\right) f} \tag{3.40}$$

After following the same procedure as in ΔN effect case (Equation 3.31), the PSD of the total fluctuation of the drain current due to $\Delta\mu$ effect is given by:

$$\frac{S_{I_D^2}}{I_D^2}\Big|_{\Delta\mu} = S_D\,\big|_{\Delta\mu}\, K_D\,\big|_{\Delta\mu} \tag{3.41}$$

with

$$S_D\,\big|_{\Delta\mu} = \frac{a_{\mathrm{H}} q^2}{KTWLnC'_{OX} f} \tag{3.42}$$

and

$$K_D\,\big|_{\Delta\mu} \triangleq \frac{1}{1+q_s+q_d}\left[1+\frac{ln\left(q_s/q_d\right)}{2\left(q_s-q_d\right)}\right] \tag{3.43}$$

Charge-based Equation 3.41 models the $\Delta\mu$ effect and is included in the new 1/f noise EKV3 compact model [24, 33] after being implemented in Verilog-A. The term $S_D\mid_{\Delta\mu}$ (Equation 3.42) is independent of operating conditions while $K_D\mid_{\Delta\mu}$ (Equation 3.43) describes the bias-dependence of mobility fluctuation effect.

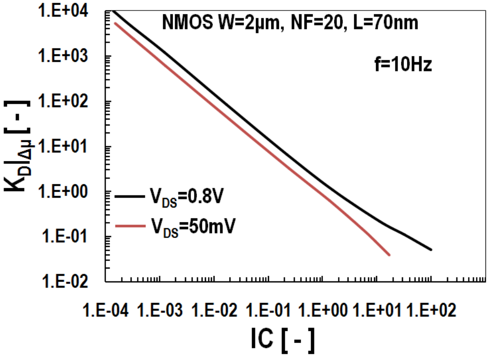


Figure 3.10: $K_D\mid_{\Delta\mu}$ vs. IC for an NMOS with $W = 2\,\mu m$, $NF = 40$, $L = 70\,nm$ in both saturation and linear region. Equation 3.43.

The behavior of $K_D\mid_{\Delta\mu}$ versus inversion coefficient IC is illustrated in Figure 3.10 for an NMOS device from $90\,nm$ CMOS technology node with $W = 2\,\mu m$, NF (number of fingers) $= 40$ and $L = 70\,nm$ at $f = 10\,Hz$ for both linear and saturation region [24]. It is quite obvious that $\Delta\mu$ effect is dominant in subthreshold region while it becomes insignificant in strong inversion regime. It can easily be concluded that a_H parameter related to this effect can be extracted from weak inversion.

3.4.5 Series Resistance Effect

An additional effect can give rise to 1/f noise under specific conditions and this is the source and drain series resistance effect [22, 191, 192]. This 1/f noise contribution can be modeled by two voltage sources in series with the resistances at source and drain, R_S, R_D respectively. Assuming that R_S, R_D are both equal to $R_\alpha/2$, the PSD of the drain current fluctuation due to series resistance effect is given by:

$$\frac{S_{I_D^2}}{I_D^2}\mid_{\Delta R}=\frac{S_{\Delta V_R^2}}{I_D^2}\,\frac{G_{ms}^2+G_{md}^2}{\left[1+(G_{ms}+G_{md})R_a/2\right]^2} \tag{3.44}$$

where $S_{\Delta V_R^2}$ is the PSD of the 1/f noise voltage sources in series with R_S, R_D mentioned above. Assuming that $(G_{ms}+G_{md})R_a/2 \ll 1$, then Equation 3.44 turns to:

$$\frac{S_{I_D^2}}{I_D^2}\mid_{\Delta R}=S_{\Delta R^2}\left(G_{ms}^2+G_{md}^2\right) \tag{3.45}$$

where $S_{\Delta R^2} = S_{\Delta V_R^2} I_D^2$. The charge-based formulation of Equation 3.45 is given by:

$$\frac{S_{I_D^2}}{I_D^2} \mid_{\Delta R} \simeq S_{\Delta R^2} G_{SPEC}^2 \left(q_s^2 + q_d^2 \right) \tag{3.46}$$

due to Equations 2.38, 2.39 . The bias-dependent term $K_D \mid_{\Delta R} = q_s^2 + q_d^2$ of Equation 3.46 shows that the contribution of series resistance effect becomes dominant at very strong inversion while it is insignificant in moderate and weak inversion.

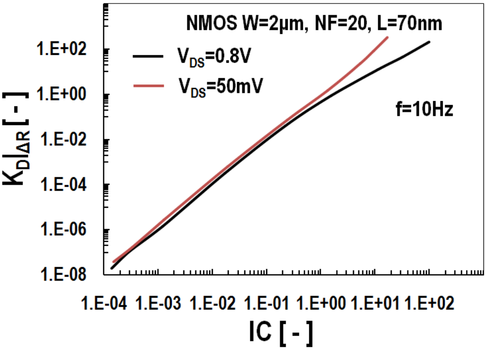


Figure 3.11: $K_D \mid_{\Delta R}$ vs. IC for an NMOS with $W = 2\,\mu m$, $NF = 40$, $L = 70\,nm$ in both saturation and linear region. Equation 3.46.

This behavior is shown in Figure 3.11 while $S_{\Delta R^2}$ which will be used as a model parameter can be extracted from the high current regime after all the other parameters related to carrier number and mobility fluctuation effects (N_T, α_c, a_{H}) have already been extracted.

3.4.6 Charge-Based 1/f Noise Model - EKV Implementation

The total PSD of flicker noise results from summing the individual 1/f noise components as described before, namely the components due to number fluctuations, mobility fluctuations, and series resistance fluctuations (Sections 3.4.3, 3.4.4, 3.4.5), given by the Equations 3.38, 3.41, 3.46, respectively. The final expression of flicker noise in MOSFETs, as implemented in the EKV3 model [33], is given by:

$$\frac{S_{I_D^2}}{I_D^2} = \frac{S_{I_D^2}}{I_D^2} \mid_{\Delta \mathrm{N}} + \frac{S_{I_D^2}}{I_D^2} \mid_{\Delta \mu} + \frac{S_{I_D^2}}{I_D^2} \mid_{\Delta R} \tag{3.47}$$

As shown in Figures 3.9, 3.10, 3.11, each of these effects is dominant under different operating conditions. This will be addressed later when our new model will be validated with data from two different experimental CMOS technology nodes at

180 and 90 nm. Carrier number fluctuation effect (ΔN) dominates in moderate and early strong inversion ($roughly\, 0.03 < IC < 30$), mobility fluctuation effect ($\Delta\mu$) in weak inversion ($IC < 0.03$) whereas series resistance effect (ΔR) in very strong inversion ($IC > 30$) and is apparent mostly for short channel devices.. Further qualitative analysis and evaluation of the behavior of the model will take place later on after comparing the model results with real data measured in our lab.

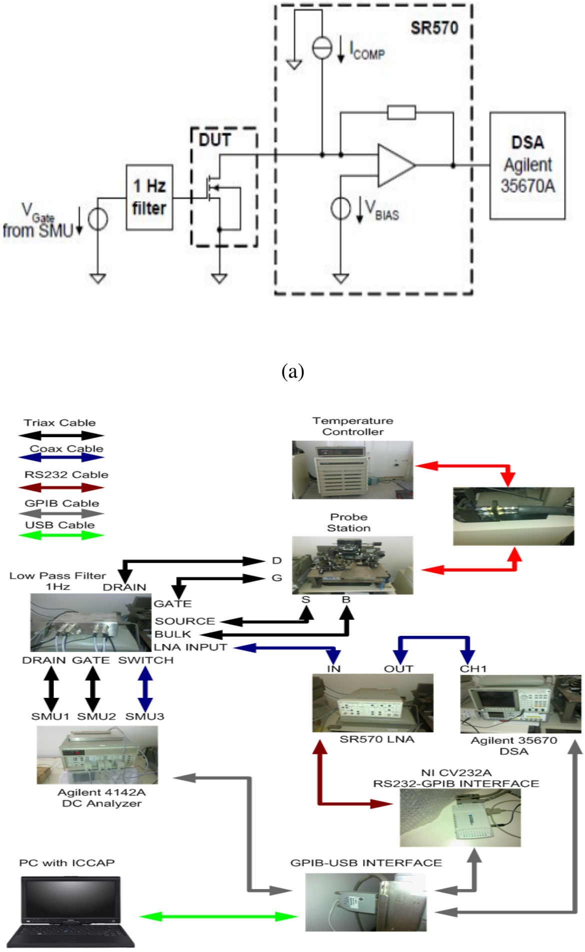
The physical equations of the 1/f noise model presented above have been coded in Verilog-A and integrated in the EKV3 model code. Since 1/f noise equations are bias-dependent, the 1/f noise model is strongly related to the IV model. Consquently, a correct extraction of the DC parameters of EKV3 model is required before flicker noise parameters are extracted. The EKV3 model is a complete model including all the effects which define the behavior of a MOSFET and as a result the DC quantities which appear in 1/f noise equations already include dependence on bias conditions and geometry. For example, the slope factor n which appears in $S_D\,|_{\Delta N}$, $S_D\,|_{\Delta\mu}$ “ bias-independent” quantities (Equations 3.32, 3.42) is in fact slightly bias-dependent, as well as geometry-dependent as predicted by the IV model. Consequently this will also be reflected in the 1/f noise model. The same can be concluded for carrier mobility μ, oxide capacitance per unit area C'_{OX} and effective width and length of the transistor W_{EFF}, L_{EFF}. The 1/f noise model is already included in known simulators such as specte, spice, hpeesofsim etc.

3.4.7 1/f Noise Measurement Set-up

Before validatiion of our new model with experimental data, the 1/f noise measurement set-up is briefly described. It consists off the following instruments:

- Cascade Microtech Probe Station
- Standford Research SR570 Low Noise Amplifier
- Agilent 35670 Dynamic Signal Analyzer
- HP 4142A Parameter Analyzer
- Low-pass Filter (1 Hz)
- USB to GPIB Interface

On-wafer measurements were performed using a Cascade Microtech probe station with Microchamber, and devices were biased via low pass filter (1 Hz) from an HP 4142B Source Measurement Unit. The drain current noise is amplified with a Standford Research SR570 LNA, and analyzed with an Agilent 35670A DSA. In Figure 3.12, the 1/f noise measurement set-up is illustrated both in a diagram (Figure 3.12a) and in full detail with photos of the instruments, the cables and the interconnections (Figure 3.12b). The whole system was provided by AdMOS. Software used to make the measurements was Agilent ICCAP while a specialized user interface which permits the simple performance of the measurements was also implemented by AdMOS and provided to us.



(a)

(b)

Figure 3.12: 1/f noise measurement set-up a) basic diagram and b) complete set-up with all instruments and interconnections

Through this software, one can make IV measurements firstly by defining simple transfer and output characteristic set-ups, in order to ensure the correct operation of the device and then by choosing specific bias points which have already been included in IV set-ups, can make the 1/f noise measurements. An indicative example of measured noise is presented in Figure 3.13, where the noise of an NMOS transistor of 180 nm experimental CMOS process with $W = 5\,\mu m$ and $L = 2\,\mu m$ is shown at different gate voltage values at saturation region. It is important to mention here that the whole 1/f noise analysis in this Thesis is mainly based on the bias-dependence of flicker noise. In order to study this dependence, a normalization must be done as far as frequency is concerned. The best approach is to see flicker noise at 1 Hz and the way to achieve this is to multiply 1/f noise data with frequency and then average the result in order to extract one value at 1 Hz. This procedure is followed in almost every bias-dependent analysis of 1/f noise that takes place in the rest of this Thesis and is shown schematically in Figure 3.14. Special attention should be paid at the corner frequency of each spectrum. The lower the inversion level, the lower the f_c becomes as it can be seen in Figure 3.13 and thus the above normalizing method should be applied in a range of frequencies where 1/f noise behavior exists.

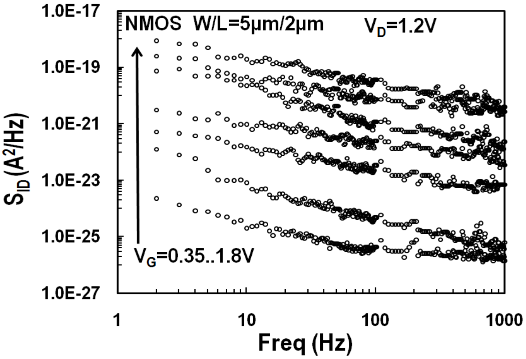


Figure 3.13: Measured noise S_{ID} vs. frequency for an NMOS with $W = 10\,\mu m$, $L = 180\,nm$ at saturation region ($V_D = 1.2\,V$) for different gate voltage values ($V_G = 0.35, 0.4, 0.5, 0.6, 0.8, 1.2, 1.8\,V$).

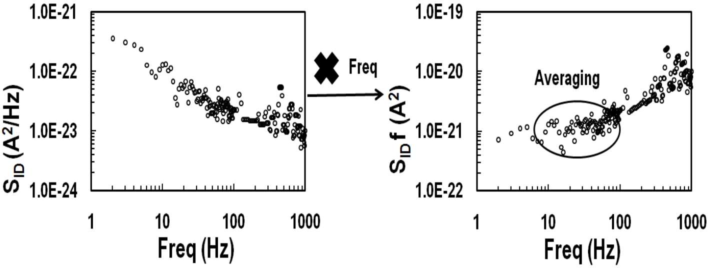


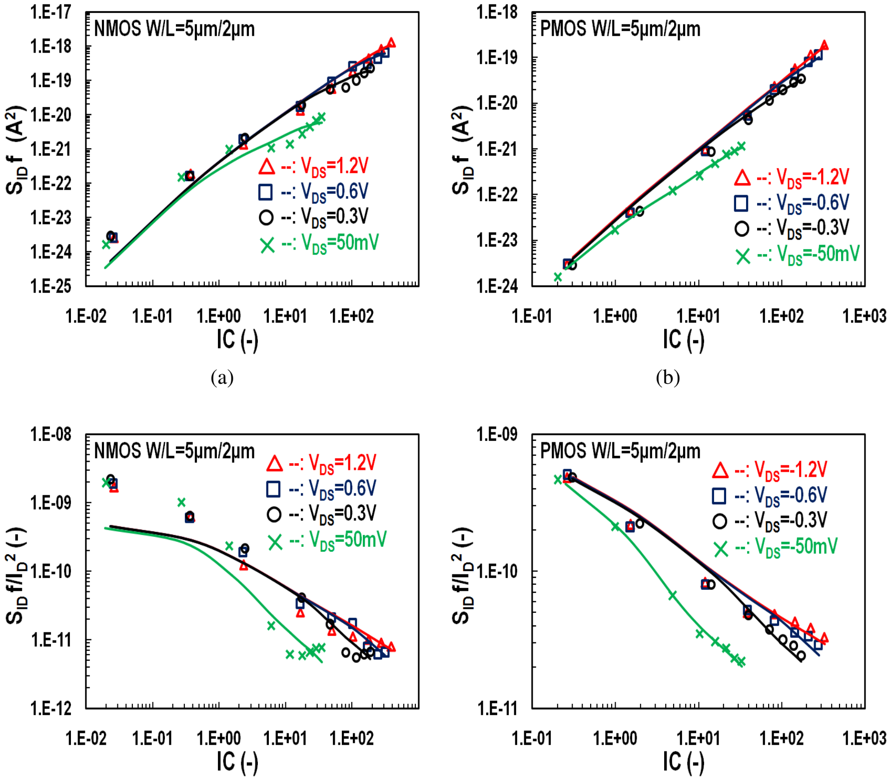
Figure 3.14: Procedure followed to extract average 1/f noise at 1 Hz

3.4.8 Results-Discussion

After presenting the fundamental physics of 1/f noise in MOSFETs and after implementing a compact model based on this theory, our model will be now validated at two experimental CMOS technology nodes; one at $180\,nm$ measured in our lab as mentioned before and another at $90\,nm$ provided by the industry. Bias-dependence and scaling of 1/f noise which is an important subject for the design of analog/RF integrated circuits in scaled CMOS technology, is examined in this section including experimental characterization and compact modeling for both NMOS and PMOS devices in both nodes mentioned above [24, 33]. The 1/f noise compact model approach is based on a charge-based formulation as presented analytically in the previous sections, including carrier number fluctuation, mobility fluctuation and series resistance fluctuation 1/f noise mechanisms (Equations 3.38, 3.41, 3.46, 3.47). In $180\,nm$ CMOS process, the complete compact model is applied while in $90\,nm$, series resistance effect is excluded while a simpler approach is used for carrier number fluctuation effect (Equation 3.37). 1/f noise bias-dependence and scaling is covered over a wide range of geometry and bias, from long to short channel, weak to strong inversion and linear to saturation regimes. The carrier number fluctuation model allows to well represent increased noise in strong inversion while mobility fluctuation is found to be significant in deep weak inversion. As a result, input referred noise (Equation 3.7), shows a minimum in moderate inversion while in $180\,nm$ CMOS, series resistance effect causes an additional increase of 1/f noise in very strong inversion. For both technology nodes tested, the new 1/f noise compact model provides a good qualitative fit for every bias and area conditions.

180 nm CMOS Process

Transistors of large geometry and channel length ($W = 5\,\mu m$, $L = 2\,\mu m$), and of short geometry ($W = 10\,\mu m$, $L = 180\,nm$) were measured covering the range of gate voltage, $0.4V > |V_G| > 1.6V$ and drain voltage $|V_D| = 50\,mV$, $300\,mV$, $600\,mV$, $1.2\,V$. In order to obtain data sufficient to study qualitative 1/f noise behavior, the spectra of 3 samples were measured and then multiplied by frequency and averaged in order to see noise at $1\,Hz$. In Figures 3.15, 3.16, 3.17, 3.18 [33], the PSD of 1/f noise for both NMOS and PMOS devices is represented in the form of $S_{ID} * f$, $S_{ID}/I_D^2 * f$, and finally $S_{VG} * f * W * L$, all versus inversion coefficient IC. The normalized drain current can then easily be interpreted as strong inversion ($IC > 10$), moderate inversion ($0.1 < IC < 10$) and weak inversion ($IC < 0.1$). The simulated model is shown for the two geometries, short and long transistors, both in saturation and linear modes. As mentioned before, the representation of 1/f noise versus IC allows for an immediate interpretation in terms of inversion conditions, but also eases the comparison among different device types and sizes. Table 3.1 [33] shows the corresponding parameters extracted for either type of device. Note that a single parameter set is used for each type of transistors for all geometries and in all bias conditions.

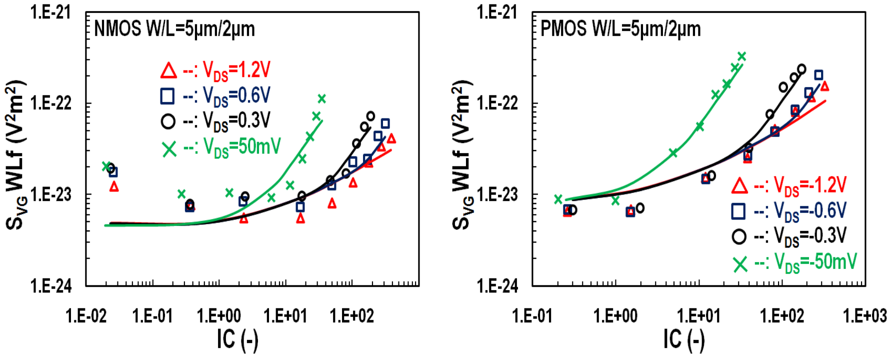


(a) (b)

(c) (d)

Figure 3.15: PSD of 1/f noise at 1 Hz a,b) in drain current $S_{ID} * f$, and c,d) divided with the square of drain current $S_{ID}/I_D^2 * f$ vs. inversion coefficient IC from weak to strong inversion at linear ($|V_{DS}| = 50\,mV$) and saturation ($|V_{DS}| = 1.2, 0.6, 0.3\,V$) modes. NMOS (left) and PMOS (right) transistors, with $W = 5\,\mu m$ and $L = 2\,\mu m$ are shown for both measurement (markers) and model (lines).

The carrier number fluctuation model accounts for the increased 1/f noise for either type of transistors, in linear and saturation modes, over most of the moderate to lower strong inversion range. The Coulomb scattering coefficient has a great effect on the increase of input referred noise at high levels of inversion. On the other hand, the mobility fluctuation model is able to well represent increased 1/f noise at low levels of inversion. Series resistance model represent the increase of 1/f noise in strong inversion for short device.



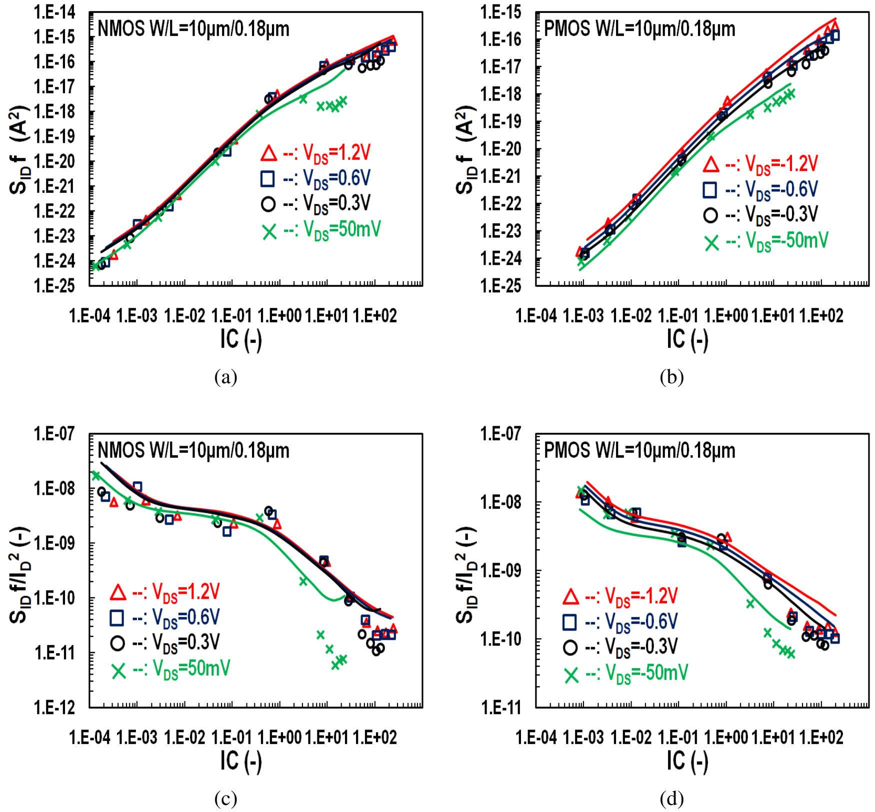
(a) (b)

Figure 3.16: PSD of 1/f noise at $1\,Hz$ in gate voltage normalized with area $S_{VG} * f * W * L$ vs. inversion coefficient IC from weak to strong inversion at linear ($|V_{DS}| = 50\,mV$) and saturation ($|V_{DS}| = 1.2, 0.6, 0.3\,V$) modes. NMOS (a) and PMOS (b) transistors, with $W = 5\,\mu m$ and $L = 2\,\mu m$ are shown for both measurement (markers) and model (lines).

In more detail, the effect of each 1/f noise contribution to the total 1/f noise is illustrated in Figure 3.19, where normalized input noise $S_{VG} * f * W * L$ is shown versus inversion coefficient IC for a short NMOS device at saturation. Generally speaking, the overall performance of the new 1/f noise model is quite adequate and especially in PMOS devices the results are even better and this can be attributed to better noise immunity of PMOS due to the presence of the n-well.

Parameter	Units	NMOS	PMOS
N_T	$eV^{-1}cm^{-3}$	$9.6.10^{16}$	$9.44.10^{17}$
a_C	VsC^{-1}	$1.1.10^4$	$1.0.10^5$
a_H	$-$	$1.0.10^{-7}$	$3.0.10^{-7}$
E_{CRIT}	V/m	$2.5.10^6$	$8.0.10^6$
$S_{\Delta R}$	$\Omega^2 Hz^{-1}$	$1.0.10^{-7}$	$1.0.10^{-6}$

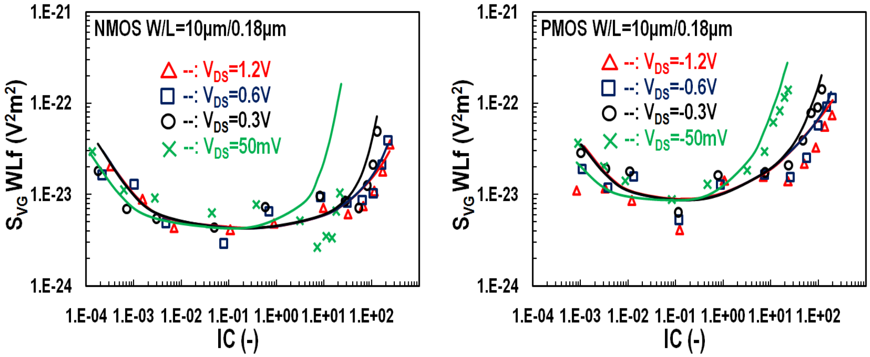
Table 3.1: 1/f Noise model parameters for experimental $180\,nm$ CMOS node



(a) (b)

(c) (d)

Figure 3.17: PSD of 1/f noise at 1 Hz a,b) in drain current $S_{ID} * f$, and c,d) divided with the square of drain current $S_{ID}/I_D^2 * f$ vs. inversion coefficient IC from weak to strong inversion at linear ($|V_{DS}| = 50\,mV$) and saturation ($|V_{DS}| = 1.2, 0.6, 0.3\,V$) modes. NMOS (left) and PMOS (right) transistors, with $W = 10\,\mu m$ and $L = 0.18\,\mu m$ are shown for both measurement (markers) and model (lines).



(a) (b)

Figure 3.18: PSD of 1/f noise at $1\,Hz$ in gate voltage normalized with area $S_{VG} * f * W * L$ vs. inversion coefficient IC from weak to strong inversion at linear ($|V_{DS}| = 50\,mV$) and saturation ($|V_{DS}| = 1.2, 0.6, 0.3\,V$) modes. NMOS (a) and PMOS (b) transistors, with $W = 10\,\mu m$ and $L = 0.18\,\mu m$ are shown for both measurement (markers) and model (lines).

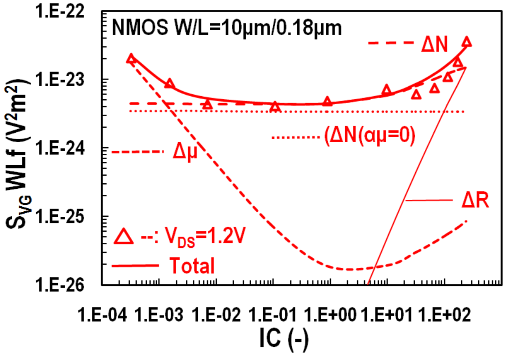
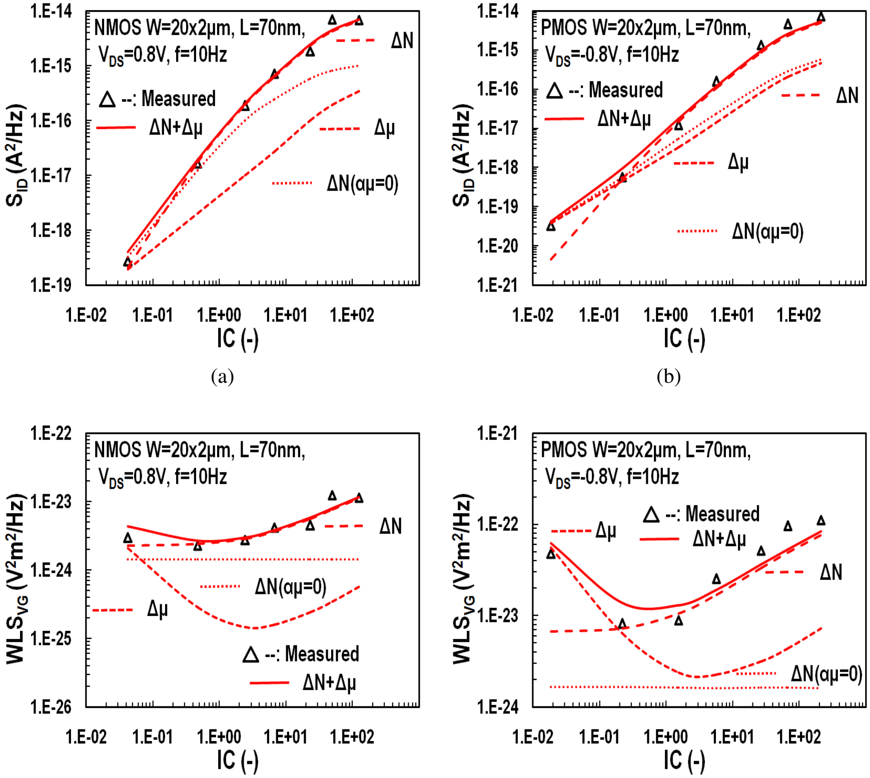


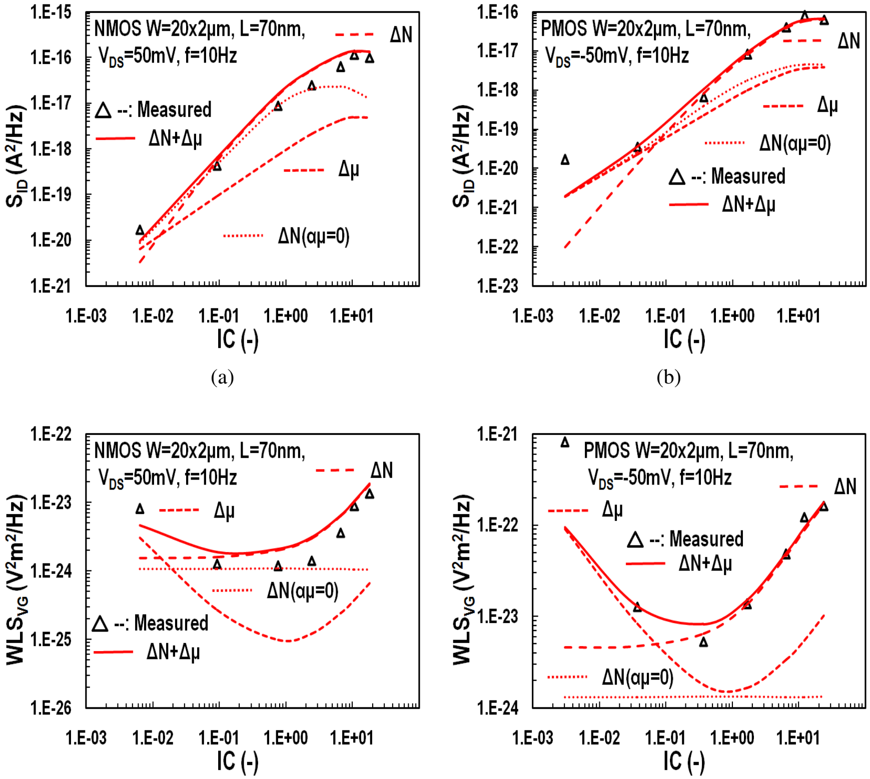
Figure 3.19: Input noise normalized with area, referred to $1\,Hz$, $S_{VG} * f * W * L$ vs. inversion coefficient IC for an NMOS transistor with $W = 10\,\mu m$ and $L = 180\,nm$ at saturation region $V_{DS} = 1.2\,V$. Measurement (markers), full model (lines), with different noise contributions (dashed and dotted lines) are shown.



(a) (b)

(c) (d)

Figure 3.20: PSD of 1/f noise at $10\,Hz$ in drain current S_{ID} (a, b) and normalized with area gate voltage $S_{VG} * W * L$ (c, d) vs. inversion coefficient IC from weak to strong inversion at saturation ($|V_{DS}| = 0.8\,V$) mode for both NMOS (left column) and PMOS (right column) transistors, with $W = 20x2\,\mu m$ and $L = 70\,nm$. Measurement (markers), full model (lines), with different noise contributions (dashed and dotted lines) are shown.



(a) (b)

(c) (d)

Figure 3.21: PSD of 1/f noise at $10\,Hz$ in drain current S_{ID} (a, b) and normalized with area gate voltage $S_{VG} * W * L$ (c, d) vs. inversion coefficient IC from weak to strong inversion at linear ($|V_{DS}| = 50\,mV$) mode for both NMOS (left column) and PMOS (right column) transistors, with $W = 20x2\,\mu m$ and $L = 70\,nm$. Measurement (markers), full model (lines), with different noise contributions (dashed and dotted lines) are shown.

A simpler version of our new 1/f noise compact model is validated with flicker noise measurements at $90\,nm$ CMOS. In this approach, series resistance effect is excluded while carrier number fluctuation effect does not include mobility degradation due to velocity saturation-channel length modulation effect (Equation 3.37 instead of Equation 3.38). The bias-dependence of 1/f noise data from both NMOS and PMOS multifinger devices with $W = 20x2\,\mu m$ and $L = 70\,nm$ is investigated in a wide range of gate voltage values, $0.1\,V > V_G > 1.2\,V$ at both linear $|V_D| = 50\,mV$ and saturation $|V_D| = 0.8\,V$ region. The devices under test show a distinct 1/f noise behavior. In Figures 3.20, 3.21 [24], the PSD of 1/f noise for both NMOS and PMOS devices is represented in the form of S_{ID} and $S_{VG} * W * L$ at $f = 10\,Hz$, versus inversion coefficient IC. The individual noise components of carrier number fluctuation (McWhorter) and mobility fluctuations (Hooge) are shown, as well as their sum, from weak to strong inversion both in saturation and linear modes. A simple 1/f noise model assuming a constant input referred 1/f noise PSD is also shown for comparison (Equation 3.37 with αμ product equal to zero). As in $180\,nm$ CMOS case, the carrier number fluctuation model is capable of well representing the increased noise for either type of transistors, in linear and saturation modes, over most of the moderate to strong inversion range. On the other hand, mobility fluctuation model, similarly to $180\,nm$ CMOS, is able to well represent increased noise at low levels of inversion.Table 3.2 [24] shows the corresponding parameters extracted for either type of device.

Parameter	Units	NMOS	PMOS
N_T	$eV^{-1}cm^{-3}$	$3.2.10^{16}$	$3.2.10^{16}$
a_C	VsC^{-1}	$1.0.10^{4}$	$1.0.10^{5}$
a_H	–	$7.0.10^{-7}$	$1.0.10^{-5}$

Table 3.2: 1/f Noise model parameters for experimental 90nm CMOS node

Important Conclusions

The new charge-based 1/f noise compact model was tested at two different experimental technology nodes and the results were more than satisfying and some very important conclusions can be made [24, 33].

- Input referred 1/f noise in PMOS devices is higher than in NMOS while the observed bias-dependent behavior follows a similar trend for either type of device.
- In older simpler approaches of carrier number fluctuation effect [145, 170, 176, 177], Coulomb scattering was not taken into account ($\alpha\mu = 0$) and as a result input referred noise was constant versus inversion coefficient. But it is proven experimentally that input noise increases from moderate to strong inversion and the complete carrier number fluctuation model allows to well represent this increase for both NMOS and PMOS transistors. Furthermore, in complete version of the model [33], velocity saturation is accounted for, and the whole noise model is tightly related to the underlying charge model, therefore accounting for other short channel effects, such as channel length modulation.
- The mobility fluctuation is significant only in deep weak inversion and the corresponding model allows to well represent the corresponding increase of

noise. This is shown experimentally for the first time [24, 33]. It is important to mention here that while both carrier number and mobility fluctuation effects are technology-dependent, carrier number fluctuation effect appears to be always present while the appearance of mobility fluctuation effect depends on process.

- The combined number fluctuation, mobility fluctuation and series resistance fluctuation model allows to well represent all the bias-dependence observed over a wide range of bias conditions. As a result, input referred noise shows a minimum in moderate inversion increasing the attractiveness of moderate inversion design.

- From moderate inversion region, N_T parameter can be extracted either from normalized with the square of drain current S_{ID}/I_D^2 output noise or from input referred noise S_{VG}. In more detail, S_{ID}/I_D^2 reaches a plateau in moderate inversion while S_{VG} a minimum and since mobility fluctuation, Coulomb scattering and series resistance effects are insignificant in this region, N_T can be extracted. Both S_{ID}/I_D^2 and S_{VG} increase in weak inversion and from there a_H can be extracted, as has been shown for the first time. a_C can be extracted from the increase of both S_{ID}/I_D^2 and S_{VG} in strong inversion after the extraction of N_T and a_H. Finally $S_{\Delta R}$ can be extracted from a short channel device in very strong inversion. This parameter extraction procedure can be pictured in Figure 3.19. As mentioned earlier in this chapter, the complete 1/f noise model has been implemented in the charge-based EKV3 MOS transistor model and thus all IV quantities used in 1/f noise equations such as the inversion charges q_s, q_d as well as mobility μ, slope factor n etc are evaluated from the full charge-based compact model.

Chapter 4

Low-Frequency Noise in HV-MOSFETs

4.1 Introduction

Low frequency noise in High-Voltage MOSFETs, especially under high-voltage conditions, remains largely uninvestigated. The device under test as far as 1/f noise analysis in HV devices is concerned in this Thesis, is the RESURF LDMOS which was described in detail in chapter two (Section 2.2.2.2). Until nowadays LV 1/f noise models were used to describe 1/f noise at HV-MOSFETs since there was the belief that LV channel part was the only contributor to 1/f noise in these devices. Recent work has shown that this is not the case since the characteristics of 1/f noise in LDMOS are significantly different than standard LV-MOSFETs due to additional noise mechanisms which arise in the extended drain region and more specifically in the extension of gate oxide in the drift region [193, 194]. Scope of our work was to develop a new complete compact 1/f noise model for LDMOS transistors for the first time and this task was accomplished [27].

Although the operating principles of an LDMOS device date back in previous decades, flicker noise of this kind of transistors has been given the appropriate attention only recently due to the plenty important analog applications that LDMOS can be used in. Such applications can be in automotive, medical and industrial electronics, RF and cellular communications and other circuits with voltage requirements in the range of $10 - 120\,V$ such as gate drives, voltage converters, LED drivers, and high-voltage operational amplifiers. These circuits are sensitive to 1/f noise. Furthermore HV-MOS technologies that combine HV devices with base RFCMOS process can offer higher levels of integration for system-on-chip (SOC) applications. In such SOC applications, such as hand-held devices, where HV-MOS devices are used as switches, flicker noise can become significant if it couples to other circuits through the substrate. Furthermore, 1/f noise can especially affect the performance of oscillators, analog baseband, and bandgap reference circuits.

Apart from the above, flicker noise can be a nondestructive, powerful characterization tool for the health assessment of LDMOS transistors and serves as a figure of merit for the device reliability. LDMOS devices have become of great interest due to their large voltage handling capability. These devices can stand high current densities, severe hot carrier injection, on-resistance degradation, fast interface trap generation and trapping/detrapping mechanism leading to considerable 1/f noise degradation. In more detail, when the carriers are lying beneath additional dielectric/Si interfaces in the extended drain, drain current fluctuations through further trapping/detrapping are increased and thus additional 1/f noise is produced .

After this introduction, the fundamental physical procedure that generates 1/f noise in LDMOS is presented [193, 194, 195] with giving attention to the lack of complete compact models [196, 197, 198]. After that, the 1/f noise measurement setup as well as the devices under test are presented thoroughly and then we focus on the development of our complete 1/f noise compact model for LDMOSFETs [27] which is charge-based in agreement with EKV3 formulation. The model validation for a wide range of devices, dimensions and operating conditions follows [34] whereas, a detailed 1/f noise parameter extraction procedure which was proposed both for the LV channel of the device [199] as well as for the whole transistor including drift region contribution to flicker noise [35] is presented. Finally some important conclusions are drawn.

4.2 1/f Noise Sources in HV-MOSFETs - Basic Physics

Despite the fact that until recently, 1/f noise models of standard LV CMOS devices were used to model 1/f noise in HV devices, LDMOS do not follow such models especially under conditions where flicker noise being contributed by drift region becomes significant. This noise source arising from drift region and especially from the extension of gate oxide which overlaps with drift region superficially, was recently experimentally observed [193, 194, 196]. In more detail, carrier fluctuations due to trapping/detrapping mechanism in the S_i/S_iO_2 interface occur not only in channel part as was expected but also in the overlap region in drift extension. This is the only additional source of 1/f noise in LDMOS since bulk resistance fluctuations under the field oxide (FOX) of drain region were found to be negligible [194]. Furthermore, for transistors with same channel and gate overlap length, those with longer FOX are observed to have lower 1/f noise. This occurs because the longer FOX provides more extent for the carriers underneath the field oxide to spread out towards bulk and thus the high current density as well as the corresponding carrier fluctuations are reduced [197].

While flicker noise in drift region arises from the accumulated region below the gate-drain overlap where electrons can flow at the surface, it becomes significant only under low drain and higher gate voltage conditions as well as for longer channel length devices. For lower gate voltages, drift region is not yet activated while for short channel devices, the LV channel noise dominates. The latter can be justified since only a fraction of electrons (or holes) travel along the gate oxide interface in the gate-drain overlap region, whereas others take the subsurface path through the bulk. The reduction in the number of electrons which flow across the gate oxide interface effectively reduces the contribution of noise from this region and this is the case for short channel transistors [195]. Under saturation, 1/f noise arising from channel part is still dominant, with the exception that the design of drift region will have an impact on the flicker noise in LDMOS devices, through its effect on the quasi-saturation behavior [195]. Furthermore, self-heating effect under high drain and gate voltage conditions which affect current-transconductance charcteristics of the device can also affect flicker noise through them [34, 35].

The same conclusions as above can be extracted following a different approach using DC stress measurements [193, 194, 197]. In the work from this group, the effect of DC stress on flicker noise was examined while a model for flicker noise in LDMOS was proposed [196, 198]. In more detail, under low gate voltage conditions where LV channel noise dominates over the contribution from drift region, the overall flicker noise of the device does not change with stress while for higher gate voltages when drift region noise becomes significant, the overall noise is increased with stress. This increase is obtained in the inherent noise of the extended drain, due to degradation in the extended drain region under the gate oxide region. High-voltage stressing causes an increase in the interface traps, thus increasing 1/f noise due to more intense trapping/detrapping mechanism [193]. The group has demonstrated that the relative percentage of degradation with stressing time in 1/f noise is much higher and occurs much earlier than that for the DC parameters. From this degradation behavior, an early lifetime prediction method for the LDMOS devices was shown in [196] . While DC stressing took part in high-voltage values towards the limits of the devices, 1/f noise measurements took place in linear region regime as there the noise contribution from drift region becomes significant as mentioned above. The model proposed from this group [196, 198] was based on carrier number and the correlated mobility fluctuation theory as in the well known unified model [173] but has been modified to account for the fluctuations in the extended drain and the channel. Unlike [173], nonuniform trap distribution has been taken into account with respect to position in the gate oxide and band-gap energy. While this work can be described quite remarkable, the resulting model can not be considered compact or complete as it will be shown in the following section.

4.3 A Complete Charge-Based 1/f Noise Compact Model for LDMOS Devices

4.3.1 General Considerations

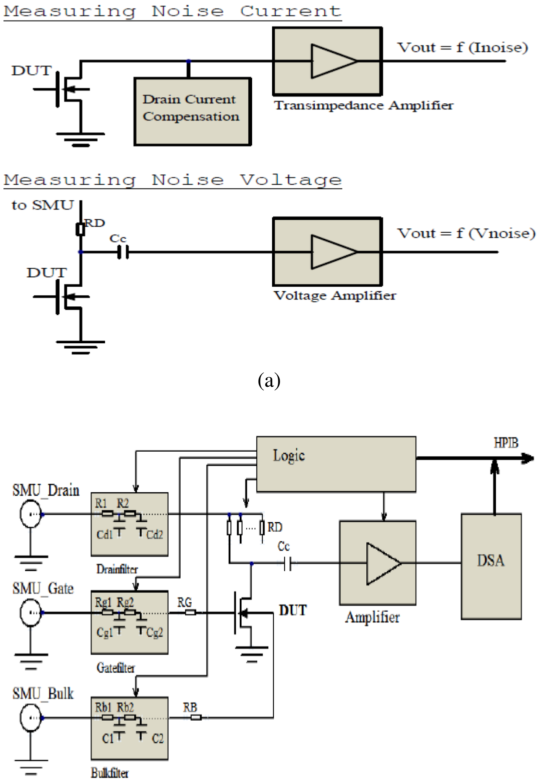
In this section, our recently established charge-based 1/f noise model for LDMOS [27] is presented. As mentioned before this model is both compact and complete and this is something shown for the first time. Initially the measurement procedure is described and then the model is introduced in detail. First, the equations of the model and its validation with experimental data is presented in [27]. A more detailed analysis emphasizing the behavior of both model and measured 1/f noise versus drain voltage, containing a very detailed bias range, is then presented in [34]. After this, a complete 1/f noise parameter extraction procedure is established firstly for the LV channel part when flicker noise from drift region is insignificant [199] and then for the whole device regardless of operating conditions and device dimensions [35]. The schematic of the LDMOS device used in this analysis is shown in Figure 2.16 .

The effect of drift region on 1/f noise remained unclear until recently due to the difficulty of performing 1/f noise measurements under high drain voltages, on the order of tens of volts. This was mainly due to the lack of adequate measurement equipment, which usually restricts LF noise to be measured up to just a few volts, usually generated from batteries. A new dedicated measurement set up provided by AdMOS which allowed measuring 1/f noise of LDMOS devices up to 200 V at the drain, was used in this work and is presented in detail in the following section. Flicker noise of many types of both n- and p-channel LDMOSFETs was measured over a very large range of gate and drain bias conditions at long as well as short channel lengths. An important amount of measurement data on different devices and a large range of bias conditions has been collected. For reasons of clarity, the set of experimental data is described for each individual analysis, namely:

- 1/f noise model presentation [27]
- detailed evaluation of behavior of 1/f noise model versus drain voltage [34]
- 1/f noise parameter extraction procedure [35, 199]

4.3.2 1/f Noise Measurement Set-up at High V_{DS}

To palliate the absence of adequate measurement equipment, a new measurement system is described in this work, which allows us to measure 1/f noise of LDMOSFETs up to 100–200 V, generated from low-pass-filtered source measurement units (SMUs). This 1/f noise measurement system was designed by AdMOS. To measure noise in semiconductor devices, there are two choices: Either noise current or noise voltage may be measured. Since we are dealing with semiconductor devices in which the noise produced depends on their operating point, a specified drain current should be delivered to a MOSFET, for example.



(a)

(b)

Figure 4.1: a) Set-ups for noise measurements on semiconductor devices. Top: Noise current measurement using a transimpedance amplifier and a current source. Bottom: Noise voltage measurement with additional drain resistor and blocking capacitor. b) Block diagram of the proposed and built noise measurement system to measure low frequency noise of HV devices.

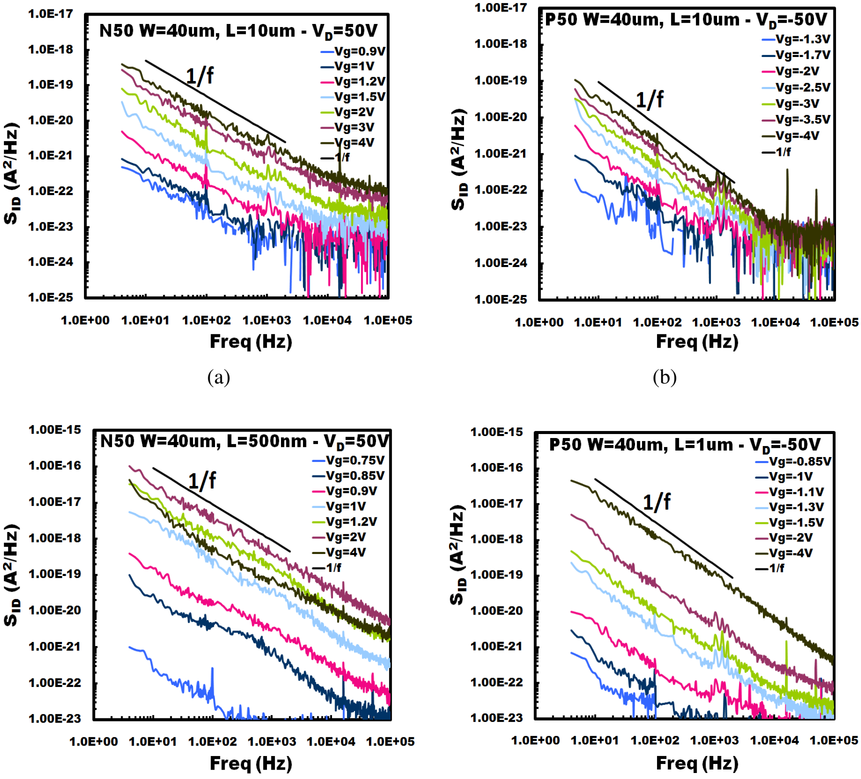
Figure 4.1a shows both measurement set-ups. The complete measurement set-up, shown in Figure 4.1b, consists of an embedded low-noise amplifier (LNA) and fourth-order low-pass RC filters, which are used to prevent the SMU noise entering the gate or the drain of the device under test (DUT). The LNA consists of several OP-Amps in parallel, reducing the noise voltage by the square root of the number of OP-Amps [200, 201]. Apart from the noise of the DUT to be measured, there is a series of other parasitic noise sources to be considered: 1) thermal noise from R_D, 2) amplifier voltage noise, and 3) amplifier current noise. The additional noise sources disturbing the measurement effort are constant, depending either on resistance or on individual noise values of the OP-Amps, as well as on temperature. The undesired noise components can be eliminated from the measurements by implementing a calibration procedure, which identifies the actual noise of each of the amplifiers and drain resistors. The measurement system which was built is described by the corresponding block diagram shown in Figure 4.1b and measures current noise. Measurement of noise at a specified voltage delivered to the drain of a MOSFET through a large-order passive lowpass filter requires RC networks in the current path, while LC networks are unhandy for frequencies in the subhertz range. Therefore, the voltage set at the SMU needs to be significantly higher for acceptable drain currents than the necessary drain voltage for a given bias point. To get reliable and repeatable measurements, the actual drain voltage needs to be controlled at measurement time without inserting additional noise sources.

4.3.3 Model Implementation

According to recent work [193, 194, 195, 197], some noise mechanisms are attributed to the extension of gate oxide in the drift region, as well as to the quasi-saturation and self-heating effect, influencing the 1/f noise of the whole HV device. The effect of HV stress on LF noise is analyzed in [193, 194, 197] but is restricted to noise at low drain bias only; conversely, in [195], flicker noise of lateral double-diffused MOSFETs (LDMOSFETs) is analyzed under high drain voltage. However, the analysis is restricted to n-channel devices, while p-channel devices are not covered. Although fits of an LF noise compact model to data [195] have been claimed, no such graphs were actually provided. Furthermore, a new model for 1/f noise in LDMOSFETs is indeed proposed in [196, 198] but is limited in linear region operation and does not propose a final analytical and compact equation.

Our new compact 1/f noise model for LDMOSFETs is based on a new charge-based compact HV-MOSFET model recently established, which describes accurately the DC and RF behavior of the device covering both the drift region and the low-voltage (LV) channel [31, 32, 132]. The modeling of the LV part of the HV-MOSFET is, in many ways, similar to the EKV3 compact model. In standard bulk MOSFETs, the three basic contributions to flicker noise are carrier number fluctuations and mobility fluctuations [159, 188]. Recently as shown in the previous chapter, a charge-based 1/f noise model has been included in the EKV3 model and validated for 90 and 180 nm bulk CMOS [22, 24, 33]. This charge-based 1/f noise model for LV transistors is adapted and implemented in the HV-MOSFET model and extended to cover additional effects on 1/f noise observed in HV-MOSFETs.

4.3.3.1 Experimental Data Description



(a) (b)

(c) (d)

Figure 4.2: PSD of 1/f noise drain current S_{ID} vs. frequency for $50\,V$ long (a,b) and short (c,d) n- and p-channel LDMOSFETs at different V_G values from weak to strong inversion. Frequency dependence is close to 1/f.

Flicker noise spectra were measured on four types of LDMOSFETs of the $0.35\,\mu m$ HV-MOS technology from ams AG[1]. Both n- and p-channel LDMOSFETs with $T_{OX} = 15\,nm$, rated at 50 and $20\,V$, respectively—designated here with the acronyms N50, P50, N20 (isolated device), and P20—were measured in the range of $4\,Hz$–$100\,kHz$. For each device, wide-long transistors with $W = 40\,\mu m$, $L = 10\,\mu$m (all types) and wide-short transistors with $W = 40\,\mu m$, $L = 0.5\,\mu m$ (N50 and N20), $L = 1\,\mu m$ (P50),

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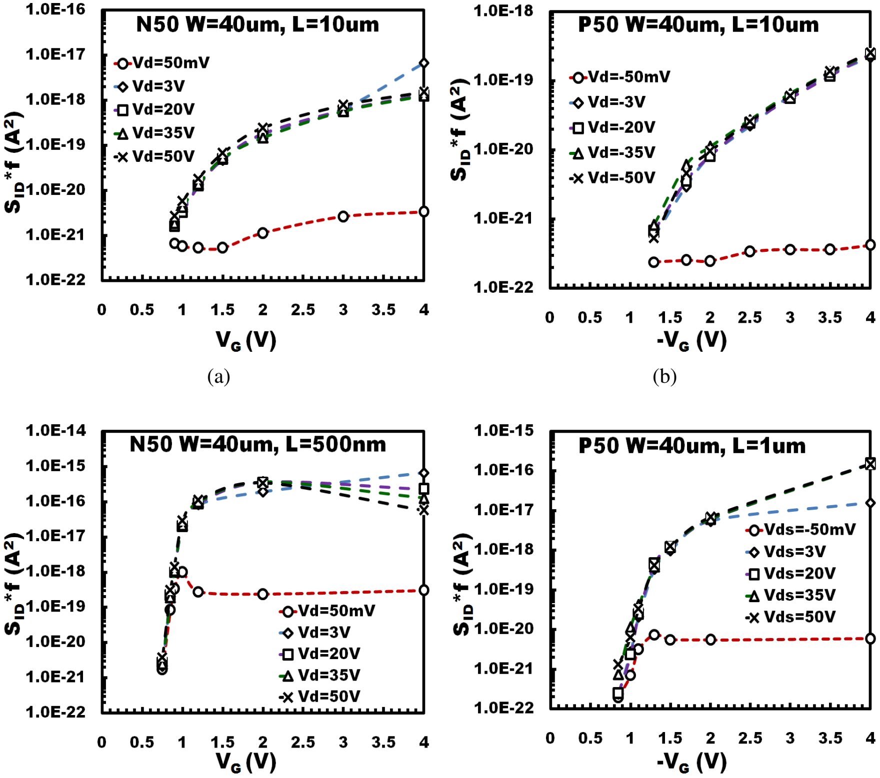
[1] Austria Microsystems

and $L = 0.6\,\mu m$ (P20) were measured at five V_D values (from $50\,mV$ up to 20–50 V) and seven V_G values (from weak to very strong inversion). The length of the drift region is constant for a given type of transistor.



(a) (b)

(c) (d)

Figure 4.3: Averaged PSD of 1/f noise drain current S_{ID} vs. V_G at $1\,Hz$ for $50\,V$ long (a,b) and short (c,d) n- and p-channel LDMOSFETs at $|V_D| = 50\,m$, 3, 20, 35, $50\,V$.

In Figure 4.2 [27], the power spectral density S_{ID} for N50 and P50 devices at $V_D = 50\,V$ is shown. It can be observed that the noise measurements are very reliable even for such high drain voltage. The frequency dependence is close to 1/f throughout the lower decades of frequency. For each transistor geometry, four different devices were measured, and an average value was calculated. To examine the bias-dependence of measured flicker noise, the procedure described in Figure 3.14 is followed. Thus, Figure 4.3 [27] shows the bias-dependence versus V_G for all five V_D values for N50 and P50 long and short devices. Noise at the drain and at the gate is related as shown in Equation 3.7. As it will be shown later, 1/f noise follows the behavior of gate transconductance g_m. In long devices, the noise bias-dependence resembles that in LV-MOSFETs. However, particularly in the short N50 device, a decrease of noise can be observed for high V_D and V_G values, which comes from the dependence of noise on g_m as it will be detailed below.

4.3.3.2 Model Equations

The HV-MOSFET compact model [32, 132] provides a coherent description of all quantities of interest such as current, transconductances, etc., as functions of normalized inversion charges evaluated at source and K-point (Figure 2.16), q_s, and q_k, respectively. On the other hand, velocity saturation in the drift region, which is the cause of quasi-saturation in HV-MOSFETs, is modeled by a physics-based description [32]. A reduction of g_m due to quasi-saturation will also reduce 1/f noise in HV-MOSFETs, which is accounted for in the compact model in a natural way. In the following, the modeling of 1/f noise contributions is divided into two parts, the LV channel—the main contributor—and the drift region as [27]:

$$\frac{S_{I_D^2}}{I_D^2} = \frac{S_{I_D^2}}{I_D^2}\Big|_{\Delta \mathrm{N}_{LV}} + \frac{S_{I_D^2}}{I_D^2}\Big|_{\Delta \mu_{LV}} + \frac{S_{I_D^2}}{I_D^2}\Big|_{\Delta \mathrm{N}_{DRIFT}} \tag{4.1}$$

LV Part

In our new HV-MOSFET 1/f noise model, the LV part up to the K-point follows the approach adopted by the EKV3 1/f noise compact model for conventional CMOS [22, 24, 33]. Basically, the normalized inversion charge at the K-point q_k takes the role of the normalized inversion charge at the drain q_d. These charges as well as other quantities such as mobility μ and slope factor n are evaluated from the charge-based DC compact model. The total noise PSD of drain current from source to the K-point is given by the sum of contributions from carrier number fluctuations ΔN [159] and mobility fluctuations $\Delta\mu$ [188] in Equation 4.1. The carrier number fluctuation contribution is caused by the trapping mechanisms into the oxide and is given by [27]:

$$\begin{gathered}\frac{S_{I_D^2}}{I_D^2}\Big|_{\Delta N_{LV}} = \frac{q^4 N_T \lambda}{kTWLn^2 C_{OX}'^2 f} \\ \left[\frac{1}{2i_{d0}^2}\frac{i_{dlc}}{1+\lambda_c\left(q_s-q_k\right)} ln\left(\frac{q_s+0.5-\frac{\lambda_c}{2}i_{dlc}}{q_k+0.5-\frac{\lambda_c}{2}i_{dlc}}\right)+\left(\frac{\alpha\mu}{2}\right)^2+\frac{\alpha\mu}{1+q_s+q_k}\right]\end{gathered} \tag{4.2}$$

which is in full agreement with Equation 3.38 used for the 1/f noise model for LV-MOS with just replacing q_d with q_k. N_T is the oxide volumetric trap density per unit energy in $eV^{-1}cm^{-3}$ evaluated close to the Fermi energy level EF, k is the Boltzmann constant, n is the slope factor, f is the frequency, $\lambda = 0.1\,nm$ is the tunneling attenuation distance. In Equation 4.2, the term in brackets represents the bias-dependent part of the noise, depending on the normalized drain current:

$$i_{dlc} = \frac{q_s^2 + q_s - q_k^2 - q_k}{1 + \lambda_c (q_s - q_k)} \tag{4.3}$$

which is equivalent with Equation 2.35 of LV-MOS with just the replacement of q_d with q_k. λ_C is given by Equation 2.36 and is related to the velocity saturation of LV channel. The second and the third term of Equation 4.2 represent the influence of Coulomb scattering, with $\alpha \triangleq \alpha_c (-Q_{SPEC})$ and α_c is a parameter as in the 1/f noise model for LV-MOSFETs. The latter effect is notable in strong inversion, where a significant increase in gate referred noise may be observed.

Mobility fluctuation is described as in the 1/f noise model for LV devices [22, 24, 33] as [27]:

$$\frac{S_{I_D^2}}{I_D^2} |_{\Delta\mu_{LV}} = \frac{a_{\mathrm{H}} q^2}{KTWLnC'_{OX} f} \frac{1}{1 + q_s + q_k} \left[1 + \frac{ln(q_s/q_k)}{2(q_s - q_k)} \right] \tag{4.4}$$

which is equivalent with Equation 3.41 of LV-MOS with just the replacement of q_d with q_k. a_H is the unitless Hooge parameter and this fluctuation term appears mostly in weak-moderate inversion.

Drift Region Part

As it can be seen from Figure 2.16, the drift region has some differences from the LV part of an HV-MOSFET. In this region and because of the n-type doped drain, the mobile charge is accumulated. In the following, we propose a new charge-based model covering 1/f noise in the drift region. The gate oxide is extended by a certain length L_{OVD} at the surface of the drift region, and this could cause an extra contribution to 1/f noise because of trapping mechanism as mentioned earlier in this chapter even though there is no inversion in the drift region part. After the K-point, the current flow is spread through the volume underneath gate and field oxides in the drift region [101, 195, 202, 203]. This means that even though number of charges that flow at the surface of the gate oxide extension is small in comparison to the total amount of charges in the drift region, they still can be trapped/detrapped and thus generate a carrier fluctuation effect and contribute to 1/f noise. We can also assume that normalized charge at the edge of L_{OVD} is quite low in comparison with q_k, and we may neglect it. Carrier number fluctuation contribution from the surface of drift region across the gate extension can be expressed, following Equation 4.2, as [27]:

$$\frac{S_{I_D^2}}{I_D^2} |_{\Delta\mathrm{N}_{DRIFT}} = \frac{q^4 N_{TDR} \lambda}{kTWL_{OVD} C'^2_{OX} f} \frac{1}{2 i_{drift}} ln(1 + 2q_k) \tag{4.5}$$

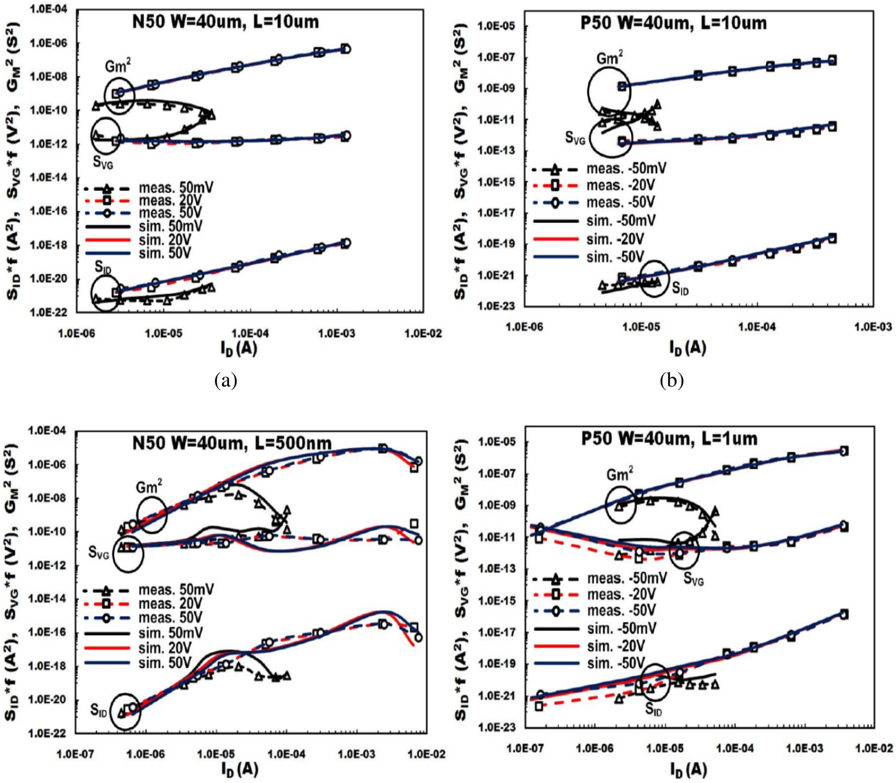
where N_{TDR} is the oxide volumetric trap density per unit energy in $eV^{-1}cm^{-3}$ in the extension of thin oxide in the drift region and i_{drift} is the normalized current in the drift region which is expressed as [32]:

$$i_{drift} = \bar{n}\frac{v_d - v_k}{1 + \frac{v_d - v_k}{e_C}} \tag{4.6}$$

where $\bar{n}$ is the average normalized carrier density in the drift region, $v_{d(k)} = V_{d(K)}/U_T$, and $e_C = E_C L_{DK}/U_T$, where L_{DK} is the length of the depletion area in the drift region. In saturation region, the quasi-saturation effect causes a dependence of 1/f noise on V_D at higher values of gate voltage. There, the velocity of electrons in drift region is saturated, while the channel is not yet saturated. This effect is covered by the DC model, so no extra noise equations are required.

4.3.3.3 Results

In Figures 4.4 and 4.5 [27], the PSD of 1/f noise is shown for the four N50, P50, N20, and P20 devices with long and short channel transistors. In each plot, output and input noise S_{ID} and S_{VG}, referred to $1\,Hz$, as well as g_m^2 are presented versus drain current. For each transistor, all those mentioned earlier are shown for three different values of V_D from linear region up to saturation with the maximum value of V_D depending on the device. Measured data and model are presented for each case. Note that one single model parameter set is used for each type of device, irrespective of channel length. The model shows a consistent behavior in all cases, and it provides a good overall qualitative fit with measured data. As a basic observation, the drain current noise follows the behavior of g_m^2. In cases where g_m^2 decreases, 1/f noise is also reduced. In long devices and in saturation, where the drift region does not play a very important role, the fitting is almost ideal. In linear region of long devices in strong inversion, the good fit was achieved because of the simple carrier number fluctuation model (Equation 4.5) through the thin oxide extension in the surface of the drift region. In Figure 4.6 [27], the different contributions to 1/f noise under linear and saturation modes are shown for long channel devices. The contribution of the drift part is significant—more clearly for NMOS and less for PMOS—only in linear mode strong inversion. In saturation, even more so for short channel devices, the noise from the drift part is dominated by channel noise, by more than an order of magnitude, at all levels of current. In short devices, results are also quite good with the exception of the short N20 device, where noise is overestimated in the moderate current range. In general, the model seems to follow the measurements and in most cases the results are satisfactory. Table 4.1 [27] shows the corresponding parameters extracted for all four types of devices. One set of parameters covers all channel lengths and bias conditions of a given type of transistor. Generally speaking, carrier number fluctuation model of the LV part is responsible for the increase of noise in moderate and strong inversion. More specifically in strong inversion, the contribution of Coulomb scattering to the carrier number fluctuation is dominant while in moderate inversion is insignificant whereas mobility fluctuation effect is dominant in weak inversion regime [22, 24, 33, 186]. In p-channel devices, this effect is clearly apparent (increase of input referred noise in weak inversion) resulting in a nonzero value of the parameter α_H, while it is not observed in the present n-channel devices. As for carrier number fluctuation related to the drift region, it becomes significant in linear region, strong inversion of long devices as it is clear in Figure 4.6. In summary, a consistent model of 1/f noise in HV-MOSFETs including the contribution of the drift part is presented for the first time. Drift region noise is apparent only in long devices in strong inversion and linear mode.



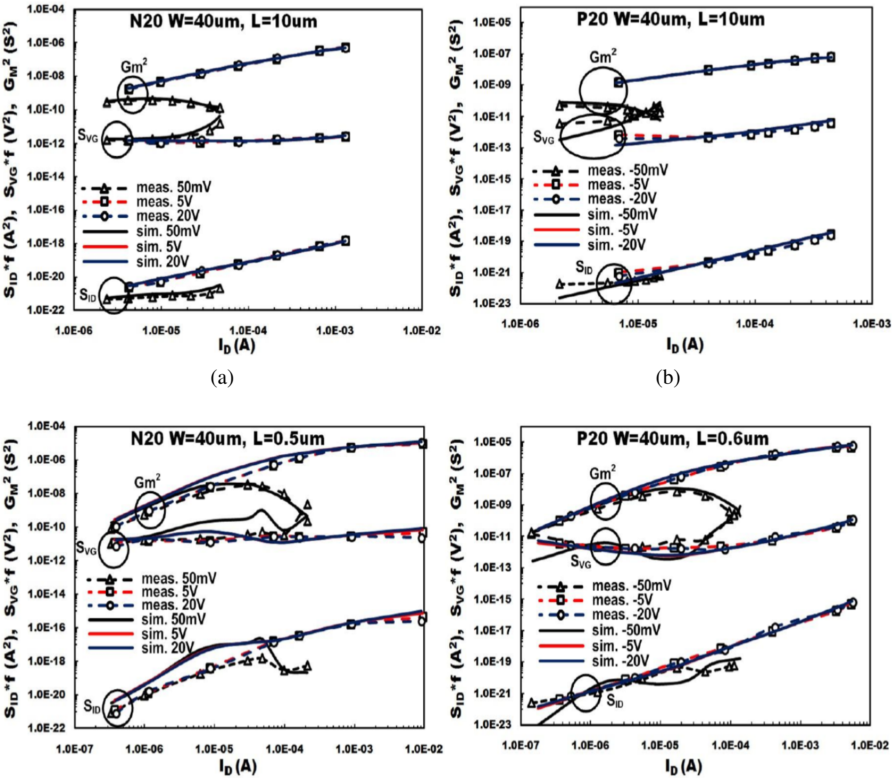
(a)

(b)

(c)

(d)

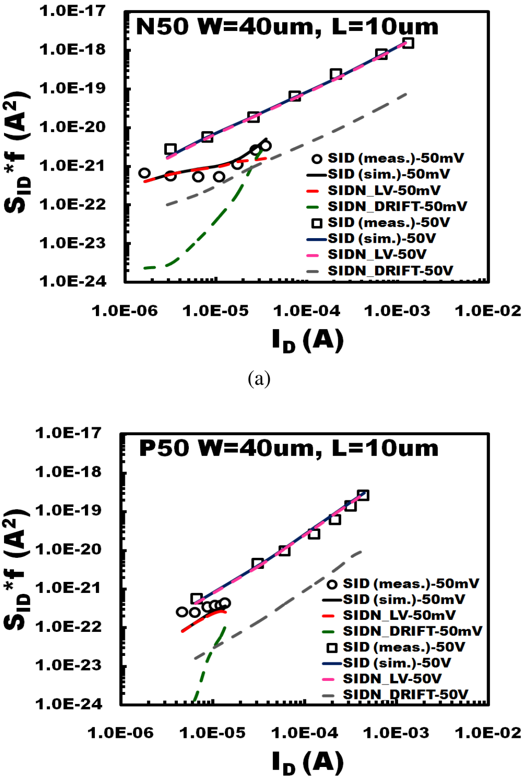
Figure 4.4: 1/f noise PSD S_{ID} and S_{VG}, referred to as $1\,Hz$, as well as g_m^2 , versus drain current I_D (with $|V_G|$ up to $4\,V$), for N50 (a,c) and P50 (b,d) transistors. (Upper row) Long device ($W = 40\,\mu m$, $L = 10\,\mu m$). (Lower row) short device ($W = 40\,\mu m$, $L = 0.5\,\mu m$ for N50 and $W = 40\,\mu m$, $L = 1\,\mu m$ for P50). Linear ($|V_D| = 50\,mV$) and saturation ($|V_D| = 20\,V, 50\,V$) modes are shown for both (markers) measurement and (lines) model.



(a) (b)

(c) (d)

Figure 4.5: 1/f noise PSD S_{ID} and S_{VG}, referred to as $1\,Hz$, as well as g_m^2 , versus drain current I_D (with $|V_G|$ up to $4\,V$), for N20 (a,c) and P20 (b,d) transistors. (Upper row) Long device ($W = 40\,\mu m$, $L = 10\,\mu m$). (Lower row) short device ($W = 40\,\mu m$, $L = 0.5\,\mu m$ for N20 and $W = 40\,\mu m$, $L = 0.6\,\mu m$ for P20). Linear ($|V_D| = 50\,mV$) and saturation ($|V_D| = 5\,V, 20\,V$) modes are shown for both (markers) measurement and (lines) model.



(a)

(b)

Figure 4.6: 1/f noise PSD S_{ID} and S_{VG}, referred to $1\,Hz$, versus drain current I_D (with $|V_G|$ up to $4\,V$), for (a) N50 and (b) P50 transistors with $W = 40\,\mu m$, $L = 10\,\mu m$ both for Linear ($|V_D| = 50\,mV$) and saturation ($|V_D| = 50\,V$) modes. Effects of carrier number fluctuation effect from LV part ($SIDN_{LV}$) and drift region [(dashed) ($SIDN_{DRIFT}$)] is shown. (Markers) measurements; (lines) model.

Parameter	Units	N50	P50	N20	P20
N_T	$eV^{-1}cm^{-3}$	$1.87.10^{16}$	$6.2.10^{14}$	$1.87.10^{16}$	$1.87.10^{14}$
a_C	VsC^{-1}	$3.0.10^{3}$	85.10^{3}	$2.2.10^{3}$	155.10^{3}
a_H	-	0	$1.35.10^{-9}$	0	5.10^{-9}
E_{CN}	V/m	30.10^{6}	$5.47.10^{6}$	$1.4.10^{6}$	$5.87.10^{6}$
N_{TDR}	$eV^{-1}cm^{-3}$	$1.25.10^{13}$	$6.2.10^{12}$	$6.2.10^{12}$	$6.2.10^{12}$

Table 4.1: 1/f Noise HV model parameters for both 50 and $20\,V$ devices under test

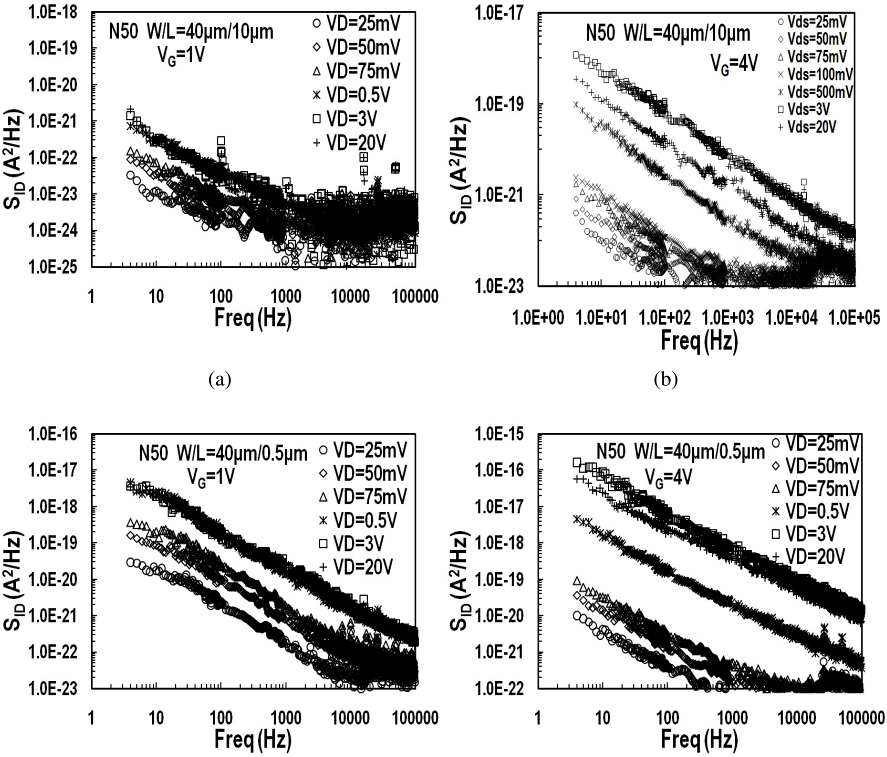
As a matter of course, the values of extracted 1/f noise parameters of the LDMOSFETs may need to be re-adjusted if changes are made to the implementation of the IV model. Furthermore, apart from the simulations of the Verilog-A code with Spectre simulator, parts of the model evaluation such as parameter extraction procedure, took place by just solving analytically all the equations from IV to 1/f noise level and this also resulted in different values of the parameters. Moreover, despite the fact that all the sections of this chapter refer to the same type of devices, each time we focus on slightly different operating conditions. Finally, in Table 4.1, one set of 1/f noise parameters was extracted for both long and short transistor of each device type which is not the case in the rest of this chapter. As a result of all the above notices, tables with the values of the 1/f noise parameters that follow in following sections might have different values than in Table 4.1, for the same devices.

4.3.4 Analysis of V_D Dependence of 1/f Noise in HV-MOSFETs - Model Validation

The behavior and dependence of 1/f noise versus drain bias in high-voltage (HV-) MOSFETs is examined in this section of the Thesis. Flicker noise of $50\,V$ n- and p-channel HV-MOSFETs which was measured over a large range of gate and drain bias conditions, is used for this purpose. Drain voltage steps were chosen very small in linear region while enough points were also measured in saturation regime up to $20\,V$. Recent work on characterization and modeling on flicker noise of HV devices proved that while the overall noise is mostly dominated by the noise originating in the channel, the drift region generated noise is apparent and comparable to channel noise only in linear operation especially in strong inversion region of long channel devices [27, 195, 198]. In order this to be clear, we focus here on the behavior of flicker noise versus drain bias for all inversion regime, providing a comprehensive analysis and detailed modeling of 1/f noise in LDMOSFETs [34] based on our recently established 1/f noise model presented in the previous Section 4.3.3 [27].

4.3.4.1 Experimental Data Description

Measurements were performed on both n- and p-channel $50\,V$ MOSFETs of the $0.35\,\mu m$ HV-MOS technology from ams AG as detailed before in Section 4.3.3. Wide-long transistors with $W = 40\,\mu m$, $L = 10\,\mu m$ for both N50 and P50 devices and wide-short transistors with $W = 40\,\mu m$, $L = 0.5\,\mu m$ for N50 and $W = 40\,\mu m$, $L = 1\,\mu m$ for P50 were measured at different V_G and V_D values. Steps of drain voltage were chosen very small in linear region from $25\,mV$ up to $1\,V$ while enough points were also measured in saturation regime up to $20\,V$. Gate voltage values were also chosen from weak to strong inversion regime. The frequency range was from $4\,Hz$ up to $100\,kHz$. Slope AF of 1/f noise was considered ideally equal to 1. In Figure 4.7, the measured PSD of drain current versus frequency is presented for N50 long and short transistors at different bias conditions. Both at low and high gate voltage, noise is increasing in linear region while it seems to be saturated for higher V_{DS} values in a similar way as an output characteristic of a MOS device [34].

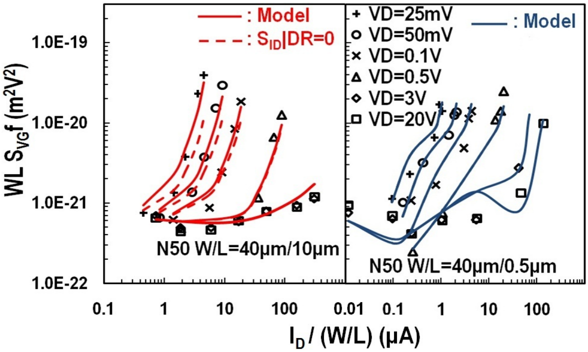


(a) (b)

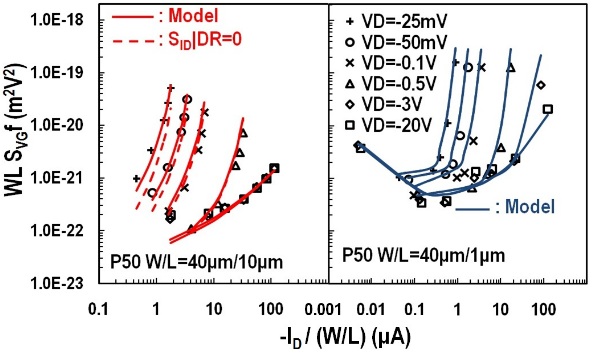
(c) (d)

Figure 4.7: PSD of 1/f noise drain current S_{ID} vs. frequency for $50\,V$ long (a,b) and short (c,d) n-channel LDMOSFETs at $V_G = 1\,V$ (a,c) and $V_G = 4\,V$ (b,d) for $(V_D = 25\,mV, 50\,mV, 75\,mV, 100\,mV, 500\,mV, 3\,V, 20\,V)$

4.3.4.2 Results



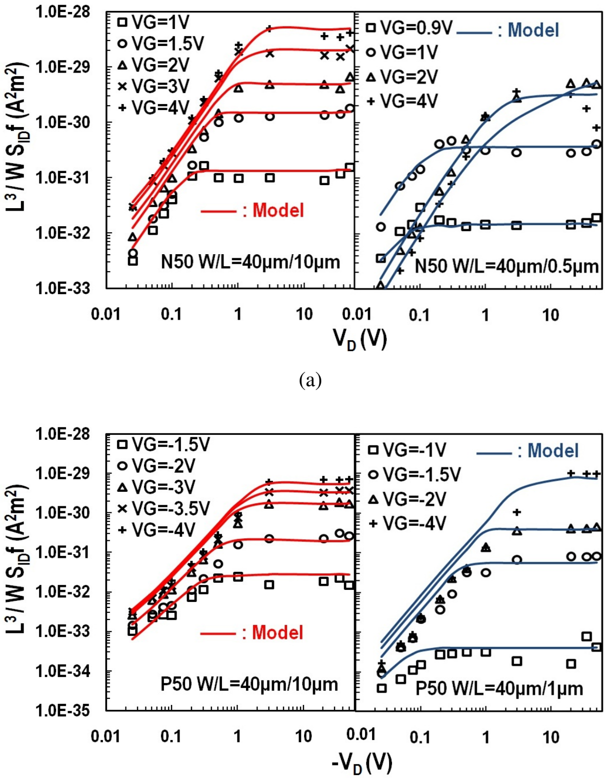
(a)



(b)

Figure 4.8: Input noise S_{VG}, normalized with WL, referred to $1\,Hz$, at different V_D values, vs. area normalized drain current $I_D/(W/L)$, for N50 (a) and P50 (b) transistors. Long (left subplot) and short device (right subplot) are shown; markers: measured, lines: model (no drift region noise: dashed lines).

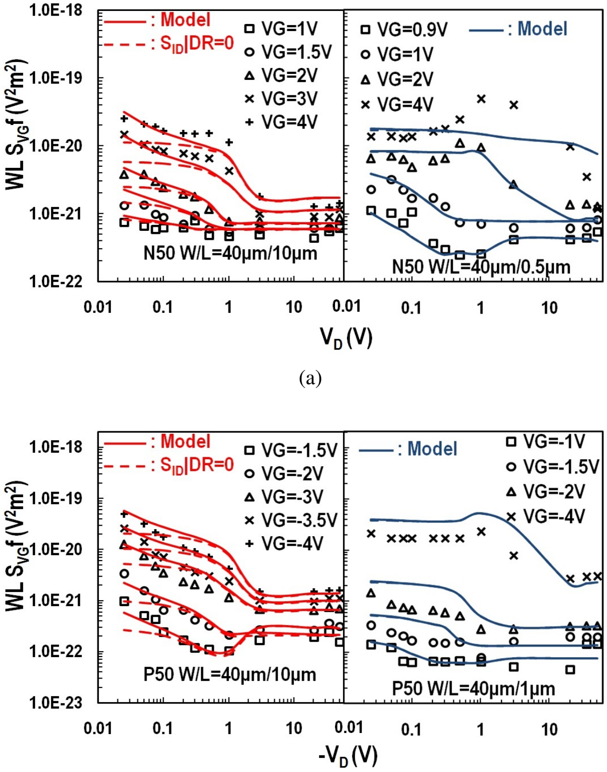
The main goal of the present analysis is to examine thoroughly the behavior of 1/f noise versus V_D in HV devices. As it has already been mentioned, the only significant contribution of 1/f noise coming from the drift region in these devices, takes place in linear region, strong inversion and for long channel devices [27, 195]. It is caused by a carrier number fluctuation effect at gate oxide extension in drift region which becomes comparable to the noise coming from the channel at the above conditions. Our recently established model includes this effect through Equation 4.5. A first validation of the model with the data referred to this section is shown in Figure 4.8 [34] both for long and short n- and p-channel devices. Input noise $S_{VG} = S_{I_D^2}/g_m^2$, normalized with device area WL and referred to $1\,Hz$ versus normalized drain current $I_D/(W/L)$ are shown for all different V_{DS} values from deep linear to high saturation region where the model seems very consistent with data. The model without the contribution of drift region is also shown and as it was expected it differs from the full model in linear operation and strong inversion of long devices, where noise from drift is significant [27, 34].



(a)

(b)

Figure 4.9: Output noise S_{ID}, multiplied with L^3/W, referred to $1\,Hz$, at different V_G values, vs. drain voltage V_D, for N50 (a) and P50 (b) transistors. Long (left subplot) and short device (right subplot) are shown; markers: measured, lines: model (no drift region noise: dashed lines).



(a)

(b)

Figure 4.10: Input noise S_{VG}, multiplied with WL, referred to $1\,Hz$, at different V_G values, vs. drain voltage V_D, for N50 (a) and P50 (b) transistors. Long (left subplot) and short device (right subplot) are shown; markers: measured, lines: model (no drift region noise: dashed lines).

An appropriate way to fully understand the drain bias-dependence of 1/f noise and examine if our model [27] is adequate, is to express 1/f noise versus drain bias for different inversion conditions. The results in Figures 4.9, 4.10 [34] are quite convincing regarding the consistency of the model in all bias conditions. In Figure 4.9, normalized S_{ID} and in Figure 4.10, normalized S_{VG} both referred to $1\,Hz$, are shown versus drain voltage from weak to strong inversion both for long and short n- and p-channel devices. S_{VG} is multiplied by the area $W \cdot L$ to factor out the device dimension effect, while S_{ID} is multiplied by $L^3 \cdot W$ to eliminate device dimension and transconductance effects. Markers represent the measured data while lines the model. Dashed lines in S_{VG} plots (Figure 4.10) show the model without the drift region effect on noise. We first notice that in Figure 4.9, output noise S_{ID} versus V_D

resembles an output characteristic (I_D versus V_D) since it increases in linear region and it reaches saturation after a specific value of drain voltage. This V_{DSAT} seems to increase with inversion level in agreement with the basic IV theory. Furthermore in the n-channel short device, quasi-saturation and its effect on 1/f noise is apparent. We have mentioned previously in this chapter that apart from linear region, 1/f noise arising from drift region can also contribute to the total 1/f noise of the device in saturation mode through the quasi-saturation effect. This had not been clearly observed until now. Our model can follow this behavior of noise at high gate voltage values due to quasi-saturation effect, through the correct and complete DC model [32]. Moreover in the same short N50 device where drain current is quite high, there seems to be a decrease of noise in high drain and gate voltage bias ($V_G = 4\,V$, $V_D = 20\,V$). This is probably due to self-heating effect which is not covered by the model yet. The contribution of the drift region is best observed in S_{VG} (Figure 4.10) both for n- and p-channel long transistors. The dashed line represents the model without drift region effect and as it can be seen it remains constant for linear region and for higher gate voltages. But measured S_{VG} shows an increase in the above conditions which is perfectly predicted by the full model. In Table 4.2 [34], the values of the parameters of the model for each device are addressed. The drift region noise is apparent only in long channel devices.

Parameter	Units	N50 40x10	N50 40x05	P50 40x10	P50 40x1
N_T	$eV^{-1}cm^{-3}$	$1.7.10^{16}$	1.10^{16}	5.10^{14}	2.10^{14}
a_C	VsC^{-1}	4.10^{3}	3.10^{3}	80.10^{3}	135.10^{3}
a_H	-	0	0	0	$1.5.10^{-7}$
N_{TDR}	$eV^{-1}cm^{-3}$	1.10^{11}	0	5.10^{10}	0

Table 4.2: 1/f Noise HV model parameters for $50\,V$ devices under test

If we compare the values of 1/f noise parameters from Tables 4.1, 4.2, we can observe some slight but also some more important differences despite the fact that they refer to the same N50, P50 transistors. At a first glance this does not make sense but if we look deeper to what happened there is an explanation. First of all, values in both cases were extracted from simulations of the Verilog-A code implemented for the new 1/f noise model for LDMOSFETs. While the operating conditions are similar, they are not the same. In case of Table 4.1 [27], data and model were fitted at three V_D values ($|V_D| = 50\,V, 20\,V, 50\,mV$) with only one at linear region ($|V_D| = 50\,mV$). On the other hand, in Table 4.2 [34], more attention was given to linear region with more than five V_D values lower than $|1|\,V$. Moreover, while in first case one parameter set was extracted for both long and short channel lengths, in the second one a parameter set was used for each channel length. Finally, as far as Verilog-A code implementation is concerned, there is a difference of q_k calculation between the two approaches. For all the above reasons, parameters N_T, a_C, a_H have some numerical differences which are not very significant though. The parameter N_{TDR} on the other hand has a quite remarkable difference - almost two decades - between the two approaches. This can be justified due to a different implementation of statement instruction of Verilog-A that was adopted after the work related to Table 4.1, was published [27]. Briefly, while in first approach (Table 4.1), flicker noise was calculated both between Source and K-point node (LV part) and K-point and Drain node (Drift part) and the total flicker noise calculation was taking into consideration these parts, in the second approach (Table 4.2) the total flicker noise was directly calculated from Source to Drain node. The latter seems physically more correct since the noise equations are charge-based and thus bias-dependent so they can predict where each contribution will dominate and where it will be negligible.

4.3.5 Methodology for 1/f Noise Parameter Extraction for High-Voltage MOSFETs

Flicker noise in high-voltage MOSFETs has been given considerable attention and has contributed to the basic understanding of 1/f noise mechanisms in these devices [193, 194, 195]. Compact models have been established [27, 34, 198]; however, no complete procedure has been proposed so far for the extraction of the 1/f noise parameters related to all noise contributions in a wide range of operation of the HV devices. Former work has proposed a simple noise parameter extraction method for standard MOSFETs [170, 184, 186] but in HV devices, additional noise sources contribute to total 1/f noise.

As detailed before, a physical charge-based model is used to cover the low-voltage part of the HV-MOSFET – bearing many similarities with the EKV3 compact model [31] – while the drift region part also uses a charge-based modeling approach [32]. Our recently established 1/f noise model for HV-MOSFETs [27] exploits this charge-based framework. According to this 1/f model, the channel region remains the dominant contributor to flicker noise. Carrier number fluctuation, Coulomb scattering, mobility fluctuation and series resistance are the dominant flicker noise sources from weak to strong inversion region for low-voltage (LV-) MOSFETs [22, 170, 172, 173, 176, 184, 186] as well as for the LV-channel part of HV-MOSFETs [27, 34]. The carrier number fluctuation effect, which prevails in moderate inversion, is the result of the trapping/detrapping effect in the oxide and is described by parameter N_T which represents the number of trapped charges per unit area. The Coulomb scattering mechanism contributes to noise in early strong inversion by affecting the mobility of the device and is described by parameter a_C which is the Coulomb scattering coefficient. The mobility fluctuation effect is dominant in weak inversion and is described by parameter a_H. Series resistance contribution can influence only at high currents and is characterized by the $S_{\Delta R}$ parameter. The above effects are correctly introduced in the EKV3 1/f noise model for LV-MOSFETs [22, 24, 33] as well as in our 1/f noise model for LDMOS transistors [27, 34]. Series resistance effect was added later with same approach as Equation 3.46 with replacing q_d with q_k:

$$\frac{S_{I_D^2}}{I_D^2}\,|_{\Delta R_{LV}} \simeq S_{\Delta R^2} G_{SPEC}^2 \left(q_s^2+q_k^2\right) \tag{4.7}$$

and thus Equation 4.1 becomes:

$$\frac{S_{I_D^2}}{I_D^2} = \frac{S_{I_D^2}}{I_D^2}\,|_{\Delta N_{LV}} + \frac{S_{I_D^2}}{I_D^2}\,|_{\Delta \mu_{LV}} + \frac{S_{I_D^2}}{I_D^2}\,|_{\Delta R_{LV}} + \frac{S_{I_D^2}}{I_D^2}\,|_{\Delta N_{\mathrm{DRIFT}}} \tag{4.8}$$

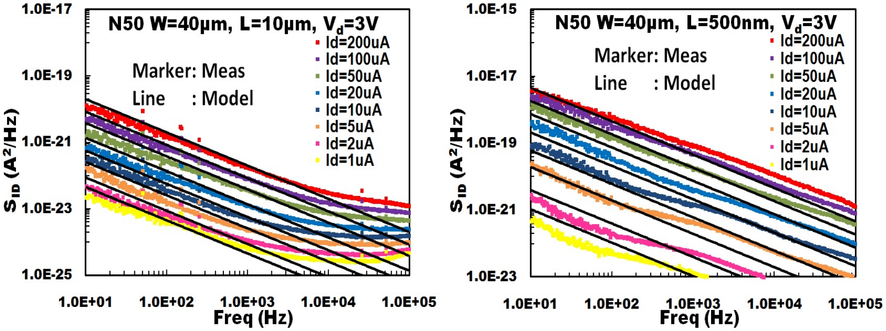
Furthermore, short channel effects like quasi-saturation affect 1/f noise and are accounted for via the charge-based IV model [32]. In HV-MOSFETs, an additional noise source is attributed to the extension of the gate oxide in drift region which affects the whole device especially for long channel and under low drain bias conditions. A carrier number fluctuation model is applied in this region. This effect is described by parameter N_{TDR}, which is much smaller than N_T and can be significant only in linear region for long channel devices, where noise coming from the channel is low enough to be comparable to noise coming from the drift region [27, 34].

In this section, the 1/f noise parameter extraction methodology is divided into two procedures. Firstly, a simpler one for flicker noise arising from the LV-channel of the LDMOS device [199] and after the most complete one which refers to the whole device including drift region as well as to all possible effects that can create 1/f noise [35].

4.3.5.1 Simple 1/f Noise Parameter Extraction Method for the LV part of LDMOSFETs

An 1/f noise parameter extraction method for HV-MOSFETs at $3\,V$ drain bias is presented in this section. In this region the overall noise is mostly dominated by the noise originating in the channel. The bias-dependence of flicker noise, related to transconductance-to-current ratio, allows for an easy means to determine related noise parameters. Though measured data are limited, parameters related to carrier number fluctuation effect may be found. $50\,V$ n-channel HV-MOSFETs are investigated for long as well as short channel lengths. The parameter extraction method is applied to the recently established 1/f noise model for HV-MOSFETs [27], showing a good agreement among model and experimental data.

For the purpose of the present case, flicker noise data of both long and short N50 transistor performed at $3\,V$ drain bias for 7 current points, were used. Under these operating conditions, we assume that channel contribution in 1/f noise will be dominant. The current ranges from moderate inversion to the lower end of strong inversion, where carrier number fluctuation is the main noise contributor. The goal here is to provide a helpful flicker noise parameter extraction methodology when biasing is such that 1/f noise is dominated by noise generated in the channel region, due mainly to carrier number fluctuation. Starting from CV-IV data, fundamental quantities, such as I_{SPEC} are calculated [204], which are then used in noise equations for parameter extraction. In Figure 4.11 [199], the power spectral density S_{ID} is shown both for the measurements and the model [27]. The model is simulated after the extraction of the parameters in this section and its consistency is good for all bias conditions.

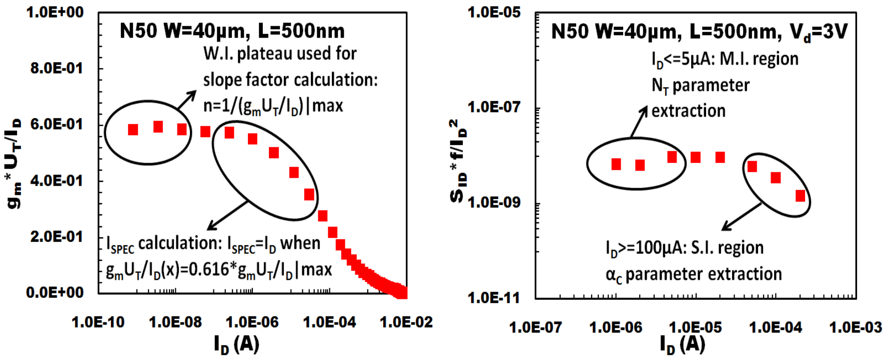


(a) (b)

Figure 4.11: PSD of drain current noise S_{ID} for long (a) and short (b) N50 transistors at $V_D = 3\,V$ for 8 different I_D values from $1\,\mu A$ to $200\,\mu A$. Long device ($W = 40\,\mu m$, $L = 10\,\mu m$) and short device ($W = 40\,\mu m$, $L = 0.5\,\mu m$).

Extraction of IV Parameters

It is essential to have a correct DC model in order to implement an 1/f noise model, since certain quantities of the DC model, such as transconductance (g_m), slope factor (n), specific current (I_{SPEC}) and electron mobility (μ), are used in the noise equations. In order to calculate the noise parameters these quantities must be extracted first. g_m can be calculated as the derivative of the measured drain current. For obtaining n, I_{SPEC} and μ, a specific procedure must be followed [204]. Transconductance-to-current ratio ($g_m U_T / I_D$) shown in Figure 4.12a [199], is very helpful in the extraction of these DC parameters. In the weak inversion regime n can be calculated as: $n = \frac{1}{g_m U_T / I_D}\big|_{max}$ while again from the transconductance-to-current ratio plot, I_{SPEC} corresponds to the current where $g_m U_T / I_D$ equals 0.616 of its maximum value [204]. Specific current is defined as $I_{SPEC} = 2nU_T^2 \mu C'_{OX} \frac{W}{L}$ and given that $T_{OX} = 15\,nm$, electron mobility can be easily calculated. Figure 4.13 [199] shows a general flowchart of the parameter extraction procedure where the first three blocks refer to IV parameter extraction.



(a) (b)

Figure 4.12: a) Transconductance-to-current ratio versus I_D, b) 1/f noise power spectral density referred to $1\,Hz$ and divided by I_D^2, versus I_D, for a short channel NMOS $50\,V$ device.

1/f Noise Parameter Extraction

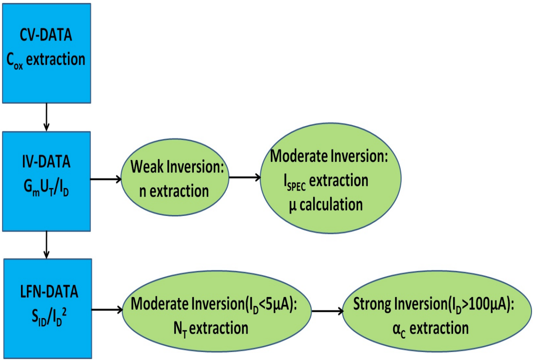


Figure 4.13: 1/f noise parameter extraction flow.

The basic simpler carrier number fluctuation model in the channel region is described by Equation 3.34 [177, 184, 186]. Of course things are somewhat more complicated as far 1/f noise in LDMOSFETs is concerned [27], but this formula can be considered sufficient for a first evaluation of 1/f noise parameters. Figure 4.12b [199] shows the bias-dependence of 1/f noise referred to $1\,Hz$. In all cases the normalization was applied from $10\,Hz$ to $1\,kHz$. Each of the noise parameters, N_T, and α_C, can be extracted from different inversion levels. For $I_D < 5\,\mu A$ in the moderate inversion region, the second term of Equation 3.34 related to Coulomb scattering can be neglected so that:

$$\frac{S_{I_D^2}}{I_D^2}\,|_{\Delta N}= \frac{KTq^2N_T\lambda}{WLC_{OX}'^2 f}\left(\frac{g_m}{I_D}\right)^2 \tag{4.9}$$

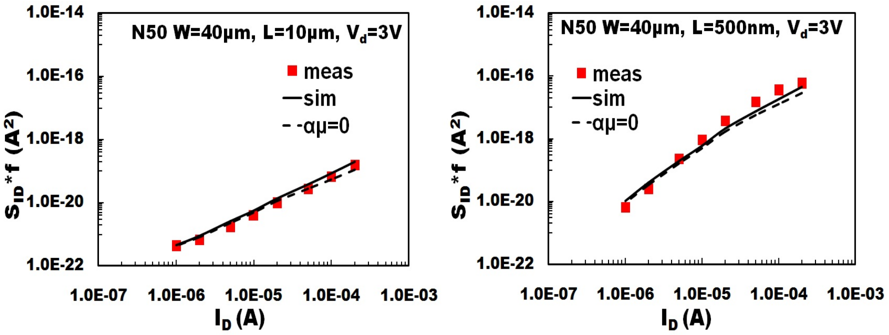
In this way the parameter N_T can be determined. For $I_D > 100\,\mu A$, the Coulomb scattering effect dominates and from Equation 3.34, the α_C parameter can be extracted. This procedure is shown in the last two blocks of Figure 4.13 [199]. All the parameters that were extracted from IV and 1/f noise data, are shown in Table 4.3 [199], for long and short n-channel devices.

Parameter	Units	N50 40x10	N50 40x05
n	-	1.32	1.35
I_{SPEC}	A	$1.4.10^{-6}$	20.10^{-6}
μ	$cm^2\,(Vs)^{-1}$	740	1230
N_T	$eV^{-1}cm^{-3}$	$1.62.10^{16}$	$2.7.10^{16}$
a_C	VsC^{-1}	3.10^3	6.10^3

Table 4.3: 1/f Noise HV model extracted parameters for n-channel $50\,V$ devices under test

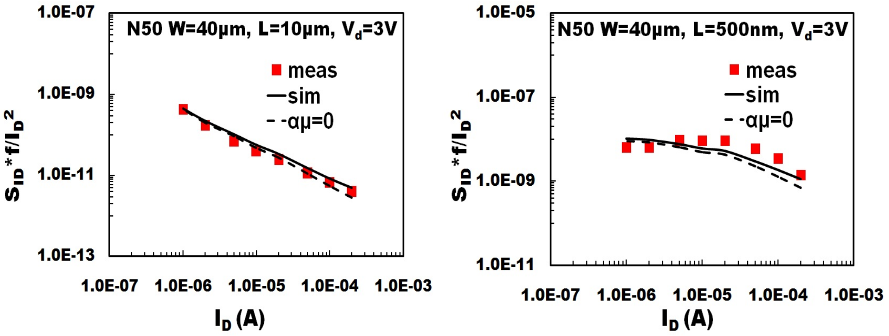
Model Validation

As mentioned above, a new complete 1/f noise model for HV-MOSFETs was recently established [27]. The values of the noise parameters extracted according to the previous paragraph were used for the simulations. Modeling results are shown in Figures 4.14, 4.15, 4.16 [199] both for long and short n-channel devices. Output noise, output noise divided by I_D^2, as well as input noise S_{VG} versus I_D are shown. In each case, the complete model is represented by a thick line and the model without the Coulomb scattering effect ($\alpha\mu = 0$) is represented by a dashed line. It is clear that these two lines almost coincide in moderate inversion regime which means that indeed in this region the Coulomb scattering effect on noise is negligible. Generally speaking, the model shows a very consistent behavior especially for long n-channel devices. For the short device, results are not perfect due to the limited current range for the extraction of the parameter α_C. For such a device, the highest level of measured current ($I_D = 200\,\mu A$) is just slightly above the onset of strong inversion. On the other hand, the decrease of noise observed in S_{VG} for the same short channel device at lower currents may be regarded as non-typical, and is actually a result of the slight departure from 1/f in the noise spectra of the short channel device, as seen in Figure 4.11. We note that in Table 4.3, the 1/f noise parameters for the long and short channel devices are reasonably close. Furthermore, they are quite close to the values from Tables 4.1 [27] and 4.2 [34] which confirms the consistency of the method.



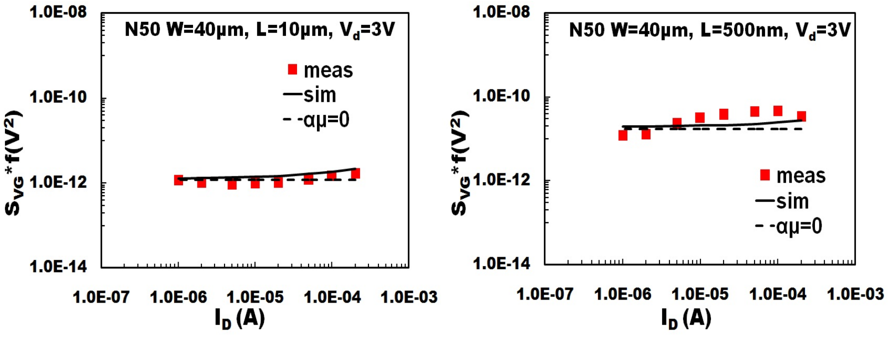
(a) (b)

Figure 4.14: 1/f noise PSD S_{ID}, referred to $1\,Hz$, vs. drain current I_D, for $50\,V$ transistors. a) Long device ($W = 40\,\mu m$, $L = 10\,\mu m$). b) Short device ($W = 40\,\mu m$, $L = 500\,nm$); measurement (markers) and model (lines).



(a) (b)

Figure 4.15: 1/f noise PSD S_{ID}/I_D^2, referred to $1\,Hz$, vs. drain current I_D, for $50\,V$ transistors. a) Long device ($W = 40\,\mu m$, $L = 10\,\mu m$). b) Short device ($W = 40\,\mu m$, $L = 500\,nm$); measurement (markers) and model (lines).



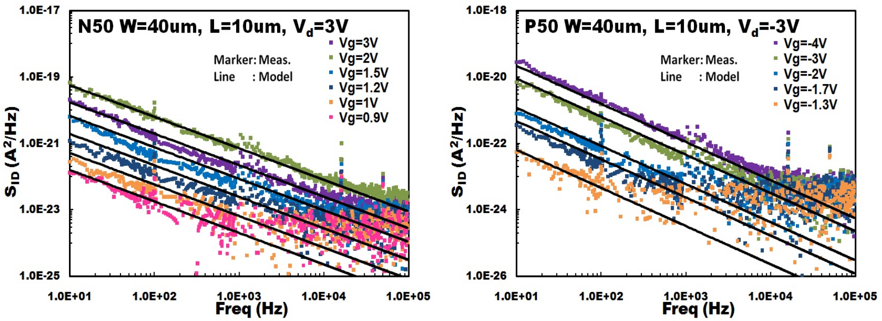
(a) (b)

Figure 4.16: 1/f noise PSD S_{VG}, referred to $1\,Hz$, vs. drain current I_D, for $50\,V$ transistors. a) Long device ($W = 40\,\mu m$, $L = 10\,\mu m$). b) Short device ($W = 40\,\mu m$, $L = 500\,nm$); measurement (markers) and model (lines).

4.3.5.2 Complete 1/f Noise Parameter Extraction Method for LDMOSFETs

The simple 1/f noise parameter extraction presented in the previous section has the advantage to be quite straightforward, but nevertheless has some important disadvantages. Firstly, it is limited to the extraction of parameters related only to the channel part and not to the drift region effect on 1/f noise. Even for the LV part, parameters related to channel carrier number fluctuation effect, N_T, and α_C, are the only to be extracted while mobility fluctuation or series resistance effects are not taken into consideration. A detailed 1/f noise parameter extraction method for high-voltage (HV) MOSFETs at low ($50\,mV$) and medium ($3\,V$) drain biases is proposed for first time [35]. In $V_D = 3\,V$ region, noise coming from the channel is dominant while in linear region there is an extra contribution of noise from the drift region part especially for long channel devices in strong inversion region. Flicker noise of $50\,V$ and $20\,V$ n- and p-channel HV-MOSFETs was measured over a large current range from weak to strong inversion [27], making possible the extraction of the noise parameters related to the different noise contributions, such as mobility fluctuations in low current regime, carrier number fluctuations and Coulomb scattering in medium and high current regime. In some cases, series resistance noise contribution especially at high current is apparent as well. The parameter extraction procedure is devised for a recently established charge-based flicker noise model for HV-MOSFETs [27]. Noise parameters related to the carrier number fluctuation effect in the gate oxide extension in drift region are also extracted in high current regime of long channel devices under low drain bias condition. For the description of the non ideal slope of flicker noise spectra $1/f^{AF}$, the frequency exponent AF may take values slightly different from 1. As a first step, before the noise parameters related to the above effects are extracted, AF should be determined directly from noise data and used in the following procedure for the extraction of noise parameters.

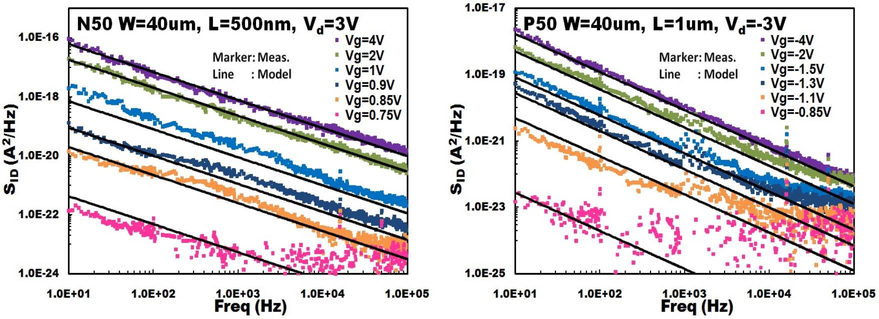
A complete noise parameter extraction procedure demands a reliable evaluation of some CV-IV fundamental quantities which are then used in noise equations for parameter extraction, such as the specific current I_{SPEC} [204]. As it has been shown in Figures 2.25, 2.26, the IV part of the recently established model [32] predicts very well the DC behavior of such devices for all regions of operation for a $50\,V$ NMOS device. Figures 4.17, 4.18, 4.19 [35] show the power spectral density S_{ID} both for the measurements and the model [27]. $50\,V$ long and short n- and p-channel transistors are shown at $V_D = 3\,V$ while same short devices are shown at $V_D = 50\,mV$. The consistency of the model is good for all bias conditions. The range of frequencies between $10\,Hz$ and $100\,Hz$ is closest to 1/f and is used for the extraction of noise parameters. The extracted parameters are used for the simulations shown in Figures 4.17, 4.18, 4.19.



(a)

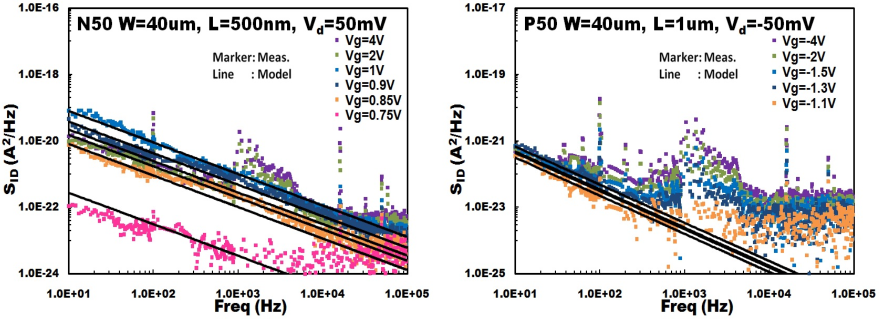
(b)

Figure 4.17: Power spectral density of drain current noise S_{ID} for $50\,V$ long (a) n- and (b) p-channel HV-MOSFETs at $V_D = 3\,V$, at different V_G values. The model (lines) accounts for spectral dependence slightly differing from 1/f.



(a) (b)

Figure 4.18: Power spectral density of drain current noise S_{ID} for $50\,V$ short (a) n- and (b) p-channel HV-MOSFETs at $V_D = 3\,V$, at different V_G values. The model (lines) accounts for spectral dependence slightly differing from 1/f.



(a) (b)

Figure 4.19: Power spectral density of drain current noise S_{ID} for $50\,V$ short (a) n- and (b) p-channel HV-MOSFETs at $V_D = 50\,mV$, at different V_G values. The model (lines) accounts for spectral dependence slightly differing from 1/f.

Extraction of IV Parameters

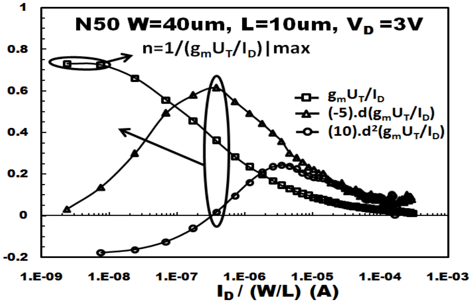


Figure 4.20: Transconductance-to-current ratio with its 1st and 2nd order derivative versus normalized drain current, for a long channel NMOS $50\,V$ device.

The parameter extraction procedure presented in this work, is based on the recently established charge-based 1/f noise model for HV-MOSFETs [27]. Some fundamental IV quantities, such as normalized charges (q_s, q_k), slope factor (n), specific current (I_{SPEC}) and electron mobility (μ), are used in the 1/f noise equations as presented above [27]. In order to extract the 1/f noise parameters, these quantities must be extracted first. As described in previous section, they are calculated by the IV model but in this work we evaluate them analytically from specific CV-IV data. Values coming from simulation are just used for confirmation. T_{OX} of these devices is known ($15\,nm$) while the slope factor n, the specific current I_{SPEC} and mobility μ are calculated from $g_m U_T/I_D$ measured data [199, 204]. In Figure 4.20 [35], the transconductance-to-current ratio $g_m U_T/I_D$ with its 1st and 2nd order derivative versus drain current normalized with device aspect ratio is shown for a long NMOS $50\,V$ transistor. Effective length and width of the device are taken from the IV model. In weak inversion regime n can be calculated as: $n = \frac{1}{g_m U_T/I_D}\,|_{max}$ while when the 2nd order derivative of transconductance-to-current ratio equals zero, drain current equals to: $I_D = I_{SPEC}(1+\sqrt{2})/2$ and from there I_{SPEC} is extracted through which electron mobility μ can be calculated. The following equations permit the calculation of normalized charges through the measured transconductance (g_m) and the calculated I_{SPEC} [22]:

$$\begin{gathered}\frac{g_m}{G_{spec}} = \frac{q_s - q_k}{n} \\ \frac{I_D}{I_{SPEC}} = (q_s - q_k) + (q_s + q + 1)\end{gathered} \tag{4.10}$$

Steps 1 and 2 of Figure 4.21 [35] describe the extraction of CV and IV quantities.

1/f Noise Parameter Extraction

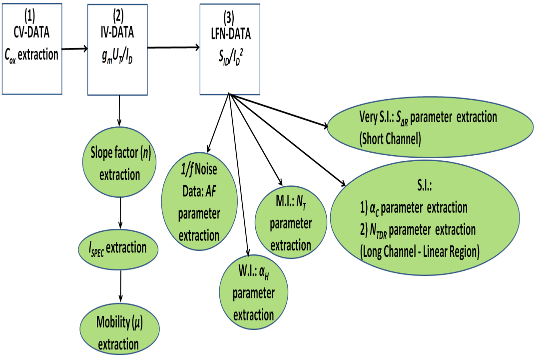
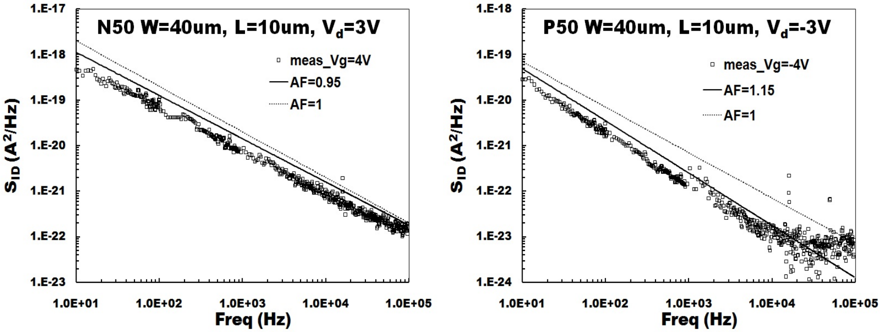


Figure 4.21: 1/f Noise parameter extraction flow chart.

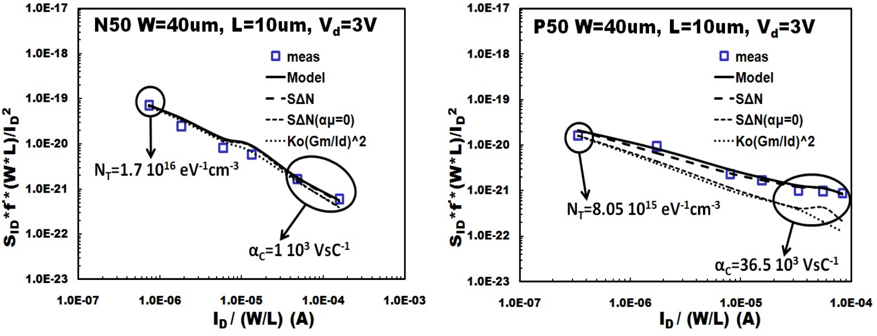


(a) (b)

Figure 4.22: Power spectral density of drain current noise S_{ID} for $50V$ long a) n- and b) p-channel HV-MOSFETs at $|V_D| = 3V$, $|V_G| = 4V$ for the extraction of frequency exponent AF of flicker noise.

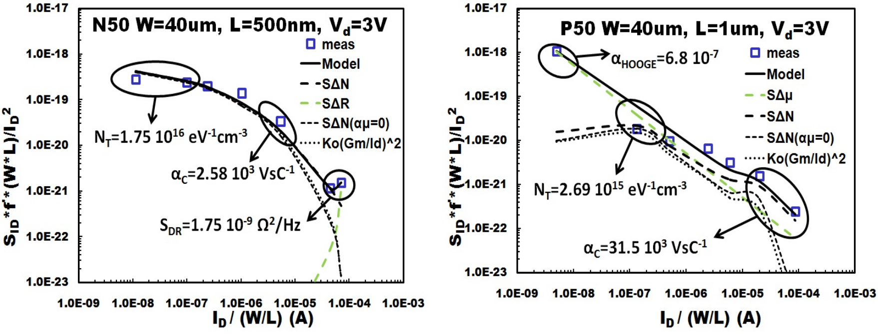
Step 3 of Figure 4.21 [35] describes the 1/f noise parameter extraction. Firstly, from flicker noise data versus frequency, the slope factor AF can be extracted. The next step is to multiply all the noise data with the factor f^{AF} for all frequencies to factor out the frequency dependence. By averaging the obtained data in a certain range (typically from $10Hz$ to $100Hz$), one noise value can be extracted for each bias point. Figure 4.22 [35] shows the extraction of AF in comparison with the ideal flicker noise slope for long N and P $50V$ devices for $V_D = 3V$. Since normalized charges are calculated, 1/f noise equations from [27] above can be used . The output noise S_{ID} divided by I_D^2 , is used for extracting the noise parameters in different operating conditions [170, 184, 186]. In moderate inversion, this quantity is constant versus current and from there the N_T parameter can be extracted, since Coulomb scattering contribution is not significant. The two last terms in the bracket in Equation 4.2 which contain the $a\mu$ product can be neglected [22, 24, 177, 184, 186, 199]. Then in early strong inversion, where S_{ID}/I_D^2 starts to decrease at increasing drain current, the Coulomb scattering related parameter a_C is obtained from Equation 4.2. A sudden increase of S_{ID}/I_D^2 at highest currents is an indication that there is an effect of series resistance on noise [22, 186], and the related parameter S_{DR} can be extracted by Equation 4.7. This effect is usually present in short channel devices. Finally, if there is an increase of S_{ID}/I_D^2 in the very low current region, mobility fluctuation mechanism contributes to noise and a_H parameter is extracted [22, 24, 186]. This can be done through Equation 4.4. All the above describe the parameter extraction of 1/f noise coming mainly from the channel region. As previously established [27], the carrier number fluctuation effect in the extension of gate oxide over the drift region can be significant only in linear region of long channel devices. There, an increase of S_{ID}/I_D^2 is noticed in early strong inversion and from there N_{TDR} is calculated via Equation 4.5. i_{drift} normalized current in drift region is directly taken from the IV model.

Figures 4.23, 4.24, 4.25, 4.26, 4.27, 4.28 [35] show the S_{ID}/I_D^2 normalized with device area, referred to $1\,Hz$, versus normalized drain current for all devices. Specifically, long transistors are shown for drain bias of $3\,V$ and$50\,mV$, since at $50\,mV$ the effect of drift region is apparent while short transistors are shown only with drain bias of $3\,V$. In each of the 12 plots presented, the values of the extracted parameters are shown as well as the point where these parameters were extracted. In all cases of $V_D = 3\,V$ both for long and short transistors, N_T and a_C parameters are extracted. It is clear that in moderate inversion the $a\mu$ product is negligible. In long transistors at $V_D = 50\,mV$, N_{TDR} is extracted. The series resistance parameter S_{DR} seems to play a role only in the short n-channel $50\,V$ device. The mobility fluctuation effect parameter a_H appears only in short $50\,V$ and $20\,V$ p-channel devices. The different contributions are shown with dashed line in every plot in order to confirm that each effect is dominant in a different region, as described above. A simple carrier number fluctuation model $K_o(g_m/I_D)^2$ is also shown for comparison [177, 184, 186]. As it can be seen in the Figures 4.23, 4.24, 4.25, 4.26, 4.27, 4.28, this simple approach almost coincides with the complete model when $a\mu \approx 0$ in linear region. In saturation region, there are some slight differences especially at higher currents. Tables 4.4, 4.5 [35] show all the IV and noise parameters extracted for each transistor.



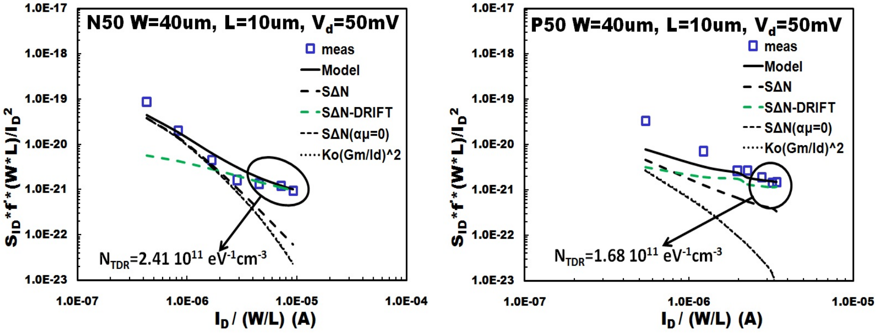
(a) (b)

Figure 4.23: 1/f noise PSD S_{ID}/I_D^2 normalized with $1/(WL)$, referred to $1\,Hz$, vs. normalized drain current $I_D/(W/L)$, for (a) N50 transistors and (b) P50 transistors. Long devices ($W = 40\,\mu m$, $L = 10\,\mu m$) are shown at $\mid V_D \mid = 3\,V$. Measurement (markers), full model (lines), with different noise contributions (dashed and dotted lines).



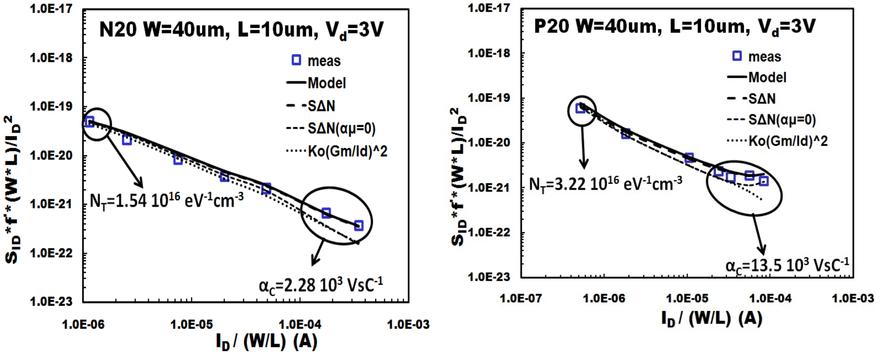
(a) (b)

Figure 4.24: 1/f noise PSD S_{ID}/I_D^2 normalized with $1/(WL)$, referred to $1\,Hz$, vs. normalized drain current $I_D/(W/L)$, for (a) N50 transistors and (b) P50 transistors. Short devices ($W = 40\,\mu m$, $L = 0.5\,\mu m$ for N50, $L = 1\,\mu m$ for P50) are shown at $\mid V_D \mid = 3\,V$. Measurement (markers), full model (lines), with different noise contributions (dashed and dotted lines).



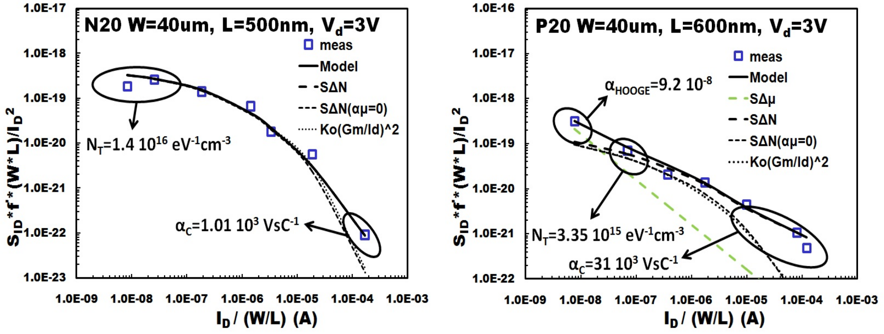
(a) (b)

Figure 4.25: 1/f noise PSD S_{ID}/I_D^2 normalized with $1/(WL)$, referred to $1\,Hz$, vs. normalized drain current $I_D/(W/L)$, for (a) N50 transistors and (b) P50 transistors. Long devices ($W = 40\,\mu m$, $L = 10\,\mu m$) are shown at $\mid V_D \mid = 50\,mV$. Measurement (markers), full model (lines), with different noise contributions (dashed and dotted lines).



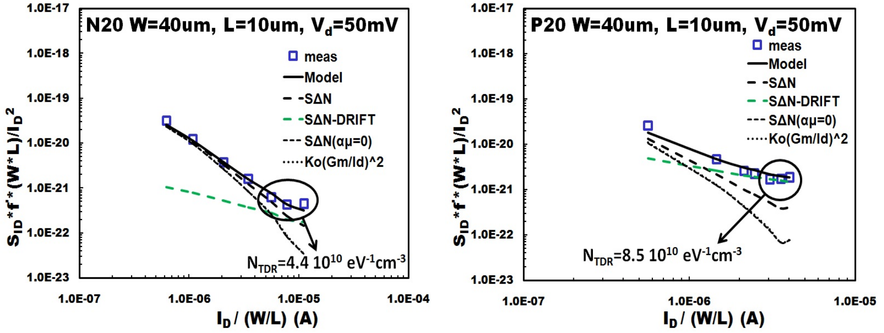
(a) (b)

Figure 4.26: 1/f noise PSD S_{ID}/I_D^2 normalized with $1/(WL)$, referred to $1\,Hz$, vs. normalized drain current $I_D/(W/L)$, for (a) N20 transistors and (b) P20 transistors. Long devices ($W = 40\,\mu m$, $L = 10\,\mu m$) are shown at $\mid V_D \mid = 3\,V$. Measurement (markers), full model (lines), with different noise contributions (dashed and dotted lines).



(a) (b)

Figure 4.27: 1/f noise PSD S_{ID}/I_D^2 normalized with $1/(WL)$, referred to $1\,Hz$, vs. normalized drain current $I_D/(W/L)$, for (a) N20 transistors and (b) P20 transistors. Short devices ($W = 40\,\mu m$, $L = 0.5\,\mu m$ for N20, $L = 0.6\,\mu m$ for P20) are shown at $\mid V_D \mid = 3\,V$. Measurement (markers), full model (lines), with different noise contributions (dashed and dotted lines).



(a) (b)

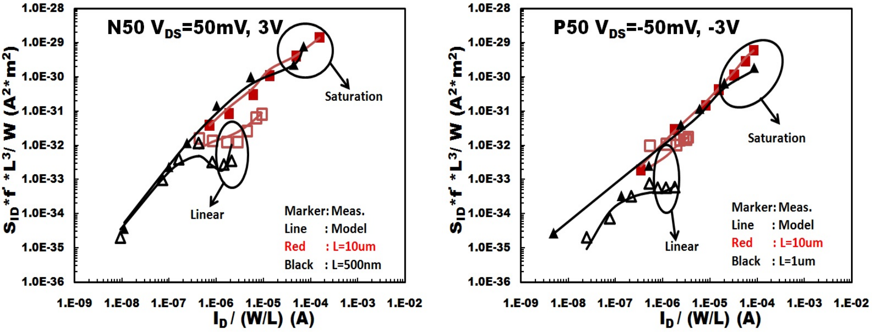
Figure 4.28: 1/f noise PSD S_{ID}/I_D^2 normalized with $1/(WL)$, referred to $1\,Hz$, vs. normalized drain current $I_D/(W/L)$, for (a) N20 transistors and (b) P20 transistors. Long devices ($W = 40\,\mu m$, $L = 10\,\mu m$) are shown at $\mid V_D \mid = 50\,mV$. Measurement (markers), full model (lines), with different noise contributions (dashed and dotted lines).

Parameter	Units	N50 40x10	N50 40x05	P50 40x10	P50 40x1
n	-	1.32	1.35	1.22	1.17
I_{SPEC}	A	$8.95.10^{-7}$	$2.58.10^{-5}$	$1.67.10^{-7}$	$1.61.10^{-6}$
μ	$m^2\,(Vs)^{-1}$	0.0579	0.132	0.0118	0.0159
AF	-	0.95	0.95	1.15	1.15
N_T	$eV^{-1}cm^{-3}$	$1.7.10^{16}$	$1.75.10^{16}$	$8.05.10^{15}$	$2.69.10^{15}$
a_C	VsC^{-1}	1.10^3	$2.58.10^3$	$36.5.10^3$	$31.5.10^3$
a_H	-	-	-	-	$6.8.10^{-7}$
N_{TDR}	$eV^{-1}cm^{-3}$	$2.4.10^{11}$	-	$9.6.10^{10}$	-
S_{DR}	Ω^2Hz^{-1}	-	$1.75.10^{-9}$	-	-
K_O	$C^2eV^{-1}cm^{-2}$	$2.87.10^{-27}$	$2.96.10^{-27}$	$1.36.10^{-27}$	$4.54.10^{-28}$

Table 4.4: 1/f Noise HV model extracted parameters for $50\,V$ devices under test

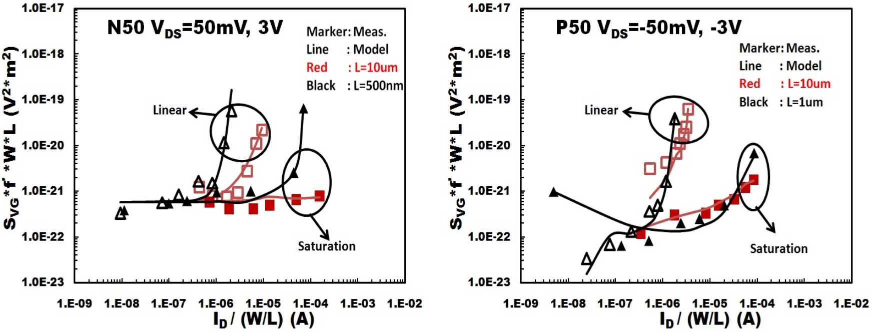
Parameter	Units	N20 40x10	N20 40x05	P20 40x10	P20 40x06
n	-	1.3	1.33	1.27	1.145
I_{SPEC}	A	$8.24.10^{-7}$	$2.19.10^{-5}$	$1.7.10^{-7}$	$4.68.10^{-6}$
μ	$m^2\,(Vs)^{-1}$	0.054	0.113	0.0116	0.036
AF	-	1	0.95	1.18	1.18
N_T	$eV^{-1}cm^{-3}$	$1.54.10^{16}$	$1.4.10^{16}$	$3.22.10^{16}$	$3.35.10^{15}$
a_C	VsC^{-1}	$2.28.10^3$	$1.01.10^3$	$13.5.10^3$	31.10^3
a_H	-	-	-	-	$6.8.10^{-8}$
N_{TDR}	$eV^{-1}cm^{-3}$	$4.4.10^{10}$	-	$8.5.10^{10}$	-
S_{DR}	Ω^2Hz^{-1}	-	-	-	-
K_O	$C^2eV^{-1}cm^{-2}$	$2.6.10^{-27}$	$2.37.10^{-27}$	$5.44.10^{-27}$	$5.66.10^{-28}$

Table 4.5: 1/f Noise HV model extracted parameters for $20\,V$ devices under test



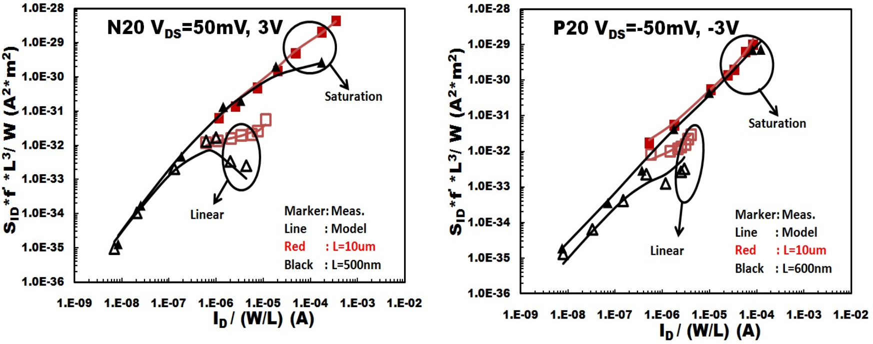
(a) (b)

Figure 4.29: 1/f noise PSD S_{ID}, multiplied by L^3/W referred to $1\,Hz$, vs. normalized drain current $I_D/(W/L)$, for (a) N50 transistors and (b) P50 transistors is shown for both linear and saturation regions. Long channel (squares) and short channel (triangles) are shown in the same plot. Measurement (markers) and model (lines).



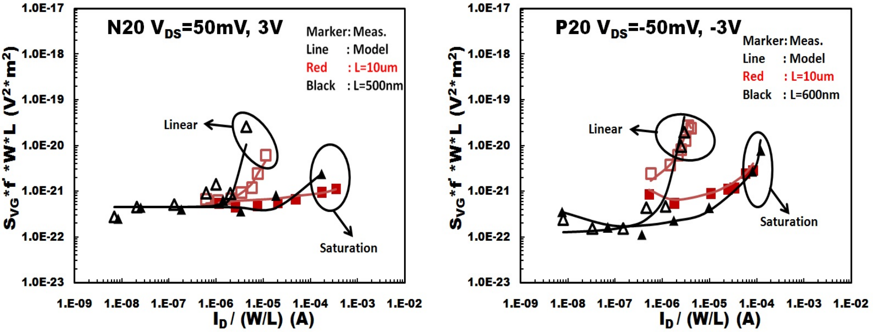
(a) (b)

Figure 4.30: 1/f noise PSD S_{VG}, multiplied by WL referred to $1\,Hz$, vs. normalized drain current $I_D/(W/L)$, for (a) N50 transistors and (b) P50 transistors is shown for both linear and saturation regions. Long channel (squares) and short channel (triangles) are shown in the same plot. Measurement (markers) and model (lines).



(a) (b)

Figure 4.31: 1/f noise PSD S_{ID}, multiplied by L^3/W referred to $1\,Hz$, vs. normalized drain current $I_D/(W/L)$, for (a) N20 transistors and (b) P20 transistors is shown for both linear and saturation regions. Long channel (squares) and short channel (triangles) are shown in the same plot. Measurement (markers) and model (lines).



(a) (b)

Figure 4.32: 1/f noise PSD S_{VG}, multiplied by WL referred to $1\,Hz$, vs. normalized drain current $I_D/(W/L)$, for (a) N20 transistors and (b) P20 transistors is shown for both linear and saturation regions. Long channel (squares) and short channel (triangles) are shown in the same plot. Measurement (markers) and model (lines).

In contrast to [27], [34], [199], noise spectral dependence different than 1/f has been accounted for, in the present analysis. Noise exponents are found to be about 0.95 and 1.15 for n- and p-channel devices, respectively. Long and short channel devices show a similar spectral dependence, except in the N20 devices, where AF values slightly differ. The 1/f noise parameters extracted above (Tables 4.4, 4.5), are used in the simulations. In Figures 4.29, 4.30, 4.31, 4.32 [35], the results are shown for all the transistors. Lines represent the model while markers represent the measurements. Noise data for long and short channel devices are normalized and shown in the same graph, so as to compare the noise for different channel lengths. Long channel measurements and simulations are shown with red color while short channel are shown with black. In each case, linear ($|V_D| = 50\,mV$) and saturation ($|V_D| = 3\,V$) regions are presented in the same plot. Normalized output noise S_{ID} and input noise S_{VG} are shown. S_{VG} is multiplied by the area WL to factor out the device dimension effect, while S_{ID} is multiplied by L^3W so as to eliminate device dimension and transconductance effects. Current is also normalized by dividing by the aspect ratio W/L. $W$and L denote effective device dimensions as obtained from the DC model.

The results seem to be very good, since in all cases the model and measurements show a very consistent behavior. The wide range of noise data allowed for an extraction of the noise parameters for every different noise contribution, and these full parameter sets are responsible for the very nice evaluation of the model. It is also apparent that the behavior of the normalized noise for both long and short channel devices is quite similar after factoring out the size and transconductance effects. In some cases (N20, P50 short channel devices), the output noise seems to decrease in saturation at high currents. This happens probably because of the self-heating effect present in these devices. It is also important to mention that the values of the parameters shown in Tables 4.4, 4.5, are generally quite close between long and short channel lengths, implying that the scaling behavior of the 1/f noise model is also very consistent with geometry. The parameters regarding the noise from drift region (N_{TDR}, which will have an impact only in longer channel devices) and from series resistance (S_{DR}, which will have an impact only in shorter channel devices) could be applied to all channel lengths. Note that in [27] a single parameter set was used covering long and short devices, contrary to the present work. Generally, possible differences with the values from other Tables (Tables 4.1, 4.2, 4.3) from this chapter can be found which are due to several reasons mentioned before.

4.4 Conclusions

The first objective of this chapter was to successfully explore the LDMOS transistor and locate any possible sources that generate 1/f noise. In the LV channel part, flicker noise is caused by the same effects as in standard MOSFETs such as carrier number fluctuation due to trapping/detrapping mechanism in the oxide interface, mobility fluctuation effect and series resistance effect. In the drift region part, 1/f noise is observed due to the same trapping/detrapping effect as above which is now generated in the extension of gate oxide which overlaps with drift region. This carrier number fluctuation effect creates flicker noise which becomes significant and comparable to the channel noise under linear region and strong inversion modes and for longer channel devices. In saturation region, quasi-saturation and self-heating effect seem to affect 1/f noise. All the above have been experimentally observed in our work [27, 34, 35] as in works from other groups [193, 194, 195, 198].

The second goal of the present chapter was to develop a complete compact charge-based 1/f noise model for LDMOSFETs which will include all the above effects. A few modeling approaches were available in literature until now [198] without providing a compact solution. As a first step to solve the problem related to the execution of 1/f noise measurements at high drain voltages, a dedicated set-up provided by AdMOS allowing to measure 1/f noise in HV devices up to $200\,V$ has been presented. 1/f noise was measured on different n- and p-channel devices over a wide range of bias conditions for long and short channel devices up to $50\,V$. The 1/f noise compact model was implemented and its results have been presented consistently over all bias ranges [27]. Since the basic contribution of drift region to 1/f noise takes place under low drain voltage conditions, a comprehensive analysis of 1/f noise behavior versus drain voltage for HV devices was accomplished based on our new model [34] which can lead to a more accurate understanding of 1/f noise in HV-MOSFETs. Drift region effect on 1/f noise in long channel devices in strong inversion and linear region can be observed very clearly in this analysis of 1/f noise versus drain bias. Output noise S_{ID} shows an $\sim I_D\, vs. V_D$ shape while S_{VG} seems to remain constant versus drain voltage in linear region and strong inversion when flicker noise is contributed only by the channel in long channel devices. The effect of drift region causes an increase in noise for low V_D and high V_G, L and this is fully covered by the model. Furthermore, quasi-saturation effect and how it influences flicker noise especially in N50 short channel device is also unambiguous in this analysis [34]. Finally, self-heating effect on 1/f noise is noticed under high-voltage and current conditions but not yet included in the model. In conclusion, the present model [27, 34] can cover a wide range of bias and geometrical conditions of low frequency noise in HV-MOSFETs.

The implementation of an accurate 1/f noise parameter extraction method for LDMOSFETs follows naturally after the establishment and validation of our new model. This procedure took place into two different approaches; a simpler one presented first at [199] and a second more complete that followed [35]. As far as the first one is concerned [199], a methodology, strongly related to the g_m/I_D ratio, was applied and despite the somewhat limited available data range, the basic 1/f noise parameters related to carrier number fluctuation and correlated mobility fluctuation effects could be easily determined. The recently established 1/f noise model for HV-MOSFETs [27, 34] showed good results versus experiment. This work was the basis for the more complete extraction method that follows [35]. The latter is a comprehensive methodology for extracting 1/f noise parameters in HV-MOSFETs. Because of the wide data range in terms of bias and geometry, all noise parameters related to noise contributions both from channel and drift region are extracted in distinct operating regions, where each of the effects considered is dominant. The procedure has been applied to $50\,V$ and $20\,V$ long and short channel n- and p-type HV-MOSFETs, from 1/f measurements covering weak to strong inversion in linear and saturation regimes. The comparisons of noise data from devices with different geometries and for different bias conditions provide insight into the overall noise behavior of HV-MOSFETs. The individual contributions to 1/f noise from carrier number fluctuation, mobility fluctuation, series resistance fluctuation and drain extension, are shown and analyzed in detail. The application of the parameter extraction methodology with the recently established 1/f noise model for HV devices [27] gives excellent results for a wide variety of different bias conditions. The resulting parameter values for long and short channel devices are consistent, resulting in a well scalable model.

Chapter 5

Low-Frequency Noise Variability Modeling in MOSFETs

5.1 Introduction

Physical models, as addressed in previous chapters, describe the mean value behavior of LFN. The description of statistical variation of LFN may be considered to be equally significant as the description of mean value of LFN in MOSFETs. As mentioned before, LFN is successfully used as a reliable characterization tool to evaluate the quality of the MOSFET through its dielectric interface. It also is an important factor limiting the performance of analog and RF applications. Therefore the creation of correct LFN variability models is really crucial. The scope of our work was to discover the relation between the effects that generate LFN noise in MOSFETs and its variability and then to succeed in implementing a physics-based, charge-based compact model which describes this variability. Noise performance may strongly vary between different devices on one chip, and moreover even between different operating points of a single device. Scaling down of CMOS technologies leads to both shrinking of device area and operation in subthreshold region. In smaller-sized MOSFETs, noise fluctuations are area dominated but in moderate- to large- sized transistors ($Area \ggg 1\mu m^2$), variability of LFN also shows a strong bias-dependency.

As described in detail in Section 3.4.3, in small devices LFN is dominated by random telegraph signals (RTS) which are caused by the capture and subsequent emission of charges at discrete trap levels near the oxide interface [139, 144, 162, 205, 206, 207, 208]. Each carrier trapped close to the silicon oxide interface causes RTS in time domain, corresponding to a Lorentzian spectrum. This trapping/detrapping approach assumes a distribution of trapping times that arise from the transition of electrons from the semiconductor surface to traps located in the oxide. The Lorentzian-like spectra are responsible for strong LFN deviation in small area devices where number of traps is quite low [162].

The power spectral density (PSD) of LFN in moderate- to large-sized transistors commonly used in analog/RF applications results from the superposition of such Lorentzians while the increased number of traps ensures the inversely proportional to frequency behavior ($\sim 1/f$). In more detail, a distribution of time constants within this superposition can give rise to a spectrum that varies inversely with frequency when the number of traps is quite high which is the case in large devices [139]. Carrier number (ΔN) [159] and mobility fluctuations ($\Delta\mu$) [188, 189, 190] are considered as the main causes of low frequency noise. While their incidence on the bias-dependence of LFN has been well investigated, the way these noise mechanisms contribute to the bias-dependence of variability of LFN has been less well understood. 1/f noise variability is minimum in high current region whereas it has been shown to be maximized in weak inversion [209, 210, 211], while increased drain bias also increases noise variability due to the non-uniformity of channel in saturation [207, 208]. Our measured data confirm this bias-dependence of 1/f noise variability [28, 29]. It is also proved that there is little effect on noise deviation due to current or transconductance dispersion. Until today, no compact model has been proposed to explain this bias-dependence in detail. In combination with the charge-based formulation of LFN [21, 22, 24, 33], we propose a new charge-based compact model for bias-dependence of LFN variability for the first time [28, 30]. In [28], the complete model including both ΔN and $\Delta\mu$ effects is presented while in [30], the model regards only ΔN effect and is validated with data taken from bibliography [211] both for bias and area dependence. Furthermore in [30], fundamental properties of log-normal distribution are taken into consideration since LFN deviation seems to follow such a distribution as it is shown in Figure 5.1 [30].

In the introduction above, the main aspects of 1/f noise variability that are covered in this chapter, are briefed. After this, a short reference in previous attempts of modeling 1/f noise variability is listed with giving attention to the benefits of our work. Finally, our physics-based analysis resulting in a complete compact model for 1/f noise variability in MOSFETs is presented. Despite the fact that the statistical sample of data is not sufficient in HV-MOSFETs, as presented in Chapter 4, the model can also be applied to the LV part of HV devices since the effects that generate 1/f noise there (ΔN and $\Delta\mu$) are the same as in LV-MOSFETs.

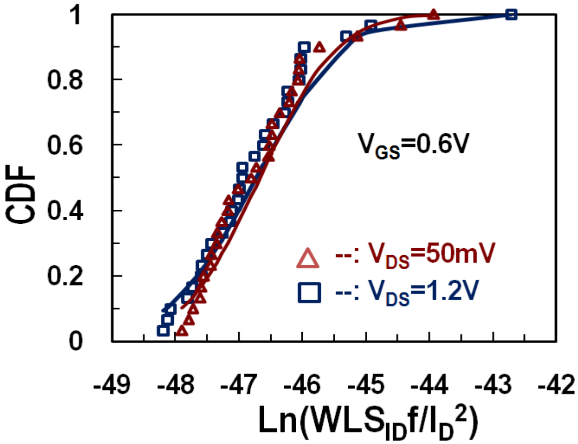


Figure 5.1: Cumulative Distribution Function (CDF) of normalized power spectral density of the logarithm of drain current noise S_{ID} for 30 moderately-sized nMOSFETs, shows a log-normal distribution.

5.2 Existing Approaches

Previous studies of statistical LFN variability have focused mainly on area-dependence [211, 212, 213, 214, 215, 216], while attempts have been made to describe the bias-dependence of noise variability [207, 208, 209]. A simple empirical model relating 1/f variability to transconductance-to-current ratio g_m/I_D [29] which provides satisfactory results for saturation from weak to strong inversion was proposed from our group and is presented in Appendix A. However, no physics-based and truly compact model for the bias-dependence of LFN variability in MOSFETs had been proposed so far until the present work [28, 30].

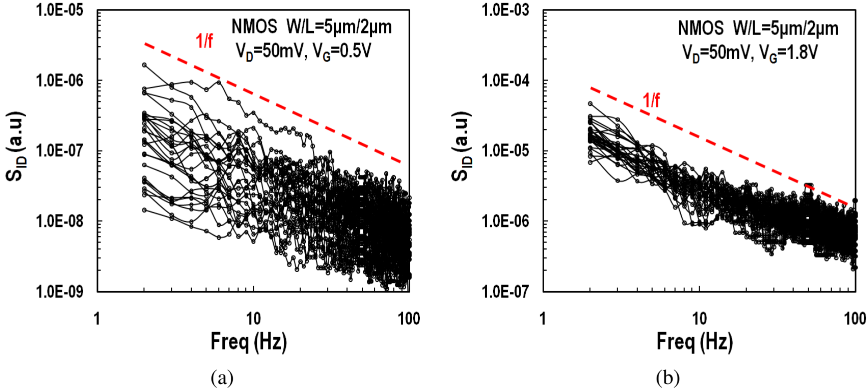
For additional information, LFN variability studies [212, 213, 215, 216] generally propose an area scaling of the noise variability, $\sigma[log(S_{ID})]$, based on a $1/\sqrt{area}$-dependence. In [217], the reasons why $\sigma[log(S_{ID})]$ deviates from the $1/\sqrt{area}$-dependence are presented based on the statistics of sums of lognormal distributions, but eventually it relies on a rather arbitrary empirical function to fit the variability area scaling. On the contrary, in [211], the fact that LFN variability should not follow a $1/\sqrt{area}$-dependence is proved due to the fact that LFN follows a log-normal distribution. Apart from the bias- and area-dependence of LFN variability, it is shown that it can also be affected by frequency [208, 218] and temperature [218].

5.3 A Charge-Based Compact Model for 1/f Noise Variability in MOSFETs

5.3.1 General Considerations

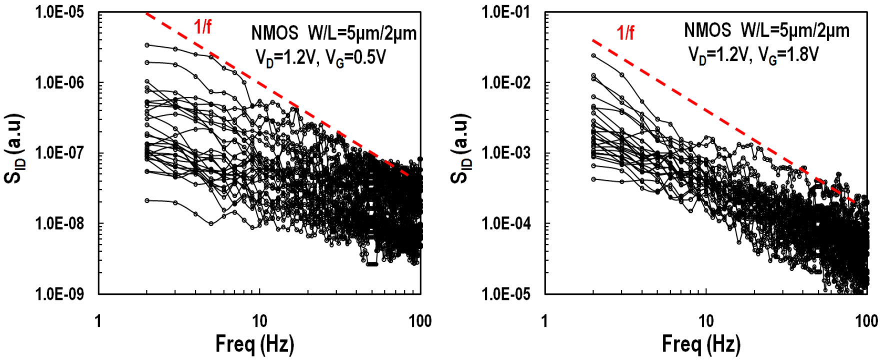
As stated before, the main goal of the present work was to propose a complete physics-based compact model of 1/f noise variability in all operating regions of the MOSFET. A charge-based model of flicker noise including ΔN and $\Delta\mu$ fluctuations has been described formerly [21, 22, 24, 33]. In this work, we apply the fundamental mathematical principles of statistics to the above charge-based model of ΔN and $\Delta\mu$ fluctuations. The resulting compact model provides new insight into bias-dependence of 1/f noise variability of MOSFETs. The model is shown to agree with measurements in n- and p-channel MOSFETs in all bias conditions, and results are in general agreement with known literature. The model for noise variability can easily be implemented in the charge-based EKV3 1/f noise compact MOSFET model [22, 24, 33].

5.3.2 Devices and Measurements



(a) (b)

Figure 5.2: Relative power spectral density of drain current noise S_{ID} for n-channel MOSFETs with $W/L = 5\,\mu m/2\,\mu m$ at $V_{DS} = 50\,mV$ for (a) $V_{GS} = 0.5\,V$ around threshold and (b) $V_{GS} = 1.8\,V$ at strong inversion.

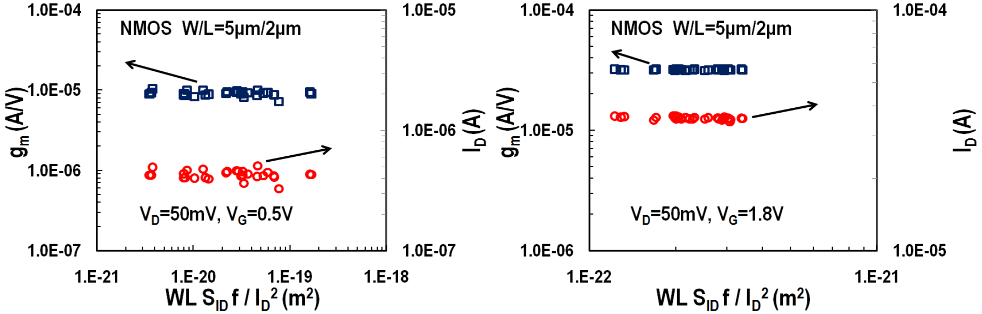


(a) (b)

Figure 5.3: Relative power spectral density of drain current noise S_{ID} for n-channel MOSFETs with $W/L = 5\,\mu m/2\,\mu m$ at $V_{DS} = 1.2\,V$ for (a) $V_{GS} = 0.5\,V$ around threshold and (b) $V_{GS} = 1.8\,V$ at strong inversion.

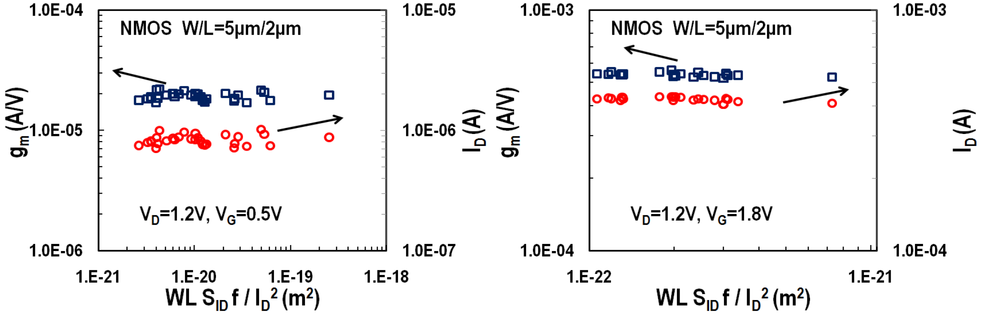
On-wafer 1/f noise measurements were perofrmed on n- and p-channel devices in an experimental $180\,nm$ CMOS process flow. The same process was used for the evaluation of the charge-based EKV3 1/f noise MOSFET compact model [22, 24, 33] in Section 3.4.8 and the measurements were also performed at our lab with the same set-up as in Section 3.4.7. Flicker noise spectra of 30 dies of NMOS and PMOS $W/L = 5\,\mu m/2\,\mu m$ transistors were measured over one wafer. Both saturation and linear regimes with $|V_{DS}| = 1.2\,V$ and $50\,mV$, respectively are covered from weak to strong inversion with $|V_{GS}| = 0.35, 0.4, 0.45, 0.5, 0.55, 0.6, 0.8, 1.2, 1.8\,V$. Additionally, drain bias-dependence is analyzed, with $|V_{DS}| = 0.05, 0.15, 0.3, 0.6, 1.2V$ at two gate voltage values, $|V_{GS}| = 0.6, 1.2\,V$, to closely examine the bias-dependence of 1/f noise variability versus bias conditions. The measured frequency range was from $2\,Hz$ up to $2\,kHz$. Figures 5.2, 5.3 [28] show the measured spectra of $W/L = 5\,\mu m/2\,\mu m$ transistors in different cases with a slope close to 1/f. Variability of 1/f noise is clearly seen to be maximized at low gate bias, and at high drain bias. Similar behavior can be observed in PMOS devices. In order to investigate the effect of deviation of drain current and transconductance on flicker noise, Figures 5.4, 5.5 are produced for the same device and the same operating conditions as in Figures 5.2, 5.3. In every case, little effect is observed and this enhances the theory that noise variability is mainly due to trap statistics [209].

As mentioned above, both area and bias dependence of our model is validated in [30]. In fact, data from an $140\,nm$ CMOS process, for an N-channel MOSFET with geometry $W/L = 8\,\mu m/160\,nm$ were taken from [211]. Operating conditions cover weak to strong inversion, with $V_{GS} = 0.4, 0.5, 0.6, 0.8, 1, 1.4, 1.8\,V$ at three drain voltages ($V_{DS} = 0.1, 0.5, 1.8\,V$), from linear to saturation. Additionally, standard deviation values of natural logarithm of normalized output noise are available for different area values at three bias conditions, a)$V_{DS} = 0.1, V$, $V_{GS} = 0.8, V$, b)$V_{DS} = 0.1, V$, $V_{GS} = 1.4, V$, c)$V_{DS} = 1.8, V$, $V_{GS} = 1.4, V$ in order to study the geometrical scaling of deviation of LFN.



(a) (b)

Figure 5.4: Variations of transconductance g_m (left) and drain current I_D (right) with normalized noise $WL * S_{ID}/I_D^2$, referred to $1\,Hz$, for n-channel MOSFETs with $W/L = 5\,\mu m/2\,\mu m$ at $V_{DS} = 50\,mV$ for (a) $V_{GS} = 0.5\,V$ around threshold and (b) $V_{GS} = 1.8\,V$ at strong inversion.



(a) (b)

Figure 5.5: Variations of transconductance g_m (left) and drain current I_D (right) with normalized noise $WL * S_{ID}/I_D^2$, referred to $1\,Hz$, for n-channel MOSFETs with $W/L = 5\,\mu m/2\,\mu m$ at $V_{DS} = 1.2\,V$ for (a) $V_{GS} = 0.5\,V$ around threshold and (b) $V_{GS} = 1.8\,V$ at strong inversion.

5.3.3 Model Implementation for LV-MOSFETs

5.3.3.1 Physical 1/f Noise Ln-Mean Value Model Extraction

As presented in detail in Sections 3.4.3, 3.4.4, the basic contributors to LFN are ΔN and $\Delta\mu$ effects and a charge-based model for the mean value of LFN covering these effects has been proposed [22, 24, 33]. ΔN and $\Delta\mu$ contributors are being expressed with Equations 3.37, 3.41 while the total model through Equation 3.47 with series resistance effect being neglected in the present analysis. Before proceeding to the 1/f noise variability analysis, the mean value model should be extracted first for both $180\,nm$ and $140\,nm$ CMOS processes available in this work.

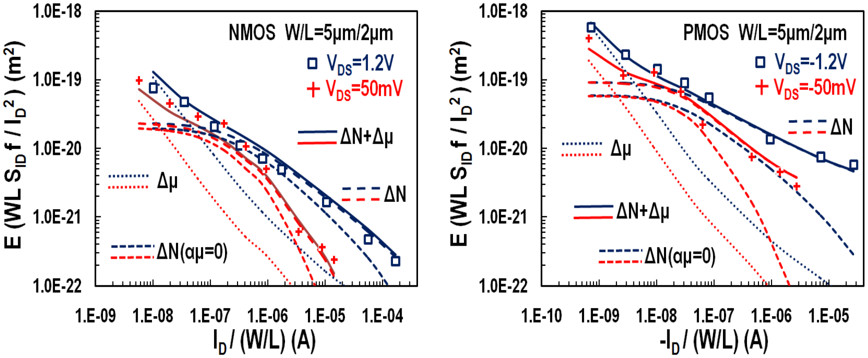
Parameter	Units	N5X2	P5X2	N8X016
N_T	$eV^{-1}cm^{-3}$	3.10^{16}	1.10^{17}	$6.5.10^{17}$
a_C	VsC^{-1}	7.10^{3}	$1.3.10^{5}$	2.10^{3}
a_H	–	1.10^{-6}	2.10^{-6}	–

Table 5.1: 1/f Noise model parameters for mean value of 180, $140nm$ CMOS nodes

180 nm CMOS Process

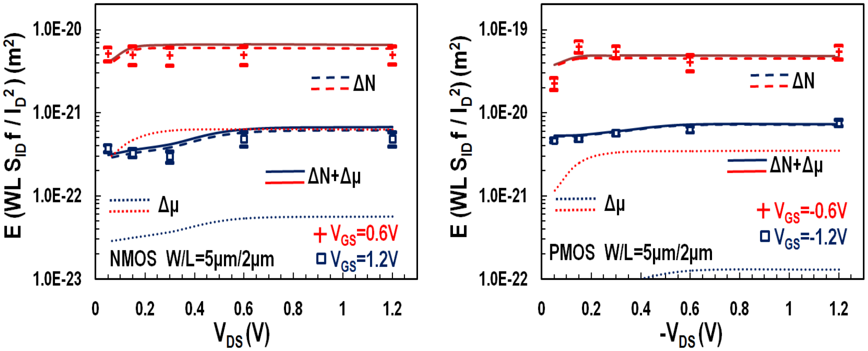
The model shows a good qualitative fit to the ln-mean data shown in Figures 5.6, 5.7, with extracted parameters as in Table 5.1 [28]. The extracted parameters listed in Table 5.1, are quite different than the ones in Table 3.1 despite the fact that they both refer to the same experimental $180\,nm$ CMOS process flow. The main reason for this is that now the ln-mean of 30 measured samples is calculated while in the previous case a simple average of 3 samples was calculated. Furthermore, now the parameters in Table 5.1, are extracted for one single transistor ($W/L = 5\,\mu m/2\,\mu m$) while in Table 3.1, two transistors were taken into account ($W/L = 5\,\mu m/2\,\mu m$, $W/L = 10\,\mu m/180\,nm$). In Figure 5.6, the mean (expected) value $E\left(WL * S_{ID}/I_D^2\right)$, referred to $1\,Hz$, versus $I_D/(W/L)$ is shown in linear and saturation regions while in Figure 5.7, the same quantity is shown versus $|V_D|$ at two $|V_{GS}|$ values ($|V_{GS}| = 1.2\,V, 0.6\,V$). Both NMOS and PMOS devices are shown in each case.

As it can be seen from Figure 5.6, the ΔN effect determines noise level from moderate to strong inversion at high current, while correlated $\Delta N - \Delta\mu$ noise is also apparent. $\Delta\mu$ effect is dominant in subthreshold region and appears as an increase over the weak inversion plateau of $WL * S_{ID}/I_D^2$. As it will be shown in the statistical noise analysis that follows, these fundamental effects influence the 1/f noise statistics in an analogous way. In Figure 5.7, the modeled and the measured behavior concur qualitatively well, given that the model handles linear to saturation behavior without any parameter fitting. Average noise also shows error bars corresponding to normalized standard error.



(a) (b)

Figure 5.6: Mean value of output noise $WL * S_{ID}/I_D^2$, referred to $1\,Hz$, in linear and saturation region ($|V_{DS}| = 50\,mV$, $1.2\,V$) vs. drain current $I_D/(W/L)$, for a) n- and b) p-channel MOSFETs with $W/L = 5\,\mu m/2\,\mu m$. Markers: measured (ln-mean) data, lines: complete LFN model (Equation 3.47), dashed: individual contributions of number (Equation 3.37) and mobility (Equation 3.41) fluctuations.



(a) (b)

Figure 5.7: Mean value of output noise $WL * S_{ID}$, referred to $1\,Hz$, at $|V_{GS}| = 1.2\,V, 0.6\,V$, respectively, vs. drain voltage $|V_D|$, for a) n- and b) p-channel MOSFETs with $W/L = 5\,\mu m/2\,\mu m$. Markers: measured (ln-mean) data (with error bars indicating standard error of the mean), lines: complete LFN model (Equation 3.47), dashed: individual contributions of number (Equation 3.37) and mobility (Equation 3.41) fluctuations.

140 nm CMOS Process

In Figure 5.8 [30], the mean (expected) value $E\left(WL * S_{ID}/I_D^2\right)$, referred to $1\,Hz$, versus $I_D/(W/L)$ is shown at $V_{DS} = 100\,m$, 0.5 and $1.8\,V$ respectively. The model shows a good qualitative fit with extracted parameters as in last column of Table 5.1 [30]. Expected value reaches a plateau in weak inversion which is the same for all drain voltage levels. This is due to ΔN effect while $\Delta\mu$ effect, which would cause an increase of noise in subthreshold region, is negligible for the specific data. As the inversion layer gets higher, mean value noise decreases while increased drain voltage leads to increased noise.

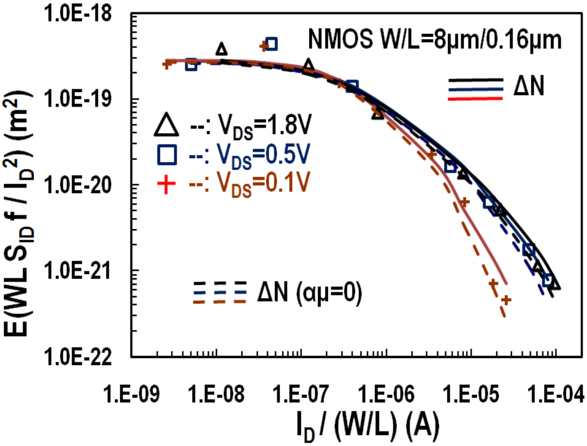


Figure 5.8: Mean value of output noise $WL * S_{ID}/I_D^2$, referred to $1\,Hz$, vs. drain current $I_D/(W/L)$ for an N-channel MOSFETs with $W/L = 8\,\mu m/160\,nm$ at $V_{DS} = 100\,m$, 0.5 and $1.8\,V$ respectively. Markers: measured data, lines: model with $\alpha\mu \cong 0.06$ depending on bias, dashed lines: model with $\alpha\mu = 0$.

5.3.3.2 Statistical 1/f Noise Model

The noise of a MOS transistor itself is in fact the standard deviation of drain current. In order to model correctly the variations of 1/f noise, the parameters that are sensitive to these variations must be identified. From the physical LFN noise model [22, 24, 33], it can be concluded that ΔN and $\Delta\mu$ effects contribute to flicker noise variability through variations of trap density N_T and of parameter a_H in Equations 3.37, 3.41 respectively. The procedure that will be followed for variance calculation, is to calculate the variance of total noise PSD for each of ΔN and $\Delta\mu$ effects. This must take place before integration along the channel as in Equation 3.30 since otherwise, each ΔI_D caused by any fluctuation (e.g. a specific trap) would have the same effect which is not valid [211]. Local noise sources in our modeling approach [22] described in Section 3.4.1 are considered uncorrelated. The variance that will be included into the integral as shown below, represents the local deviation corresponding to an elementary slice $\Delta\chi$ of the channel. Finally, by integrating from source to drain, the total variance is obtained by summing all the local contributions. According to basic statistics, we have:

$$Var(f(y)) = [\frac{\partial f}{\partial y}]^2 \sigma_y^2 \tag{5.1}$$

where σ_y is the standard deviation of y. The deviated parameters that are the number of traps N_{tr} which will be defined in the next section for ΔN and a_H for $\Delta\mu$ effect respectively.

Variance of 1/f Noise due to Carrier Number Fluctuation Effect

In this section, the variance of 1/f noise due to ΔN effect is calculated. As mentioned before, the parameter that is deviated is the number of traps:

$$N_{tr} = WLN_t \tag{5.2}$$

[205, 206] which follows a Poisson distribution [208, 209] and hence $\sigma_{N_{tr}}^2 = WLN_t$. Volumetric oxide trap density N_T is connected with the trap density N_t through Equation 3.27. The normalized PSD $WLf * S_{\delta I}/I_D^2$ of a local noise source due to ΔN effect is calculated through Equations 3.25, 3.26, 3.27 and 5.2 as [28]:

$$WLf * \frac{S_{\delta I_n^2}}{I_D^2} |_{\Delta N} = \left(\frac{1}{q_i + 1/2} + \alpha\mu\right)^2 \frac{N_{tr}}{W\Delta\chi N_{SPEC}^2} \tag{5.3}$$

where N_{SPEC} is the specific carrier density in cm^{-2} defined in Section 3.4.3. According to Equation 3.10, the PSD of the total normalized noise current fluctuation $WLf * S_{ID}/I_D^2$ due to ΔN effect can be calculated similarly to Equation 3.30 by integrating Equation 5.3 along the channel. By changing integral variable as $\xi = \chi/L$ and by using Equations 5.2, 5.3 we end up [28]:

$$\begin{gathered} WLf * \frac{S_{I_D^2}}{I_D^2} |_{\Delta N} = \frac{1}{L^2} \int_0^L \Delta x WLf * \frac{S_{\delta I_n^2}}{I_D^2} |_{\Delta N} \, dx = \\ \frac{1}{L^2} \int_0^L \left(\frac{1}{q_i + 1/2} + \alpha\mu\right)^2 \frac{N_{tr}}{WN_{SPEC}^2} dx = \\ \frac{1}{LWN_{SPEC}^2} \int_0^1 \left(\frac{1}{q_i + 1/2} + \alpha\mu\right)^2 N_{tr} d\xi \end{gathered} \tag{5.4}$$

To calculate the variance of Equation 5.4 we have [28]:

$$\begin{aligned}
&Var\left(WLf*\frac{S_{I_D^2}}{I_D^2}\mid_{\Delta N}\right)=\\
&\left(\frac{1}{LWN_{SPEC}^2}\right)^2 Var\int_0^1\left(\frac{1}{q_i+1/2}+\alpha\mu\right)^2 N_{tr}d\xi=\\
&\left(\frac{1}{LWN_{SPEC}^2}\right)^2\int_0^1 Var\left[\left(\frac{1}{q_i+1/2}+\alpha\mu\right)^2 N_{tr}\right]d\xi
\end{aligned}\tag{5.5}$$

where we have used $Var(\alpha x)=\alpha^2 Var(x)$. The variance in Equation 5.5 now appears within the integral since local noise sources are considered uncorrelated and thus $(Var(\Sigma x_i)=\Sigma(Var(x_i)))$ where x_i is the local noise source. To calculate variance due to number of traps, the partial derivative of the integrand of Equation 5.5 with respect to number of traps N_{tr} should be calculated [28]:

$$\begin{aligned}
&Var\left[\left(\frac{1}{q_i+1/2}+\alpha\mu\right)^2 N_{tr}\right]=\\
&\left[\frac{\vartheta\left(\left(\frac{1}{q_i+1/2}+\alpha\mu\right)^2 N_{tr}\right)}{\vartheta(N_{tr})}\right]^2\sigma_{N_{tr}}^2=\left(\frac{1}{q_i+1/2}+\alpha\mu\right)^4 WLN_t
\end{aligned}\tag{5.6}$$

By substituting Equation 5.6 into Equation 5.5 and by changing the integration variable $d\xi$ to dq_i according to $dq_i/d_\xi=-i_d/(2q_i+1)$ as in Equation 3.31, we can calculate the total variance due to ΔN effect as [28]:

$$\begin{aligned}
&Var\left(WLf*\frac{S_{I_D^2}}{I_D^2}\mid_{\Delta N}\right)=\\
&\left(\frac{1}{LWN_{SPEC}^2}\right)^2 WLN_t\frac{2}{i_d}\int_{q_d}^{q_s}\left(\frac{1}{q_i+1/2}+\alpha\mu\right)^4(q_i+1/2)\,dq_i=\\
&\frac{N_t}{N_{SPEC}^4 WL}\left(\begin{array}{c}\frac{1}{(q_s+0.5)^2(q_d+0.5)^2}+(\alpha\mu)^4+\frac{8(\alpha\mu)^3}{1+q_s+q_d}+\\ \frac{12(\alpha\mu)^2}{i_d}ln\left(\frac{1+2q_s}{1+2q_d}\right)+\frac{8(\alpha\mu)}{(q_s+0.5)(q_d+0.5)(1+q_s+q_d)}\end{array}\right)
\end{aligned}\tag{5.7}$$

where the charge-based expression in the last parenthesis can be renamed as $\Lambda_D\mid_{\Delta N}$.

Variance of 1/f Noise due to Mobility Fluctuation Effect

In the following, the variance due to $\Delta\mu$ effect because of fluctuation of α_{H} parameter is calculated. The normalized noise PSD $WLf*S_{\delta I}/I_D^2$ of a local noise source due to $\Delta\mu$ effect is calculated through Equation 3.39 as [28]:

$$WLf * \frac{S_{\delta I_n^2}}{I_D^2} |_{\Delta\mu} = \frac{1}{q_i} \frac{\alpha_H WL}{W\Delta\chi N_{SPEC}} \tag{5.8}$$

According to Equation 3.10 and by integrating Equation 5.8 along the channel after changing integral variable as $\xi = \chi/L$, the PSD of the total normalized noise current fluctuation $WLf * S_{ID}/I_D^2$ due to $\Delta\mu$ effect can be calculated as [28]:

$$\begin{gathered} WLf * \frac{S_{I_D^2}}{I_D^2} |_{\Delta\mu} = \frac{1}{L^2} \int_0^L \Delta x WLf * \frac{S_{\delta I_n^2}}{I_D^2} |_{\Delta\mu} dx = \\ \frac{1}{L^2} \int_0^L \frac{1}{q_i} \frac{\alpha_H WL}{WN_{SPEC}} dx = \\ \frac{1}{N_{SPEC}} \int_0^1 \frac{1}{q_i} \alpha_H d\xi \end{gathered} \tag{5.9}$$

To calculate the variance of Equation 5.9 we have [28]:

$$\begin{gathered} Var\left(WLf * \frac{S_{I_D^2}}{I_D^2} |_{\Delta\mu} \right) = \\ \left(\frac{1}{N_{SPEC}} \right)^2 \int_0^1 Var\left[\frac{1}{q_i} \alpha_H \right] d\xi \end{gathered} \tag{5.10}$$

The variance of the quantity $\left[\frac{1}{q_i}\alpha_H\right]$ can be calculated by using Equation 5.1 [28]:

$$\begin{gathered} Var\left[\frac{1}{q_i} \alpha_H \right] = \left[\frac{\vartheta\left(\frac{1}{q_i} \alpha_H \right)}{\vartheta\left(\alpha_H \right)} \right]^2 \sigma_{a_H}^2 = \\ \left(\frac{1}{q_i} \right)^2 \sigma_{a_H}^2 \end{gathered} \tag{5.11}$$

By substituting Equation 5.11 into Equation 5.10 and by changing the integral variable $d\xi$ to dq_i according $dq_i/d_\xi = -i_d/\left(2q_i+1\right)$, we can calculate the total variance due to $\Delta\mu$ effect as [28]:

$$\begin{gathered} Var\left(WLf * \frac{S_{I_D^2}}{I_D^2} |_{\Delta\mu} \right) = \\ \frac{\alpha_H}{WLN_{SPEC}^3} \frac{1}{i_d} \int_{q_d}^{q_s} \left(\frac{2}{q_i} + \frac{1}{q_i^2} \right) dq_i = \\ \frac{\alpha_H}{WLN_tN_{SPEC}^3} \frac{1}{i_d} \left(2ln\left(\frac{q_s}{q_d} \right) + \frac{q_s - q_d}{q_d q_d} \right) \end{gathered} \tag{5.12}$$

No information is a priori available on the standard deviation of α_{H} parameter. We can assume here that $\sigma^2_{\alpha_H} = \alpha_H/(WLN_{SPEC})$, so that ΔN and $\Delta\mu$ effects will have similar geometrical scaling.

Total Variance of 1/f Noise in MOSFETs

To calculate the total variance of 1/f noise, contributions to variance from ΔN and $\Delta\mu$ effects should be added since if X, Y are uncorrelated and $Z = X + Y$ then $Var(Z) = Var(X) + Var(Y)$. In the mean value model, total 1/f noise is calculated by adding the contributions of ΔN and $\Delta\mu$ effects (Equation 3.47). Thus, total variance of 1/f noise can be calculated by adding Equations 5.7, 5.12 as [28]:

$$Var\left(WLf*\frac{S_{I_D^2}}{I_D^2}\right) = Var\left(WLf*\frac{S_{I_D^2}}{I_D^2}|_{\Delta N}\right) + Var\left(WLf*\frac{S_{I_D^2}}{I_D^2}|_{\Delta\mu}\right) \tag{5.13}$$

Equations 5.7, 5.12 and 5.13 describe the new statistical charge-based 1/f noise compact model [28]. The new model provides an explicit and truly compact formulation of bias-dependent 1/f noise variability, formulated as a function of inversion charge densities at source and drain, q_s and q_d. The parameters of the physical model presented in Table 5.1 (N_T, α_C, α_H), can be used in the statistical model. However, to allow for some flexibility in the statistical model, the following parameters are defined:

$$\begin{aligned} E_{NT} &\approx N_{TS}/N_T \\ E_{\alpha C} &\approx \alpha_{CS}/\alpha_C \\ E_{\alpha H} &\approx \alpha_{HS}/\alpha_H \end{aligned} \tag{5.14}$$

where N_{TS}, α_{CS}, α_{HS} can be used in Equations 5.7 and 5.12.

Standard Deviation of $\sigma\left(ln\left(WL*S_{I_D^2}/I_D^2\right)\right)$ due to Carrier Number Fluctuation Effect

As mentioned before, 1/f noise data follow a lognormal distribution as it can be seen in Figure 5.1. Thus the basic properties of this distribution can be used [30, 211]:

$$\sigma\left(ln\left(\frac{S_{I_D^2}}{I_D^2}|_{\Delta N}*WLf\right)\right) = \sqrt{ln\left(1+\frac{Var\left(WLf*\frac{S_{I_D^2}}{I_D^2}|_{\Delta N}\right)}{E\left(WLf*\frac{S_{I_D^2}}{I_D^2}|_{\Delta N}\right)}\right)} \tag{5.15}$$

where for the purpose of this Thesis we focus on the standard deviation of the natural logarithm of normalized output noise due to ΔN effect. Variance is given by Equation

5.7 while expected value can be calculated by Equations 3.27, 3.37 as:

$$E\left(WLf * \frac{S_{I_D^2}}{I_D^2}\,|_{\Delta N}\right) = \frac{4N_t}{N_{SPEC}^2} K_D\,|_{\Delta N} \tag{5.16}$$

and thus Equation 5.15 becomes:

$$\sigma\left(ln\left(\frac{S_{I_D^2}}{I_D^2}\,|_{\Delta N} * WLf\right)\right) = \sqrt{ln\left(1+\frac{E_{NT}}{16WLN_t}\frac{\Lambda_D\,|_{\Delta N}}{K_D\,|_{\Delta N}}\right)} \tag{5.17}$$

if we take into consideration Equation 5.14. The ratio of variance divided by the squared expected value in Equations 5.15, 5.17 is called normalized variance and is of great importance as it will be proved later on.

5.3.3.3 Results

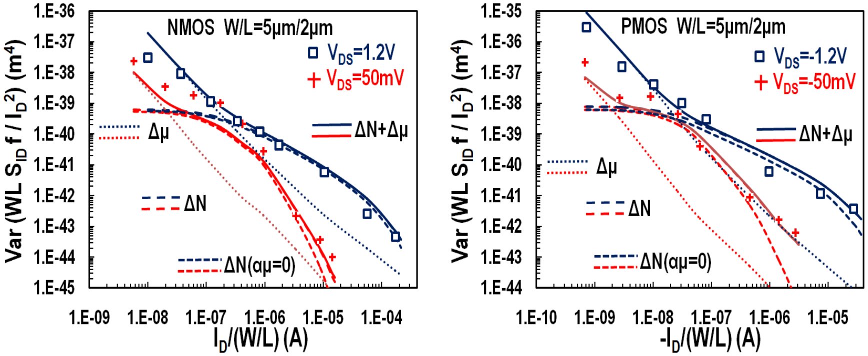
The proposed model for 1/f noise variability will be validated both with data measured at our lab from an 180 nm CMOS process and with data taken from bibliography from an 140 nm CMOS process [211]. In the case of 180 nm, both ΔN and $\Delta\mu$ effects seem to be significant as it is shown in Figures 5.6, 5.7 while in 140 nm, $\Delta\mu$ effect is negligible as is illustrated in Figure 5.8. Furthermore, in 140 nm CMOS process, the scaling of the model over different-sized transistors is examined. The parameters of the statistical model, E_{NT}, $E_{\alpha C}$ and $E_{\alpha H}$, shown in Table 5.2 [28, 30], are obtained by fitting Equation 5.13 to measured variance. Bias-dependency of LFN is very interesting. As it will be shown below, ΔN and $\Delta\mu$ effects will determine variance in the region where each effect is dominant in the LFN model. Thus ΔN will affect 1/f noise variance mostly in moderate and strong inversion while $\Delta\mu$ in subthreshold region.

Parameter	N5X2	P5X2	N8X016
E_{NT}	1	4	6.1
E_{aC}	0.3	0.25	0.1
E_{aH}	0.1	0.1	–

Table 5.2: 1/f Noise variability model parameters of 180 nm, 140 nm CMOS nodes

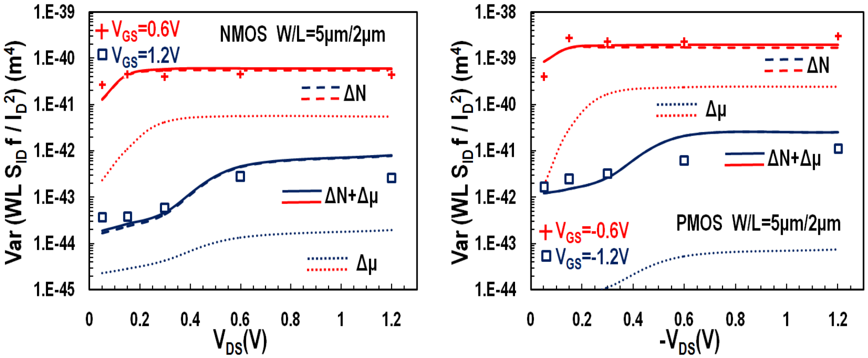
180 nm CMOS Process

The bias-dependence of the proposed model (Equation 5.13) is analyzed in Figures 5.9, 5.10 [28], for the same data for which the ln-mean data have been shown in Figures 5.6, 5.7. In Figure 5.9, the variance of normalized output noise at 1 Hz – $Var\left(WL * S_{ID}/I_D^2\right)$ – is shown versus drain current for both NMOS and PMOS $W/L = 5\,\mu m/2\,\mu m$ transistors in linear and saturation regimes. It is clear from our data that, for both low and high V_{DS}, variance is minimum in strong inversion and it becomes maximum in weak inversion, following a trend bearing similarity with ln-mean 1/f noise trend in Figure 5.6. In addition, in saturation region, variance is higher in comparison to linear region for every drain current value [207, 208, 211]. The complete model follows the data qualitatively well and with an appreciable consistency. Dashed lines representing the different noise deviation contributors provide interesting insight. The ΔN effect is seen to be dominant in moderate to strong inversion. In weak inversion, the deviation due to ΔN effect in linear mode and saturation coincides. Furthermore, as the inversion level increases, the correlated number and mobility fluctuation ($\alpha\mu$ product) – most clearly apparent in PMOS – is seen to contribute to statistical 1/f noise variance. This has been mentioned in [207, 208, 209], however, no physics-based compact model had been proposed. Detailed data are shown for both linear and saturation regimes in weak inversion. The increased deviation under high V_{DS} conditions in comparison to linear region is well modeled through the mobility fluctuation ($\Delta\mu$) effect. The $ln(q_s/q_d)$ term in Equation 5.12 is dominant in weak inversion and leads to higher variation in saturation, where (q_s/q_d) becomes very large. Conversely, in linear region, q_d is comparable to q_s. In Figure 5.10, variance of flicker noise is shown versus drain voltage for both NMOS and PMOS devices at two gate voltage values; one near threshold voltage and one at strong inversion region ($|V_{GS}| = 1.2\,V, 0.6\,V$), corresponding to Figure 5.7. The model again shows qualitatively good results.



(a) (b)

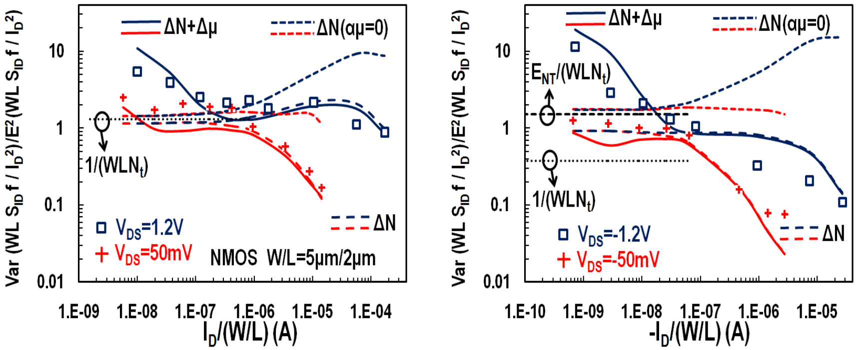
Figure 5.9: Variance of output noise $WL * S_{ID}/I_D^2$, referred to $1\,Hz$, in linear and saturation region ($|V_{DS}| = 50\,mV, 1.2\,V$) vs. drain current $I_D/(W/L)$, for a) n- and b) p-channel MOSFETs with $W/L = 5\,\mu m/2\,\mu m$. Markers: measured, lines: complete model (Equation 5.13), dashed: individual contributions of number (Equation 5.7) and mobility (Equation 5.12) fluctuations.



(a) (b)

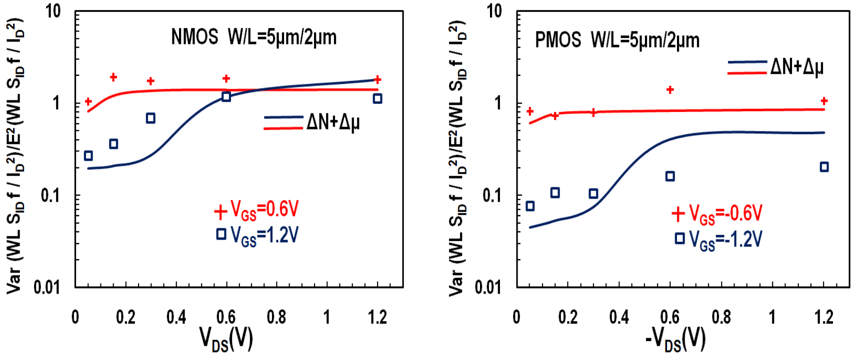
Figure 5.10: Variance of output noise $WL*S_{ID}/I_D^2$, referred to $1\,Hz$, at $|V_{GS}| = 1.2\,V, 0.6\,V$, respectively, vs. drain voltage $|V_D|$, for a) n- and b) p-channel MOSFETs with $W/L = 5\,\mu m/2\,\mu m$. Markers: measured, lines: complete model (Equation 5.13), dashed: individual contributions of number (Equation 5.7) and mobility (Equation 5.12) fluctuations.

Some interesting observations can be made by examining the normalized variance of output noise, $Var\left(WLS_{I_D^2}/I_D^2\right)/E\left(WLS_{I_D^2}/I_D^2\right)$ as shown in Figures 5.11, 5.12. As noted in Section 5.3.3.2, the number of traps $N_{tr} = WLN_t$ is supposed to follow a Poisson distribution and hence $Var(N_{tr}) = WLkTN_T$. In weak or moderate inversion (in absence of $\Delta\mu$ effect, supposing $\alpha\mu \approx 0$), we find that normalized variance $Var\left(WLS_{I_D^2}/I_D^2\right)/E\left(WLS_{I_D^2}/I_D^2\right) = 1/WLN_t$. This quantity is indicated in Figure 5.11. For the NMOS case, this observation is reasonably well confirmed, if we ignore the incidence of $\Delta\mu$ effect. Hence, this indicates that the above reasoning is correct and supports the Poisson distribution of number of traps N_{tr}. For PMOS, the E_{NT} parameter differs from unity; the normalized variance is $Var\left(WLS_{I_D^2}/I_D^2\right)/E\left(WLS_{I_D^2}/I_D^2\right) = E_{NT}/WLN_t$, illustrating the usefulness of introducing some flexibility in the statistical model. Accordingly, in the PMOS case, the assumption of Poisson distributed N_{tr} is less well supported [28]. The latter expression is confirmed by Equation 5.17 since $\Lambda_D\,|_{\Delta N}\,/\,(16*K_D\,|_{\Delta N})$ equals to unity in weak and early moderate inversion [30]. Interestingly, the ΔN($\alpha\mu = 0$) model in linear mode is shown to be practically independent of drain current (hence V_G) from weak to strong inversion. In strong inversion saturation, the ΔN($\alpha\mu = 0$) shows increased normalized variance with respect to weak-moderate inversion. In either case, the non-zero $\alpha\mu$ product is responsible for the drop of normalized variance in strong inversion.



(a) (b)

Figure 5.11: Normalized variance of output noise $WL * S_{ID}/I_D^2$, referred to $1\,Hz$, in linear and saturation region ($|V_{DS}| = 50\,mV$, $1.2\,V$) vs. drain current $I_D/(W/L)$, for a) n- and b) p-channel MOSFETs with $W/L = 5\,\mu m/2\,\mu m$. Markers: measured, lines: complete model (Equation 5.13), dashed: individual contributions of number (Equation 5.7) and mobility (Equation 5.12) fluctuations.

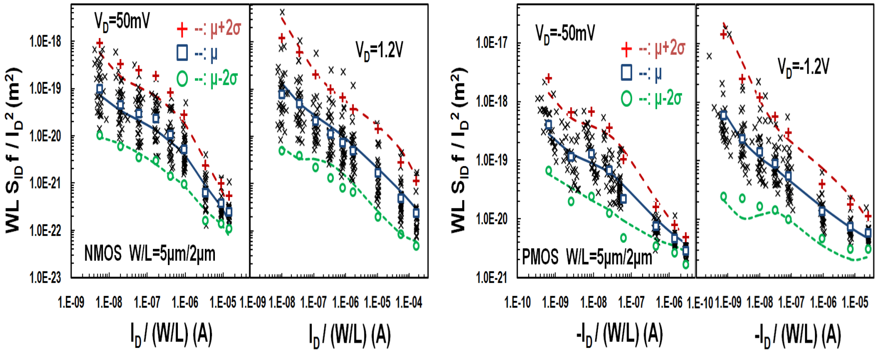


(a) (b)

Figure 5.12: Normalized variance of output noise $WL * S_{ID}/I_D^2$, referred to $1\,Hz$, at $|V_{GS}| = 1.2\,V, 0.6\,V$, respectively, vs. drain voltage $|V_D|$, for a) n- and b) p-channel MOSFETs with $W/L = 5\,\mu m/2\,\mu m$. Markers: measured, lines: complete model (Equation 5.13), dashed: individual contributions of number (Equation 5.7) and mobility (Equation 5.12) fluctuations.

Generally speaking, the noise measurements are very sensitive, particularly in weak inversion [210]. As a consequence the handling of statistical noise quantities is very sensitive, particularly so the normalized variance of noise, but even for variance and average noise. Based on the log-normal distribution of noise [30, 211, 213, 214, 215, 216], ln-mean data is shown for average noise while variance is calculated from $\sigma\left(ln\left(WL*S_{I_D^2}/I_D^2\right)\right)$ and normalized variance is obtained inverting the Equation 5.15 [30, 211].

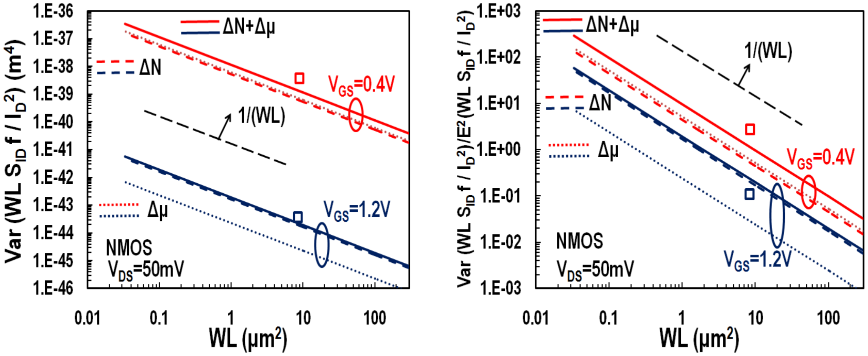
Figure 5.13 [28] presents the detailed data of measured normalized flicker noise $WL*S_{ID}/I_D^2$ at $1\,Hz$ versus normalized drain current, for NMOS and PMOS transistors with $W/L = 5\,\mu m/2\,\mu m$ with $|V_{DS}|$ equal to $1.2\,V$ and $50\,mV$. The model is shown to represent well the mean value of noise as well as its standard deviation $\sigma\left(WL*S_{ID}/I_D^2\right)$. In each case, the markers represent the measured noise values for all devices on the wafer, while lines represent statistical (average) noise model integrated in the EKV3 charge-based compact model, extracted from the ln-averaged noise data. The dashed red and green lines represent the $\pm 2\sigma$ standard deviation as extracted by the model (Equation 5.13) proposed in the present work, and give a reasonable estimate of the respective data spread (markers). This representation confirms the consistency among physical and statistical charge-based 1/f noise models.



(a) (b)

Figure 5.13: Output noise $WL*S_{ID}/I_D^2$, referred to $1\,Hz$, vs. drain current $I_D/(W/L)$, measured for a) N-channel and b) P-channel devices with geometry $W/L = 5\,\mu m/2\,\mu m$ in linear region at $|V_{DS}| = 50\,mV$ (left subplot) and saturation region at $|V_{DS}| = 1.2\,V$ (right subplot). Measured noise: crosses. Measured ln-mean noise, ±2-sigma deviation: open markers. EKV3 model: average noise (lines), ±2-sigma deviation (dashed).

Finally, Figure 5.14 illustrates the geometrical scaling inherent in the present statistical LFN model. Either ΔN and $\Delta\mu$ effects show a scaling of variance vs. area $Var\left(WL*S_{ID}/I_D^2\right) \sim (WL)^{-1}$– or equivalently, a scaling of standard deviation vs. area $\sigma\left(WL*S_{ID}/I_D^2\right) \sim (WL)^{-1/2}$, as is observed e.g. in [208] for smaller area devices. The same applies for normalized variance $Var\left(WL * S_{ID}/I_D^2\right)/E\left(WL * S_{ID}/I_D^2\right) \sim (WL)^{-1}$ [212].

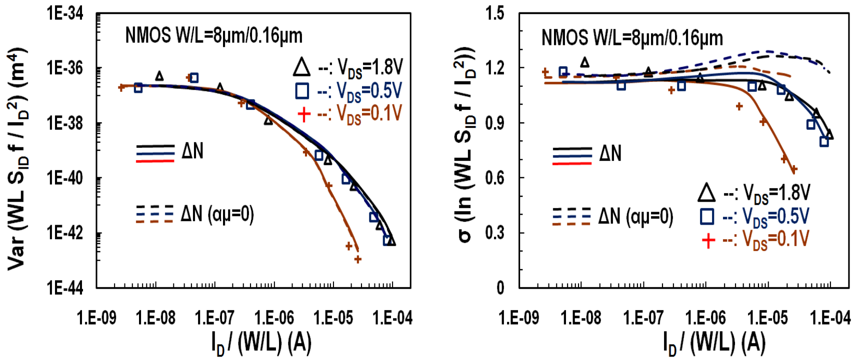


(a) (b)

Figure 5.14: Variance (a) and normalized variance (b) of normalized output noise vs. area in linear mode, showing the same $1/(WL)$ scaling trends for variability due to ΔN and $\Delta\mu$ variations.At $V_{GS} = 1.2\,V$, ΔN effect dominates, while $\Delta\mu$ effect dominates at $V_{GS} = 0.4\,V$. Lines: entire model (ΔN+$\Delta\mu$), dashed: ΔN contribution. dotted: $\Delta\mu$ contribution, markers: measured data of $W/L = 5\,\mu m/2\,\mu m$ NMOS device.

140 nm CMOS Process

The bias-dependence of the proposed model (Equation 5.13) is also confirmed for an NMOS short channel device with $W/L = 8\,\mu m/160\,nm$ from an $140\,nm$ CMOS process [211]. The variance, as well as the standard deviation of the natural logarithm of normalized output noise referred to $1\,Hz$, are shown versus drain current in Figure 5.15 [30], for the same data for which the mean data have been shown in Figure 5.8. The model shows a good qualitative fit to the variability data with extracted parameters as in Table 5.2. As in $180\,nm$ case, variance behaves similarly to mean-value as far as ΔN effect is concerned since $\Delta\mu$ effect is negligible here. As far as standard deviation of logarithm of noise is concerned, it has a similar behavior with normalized variance for the $180\,nm$ CMOS process as it is shown in Figure 5.11. This is reasonable due to Equation 5.15 which connects these two quantities. The effect of $\alpha\mu$ product is confirmed in this process also since the standard deviation of natural logarithm of noise demonstrates a high sensitivity to it.



(a) (b)

Figure 5.15: a) Variance and b) standard deviation of the natural logarithm of of output noise $WL*S_{ID}/I_D^2$, referred to $1\,Hz$, vs. drain current $I_D/(W/L)$ for an N-channel MOSFETs with $W/L=8\,\mu m/160\,nm$ at $V_{DS}=100\,m$, 0.5 and $1.8\,V$ respectively. Markers: measured data, lines: model with $\alpha\mu \cong 0.06$ depending on bias, dashed lines: model with $\alpha\mu=0$.

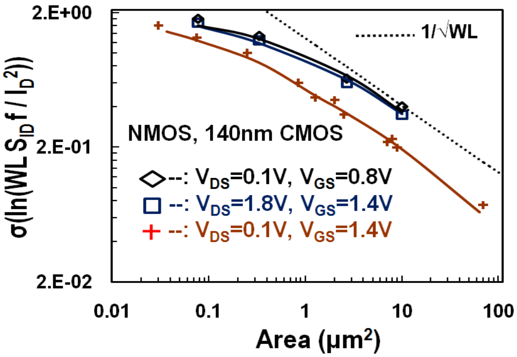


Figure 5.16: Normalized standard deviation of LFN for NMOS devices vs. area at different bias conditions. Open markers: measured data of $140\,nm$ CMOS, lines: model. The dotted line indicates $1/\sqrt{WL}$ scaling.

In order to confirm the geometrical scaling of the model with gate are, Figure 5.16 shows data from $140\,nm$ CMOS process [211] for NMOS devices. In this graph, data is plotted versus area at various bias points including linear and saturation regions as well as moderate and strong inversion. The same parameters are used as in Figure 5.15. The consistency of area scaling of the variability model is expected due to the adoption of lognormal statistics of LFN variability as in

[30, 211]. It is clear that the model follows the scaling properties of [211], namely $\sigma ln(S_{ID}) \sim \sqrt{ln[1+K/(WL)]}$ resulting in $\sigma ln(S_{ID}) \sim 1/\sqrt{WL}$ for large area devices.

5.3.4 Model Implementation for HV-MOSFETs

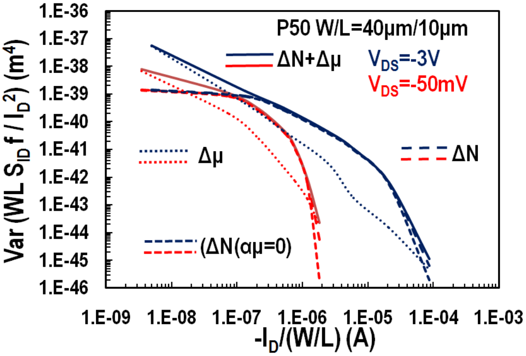


Figure 5.17: Variance of output noise $WL*S_{ID}/I_D^2$, referred to $1\,Hz$, in linear and saturation region ($V_{DS} = -50\,mV$, $-3\,V$) vs. drain current $I_D/(W/L)$, for a P50 HV-MOSFET with $W/L = 40\,\mu m/1\,\mu m$. Lines: complete model (Equation 5.20), dashed: individual contributions of number (Equation 5.18) and mobility (Equation 5.19) fluctuations.

As it was shown in Chapter 4, 1/f noise in HV-MOSFETs is mostly generated by the channel part while noise from drift region becomes significant under specific circumstances such as low drain voltage and long channel length. The channel part of a HV device is quite similar with a conventional LV-MOS transistor and thus carrier number fluctuation as well as mobility fluctuation effects that are the main 1/f noise generators in LV-MOSFETs, also prevail in the channel part of the HV device. Equations 4.2, 4.4, which describe ΔN and $\Delta\mu$ effects in LV part of HV-MOSFETs respectively [27], are equivalent with Equations 3.38, 3.41 which refer to the LV 1/f noise model [24, 33] with just replacing normalized drain charge q_d with normalized K-point charge q_k. Since the fundamental principles of 1/f noise generation are the same in the channel part of both LV and HV devices, we can assume that the physics-based model for the variability of 1/f noise in MOSFETs presented above [28] can be applied to HV-MOSFETs as well. Unfortunately, this modeling approach can not be validated here with data since no sufficient sample of measurements is available in LDMOS devices under test.

Nevertheless, Equations 5.7, 5.12 and 5.13, referring to LV-MOSFETs can also be used for HV-MOSFETs with q_k replacing q_d as the “inner” drain of the LV part of the HV device. Thus for ΔN effect we can assume:

$$
\begin{aligned}
&Var\left(WLf * \frac{S_{I_D^2}}{I_D^2}\,|_{\Delta N_{LV}}\right) = \\
&\left(\frac{1}{LWN_{SPEC}^2}\right)^2 WLN_t \frac{2}{i_d}\int_{q_k}^{q_s}\left(\frac{1}{q_i+1/2}+\alpha\mu\right)^4 (q_i+1/2)\,dq_i = \\
&\frac{N_t}{N_{SPEC}^4 WL}\left(\begin{matrix}\dfrac{1}{(q_s+0.5)^2+(q_k+0.5)^2}+(\alpha\mu)^4+\dfrac{8(\alpha\mu)^3}{1+q_s+q_k}+\\ \dfrac{12(\alpha\mu)^2}{i_d}ln\left(\dfrac{1+2q_s}{1+2q_k}\right)+\dfrac{8(\alpha\mu)}{(q_s+0.5)(q_k+0.5)(1+q_s+q_k)}\end{matrix}\right)
\end{aligned}
\tag{5.18}
$$

and for $\Delta\mu$ effect:

$$
\begin{aligned}
&Var\left(WLf * \frac{S_{I_D^2}}{I_D^2}\,|_{\Delta\mu_{LV}}\right) = \\
&\frac{\alpha_H^2}{WLN_tN_{SPEC}^2}\frac{1}{i_d}\int_{q_k}^{q_s}\left(\frac{2}{q_i}+\frac{1}{q_i^2}\right)dq_i = \\
&\frac{\alpha_H^2}{WLN_tN_{SPEC}^2}\frac{1}{i_d}\left(2ln\left(\frac{q_s}{q_k}\right)+\frac{q_s-q_d}{q_sq_k}\right)
\end{aligned}
\tag{5.19}
$$

while the total variance can be calculated as:

$$
Var\left(WLf * \frac{S_{I_D^2}}{I_D^2}\right) = Var\left(WLf * \frac{S_{I_D^2}}{I_D^2}\,|_{\Delta N_{LV}}\right) + Var\left(WLf * \frac{S_{I_D^2}}{I_D^2}\,|_{\Delta\mu_{LV}}\right) \tag{5.20}
$$

Statistical 1/f noise parameters similar to Equation 5.14, can also be used for the 1/f noise variability model for HV-MOSFETs. In Figure 5.17, the variance of 1/f noise in a P50 short device, with $W = 40\,\mu m$, $L = 1\,\mu m$, is shown versus normalized drain current for linear and saturation regions ($V_{DS} = -50\,mV$, $-3\,V$). 1/f noise parameters from Table 4.2 were used for the mean value model while for the variability model, the 1/f noise statistical parameters of the PMOS device from Table 5.2 were used and the specific device was chosen since both ΔN and $\Delta\mu$ effects seem to be active. In accordance to LV-MOSFETs (Figure 5.9), the same conclusions can be drawn for this HV device as far as 1/f noise statistics are concerned. Thus, 1/f noise variability increases in weak inversion due to $\Delta\mu$ effect while noise variability from moderate to strong inversion is dominated by the ΔN effect. Furthermore, as the inversion level increases, the correlated number and mobility fluctuation ($\alpha\mu$ product) is seen to contribute to statistical 1/f noise. Furthermore, 1/f noise variability is higher in saturation than linear regime at all levels of inversion. This is covered by ΔN effect in moderate to strong inversion but in weak inversion, deviation due to ΔN effect seems to coincide. It is $\Delta\mu$ effect that seems to explain the increased variability in saturation region in weak inversion.

5.4 Conclusions

This chapter of our Thesis investigates in detail the bias-dependence of 1/f noise variability in large-area, standard bulk MOSFETs. An analytical statistical compact model is developed, based on number and mobility fluctuation mechanisms ΔN and $\Delta\mu$, where the flicker noise variability is obtained from the variability of trap density N_T and Hooge parameter α_H, respectively. Variability affecting current, transconductance (via the inversion charge densities at source and drain) is naturally reflected also in the noise model, however, the total noise variability is mainly due to variability of number of traps and mobility fluctuations, which are essentially uncorrelated with the former. The resulting compact model allows for the first time to cover the observed variability of 1/f noise over all bias conditions, from weak to strong inversion, as well as from linear to saturation regions. Data measured at our lab are from an experimental $180\,nm$ CMOS process on n- and p-channel devices while data are also taken from bibliography from an $140\,nm$ CMOS process [211]. ΔN and $\Delta\mu$ effects affect 1/f noise statistics in a consistent and similar way they affect 1/f noise ln-mean value. ΔN effect is responsible for noise variance behavior in moderate and strong inversion, while $\Delta\mu$ effect (if present) may dominate in weak inversion. This work leads to a consistent model of variance of 1/f noise , containing both ΔN (including correlated ΔN-$\Delta\mu$ noise) and $\Delta\mu$ components. The noise variability model is highly consistent with the noise model at all bias conditions. Its parameters can actually be estimated from the parameters of the noise model itself, and may be further refined based on measured data. The bias-dependence of the statistical 1/f noise model has been validated for both gate and drain bias dependence [28, 30]. The geometrical scaling of the statistical noise model is also validated [30] and proved to be consistent with [211]. Finally and due to strong similarity of LV MOSFETs with the LV part of HV-MOSFETs, the developed 1/f noise variability model can be applied to HV-MOSFETs by just replacing normalized drain charge q_d with normalized K-point charge q_k. Unfortunately, not enough data were available in order the model to be validated in such power devices.

Chapter 6

Conclusions

The fundamental original contributions of this Thesis are presented in this conclusive chapter. Low frequency noise is very crucial in modern analog and RF design which makes the need of reliable compact models very important. Charge-based compact modeling of both mean value of 1/f noise in HV MOSFETs presented in Chapter 4, and variability of 1/f noise in moderately-sized MOSFETs in Chapter 5, constitutes a state-of the art situation since no physics-based compact models were available until now to the best of our knowledge. An attempt to model the statistics of 1/f noise in HV-MOSFETs is also presented based on the similarity of the channel part of a HV-MOSFET with an LV-MOSFET, but no sufficient data are available to validate this effort.

Before addressing the innovative issues of this work in Chapters 4, 5 mentioned above, an explicit analysis of 1/f noise physics in MOSFETs is presented in Chapter 3. It is proven throughout our research, that the main phenomena that generate LFN in MOSFETs such as carrier number fluctuation, mobility fluctuation and series resistance effects, are responsible for creation of LFN in HV-MOSFETs and are also connected with LFN variability. A new charge-based 1/f noise compact model is addressed in Chapter 3 [24, 33] describing the above effects which is of great importance since it will be the basis for the rest of the modeling work in this Thesis. This model was successfully validated at two different experimental CMOS processes at 180 nm, 90 nm.

In Chapter 4, a new complete 1/f noise compact model for LDMOS transistors is proposed and validated for the first time [27, 34, 35] as the few modeling approaches available until now do not establish a compact solution. Until recently, LV part of the HV-MOSFETs was considered to be the only source generating LFN and as a result LV 1/f noise models were used for these devices. Recent research has revealed additional 1/f noise sources in the extension of gate oxide in the drift region of an LDMOS device which were unexplored until now mainly because of lack of adequate 1/f noise measurement set up under high-voltage conditions. In the context of this Thesis, the 1/f noise of an LDMOS transistor was measured and characterized for a 350 nm HV-MOS process provided by AMS. For the purpose of this characterization, a new measurement set-up was provided by AdMOS permiting 1/f noise measurements up to 200 V and this was an important breakthrough for the accomplishment of our research. The next step would be to explore and locate all the 1/f noise sources both in channel part and drift region of the LDMOS transistor. In the channel part which is similar with a conventional LV-MOSFET, flicker noise is caused by the same effects as in standard MOSFETs such as carrier number fluctuation due to trapping/detrapping mechanism in the oxide interface, mobility fluctuation effect and series resistance effect. A similar trapping/detrapping mechanism in the extension of the gate oxide which overlaps with drift region can create an additional 1/f noise source in the HV part of the device. Flicker noise which is generated by this carrier number fluctuation effect, becomes significant and comparable to noise arising from the channel in linear region and strong inversion of long channel transistors. Furthermore, the quasi-saturation effect which is a characteristic effect taking place only in HV-MOSFETs also affects flicker noise.

All the above effects are successfully included into the new complete charge-based 1/f noise compact model for LDMOSFETs [27] and the validation of the model gives outstanding results over all possible operating conditions from weak to strong inversion, for linear and saturation modes and for a lot of different device geometries [34]. In more detail, when 1/f noise is shown versus drain bias, the effect of the drift region on it under linear regime and strong inversion of long devices can be spotted very clearly. In fact, S_{ID} ressembles an output characteristic while S_{VG} remains constant when drift region contribution is de-activated and starts to increase when it becomes active. Furthermore, quasi-saturation and self-heating effect are also clearer when 1/f noise is shown versus drain voltage.

The next accomplishment of our work presented in Chapter 4, is the proposal of an accurate 1/f noise parameter extraction methodology for LDMOSFETs, something that is also implemented for the first time [35]. A simpler methodology was firstly proposed [199] focusing mainly on the LV part of the transistor while the most comrehensive one followed [35]. In the latter, a wide bias and geometry data range was used and as a result each 1/f noise parameter is extracted from the operating region that is dominant. The usage of the values of the extracted parameters to the new 1/f noise model gives excellent results.

1/f noise variability modeling is considered of equal importance with the mean value 1/f noise models in MOSFETs. In fact, there is a strong relation between the effects that are responsible for creating 1/f noise such as carrier number fluctuation and mobility fluctuation, and the statistical behavior of flicker noise. A more important and useful observation is that each effect affects 1/f noise variability under the conditions where it is dominant. All the above are analyzed in Chapter 5 while a new charge-based compact model for LFN variability in moderately-sized MOSFETs is proposed for first time [28], [30].

In more detail, the bias-dependence of 1/f noise variability is investigated for both n- and p-channel MOSFETs with $W/L = 5\,\mu m/2\,\mu m$ from an $180\,nm$ CMOS process with data measured at our lab. Furthermore, data taken from bibliography from an $140\,nm$ CMOS process [211], is also used for the validation of the model. More specifically, the bias-dependence of 1/f noise variability is investigated for an N-channel MOSFET with geometry $W/L = 8\,\mu m/160\,nm$ while area-dependence is also studied since standard deviation values of natural logarithm of normalized output noise for different area values at three bias conditions are also taken from[211]. The proposed compact 1/f noise variability model covers all the operating conditions, from subthreshold to higher current region as well as linear and saturation modes for the first time while it also provides an excellent geometrical scaling behavior. The model is developed, based on carrier number fluctuation and mobility fluctuation effects where the 1/f noise variability is caused by the deviation of trap density N_T and Hooge parameter α_H respectively. The most important experimental conclusion that is also covered by the model in a perfect way, is that carrier number fluctuation and mobility fluctuation phenomena affect 1/f noise statistical behavior in a similar way they affect the mean value of noise. ΔN effect is responsible for the behavior of 1/f noise variability in moderate and strong inversion while $\Delta\mu$ is dominant in weak inversion. The new 1/f noise variability model gives excellent results while it is highly consistent with the mean value model over all operating regions.

Appendix A

Empirical Model for Low Frequency Noise Variability in Moderately Sized MOSFETs

In this Appendix, an empirical model for the gate voltage dependecne of 1/f noise variations in moderately-sized transistors and saturation region is proposed [29]. We show that the gate voltage dependence may be related to transconductance-to-current ratio g_m/I_D. Extensive measurements of low frequency noise variability in an experimental $180\,nm$ CMOS confirm the newly proposed model.

A.1 Introduction

As explained in detail in Chapter 5, in smaller-sized devices, noise fluctuations are area dominated. In moderate- to large-sized transistors ($Area \ggg 1\mu m^2$), normalized noise fluctuations are roughly independent of area, but show a distinct degradation towards weak inversion (subthreshold). Althoug a new charge-based 1/f noise variability compact model was recently proposed [28] and presented in Chapter 5, this empirical formulation described here might be quite useful from design point of view since it relates bias-dependence of flicker noise variability with the very important g_m/I_D ratio. In fact the standard deviation of the logarithm of normalized noise follows this g_m/I_D trend. Devices under test are the same as the ones analyzed in Chapter 5 (NMOS-PMOS with $W/L = 5\,\mu m/2\,\mu m$) while the measurements were executed in our lab and for the specific task only the high drain voltage data ($|V_{DS}| = 1.2V$) were used while gate voltage values covered from weak to strong inversion with $|V_{GS}| = 0.35, 0.4, 0.45, 0.5, 0.55, 0.6, 0.8, 1.2, 1.8\,V$.

A.2 Model Implementation

The first step in this work was to calculate the standard deviation for each device at each bias point measured. Initially, output noise divided by squared drain current normalized with device area – $WL * S_{ID}/I_D^2$ – was extracted at $1\,Hz$. Because of the log-normal behavior of the statistics of LF noise [210, 211], it is more relevant to calculate the standard deviation of $log\left(WLf * S_{ID}/I_D^2\right)$. The most widely used carrier number fluctuation model from FBP approach is given by Equation 3.34 and is described by two basic parameters introduced in Section 3.4.3: N_T and α_C. The statistical deviation of these two parameters plays a significant role in the variability of flicker noise. Former work [162, 206, 208, 209, 212, 213, 215, 216] has shown the correlation between N_T parameter and noise variability coming from device dimensions. Small-area devices have a low number of traps and therefore RTS noise is observed, which leads to increased noise variability. N_T parameter follows Poisson statistics [208, 209], and therefore the relative standard deviation of the number of traps equals:

$$\sigma_{N_t} = \frac{1}{\sqrt{N_t WL}} \tag{A.1}$$

where N_t is the trap density in cm^{-2}. Equation A.1 can describe the dependence of 1/f noise variability with device dimensions but not with gate voltage. Since the mean value 1/f noise model in Equation 3.34 connects 1/f noise with g_m/I_D ratio, the motivation of this work was to test if the same is valid for the variability of 1/f noise. Based on the above observation, a new complete statistical LFN model is proposed in this work, which covers both the area-dependent and the bias-dependent statistical behavior of 1/f noise as follows [29]:

$$\sigma\left[log\left(WLf * \frac{S_{ID}}{I_D^2}\right)\right] = \sqrt{B^2 \frac{g_m U_T}{I_D} + \frac{A^2}{WL}} \tag{A.2}$$

where $A = 1/\sqrt{N_t}$ and B are the statistical model parameters. The bias-dependent, unitless term $g_m U_T/I_D$ maximizes noise variability in weak inversion for large-area devices. Equation A.2, without the bias-dependent term reduces to the formerly used equation [213, 215, 216].

A.3 Results and Discussion

The behavior of the proposed model is presented in Figure A.1 [29]. The standard deviation of flicker noise versus normalized drain current $I_D/(W/L)$ for both NMOS and PMOS transistors with $W/L = 5\,\mu m/2\,\mu m$ is shown. In these moderately- to large-sized devices, the bias-dependent term plays an important role. Variability of 1/f noise follows a $g_m U_T/I_D$ behavior as discussed before and proposed in the present work. NMOS devices show a higher noise variability than PMOS. The parameter B can be determined by matching the model to these measurements. Table A.1 [29] includes the extracted parameters for both NMOS and PMOS devices. The consistency of the model seems quite good in all cases of device type, size, and bias conditions.

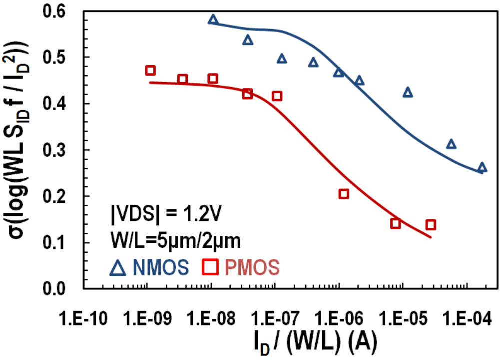


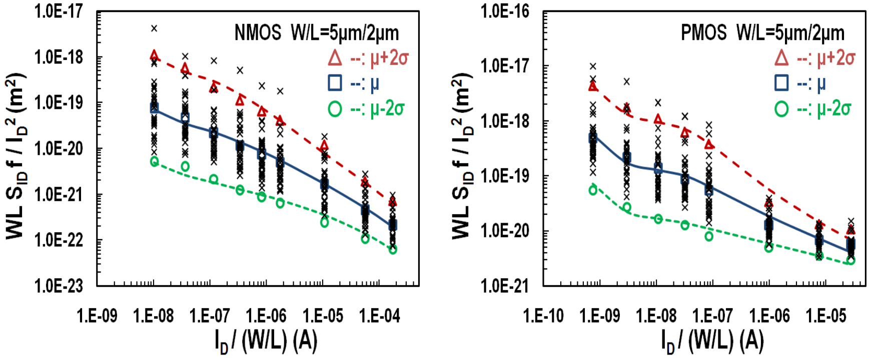
Figure A.1: Normalized standard deviation of the logarithm of output noise $log\left(WL*S_{ID}/I_D^2\right)$, referred to $1\,Hz$, measured in saturation region ($|V_{DS}| = 1.2\,V$) vs. normalized drain current $I_D/(W/L)$, for n- (blue) and p-channel (red) MOSFETs with $W/L = 5\,\mu m/2\,\mu m$. Measurement (markers), full model (lines).

Parameter	NMOS	PMOS
$A\ (\mu m)$	0.11	0.9
B	0.98	0.53

Table A.1: Parameters of 1/f Noise variability model

Figure A.2 [29] presents a more detailed analysis of flicker noise and its standard deviation versus normalized drain current. Both NMOS and PMOS transistors with $W/L = 5\,\mu m/2\,\mu m$ are shown in left and right plot, respectively. Output noise S_{ID}/I_D^2 is normalized with device area and referred to $1\,Hz$. In each case, the markers represent the measured noise values for all devices on the wafer, while blue solid lines represent statistical noise model integrated in the EKV3 charge-based compact model, extracted from the log-averaged noise data. The noise parameters extracted for the physical EKV3 model are comparable to Table 5.1 with the usage of Equation 3.34. The dashed red and green lines in Figure A.2, represent the $\pm 2\sigma$ standard deviation as extracted by the model proposed in the present work. To produce the $\pm 2\sigma$ plots, we first calculate the $10^{\pm 2\sigma(sim)}$ for each case just to take out the log term and then multiply the result with the extracted average noise of the compact model.

Note that the statistical noise model proposed in this work gives overall very good results. The behavior of simulated $\pm 2\sigma$ plots follows qualitatively well the dispersion of noise measurements. The choice of $\pm 2\sigma$ values of variation is however just indicative, and the model user may choose a larger spread, e.g. $\pm 3\sigma$.



(a) (b)

Figure A.2: Output noise $WL * S_{ID}/I_D^2$, referred to $1\,Hz$, measured in saturation at $V_{DS} = 1.2\,V$, for transistors with geometry $W/L = 5\,\mu m/2\,\mu m$ vs. normalized drain current $I_D/(W/L)$, for a) NMOS and b) PMOS. Measured noise: crosses. Measured log-mean noise, ±2-sigma deviation: open markers. EKV3 model: average noise (lines), ±2-sigma deviation (dashed).

A.4 Conclusions

A thorough investigation of low frequency noise variability was performed in an experimental $180\,nm$ CMOS process. Shrinking of device dimensions leads to higher noise variability due to RTS noise caused by decreased number of traps. Conversely, in moderately- to large-sized transistors, the normalized variability of 1/f noise is not anymore area related, but becomes strongly bias-dependent: a distinct increase of normalized noise variability is observed when lowering the gate voltage, and a maximum plateau is reached in weak inversion. A new, simple and explicit statistical 1/f noise model is proposed to describe these effects, relating flicker noise variability to both area and gate bias [29]. While maintaining the habitual area-dependent parameter, A, for small area devices, the model proposes the area-independent term, B, to be bias-dependent with the transconductance-to-current ratio g_m/I_D. This provides for the first time a simple means for evaluating the noise dispersion in moderately- to large-sized devices, depending on level of inversion and device area. This simple hand calculation model may be used independently of a compact model, providing the parameters A and B are known.

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Curriculum Vitae

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Objective

- To obtain a Postdoctoral position in the broader field of micro- and nanoelectronic devices, circuits and systems, in order to apply and broaden my research expertise.

Summary

- I was born in Chania, Crete, Greece in 1981. I obtained the Diploma in Electronic and Computer Engineering, the M.Sc. degree and the Ph.D. from the School of Electronic & Computer Engineering, Technical University of Crete, Chania, Greece, in 2006, 2010, and 2016, respectively. The subject of my Ph.D. thesis is "Statistical charge-based modeling of 1/f noise in standard and high-voltage MOS transistors". I have participated in a number of European (FP7) as well as National R&D projects, as well as industry-funded projects. I have been an invited researcher with ams, Austria (2010-2011) and with AdMOS, Germany (2012). I have been a member of the EKV3 advanced MOSFET compact model development team since 2010. I am currently a research associate with the School of Electronic & Computer Engineering, Technical University of Crete, Chania, Greece, with emphasis on noise characterization and compact modeling of micro-/nanoelectronic devices. I have authored or co-authored 15 articles in peer reviewed scientific journals and conferences.

Work Experience

2010-2016	Semiconductor Researcher, School of Electronic & Computer Engineering, Technical University of Crete
2006-2016	Teaching Assistant (Electronics II, Analog CMOS Design), School of Electronic & Computer Engineering, Technical University of Crete
2012	Internship with ADMOS GmbH, Frickenhausen, Germany (2 months)
2010-2011	Internship with Austriamicrosystems AG, Unterpremstätten, Austria (12 months)

Education

2010–2016	Ph.D. School of Electronic & Computer Engineering, Technical University of Crete. Thesis: “Statistical Charge-Based Modeling of 1/f Noise in Standard and High-Voltage MOS Transistors”
2006–2010	MSc. School of Electronic & Computer Engineering, Technical University of Crete. Thesis: “1/f Noise Characterization in Advanced CMOS Technologies”
1999-2006	M. Eng. School of Electronic & Computer Engineering, Technical University of Crete. Grade: 7.56/10

Technical & Computer Skills

TECHNICAL SKILLS:	Characterization and compact modeling of standard CMOS, multigate CMOS, HV-MOS technologies Extraction of complete EKV2.6, EKV3, BSIM4, BSIM6 models in projects with industry (EM Microelectronic-Marin SA, Austriamicrosystems AG, AdMOS, Toshiba) Specialist in implementation of compact models in Verilog-A On-wafer measurements - DC, CV, Low Frequency Noise and RF setup and measurements
COMPUTER SKILLS:	Experienced user of ICCAP, Cadence and ADS

Research projects

2011–2013	NANOsympraxis, Multigate MOSFET nanotransistors: compact models for current and noise – development of automated design tools for nanoelectronics, “Synergasia 2009” Project Nr. 09ΣΥΝ-42-998, General Secretariat of Research and Technology (GSRT). Duration: 2011 – 2014
2011–2013	NexGenMiliWave, Next Generation Millimeter Wave Backhaul Radio, “Corallia” Hellenic Technology Cluster Initiative in Microelectronics, Phase 2, Project Nr. ΜΙΚΡΟ2-ΣΕ-Β/Ε-ΙΙ. Duration: 2009 – 2013
2010-2012	COMON, COmpact MOdelling Network, FP7-PEOPLE-2007-3-1-IAPP, Grant Nr. 218255, Marie Curie Industry Academia Partnership & Pathways, of the European Community. Duration: Dec. 2008 – Nov. 2012
2013-2014	EKV3.0 and EKV2.6 MOST modeling in ALP018D: EM 0.18µm CMOS process with embedded FLASH (EM MICROELECTRONIC SA 5)

2014-2015	Noise characterization of native, circular and buried channel MOSTs in EM 0.18µm CMOS process (EM MICROELECTRONIC SA 8)
2015	STD.LV NMOST LFN characterization 110nm CMOS (EM MICROELECTRONIC SA 9)
2015	EKV3.0 MOST modelling for EM 0.11µm-logic CMOS process (EM MICROELECTRONIC SA 10)
2016	Development of new mismatch model in subthreshold (EM MICROELECTRONIC SA 11)

Language Skills

FLUENT:	English
MOTHER TONGUE:	Greek

Personal Interests

Sports (Playing volleyball in a team for about 20 years)
Music, Cinema

Publications

Journals

1. **N. Mavredakis**, N. Makris, P. Habas, and M. Bucher, "Charge-Based Compact Model for Bias-Dependent Variability of 1/f Noise in MOSFETs," submitted to *IEEE Trans. Electron Devices*, 2016.

2. **N. Mavredakis**, W. Pflanzl, E. Seebacher, and M. Bucher, "Methodology for 1/f Noise Parameter Extraction for High Voltage MOSFETs," *Solid State Electronics*, Vol. 103, pp 202-208, January 2015.

3. A. Antonopoulos, M. Bucher, K. Papathanasiou, N. Makris, **N. Mavredakis**, R. K. Sharma, P. Sakalas, M. Schroter, "Modeling of High Frequency Noise of Silicon MOS Transistors for RFIC Design," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, special issue on Modeling of high-frequency silicon transistors*, Vol. 27, Issue 506, pp 802-811, 2014.

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5. **N. Mavredakis**, M. Bucher, R. Friedrich, A. Bazigos, F. Krummenacher, J. M. Sallese, T. Gneiting, W. Pflanzl, and E. Seebacher, "Measurements and Compact Modeling of 1/f Noise in HV-MOSFETs," *IEEE Trans. Electron Devices*, Vol. 60, No. 2, pp 670-676, February 2013.

Conferences

1. **N. Mavredakis**, and M. Bucher, “Compact Model for Variability of Low Frequency Noise due to Number Fluctuation Effect” to be presented in *46th Europ. Solid-State Device Res. Conf. (ESSDERC)*, Lausanne, Switzerland, September 12-15, 2016.

2. **N. Mavredakis**, W. Pflanzl, E. Seebacher, T. Gneiting, and M. Bucher, “Analysis of Drain Bias Dependence of 1/f Noise in HV-MOSFETs,” in *23rd Int. Conf. on Noise and Fluctuations (ICNF)*, Xian, China, June 2-6, 2015.

3. **N. Mavredakis**, P. Habas, A. Acovic, R. Meyer, and M. Bucher, “Variability of Low Frequency Noise in Moderately-Sized MOSFETs - a Model for the Area and Gate Voltage-Dependence,” in *23rd Int. Conf. on Noise and Fluctuations (ICNF)*, Xian, China, June 2-6, 2015.

4. K. Fellas, **N. Mavredakis**, W. Pflanzl, E. Seebacher, and M. Bucher, “Simple 1/f Noise Parameter Extraction Method for High-Voltage MOSFETs,” in *29th Int. Conf. on Microelectronics (MIEL 2014)*, pp. 89-92, Belgrade, Serbia, May 12-15, 2014.

5. R.K. Sharma, A. Antonopoulos, **N. Mavredakis**, M. Bucher,“Impact of Design Engineering on RF linearity and Noise Performance of Nanoscale DG SOI MOSFETs,” in *14th Int. Conf. on Ultimate Integration of Silicon, (ULIS 2013)*, pp 145-148, Warwick, UK, March 19-21, 2013.

6. R.K. Sharma, A. Antonopoulos, **N. Mavredakis**, M. Bucher,“Analog/RF Figures of Merit of Advanced DG MOSFETs,” in *8th Caribbean Conf. on Devices, Circuits and Systems, (ICCDCS 2012)*, pp 1-4, Mexico, March 14-17, 2012.

7. **N. Mavredakis**, A. Antonopoulos, and M. Bucher, “Measurement and Modeling of 1/f Noise in 180nm NMOS and PMOS Devices,” in *Proc. 5th European Conf. on Circuits & Systems for Communications (ECCSC)*, pp. 86-89, Belgrade, Serbia, November 23-25, 2010.

8. **N. Mavredakis**, A. Antonopoulos, and M. Bucher, “Bias Dependence of Low Frequency Noise in 90nm CMOS,” in *Proc. NSTI-Nanotech/Microtech*, vol. 2, pp. 805-808, Anaheim, California, June 21-25, 2010.

9. A. Antonopoulos, **N. Mavredakis**, N. Makris, M. Bucher,“System level analysis of a direct-conversion WiMAX receiver at 5.3GHz and corresponding mixer design,” in *15th Int. Conf. on Mixed Design of Integrated Circ & Syst. (MIXDES 2008)*, pp. 291-296, Poznan, Poland, June 19-21 2008.

10. **N. Mavredakis**, and M. Bucher, “Inversion-Level Based Design of a 5.5GHz RF CMOS Low-Noise Amplifier,” in *13th IEEE Int. Conf. on Electronics, Circ. & Syst. (ICECS 2006)*, pp 74-77, Nice, France, December 10-13, 2006.