Electrical Characterization and Compact Modeling of Power D-MOSFETs

Diploma Thesis

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Acknowledgments

This Diploma Thesis is dedicated to my parents who throughout these years they supported me economically and mentally but most importantly they were proud of me and my work.

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Finally I want to heartily thank my girlfriend who encouraged me the last months of my work and helped me mentally to overcome any difficulties.

Abstract

The purpose of this diploma thesis is to investigate the electrical behavior of two kinds of modern power transistors, namely Lateral (LDMOS) and Vertical (VDMOS) devices. N-type transistors have been characterized experimentally by both static and dynamic techniques. The measurement setups are discussed along with the equipment used to conduct those measurements. Different transistor geometries are investigated where available. Subsequently, parameter extraction techniques are employed, and the statistics of parameter spread is established. For the VDMOS devices in particular, a modelling approach will be followed, with the measurements being the basis for parameter extraction for the EPFL-HV compact model.

This thesis is organized as follows: Chapter 1 is a brief introduction about the importance of D-MOS technology and the model that will be used to simulate their operation, in Chapter 2 the structure and operation of bulk-MOS and the two types of DMOS transistor is described and in Chapter 3 a description of the EPFL-HV MOSFET model is given along with an explanation of the phenomena it can simulate. Chapters 4 and 5, are dedicated to the experimental measurements of two device families, with 4 devices being analyzed three lateral and one vertical. In Chapter 5 the parameter extraction methodology for the EPFL-HV is also described and demonstrated. Finally, Chapter 6 contains the conclusion of this thesis with the experimental deductions and proposals for possible future work.

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1 Introduction

1.1 Modeling of power D-MOSFETs

The MOS transistor (metal oxide semiconductor transistor) is the basic component in integrated circuits and is also widely used in analog and digital applications as a discrete part. The length of each transistor is becoming shorter every year with a minimum of 7nm nowadays. While there are many uses for low power MOS transistors, such as integrated circuits, there is a large requirement in commercial and industrial applications for high power capability components. These components are to be used in high voltage and high current switching applications, for example DC to DC converters, AC to DC power inverters and electric automobile systems. This is exactly the region where Double Diffused MOS (DMOS) transistors have their most significant role. The advantages of DMOS technology include high current carrying capability with low power dissipation even at relatively small device packages, high frequency switching operation and low manufacturing cost due to their wide use. Different structures and semiconductor materials, like SiC or even graphene are being investigated with the aim of improving performance, maximizing device durability and minimizing power losses.

In order for MOS technology to improve, operation on the physical as well as electrical level needs to be better understood and characterized. Specifically for DMOSFETs there are currently several models in use (most widespread are the “BSIM-HV" and "HiSIM-HV" models), which consist of a large number of parameters, making their use more complicated.. For these reasons, it is very important for compact models, describing these transistors, to be accurate and detailed, while maintaining a small parameter count. In this thesis, the EPFL compact model for Lateral and Vertical double diffused MOSFET [1] will be used to describe the operation of a VDMOS transistor, specifically, BS170 by *Fairchild™* [3] will be examined as an example of a VDMOS transistor and three different geometries belonging to a commercially available 500nm High Voltage MOS technology as samples of LDMOS transistors. The results provide insight into the device behavior for designers interested in incorporating them in a particular application.

1.2 Electrical characterization of power D-MOSFETs

Emphasis will be given to the electrical performance for all devices as measured through IV (current-voltage) curves, as well as basic analog design parameters such as threshold voltage, on-resistance, mobility and slope factor. In order to achieve better accuracy in our results, a statistical analysis has been made by measuring at least ten transistors of each type. Especially for the 500nm HV-LDMOS transistors, all three geometries on the packaged chip are measured and compared respectively. Finally, graphs will be presented containing statistical averages of measured data and the simulated curves produced by parameter extraction and fitting of the EPFL-HV model.

2 D-MOS device structure and operation

In the DMOS transistor the channel length is determined by the higher diffusion rate of the p-dopant compared to the n+-dopant of the source in order to yield very short channels without depending on a lithographic mask. The p-diffusion serves as channel doping and has good punch-through control. Following this, there is a lightly doped n--drift region which is long compared to the channel, and it minimizes the peak electric field in this region. The field near the drain is the same as in the drift region while the drift region can be either lateral or vertical. (see figure 2.1)

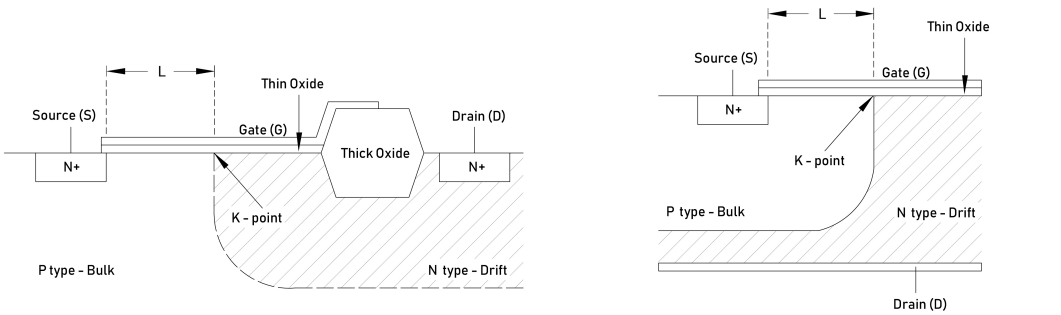
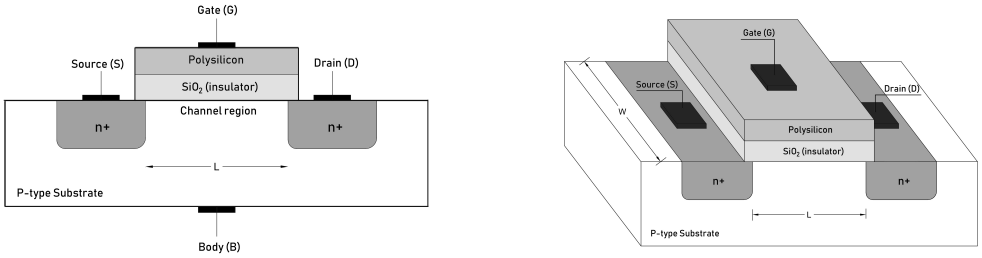


Figure 2.1: Structure of lateral DMOS (a) and vertical DMOS (b) where L is the length of the inner low-voltage MOS transistor, K point is the surface point where the doping of the device changes type.

Over the years, many models have been developed that were used to simulate and approach the behavior of a HV-MOSFET. The empirical equations used by those models to capture the physical phenomena of the drift region, has made it necessary for new physics-based models to emerge. In this thesis the EPFL-HV compact model [1] will be examined, which separates the device's operation in two parts, the low-voltage part that is modeled as a typical MOS transistor using an EKV charge-based approach [4, 5, 6] [4, 5, 6] and the high-voltage part which is covered by the drift-region model, which uses approximations to provide an analytical solution for the 2-D electrostatic field equations in the drift. The low-voltage part is located between the source and the K-point, just under the gate dielectric, at the point where the bulk doping changes polarity and becomes the lightly doped drift, while the drift region lies between the K-point and the drain. Below, the basic characteristics of those parts will be presented respectively.

2.1 Low Voltage Part

The low-voltage part can be described as an inner MOSFET and the K-point acts like the inner drain. This means that the channel is formed between the source terminal and the K-point. In this subsection, basic MOSFET operation will be analyzed and some important electrical characteristics that are presented further on in this thesis will be introduced. In figure 2.2 the typical structure of an nMOSFET is depicted. It has four terminals: S (source), G (gate), D (Drain) and B (Bulk) and the channel is formed when a positive voltage is applied to the gate.



) b)

Figure 2.2: Cross section (a) and 3-D view (b) of an n-type MOS transistor

2.1.1 Basic charge model definitions

First, the basic charge model definitions and operation will be presented. For simplicity and due to the fact that nMOSFETs are more commonly encountered, the following explanation will be for n-type devices. At the beginning, if 0V or a low voltage is applied to the gate, there is no channel formation and the transistor is in the off-state or, for low positive voltages, in the subthreshold or weak inversion region. When a sufficiently large positive bias is applied to the gate, so that a surface inversion layer is formed between the two n-wells (source and drain diffusions), they become connected by a conductive surface n-channel through which a large current can flow. This happens because holes from the body are driven away from the gate and and the channel becomes populated by electrons between the p-substrate and the insulator. The conductance of this channel can be modulated by varying the gate voltage which controls the electron density in the inversion layer. When the channel is formed and current flows, the transistor is said to be "on".

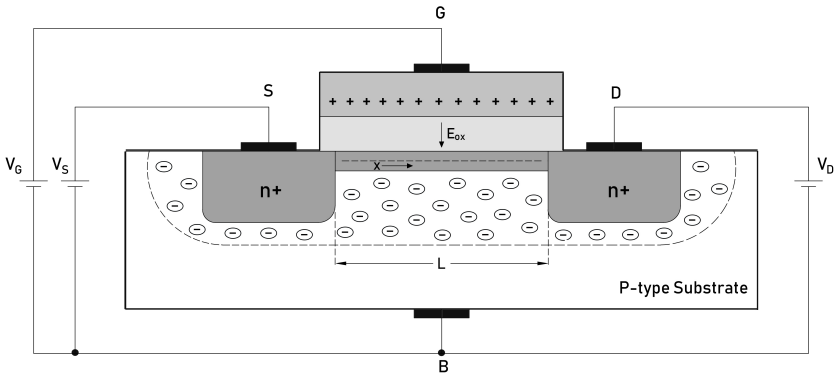


Figure 2.3: Cross section of an nMOSFET in inversion

Consequently, the transistor enters the linear region where gate to source voltage is higher than the threshold voltage and the drain to source voltage is less than the difference of gate to source voltage minus the threshold voltage. The drain current is rising linearly as the drain voltage rises and the MOSFET operates like a resistor. When the drain bias overcomes the difference described before, the drain current becomes constant and the transistor enters the saturation region. In saturation, the channel voltage at the drain end becomes lower than the threshold voltage, thus the channel there becomes "pinched-off". Electrons spread out and conduction is not through a narrow channel but through a broader current distribution extending away from the interface and deeper in the substrate. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate-source voltage. The two regions are depicted in figures 2.4 and 2.5.

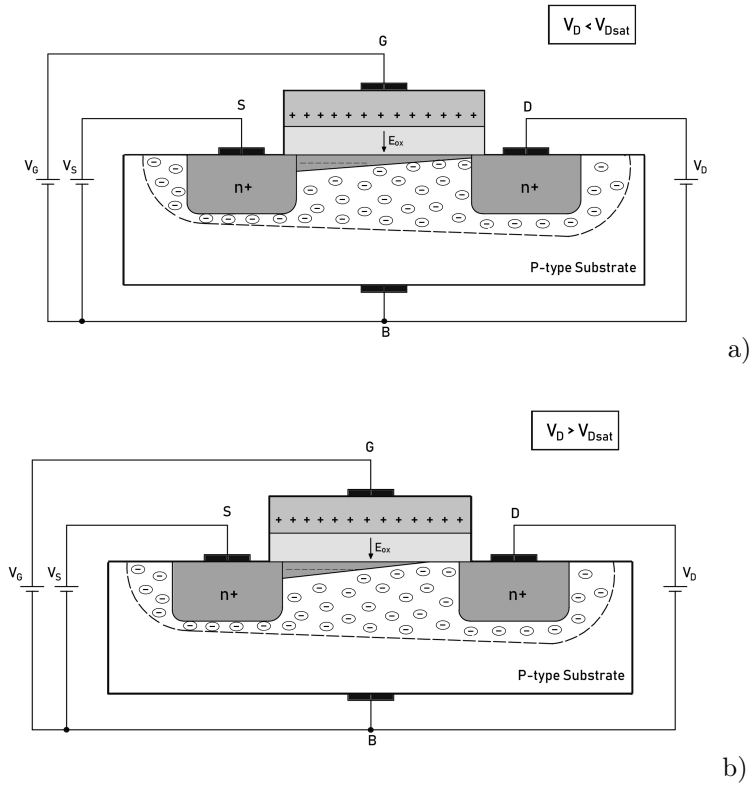


Figure 2.4: Linear region (a) and saturation region (b) of nMOS transistor where V_{Dsat}=V_g-V_{th}.

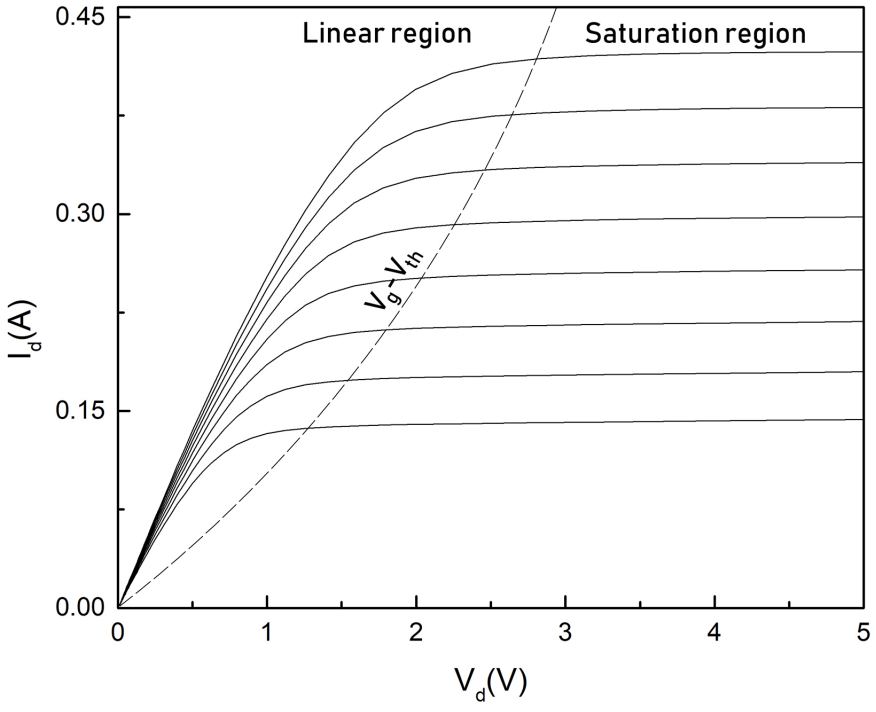


Figure 2.5: Linear and saturation region in drain current versus drain voltage diagram.

Sometimes as the channel length is reduced, there can exist a leakage current between drain and source at weak-inversion region even if the transistor should be in the off-state. This happens when the drain bias is a lot higher than threshold voltage and it causes a thin channel to form.

2.1.2 MOS transistor transconductances

Another useful characteristic is the gate transconductance (g_m). The transconductance of a transistor reflects how much current a transistor can produce with the application of voltage across its gate. It measures the sensitivity between the output current and input voltage and is calculated by the first derivative of the drain current versus gate voltage. By working in the weak-inversion region, the MOSFET delivers the highest possible transconductance-to-current ratio, namely: $\frac{g_m}{I_d}$.

Additionally, the first derivative of the drain current versus drain voltage, is called output or drain conductance (g_d). In the saturation region it is a measure of how close the transistor can get to the ideal constant current source. Below, the use of g_{ds} in the linear region for the extraction of the transistor on-resistance will be explained.

2.1.3 Threshold voltage

The threshold voltage (V_{th}) is the voltage between gate and source, able to cause surface inversion under the gate, close to the source terminal. Once inversion has taken place, charge carriers from the source can enter the surface region (channel region) between the source and drain and they are ready to conduct current between the two if there is a voltage difference between them. Threshold voltage can be determined either for linear or saturation region and one of the most easily applicable methods for its determination is the "constant current method" [7]. A sufficiently low threshold current (I_{th}) value (tens to hundreds of nA) is chosen, it is then scaled according to the device dimensions (multiplied by $\frac{W}{L}$) and the voltage that corresponds to the resulting current is interpolated from the measurements. This method is used in this thesis in order to extract the V_{th}, at an I_{th} equal to $100\frac{W}{L}$nA as shown in figure 2.6.

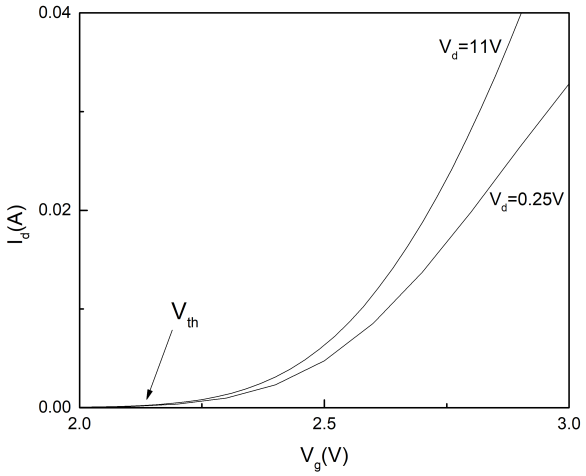


Figure 2.6: Drain current to gate voltage diagram and the threshold voltage at saturation (V_d=11V) and linear region (V_d=0.25V).

2.1.4 Sub-threshold Slope factor

In the log(I_D) vs V_G diagram, at a constant drain bias voltage, for the weak inversion region the curve is expected to appear linear, as the subthreshold current has an exponential relationship with gate voltage ($I_D \propto \exp[\frac{V_G - n \cdot V_S}{n \cdot U_T}]$). The slope of this line is the subthreshold slope (n). For

digital or switching applications it can be seen as a source of device leakage (drain current in the off-state) and is considered a figure of merit for the quality of a device. In analog design however, whole designs can be based in this operation region as it can give the best transconductance and lowest power consumption. A steeper slope (lower n, closer to unity) means the device gets out of the subthreshold region faster and is considered a good characteristic. The way to extract the slope factor, as has also been applied here, is through the normalized transconductance efficiency $\frac{g_m U_t}{I_D}$ versus I_d diagram, where the plateau value reached in weak inversion, equals the inverse of the slope factor.

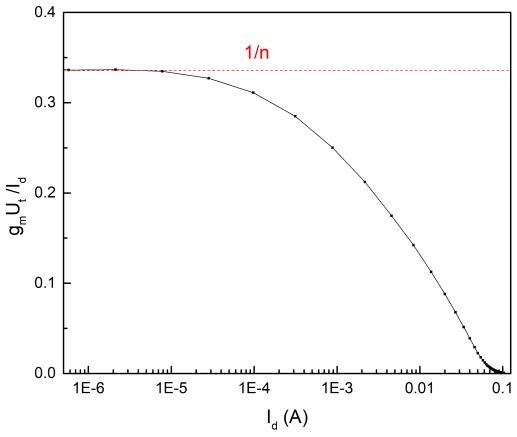


Figure 2.7: Subthreshold Slope Factor extraction from $\frac{g_m U_t}{I_d}$ versus I_d diagram (n=slope factor).

2.1.5 On resistance

The resistance across drain and source when the MOSFET is in the "on" state is called on resistance (R_{DSon} or R_{on}) and is one of the most prominent specifications on datasheets for discrete power MOSFETs. It is most meaningful when extracted for the transistor operating in the linear region ($V_g > V_{th}$ and $V_D < V_G - V_{th}$ with the assumption of a constant operating temperature), as this is the area of interest in switching applications, where a lower R_{on} will guarantee lower heat dissipation and longer device service life. Lower on-resistance is also better because the transistor has a lower voltage drop which translates to more voltage available for the load being switched. The extraction method applied in this thesis was the calculation of the mean value of the drain-source resistance (R_{ds}) of the transistors in the linear regime, which in turn was calculated from the inverse of the output (or drain) transconductance, g_{ds} at appropriate V_D and V_G values.

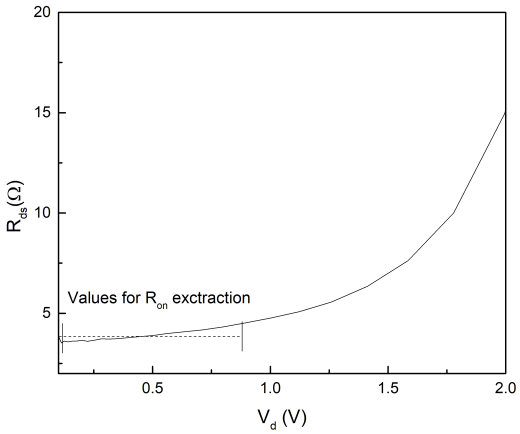


Figure 2.8: R_{ds} versus $V_D$diagram scaled at linear region where the mean of the almost constant R_{ds} values equals to R_{on}.

2.1.6 Mobility

The carrier mobility describes how quickly a charge carrier can move through a metal or semiconductor when accelerated by an electric field. In this thesis, the mobility of the electrons moving through the channel layer under a very low drain voltage is extracted, which is called low-field surface mobility (μ_0) and its unit is $\frac{cm^2}{(Vs)}$ (SI $\frac{m^2}{(Vs)}$). The method to extract μ_0 is based on the combined exploitation of the I_d-$V_g$and g_m-$V_g$characteristics, and attempts to avoid the effects of mobility reduction with gate voltage on the determination both of the threshold voltage and of the low field mobility parameter. This method concludes in the equation $\frac{I_d}{g_m^{1/2}} = (\frac{W}{L}\mu_0 C_{ox} V_d)^{1/2}(V_g - V_t)$ where the quantity $\frac{I_d}{g_m^{1/2}}$ in strong inversion should be linear in gate voltage with the intercept and slope giving the charge threshold voltage V_{th}, and the low field mobility parameter μ_0 (assuming W, L and C_{ox} are known) respectively. [8] The extraction of mobility is now possible through $\frac{I_d}{g_m^{1/2}}$ versus $V_g$diagram as shown in figure 2.9.

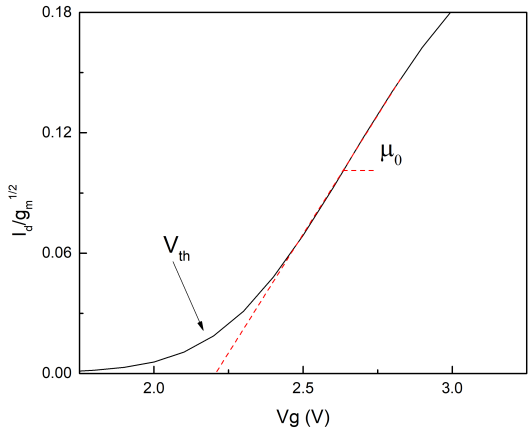


Figure 2.9: $\frac{I_d}{g_m^{1/2}}$ versus V_g diagram and the slope that equals the low field mobility parameter μ_0

2.2 High-Voltage Part

2.2.1 Drift Region

The second element of the EPFL-HV compact model is the high-voltage part or the drift region. Drift region is the area from the K point to the drain terminal which has the same doping type as the source and drain, albeit at a lower concentration. In order to study this region, a physics-based approach has been developed [1], according to which this part is treated separately from the low voltage part as a single dimensional problem. However the drift region can not be measured as a single unit and this model must be integrated into a wider macromodel that will cover both parts of the HV-MOS device. For example, the nonuniform doping across the channel has a crucial impact on the whole behavior of the HV-MOSFET and there are also higher order effects such as a self heating effect and quasi-saturation that have to be considered to simulate the behavior of HV-MOS devices. These effects will be discussed in Chapter 3.

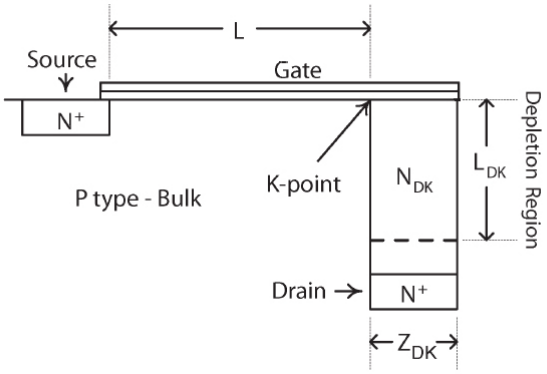


Figure 2.10: Simplified structure of an HV-MOSFET

2.3 Two types of D-MOS

As stated before, there are different types of D-MOS transistors based on the relative position of the drift region and the drain terminal. Below, lateral and vertical power D-MOS transistors will be described, in accordance with the devices that have been measured experimentally.

2.3.1 Lateral D-MOS structure

The lateral diffused MOSFET (LDMOS) is an asymmetric power MOSFET designed for low on-resistance and high blocking voltage. Its main difference from VDMOS transistor structure is that the drain terminal is in the same plane as the source terminal, which implies that the drift region is the lateral extension of the low-voltage channel (figure 2.11).

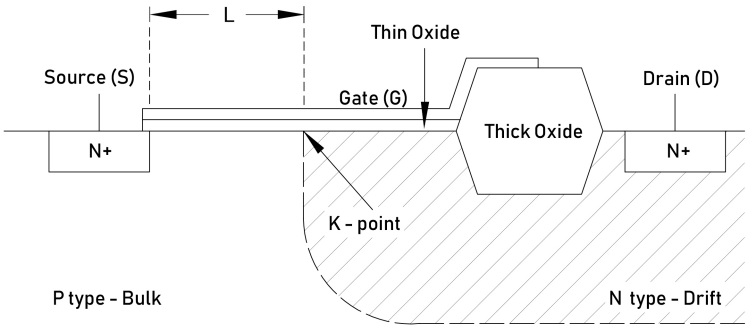


Figure 2.11: Structure of lateral D-MOS

2.3.2 Vertical D-MOS structure

On the other hand, vertical diffused MOSFET (VDMOS) differ from LDMOS in the drift region. The drain terminal is in a vertical position compared to the source, and as a consequence there is an angle between drift region and low-voltage channel. The current flow is not planar anymore but instead it follows a two-dimensional route. (see figure 2.12)

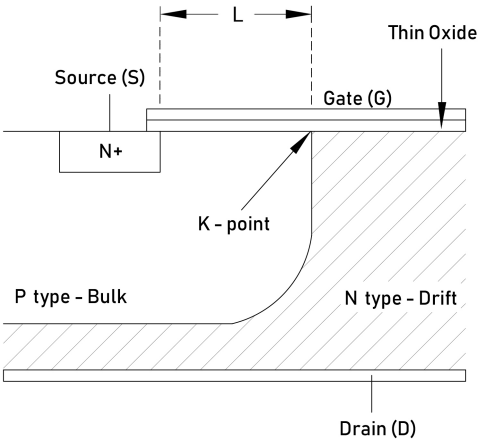


Figure 2.12: Structure of vertical D-MOS

3 EPFL HV-MOSFET compact model

3.1 Model description

The EPFL high voltage MOSFET model is a compact model designed to simulate the operation of both lateral and vertical DMOS devices. It follows the methodology that has been described in chapter 2, where the two models (low voltage part, drift region part) are analyzed individually and are then combined in one 2-d compact model. Below, some higher order effects and some key equations are presented.

3.1.1 Model equations

Model equations are divided into graded levels, starting from quantities that do not depend on device geometry, temperature and voltage and concluding to quantities that are more complex. Moreover, the model gives the ability to choose between using physical or electrical parameters such as the mobility in low voltage part and the drift region (U0, U0DR vs KP, KPDR) and the velocity saturation in low voltage part and the drift region (VSAT,VSATDR vs UCRIT, UCDR).

Model Level

Model level is the lower level where variables are calculated according to the model parameter TNOM (nominal temperature). The thermodynamic voltage and the intrinsic concentration are calculated after the following equations:

$$U_{T_{nom}} = \frac{k \cdot T_{nom}}{q}$$
$$n_{i.nom} = 3.87 \cdot 10^{22} \cdot T_{nom}^{3/2} \cdot e^{-7000/T_{nom}}$$

where k is the Boltzmann constant and q is the elementary charge.

Geometry dependence

Equations in this level, calculate the effective dimensions after the nominal dimensions as the length and the width and the corresponding parameters. For example:

$$L_{eff} = L + \Delta L$$

where ΔL is the length offset of gate oxide region.

Another important equation that calculates the drain current in all the modes of operation of the transistor is:

$$I_d = \beta \int_{V_s}^{\infty} \frac{-Q_i}{C_{ox}} dV - \beta \int_{V_d}^{\infty} \frac{-Q_i}{C_{ox}} dV$$

where Q_i is the inverted charge density and β is the transfer parameter given by:

$$\beta = \mu C_{ox} \frac{W}{L}$$

3.1.2 High order effects

Higher order effects are electrical or physical phenomena that occur while the device operates and could, for older technologies or for more simplistic models, be considered negligible. Ideally, if those effects didn't exist, the transistor would operate according to the long channel mathematical equations and it would be easy to understand. Of course, this is unrealistic and this is why all models (this one included) are surrounded by a series of extensions in order to describe some higher order effects. Some of the effects that were encountered, are explained below.

Vertical field mobility effect

There is a dependence of the mobility of the vertical field because the inverse charge is not homogeneous in the channel. The mobility is reduced due to the existence of the surface scattering effect which happens when the electric field of the gate attracts carriers towards the oxide-semiconductor interface. The parameters related to this effect are E0 (first order coefficient for mobility reduction due to vertical field), E1(second order coefficient for mobility reduction due to vertical field) and ETA (mobility reduction due to vertical field factor).

Velocity saturation effect

The linear relationship between the longitudinal field and the velocity of the carriers is preserved only for low intense filed and for greater values the velocity will tend to the maximum value. This is happening because the carriers can obtain a maximum of velocity while the longitudinal field keeps rising due to the gate charge. The parameters related to this effect are VSAT (saturation velocity) and UCRIT (longitudinal critical field).

Channel Length Modulation

The channel may be divided into two parts, one with velocity saturation and one linear whose length must be calculated. This is called channel modulation and the parameters related to this are LAMBDA (Lambda factor) and LC (characteristic length for channel length modulation)

Drain Induced Barrier Lowering

The voltages at the gate and source at the ends of the channel also influence the surface potential throughout the channel. Usually the drain bias is higher than voltage at the source which results in a decrease in the threshold voltage when the voltage at the drain increases. This is called DIBL effect (Drain Induced Barrier Lowering) and the parameters related to this effect are ETAS (subthreshold barrier lowering characteristic length coefficient), SIGMAS (subthreshold barrier lowering body bias coefficient), ALPHAS (subthreshold barrier lowering smoothing coefficient) and BETAS(subthreshold barrier lowering scaling factor).

4 Lateral n-type HV-MOSFET analysis

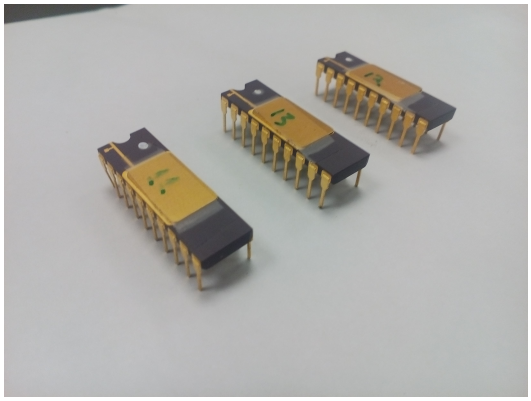


Figure 4.1: Packages of three isolated high voltage n-channel transistors

In this section, measurements on the 500nm isolated high voltage n-channel transistors are being presented. The package tested, as illustrated on figure 4.1, has three inner lateral DMOS transistors with different geometries. The smallest transistor has a width of 10µm and length of 0,5µm, the intermediate one has a width of 40µm with the same short length and the largest has a width of 40µm and length of 10µm. The gate and the source terminals of the three transistors are connected together respectively. They are all fabricated in a common p-well. The connections between transistor's terminals, the common bulk and the package's pins are shown in the two diagrams beneath(figure 4.2 and figure 4.3).

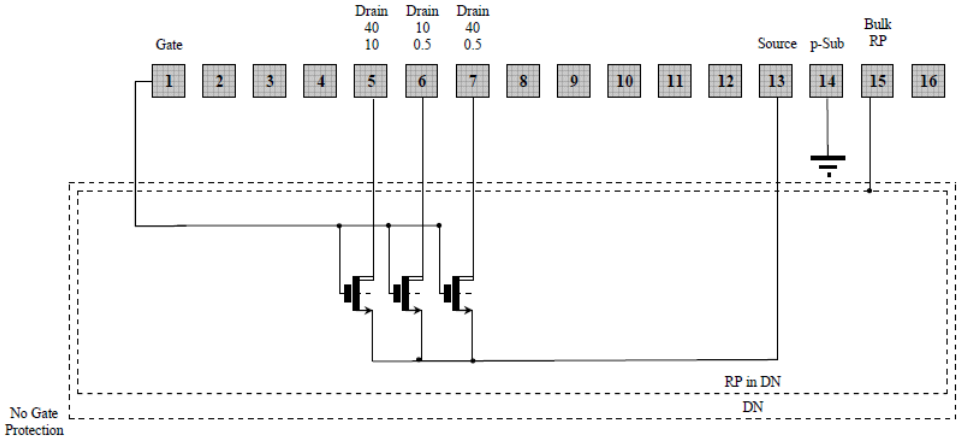


Figure 4.2: Inner package connection scheme

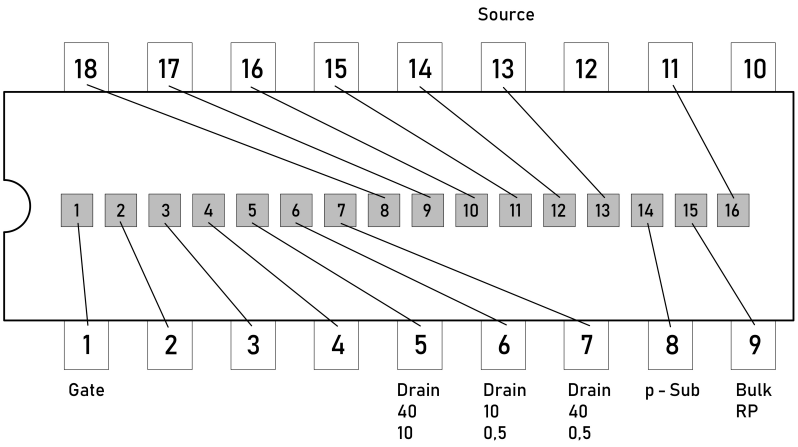


Figure 4.3: Outer package - pin connection

The measurements were carried out on 10 packages, each of which consists of the three geometries listed above. Every package has been placed on a *HP Agilent 16058A test fixture kit* with a *dual in line package (18pin)* socket. That unit was connected to a HP4145A *semiconductor parameter analyzer* which applied to the *HP16058A* voltage and current at the gate, bulk, source and drain, while measuring the resulting drain current. The HP4145A was also connected to a computer with a *GPIB-USB Interface* where the desired values for voltage and current were chosen and the results were extracted though the software *ICCAP by Agilent*. Further statistical analysis of all the acquired data was implemented on *OriginPro of OriginLab*.

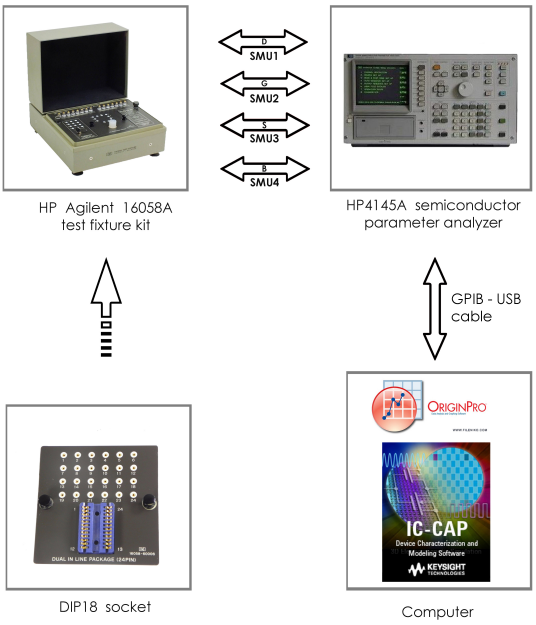


Figure 4.4: Block diagram with cable connections

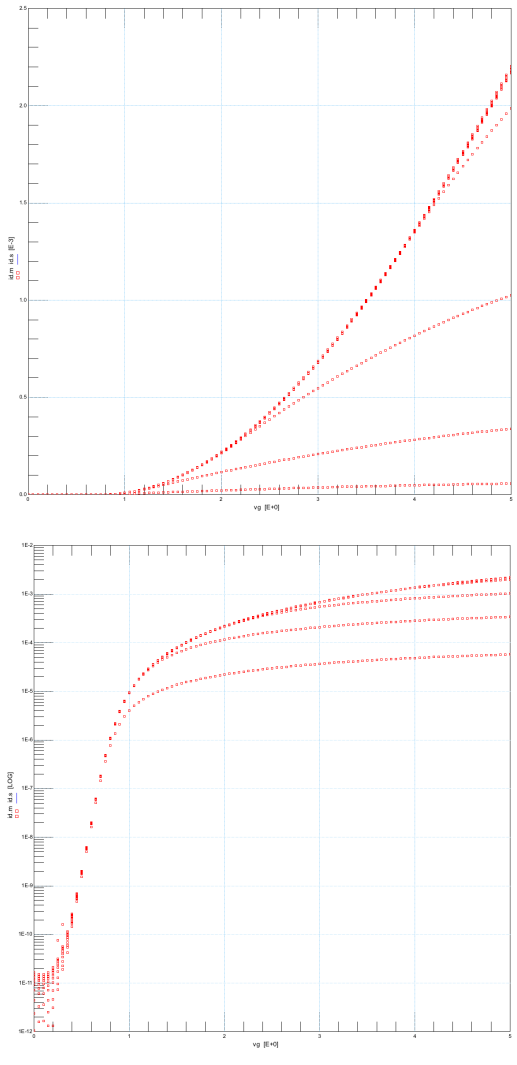
The experimental procedure for each device consisted of I-V measurements for transfer and output characteristic curves. The voltage values for the gate (0-5 V) cover weak and strong inversion and the voltage values for drain (0-20 V) cover both linear and saturation region. Afterwards, the I-V measurements were analyzed to export basic device operation and design parameters, specifically threshold voltage, slope factor and mobility (exported from I_dV_g, g_m) and on resistance (exported from I_dV_d, g_{ds}).

4.1 Statistical analysis of W=40µm, L=10µm transistor

Firstly, the measurements of the large high voltage mosfet geometry with a width of 40µm and length of 10µm will be presented. The calculated values of $V_{th,linear}$,$V_{th,saturation}$, slope factor, R_{on} and $\mu_0$are extracted for each transistor individually and plotted along their mean value. The standard deviation (σ) was also calculated for the sample, and dotted lines are plotted representing a $\pm 2\sigma$ spread

4.1.1 I-V curves

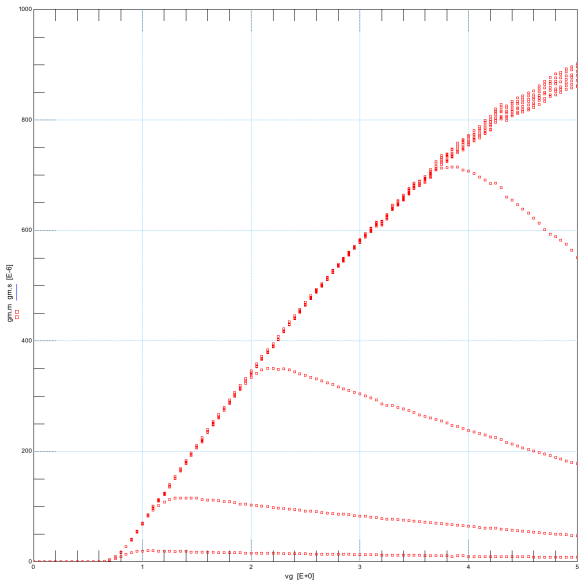
In the following I-V curves, the I_d represents the mean value of the drain current, on a number of 10 HV-MOSFETs. According to this, g_m, g_{ds} and g_mU_t/I_d are also calculated by the average values that are extracted from measurements.



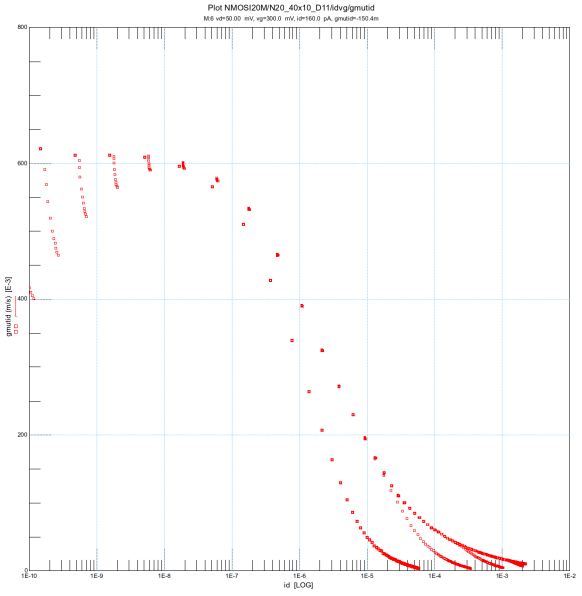
a)

b)

Figure 4.5: Measured Value of I_d vs V_g(a) and log(I_d) vs V_g(b) for 10 HV-MOSFETs with W/L=40µm/10µm from weak to strong inversion (V_g=0-5V) and for multiple V_d (V_d=0.05-20V)



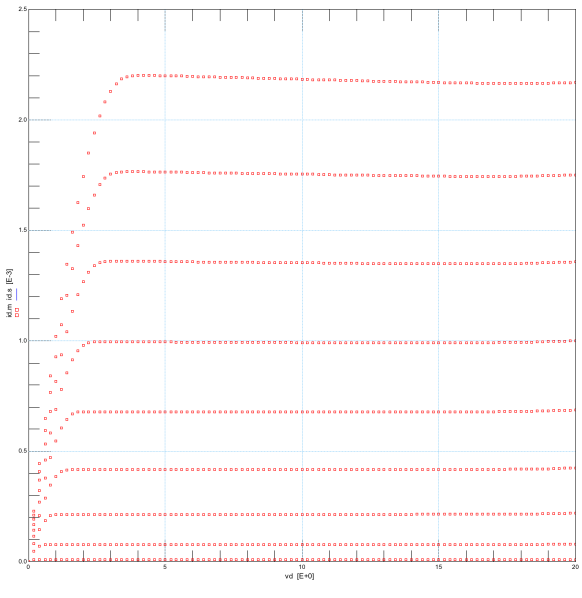
a)



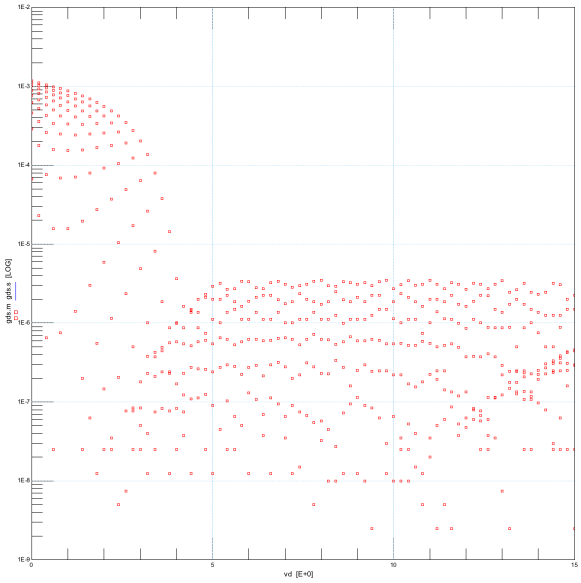
b)

Figure 4.6: Measured transconductance $g_m$vs V_g(a) and $g_m U_t/I_d$ vs I_d(log axis)(b) for 10 HV-MOSFETs with W/L=40µm/10µm

Figure 4.5 presents the average current value versus voltage gate for several drain voltages and is used to extract the threshold voltage at low drain voltage (linear region) and at high drain voltage (saturation region). As expected, transistor operates in both weak and strong inversion for all drain voltages. At last $g_m U_t/I_d$ vs I_d diagram used to extract the slope factor of the device.



a)



b)

Figure 4.7: Measured I_d vs V_d(a) and g_{ds} vs V_g(b) for 10 HV-MOSFETs with W/L=40µm/10µm from linear to saturation (V_d=0-20V) and for multiple V_g(V_g=1-5V)

In the last figure where I_d-V_d measurements are shown, the self heating effect can be observed for the two higher gate voltages. Output conductance is also presented in (b) but there is clear distinction between the measurements only in the linear region.

4.1.2 Threshold Voltage

The threshold voltage of each device was calculated twice, in linear and in saturation region respectively.

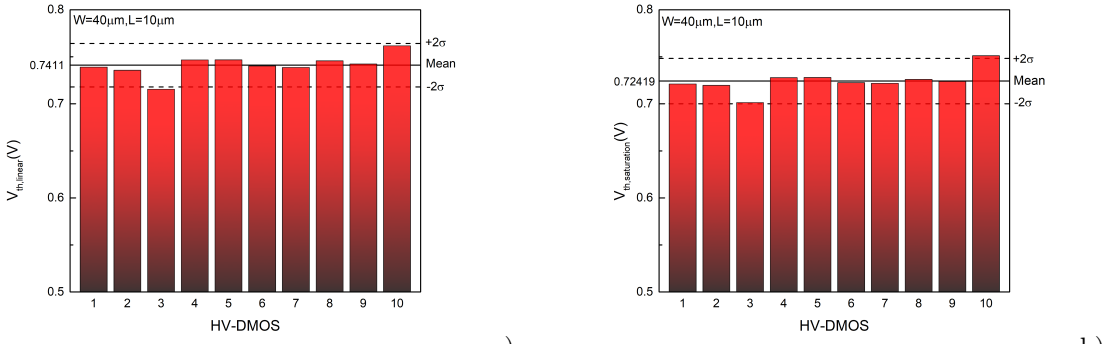


Figure 4.8: Threshold voltage in linear (a) and in saturation (b) and the average values E($V_{th,linear}$) =741.13mV, E($V_{th,saturation}$)=724.19mV for W/L=40µm/10µm

The mean value of the threshold voltage in the linear region (E($V_{th,linear}$)=741.13mV) is higher than the threshold voltage in saturation (E($V_{th,saturation}$)=724.19mV) because higher voltage at the drain makes the transistor turn on faster, thus lowering its effective V_{th} in the saturation region, an effect mainly observed in shorter channel transistors known as "Drain Induced Barrier Lowering" (DIBL), where not only the gate but also the drain electrode plays a major role in channel formation.

4.1.3 Slope Factor

Slope factor is extracted as mentioned before from the $\frac{g_m U_t}{I_d}$ versus I_d diagram. The mean value of the measured transistors is E(n)=1.654.

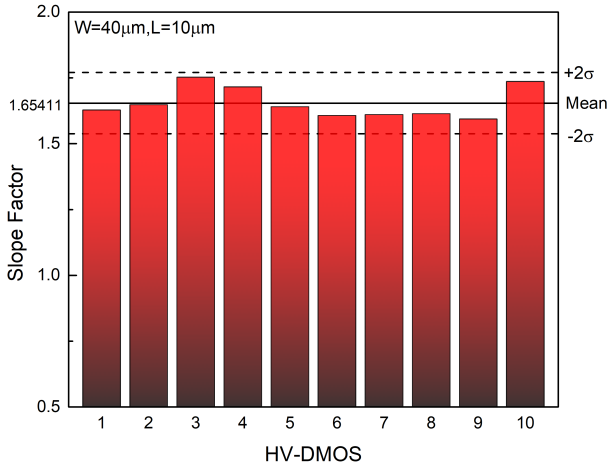


Figure 4.9: Slope factor and the average value E(n)=1.654 for W/L=40µm/10µm

4.1.4 Mobility

As described in Chapter 2 mobility is extracted from $\frac{I_d}{g_m^{1/2}}$ versus V_g diagram. The average value of the transistors mobility is E(μ_0)=390.87 cm^2/Vs.

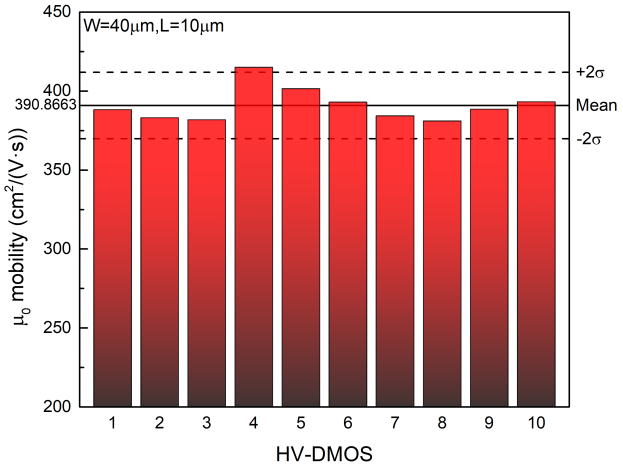


Figure 4.10: Mobility (μ_0) and the average value E(μ_0)=390.87 cm^2/Vs for W/L=40µm/10µm

4.1.5 On Resistance

On resistance is extracted from g_{ds}curve and the mean value is $E(R_s) = 1207.67\Omega$.

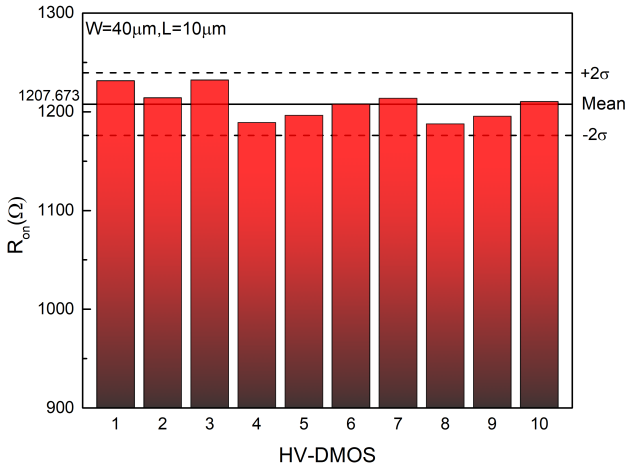


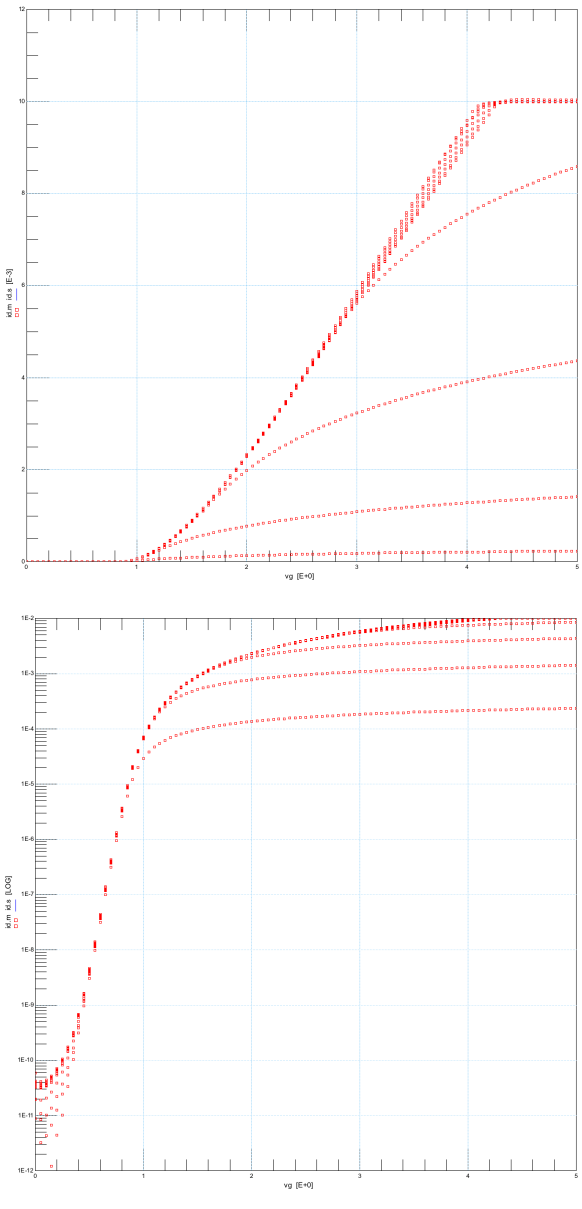
Figure 4.11: On resistance and the average value $E(R_s) = 1207.67\Omega for W/L = 40m/10m$

4.2 Statistical analysis of W=40µm, L=0.5µm transistor

Beneath, the measurements of the second transistor are presented. It has the same width with the first (40µm) but its length is shorter. (0.5µm)

4.2.1 I-V curves

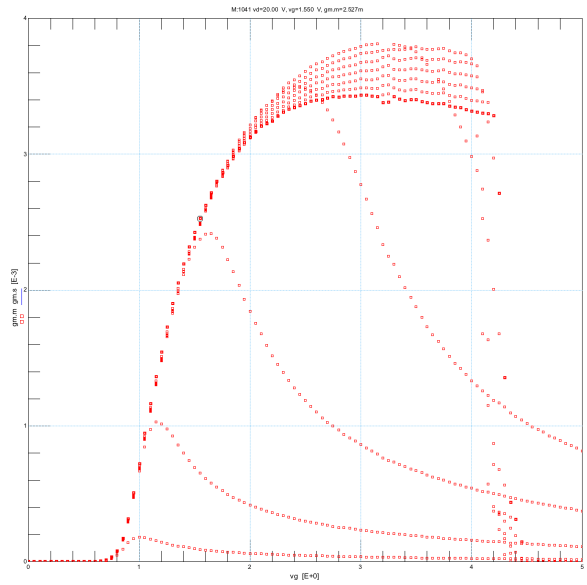
The current-voltage graphs have been measured at the same values for voltage at drain and gate as for the first transistor. Transconductances g_m and $g_{ds}$are calculated and plotted also. The figures show the mean value of 10 devices.



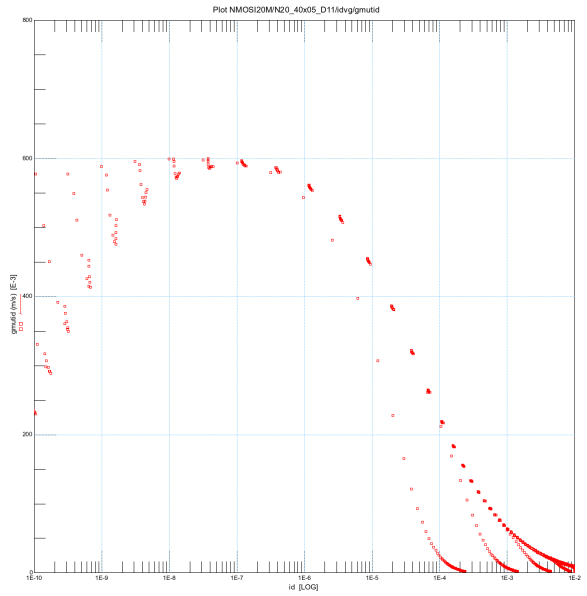
a)

b)

Figure 4.12: Measured Value of I_d vs V_g(a) and log(I_d) vs V_g(b) for 10 HV-MOSFETs with W/L=40µm/0.5µm from weak to strong inversion (V_g=0-5V) and for multiple V_d (V_d=0.05-20V)

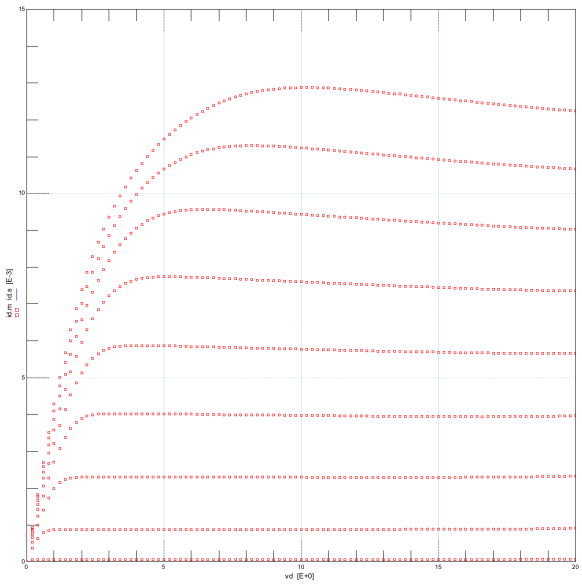


a)

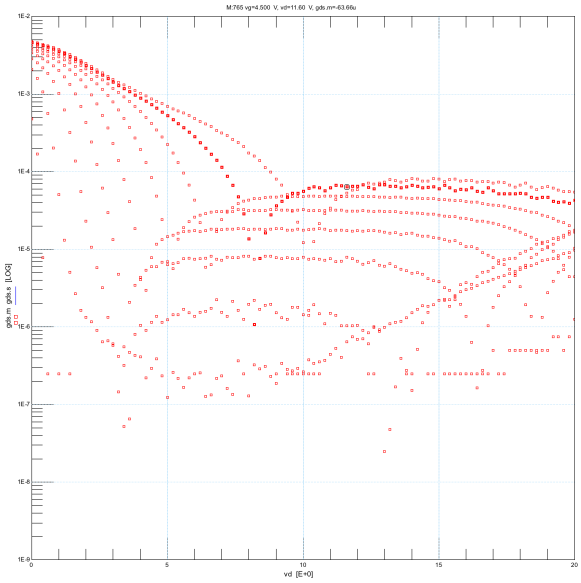


b)

Figure 4.13: Measured Value of transconductance $g_m$vs V_g(a) and $g_m U_t/I_d$ vs I_d(log axis)(b) for 10 HV-MOSFETs with W/L=40µm/0.5µm



a)



b)

Figure 4.14: Measured Value of I_d vs V_d(a) and g_{ds} vs V_g(b) for 10 HV-MOSFETs with W/L= 40µm/0.5µm from linear to saturation (V_d=0-20V) and for multiple V_g(V_g=1-5V)

As with the first transistor, the self heating effect can be noticed at I_d vs $V_d$curve for the values of V_g=3, 3.5, 4, 4.5, 5V. As the gate voltage increases it becomes more intense. Additionally, at figure 4.12 (a), drain current reaches the SMU compliance limit of 10 mA, when drain voltage is higher than 5 V and gate voltage is higher than 4V.

4.2.2 Threshold Voltage

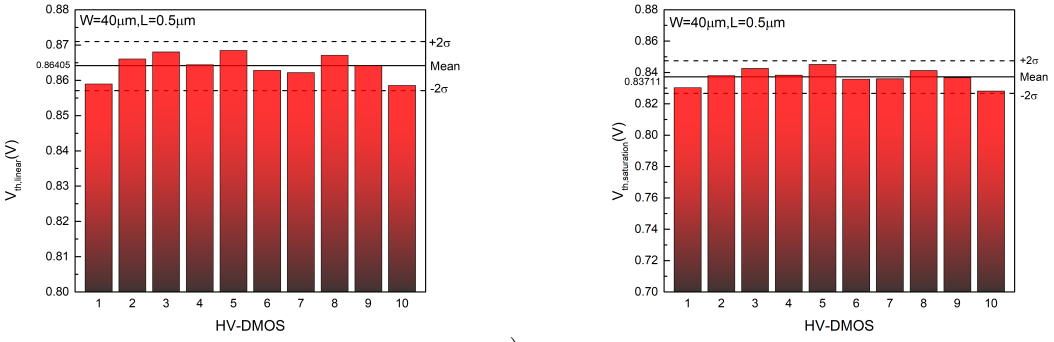


Figure 4.15: Threshold voltage in linear (a) and in saturation (b) and the average values E($V_{th,linear}$) =864.05mV, E($V_{th,saturation}$)=837.11mV for W/L=40µm/0.5µm

As with the first geometry, the linear threshold voltage is higher than the saturation threshold voltage. The value is higher because channel length is shorter and their relevance is reversed. The mean values are E($V_{th,linear}$)=864.05mV, E($V_{th,saturation}$)=837.11mV.

4.2.3 Slope Factor

Slope factor mean value is almost equal to the first geometry. (E(n)=1.675)

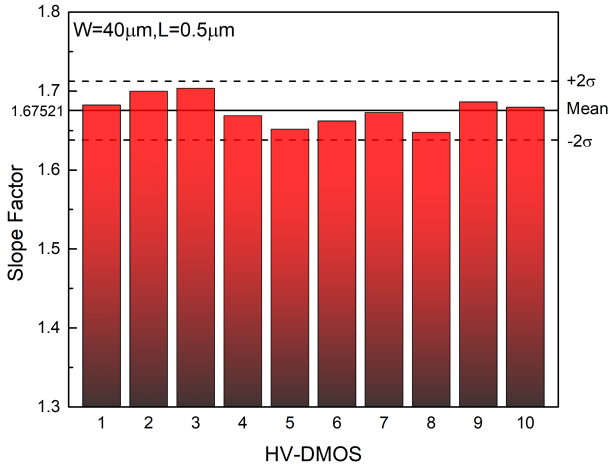


Figure 4.16: Slope factor and the average value E(n)=1.675 for W/L=40µm/0.5µm

4.2.4 Mobility

As shown in figure 4.17, two transistor measurements have a relatively big difference, nevertheless they are inside the limits of $\mp 2\sigma$. Mean value equals E(μ_0)=154.16 cm^2/Vs

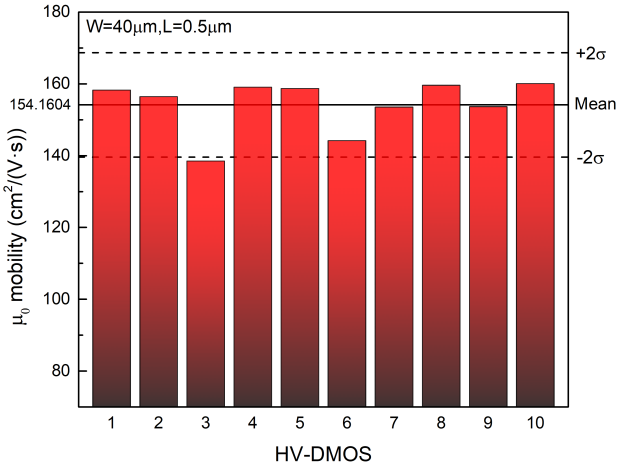


Figure 4.17: Mobility (μ_0) and the average value E(μ_0)=154.16 cm^2/Vs for W/L=40µm/0.5µm

4.2.5 On Resistance

On resistance measurements of the W/L=40µm/0.5µm geometry have a relatively high spread. Mean value is also the lowest of all three geometries, which is to be expected as this is the shortest and widest of all available geometries. (E(R_s) = 283.6372Ω).

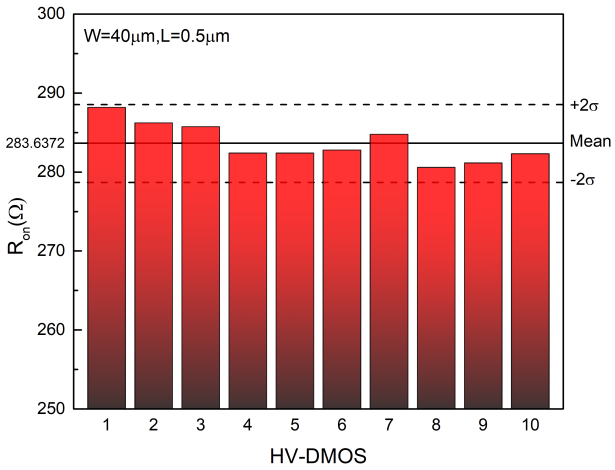


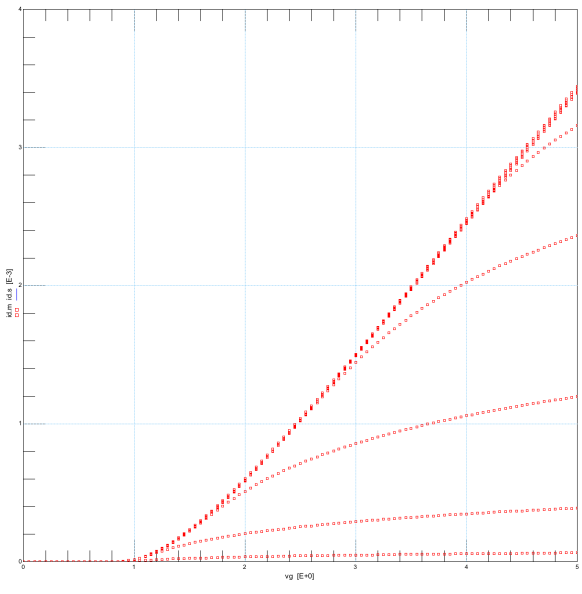
Figure 4.18: On resistance and the average value $E(R_s) = 283.6372\Omega for W/L = 40m/0.5m$

4.3 Statistical analysis of W=10µm, L=0.5µm transistor

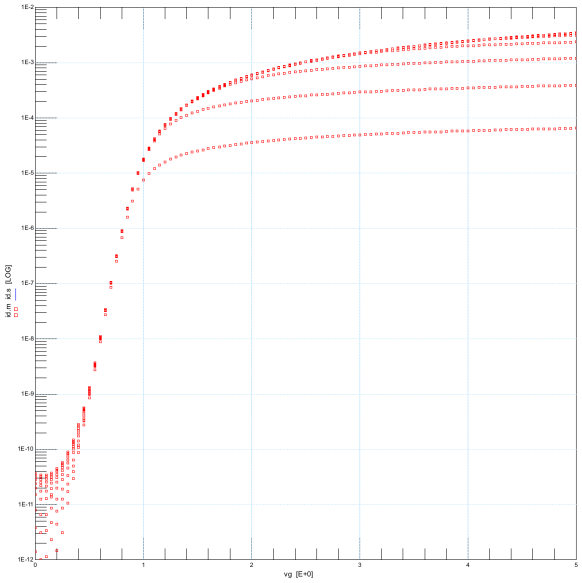
Lastly, the measurements of the third transistor are presented. It has the narrowest width (10µm) and the same length as the previous transistor(0.5µm).

4.3.1 I-V curves

Again the average values for the 10 devices are calculated and plotted in current-voltage graphs. Transconductances (g_{ds},g_m) are also shown in fig 4.20 and fig 4.21.

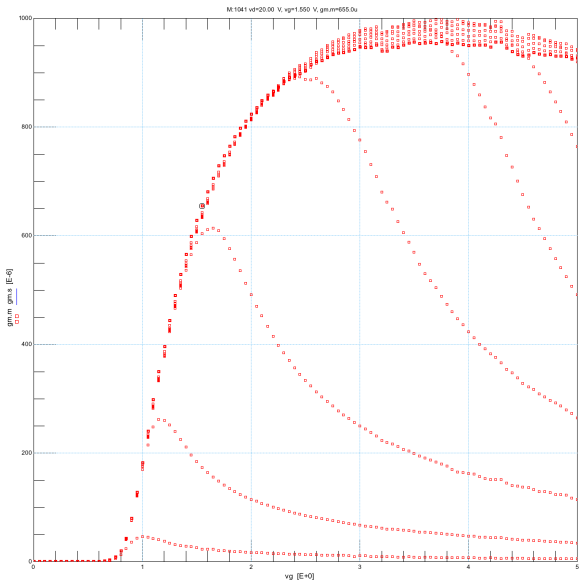


a)

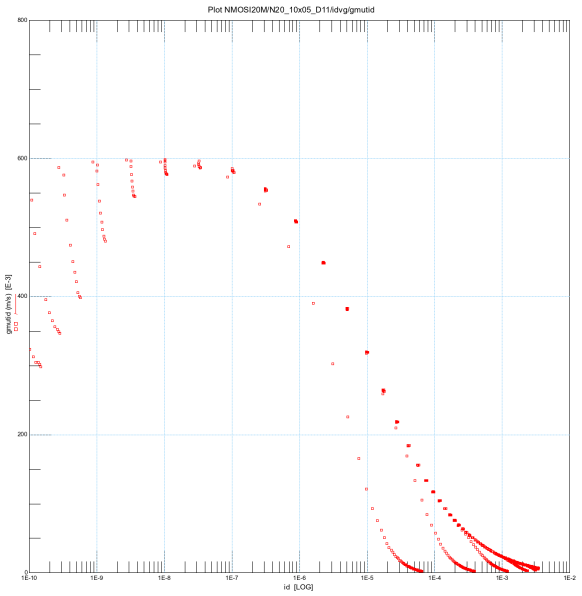


b)

Figure 4.19: Measured Value of I_d vs V_g(a) and log(I_d) vs V_g(b) for 10 HV-MOSFETs with W/L=10µm/0.5µm from weak to strong inversion (V_g=0-5V) and for multiple V_d (V_d=0.05-20V)

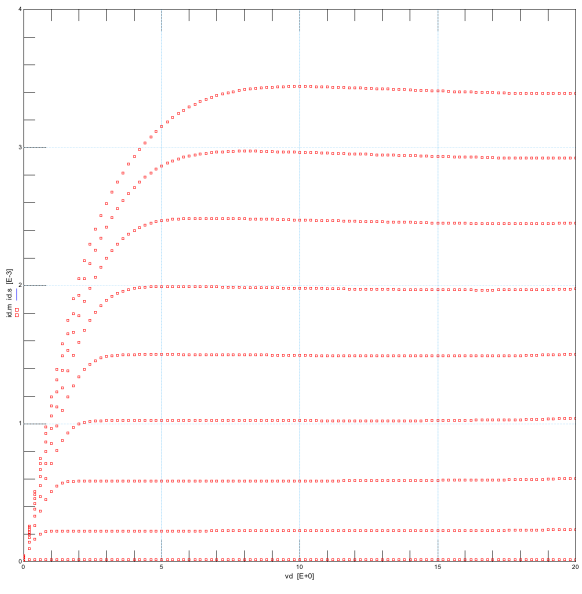


a)

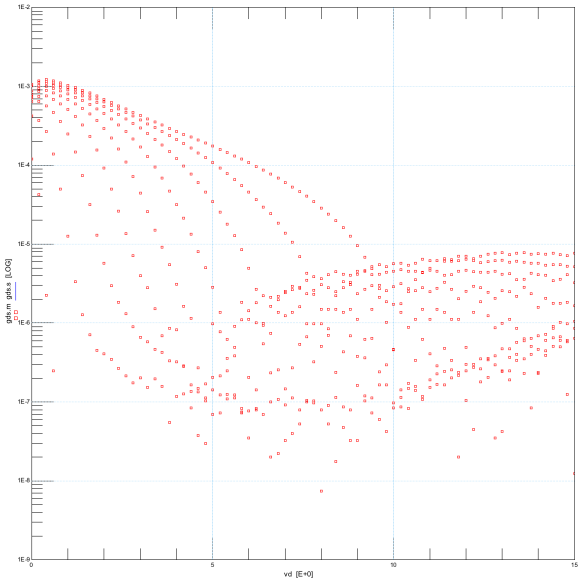


b)

Figure 4.20: Measured Value of $g_m$vs V_g(a) and $g_m U_t/I_d$ vs I_d(log axis)(b) for 10 HV-MOSFETs with W/L=10µm/0.5µm



a)



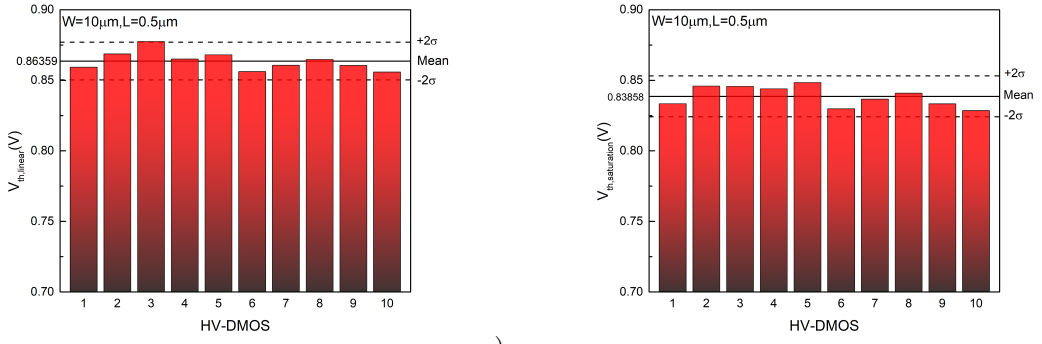
b)

Figure 4.21: Measured Value of I_d vs V_d(a) and g_{ds} vs V_g(b) for 10 HV-MOSFETs with W/L= 10µm/0.5µm from linear to saturation (V_d=0-20V) and for multiple V_g(V_g=1-5V)

Again the self heating effect is obvious at I_d vs $V_d$for drain voltage of 4V and more.

4.3.2 Threshold Voltage

As expected the threshold average voltages are very close to the values of the second geometry because both geometries have the same length. (E($V_{th,linear}$)=863.59mV, E($V_{th,saturation}$)=838.58mV)



a) b)

Figure 4.22: Threshold voltage in linear (a) and in saturation (b) and the average values $E(V_{th,linear})$ =863.59mV, $E(V_{th,saturation})$=838.58mV for W/L=10µm/0.5µm

4.3.3 Slope Factor

Slope factor mean value is practically the same for all the three geometries. (E(n)=1.685)

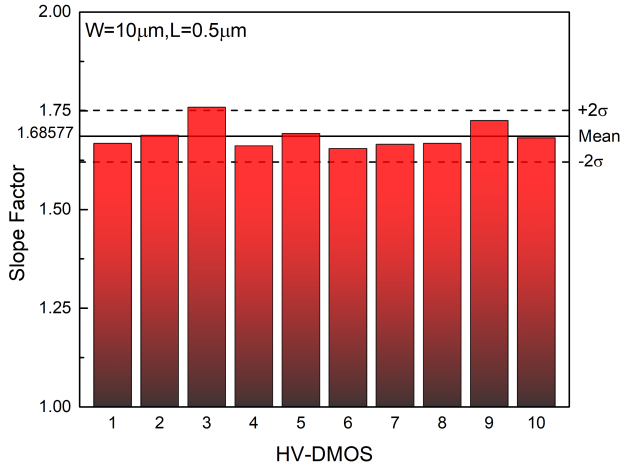


Figure 4.23: Slope factor and the average value E(n)=1.685 for W/L=10µm/0.5µm

4.3.4 Mobility

Mobility for W/L=10µm/0.5µm geometry is very close to the previous geometry (W/L=40µm/0.5µm) as both geometries represent short channel transistors. The mean value is $E(\mu_0)$=151.25 cm^2/Vs.

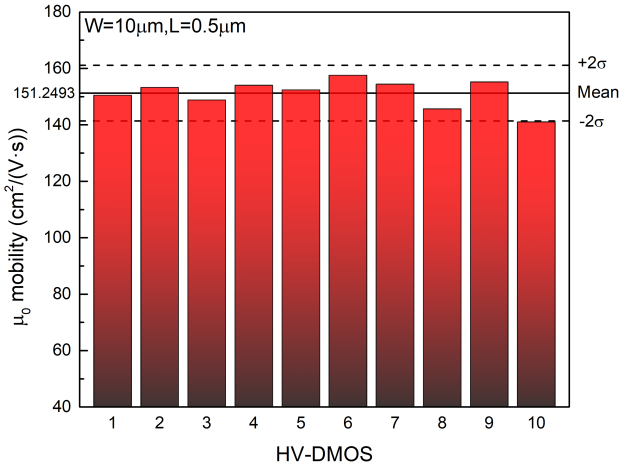


Figure 4.24: Mobility (μ_0) and the average value E(μ_0)=151.25 cm^2/Vs for W/L=10µm/0.5µm

4.3.5 On Resistance

Finally, the on resistance for the smallest devices has mean value of $E(R_{on}) = 1023.49\Omega$.

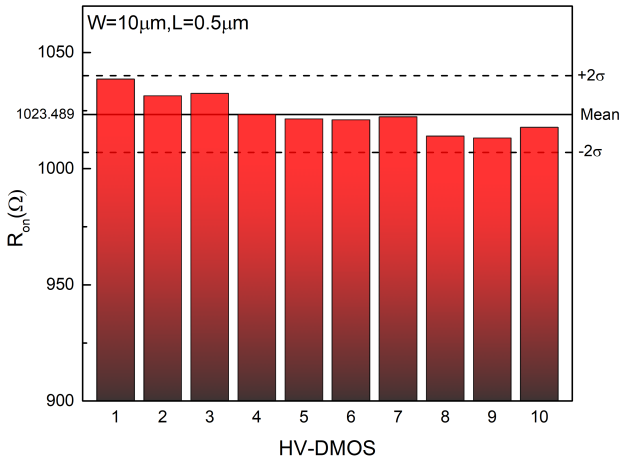


Figure 4.25: On resistance and the average value $E(R_{on}) = 1023.49\Omega for W/L = 10m/0.5m$

4.4 Overall high voltage LDMOS extracted measurements

	W/L=40µm/10µm	W/L=40µm/0.5µm	W/L=10µm/0.5µm
$V_{th,linear}$(mV)	741.13	864.05	863.59
$V_{th,saturation}$ (mV)	724.19	837.11	838.58
Slope Factor	1.654	1.675	1.685
Mobility (cm^2/Vs)	390.87	154.16	151.25
On Resistance (Ω)	1207.67	283.64	1023.49

Table 4.1: Aggregate of mean values for all geometries.

The extracted parameters for all geometries of the high voltage LDMOS transistors (nLDMOS=10) are as expected. Threshold voltage at W/L=40µm/0.5µm and W/L=10µm/0.5µm geometries is higher than for W/L=40µm/10µm because their channel is shorter and it is almost the same for the two devices of equal length. Mobility is also very close for the two smaller geometries because the W/L=40µm/0.5µm transistor and the W/L=10µm/0.5µm both operate as short channel tranistors. Finally, on-resistance of the smallest transistor is almost 4 times more than the W/L=40µm/0.5µm transistor which makes sense as they share the same length but the width of the smallest transistor is four times smaller.

5 Vertical n-type DMOSFET (BS170)

In this Chapter n-type power VDMOS transistors are being discussed. First, current-voltage diagrams will be presented with the addition of extracted characteristic parameters and afterwards the simulation procedure along with the fitting model parameters will be explained.

5.1 Statistical Analysis of the transistor

This section consists is centered around the statistical analysis of thirteen BS170 transistors. A dedicated heatsinked socket has been constructed for the purpose of this work. BNC connectors were used in order to connect the test socket with the DC analyzer (HP 4142B) through TRIAX to BNC adaptors and shielded cables, while a turned-pin socket was used to ensure adequately low contact resistance with the device under test (DUT). Heatsink compound was applied on every DUT prior to inserting in the socket and a metal spring-clip was used to exert enough pressure for good heat-transfer while still allowing for easy swapping of DUTs. For the drain voltage and current, two BNC cables were employed in a Kelvin measurement setup, connected together as close to the socket as possible, utilizing the remote-sense capabilities of the Source Measurement Unit (SMU) in the HP4142B. The above setup allowed a maximum of 700mA (well above the safe operating current for continuous operation) to be recorded with minimal loss in accuracy. The HP4145A is also connected to a computer with a GPIB-USB Interface where the desired values for voltage and current were chosen and the results were extracted though the software ICCAP by Agilent. Finally some of the diagrams were made in Origin-Pro, a software able to plot the desired measurements with their mean value and the calculated error bars. (In this thesis every mean calculation was plotted with $\pm 2\sigma$ limitation). (figure 5.1)

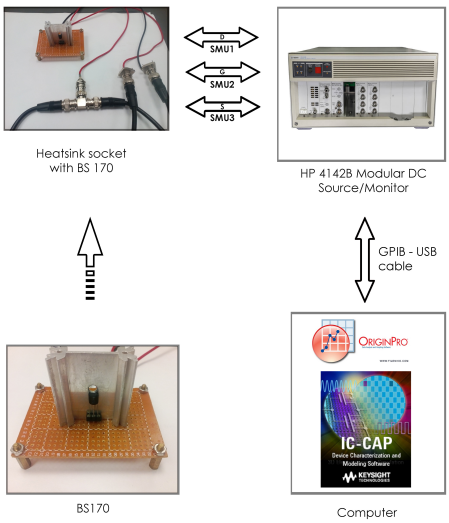
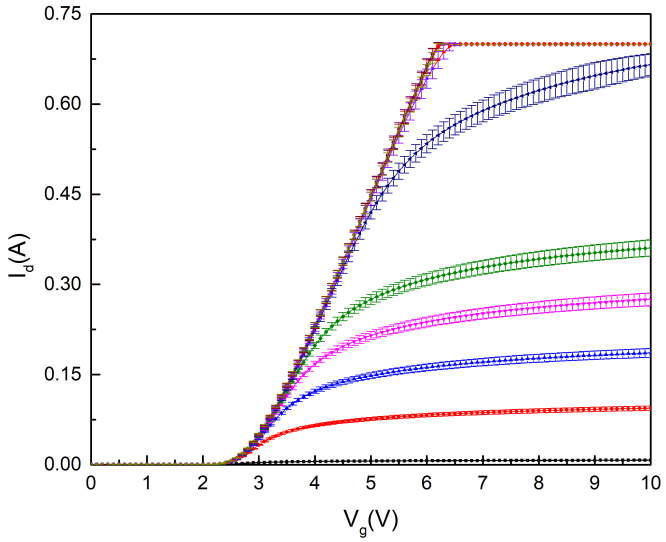


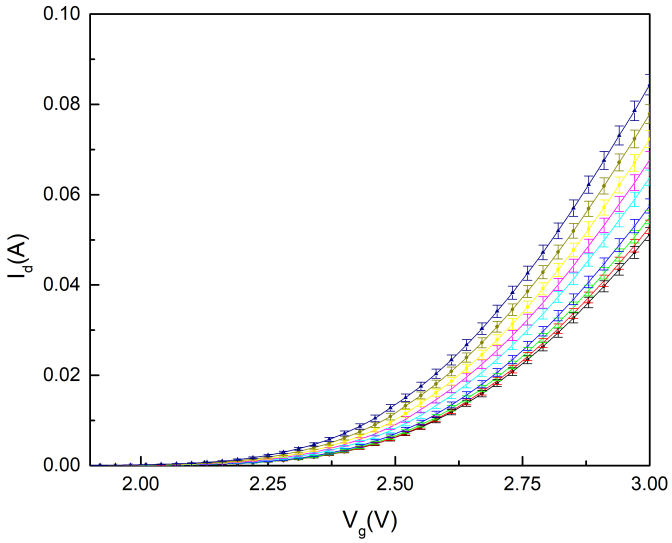
Figure 5.1: Block diagram for power VDMOS BS170 with cable connections

5.1.1 I-V curves

To begin with, the mean value of current versus gate voltage is plotted. The range of the drain bias starts at 0.02V and ends at 43V. The higher drain voltages are measured until gate voltage equals 3 V while lower V_d(V_d<7V) reach 10V respectively. A closer look at figure 5.2 (a) shows that for drain voltage of 3, 4, 5, 6 V the drain current reaches the compliance limit. Moreover, error bars are getting wider as the current rises which is related to the current spread of the BS170. This is shown clearly at figure 5.3 where a low (0.25V) (a) and a high (11V) (b) drain voltages have been chosen to plot the $I_d - V_g$ curve. With gray colour are the measurements of each transistor and with black colour is the mean value. Red and green colours represent the highest and the lowest $I_d - V_g$ boundary respectively. (highest curve equals the mean values $+2\sigma$ and -2σ for lowest).

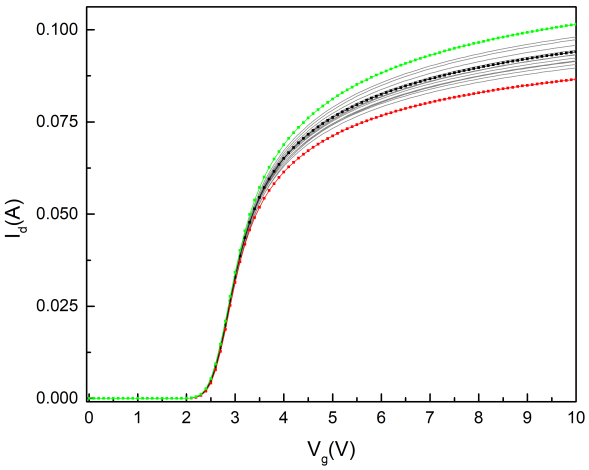


a)

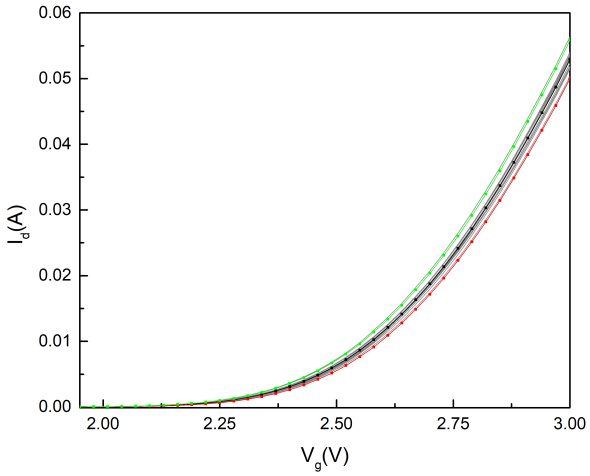


b)

Figure 5.2: Mean values of drain current versus gate voltage for V_d=0.02, 0.25, 0.5, 0.75, 1, 2, 3, 4, 5, 6 V (a) and for V_d=7, 11, 15, 19, 23, 27, 31, 35, 39, 43 V (b)



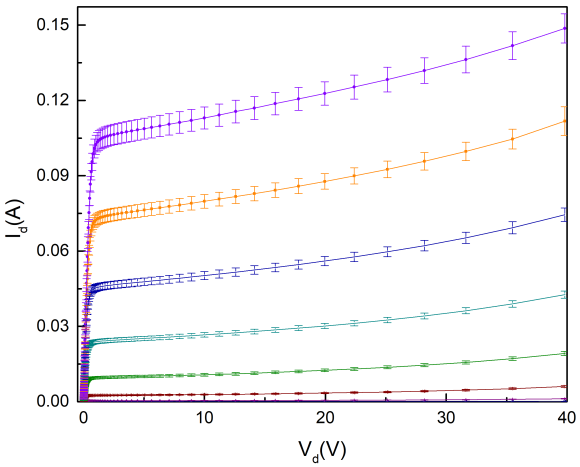
a)



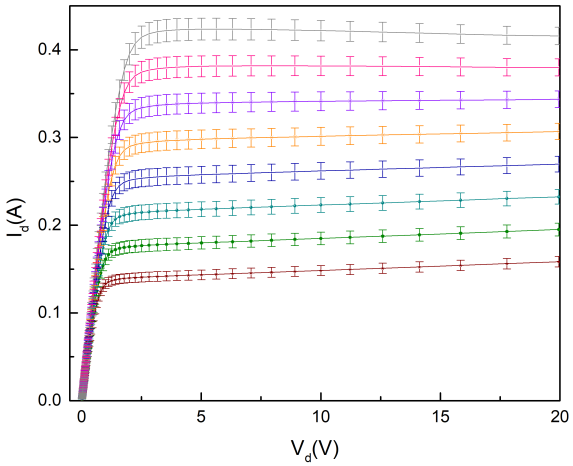
b)

Figure 5.3: Measured drain current versus gate voltage for 10 devices plotted with the mean value E (black line) and mean value E $\pm 2\sigma$ (green-red line) at V_d= 0.25(a), V_d= 11(b)

Almost the same procedure has been followed, for the drain current versus drain voltage plots. In the first diagram where the lowest gate voltages are pictured, both of the operation regions (linear and saturation) can be noticed. This can be seen in the second diagram too, but not in the third where the transistor operates in linear mode for the chosen values of gate voltage. Drain voltage range in each figure is calculate according to current compliance limit in order the measurements to be more accurate. Finally, the self heating effect is noticeable in figure 5.4 (b) for the 2 highest gate voltages (4.6 V, 5 V) and is illustrated at figure 5.5 where $I_d - V_d$ curves of each transistor are compared for two different values of V_g(3.6 V, 5 V).



a)



b)

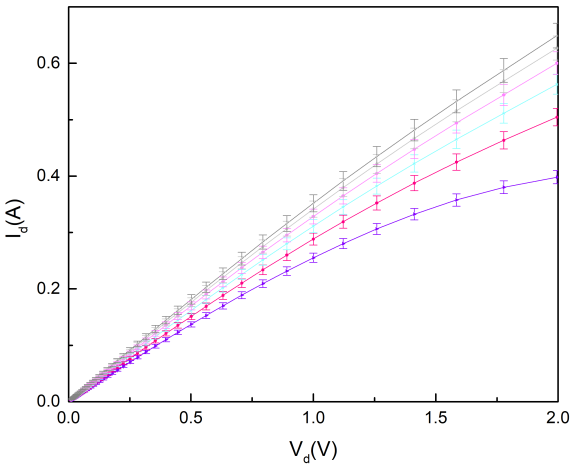
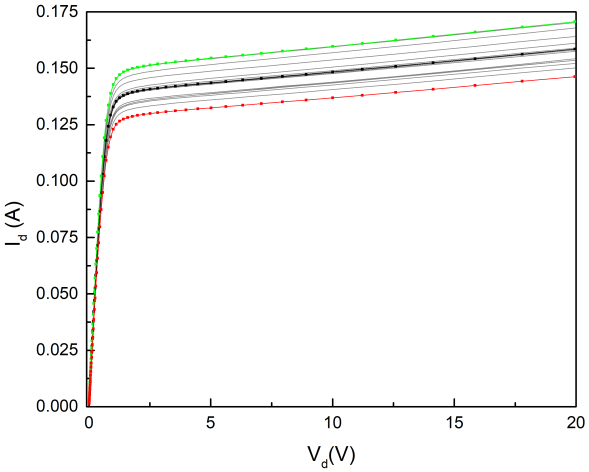
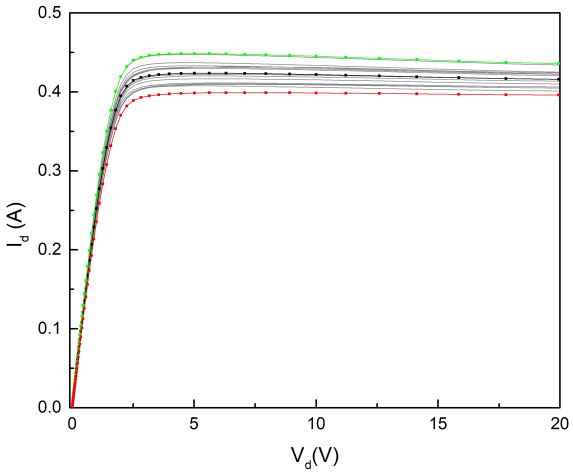


Figure 5.4: Mean values of drain current versus drain voltage for V_g=1.8, 2, 2.2, 2.4, 2.6, 2.8, 3, 3.2, 3.4 V (a), for V_g=3.6, 3.8, 4, 4.2, 4.4, 4.6, 5 V (b) and for V_g=5, 6, 7, 8, 9, 10 V (c)



a)



b)

Figure 5.5: Measured drain current versus drain voltage for 13 devices plotted with the mean value E (black line) and mean value E $\pm 2\sigma$ (green-red line) at V_d= 3.6 V (a), V_d=5 V (b)

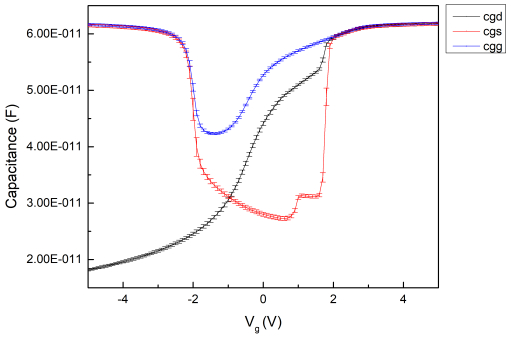


Figure 5.6: Measured capacitances C_{gg} (gate to all the other terminals connected together capacitance, blue line), C_{gd} (gate to drain capacitance, black line) and C_{gs}(gate to source capacitance, red line)

At last, dynamic characteristics are plotted. Gate to source, with drain floating (C_{gs}) and gate

to drain with source floating (C_{gd}) as well as the gate capacitance with all the other terminals connected together to ground (C_{gg}) were measured. Due to lack of correct subcircuits for simulation ((C_{gs}),(C_{gd})) as well as apparent initial model incompatibility (C_{gg}), simulated data are not available and could not be produced as part of this thesis. We can, however, note the tight grouping of the measured curves which insignificant variation among all thirteen measured devices ($\sigma = 0.3$) .

5.1.2 Threshold Voltage

The threshold voltage for BS170 is extracted for two values of drain bias (Vd = 0.25, 11V). The mean values show that the threshold voltage in linear operation is higher than saturation, as occurs in most MOS technologies. ($V_{th,linear} = 2.22V, V_{th,sat} = 2.20V$) Once more this can be explained as a manifestation of the DIBL effect where higher drain voltages induce reduction of threshold voltage (figure 5.6). However it has to be noted that for discrete power devices, variability between different manufacturers and even within the same batch greatly overshadow such minute changes. Lastly, by cross-check the value of threshold voltage presented in the device datasheet [3] ($V_{th.dsh} = 2.1V$), the measured average value is almost the same ($V_{th.ms} = 2.2V$).

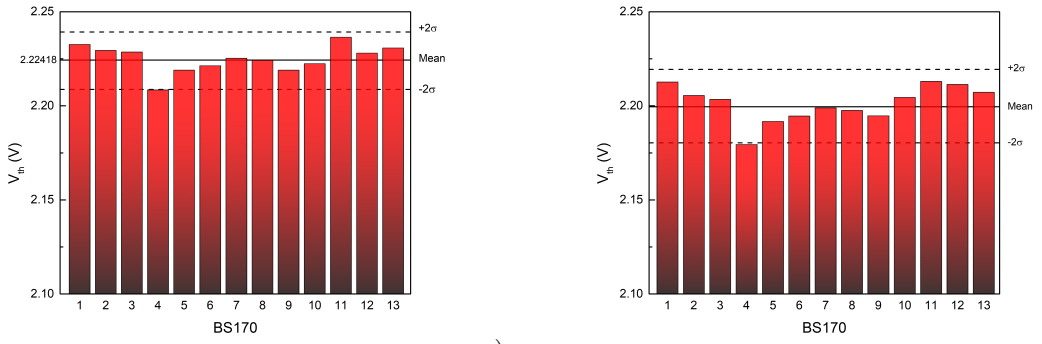


Figure 5.7: Threshold voltage in linear region (V_d=0.25V) (a) and in saturation (V_d= 11V)(b) with average values $V_{th,lin}$=2.22 V, $V_{th,sat}$=2.20 V respectively.

5.1.3 Slope Factor

Slope factor extracted from $\frac{g_m U_t}{I_d}$ versus I_d as described in Chapter 2. In figure 5.7, and the mean values at linear and saturation region, are almost equals. ($E(n_{lin}) = 3.02, E(n_{sat}) = 3.07$)

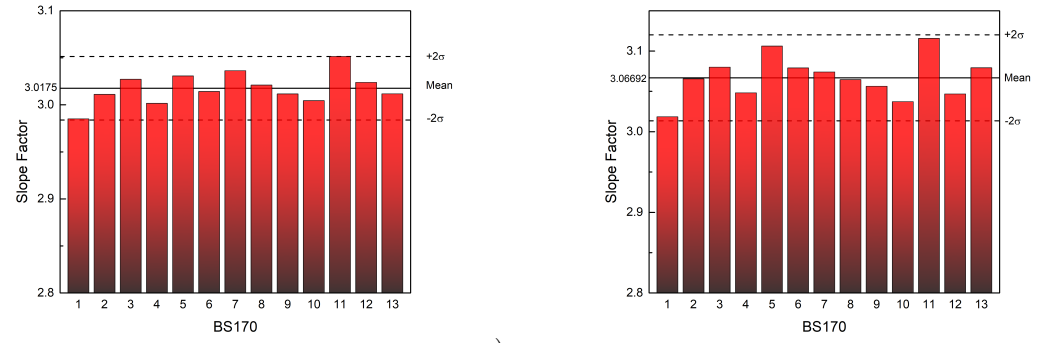


Figure 5.8: Slope factor in linear region (V_d=0.25V) (a) and in saturation (V_d= 11V)(b) with average values E_{lin}=3.02, E_{sat}=3.07 respectively.

5.1.4 Mobility

The low field mobility mean value is also extracted from ($E(_0) = 70.39\frac{cm^2}{Vs}$)and plotted with the individual measurements for each transistor. (figure 5.8)

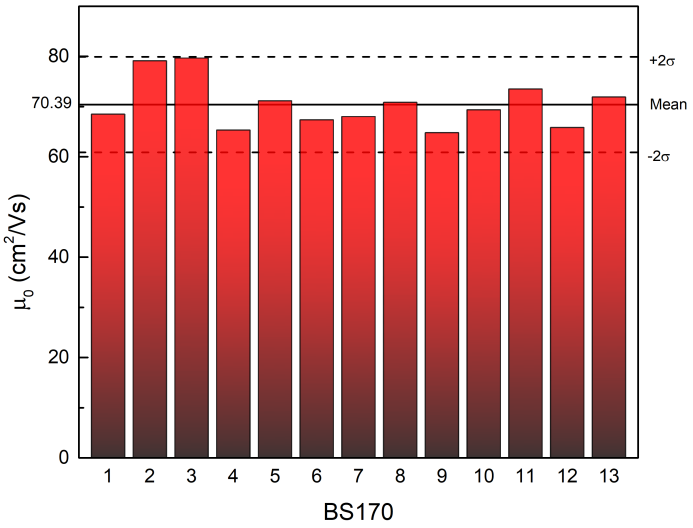


Figure 5.9: Mobility μ_0 and the mean value E(μ_0)=$70.39\frac{cm^2}{Vs}$

5.1.5 On-resistance

The on resistance of the BS170 has a mean value of $E(R_{DSon}) = 2.90\Omega$ o which is quite smaller than the high voltage LDMOS. The explanation is that BS170 are designed to operate with much higher current than HV-LDMOS that are primarily made for integrated chips. The mean value (E(R_{on})=2.90Ω) is in excellent agreement with the BS170 datasheet [3], where the on resistance values given by the manufacturer range between a typical value of 1.2 Ω up to a maximum of 5 Ω.

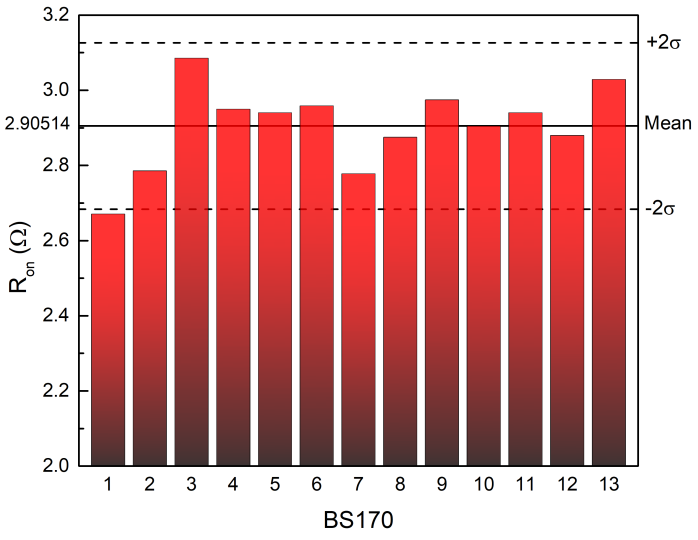


Figure 5.10: On resistance and the mean value E(R_{on})=2.90Ω

5.1.6 Capacitance

After taking into consideration supplementary C-V measurements between gate and drain (source open), gate and source (drain open) and also considering the maximum allowed gate voltage of the device ($\pm 20V$), we estimated that approximately 20 pF should be attributed to overlap capacitance, therefore reducing the effective Cox to approximately 40pF from the original 60 pF. From this C'_{ox} was calculated as 1.8 $\frac{mF}{cm^2}$ which was later used in parameter extraction and model fitting. The BS170 datasheet [3] providea a C_{gate} value of almost $6E^{-11}$F which is very close to the one we measured. The mean value that results from this reduction is presented in figure 5.10.

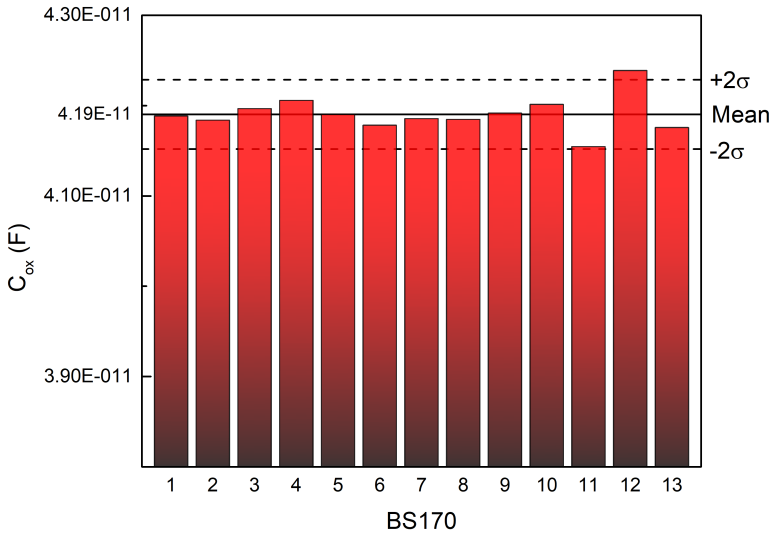


Figure 5.11: Measured total capacitance (c_{gate}) of the transistors and the mean value $E(C_ox) = 4.19E^{-11}$ F

5.2 Parameter extraction

In this section some essential guidelines for the parameter extraction procedure of the model are investigated. It has been described earlier in this thesis that the device can be analyzed in two different parts but the electrical behaviour of the transistor can only be considered as a whole. However the study of those parts and especially of the low-voltage part can be used as a good starting point for parameter extraction because it operates as a regular MOS device of whose measurements we can use to calculate basic parameters. This is in general the guideline for this procedure: at first the basic characteristics of the high voltage MOSFET are calculated, then the elementary parameters are being modified and step by step more complex parameters are used in order to simulate the model. One very important advantage of the EPFL HV-MOSFET compact model is that it gives the user the option to choose between the electrical or the physical component of a parameter which makes this model very versatile.

5.2.1 Procedure

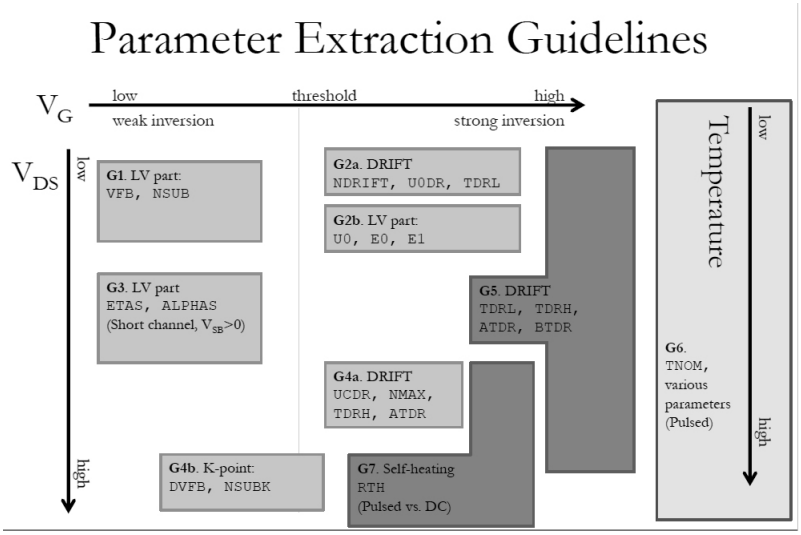


Figure 5.12: EPFL HV-MOSFET compact model guideline for parameter extraction [?]

In figure 5.11, is the methodology that was used in order to simulate the operation of the transistor and to extract the parameters [2]. Each part of the guideline will be described. The electrical parameters were used instead of the physical ones in this thesis.

G1.Low-voltage part, V_dslow

In this step, the inner MOS operates in linear and weak inversion region because of the low voltage at the drain and the gate. Zero bias threshold voltage (V_{T0}) and body effect factor at the the source side of the channel were extracted(GAMMA).

G2.High-voltage part, $V_{ds}low$ As the current rises, the inner MOS channel is driven to strong inversion and the high voltage part of the transistor becomes noticeable. While the drift region is operating under high gate voltage, current flow thickness(TDRL), drift region modulation factor (GAMMAD) and low-field transconductance factor are extracted (KP,KPDR). In addition, more mobility characteristics are extracted as the E0, E1, ETA which are parameters related to a higher order effect, mobility reduction due to vertical field. In order to achieve better fitting, recursive adjustments had to be made in those mobility parameters.

G3.Low-voltage part, $V_{ds}high$ In this part, the device operates in weak inversion but with high bias at the drain. Once more the low-voltage part is the dominant element of the device but this time it operates under higher potential difference between drain and source. Parameters related to drain-induced barrier lowering (DIBL) effect could be extracted here (ALPHAS, BETAS, SIGMAS, ETAS).

G4.High-voltage part, $V_{ds}high$ The drift region is the most important and leading region in this step. High voltage is applied to gate and drain, and the current is mostly affected by the drift region parameters such as the maximum relative carrier concentration in the drift region (NMAX) and drift velocity saturation (UCDR). Additionally, in comparison with the second step (G2) where drain bias was lower, a germinal extraction of parameters related to the quasi-saturation effects (TDRH, ATDR) is made. Moreover, this step is ideal for K-point parameters extraction such as threshold voltage near the drain end (DVT0) and body effect factor (GAMMAK) because its role is more distinct while none of the two parts of the device are dominating and while gate bias transits from low to high values.

G5.High-voltage part versus V_{ds} analysis

In this step, the parameters of the two previous guidelines are re-calculated but this time from the point of view of I_dvsV_d analysis. It is better for quasi-saturation effects to be studied in this step along with fine tuning parameter BTDR. Once more, recursive tuning to those parameters is performed by going through the last three steps (G5->G3->G4->G5->..).

G6.Study of temperature dependence

After our model is fitted to BS170 measurements for a specific value of TNOM (reference temperature), it is important to repeat the whole process again (step 1-5) at different temperatures. This procedure makes it possible to extract the temperature-dependent characteristics because in order to simulate the model, temperature coefficients of the already extracted parameters will be used in their place. In our case, this step was skipped because our measurements were taken for a single temperature only. These parameters were left at their default values.

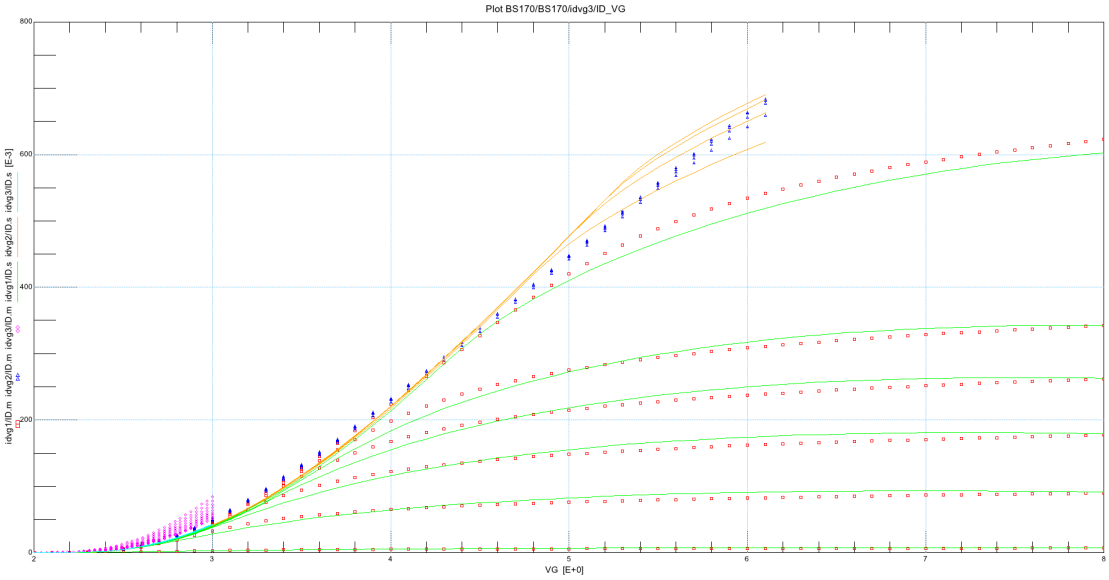
G7.Self heating, $I_d vs V_{ds}, highest value of V_{ds}$

Self heating effect as described before, can be noticed deep in saturation region for high drain bias. This is simulated by extracting the parameter of thermal resistance (RTH) at zero injected power.

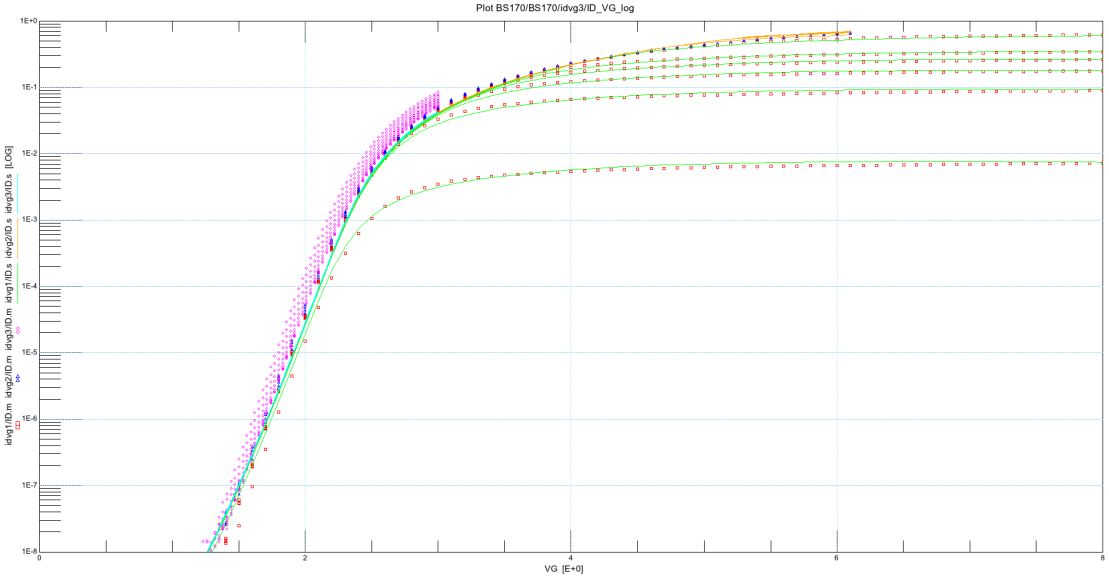
Lastly, it is important to mention that two more operational parameters were added to the EPFL-HV compact model and into the verilog-a code. The first parameter is NUV which was used to fit the model properly on the subthreshold slope and the other one is MULT (from multiplicity) that was used in order to make the model able to simulate arrays of parallel transistors.

5.2.2 Model Fitting

The process of parameter extraction was finished when there was no other change that would lead to better fitting. Both simulated (lines) and measured (markers) results are plotted below. Figure 5.12 shows the drain current versus gate voltage diagrams where for lower drain voltages the model is more accurate. For higher values of drain bias we were unable to correctly account for the DIBL effect. In the gate transconductance plot (figure 5.13) the previous deductions are also visible and the simulation curve for higher drain voltages is becoming sharper unlike the measured. Figure 5.14 where the $I_d - V_d$ diagram is depicted, shows that the best fit occurs at a gate voltage of 4V. Additionally, the self heating effect can be observed for the higher values of drain bias and the model fitting closely follows the measurement trend. In the linear region ($V_d = 0...2V$), model fits quite well to the measurements which is important because those values are used to extract the on resistance (figure 5.15). To conclude, the simulation of the BS170 is not totally accurate but it approaches the measured values without big differences and it describes most of the higher order effects, both for the low-voltage part and the drift region, at an adequate level.



a)



b)

Figure 5.13: Simulated (lines) compare to measured (symbols) values of drain current versus gate voltage (with a range of 2 to 8V) (a) and logarithmic drain current versus gate voltage (b) whereas the values of drain bias are (V_d=0.02, 0.25, 0.5, 0.75, 1, 2, 3, 4, 5, 6, 7, 11, 15, 19, 23, 27, 31, 35, 39, 43 V)

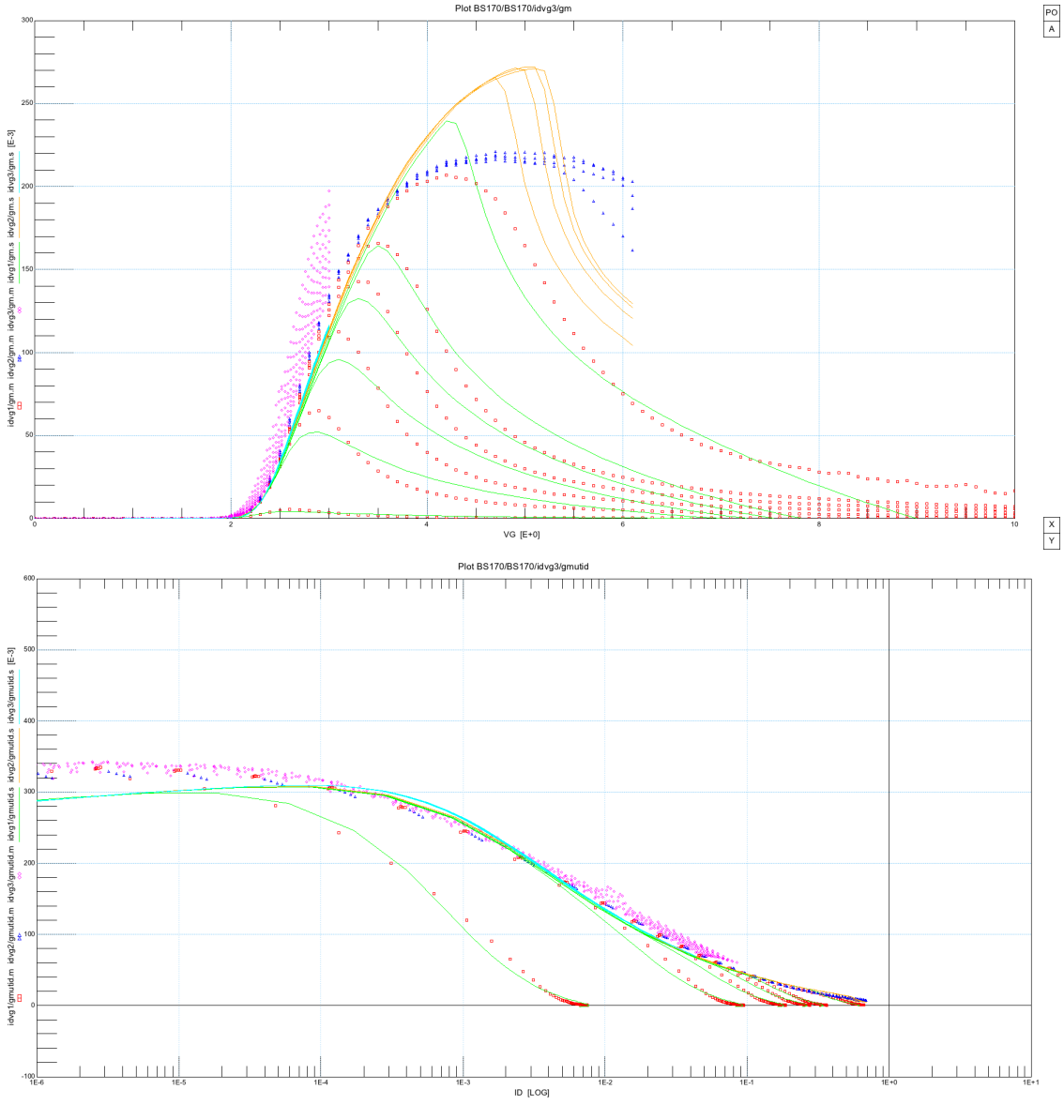
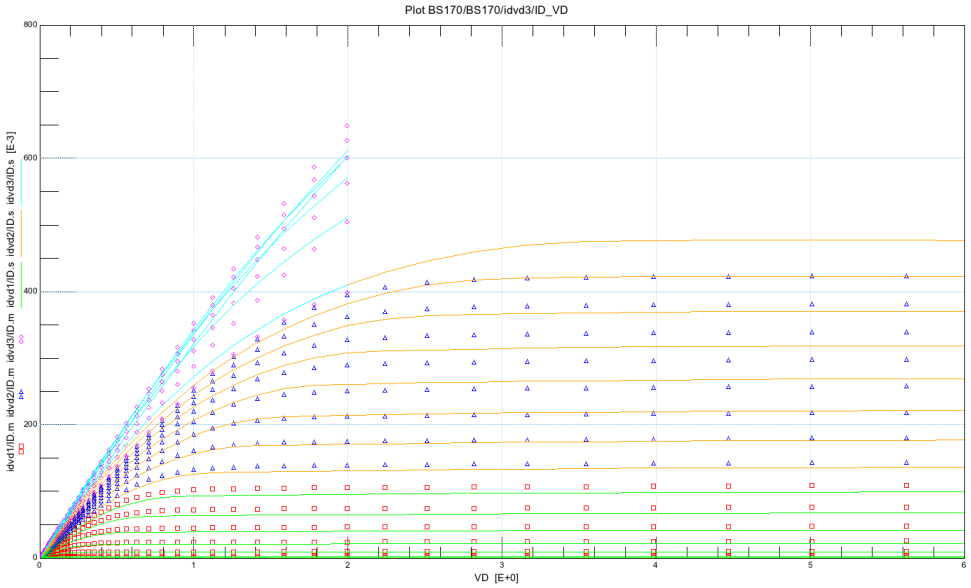
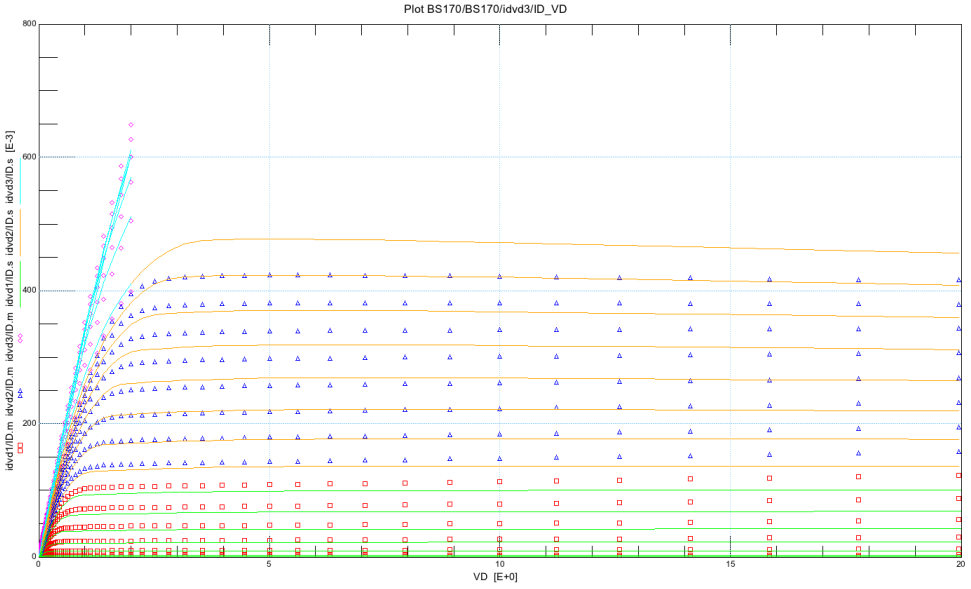


Figure 5.14: Simulated (lines) compare to measured (symbols) values of transconductance versus gate voltage (a) and $\frac{g_m U_t}{I_d}$ versus drain current (b) whereas the values of drain bias are (V_d=0.02, 0.25, 0.5, 0.75, 1, 2, 3, 4, 5, 6, 7, 11, 15, 19, 23, 27, 31, 35, 39, 43 V)

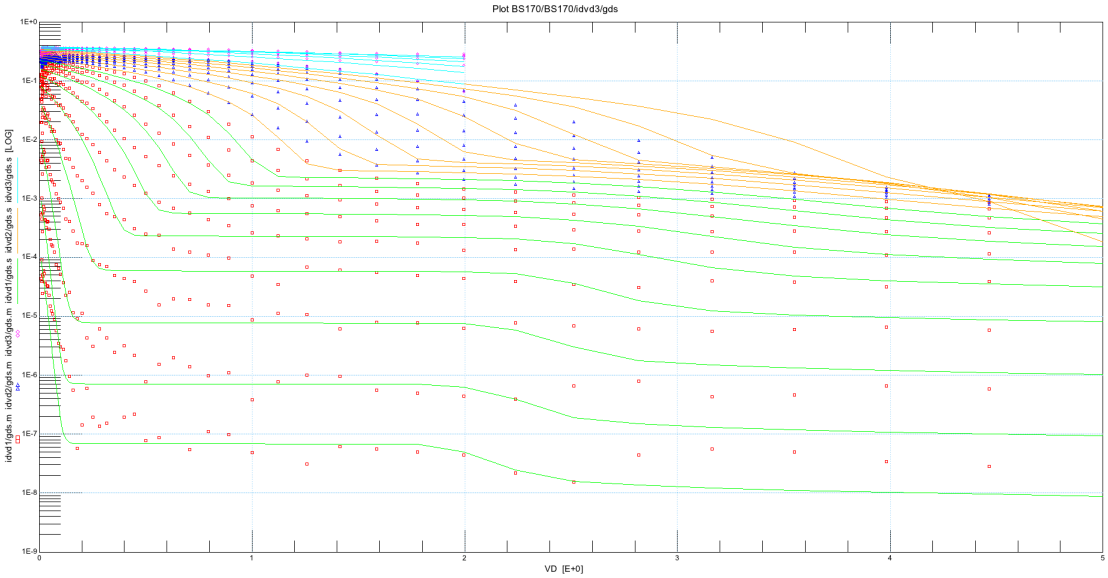


a)



b)

Figure 5.15: Simulated (lines) compare to measured (symbols) values of drain current versus drain voltage at $V_g = 5V$ (a) and at $V_g = 20V$ (b) whereas the values of gate bias are (V_g=1.8, 2, 2.2, 2.4, 2.6, 2.8, 3, 3.2, 3.4, 3.6, 3.8, 4, 4.2, 4.4, 4.6, 4.8, 5, 6, 7, 8, 9, 10 V)



a)

Figure 5.16: Simulated (lines) compare to measured (symbols) values of output conductance versus drain voltage whereas the values of gate bias are (V_g=1.8, 2, 2.2, 2.4, 2.6, 2.8, 3, 3.2, 3.4, 3.6, 3.8, 4, 4.2, 4.4, 4.6, 4.8, 5, 6, 7, 8, 9, 10 V)

5.2.3 Extracted parameter values

At last, the whole set of parameters that are used for simulation with the EPFL HV model are presented. They comprise the full modelcard of the BS170 which can be used with the simulator SPECTRE (by Cadence).

*****MAIN PHYSICAL AND ELECTRICAL PARAMETERS*****
TOX = 0
COX = 0.00185567
VFB = -1000
VT0 = 2.31
NSUB = 0
PHIF = 0
GAMMA = 1.22
DVFB = -1000
DVT0 = -0.00912011
NSUBK = 0
PHIFK = 0
GAMMAK = 1.2
NUV = 1.8

*****MOBILITY PARAMETERS*****
U0 = 0
KP = 0.00014388

*****MOBILITY REDUCTION DUE TO VERTICAL FIELD*****
E0 = 9.59401E+07
E1 = 1.14815E+08
ETA = 0.753356

*****BIAS DEPENDENCE AND LENGTH SCALING OF EQUIVALENT PINCH-OFF VOLTAGE GRADIENT*****
DGC1 = 0.25

DGC2 = 0
DGE = 0.5

*****NON-UNIFORM DOPING LENGTH SCALING FACTOR FOR INTERMEDIATE AND LONG CHANNEL DEVICES*****
LDG = 1E-06

*****GEOMETRICAL PARAMETERS (SHORT AND NARROW CHANNEL CORRECTIONS)*****
DL = 5.47016E-07
DW = 7.99418E-05
DWD = 0

*****REVERSE SHORT CHANNEL EFFECT*****
LR = 1
QLR = 0
NLR = 0

*****SUBTHRESHOLD BARRIER LOWERING*****
ETAS = 0.5
SIGMAS = 0.1
ALPHAS = 1
BETAS = 0.1

*****VELOCITY SATURATION*****
VSAT = 0
UCRIT = 2.5397E+07

*****CHANNEL LENGTH MODULATION*****
LAMBDA = 1.8197
LC = 1E-06

*****GEOMETRICAL PARAMETERS*****
LDR = 8E-05
TDRL = 2.39883E-09
TDRH = 2.18776E-09
TDRLS = 0
TDRHS = 0

*****GATE OVERLAP LENGTH OVER THE DRIFT REGION (USED IN AC BEHAVIOUR)*****
LOVD = 1.5E-07
DLC = 5E-08

*****CHARGE SHEET LAYER ACCUMULATION THICKNESS*****
DACC = 2E-08

*****MAIN PHYSICAL AND ELECTRICAL PARAMETERS*****
NDRIFT = 0
PHIFD = 0
GAMMAD = 0.532108

*****DRIFT MOBILITY PARAMETERS*****
U0DR = 0
KPDR = 0.000547016

*****DRIFT VELOCITY SATURATION*****
VSATDR = 0
UCDR = 1.80302E+07

*****QUASI-SATURATION*****
ATDR = 1
BTDR = 0.2

*****MAXIMUM DOPING AT THE DRAIN SIDE*****
NMAX = 40.5

*****IMPACT IONIZATION CURRENT*****
IBA = 1E+08
IBB = 2E+08
IBN = 1
IBH1 = 30
IBH2 = 1

*****SELF HEATING*****
RTH = 17.2187
CTH = 0

*****TEMPERATURE PARAMETERS*****
TNOM = 27
TCVT0 = 0
TCDVT0 = 0
TCVFB = -0.001
TCDVFB = 0
TCRTH = 0
BEX = -1.5
BDREX = -1.5
UCEX = 1.5
UCDREX = 1
E0EX = 0
E1EX = 0
TCNMAX = 0
TCETAS = 0
TCTDRL = 0
TCTDRH = 0
TCATDR = 0
TCBTDR = 0
IBBT = 0

*****OVERLAP CAPACITANCES*****
CGBO = 0
CGSO = 0
CGDO = 0
XQDO = 0

*****SOURCE-BULK AND DRAIN-BULK JUNCTION DIODE PARAMETERS*****
GMIN = 1E-12
NS = 1
ND = 1
JS = 0
JSSW = 0

JSSWG = 0
JD = 0
JDSW = 0
JDSWG = 0
CJS = 2E-05
CJSSW = 0
CJSSWG = 0
CJD = 0.0001
CJDSW = 0
CJDSWG = 0
MJS = 0.8
MJSSW = 0.7
MJSSWG = 0.7
MJD = 0.5
MJDSW = 0.4
MJDSWG = 0.4
PBS = 0.8
PBSSW = 0.6
PBSSWG = 0.6
PBD = 0.6
PBDSW = 0.5
PBDSWG = 0.5
TTS = 0
TTD = 0
XTIS = 3
XTID = 3
TCJ = 0
TPB = 0

*****GATE RESISTANCE*****
RGSH = 3
RG = 0

6 Conclusions

While this work has resulted in a good first model for the static behaviour of the BS170 transistors, future work will need to be more centered around the dynamic operation of the devices. Further and in depth study of the capacitive response will enrich the parts of the model concerned with AC behaviour. Another possibility for further study could be the thermal characterization and fitting of the model at different temperatures, which would also result in a more accurate description of the self-heating effect. It should also be mentioned that as such devices are mostly used for switching, their transient response is a topic of much interest and the EPFL-HV model can accommodate that.

On the subject of the EPFL-HV model, further work can be done to incorporate into the code even more phenomena encountered during (D)MOS operation. Much work can be done on the continual development of the model and one obvious suggestion would be to incorporate a mechanism to describe the reverse junction breakdown in MOS transistors.

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