TECHNICAL UNIVERSITY OF CRETE

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Design of low power operational transconductance amplifiers (OTAs) in two generations of Bulk CMOS

by

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"To the memory of my grandmother Maria and my uncle George"

Chania, December 2019

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Abstract

The continued need for accurate design methodologies mandates an ongoing research in this field. In this work, the Inversion Coefficient (I_C) based methodology for low-power, low-voltage MOSFET design was explored. This methodology is based on design-oriented transistor parameter extraction, such as I_0 (technology current), slope factor n, transconductance parameter K_P etc. and several important performance metrics in the form of Figures-of-Merit (FoM), such as g_m/I_D and A_V (intrinsic gain). To test the accuracy of this approach, two different operational transconductance amplifier (OTA) topologies were designed in low power mode of operation (power dissipation $24uW$), a current mirror p-input, single-ended OTA and a p-input, fully differential, folded cascode (FDFC) OTA. To accentuate the prediction capability of this methodology, two process design kits (PDKs) were used; a 65nm bulk CMOS PDK and a 90nm bulk CMOS PDK. The structural design flow includes the procedure of parameter extraction for both PDKs, the mathematical analysis of each circuit, the design validation and optimization via simulation. All four designs were developed in Virtuoso ADE by Cadence and simulated using Spectre Simulation Platform. Open-Loop Gain (A_0), Gain Bandwidth (GBW), Phase Margin (PM), Slew Rate (SR), Input and Output Voltage ranges, Input referred Noise and Input DC offset were set as circuit performance criteria. Finally, comparative results between circuit topologies and technology nodes are presented and discussed.

Περίληψη

Η διαρκής ανάγκη για ακριβείς μεθοδολογίες σχεδίασης απαιτεί μια συνεχή έρευνα στον τομέα αυτό. Σε αυτή την εργασία, διερευνήθηκε η μεθοδολογία που βασίζεται στον δείκτη αναστροφής (I_C) για σχεδιασμό κυκλωμάτων με MOSFET, χαμηλής ισχύος και χαμηλής τάσης. Αυτή η μεθοδολογία βασίζεται στην εξαγωγή παραμέτρων των τρανσίστορ προσανατολισμένη στη σχεδίαση, όπως το I_0 (ρεύματος τεχνολογίας), τον συντελεστής κλίσης n, την παράμετρο διαγωμιμότητας K_P κλπ. και αρκετές σημαντικές μετρικές απόδοσης (FoM), όπως g_m/I_D and A_V (ενδογενές κέρδος). Για να εξεταστεί η ακρίβεια αυτής της προσέγγισης, σχεδιάστηκαν δύο διαφορετικές τοπολογίες τελεστικών ενισχυτών διαγωγιμότητας (OTA) σε λειτουργία χαμηλής ισχύος (απόδοση ισχύος $24uW$), έναν p-εισόδου καθρέφτη ρεύματος τελεστικό ενισχυτή διαγωγιμότητας OTA μονής εξόδου και έναν τελεστικό ενισχυτή διαφορικής εξόδου (FDFC) OTA. Για να τονισθεί η δυνατότητα πρόβλεψης της συγκεκριμένης μεθοδολογίας, χρησιμοποιήθηκαν δύο διαφορετικά κιτ σχεδιασμού (PDKs)· ένα CMOS PDK 65nm και ένα CMOS PDK 90nm. Η διαδικασία δομικής σχεδίασης περιλαμβάνει την εξαγωγή παραμέτρων και για τα δύο PDK, τη μαθηματική ανάλυση κάθε κυκλώματος, την επαλήθευση των αποτελεσμάτων της σχεδίασης και τη βελτιστοποίηση μέσω προσομοίωσης. Και οι τέσσερις σχεδιάσεις αναπτύχθηκαν στο Virtuoso ADE από την Cadence και προσομοιώθηκαν με τη χρήση του Spectre Simulation Platform. Το κέρδος ανοικτού βρόχου (A_0), το εύρος ζώνης κέρδους (GBW), το περιθώριο φάσης (PM), ο ρυθμός μετατόπισης (SR), τα εύρη τάσης εισόδου και εξόδου, καθορίστηκαν ως κριτήρια απόδοσης κυκλώματος. Τέλος, παρουσιάζονται και αναλύονται συγκριτικά αποτελέσματα μεταξύ των τοπολογιών και των διαφορετικών τεχνολογιών.

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1 Introduction

1.1 Technology Parameters extraction and OTAs design and implementation

Commercial process design kits PDKs are commonly used from designers, in both industry and research environments, in order to create schematic and and layout circuit topologies for various circuitry products. Standard bulk CMOS processes of 90nm and 65nm are typically used in circuits such as: electronics for sensors, analog filters, RF front-ends, microprocessors etc. can be mentioned as indicative examples of designs to be implemented for real-life application. Current thesis provides an insight analysis of how two commercial bulk CMOS process PDKs, of 90nm and 65nm processes, can be used, from designers perspective, in order to provide the best possible solution in the design procedure of a the basic analog unit circuit of an OTA (Operational Transconductance Amplifier). For this reason, the thesis is divided into two parts. In the first part, the basic structural unit of a CMOS technology, the MOSFET, is used in order to extract the main technology parameters of both PDKs. Parameters like oxide capacitancies, slope factor, carrier mobility, DC gain, early voltage, mismatch and low frequency noise and basic figures of merit such as transconductance efficiency are extracted and compared for various channel lengths and widths and for both technologies. In the second part, the extracted parameter's values together with some proposed design optimization methodologies, based on parameter tradeoffs, are used, in order to extract the best possible OTA designs out of each of the two aforementioned technologies.

1.2 Thesis structure

The context of this thesis is organized as follows: in current section a brief introduction in the thesis contents. In section 2, the basic MOSFET device physics and structure will be demonstrated. In section 3, technology parameters extraction will be detailed discussed. Finally, in section 4 Operational Transconductance Amplifiers (OTAs) will by analytically described.

2 Basic MOSFET device physics and structure

The metal–oxide–semiconductor field-effect transistor, commonly abbreviated as MOSFET [1], is a field-effect semiconductor device. It has an insulated gate, whose voltage determines the conductivity of the device. This ability to change conductivity with the amount of applied voltage can be used for amplifying or switching electronic signals.

Although, there are two major types of three-terminal semiconductor devices: the metal-oxide-semiconductor field-effect transistor (MOSFET), which is studied in this chapter, and the bipolar junction transistor (BJT) and each of the two transistor types offers unique features and areas of application, the reason that the MOSFET has become by far the most widely used electronic device, especially in the design of ICs (integrated circuits) is that it requires almost no input current to control the load current, when compared with bipolar transistors (bipolar junction transistors, or BJTs).

Also, in enhancement mode MOSFET, voltage applied to the gate terminal increases the conductivity of the device, in depletion mode transistors, voltage applied at the gate reduces the conductivity [2]. MOSFETs are also capable of high scalability (Moore's law) [2], with increasing miniaturization [3], and can be easily scaled down to smaller dimensions [3]. Moreover, they consume much less power, and allow higher density, than bipolar transistors. The MOSFET is also cheaper in most cases and has relatively simple processing steps, resulting in a high manufacturing yield. MOSFETs can be made with either p-type or n-type semiconductors (PMOS or NMOS logic, respectively), complementary pairs of MOS transistors can be used to make switching circuits with very low power consumption, in the form of CMOS (complementary MOS) logic.

The name "metal–oxide–semiconductor" (MOS) typically refers to a metal gate, oxide insulation, and semiconductor (typically silicon). Strictly speaking, in modern technology the "metal" in the name MOSFET is sometimes a misnomer, because the gate material can be a layer of polysilicon (polycrystalline silicon). Similarly, "oxide" in the name can also be a misnomer, as different dielectric materials can be used with the aim of obtaining strong channels with smaller applied voltages [4].

In today's IC industry, the MOSFET is by far the most widely used transistor in both digital circuits and analog circuits. While initially CMOS was used exclusively for digital design, the constant push to lower costs and increase the functionality of ICs has resulted in it being used for analog-only, analog/digital, and mixed-signal (chips that combine analog circuits with digital signal processing) designs [4].

2.1 Structure of a MOSFET transistor

Figure 2.1 (a) shows the cross-section of an nmos transistor. We observe three diffusion regions of type p+ and n+ which are implemented on a p-type silicon substrate (single-crystal silicon wafer that provides physical support for the device and for the entire circuit in the case of an integrated circuit) [1].The two regions of type n+, will be as we will see below, two of the four terminals of the nmos transistor. The two similar heavily doped n-type regions, indicated in the figure, are the n+ Source (S) and the n+ Drain (D) regions, which are created in the substrate as mentioned above. The source is defined as the region that provides the charge carriers (electrons in the case of NMOS devices) and the Drain as the region that collects them [5]. These two regions, are similar as there are diffusion regions of type n+ and also occupy the same surface with the same diffusion thickness.

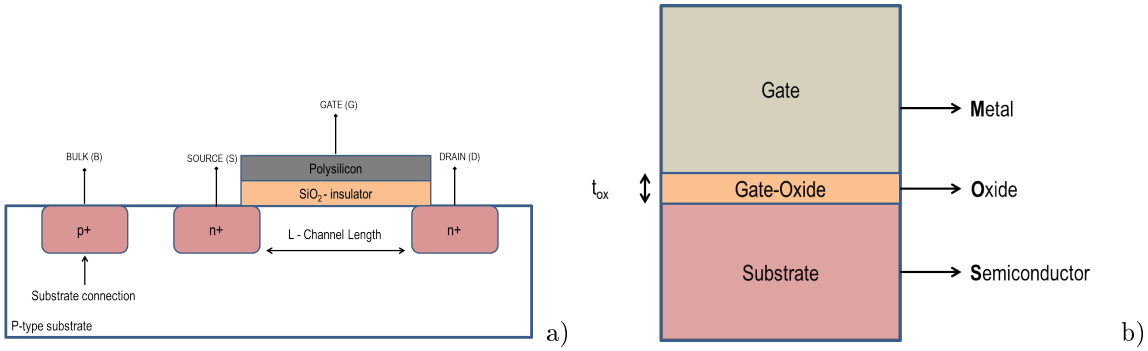


Figure 2.1: Cross section of (a) an n-type MOSFET (Substrate connection is also depicted) (b) Zoomed Gate region.

The third terminal of the transistor is the Gate (G). The material with which the gate is made is usually a metal or polysilicon-poly. Figure 2.1(b), shows the zoomed gate area. We can see, that there is material between the gate and the substrate that isolates the gate from the substrate so that there is no electrical contact between them. This material is called gate-oxide and the thickness of the t_{ox} is in the order of several Angstrom ($\sim 10^{-10}$) depending on the manufacturing technology [1].

So the transistor is made up of three layers beneath each other. At the top level there is the gate metal, just below the gate oxide and at the lower level is the p-type semiconductor and it is essentially the backbone of the integrated circuit. Due to this structure its name is: Metal-Oxide-Semiconductor => MOS. The substrate is the base on which the MOS transistors and all the electronic components of an integrated circuit are manufactured. In essence, the substrate is the fourth terminal of the transistor, since a potential must always be applied to it, which is always equal to the lowest potential applied to an integrated circuit. P+ diffusion is the necessary substrate contact and is used to properly polarize the substrate to the lowest potential.

Figure 2.2(a)(b), shows the structure of an NMOS transistor in all dimensions. An electron channel is formed between the source and the drain terminals. The distance L between these terminals is called channel length. The islets of type n+ extend to a width equal to W which is respectively called channel width. The designer of an NMOS can select the values of W and L depending on the specifications of the circuit designing it.

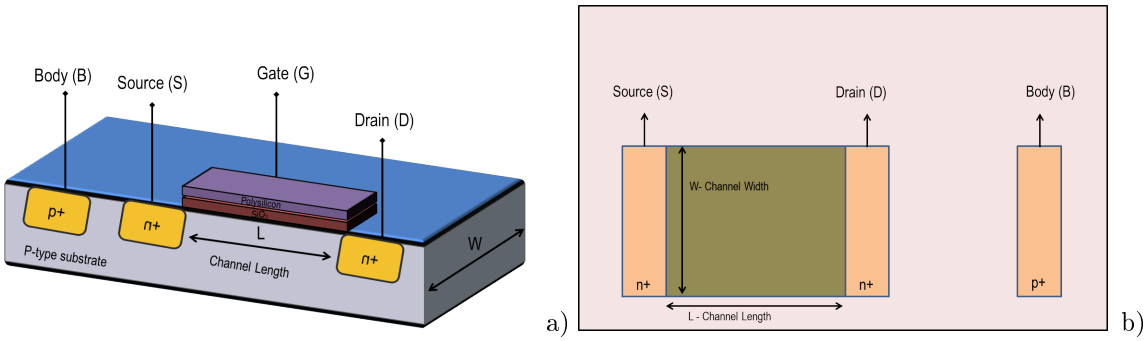


Figure 2.2: Physical structure of the NMOS transistor: (a) perspective view (b) top view.

Figure 2.3 shows a cross-sectional view of a p-channel MOSFET. The structure is similar to that of the NMOS device except that here the substrate is n+ type and the source and the drain regions are p+ type. All semiconductor regions are reversed in polarity relative to their counterparts in the NMOS case. The PMOS and NMOS transistor are said to be complementary devices [1].

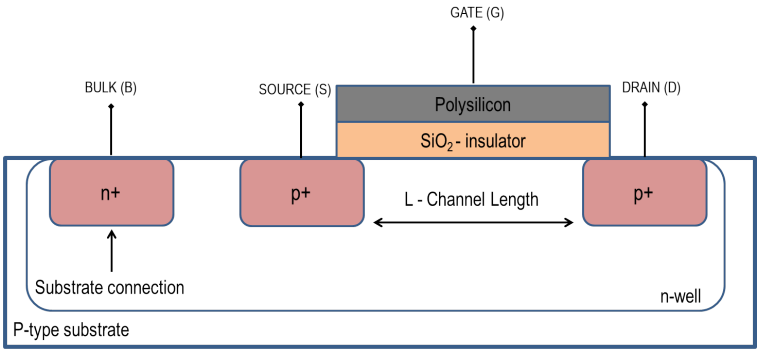


Figure 2.3: Cross section of a p-type MOSFET

In complementary MOS (CMOS) technologies, both NMOS and PMOS transistors are available. From a simplistic viewpoint, the PMOS device is obtained by all of the doping types (including the substrate), but in practice, NMOS and PMOS devices must be fabricated on the same wafer. i.e., the same substrate. For this reason, one device type can be placed in a "local substrate" usually called a "well". In today's CMOS processes, the PMOS device is fabricated in a n-well, Figure 2.3. The n-well must be connected to a potential such that the S/D junction diodes of the PMOS transistor remain reversed-biased under all conditions. In most circuits, the n-well is tied to the most positive supply voltage [5].

Figure 2.3, shows a cross section of a CMOS chip illustrating how the PMOS and NMOS transistors are fabricated. Observe that while the NMOS transistor is implemented directly in the p-type substrate, the PMOS transistor is fabricated in a specially created n+ region, known as an n-well as described above. The two devices are isolated from each other by a thick region of oxide that functions as an insulator. Not shown on the diagram are the connections made to the p-type body and to the n-well. The latter connection serves as the body terminal for the PMOS transistor [1].

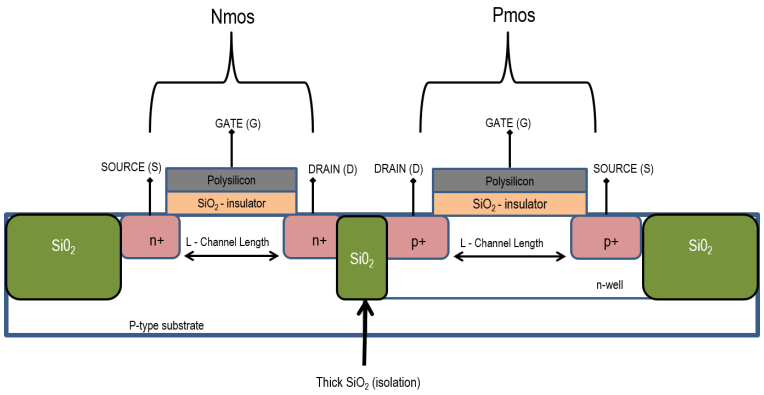


Figure 2.4: Cross-section of a CMOS integrated circuit.

A variety of symbols are used for the MOSFET. The basic circuit symbols used to represent NMOS and PMOS transistors are shown in Figure 2.5(a)(b). The symbols in this figure contain all four terminals, with the substrate denoted by "B" (bulk) rather than "S" to avoid confusion with the source [5].

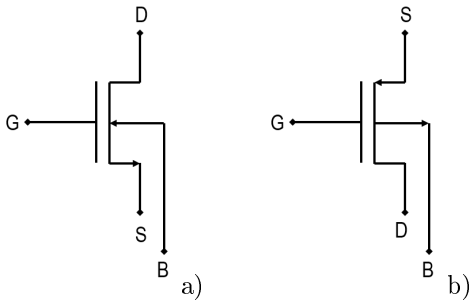


Figure 2.5: Circuit symbols: (a) NMOS (b) PMOS.

2.2 Basic description of MOSFET operation

2.2.1 Creating a channel for current conduction

With zero gate voltage, $V_{GS} = 0$, the two back-to-back p-n diodes formed by n+ source and drain diffusion areas and p-type substrate, prevent current conduction from drain to source when a positive V_{DS} voltage applied [1].

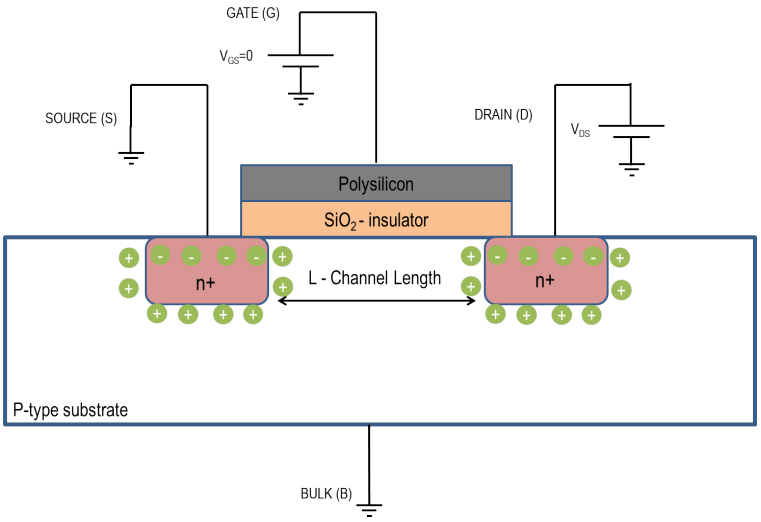


Figure 2.6: NMOS transistor with zero voltage applied to the gate.

When a positive voltage V_{GS} is applied, electrons are attracted from the heavily doped n+ source and drain regions into the channel area. When a sufficient number of electrons accumulate near the surface, an n-type region is created, connecting source and drain terminals, as indicated in Figure 2.7. When a voltage is applied between drain and source, current will flow through this induced n-type region, carried by the mobile charge. Correspondingly, the MOSFET of Figure 2.7 is called an n-channel MOSFET or, alternatively, an NMOS transistor. The value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form the conducting channel is called the threshold voltage and is denoted V_{TH}. For an n-channel MOSFET, V_{TH} is positive and its value is determined during fabrication[1, 5].

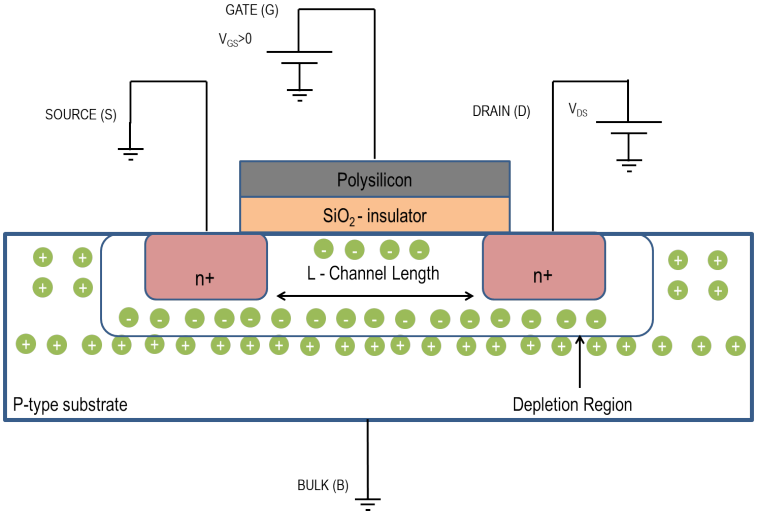


Figure 2.7: NMOS transistor with a positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate.

2.2.2 Applying V_{DS} voltage

When a positive voltage V_{DS} is applied, current I_D will flow trough channel from source to drain electrodes. The direction of I_D is considered to be opposite of that of the mobile charge flow. When V_{DS} is increased, the channel acquires a tapered shape, and its resistance increases as V_{DS} is increased, here, we assume that V_{GS} is kept constant at $V_{GS} > V_{TH}$. In this case, the device operates in the so called linear mode. In Figure 2.8(a), an NMOSFET operating in linear mode is depicted. When V_{DS} exceeds a specific value, namely saturation voltage ($V_{DS,SAT}$), the mobile charge at the drain end of the channel tends to zero and the channel is pinched-off. At this point it has to be mentioned that the source voltage is at all times at $V_S = 0V$. Although the channel does not extend the full length of the device, the magnitude of the electric field between the drain and the channel is relatively high, and therefore the device is capable of conduction. The drain current is almost constant weakly dependent versus drain voltage and mainly controlled by V_{GS}. In this case, the device operates in the saturation or active mode. Figure 2.8(b), shows an NMOSFET working at saturation [1, 6].

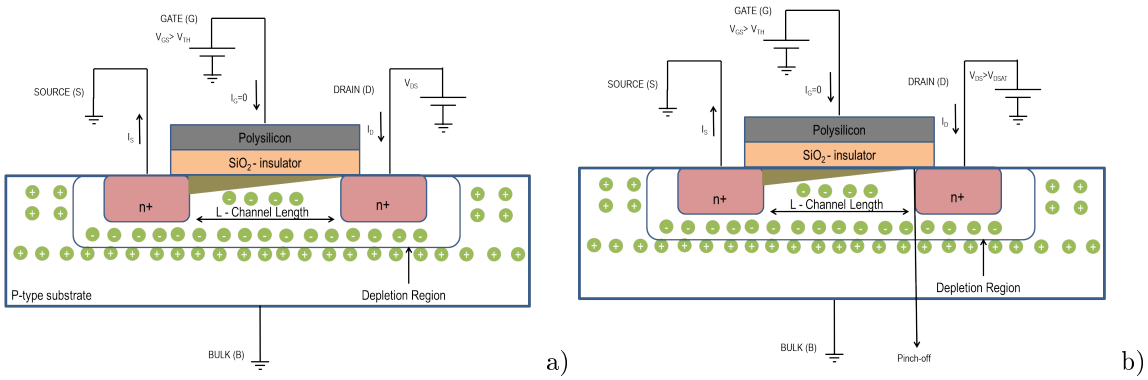


Figure 2.8: Mosfet operation: (a) Linear region (b) Channel pinch-off, saturation.

So far, the analysis is based on NMOS devices. For the PMOS counterpart, the same operation principles occur taking into consideration that negative voltages should be applied.

2.3 Inversions regions & Inversion Coefficient (I_C)

So far, the basic distinction between linear and saturation regions of a MOSFET operation was presented. In the current section, the two physical regions of operation depending on the magnitude of the effective voltage V_{EFF} ($V_{EFF} = V_{GS} - V_{TH}$) will be discussed. In this simplified approach, the value of V_{EFF} defines the inversion level of the channel and therefore a MOSFET can be either in weak or strong inversion (WI,SI). The transition region between those two regions is known as Moderate inversion (MI) [1, 5].

Weak inversion occurs when the device is operating at a sufficiently low effective gate–source voltage ($V_{EFF} = V_{GS} - V_{TH} < -72mV$), where the gate–source voltage, V_{GS}, is below the threshold voltage, V_{TH}, by at least $72mV$ for a typical bulk CMOS process. In this region, the channel is weakly inverted and drain diffusion current dominates. MOS drain current in weak inversion is proportional to the exponential of the effective gate–source voltage. Weak inversion drain current in saturation is approximated by [7]:

$$I_D = 2n\mu C'_{ox} U_T^2 (\frac{W}{L}) e^{\frac{V_G - nV_s - V_{TH}}{nU_T}}, \tag{2.1}$$

where n is the substrate factor, μ is the low field mobility, C'_{ox} is the gate-oxide capacitance per unit area, and $U_T = kT/q$ is the thermal voltage ($q = 1.602\,10^{-19}$ is the magnitude of electron charge, $k = 1.3086\,10^{-23}$ is the Boltzmann constant). Parameters W and L describe the effective width and length of the device respectively.

Strong inversion occurs for MOSFETs operating at sufficiently high effective gate–source voltages $V_{EFF} = V_{GS} - V_{TH} < -225mV$ where the gate–source voltage is above the threshold voltage by at least $225mV$. The channel is strongly inverted and drain drift current dominates. Strong inversion drain current, excluding small-geometry effects like velocity saturation and vertical field mobility reduction, is proportional to the square of the effective gate–source voltage. It is approximated by [7]:

$$I_D = 2n\mu C'_{ox} U_T^2 (\frac{W}{L})(V_G - nV_S - V_{TH})^2. \tag{2.2}$$

In Linear region of operation for both weak and strong inversion can be approximated by [7]:

$$I_D = (\mu C'_{ox})(\frac{W}{L})[V_G - V_{TH} - \frac{n}{2}(V_D + V_S)](V_D - V_S). \tag{2.3}$$

The inversion coefficient, I_C, is a numerical measure of the channel inversion, which depends on the applied bias voltage at the MOS terminals. In other words, the I_C is a normalized number that is proportional to the quantity of free carriers in the channel region. The selection of the I_C enables design within weak, moderate or strong inversion operation. Values of I_C less than 0.1 correspond to weak inversion and values above 10 in strong inversion. For values between 0.1 and 10 the transistor is operating in the transition region called moderate inversion (MI) [8].

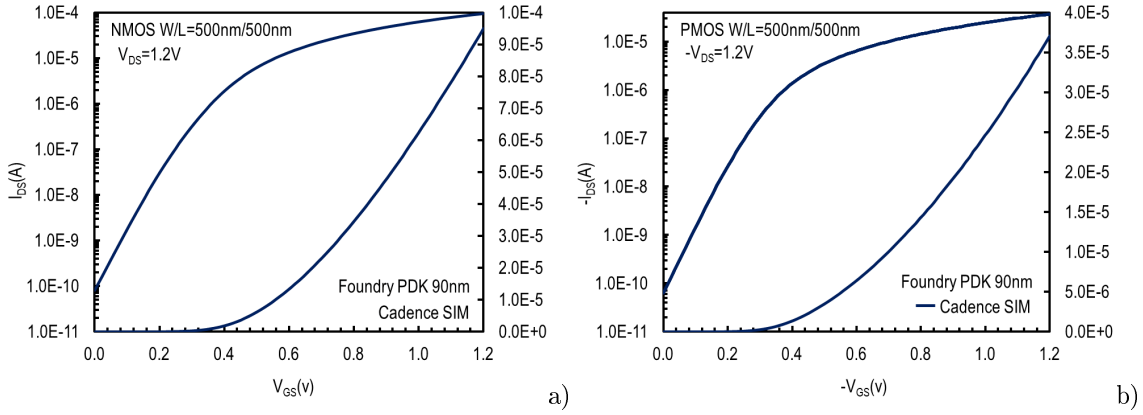
3 Technology parameters extraction

MOSFET parameters are fundamental for the correct analysis, design, and simulation of MOS circuits. The accuracy of the transistor characteristics depends not only on a good device model but also on the accuracy of fundamental parameters. The accurate determination of model parameters plays an important role in device design, process control and technology characterization [9]. Moreover, the transistor model and the associated set of model parameters are extremely important for interfacing integrated circuit designers. The accuracy of the device characteristics and, as a result, the prediction of the performance of a circuit depends not only on the device model but also on the parameter values being used. Therefore, the procedures applied to extract the device model parameters are of major importance. Extracting the values for the full set of design parameters of a MOSFET model is not simple. Difficulties in determining the values for the model parameters exist due to the approximations applied to derive the device model are, in some cases, far from reality and also the accurate determination of a given parameter sometimes depends on the value of another parameter or parameters which is or are not accurately extracted [6].

This chapter describes some procedures to extract fundamental parameters of MOSFET models such as the oxide capacitance C_{ox}, the slope factor n and technology current I_0, the transconductance Parameter K_p and the carrier mobility μ, the transconductance efficiency $\frac{g_m}{I_D}$ and the transit frequency f_T, the intrinsic gain A_V, the early Voltage U_a, the flicker or $1/f$ noise and the current and voltage MOSFET mismatch $\sigma(\frac{\delta I_D}{I_D})$, $\sigma(\delta V_G)$. We simulate and extract the values of all the $65nm$ and $90nm$ design technology parameters. For each parameter, we use a simulation setup which is prepared and we run the simulations in order to understand correctly these two bulk CMOS technologies. For all these simulations, Cadence Virtuoso IC 6.15 was used.

3.1 Simulated transfer and output $I_{DS} - V_{GS}$, $I_{DS} - V_{DS}$ characteristics

In this section typical $I - V$ characteristics of an n-type and a p-type MOSFETs with $W/L = 500nm/500nm$ are presented. Figure 3.1(a)(b) and Figure 3.3(a)(b) show the I_{DS} versus V_{GS} characteristics in saturation ($|V_{DS}| = 1.2V$) from weak to strong inversion for both 90nm and 65nm bulk CMOS technologies. Drain current is depicted on both linear and logarithmic scale. In Figure 3.1(c)(d) and Figure 3.3(c)(d) output characteristic I_{DS} versus V_{DS} are shown for the same devices. In Figure 3.2 and Figure 3.4 transfer and output $I_{DS} - V_{GS}$, $I_{DS} - V_{DS}$ characteristics, parametric sweeped for different V_{DS} and different V_{GS} respectively, are also presented. The schematic of the circuit used to derive these results is shown in Figure 3.33.



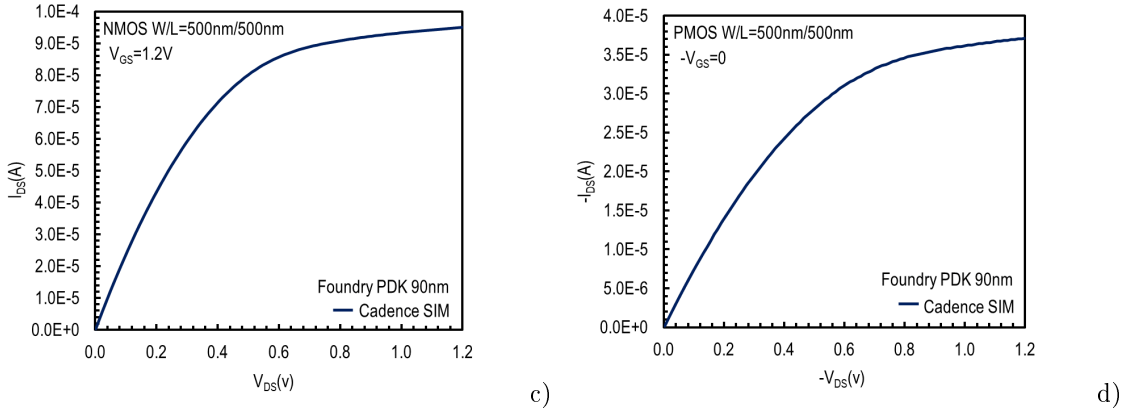


Figure 3.1: Simulated transfer and output characteristics ($W/L = 500nm/500nm$) for (a), (c) n-type and (b), (d) p-type MOSFETs of 90nm bulk CMOS process.

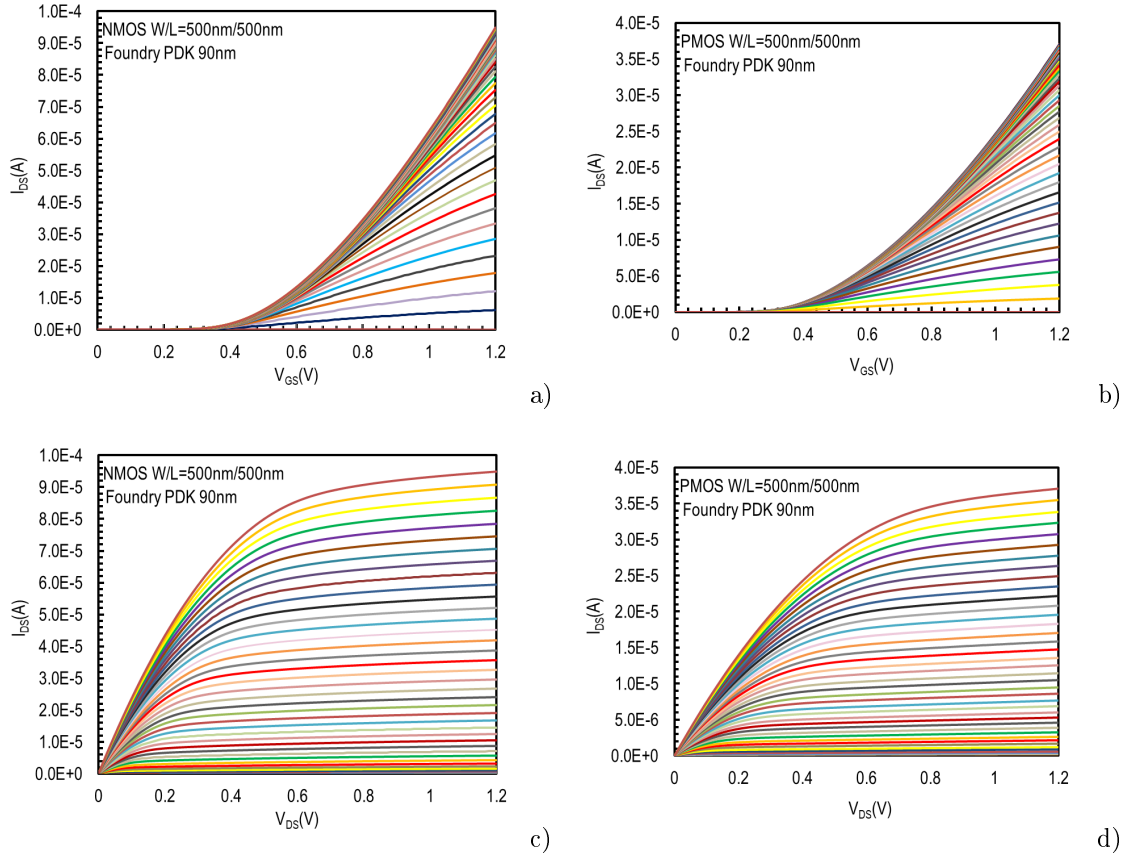


Figure 3.2: Simulated I_{DS} vs. V_{GS} (parametric sweep for different V_{GS}) and I_{DS} vs. V_{DS} (parametric sweep for different V_{DS}) characteristics ($W/L = 500nm/500nm$) for (a), (c) n-type and (b), (d) p-type MOSFETs of 90nm bulk CMOS process.

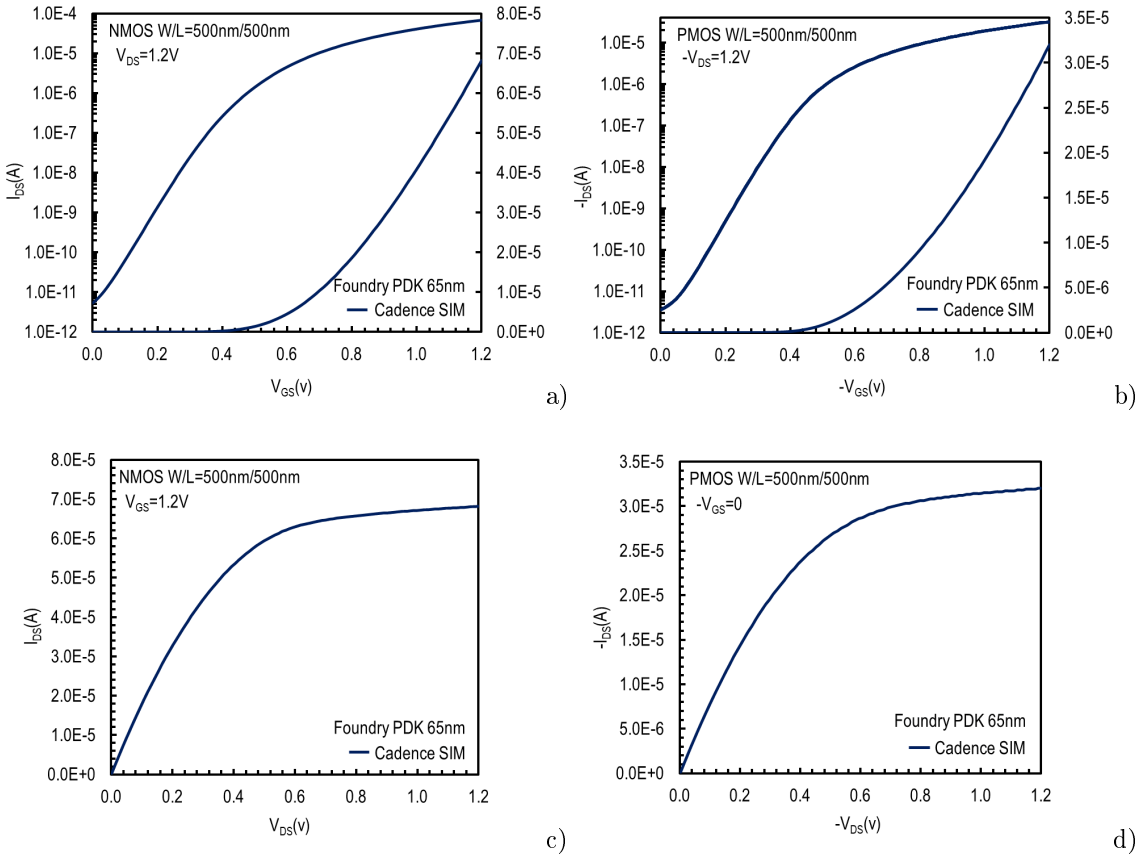


Figure 3.3: Simulated transfer and output characteristics ($W/L = 500nm/500nm$) for (a), (c) n-type and (b), (d) p-type MOSFETs of 65nm bulk CMOS process.

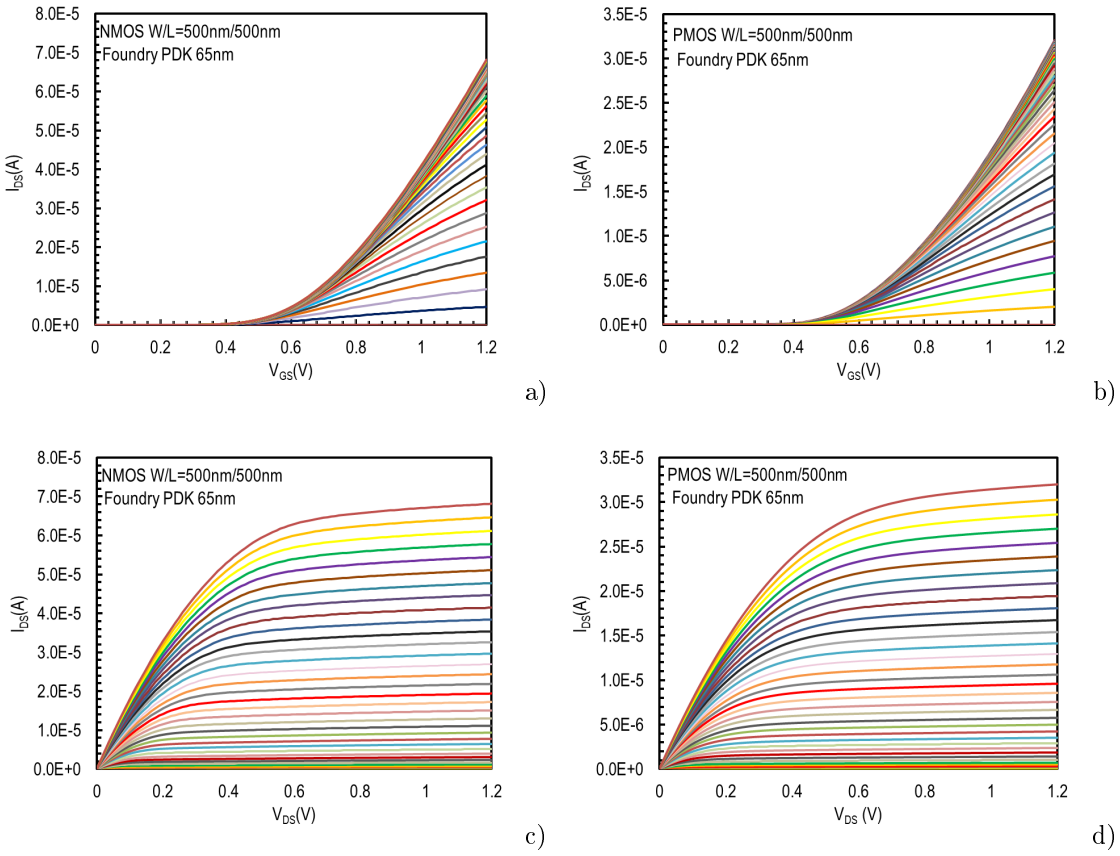


Figure 3.4: Simulated I_{DS} vs. V_{GS} (parametric sweep for different V_{GS}) and I_{DS} vs. V_{DS} (parametric sweep for different V_{DS}) characteristics ($W/L = 500nm/500nm$) for (a), (c) n-type and (b), (d) p-type MOSFETs of 65nm bulk CMOS process.

3.2 Oxide capacitance C_{ox} extraction

3.2.1 MOSFET dependency of gate-source voltage V_{GS}

In order to define C_{ox} we have to investigate the behavior of the MOSFET as a function of the gate bias. The modes of operation as a function of applied V_{GS} is typically divided into three regions. These regions are called accumulation, depletion and inversion. The transitions are however not abrupt. The MOS capacitor principle will be examined, to particularly show the impact V_{GS} has on the charge concentration in bulk.

Accumulation region (device off) Within the p-type substrate there is an excess of positive, majority carriers. By applying a negative gate voltage, these positive majority carriers are attracted toward the oxide-to-substrate interface. The holes accumulate, and an accumulation layer is thus created as we can observe in the Figure 3.5. Any free negative minority carriers in the substrate are on the other hand repelled further away from the junction. Therefore, the device is off, and the resulting electric field in the gate oxide is directed upward against the gate [10].

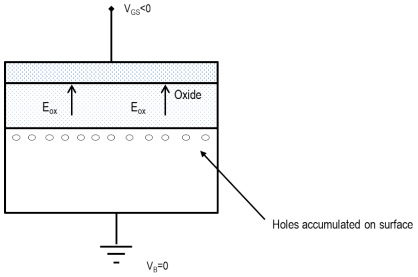


Figure 3.5: p-type MOS capacitor in accumulation region.

Depletion region (device in intermediate state)

If a small, positive gate voltage is applied, the situation turns opposite. Now the positive majority carriers are pushed out of the accumulation layer and deeper into the substrate, leaving ions of negative charge fixed in the silicon lattice. The gate bias at which the substrate semiconductor eventually reaches neutrality all over is called the flatband voltage V_{FB}. Any increase in gate voltage beyond V_{FB} causes the silicon lattice region near the bulk-to-oxide interface to become depleted from holes. This stand-off between positive gate voltage and negative ion charge near the bulk-to-oxide interface thus creates a depletion region, where there are almost no positive majority carriers left as it shown in Figure 3.6. That is, they will balance the charge of each other. This depletion region grows down into the volume of the semiconductor with increasing gate voltage. The resulting electric field in the gate oxide is directed downward against the substrate. At some point the depletion region prevails the gate voltage, and therefore stops increasing in volume. The rest of the p-type substrate is however neutral [10].

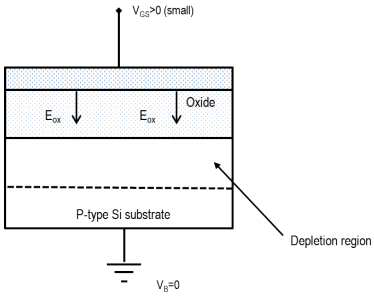


Figure 3.6: p-type MOS capacitor in depletion region.

Inversion region (device on)

If the applied gate voltage is further increased, negative minority carriers from the substrate are attracted toward the bulk-to-oxide interface. These negative minority carriers are a result of the positive majority carriers that were repelled deep into the substrate during depletion. Since the number of positive majority carriers in the p-type substrate increase due to repulsion from the bulk-to-oxide interface, negative minority carriers must be generated to maintain neutrality. Finally a continuous n-type channel region becomes present at the bulk-to-oxide interface under gate, consisting of negative minority carriers that were just created. The semiconductor material near the bulk-to-oxide interface is said to be inverted, since it now has a hole-to-electron concentration similar to that of an n-type

material. The device is at present thus in inversion region as shown in Figure 3.7. The depleted area below the channel is still present irrespective of the conducting channel, but it does not increase. Instead, the increase in gate voltage is balanced by the increase in attracted negative minority carriers. The gate voltage at which this channel is created is called the threshold voltage V_{TH} as mentioned in section 2.2. The actual threshold voltage is determined by the doping profile of the substrate. The resulting electric field is still directed downward against the substrate. It is common to divide this region into the two sub-regions weak inversion and strong inversion, which refer to the regions before and after Vth respectively. Hence the threshold voltage indicates the point at which strong inversion is reached.By adding n-type drain and source diffusions on each side of the MOS capacitor structure, the charge concentration at the bulk-to-oxide interface described above determines the condition between these two diffusions. When the device is off, the p-type region between the two diffusions acts as a barrier since it is of opposite polarity. But when the channel is present, the charge concentration at the bulk-to-oxide interface is on the other hand of the same polarity as that of the diffusions. Hence there is a direct path between drain and source where current may flow, since these minority carriers are mobile [10, 12].

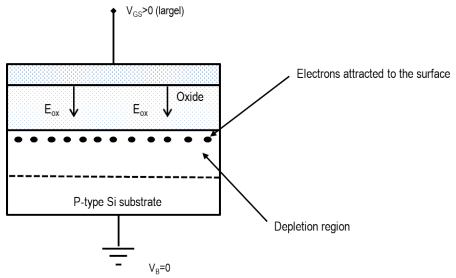


Figure 3.7: p-type MOS capacitor in inversion region.

3.2.2 MOSFET parasitic capacitances

The parasitic capacitances of the MOSFET make up an important part of the total parasitic capacitance of a specific design in addition to the interconnect delays. Analysis of MOSFET parasitic capacitances is also an often-used method for characterizing a specific MOSFET technology. This is done by measuring the MOSFET equivalent capacitance, and from this vital information can be extracted. Among the MOSFET device and process parameters which can be found from CV measurements are gate oxide thickness t_{ox} and threshold voltage V_{TH}. Capacitances associated with the MOSFET is typically classified into two major groups: oxide-related capacitances and junction capacitances. The former comes as a consequence of the gate oxide acting as a dielectric between various electrodes of the MOSFET, and will be discussed in section 3.2.3. While the latter is a result of the depletion region formed between the p-n junctions within the semiconductor material, acting as a dielectric between the diffusions and bulk. Junction capacitances will not be studied as part of this thesis [14].

3.2.3 The MOS capacitor

A simplistic drawing of a silicon-based MOS Capacitor is shown in Figure 3.8. It consists of doped silicon as the substrate, a gate electrode made of polycrystalline silicon, and silicon dioxide (symbol SiO_2) to separate gate from the substrate. The MOS capacitor actually consists of two different capacitors. These are the gate capacitance per unit area C'_{ox} and the channel junction capacitance C_{jc}. The dielectric of C'_{ox} is the always existing gate oxide, while the dielectric of C_{jc} is the depleted region created in the semiconductor during depletion. We can also define,

$$C'_{ox} = \frac{\varepsilon SiO_2}{t_{OX}} \tag{3.1}$$

where εSiO_2 is the permittivity of silicon dioxide and t_{ox} is the oxide thickness[15].

By assuming a unit sized MOS capacitor, C'_{OX} is shared between various electrodes according to the mode of operation:

- C_{gg}: is the total capacitance of a MOS capacitor seen from the gate,
- C_{gb}: is the capacitance between gate and body (Substrate).

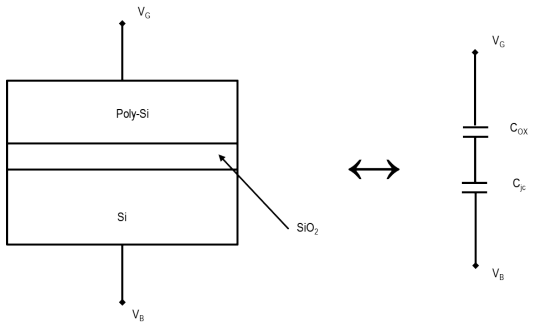


Figure 3.8: Equivalent circuit for the capacitances represented by the MOS Capacitor.

3.2.4 MOSFET Oxide-related capacitances and C_{OX} extraction methodology

The MOSFET oxide-related capacitances arise mainly due to a decomposition of the MOS capacitor total gate capacitance C_{gg}. We expect that a capacitance exists between every two of the four terminals of a MOSFET as shown in Figure 3.9. The value of each of these capacitances depend on the the region of operation for the MOSFET as we discussed in the section 3.2.1 for the MOS capacitor [5].

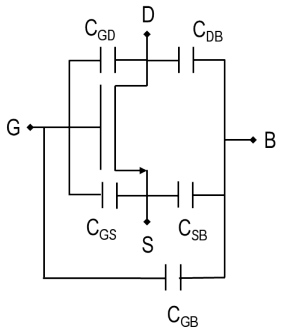


Figure 3.9: MOS capacitances.

Consider the terminal connections of n-channel MOSFET shown in Figure 3.9, a bias is applied to the gate terminal. Depending upon the gate bias there are different regions of operation in C-V curve that are accumulation, depletion and inversion as described in details for the MOS capacitor

in section 3.2.1.So, in accumulation region of operation the gate to source bias is negative because of the holes from the substrate are attracted under the gate region as described above.Therefore, there are three types of capacitances are involved that are capacitance between gate electrode and substrate (C_{gb}), capacitance between gate and drain terminals (C_{gd}) and capacitance between gate and source terminals (C_{gs}). In case that, V_{GS} is positive but less than V_{TH} for some terminal biases, the surface under the gate is depleted because the holes under the gate are displaced and leave negative immobile ions that contribute to negative. In this region of operation the capacitance between the gate and the source/drain is simply overlap capacitance while the capacitance between the gate and substrate is the oxide capacitance in series with depletion capacitance of the formed of depletion region. The MOSFET operated in this region is said to be in weak inversion or the sub threshold region. Finally, when V_{GS} is sufficiently positive and is larger than V_{TH} then a large number of electrons are attracted under the age and the surface is said to be inverted. In integrated circuits the capacitor based on MOSFETs are designed in this region of operation. As a result, from the Figure 3.10 which shows the total gate capacitance C_{gg} versus the gate voltage V_G we can assume that C_{OX} is extracted from the inversion part of this plot [16]. Also, we can define C'_{OX} by deviding C_{OX} by the aspect ratio W/L,

$$C'_{OX} = \frac{C_{OX}}{WL} \tag{3.2}$$

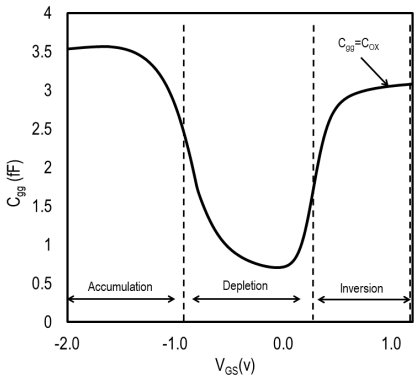


Figure 3.10: C_{gg} vs. V_G - NMOS transistor C_{OX} extraction methodology.

3.2.5 Simulation and results

In this section, simulated gate capacitance c_{gg} vs. gate voltage V_G for $W/L = 500nm/500nm$ in saturation ($\mid V_{DS} \mid = 1.2V$) for NMOS and PMOS of 65nm, 90nm bulk CMOS technologies are presented in Figure 3.11. Also, from the schematic of the circuit in Figure 3.34 and following the extract methodology mentioned above, we can see a summary of the results for the simulated PDKs in the Table 1.

Parameter	Simulated (PDK 90nm)	Simulated (PDK 65nm)	Unit
C_{OX} (NMOS) / C'_{OX} (NMOS)	3.07/12.3	3.37/13.5	fF / $^{\text{fF}}/_{\mu\text{m}^2}$
C_{OX} (PMOS) / C'_{OX} (PMOS)	2.93/11.7	3.14/12.6	fF / $^{\text{fF}}/_{\mu\text{m}^2}$

Table 1: C_{OX}, C'_{OX} simulated values for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.

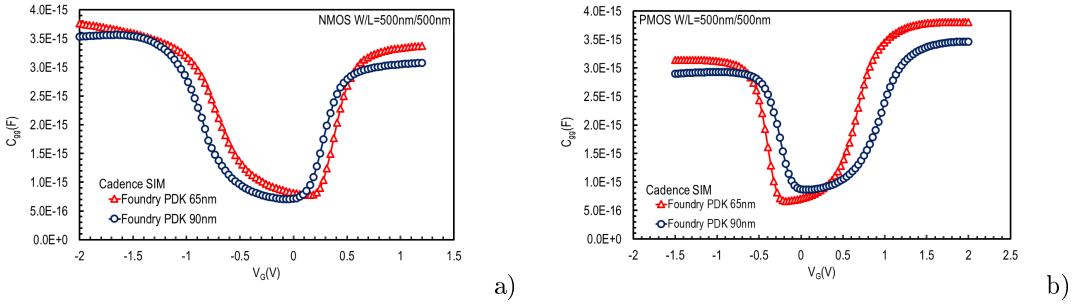


Figure 3.11: Simulated gate capacitance c_{gg} vs. gate voltage V_G ($W/L = 500nm/500nm$) in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.

3.3 Slope factor n and technology current I_0 extraction

3.3.1 Slope factor n definition

One more parameter for the characterization of MOS transistors is the slope factor or weak inversion slope n. The "ideal" slope factor is equal to one, the bulk MOS transistor, however, is characterized by a slope factor a few percent to tens of percent higher than one with nominal values from 1.2 to 1.7 depending on the bulk CMOS process. The reason for the deviation from the ideal slope factor in the bulk transistor is that a change in the gate voltage is not only accompanied by a change in the inversion charge but also by a change in the bulk charge [6]. The amount of substrate factor n appears to affect the current flow through MOSFET in all operating areas. Using n we try to approximate the effect of the substrate on the electric field that develops between the gate and the channel. The substrate coefficient is defined as shown below,

$$n \equiv \frac{\partial V_G}{\partial V_P} = 1 + \frac{\gamma}{2\sqrt{V_P + \phi}} \tag{3.3}$$

where, ϕ is the approximation of the surface potential, γ is the is the body effect factor and V_P is the pinch off voltage which corresponds to the value of the channel potential V_{ch} for which the inversion charge becomes zero in a non-equilibrium situation. The pinchoff voltage mainly depends on gate potential V_G and an effective approximation could be,

$$V_P \cong \frac{V_G - V_{TO}}{n}, \tag{3.4}$$

where V_{TO} is the threshold voltage at $V_S = 0$ [17, 18].

3.3.2 Technology current I_0 definition

A key design parameter in analog CMOS design done in submicron CMOS technology is the MOSFET inversion coefficient I_C (Inversion Factor). A design methodology that is based on the universal shape of the transconductance efficiency $\frac{g_m}{I_D}$ vs. I_C curve is very common and we will analyze it further in section 3.4. I_C is I_D, the DC drain current of the MOS device, normalized by the shape factor W/L which is also known as the MOSFET aspect ratio and a fixed process technology current I_0 [7],

$$i_C = \frac{I_D}{I_0(\frac{W}{L})}, \tag{3.5}$$

where

$$I_0(\frac{W}{L}) = I_{SPEC}, \tag{3.6}$$

I_{SPEC} is the normalization factor for the current, which is named specific current. We also know that

$$I_0 = 2nU_T^2 \mu C'_{OX}. \tag{3.7}$$

When $W = L$, from 3.7,

$$I_0 = I_{SPEC} \tag{3.8}$$

.

3.3.3 Slope factor n and technology current I_0 extraction methodology

Both, the specific current I_0 and slope factor n need to be calculated. This can be done in various ways. We will demonstrate the approach which exploits the characteristics of the normalized transconductance-to-current ratio $\frac{g_m U_T}{I_D}$. We know that when $W = L$, specific current I_{SPEC} is equal to the technology current I_0. We also know that, in saturation, there is a direct relation between the normalized tranconductance-to-current ratio and the drain current,

$$\frac{g_m U_T}{I_D} = \frac{1}{\sqrt{\frac{1}{4} + \frac{I_D}{I_{SPEC}}} + \frac{1}{2}}, \tag{3.9}$$

setting $\frac{I_D}{I_{SPEC}} = 1$,

$$\frac{1}{\sqrt{\frac{1}{4} + \frac{I_D}{I_{SPEC}}} + \frac{1}{2}} = 0.618,$$

So,

$$I_0 = 0.618((\frac{g_m U_T}{I_D})|_{max}. \tag{3.10}$$

Finally, slope factor n is can extracted from the maximum $\frac{g_m U_T}{I_D}$ vs. I_D plateau in weak inversion according to,

$$n = \frac{1}{\left(\frac{g_m U_T}{I_D} \mid_{max}\right)} \tag{3.11}$$

Figure 3.12 demonstrates normalized transconductance-to-current ratio $\frac{g_m U_T}{I_D}$ vs. drain current I_D $(W/L = 1)$, with the x-axis in logarithmic scale in order to show how specific current I_{SPEC} and slope factor n are extracted.

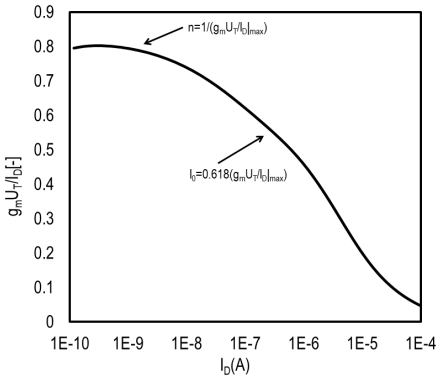


Figure 3.12: $\frac{g_m U_T}{I_D}$ vs. $I_D(W/L = 1)$ - NMOS transistor n, I_0 extraction methodology.

3.3.4 Simulation and results

In this section, Figure 3.13 shows the simulated normalized transconductance-to-current ratio $\frac{g_m U_T}{I_D}$ vs. drain current I_D ($W/L = 500nm/500nm$) in saturation ($\mid V_{DS} \mid = 1.2V$) for NMOS and PMOS of 65nm, 90nm bulk CMOS technologies. Also, from the schematic of the circuit in Figure 3.35 and following the extract methodology described above, we can see a summary of the results for the simulated PDKs in the Table 2.

Parameter	Simulated (PDK 90nm)	Simulated (PDK 65nm)	Unit
n_n (NMOS)	1.24	1.25	–
n_p (PMOS)	1.22	1.24	–
$I_{0,n}$ (NMOS)	630	390.25	nA
$I_{0,p}$ (PMOS)	330	346	nA

Table 2: n, I_0 simulated values for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.

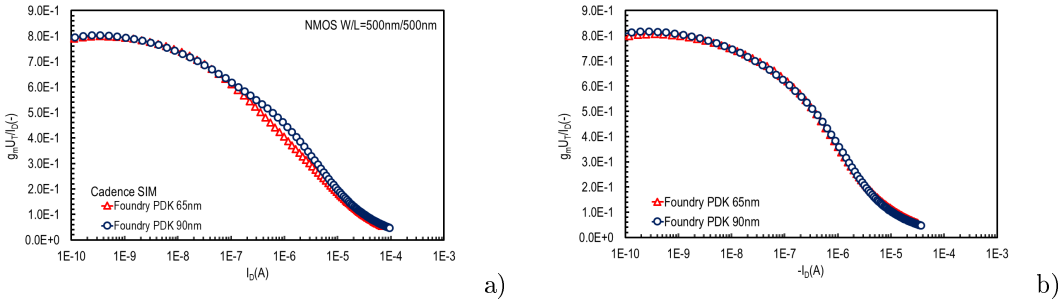


Figure 3.13: Simulated normalized transconductance-to-current ratio $\frac{g_m U_T}{I_D}$ vs. dran current I_D ($W/L = 500nm/500nm$) in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.

Both technologies show similar trend and weak inversion plot prediction. In the case of NMOS devices a slight difference is noticed in moderate inversion whereas in the case of PMOS, the weak inversion slope is almost identical in all cases.

3.4 Carrier mobility μ and transconductance parameter K_p

3.4.1 Carrier mobility μ definition

One of the most important parameters for all semiconductor devices is the mobility of the carrier flowing inside the channel. Their mobility, also known as their ability to move through the crystal, will define the electrical performances of the device. The mobility is consequently a paramount parameter, and its good knowledge is of prime importance to first understand the physics underlying the conduction mechanisms inside semiconductor devices and second to be able to model and simulate a single transistor and in turn more complex circuits. Carrier mobility μ, in MOSFET transistors is a factor which refers to the mobility of electrons and holes in the channel between drain and source terminals. The effective mobility as a function of electric field, substrate doping, and temperature is used

to determine the various mobility components (surface roughness, phonon, and coulombic scattering limited mobility components. Therefore, the channel mobility μ can be calculated from [22, 23]:

$$\frac{1}{\mu} = \frac{1}{\mu_C} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}}, \tag{3.12}$$

where $\mu_{C,}\mu_{PH,}\mu_{SR}$ are the mobility components mentioned above.

3.4.2 Transconductance parameter K_p definition

The process transconductance Parameter K_P is a constant that depends on the process technology used to fabricate an integrated circuit. Therefore, all the transistors on a given substrate will typically have the same value of this parameter [1]. The transistor's transconductance parameter K_P is obtained by multiplying mobility μ by the oxide capacitance C'_{OX},

$$K_P = \mu C'_{OX}. \tag{3.13}$$

3.4.3 Transconductance parameter K_p and carrier mobility μ extraction methodology

In order to extract transconductance parameter K_p in saturation, we can use the following sequence of equations:

$$I_D = \frac{\beta}{2n}[V_G - V_{TO} - nV_S]^2 \tag{3.14}$$

and by applying the derivative of V_G over $\sqrt{I_D}$ the result is:

$$\frac{\partial\sqrt{I_D}}{\partial V_G} = \frac{\sqrt{\beta}}{2n}. \tag{3.15}$$

Furthermore,

$$\beta = \mu C'_{OX}\frac{W}{L} \tag{3.16}$$

and from 3.13, 3.16, solving for K_P, the initial equation becomes,

$$K_P = (\frac{\partial\sqrt{I_D}}{\partial V_G})^2 2n\frac{L}{W}. \tag{3.17}$$

Finally, we can easily derive mobility μ from the equation 3.13 as follows,

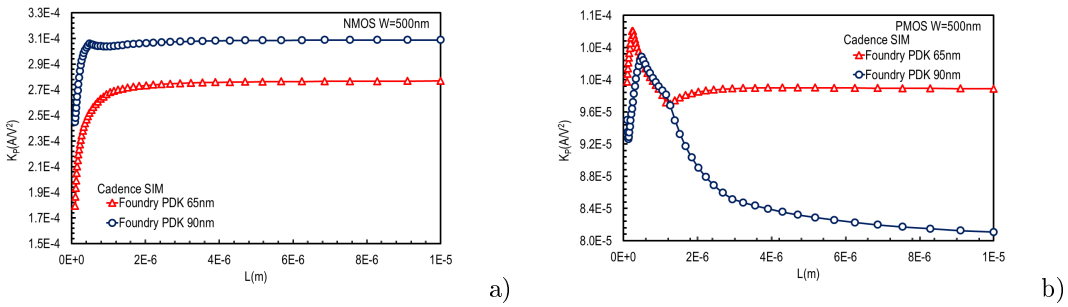
$$\mu = \frac{K_P}{C'_{OX}}. \tag{3.18}$$

3.4.4 Simulation and results

In this section, Figure 3.14, shows simulated transconductance parameter K_p vs. channel length L in saturation ($\mid V_{DS} \mid = 1.2V$) for NMOS and PMOS of 65nm, 90nm bulk CMOS technologies. The schematic of the circuit used to derive these results is depicted in Figure 3.36 and the summary of the results are also found in the Table 3.

Parameter	Simulated (PDK 90nm)	Simulated (PDK 65nm)	Unit
$K_{P,n}$ (NMOS)	306	252	$\frac{\mu A}{V^2}$
$K_{P,p}$ (PMOS)	103	102	$\frac{\mu A}{V^2}$
μ_n (NMOS)	249	187	$\frac{cm}{Vs}$
μ_p (PMOS)	88	81	$\frac{cm}{Vs}$

Table 3: K_P,μ simulated values for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.



a) b)

Figure 3.14: Simulated transconductance parameter K_p vs. channel length L ($W = 500nm$) in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.

For the n-type MOSFETs, the 90nm PDK predicts higher K_p values versus channel length L, when compared to the 65nm PDK. The p-type devices show the opposite behavior towards higher channel lengths. Therefore mentioned differences can be partially attributed to the different C_{ox} values predicted from the the tow different pdk 's. It has to be mentioned than in all cases, as expected, the K_p values are approximately ~ 3 times higher for n-type MOS devises when compared to those of the PMOS counter parts.

3.5 Transconductance efficiency $\frac{g_m}{I_D}$ and transit frequency f_T extraction

3.5.1 MOS Transconductance g_m definition

A MOSFET operating in saturation produces a current in response to its gate-source overdrive voltage, which is is defined as the voltage between transistor gate and source V_{GS} in excess of the threshold voltage V_{TH} where V_{TH} is defined as the minimum voltage required between gate and source to turn the transistor on as it is referred above. So it would be useful to define a figure of merit that indicates how well a device converts a voltage to a current. More specifically, since in processing signals, we're interested in the changes in voltages and currents, we define the figure of merit (FoM) as the change in the drain current divided by the change in the gate-source voltage. This is called transconductance and usually defined in the saturation region, denoted by g_m,

$$g_m = \frac{\partial I_D}{\partial V_{GS}}|_{V_{DS}const.} \cong \tag{3.19}$$

$$K_P \frac{W}{L}(V_{GS} - V_{TH}). \tag{3.20}$$

Therefore, g_m sets the sensitivity of the device, for a high g_m, a small change in V_{GS} results in a large change in I_D. The SI unit, the Siemens, with the symbol, S, 1 Siemens = 1 ampere per volt replaced the old unit of conductance, having the same definition, the (ohm spelled backwards), symbol,℧. In analog design, we sometimes say a MOSFET operates as a "transconductor" to indicate that it converts a voltage change to a current change. So, g_m in the saturation region is equal to [5],

$$g_m \cong K_P \frac{W}{L} V_{OV}, \tag{3.21}$$

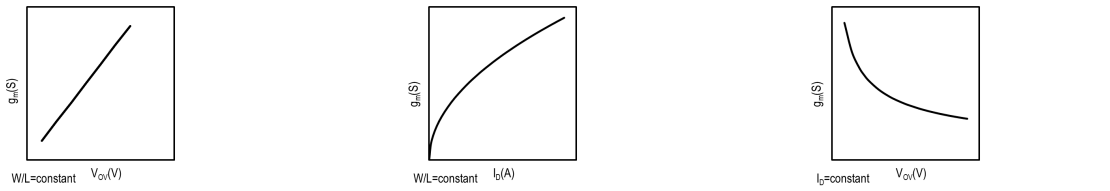
from the following approximate equation for the drain current

$$I_D = \frac{K_P}{2} \frac{W}{L}(V_{GS} - V_{TH})^2, \tag{3.22}$$

we can define again g_m as,

$$g_m \cong \sqrt{2K_P(\frac{W}{L})|I_D|} \cong \tag{3.23}$$

$$\frac{2I_D}{V_{OV}}. \tag{3.24}$$



a) b) c)

Figure 3.15: Approximate MOS transconductance as a function of overdrive and drain current.

We can easily obsverve that, g_m increases with the overdrive if W/L is constant, whereas 3.24 implies that g_m decreases with the overdrive if I_D is constant.

3.5.2 Transit frequency f_T definition

Transit frequency f_T is defined as the frequency at which the extrapolated small-signal current gain of the transistor in CS configuration falls to unity. f_T is a widely used metric for characterizing the high-frequency behavior of a MOSFET because many performances, such as the gain and the minimum noise factor, are directly linked to f_T. A good approximation of f_T is given by [26],

$$f_T = \frac{g_m}{2\pi C_{gg}}, \tag{3.25}$$

where C_{gg} is the total gate capacitance. Both g_m and C_{gg}, are bias dependent, so f_T is bias dependent too. So, we can express f_T as a function of inversion factor and channel length as follows,

$$f_T = \frac{\mu U_T}{2\pi L_{eff}^2}(\sqrt{1+4I_C}-1). \tag{3.26}$$

Therefore, from 3.26 we can easily conclude that, assuming a constant mobility, f_T increases linearly with I_C in weak inversion before increasing with $\sqrt{I_C}$ in strong inversion and also for a given I_C, f_T decreases as $1/L^2$ with increasing channel length for all regions of operation.

3.5.3 Transconductance efficiency $\frac{g_m}{I_D}$ extraction as a Figure of Merit (FoM)

The transconductance efficiency $\frac{g_m}{I_D}$ FoM is one of the most important performance metrics for analog circuit design. It is a measure of how much transconductance is produced for a given bias current and is a function of I_C. The transconductance efficiency (or its inverse) appears in many expressions related to the power optimization of analog circuits. In the normalized form, we have already used it in section 3.3.3 in order to extract slope factor n and technology current I_0[26]. We can easily extract the transconductance efficiency if we simply divide the equation 3.19 with the drain current. We plot transconductance efficiency relative to the inversion coefficient I_C, which is defined by the equation 3.5. The shape of the transconductance efficiency curve is universal for MOS operation as it shown in Figure 3.16 and is channel length and process independent until velocity saturation effects reduce transconductance efficiency. These characteristics provide important information to the designer, and they also constitute particularly difficult benchmark tests for the accuracy and adequacy of compact MOS models.

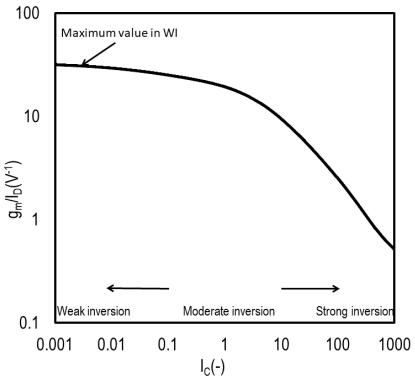


Figure 3.16: NMOS transistor transconductance efficiency $\frac{g_m}{I_D}$ (in log-log scale) typical representatation.

3.5.4 Transconductance efficiency multiplied by transit frequency $\frac{g_m f_T}{I_D}$ extraction as a Figure of Merit (FoM)

Both $\frac{g_m}{I_D}$ and f_T are very important FoMs of analog/RF design. The former characterizes the dc performance of a device while the latter characterizes its high-frequency performance. Nevertheless, exists a fundamental tradeoff between the two. Aiming for low-power operation by targeting a high $\frac{g_m}{I_D}$ at small values of I_C invariably means compromising in speed (bandwidth). This is where the FoM defined as the product of the two formerly defined metrics comes into the picture. Combining two quantities that have their maxima on the opposite ends of the I_C axis, the $\frac{g_m f_T}{I_D}$ FoM serves as design guide to locate the optimum I_C. Figure 3.17 shows a behavior that makes it useful for locating the optimum I_C. This maximum is peak lies at the higher end of the MI region for the contemporary CMOS technologies and moves deeper into the MI region with decreasing channel lengths [26].

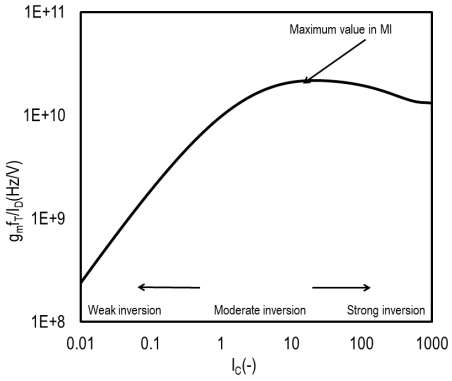


Figure 3.17: NMOS transistor transconductance efficiency multiplied by transit frequency $\frac{g_m f_T}{I_D}$ (in log-log scale) typical representatation.

3.5.5 Simulation and results

In this section, three different types of transconductance efficiency figures are presented. At first, Figure 3.18 presents the simulated transit frequency f_T vs. inversion coefficient I_C $(W/L = 500nm/500nm)$ from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process. Figure 3.19 shows the simulated transconductance-to-current-ratio $\frac{g_m}{I_D}$ vs. inversion coefficient I_C $(W/L = 500nm/500nm)$ from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process. In Figure 3.21, the simulated transconductance efficiency multiplied by transit frequency $\frac{g_m f_T}{I_D}$ vs. inversion coefficient I_C $(W/L = 500nm/500nm)$ from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process, is also presented. Finally, Figure 3.20 and Figure 3.20 show the transconductance efficiency $\frac{g_m}{I_D}$ vs. inversion coefficient I_C $(W/L = 500nm/500nm)$ from weak to strong inversion in saturation as parametric sweep for different L characteristics $(W/L = 500nm/500nm)$ for (a), (c) n-type and (b), (d) p-type MOSFETs for both 90nm and 65nm bulk CMOS technologies. The schematic of the circuit used to derive these results is depicted in Figure 3.37.

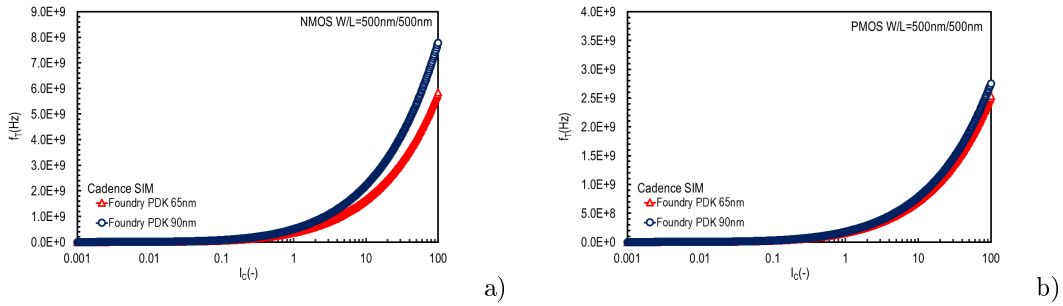
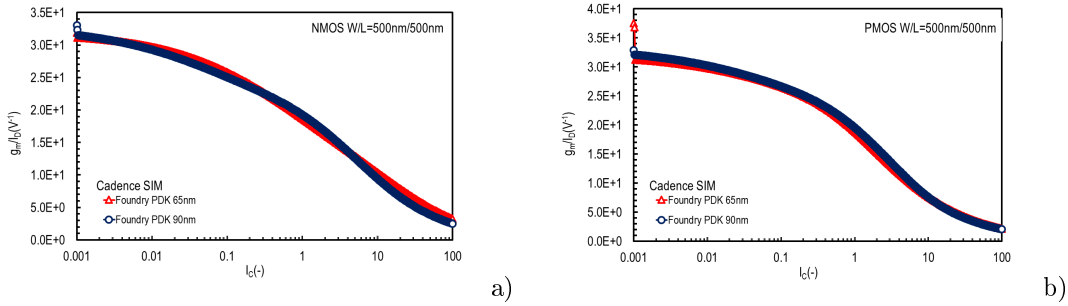
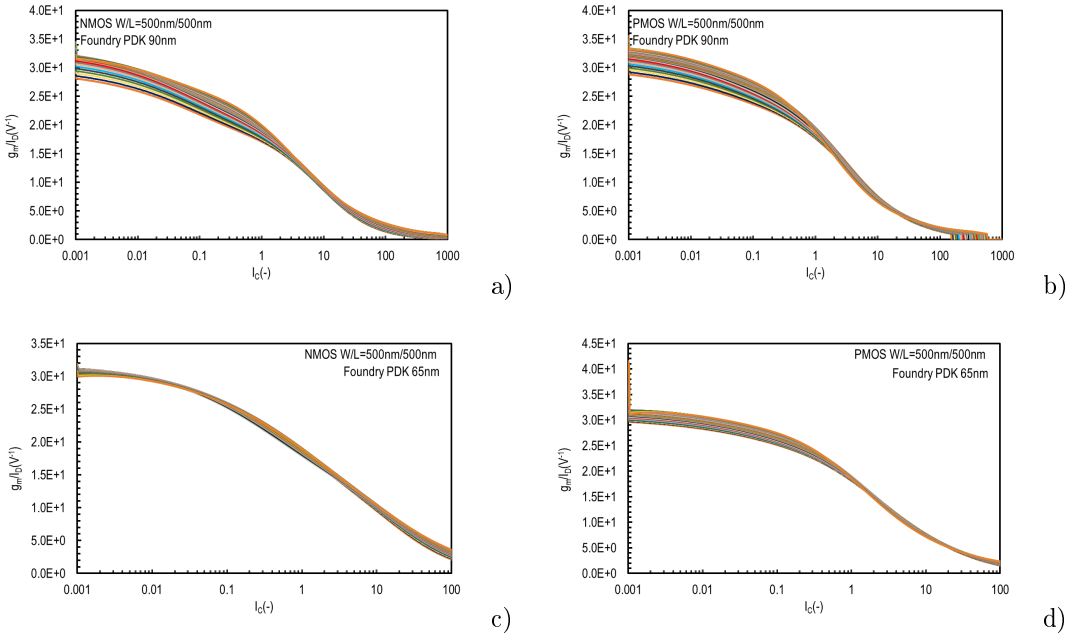


Figure 3.18: Simulated transit frequency f_T vs. inversion coefficient I_C $(W/L = 500nm/500nm)$ from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.



a) b)

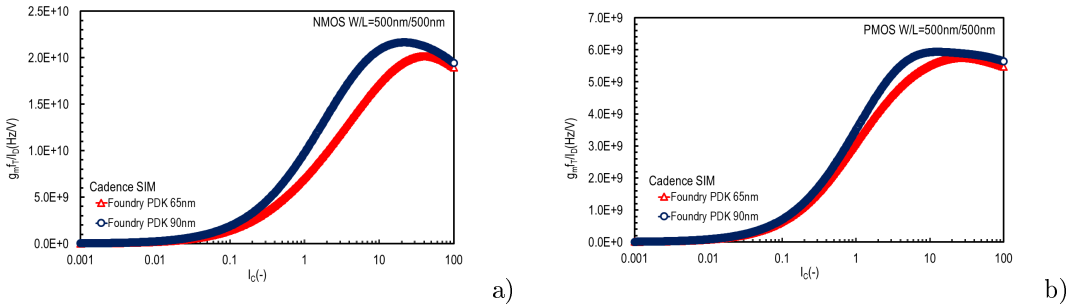
Figure 3.19: Simulated transconductance-to-current-ratio $\frac{g_m}{I_D}$ vs. inversion coefficient I_C ($W/L = 500nm/500nm$) from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.



a) b)

c) d)

Figure 3.20: Simulated transconductance-to-current-ratio $\frac{g_m}{I_D}$ vs. inversion coefficient I_C ($W/L = 500nm/500nm$) from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) (parametric sweep for different L) characteristics ($W/L = 500nm/500nm$) for (a), (c) n-type and (b), (d) p-type MOSFETs of 65nm, bulk CMOS process.



a) b)

Figure 3.21: Simulated transconductance-to-current-ratio multiplied by transit frequency $\frac{g_m f_T}{I_D}$ vs. inversion coefficient I_C ($W/L = 500nm/500nm$) from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.

Transconductance to current ratio in all cases follow the expected behavior. For both n and p-type MOSFETs, the two different PDKs show identical results. The simulated transient frequency presents slightly increased value in the case of the n-type MOSFETs of the 90nm PDK. Therefore, transconductance-to-current-ratio multiplied by transit frequency $\frac{g_m f_T}{I_D}$ present an increased value towards SI for the case of the n-type MOSFETs. It can be noticed that both PDKs predict similar behavior vs.. inversion coefficient (I_C) for the case of p-type MOSFETs.

3.6 Early Voltage U_a extraction

3.6.1 Output conductance g_{ds} in saturation and early voltage definitions

In the design of CMOS analog circuits, the Early voltage (or the output conductance) of a transistor in saturation is a fundamental parameter since it affects, for example, the accuracy of current mirrors and the gain of voltage amplifiers. In the circuit-design-oriented approach, the simplest model of the output conductance assumes it to be proportional to the drain current and inversely proportional to the Early voltage V_A as given below,

$$g_{ds} = \frac{\partial I_D}{\partial V_D} = \frac{I_D}{V_A}. \tag{3.27}$$

V_A is a constant parameter in first-order models. However, a constant Early voltage is inadequate to model the output conductance for the simulation of analog circuits. An improved model of the Early voltage considers it to be proportional to the channel length and independent of both current level and drain voltage,

$$U_a = \frac{V_A}{L}. \tag{3.28}$$

In this case, the output conductance is simply,

$$g_{ds} = \frac{I_D}{U_a L}. \tag{3.29}$$

Even though this model of the output conductance is not accurate, it provides a simple expression to quickly evaluate how the transistor output conductance is affected by the drain current and the channel length [28]. Approximation 3.29 will be extensively used throughout this thesis.

3.6.2 Early voltage U_a extraction methodology

Figure 3.21, illustrates MOS drain–source conductance calculation using the early voltage. A tangent line is drawn touching the I_D versus V_{DS} curve at the bias point (we express the MOS bias point in terms of the inversion coefficient, which is near the onset of strong inversion), and this line intersects

the V_{DS} axis at the early voltage. The drain–source conductance, g_{ds}, is the slope of the tangent line given by the drain bias current, I_D, divided by the sum of the early voltage, V_A, and drain–source bias voltage, V_{DS}. Frequently, as throughout this thesis, V_{DS} is included in V_A as shown in equation 3.27, where g_{ds} is not a constant value for the process, but depends upon the channel length, inversion level, and V_{DS}[7].

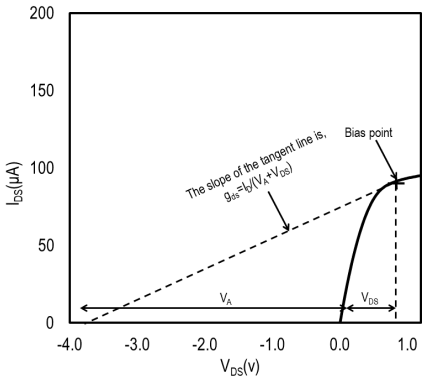


Figure 3.22: I_D vs. $V_{DS}(W/L = 1)$- NMOS transistor U_a extraction methodology.

3.6.3 Simulation and results

In this section, Figure 3.23, shows simulated early voltage U_a vs. channel length L ($W = 500nm$) in saturation ($\mid V_{DS} \mid = 1.2V$) for NMOS and PMOS of 65nm, 90nm bulk CMOS technologies. The schematic of the circuit used to derive these results is depicted in Figure 3.38 and the summary of the results are also found in the Table 4.

Parameter	Simulated (PDK 90nm)	Simulated (PDK 65nm)	Unit
$V_{A,n}$ (NMOS) /$U_{a,n}$ (NMOS)	4.028/8.057	5.18/10.37	mV / $\frac{V}{\mu m}$
$V_{A,p}$ (PMOS) /$U_{a,p}$ (PMOS)	4.024/8.049	6.27/12.53	mV / $\frac{V}{\mu m}$

Table 4: U_a simulated values for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.

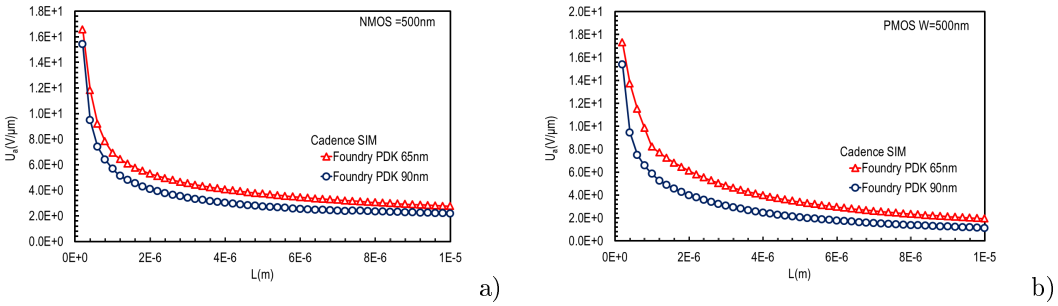


Figure 3.23: Simulated early voltage U_a vs. channel length L ($W/L = 500nm/500nm$) in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.

Early voltage U_a is increased towards shorter channel lengths values in all cases. For both n- and p-type MOSFETs, the 90nm 65nm PDK predicts slightly increased values.

3.7 Intrinsic gain A_V extraction

3.7.1 Intrinsic gain A_V definition and extraction methodology

Maximum gain of a single MOSFET transistor is called intrinsic gain, and is equal to [5],

$$A_V = g_m r_0, \tag{3.30}$$

where g_m is the transconductance as defined above, and r_0 is the output resistance of transistor, which we can easily define as,

$$r_0 = \frac{1}{g_{ds}}. \tag{3.31}$$

So, from the equations 3.19, 3.27 the intrinsic gain of a MOSFET is defined as the ratio,

$$A_V = \frac{g_m}{g_{ds}}, \tag{3.32}$$

dividing both g_{ds} and g_m by drain current and due to the equation 3.29, we conclude that,

$$A_V = \frac{\frac{g_m}{I_D}}{\frac{g_{ds}}{I_D}} = U_a L \frac{g_m}{I_D}. \tag{3.33}$$

Therefore, as we have already extract early voltage and transconductance, we can use the equation 3.33 to extract intrinsic gain as well. Finally, as we can easily observe, intrinsic gain A_V is directly proportional to the channel length of transistors. In amplifiers, one can increase channel length in order to get higher output resistance and gain as well. But, it will also increase parasitic capacitance of transistor, which will limit the bandwidth of amplifier. Channel length of transistors become smaller in modern CMOS technologies, and makes achieving high gain in an amplifier very challenging. In order to achieve high gain, there are many techniques we can follow. In the following sections, we will have a brief look to different topologies of transconductance amplifiers, and their features.

3.7.2 Simulation and results

In this section, Figure 3.24, shows simulated intrinsic gain $A_V = \frac{g_m}{g_{ds}}$ vs. inversion coefficient I_C ($W/L = 500nm/500nm$) from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for NMOS and PMOS of 65nm, 90nm bulk CMOS technologies. The schematic of the circuit used to derive these results is depicted in Figure 3.38. For the given PDKs, the intrinsic gain is shown as a function of the inversion factor. Obviously, longer L provides larger gain. The key point here is to notice that when

transistor operates in the center of moderate inversion, the gain value almost approaches its maximum, and thus it may often be an optimal design choice.

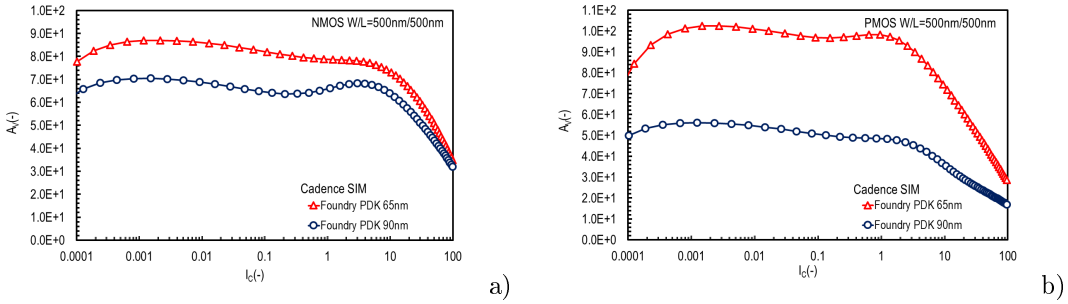


Figure 3.24: Simulated intrinsic gain $A_V = \frac{g_m}{g_{ds}}$ vs. inversion coefficient I_C $(W/L = 500nm/500nm)$ from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.

For the given PDKs, the intrinsic gain is shown as a function of the inversion factor. Obviously, longer L provides larger gain. The key point here is to notice that when transistor operates in the centre of moderate inversion, the gain value almost approaches its maximum, and thus it may often be an optimal design choice. In all cases, the predicted intrinsic gain A_V is improved in the 65nm PDK. For both n- and p-type transistors, the intrinsic gain values is relatively close for PDKs.

3.8 Flicker or $1/f$ noise extraction

3.8.1 Noise in MOSFETs

Noise limits the minimum signal level that a circuit can process with acceptable quality. Today, in terms of analog design we are constantly dealing with the problem of noise because it trades with power dessipation, speed and linearity. In this section, we are going to describe the phenomenon of noise and specifically flicker noise and its effect on analog circuits. Noise is generated in all semiconductor devices and is perceived as spontaneous random fluctuations in current or in voltage [5]. Following a general description of noise characteristics in the frequency and time domains, we can say that in MOSFETs there are several noise mechanisms coming from the channel of the device, related to local random fluctuations of the carrier velocity or the carrier density and they are observed over various frequency ranges [30]. More specifically, we can define four types of noise sources: Thermal noise, low frequency noise (LFN) or 1/f noise, generation-recombination noise (RTS) and Shot noise. Therefore, the total noise is a superinduction of all noise sources. It should also be mentioned that in frequency domain noise can be described by the Power Spectral Density (PSD) which shows how much power a signal carries at each frequency and is expressed in V^2/Hz or $Watt/Hz$ [31].

3.8.2 Flicker or $1/f$ noise definition and extraction methodology

Flicker noise is a low-frequency noise and is probably the most important, and most misunderstood, noise source in CMOS circuit design. Flicker noise is also known as $1/f$ noise pronounced "one over f" because its PSD, as we shall see, is inversely proportional to frequency [4]. The interface between the gate oxide and the silicon substrate in a MOSFET entails an interesting phenomenon, since the silicon crystal reaches an end at this interface, many "dangling" bonds appear, giving rise to extra energy states. As a result, charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing "flicker" noise in the drain current. In addition to trapping, several other mechanisms are believed to generate flicker noise [5]. The average power of flicker noise cannot be predicted easily, depending on the of the oxide-silicon interface, flicker noise may assume considerably different values and as such varies from one CMOS technology to another. The flicker

noise is more easily modeled as a voltage source in series with the gate and, in the saturation region, is given by

$$S_{VG,FLICKER} = \frac{K_F}{C_{OX}^2 W L f^{AF}}, \tag{3.34}$$

where K_F is the flicker noise factor having units of C^2/cm^2 , and AF is the frequency exponent, which has been added to consider the deviation from the ideal $1/f$ slope. K_F typical values ranging from 10^{-33} to 10^{-29} C^2/cm^2 [7].

In order to understand better how we extract flicker noise from total noise diagram, in Figure 3.24 the expected pattern of the drain-referred noise current PSD is depicted.

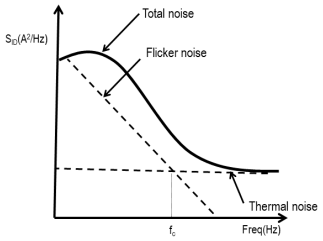


Figure 3.25: Typical drain-referred noise current PSD of a MOSFET.

Thermal noise has no dependence on frequency and so is flat a while low flicker noise, comes with a power spectra density inverse proportional to the frequency and is dominant in frequencies lower than the corner frequency (f_c), where thermal noise and flicker noise have equal PSDs [32, 33]. Flicker noise can be represented as drain current noise source (output referred noise) S_{ID}, or gate voltage noise sources (input referred noise) S_{VG} as shown in Figure 3.26.

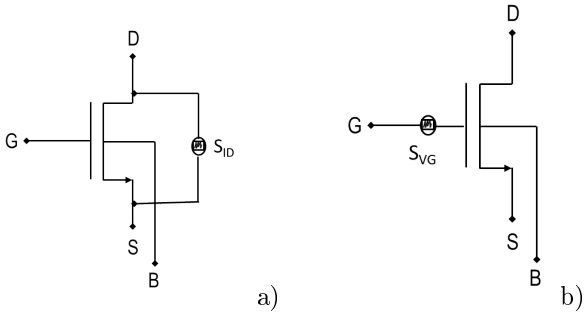


Figure 3.26: MOS noise model showing (a) drain-referred noise current and (b) gate-referred noise voltage sources along with a gate noise current source.

Output noise is measured as in this work and input noise is calculated. The expressions used for the PSD conversion between drain-referred and gate-referred noise sources are,

$$S_{ID} = S_{VG} g_{m^2} (A/\sqrt{Hz}) \tag{3.35}$$

and

$$S_{VG} = \frac{S_{ID}}{g_m^2}(V/\sqrt{Hz}), \tag{3.36}$$

where g_m is the gate transconductance in Siemens.

As standard for noise sources, the noise sources are characterized using the power spectral density (PSD) or noise power in a $1Hz$ bandwidth.

3.8.3 Simulation and results

In this section, Figure 3.27, shows the simulated drain-referred noise noise S_{ID} vs. frequency ($W/L = 500nm/500nm$) from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs for both 90nm and 65nm bulk CMOS technologies. Also, Figure 3.28 presents the simulated gate- referred noise voltage source noise S_{VG} vs. frequency ($W/L = 500nm/500nm$) from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process. The schematic of the circuit used to derive these results is depicted in Figure 3.39.

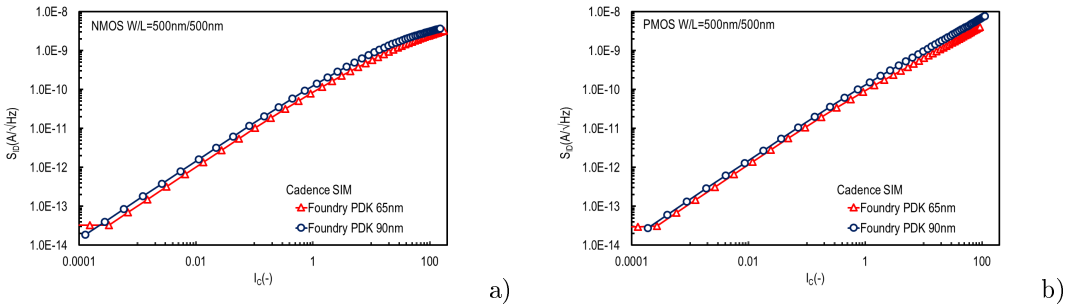


Figure 3.27: Simulated drain-referred noise S_{ID} vs. inversion coefficient in saturation ($\mid V_{DS} \mid = 1.2V$), for (a) n-type and (b) p-type MOSFETs, of 65nm and 90nm bulk CMOS process.

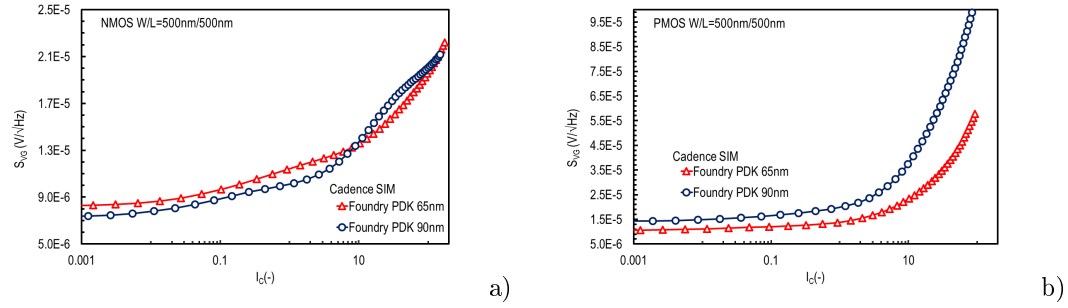


Figure 3.28: Simulated gate-referred noise S_{VG} vs. inversion coefficient in saturation ($\mid V_{DS} \mid = 1.2V$), for (a) n-type and (b) p-type MOSFETs, of 65nm and 90nm bulk CMOS process.

Output noise S_{ID}, follow the expected trend versus inversion coefficient. For both technologies marginally differences can be observed versus the inversion coefficient. Output noise is minimum in weak inversion and increasing to reach its maximum value towards strong inversion. In the case of PMOS devices 90nm PDK predicts bigger LFN values when compared to the 65nm PDK. This can be partially attributed to the minor difference of normalized transconductance efficiency.

3.9 Current and voltage MOSFET mismatch $\sigma(\frac{\delta I_D}{I_D})$, $\sigma(\delta V_G)$ extraction

3.9.1 Mismatch definition

Mismatch is an effect that arises in IC fabrication and is a limiting factor of the accuracy and reliability of many analog and digital integrated circuits. Due to mismatch two equally designed transistors display different electrical behavior. The main reason for the differences is the non-uniformity of process parameters across the wafer. Mismatch affects electrical parameters of the transistor, which in turn differ between two identically devices. Consequently the operating point and other circuit characteristics differ from their desired values [34]. Mismatch is the result of either systematic or stochastic (random) effects. Systematic effects are originated by either uncontrollable variation during the fabrication of the integrated circuit or by poor layout. At the origin of systematic mismatch can be equipment-induced non-uniformities such as temperature gradients and photo-mask size differences across the wafer. Systematic effects are important for large distances and can be combated using appropriate layout techniques. Random mismatch refers to local variation in parameters such as doping concentration, oxide thickness, polysilicon granularity, edge irregularity, etc. The first three fluctuations are called areal fluctuations because they scale with device area while the last one is called peripheral fluctuation because it scales with device perimeter. Random mismatch dominates over systematic mismatch for small distances and is generally assumed to display a Gaussian distribution characterized by its standard deviation. Stochastic mismatch requires a model to orient the I_C designer regarding sizing and biasing strategies [7, 35].

3.9.2 Current and voltage MOSFET mismatch $\sigma(\frac{\delta I_D}{I_D})$, $\sigma(\delta V_G)$ definition and extraction methodology

In order to define current and voltage mismatch we examine two basic MOSFET topologies, a current mirror and a differential pair shown in Figure 3.28.

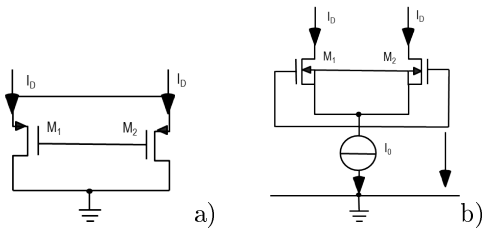


Figure 3.29: Two basic MOSFET topologies: (a) a current mirror and (b) a differential pair.

Theoretically, assuming that V_{T0} and β are uncorrelated, the square root of the normalized variance of the drain current of saturated transistors having the same gate and source voltages as in the current mirror of Figure 3.29(a) is given by,

$$\sigma(\frac{\delta I_D}{I_D}) = \sqrt{\sigma_\beta^2 + (\frac{g_m}{I_D}\sigma_T)^2}, \tag{3.37}$$

where σ_β resulting from the current-factor differences between pairs of transistors $\Delta\beta$ ($\beta = \mu C_{OX} W/L$) and is defined as,

$$\sigma_\beta = \frac{A_\beta}{\sqrt{WL}}, \tag{3.38}$$

the typical values of A_β , which do not change significantly with technology-node scaling [36], range from 1 μm to 3 μm. Also, the threshold voltage differences ΔV_{TO} modeled in the same way, thus,

$$\sigma_T = \frac{A_T}{\sqrt{WL}}. \tag{3.39}$$

The square root of the variance of the gate-voltage mismatch of two saturated transistors having the same drain current and the same source voltage as in the differential pair of Figure 3.29(b) is given by,

$$\sigma(\delta V_G) = \sqrt{\sigma_T^2 + (\frac{g_m}{I_D}\sigma_\beta)^2}. \tag{3.40}$$

For a current mirror, it can be seen from equation 3.37 that biasing the transistor in weak inversion ($I_C \ll 1$, and thus with the maximum $\frac{g_m}{I_D}$ as shown in section 3.5.3 in Figure 3.16) results in the largest current mismatch, whereas the minimum current mismatch, is obtained with the transistors operating deep in strong inversion [28]. On the other hand, for a differential pair, for example, operation of the transistors in weak inversion results in the minimum mismatch between the gate voltages, as shown in Figure 3.30(a)(b).

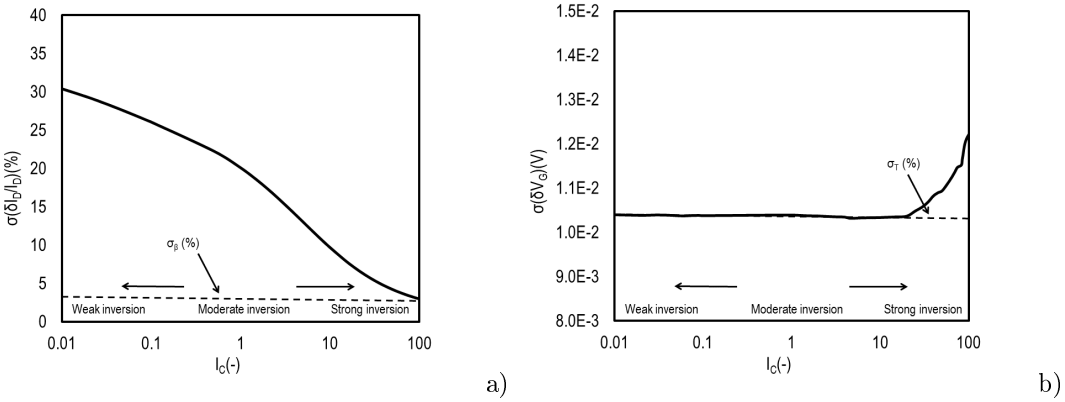


Figure 3.30: NMOS transistor (a) current mismatch $\sigma(\frac{\delta I_D}{I_D})$ and (b) voltage mismatch $\sigma(\delta V_G)$ vs. inversion coefficient I_C typical representation.

It should be noted that, in general, the design for best matching of a current mirror or a differential pair is more complicated than in the analysis above. In the design problem we must compare solutions corresponding to transistors with different geometries and biases [28]. Mismatch can be simulated in several different ways. The goal of mismatch simulation is to obtain the standard deviation of circuit properties caused by the stochastic nature of transistor model parameters. In this thesis, in order to extract the current and voltage mismatch of the two basic MOSFET topologies shown in Figure 3.29, we used simulation based on Monte-Carlo analysis, which is simple, precise and widely used. Several circuits with randomly chosen parameters according to the probability density function of the simulated parameter are generated and simulated. The most frequently used distribution is Gaussian which was also used here but the method is appropriate for any kind of distribution [34]. So, for this thesis using a special simulator tool (Cadence Virtuoso IC 6.15-ADEXL), we extracted the standard deviation of the parameters we wanted for various I_C values as we will see below.

3.9.3 Simulation and results

In this section, Figure 3.31, shows the simulated current mismatch $\sigma(\frac{\delta I_D}{I_D})$ vs. inversion coefficient I_C ($W/L = 500nm/500nm$) from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs for both 90nm and 65nm bulk CMOS technologies. In Figure 3.32, the simulated voltage mismatch $\sigma(\delta V_G)$ vs. inversion coefficient I_C ($W/L = 500nm/500nm$) from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process, is also presented. The schematics of the circuits used to derive these results are depicted in Figures 3.40, 3.41.

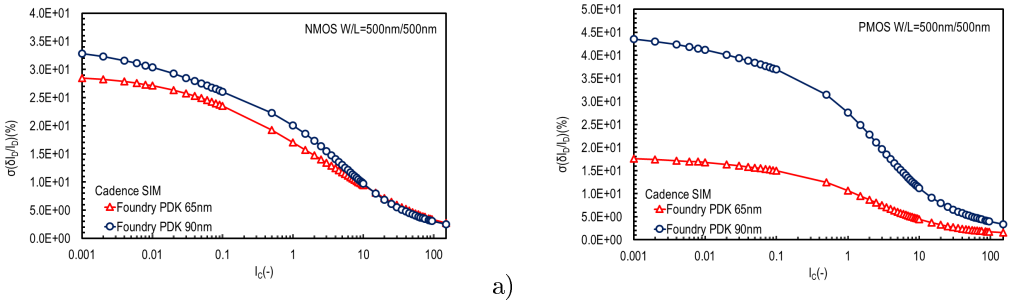


Figure 3.31: Simulated current mismatch $\sigma(\frac{\delta I_D}{I_D})$ vs. inversion coefficient I_C $(W/L = 500nm/500nm)$ from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.

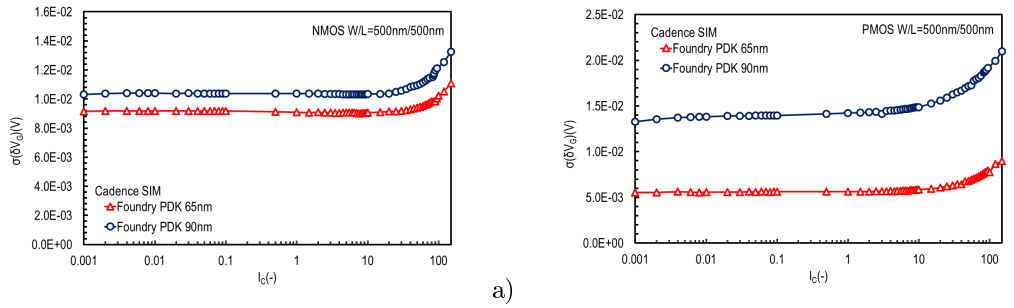


Figure 3.32: Simulated voltage mismatch $\sigma(\delta V_G)$ vs. inversion coefficient I_C $(W/L = 500nm/500nm)$ from weak to strong inversion in saturation ($\mid V_{DS} \mid = 1.2V$) for (a) n-type and (b) p-type MOSFETs of 65nm, 90nm bulk CMOS process.

Current mismatch is following the expected $\frac{g_m}{I_D}$ trend in all cases. Specifically, drain current mismatch is expected to be maximum towards weak inversion. In the case of voltage mismatch the expected behavior is predicted, minimum values towards weak inversion for both n- and p-type transistors. The 65nm PDK predicts improved matching in all cases.

3.10 Comparative results of the technology parameters

The Table 5 shows in detail the results of the extraction of the key design parameters of the two technologies 65nm and 90nm and their percentage change.

Parameter	Simulated (PDK 90nm)	Simulated (PDK 65nm)	Difference between the two technologies (%)	Unit
C_{OX} (NMOS) / C'_{OX} (NMOS)	3.07/12.3	3.37/13.5	+9.8 %	fF / $\mathrm{fF}/\mu\mathrm{m}^2$
C_{OX} (PMOS) / C'_{OX} (PMOS)	2.93/11.7	3.14/12.6	+7.2%	fF / $\mathrm{fF}/\mu\mathrm{m}^2$
n_n (NMOS)	1.24	1.25	+0.8 %	–
n_p (PMOS)	1.22	1.24	+1.6 %	–
$I_{0,n}$ (NMOS)	630	390.25	-38 %	nA
$I_{0,p}$ (PMOS)	330	346	+4.8 %	nA
$K_{P,n}$ (NMOS)	306	252	+17.6 %	$\frac{\mu A}{V^2}$
$K_{P,p}$ (PMOS)	103	102	-0.98 %	$\frac{\mu A}{V^2}$
μ_n (NMOS)	249	187	-24.9 %	$\frac{cm}{VS}$
μ_p (PMOS)	88	81	-7.9 %	$\frac{cm}{VS}$
$V_{A,n}$ (NMOS) /$U_{a,n}$ (NMOS)	4.028/8.057	5.18/10.37	+28.7 %	mV / $\frac{V}{\mu m}$
$V_{A,p}$ (PMOS) /$U_{a,p}$ (PMOS)	4.024/8.049	6.27/12.53	+55.7 %	mV / $\frac{V}{\mu m}$

Table 5: Basic design parameter extraction of of 65nm, 90nm bulk CMOS process and their percentage change.

3.11 Cadence simulation schematics

All the schematic simulations (Cadence Virtuoso IC 6.15) used to extract the parameters analyzed above are presented below.

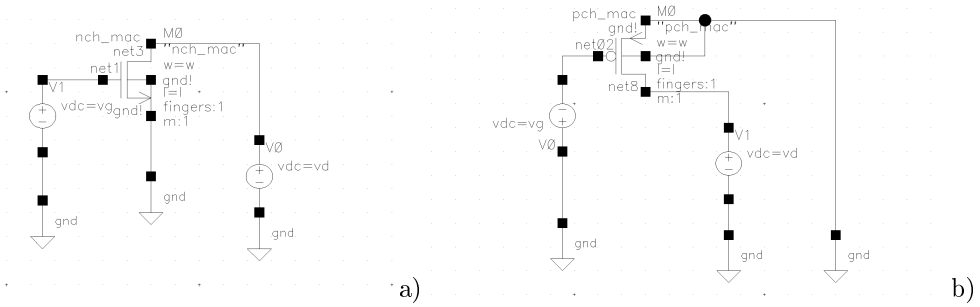


Figure 3.33: Transfer and output $I_{DS} - V_{GS}$, $I_{DS} - V_{DS}$ schematic for (a) n-type and (b) p-type MOSFETs.

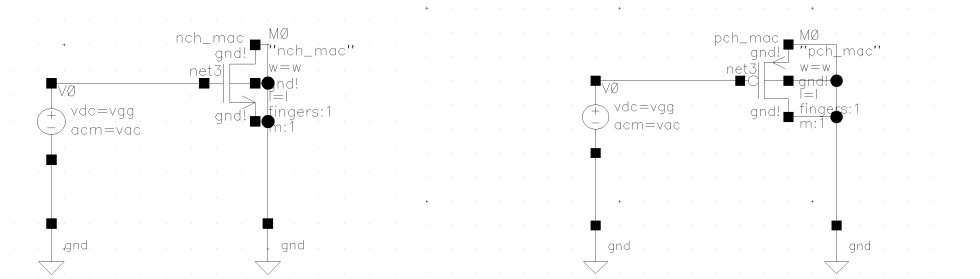


Figure 3.34: Oxide capacitance C_{OX} schematic for (a) n-type and (b) p-type MOSFETs.

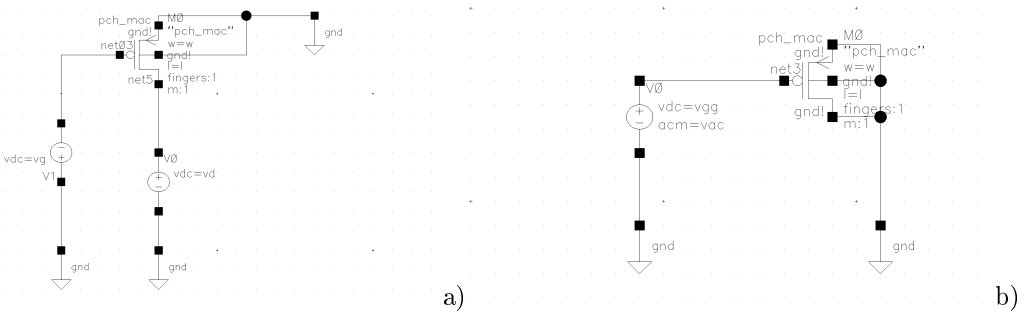


Figure 3.35: Slope factor n and technology current I_0 schematic for (a) n-type and (b) p-type MOSFETs.

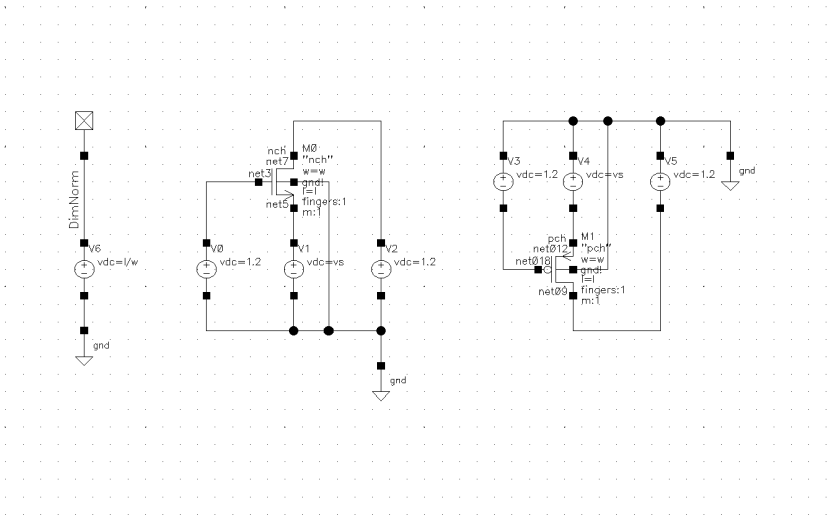


Figure 3.36: Carrier mobility μ and transconductance parameter K_p schematic for n-type and p-type MOSFETs [37].

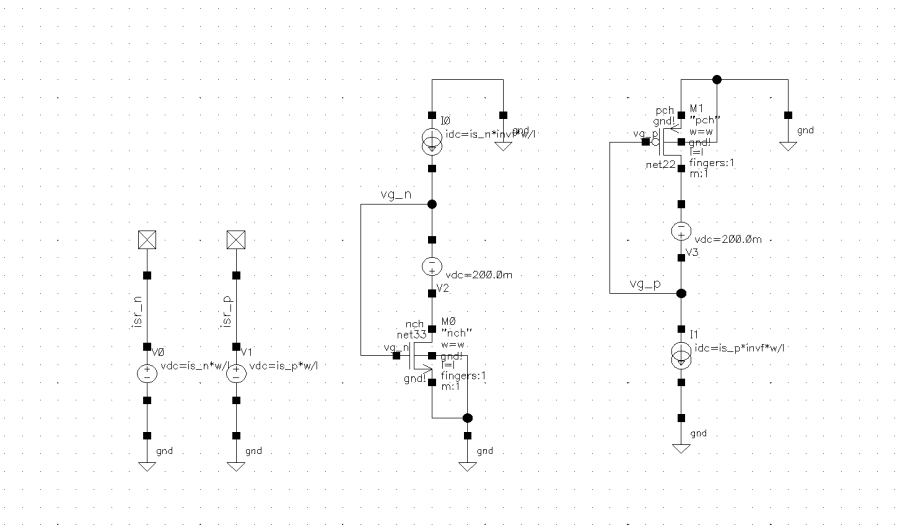


Figure 3.37: Transconductance efficiency $\frac{g_m}{I_D}$ and transit frequency f_T schematic for n-type and p-type MOSFETs [37].

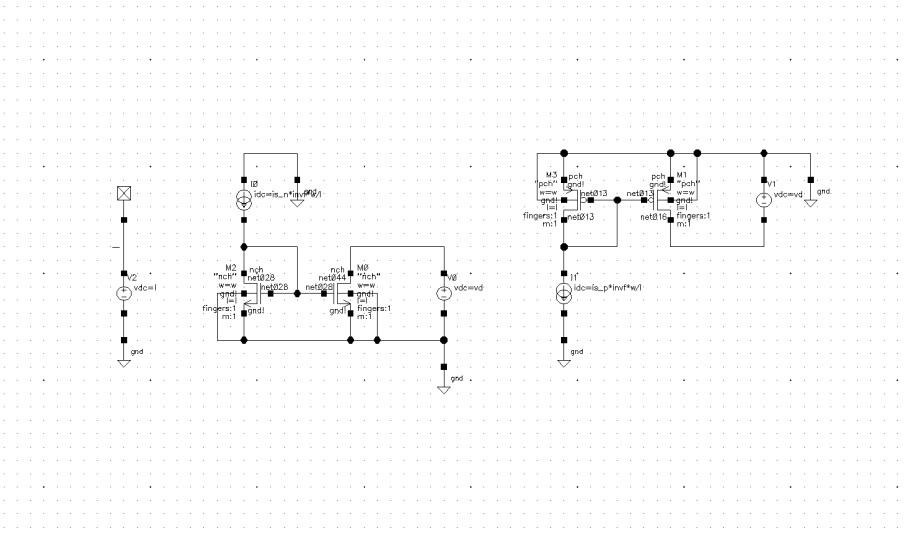


Figure 3.38: Early Voltage U_a, intrinsic gain A_V schematic for n-type and p-type MOSFETs [37].

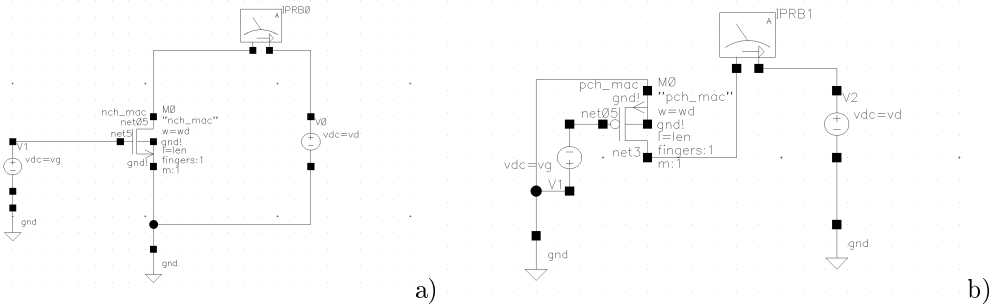


Figure 3.39: Flicker noise S_{ID} schematic for (a) n-type and (b) p-type MOSFETs.

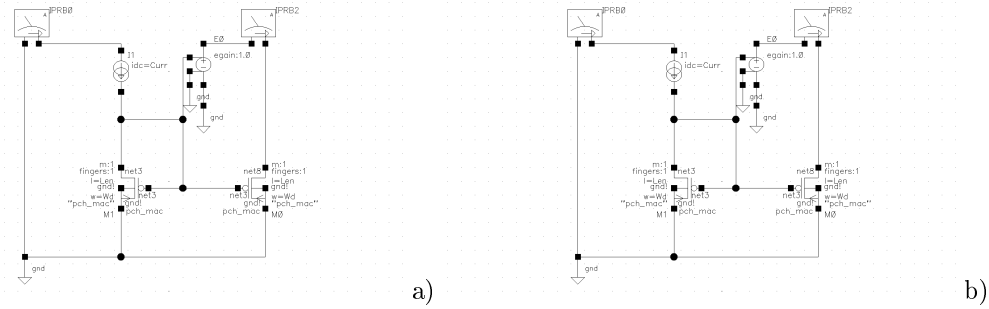


Figure 3.40: Current mismatch $\sigma(\frac{\delta I_D}{I_D})$ schematic for (a) n-type and (b) p-type MOSFETs.

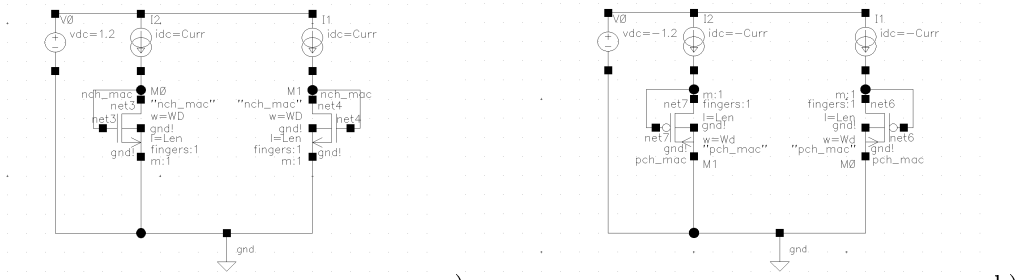


Figure 3.41: Voltage mismatch $\sigma(\delta V_G)$ schematic for (a) n-type and (b) p-type MOSFETs.

4 Operational Transconductance Amplifiers (OTAs)

Industry is continuously researching techniques to reduce power requirements, while increasing speed, to meet the demands of today's low (battery) powered wireless systems. The operational transconductance amplifier (OTA) is a fundamental building block in analog (mixed-signal) design and its performance characteristics are the foundation of system level characteristics. Improving the performance of the fundamental amplifier structure, while avoiding costly silicon area and static power increases, is critical to improving system performance.

In this section of this thesis, we discuss general design ideas and techniques for a supply voltage of $1.2V$ simple and fully differential folded cascode OTA design and biasing in two different bulk CMOS processes of 65nm and 90nm. As we have already extract and verify the values of the most important parameters of the two technologies in the previous section, the goal here is to exploit these results as much possible and use them in order to design properly these two circuits. After this process, using a prepared set of testbenches, circuits performances are verified by simulation in Cadence Virtuoso IC 6.15 as in section 3 and as a result we can extract usefull conclusions for the two discussed technologies.

4.1 Basic theoretical Analysis of OTAs

The operational transconductance amplifiers (OTAs) are amplifiers whose differential input voltage produces an output current. Its ideal behavior is characterized by a high impedance input stage and high impedance output stage, as shown in Figure 4.1.

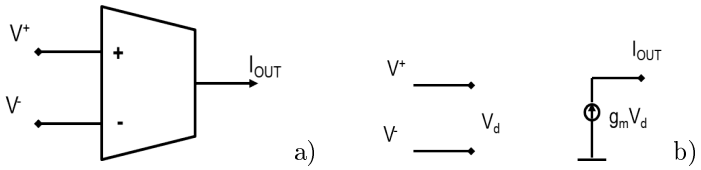


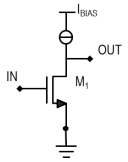
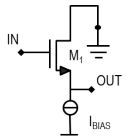
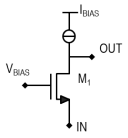
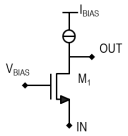
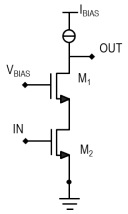
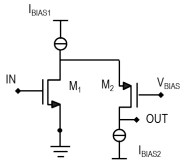
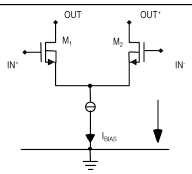
Figure 4.1: a) Ideal OTA representation b) Small-signal equivalent circuit [39].

The ideal transfer function of this device is its transconductance, denoted by g_m. The main structure of OTAs contains two stages. The first one is a differential input amplifier, which produces current fluctuations as a response to each input voltage ($V+$ and $V-$). The second stage is composed by current mirrors that mix this fluctuations into an output current and also suppress the DC bias current. MOS technology is widely used in OTAs design due to its lower power consumption, its differential input infinite impedance (even in open loop circuits) and the possibility of achieving very low transconductances (in order of uS, nS and beyond) [38]. The transconductance response of the differential input pair is not a linear function of its differential input voltage. This is caused by the equations that describe the MOS transistors and their region of operation [40]. Since weak inversion region is dominated by exponential relationships and strong inversion region by square-law formulas, moderate inversion is mostly recommended in OTA design since it offers the best trade-off between the design parameters [41].

4.1.1 Basic analog structures

Structured analog design is based on the idea that an analog cell can be divided into basic analog structures. A basic analog structure is a small analog building block consisting of one or more transistors. We can describe it by a set of design parameters that affect circuit performance. From this point of view, the design procedure becomes the same for both simple and more complicated circuits. This section is focused on the basic analog structures used, in order to examine the circuit partitioning in the section 4.1.2. A basic analog structure is described as a set of one or more transistors connected in a specific way to realize voltage-to-current conversion, current-to-voltage conversion, or both. Such a structure requires current or voltage bias, which is again realized by another basic analog structure.

Several basic analog structures connected together represent a more complex analog structure that is often called an analog cell. In the Table below are shown the basic analog structures that are more often used in order to build an analog cell. It is crucial to note that a basic analog structure is not any combination of transistors [42].

Analog structure name	Schematic	Basic description
Common source		Common source (source connected to the DC voltage supply, the input at the gate, and the output at the drain terminal) structure, converts voltage to current.
Common drain		Common drain (drain connected to the DC voltage supply, the input at the gate, and the output at the source terminal) structure, converts voltage to current and its the simplest voltage follower.
Common gate		Common gate (gate connected to the DC voltage supply, the input at the gate, and the output at the drain terminal) structure, converts voltage to current and it has small input impedance.
Diode-connected transistor		Diode-connected (gate and drain connected together) structure, converts voltage to current.
Cascode		Cascode structure, is used in voltage to current conversion, in common source and gate stage and it has high output impedance.
Folded cascode		Folded cascode structure, is used to convert voltage to current and as a cascode stage variant also.
Differential pair		Differential pair structure, converts the differential input voltage to current.

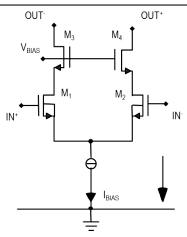
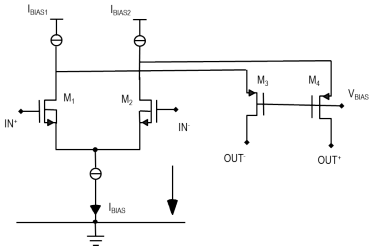
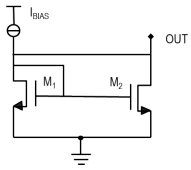
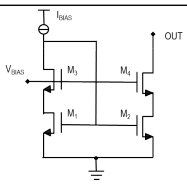
Cascoded differential pair		Cascoded differential pair structure, converts the differential input voltage to current and also used as differential pair variant.
Folded cascode differential pair		Folded cascoded differential pair structure, converts the differential input voltage to current and also used as differential pair variant similar to simple cascoded differential pair.
Current mirror		Current mirror structure, copies current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading and its also used for current multiplication or division [44].
Cascode current mirror		Cascode current mirror structure, copies current precisely, it is used for current multiplication or division and it has also high output impedance.

Table 6: Basic analog structures library [42].

Finally, we should note that except for the finite number of different basic analog structures, there is also a finite number of transistor design situations. So, we could say that a basic analog structure represents a special case of transistor-level design, where each transistor works in the given environment and only a few transistor design parameters are exist.

4.1.2 Circuit partitioning and behavioral model of an analog amplifier

Usually, operational transconductance amplifiers and operational amplifiers designs implemented as a single-ended or a fully-differential topologies. The operational transconductance amplifiers, realized as single-stage amplifiers which are classified as:

- simple OTA,
- telescopic OTA, and
- folded cascode OTA.

Two-stage operational amplifiers consist of an OTA in the first stage followed by a common source, a common drain or a cascode as illustrated in the same figure. Each stage of the analog amplifier includes a transconductance (g_m) structure that converts the input voltage to the output current, followed by a

load structure that converts the output current to the output voltage. The transconductance structure needs a current bias, because any cascoded structure requires a voltage bias. Therefore, all basic analog structures can be classified in the following way [42, 43]:

- **transconductance structures:** common source, common drain, cascode, differential pair and its cascoded variants,
- **load structures**: simple and cascode current mirrors,
- and **bias structures**: simple and cascode current mirrors, diode-connected transistor.

So, we can easily conclude that all transconductance structures have the same set of design parameters that affect the circuit performances, which we will analyze in the section 4.1.3. This helps the derivation of the basic specifications and simplifies the design procedure of the circuits that we are going to analyze.

When we refer to the behavioral model of an amplifier, we assume tha there is a simplest g_m-cell which includes the current bias structure and also provides the requires transconductance and the output current. This g_m-cell followed by a load gives the simplest behavioral model of an analog amplifier This model is useful, to do our system-level simulations for the derivation of the amplifier's specifications and it depends on the system and the application complexity. Two examples of behavioral models of an analog amplifier which we will use with minor variations and in our simulations are shown in Figure 4.2.

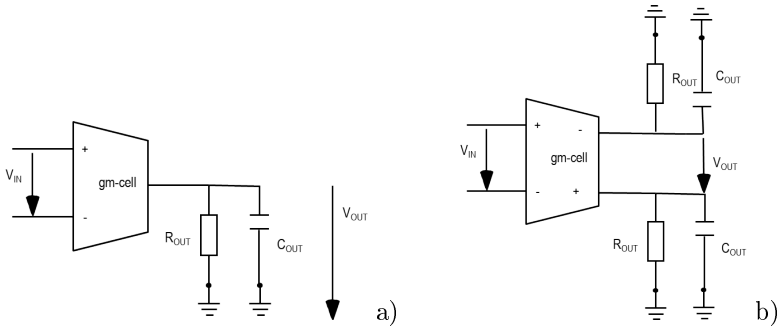


Figure 4.2: Behavioral model of an analog amplifier with a) single-ended and b) fully-differential outputs [42].

4.1.3 Definitions of the basic design parameters

Several common characterization methods are used to classify the functionality of OTA structures. These performance measurement techniques will be used to analyze designed structures via theoretical calculation and simulation with the procedures presented in the following chapters. A list of the measured characteristics is provided below:

- Gain- A_0 $[dB]$
- Gain Bandwidth product– GBW $[rad/s]$
- Phase Margin- PM [°]
- Power consumption- P $[W]$
- Common-mode input range- CMR $[V]$
- Output-voltage swing- V_{OUT} $[V]$
- Slew Rate- SR $[V/s]$

- Noise– $[nV/\sqrt{H_Z}]$
- Offset- $[mV]$

Open-loop gain (usually referred to as A_0 $[dB]$) is the gain of the amplifier without the feedback loop being closed, hence the name "open-loop". This gain is flat from dc to what is referred to as the dominant pole. From there it falls off at $6dB/octave$ or $20dB/decade$. (An octave is a doubling in frequency and a decade is $x10$ in frequency). This is referred to as a single-pole response. It will continue to fall at this rate until it hits another pole in the response. This 2nd pole will double the rate at which the open-loop gain falls, that is, to $12dB/octave$ or $40dB/decade$. If the open-loop gain has dropped below $0dB$ (unity gain) before it hits the $2nd$ pole, the amplifier will be unconditional stable at any gain.

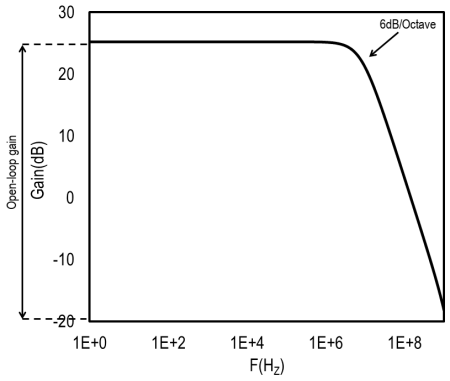


Figure 4.3: Open-Loop Gain (Bode Plot-single pole response).

The open-loop gain of each transconductance amplifier stage is defined as a product of the equivalent transconductance of the transconductance structure and the equivalent resistance seen at the output [42],

$$A_0 = g_m R_{OUT} \tag{4.1}$$

The open-loop gain can change due to output voltage levels and loading. There is also some dependency on temperature. In general, these effects are of a very minor degree and can, in most cases, be ignored [45].

Gain Bandwidth product for an amplifier is the product of the amplifier's bandwidth and the gain at which the bandwidth is measured [46]. The open-loop gain falls at 6 dB/octave. This means that if we double the frequency, the gain falls to half of what it was. In other words, if the frequency is halved, the open-loop gain will double, as shown in Figure 4.4. This gives rise to what is known as the gain bandwidth Product. If we multiply the open-loop gain by the frequency the product is always a constant. The caveat for this is that we have to be in the part of the curve that is falling at 6 dB/octave. This gives us a convenient figure of merit with which to determine if a particular amplifier is usable in a particular application [45]. The gain bandwidth product of a transconductance amplifier stage is defined as the quotient of the the equivalent transconductance of the transconductance structure and the equivalent maximal output capacitance of load structure [42],

$$GBW = \frac{g_m}{2\pi C_L}. \tag{4.2}$$

Phase Margin is the amount of phase shift that is left until you hit 180° measured at the unity gain point [45]. Just as the amplitude response does not stay flat and then change instantaneously,

the phase will also change gradually, starting as much as a decade back from the corner frequency. In order to define properly the connection between these three first parameters it is mandatory to analyze and explain the frequency response of an amplifier. The poles and zeros in the transfer function can be easily determined analyzing the gain path, i.e. the signal path from the amplifier input to the amplifier output, and using the following guidelines [5]:

- pole- corresponds to an equivalent resistance in parallel with an equivalent capacitance seen at each node in the gain path,
- zero- corresponds to an equivalent resistance in series with an equivalent capacitance in the gain path,
- positive zero- appears due to a possible feedback path in the gain path (for example as in the case of Miller capacitances),
- doublet pole-zero- appears as a consequence of two possible gain paths (for example as in the case of single-ended topology).

So, now we can define three important terms in order to understand the relation between open-loop gain, gain bandwidth product and phase margin:

- bandwidth frequency - corresponds to the dominant pole frequency f_{dp} in the open loop transfer function,
- gain bandwidth frequency f_{GBW} - corresponds to the product of the DC gain and the bandwidth frequency of the open loop transfer function,

$$f_{GBW} = A_0 f_{dp}. \tag{4.3}$$

Therefore, we could say that phase margin is given by the difference between the phase shift at the gain bandwidth frequency and the phase shift of -180°,

$$PM = 180^\circ - \varphi(f_{GBW}) \tag{4.4}$$

or the sum of the intristic capacitancies $\sum C$ in all nodes in the signal gain path,

$$PM = 180^\circ - \arctan(\frac{f_{GBW}}{f_{dp}}) - \sum \arctan(\frac{f_{GBW}}{f_{ndp}}). \tag{4.5}$$

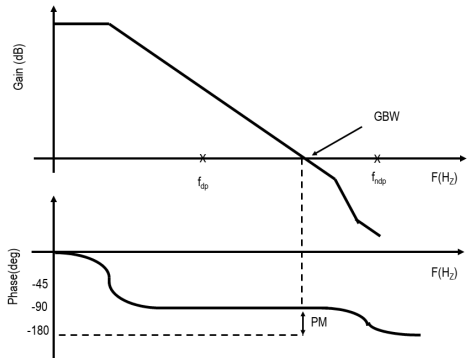


Figure 4.4: Bode plot which illustrates of dominant, non-dominant pole, gain bandwidth product and phase margin extraction for an amplifier.

The first three design parameters we could say that are used in order to check the stability of all feedback loops of an amplifier. The amplifier in negative feedback is unconditionally stable if it behaves as a system of the first order, that is if there exists only one pole in its transfer function. However, there usually exist several nodes (poles) in the gain path, and thus the stability is ensured only if the phase shift of any feedback loop is bigger than -135°[42].

Power consumption or static power dissipation (P_{STATIC}) is the product of the sum of the currents flowing through the current sources or sinks with the power supply voltages and is given by [47],

$$P_{STATIC} = (V_{DD} - V_{SS}) \sum I_{BIAS}. \tag{4.6}$$

If the power consumption of the circuit is low and then it is suitable for low power applications.

Common-mode input range is defined as the range of voltage ($V_{IN}^{MAX}, V_{IN}^{MIN}$) for which the input differential pair will remain in saturation [48]. This range is determined by the amplifier structure, transistor sizes, and bias current. The maximal and minimal common-mode DC level at the input, are defined,

$$V_{IN}^{MAX}, V_{IN}^{MIN} = V_{sup} - V_{GS} - V_{DSAT,} \tag{4.7}$$

as the difference of the the saturation voltage of bias structure and the saturation voltage and the V_{GS} voltage headroom of transconductance structure from the supply voltage of the amplifier. An example is shown in the Figure 4.5. From this equation, it can be observed that $V_{IN}^{MAX}, V_{IN}^{MIN}$ depend on saturation voltages. Therefore inversion factor is the main parameter used to define the CMR of an OTA.

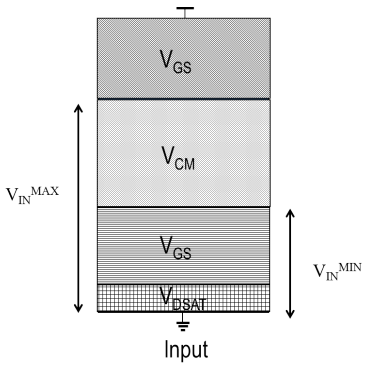


Figure 4.5: The input common-mode headroom extraction example.

Output-voltage swing also denoted as output swing, ($V_{OUT}^{MAX}, V_{OUT}^{MIN}$) corresponds to the amplitude of the output or the differential output signal for which the transistors of the output stage do not move into the (transistor) linear operating region and remains to saturation [42]. This is a spec on how much voltage we can expect from the output. If using reduced supply voltages this spec for overhead will remain constant but if we shrink the supply voltage, we need to maximize the output dynamic range. What is typically done to increase the dynamic range of an amplifier is to change the configuration of the output stage. The maximal and minimal output-voltage swing level, are defined,

$$V_{OUT}^{MAX}, V_{OUT}^{MIN} = V_{sup} - \sum V_{DSAT} \tag{4.8}$$

as the difference of the saturation voltage of load structure (and, in some cases, of transconductance structure) from the supply voltage of the amplifier. Figure 4.6 demonstrates how these two extreme voltages constitute the limits of the amplifier linear operation. Beyond these limits and up to saturation, the voltage transfer characteristic of the amplifier is nonlinear. The transfer characteristic shown in this Figure illustrates the OTA linear region, defining the output voltage headroom V_{OUT}.

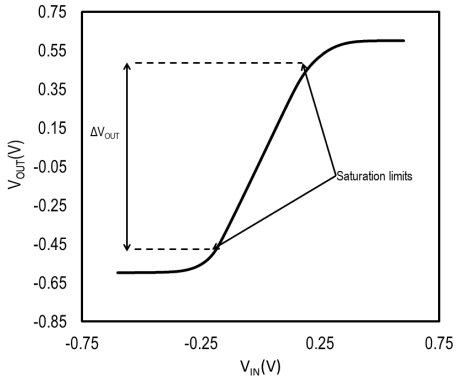


Figure 4.6: Transfer characteristic illustrates an OTA linear region.

Slew Rate of an amplifier is the maximum rate of change of voltage at its output. It is expressed in V/s (or, more probably, $V/\mu s$). Amplifiers may have different slew rates during positive and negative going transitions, due to circuit design. he speed of the amplifier corresponds to the time required for the signal at the output to establish its final value or within an acceptable error. It depends on the capacitive load, the parasitic capacitances in the nodes in the gain path, as well as on the currents available to charge or discharge these capacitances. Therefore, it can be characterized by the slew rate [42]. Slew rate is defined as the ratio of the maximal available large signal current and the equivalent capacitance seen at the output,

$$SR = \frac{\partial_{OUT}}{\partial t} = \frac{I_{OUT}}{C_L}. \tag{4.9}$$

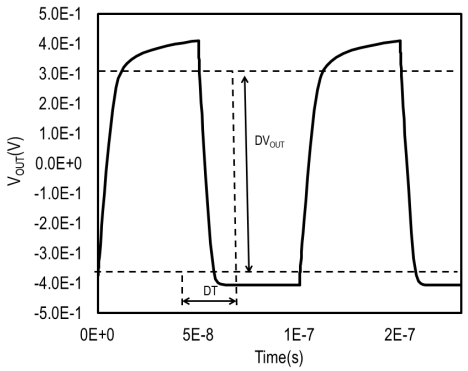


Figure 4.7: Slew Rate extraction example.

Noise contribution is modeled as an equivalent voltage source at the transistor gate equal to its input referred noise voltage spectral density and It consists of the thermal noise component and the flicker noise component as already analyzed in section 3.8. The amplifier noise is expressed as the equivalent input referred noise voltage spectral density and is defined as,

$$V_{n,eq}^2 = V_{n,eq}^2 - (\frac{g_{m,mirr}}{g_m}) \sum V_{n,eq}^2 \tag{4.10}$$

the difference between the noise contribution of all transistors except cascodes and the ratio of the transconductances of transconductance and load structure [7, 42].

Offset is practically, a nonzero output voltage (offset) that will be present and is due to random and systematic errors and is called offset due to the fact that ideally, if both inputs of the amplifier are grounded, the output voltage should be zero [4, 49]. We could say that, offset is presented due to random and systematic errors,

- **Random Offset** is due to mismatches in the input stage as a result of fabrication including (but not limited to): threshold voltage differences and geometric differences. Random errors can be estimated via Monte Carlo simulations as we will see in the following analysis of our OTA topologies.
- **Systematic offset** is inherent to the design. Systematic errors can be the result of non-symmetries in the OTA design, creating voltage and current mismatches. The systematic offset can be determined via simulation and will be evident in the DC sweep simulation as the offset from the zero-zero intercept where the input voltage and output voltage should both equal zero.

For each pair of matched transistors in the circuit, the gate voltage mismatch contribution is modeled as an equivalent voltage source in the transistor gate equal to its gate voltage mismatch standard deviation. It is important to note that, the differential pair usually represents the input stage of the circuit and converts the small input signal into a current and also the cascode transistors do not contribute to the input voltage mismatch and as a result we have to simply compute the standard deviation of the differential pair. The amplifier offset is expressed as the equivalent input referred offset, calculated as,

$$V_{os}^2 = V_{m,eq}^2 - (\frac{g_{m,mirr}}{g_m}) \sum V_{m,eq}^2 \tag{4.11}$$

the difference between the voltage mismatch contribution of all transistors except cascodes and the ratio of the transconductances of transconductance and load structure [7, 42]. The statistical dispersion is inversely proportional to the area of the device as derived from the mismatch analysis of section 3.9. Therefore, in order to achieve a given matching precision, one has to design large enough components, obviously, the designer faces an important trade-off between precision and circuit area when using only matching properties. But there are also many other techniques that allow to increase the precision of poor circuit elements. Instead of focusing on building high-precision devices, we can build low-precision components and try to optimize their imperfections later on based on the application used on. There are a lot of techniques, each one having its specific application fields. We are going to analyze a simple trade off technique in the next section of this thesis [37].

4.2 Simple OTA design

4.2.1 Theoretical design and operation

A simple, one stage, Operational Transconductance Amplifier (OTA) configuration is shown in Figure 4.8.

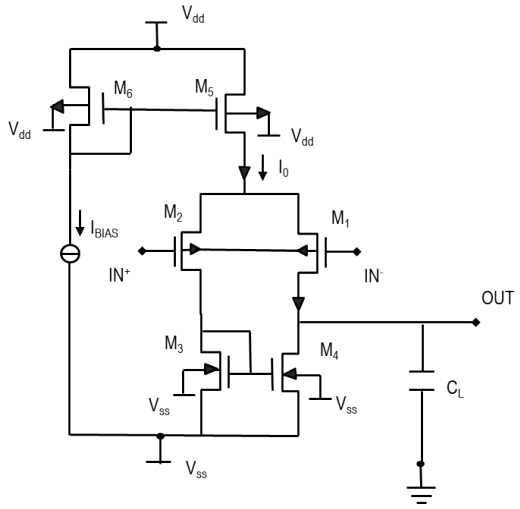


Figure 4.8: Simple one stage Operational Transconductance Amplifier (OTA) [37].

The OTA employs a PMOS input differential pair and two current mirrors, one PMOS and one NMOS. The differential input pair is comprised of transistors M_1, M_2. The differential pair is biased by the PMOS current mirror M_5, M_6. The NMOS current mirror M_3, M_4 reflect currents generated in the differential pair to the output shell. The simple OTA shown above uses a differential pair in conjunction with two current mirrors to convert an input voltage into an output current. For a common mode input voltage, the currents are constant and will be: $I_{d1} = i_{d2} = I_{BIAS}/2$, and $I_{OUT} = 0$. A differential input signal will generate an output current proportional to the applied differential voltage based on the transconductance of the differential pair. However, the simple OTA is only capable of producing an output current with a maximum amplitude equal to the bias current in the output shell. For this reason, the conventional OTA is a referenced as a class A structure capable of producing maximum signal currents equal to that of the bias current applied. Slew rate (SR) is directly proportional to the maximum output current and is defined as the maximum rate of change of the output voltage. For a single stage amplifier, the slew rate is the output current divided by the total load capacitance. This simple OTA topology will possible suffer from the fact that high speed requires large bias currents which translates to large static power dissipation so as these requirements are difficult to achieve with this topology, we will also propose and analyze a Fully Differential Folded Cascode structure with Local Common Mode Feedback (LCMFB) circuit, presented in section 4.3, in which we can meet better these requirements [48, 50]. These circuits are simulated for the same specifications but with the appropriate sizing in Cadence Virtuoso IC 6.15 environment for both 65nm and 90nm PDKs. Therefore, we could extract useful conclusions about the use and functionality of these two technologies and their suitability for specific applications, and we can better understand how the theoretical approach of these circuits responds to real simulation conditions and how the resulting tradeoffs can be treated with appropriate techniques in order to optimize the circuits and achieve better performance. The schematic used in order to simulate this topology is shown in Figure 4.44.

4.2.2 Specifications and sizing

The circuit is designed to meet the following specifications, which will be verified by simulation for both 65nm and 90nm technologies.

Parameter	Specifications	Unit
Technology	$65, 90$	nm
Supply Voltage	$+/-0.6$	V
Open-loop gain	> 25	dB
GBW	150	MH_Z
Slew Rate	100	$\frac{V}{\mu s}$
Load capacitance	100	fF

Table 7: Simple OTA parameters design specifications [37].

The next step is to size step by step this simple OTA, in order to do this calculations we use the calculated parameters of the section 3. They are demonstrated for both technologies in the Table 8. Also, the basic physical constants used, are shown in Table 9. All the calculations of the parameters that used in this section of the thesis are calculated in Matlab as shown in Appendix section A.1 and they are explained below.

Technology Parameters	Value 90nm PDK	Value 65nm PDK	Unit
$n_n(NMOS)/n_p(PMOS)$	1.24/1.22	1.25/1.24	-
$K_{P,n}(NMOS)/K_{P,p}(PMOS)$	306/102.9	252/102	$\frac{\mu A}{V^2}$
$U_{a,n}(NMOS)/U_{a,p}(PMOS)$	8.057/8.049	10.37/12.53	$\frac{V}{\mu m}$

Table 8: Basic technology parameters.

Physical constants	Value	Unit
k (Boltzman's constant)	1.3810^{-23}	$\frac{J}{K}$
q (Coulomb's constant)	1.60210^{-19}	C
T_K (Temperature)	300	K

Table 9: Physical constants.

Using the inversion coefficient permits design freely in all regions of MOS operation, including moderate inversion. Moderate inversion [51], a transitional region spanning nearly two decades of drain current between weak and strong inversion, has become increasingly important in modern design. This is because it offers a compromise of high transconductance (high transconductance efficiency), low drain–source saturation voltage, minimal velocity saturation degradation of transconductance, and moderate bandwidth necessary for power-efficient, low-voltage design. For all these reasons, we have

tried to size our topology in the limits of moderate inversion. So, predictions and measurements of MOS performance will be given later in this section, with considerable emphasis on the moderate inversion region [7].

In order to size our topology properly, the circuit of the Figure 4.8 is partitioned into the following basic analog structures:

- Bias PMOS current mirror,
- input PMOS differential pair and
- active load NMOS current mirror.

We will firstly demonstrate the sizing methodology for the **90nm PDK** and then we will show more briefly the sizing of the **65nm PDK** as we follow exactly the same procedure [37].

Bias current mirror

In order to compute $I_0 = I_{BIAS}$ current we took into account the specified slew rate and the load capacitance and from the equation 4.9 we have,

$$I_{BIAS} = I_0 = SRC_L \Longrightarrow I_{BIAS} = 10\mu A. \tag{4.12}$$

We also choose $L_5 = 2L_{min} = 180nm = L_6$(it is proposed not to use transistor lengths smaller than $2L_{min}$) and $I_{C,5} = I_{C,6} = 1$ and from the equation 2.1 we can size the current mirror $M_5 - M_6$ as follows,

$$I_{C,5} = \frac{I_0}{2n_p U_T^2 K_{P,p} \frac{W_5}{L_5}} \Longrightarrow \tag{4.13}$$

$$W_5 = \frac{I_0 L_5}{2n_p U_T^2 K_{P,p} I_{C,5}} = 10.7\mu m = W_6. \tag{4.14}$$

We know that,

$$U_T = \frac{kT_K}{q} = 25.9mV. \tag{4.15}$$

Input differential pair

From the equations, 4.2, 4.9 we know that $GBW = \frac{g_m}{2\pi c_L}$ and $SR = \frac{I_{BIAS}}{C_L}$ so we have that,

$$\frac{GBW}{SR} = \frac{\frac{g_{m,2}}{2\pi c_L}}{\frac{I_{BIAS}}{C_L}} \tag{4.16}$$

and $I_{BIAS} = 2I_{d,2}$ so,

$$\frac{g_{m,2}}{I_{d,2}} = \frac{4\pi GBW}{SR} = 18.84V^{-1}. \tag{4.17}$$

Therefore, using the following equation and several different methods such as linear interpolation as it shown in Appendix section A.1 we can compute $I_{C,2} = I_{C,1}$,

$$\frac{g_{m,2}}{I_{d,2}} = \frac{1}{n_p U_T} \frac{1}{\frac{1}{2} + \sqrt{I_{C,2} + \frac{1}{4}}} \Longrightarrow I_{C,2} = I_{C,1} \approx 1.15. \tag{4.18}$$

In the next step, we can define the ratio $\frac{W_2}{L_2}$ modifying the equation 4.13 as follows,

$$\frac{W_2}{L_2} = \frac{I_{d,2}}{2n_p U_T^2 K_{P,p} I_{C,2}} = 25.9. \tag{4.19}$$

Finally, in order to size the differential pair $M_1 - M_2$ firstly we have to convert the specified open-loop gain from dB to $\frac{V}{V}$ so,

$$A_V = 10^{\frac{25}{20}} = 17.78\frac{V}{V}. \tag{4.20}$$

So, as we can easily compute $g_{m,2} = \frac{g_{m,2}}{I_{d,2}} I_{d,2} = 94.17\mu S$ and from the equation 4.1 we can also compute $R_{OUT,2}$,

$$R_{OUT,2} = \frac{A_V}{g_{m,2}} = 188.84K\Omega \tag{4.21}$$

and from the equation 3.30,

$$g_{ds,2} = \frac{2}{R_{OUT}} = 10.6\mu S. \tag{4.22}$$

Consequently, using a transformation of the equation 3.33 and knowing that $\frac{W_2}{L_2} = 25.9$ we compute W_2 and L_2 as follows,

$$g_{ds,2} = \frac{I_{d,2}}{L_2 U_{a,p}} \Rightarrow L_2 = \frac{I_{d,2}}{g_{ds,2} U_{a,p}} = 58.6nm = L_1 \tag{4.23}$$

and

$$W_2 = \frac{W_2}{L_2} L_2 = 1.5\mu m = W_1. \tag{4.24}$$

Here it is important to note that besides the theoretical approximations in the next section we will analyze the fact as we want to achieve the appropriate g_m in the input differential pair in real design conditions we increase widths and lengths of the transistors in the same way in order to maintain the $\frac{W_2}{L_2}$ ratio constant and achieve the desired value of g_m. So, we finally conclude to the quadruple of W_2, L_2,

$$L_2 = 236.4nm = L_1$$

and

$$W_2 = 0.6\mu m = W_1.$$

Active load current mirror

Here, in order to minimize the noise contribution we have that,

$$\frac{g_{m,4}}{I_{d,4}} \ll \frac{g_{m,2}}{I_{d,2}} \approx 0.5\frac{g_{m,2}}{I_{d,2}} = 9.4V^{-1} \tag{4.25}$$

So, following exactly the same methodology as in the input differential pair and from the equation 4.18 we can compute $I_{C,3} = I_{C,4}$,

$$I_{C,3} = I_{C,4} = 7.65,$$

which means in the upper limits of moderate inversion as we as we wished.
Then, as we know that $I_{d,4} = 5\mu A$ and from the equation 4.19 we can compute the $\frac{W_4}{L_4}$ ratio,

$$\frac{W_4}{L_4} = 1.28.$$

Solving in the same sequence as above the equations, 4.21, 4.22 we have that,

$$g_{m,4} = 47.08\mu S,$$

$$R_{OUT,4} = 377.6K\Omega$$

and finally

$$g_{ds,4} = 5.2\mu S.$$

Therefore, using the equation 4.23 and knowing that $\frac{W_4}{L_4} = 1.28$ we compute W_4 and L_4,

$$L_4 = 117nm = L_3$$

and

$$W_4 = 150nm = W_3.$$

For the same reasons we explained above we keep the quotient $\frac{W_4}{L_4}$ constant and double the transistor lengths and widths, so we have,

$$L_4 = 234.3nm = L_3$$

and

$$W_4 = 0.3\mu m = W_3.$$

We also have to demonstrate in brief the **65nm PDK** but we will we simply record the results as it follows exactly the same procedure.

Bias current mirror

Taking into consideration the equtaions 4.12, 4.13 and 4.14 and the fact that $L_5 = 2L_{min} = 130nm = L_6$ and $I_{C,5} = I_{C,6} = 1$ we can easily extract,

$$I_0 = I_{BIAS} = 10\mu A$$

and

$$W_5 = W_6 = 7.68\mu m.$$

Input differential pair

In addition, using the equations 4.17, 4.18, 4.19, 4.21, 4.22, 4.23 and using the same methodology we conclude that,

$$\frac{g_{m,2}}{I_{d,2}} = 18.84V^{-1},$$

$$I_{C,2} = I_{C,1} \approx 1.08,$$

$$\frac{W_2}{L_2} = 27.3,$$

$$g_{m,2} = 94.3\mu S,$$

$$R_{OUT,2} = 188.5K\Omega,$$

$$g_{ds,2} = 10.6\mu S,$$

$$L_2 = 37.6nm = L_1$$

and

$$W_2 = 1.02\mu m = W_1.$$

However, for comparison reasons we use the same technique as in 90nm PDK and we quadruple W_2, L_2, so,

$$L_2 = 150nm = L_1$$

and

$$W_2 = 4.1\mu m = W_1.$$

Active load current mirror

Since the goal remains to reduce the effect of noise and duo to the equation 4.25 we have that,

$$\frac{g_{m,4}}{I_{d,4}} = 9.42V^{-1},$$

$$I_{C,3} = I_{C,4} = 7.5,$$

$$\frac{W_4}{L_4} = 1.58,$$

$$g_{m,4} = 4.7\mu S,$$

$$R_{OUT,4} = 377.03K\Omega$$

$$g_{ds,4} = 5.3\mu S,$$

$$L_4 = 90.08nm = L_3$$

and

$$W_4 = 143nm = W_3.$$

As we want to follow the same methodology here so that the comparison between the two technologies can be precise, we also double here W_4,L_4, so,

$$L_4 = 181.7nm = L_3$$

and

$$W_4 = 0.287\mu m = W_3.$$

Sometimes the design specifications can be difficult to achieve because they may demand incommensurate values of transistor design variables [42]. There are several optimization strategies that we can use, although it is possible that the can not provide satisfactory results, so we have to find the balance between which design specifications it is more importnt to respect and the design specification that are of secondary importance. So it's very easy to understand that the optimization method we might have to do has to do with the kind of application we have to deal with and also it is a very complicated and time-consuming procedure. As the perpose of this thesis is to create two general purpose topologies in order to understand better and compare the two given PDKs, we use a very general optimization method which is not provide a general insight into the solution of the problem but it may provide better circuit-level performances. So we are trying to tune the transistor sizes and more specifically as very good metrics of operation of OTAs is the gain performance and the current matching (as it creates offsets), we double the width and the length of OTA's transistors but for different reason each one. As OTA's gain maximized by operating input pair devices at low inversion coefficients in weak or moderate inversion for high $\frac{g_m}{I_d}$ and g_m, so we want increase the channel length of the input pair device without changing the $\frac{W}{L}$ ratio as we already have the inversion coefficient that we want. We have also already see that current matching is inversly proportional to the area of the device as we can easily suppose from the mismatch analysis of section 3.9, so we have to increase Bias

transistors as well in order to achieve the circuit currents tha we want [7]. All this attempt will have a significant cost in the circuit area for both PDKs but it is an easy way to understand the better and design more appropriate circuits in the future. Therefore in the table below are demonstrated the pre-optimized and the optimized versions of simple OTA's transistors aspect ratios.

Transistors	W/L ratio-90nm PDK pre-opt	W/L ratio-90nm PDK opt	W/L ratio-65nm PDK pre-opt	W/L ratio-65nm PDK opt
$M_5 - M_6$	$10.7\mu m/180nm$	$21.4\mu m/360nm$	$7.7\mu m/130nm$	$15.4\mu m/260nm$
$M_1 - M_2$	$6\mu m/234.6nm$	$12\mu m/470nm$	$4.1\mu m/150nm$	$8.2\mu m/300nm$
$M_3 - M_4$	$0.3\mu m/234.3nm$	$0.6\mu m/469nm$	$0.29\mu m/181.7nm$	$0.57\mu m/363.5nm$

Table 10: Aspect ratios for simple OTA transistors for both 90nm and 65nm PDKs.

Finally, if we consider as the non-ideal metric the product of the width and the length of the transistors, then we can draw two very basic conclusions before running our simulations. So, if we assume that A is the transistor area for the 90nm technology and $\bar{A}$ is the area for the 65nm technology and also A_{opt} and $\bar{A_{opt}}$ the optimized versions respectively then we have the following results.

For **90nm PDK,**

$$A_{1-2} = 2(L_1 W_1) = 2.8\mu m^2, \tag{4.26}$$

$$A_{3-4} = 2(L_3 W_3) = 0.14\mu m^2, \tag{4.27}$$

$$A_{5-6} = 2(L_5 W_5) = 3.9\mu m^2, \tag{4.28}$$

$$A = A_{1-2} + A_{3-4} + A_{5-6} = 6.8\mu m^2. \tag{4.29}$$

Also, from the above equations 4.26, 4.27, 4.28, 4.29 after optimization we have that,

$$A_{1-2-opt} = 11.4\mu m^2,$$

$$A_{3-4-opt} = 0.56\mu m^2,$$

$$A_{5-6-opt} = 15.4\mu m^2,$$

$$A_{opt} = 27.4\mu m^2.$$

So, can easily observe that after the optimization we have an increase 302.94% in the total transistor area which a an important increase and we have to examine if it is value for the results that produce.

For **65nm PDK** respectively from the above equations 4.26, 4.27, 4.28, 4.29 we have that,

$$\bar{A_{1-2}} = 1.23\mu m^2,$$

$$\bar{A_{3-4}} = 0.1\mu m^2,$$

$$\bar{A_{5-6}} = 1.9\mu m^2,$$

$$\bar{A} = 3.34\mu m^2.$$

and as we follow the same procedure after the optimization we have,

$$A_{1-\bar{2}-opt} = 4.9\mu m^2,$$

$$A_{3-\bar{4}-opt} = 0.41\mu m^2,$$

$$A_{5-\bar{6}-opt} = 7.9\mu m^2,$$

$$\bar{A_{opt}} = 13.3\mu m^2.$$

Therefore, we can observe that after the optimization procedure we have an approximately $\approx 300\%$ increase like in 90nm PDK which is reasonable as we we applied exactly the same technique. Finally, it is important to note that before every simulation performed there is a fact that we have remarkably smaller transistor area in 65nm PDK sizing for this topology with a difference with a variety of about 51.4%.

4.2.3 Results and Analysis

AC Analysis

Open-loop gain-Gain Bandwidth-Phase Margin

The open loop gain, the gain bandwidth and the phase margin were calculated and verified via simulation to provide a reference for simulation validity for both 90nm and 65nm PDKs in the same way. The theoretical circuit simulation test configuration that was used is shown in Figure 4.9 and the schematic of the circuit used to derive these results is depicted in Figure 4.47(a). Also, the Figure 4.10 is showing the gain and phase response vs. frequency on pre-optimized and optimized versions for both 90nm and 65nm, bulk CMOS technologies and in Figure 4.11 we can see the comparative results of simple OTA gain and phase response vs. frequency on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Finally, the summary of the results are found and in the table below.

Parameter	Simulation-90nm PDK pre-opt	Simulation-90nm PDK opt	Simulation-65nm PDK pre-opt	Simulation-65nm PDK opt	Unit
Open-loop gain	25.2	25.77	27.5	31	dB
GBW	142	150	116	131	MH_Z
Phase margin	89.2	84.3	90	85.92	$^\circ$

Table 11: AC analysis results for both 90nm and 65nm PDKs.

In order to derive the above results we used the theoretical analysis as defined in section 4.1 and from the equations 4.1, 4.2, 4.5 we can specify for this simple OTA structure,

$$A_0 = g_{m1,2}R_{OUT}, \tag{4.30}$$

$$GBW = \frac{g_{m1,2}}{2\pi C_L}, \tag{4.31}$$

$$PM = PM = 180^\circ - \arctan(\frac{f_{GBW}}{f_{dp}}) - \sum \arctan(\frac{f_{GBW}}{f_{ndp}}). \tag{4.32}$$

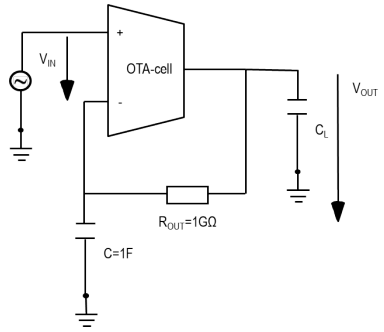


Figure 4.9: AC analysis test circuit configuration [37].

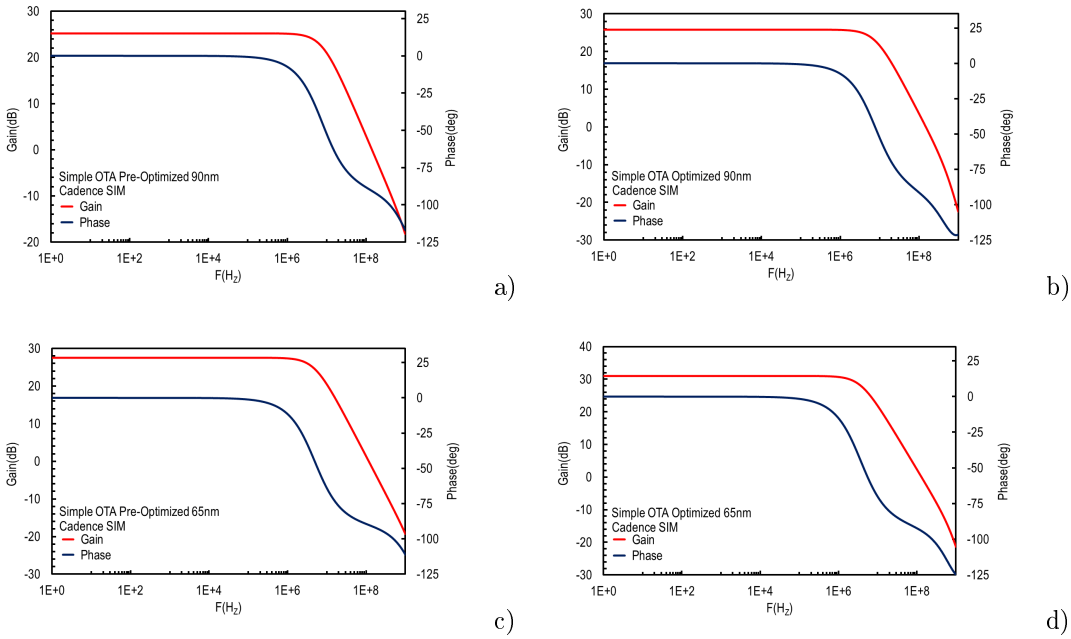


Figure 4.10: Simulated simple OTA Gain/Phase response vs. frequency on pre-optimized and optimized versions for (a), (b) 90nm and (c), (d) 65nm, bulk CMOS process.

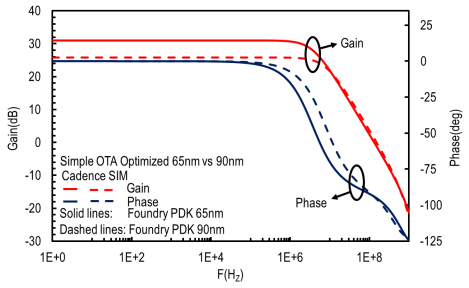


Figure 4.11: Comparative results of simple OTA Gain/Phase response vs. frequency on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Solid lines: Foundry PDK 65nm, Dashed lines: Foundry PDK 90nm.

We firstly observe that results indicate modest improvements in the open loop gain, gain bandwidth and the phase margin as a result of the optimization in both technologies. We notice that we are very close to the specification's values offered in both technologies. Also, as we know that stability requires a phase shift in the feedback signal less than 180° for open loop gain values larger than $0dB$ [4], from the results of phase margin we understand that our circuit is sufficiently stable, nevertheless as our phase margin values are more than 60°, our system is slightly under-damped, and the transient response will indicate increased slew rate at the cost of rise and fall peaking. In terms of gain, which is a criterion we are particularly interested in, we see a slightly better response in 65nm PDK and if we take into account the fact that the transistor's area is much smaller and the minor differences in the other values then we can easily conclude that in this particular analysis 65nm technology has a little better results.

Transient analysis

Slew rate

The slew rate was calculated and verified via simulation to provide a reference for simulation validity for both 90nm and 65nm PDKs in the same way. The theoretical circuit simulation test configuration that was used is shown in Figure 4.12 and the schematic of the circuit used to derive these results is depicted in Figure 4.50(a). Also, the Figure 4.13 is showing transient response on pre-optimized and optimized versions for both 90nm and 65nm, bulk CMOS technologies and in Figure 4.14 we can see the comparative results of simple OTA transient response on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Finally, the summary of the results are found and in the table below.

Parameter	Simulation-90nm PDK pre-opt	Simulation-90nm PDK opt	Simulation-65nm PDK pre-opt	Simulation-65nm PDK opt	Unit
Slew rate	$+76.1/-104$	$+65.1/-90$	$+67.3/-93$	$+66.1/-85.37$	$\frac{V}{\mu s}$

Table 12: Transient analysis results for both 90nm and 65nm PDKs.

In order to derive the above results we used the theoretical analysis as defined in section 4.1 and from the equation 4.9, we can specify for this simple OTA structure,

$$SR = \frac{I_{BIAS}}{C_L}. \tag{4.33}$$

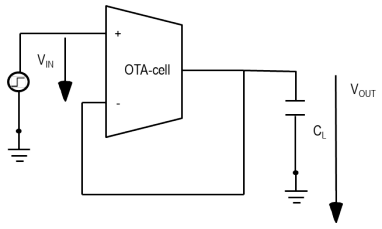


Figure 4.12: Transient analysis test circuit configuration [37].

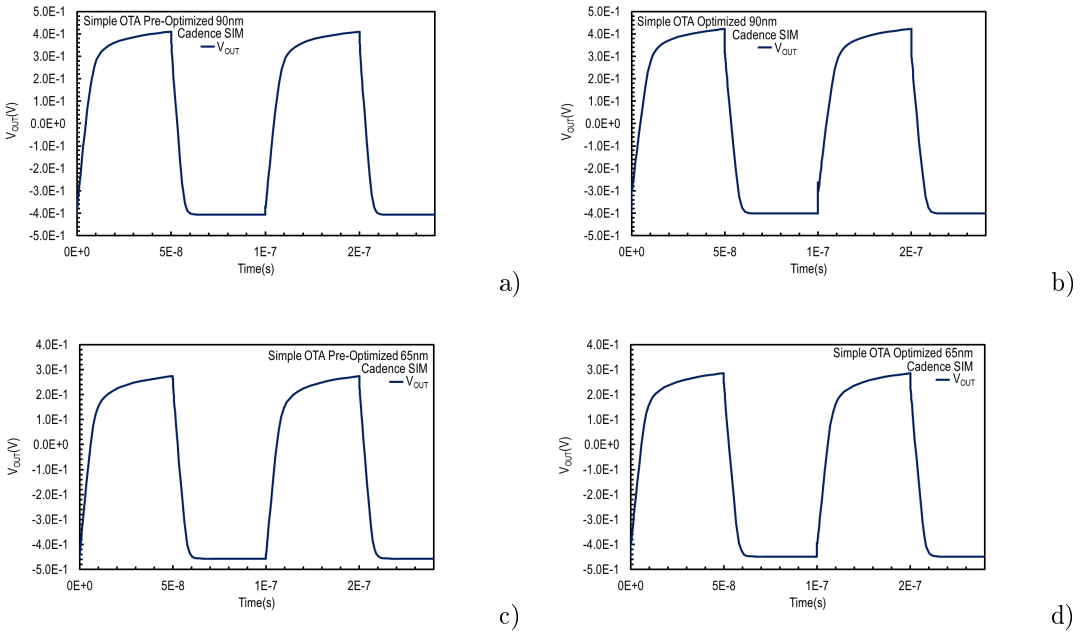


Figure 4.13: Simulated simple OTA slew rate on pre-optimized and optimized versions for (a), (b) 90nm and (c), (d) 65nm, bulk CMOS process.

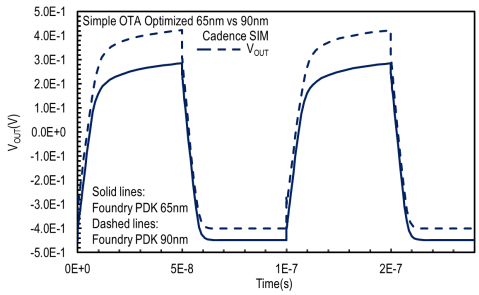


Figure 4.14: Comparative results of simple OTA slew rate on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Solid lines: Foundry PDK 65nm, Dashed lines: Foundry PDK 90nm.

Firstly, we can see that we almost meet with the given specification for both technologies. Moreover, we could also observe that after the implementation of the optimized structures we have slightly worse results in this parameter. Finally, as in AC analysis we conclude that as the results in optimized version are similar, we may prefer 65nm PDK as it has lower area cost.

DC Analysis

Input common-mode range (CMR)

The input common-mode range was calculated and verified via simulation to provide a reference for simulation validity for both 90nm and 65nm PDKs in the same way. The theoretical circuit simulation test configuration that was used is shown in Figure 4.15 and the schematic of the circuit used to derive these results is depicted in Figure 4.48(a). Also, the Figure 4.16 is showing common-mode input range vs. power supply voltage on pre-optimized and optimized versions for both 90nm and 65nm, bulk CMOS technologies and in Figure 4.17 we can see the comparative results of simple OTA common-mode input range vs. power supply voltage on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Finally, the summary of the results are found and in the table below.

Parameter	Simulation-90nm PDK pre-opt	Simulation-90nm PDK opt	Simulation-65nm PDK pre-opt	Simulation-65nm PDK opt	Unit
Input common mode range	$+0.219$ $/-0.119$	$+0.240$ $/-0.155$	$+0,084$ $/-0.214$	$+0.108$ $/-0.219$	V

Table 13: Input common mode range analysis results for both 90nm and 65nm PDKs.

In order to derive the above results we used the theoretical analysis as defined in section 4.1, and we transform the equation 4.7, for our topology. The maximum common-mode input voltage for our simple OTA shown in Figure 4.8 corresponds to the input voltage where the drain–source voltage, $V_{DS,1,}$ of the M_1 and M_2 input pair devices is equal to their drain–source saturation voltage, $V_{Dsat,1}$. An input

voltage above this causes $V_{DS,1}$ to drop below $V_{DSsat,1}$ where M_1 and M_2 enter the ohmic, linear, or triode region causing their device transconductances and drain–source resistances to begin collapsing. As a result, operation above the maximum common-mode input voltage causes a deterioration of OTA performance [7]. The maximum common-mode input voltage is given by,

$$V_{INCMR}^{+} = V_{DD} + V_{GS,2} - V_{GS,5} - V_{Dsat,2}. \tag{4.34}$$

The minimum common-mode input voltage for the simple OTA shown in Figure 4.8 corresponds to the input voltage where the drain–source voltage, $V_{DS,3}$, of the M_3, input pair current source is equal to its drain–source saturation voltage, $V_{Dsat,3}$. An input voltage below this causes $V_{DS,3}$ to drop below $V_{Dsat,3}$ where M_3 enters the ohmic, linear, or triode region. This causes a collapse in its drain–source resistance and drain current that supplies the M_1 and M_2 input pair [7]. As a result, operation below the minimum common-mode input voltage causes a deterioration of OTA performance. The minimum common-mode input voltage is given by,

$$V_{INCMR}^{-} = V_{SS} + V_{GS,2} + V_{Dsat,3}. \tag{4.35}$$

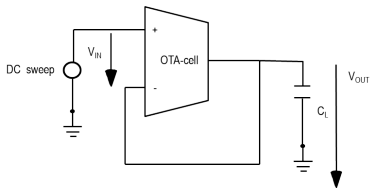


Figure 4.15: Input common mode range analysis test circuit configuration [37].

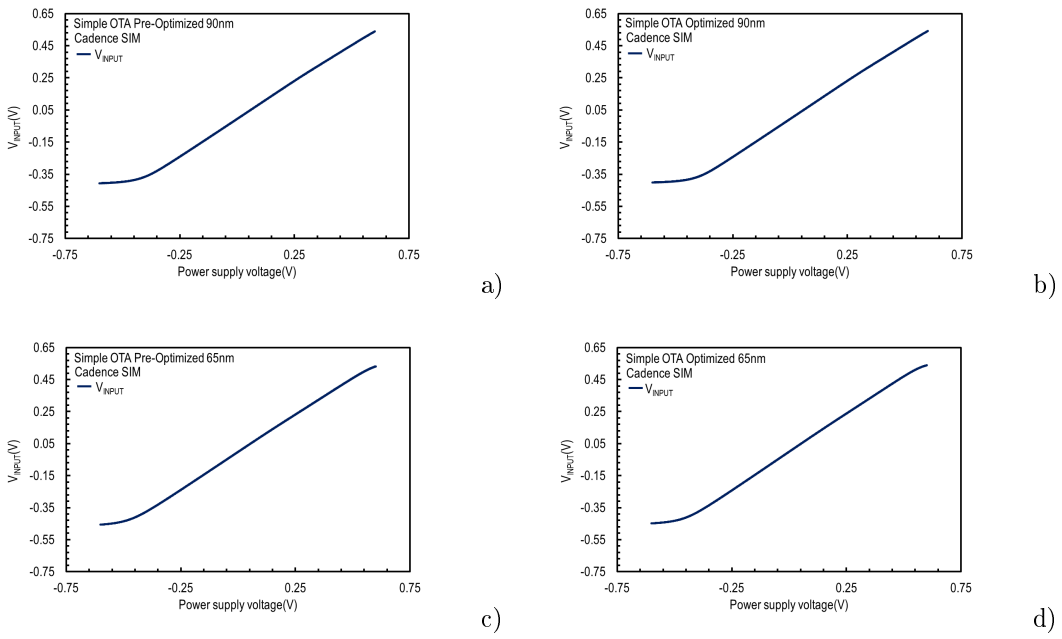


Figure 4.16: Simulated simple OTA common-mode input range vs. power supply voltage on pre-optimized and optimized versions for (a), (b) 90nm and (c), (d) 65nm, bulk CMOS process.

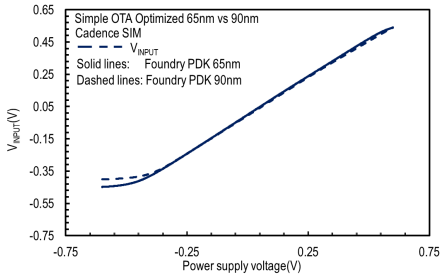


Figure 4.17: Comparative results of simple OTA common-mode input range vs. power supply voltage on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Solid lines: Foundry PDK 65nm, Dashed lines: Foundry PDK 90nm.

In this simulation it is easily deduced that the differences both after the optimizations and between the two technologies are quite small. The exception is the 65nm pre-optimized case where nevertheless we have the smallest transistor area.

Output voltage range

The output range was calculated and verified via simulation to provide a reference for simulation validity for both 90nm and 65nm PDKs in the same way. The theoretical circuit simulation test configuration that was used is shown in Figure 4.18 and the schematic of the circuit used to derive these results is depicted in Figure 4.49(a). Also, the Figure 4.19 is showing output voltage range vs. input voltage on pre-optimized and optimized versions for both 90nm and 65nm, bulk CMOS technologies and in Figure 4.20 we can see the comparative results of simple OTA output voltage range vs. input voltage on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Finally, the summary of the results are found and in the table below.

Parameter	Simulation-90nm PDK pre-opt	Simulation-90nm PDK opt	Simulation-65nm PDK pre-opt	Simulation-65nm PDK opt	Unit
Output range	$+0.242$ $/-0.142$	$+0.217$ $/-0.190$	$+0.231$ $/-0.195$	$+0.254$ $/-0.235$	V

Table 14: Output range analysis results for both 90nm and 65nm PDKs.

In order to derive the above results we used the theoretical analysis as defined in section 4.1, and we transform the equation 4.8, for our topology. The maximum output voltage for the simple OTA shown in Figure 4.8 corresponds to the output voltage where the drain–source voltage, $V_{DS,1}$, of output device M_1 is equal to its drain–source saturation voltage, $V_{Dsat,1}$. An output voltage above this causes $V_{DS,1}$ to drop below $V_{Dsat,1}$ where M_1 enters the ohmic, linear, or triode region causing a collapse in

its drain–source resistance. This results in a collapse of OTA output resistance and voltage gain [7]. The maximum output voltage is given by,

$$V_{OUT}^{+} = V_{DD} - V_{Dsat,5} - V_{Dsat,1}. \tag{4.36}$$

The minimum output voltage for the simple OTA shown in Figure 4.8 corresponds to the output voltage where the drain–source voltage, $V_{DS,4}$, of output device M_4 is equal to its drain–source saturation voltage, $V_{Dsat,4}$. An output voltage below this causes $V_{DS,4}$ to drop below $V_{Dsat,4}$ where M_4 enters the ohmic, linear, or triode region causing a collapse in its drain–source resistance. This results in a collapse of OTA output resistance and voltage gain, just like operation above V_{OUT}^{+} [7]. The minimum output voltage is given by,

$$V_{OUT}^{-} = V_{SS} + V_{Dsat,4}. \tag{4.37}$$

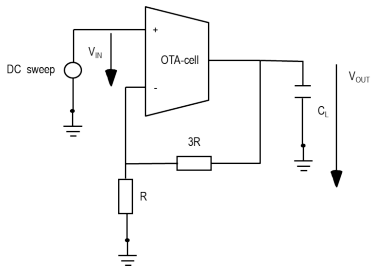


Figure 4.18: Output range analysis test circuit configuration [37].

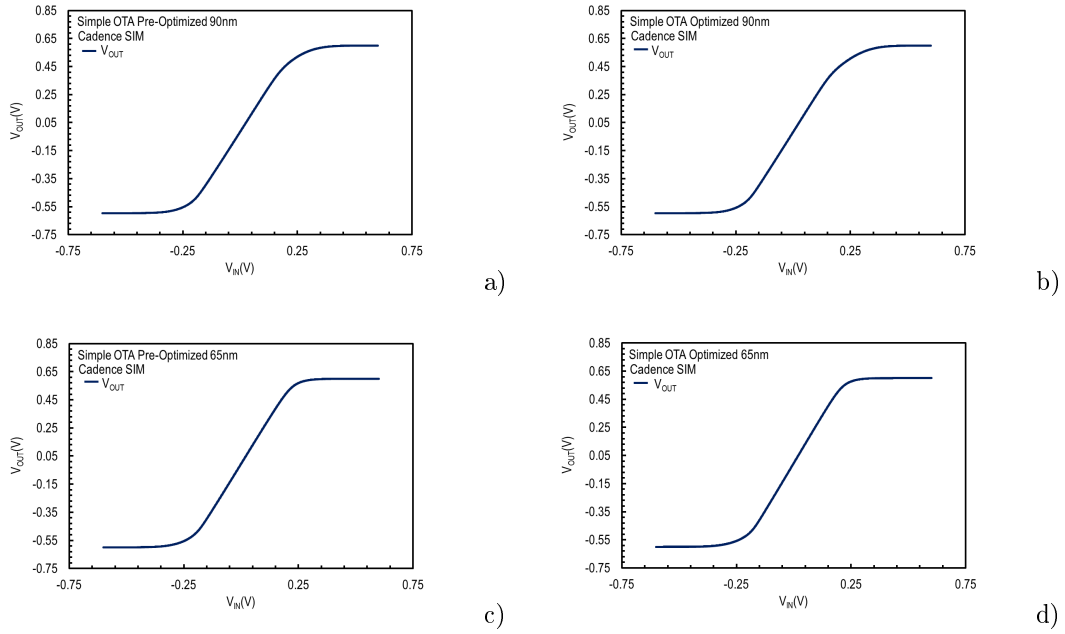


Figure 4.19: Simulated simple OTA output voltage range vs. input voltage on pre-optimized and optimized versions for (a), (b) 90nm and (c), (d) 65nm, bulk CMOS process.

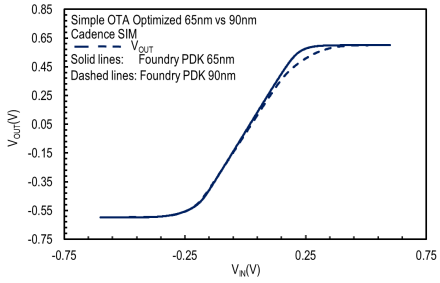


Figure 4.20: Comparative results of simple OTA output voltage range vs. input voltage on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Solid lines: Foundry PDK 65nm, Dashed lines: Foundry PDK 90nm.

One easy observation here is the fact that in both technologies and in both cases for which we ran the simulations the differencies are minor, nevertheless a remarkable output voltage headroom is observed.

Static power dissipation

As we have already referred in section 4.1, the static power dissipation is the product of the sum of the currents flowing through the current sources or sinks with the power supply voltages, in our case we have the current sources and supply voltages for both 90nm and 65nm PDKs and as a result the circuit's power consumption in both cases is given by the equation 4.6 as follows,

$$P_{STATIC} = (V_{DD-}V_{SS})2I_{BIAS} = 1.2V210\mu A = 24\mu W. \tag{4.38}$$

Parameter	Simulation-90nm,65nm PDKs	Unit
Static power dessipation	24	μW

Table 15: Power consumption analysis results for both 90nm and 65nm PDKs.

Therefore, the power comsumption in this circuit is low enough for a lot of applications. This is an important metric as in the majority of applications high gain, high bandwidth or speed, high accuracy, and low power consumption are desired.

Basic operating points and current matching

In order to examine the theoretical results, analyze OTA performance in detail and especially the current matching in this structure, we print the basic operating points as they are shown below,

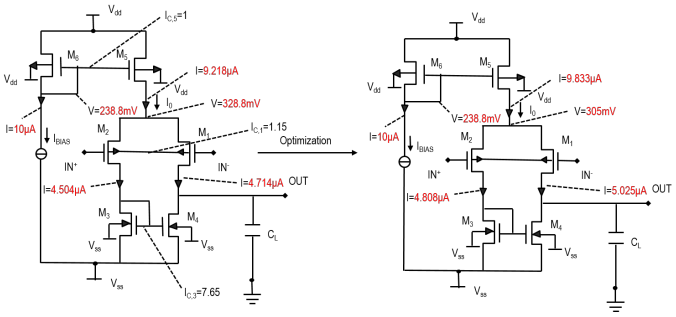


Figure 4.21: Basic operating points and current matching of simple one stage OTA of 90nm PDK.

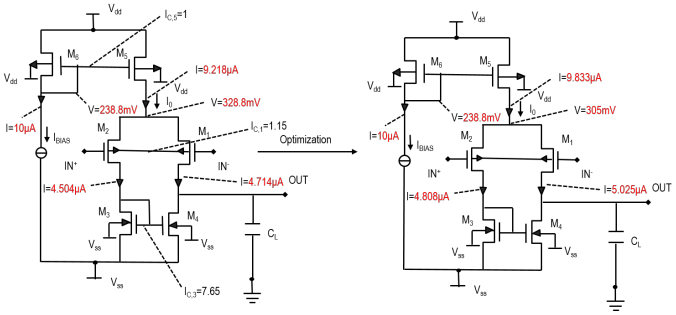


Figure 4.22: Basic operating points and current matching of simple one stage OTA of 65nm PDK.

One simple observation is the following: while there is a fairly good convergence of the ideal theoretical values, marginally improved results can be noticed in the 65nm technology. However, there is a slight divergence on the device current matching which, as already mentioned in section 4.1, creates some issues in circuit operation such as systematic offsets. We could also easily observe that after the optimization technique is used in both technologies, the current mismatch is decreased enough and that is happening due to the fact that matching is inversely proportional to the area of the device, as derived from the mismatch analysis of section 3.9. Therefore, in order to achieve a given matching precision, we have to design large enough components. In this case, an important trade-off between precision and circuit area is raised.

4.3 Fully Differential Folded Cascode OTA (FDFC OTA)

4.3.1 Theoretical Design and operation

Fully differential circuits are widely used due to their large available signal swing, and superior supply and substrate interference immunity. A fully differential architecture of folded cascode OTA is also selected as it suppresses the even harmonics which are dominant in single ended OTA structure and also because of its higher common mode rejection ratio (CMRR) and improved dynamic range. So, we need them to be able to reject the common mode disturbances. However, the disadvantage of this topology is that an extra circuit will be required to stabilize in order to set the value of the common-mode output voltage which is usually around midway between the power-supply voltages to allow maximum signal swing. It is called the common-mode feedback (CMFB) circuit which it obviously takes additional current [28, 59, 60].

In this section we will design and simulate the fully differential folded cascode OTA and an "ideal" CMFB circuit, which are shown in Figure 4.23 and Figure 4.24 .

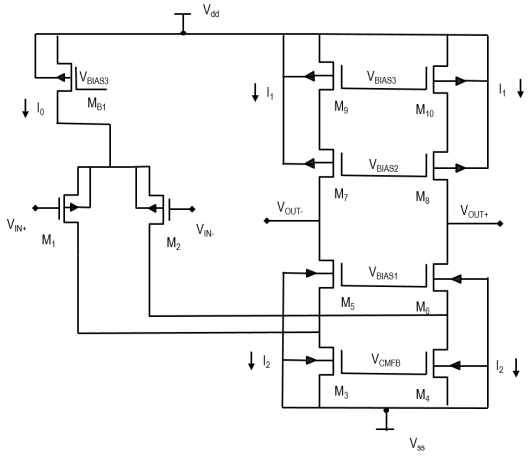


Figure 4.23: Fully Differential Folded Cascode (FDFC) OTA structure [37].

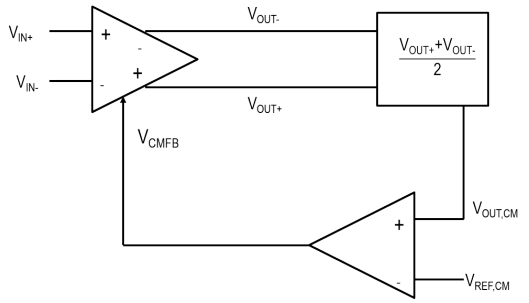


Figure 4.24: Block diagram of Common mode feedback circuit [37].

The architecture and operation of the fully differential OTA is similar to that of its single ended with the following construction exceptions. The differential amplifier of the above figure is composed of a PMOS M_1, M_2 differential pair where the common terminal of the source is polarized by a PMOS M_{B1} transistor, its purpose is to determine as independently as possible the polarization currents of the two input transistors from the common input current levels. Also the differential pair has an active load from cascode current mirrors of differential output. More specifically, the active load of the PMOS differential pair consists of the NMOS cascode current mirrors M_3, M_4,M_5, M_6. The current mirrors are polarized by external voltage sources V_{BIAS1}, V_{BIAS2}, V_{BIAS3} and V_{CMFB}. Finally, the external voltage source V_{BIAS3} polarizes the M_{B1} transistor which polarizes the differential input pair.

In the Common Mode Feedback Circuits, the common mode output voltage is stabilized by sensing the common mode output voltage and using negative feedback to adjust the common mode voltage to the desired value. The Figure 4.23 shows the block diagram of the "ideal" common mode feedback circuit (CMFB) required for the fully differential OTA structure. The Common-Mode Feed-Back (CMFB), shown here, performs three operation: it senses the common-mode output signal

$V_{OUT,CM} = (V_{OUT+} + V_{OUT-})/2$, then compares is it with the reference voltage $V_{REF,CM}$ and generates a control voltage V_{CMFB}. The $V_{REF,CM}$ voltage is usually chosen as $(V_{DD} - V_{SS})/2$, which is in the middle of the supply voltage range, in order to achieve the maximal output swing. Finally the control voltage V_{CMFB} drives the differential amplifier in such a way that the common-mode output signal is corrected, but the differential output signal is not affected. Therefore, the differential output signal is independent of the common-mode output signal. Nevertheless, the common-mode output signal can be sensitive to the differential output signal if a circuit that detects $V_{OUT,CM}$ or the CMFB amplifier is not linear.

These circuits are simulated for the same specifications but with the appropriate sizing in Cadence Virtuoso IC 6.15 environment for both 65nm and 90nm PDKs as is already mentioned in section 4.2. The schematic used in order to simulate these circuits are shown in Figure 4.45 and Figure 4.46.

4.3.2 Specifications and sizing

The circuit is designed to meet the following specifications, which will be verified by simulation for both 65nm and 90nm technologies.

Parameter	Specifications	Unit
Technology	$65, 90$	nm
Supply Voltage	$+/-0.6$	V
Open-loop gain	> 50	dB
GBW	150	MH_Z
Slew Rate	100	$\frac{V}{\mu s}$
Load capacitance	100	fF

Table 16: FDFC OTA parameters design specifications [37].

The next step is to size step by step this FDFC OTA, in order to do this calculations we use the calculated parameters of the section 3. They are demonstrated for both technologies in the Table 8 and also the basic physical constants used, are shon in Table 9 in the previous section. All the calculations of the parameters that used in this section of the thesis are calculated in Matlab as shown in Appendix section A.1 and they are explained below.

For the reasons discussed in detail in the preceding section, moderate inversion is used here as well. In order to size our topology properly, the circuit of the Figure 4.22 is partitioned into the following basic analog structures:

- A PMOS biasing transistor,
- a PMOS input differential pair,
- two PMOS cascode load current mirrors,
- and two NMOS folded load current mirrors.

We will firstly demonstrate the sizing methodology for the 90nm PDK and then we will show more briefly the sizing of the 65nm PDK as we follow exactly the same procedure exactly in the same way as in the previous section [37].

Bias currents-Differential pair

In order to compute these currents we took into account the specified slew rate, the power consumption and the load capacitance and from the equation 4.9 we have,

$$I_{BIAS} = I_0 = SRC_L \Longrightarrow I_{BIAS} = 10\mu A. \tag{4.39}$$

Also we can easy define $I_{d,1}$ as,

$$I_{d,1} = \frac{I_{BIAS}}{2} = 5\mu A,$$

also solving the equation 4.2 we have that,

$$g_{m,1} = 2\pi C_L GBW = 94.25\mu S \tag{4.40}$$

and

$$\frac{g_{m,1}}{I_{d,1}} = 18.84V^{-1}. \tag{4.41}$$

Therefore, using the following equation and several different methods such as linear interpolation as it shown in Appendix section A.1 we can compute $I_{C,1} = I_{C,2}$,

$$\frac{g_{m,1}}{I_{d,1}} = \frac{1}{n_p U_T} \frac{1}{2n_p + \sqrt{I_{C,2} + \frac{1}{4}}} \Longrightarrow I_{C,1} = I_{C,2} \approx 1.15, \tag{4.42}$$

in the next step, we can define the ratio $\frac{W_1}{L_1}$ modifying the current equation and we use the equation 4.19, as we have already seen in previous section,

$$\frac{W_1}{L_1} = \frac{I_{d,1}}{I_{C,1} 2n_p U_T^2 k_{P,p}} = 25.9. \tag{4.43}$$

Folded cascoded current mirrors

Now, the 8 transistors of the folded cascode stage will be sized. We choose an inversion factor in the center of moderate inversion for the transistors M_9, M_{10}, M_7, M_8 M_5, M_6, as we have already referred in the previous section we want to maintain small saturation voltages and keep the area consumption reasonable. On the other hand, we choose a bigger inversion factor but in the upper limits of moderate inversion, for the transistors M_3, M_4, as we want to minimize the noise contribution. So, from the equation 4.43 and the fact that $I_{d,5} = I_{d,7} = I_{d,9} = \frac{I_{BIAS}}{2} = 5\mu A$ we have that,

$$I_{C,5} = I_{C,6} = 1 \Longrightarrow \frac{W_5}{L_5} = 9.8,$$

$$I_{C,7} = I_{C,8} = 1 \Longrightarrow \frac{W_7}{L_7} = 29.8,$$

$$I_{C,9} = I_{C,10} = 1 \Longrightarrow \frac{W_9}{L_9} = 29.8,$$

and as we now that $I_{d,3} = I_{d,1} + \frac{I_{BIAS}}{2} = 10\mu A$ then,

$$I_{C,3} = I_{C,4} = 10 \Longrightarrow \frac{W_3}{L_3} = 1.97.$$

The output resistance R_{OUT} is the parallel equivalent of the output resistance of the PMOS cascode mirrors R_{UP} and the output resistance of the NMOS cascode mirrors R_{DOWN} [1],

$$R_{OUT} = R_{UP} \Big|\Big| R_{DOWN}, \tag{4.44}$$

So as we know that $r_0 = \frac{1}{g_{ds}}$,

$$R_{UP} = g_{m,7} r_{0,7} r_{0,9} \Longrightarrow R_{UP} = \frac{g_{m,7}}{g_{ds,7} g_{ds,9}} \tag{4.45}$$

and

$$R_{DOWN} = g_{m,5} r_{0,5} (r_{0,3} \Big|\Big| r_{0,2}) \Longrightarrow R_{DOWN} = \frac{g_{m,5}}{g_{ds,5}(g_{ds,1} + g_{ds,3})}. \tag{4.46}$$

Combining the above equations we can now find the R_{OUT} after converting the specified open-loop gain from dB to $\frac{V}{V}$,

$$A_V = 10^{\frac{50}{20}} = 316.22 \frac{V}{V} \tag{4.47}$$

and

$$R_{OUT} = \frac{A_V}{g_{m,1}} = 3.35 M\Omega. \tag{4.48}$$

Since we ignore the conductivity of the differential pair due to the fact that we want the differential pair length to be small in order to achieve the highest possible $\frac{W}{L}$ ratio, $n_n \approx n_p$ respected the conditions mentioned, we can calculate the following,

$$I_{C,5} = I_{C,7} \Longrightarrow g_{m,5} \approx g_{m,7} \approx \frac{1}{n_p U_T} \frac{i_{d,7}}{\frac{1}{2} + \sqrt{\frac{1}{4} + I_{C,7}}} = 97.9 \mu S. \tag{4.49}$$

As we can choose $g_{ds,5} = g_{ds,7}$ and $g_{ds,3} = g_{ds,9}$ in order to balance the conductances and as we know that $u_{a,p}$ is almost equal to $u_{a,n}$ and from the following equations,

$$g_{ds,3} = \frac{I_{d,3}}{U_{a,n} L_3}, \tag{4.50}$$

$$g_{ds,5} = \frac{I_{d,5}}{U_{a,p} L_5}, \tag{4.51}$$

$$g_{ds,7} = \frac{I_{d,7}}{U_{a,n} L_7}, \tag{4.52}$$

$$g_{ds,9} = \frac{I_{d,9}}{U_{a,p} L_9} \tag{4.53}$$

and $I_{d,5} = I_{d,7}$, $I_{d,3} = 2 I_{d,9}$ we can assume that $L_5 = L_7$, $L_3 = 2 L_9$ and $R_{UP} = R_{DOWN} = 2 R_{OUT} = 6.7 M\Omega$, we can also compute the following,

$$R_{UP} = \frac{g_{m,7}}{\frac{I_{d,7} I_{d,9}}{U_{a,p} L_7 U_{a,p} L_9}} \Longrightarrow L_7 L_9 = \frac{I_{d,7} I_{d,9} R_{UP}}{g_{m,7} U_{a,p}^2} = 0.0264 \mu m^2 \tag{4.54}$$

and

$$L_7 = L_9 = \sqrt{L_7 L_9} = 162.5 nm = L_8 = L_{10}. \tag{4.55}$$

Following the same procedure for the other two current mirrors and from the equation 4.54 we have that,

$$L_3 L_5 = \frac{R_{DOWN} I_{d,3} I_{d,5}}{g_{m,5} U_{a,n}^2} = 0.0527 \mu m^2 \tag{4.56}$$

and

$$L_3 = \sqrt{2 L_3 L_5} = 325 nm = L_4. \tag{4.57}$$

Now, we can compute the width of all current mirrors transistors from the equations below,

$$I_{C,3} = \frac{I_{d,3}}{2n_n U_T^2 K_{p,n} \frac{W_3}{L_3}} \Longrightarrow W_3 = \frac{I_{d,3} L_3}{I_{C,3} 2n_n U_T^2 K_{P,n}} = 640.3nm = W_4, \tag{4.58}$$

$$I_{C,5} = \frac{I_{d,5}}{2n_n U_T^2 K_{p,n} \frac{W_5}{L_5}} \Longrightarrow W_5 = \frac{I_{d,5} L_5}{I_{C,5} 2n_n U_T^2 K_{P,n}} = 1.6\mu m = W_6, \tag{4.59}$$

$$I_{C,7} = \frac{I_{d,7}}{2n_p U_T^2 K_{p,p} \frac{W_7}{L_7}} \Longrightarrow W_7 = \frac{I_{d,7} L_7}{I_{C,7} 2n_p U_T^2 K_{P,p}} = 4.84\mu m = W_8, \tag{4.60}$$

and

$$I_{C,9} = \frac{I_{d,9}}{2n_p U_T^2 K_{p,p} \frac{W_9}{L_9}} \Longrightarrow W_9 = \frac{I_{d,9} L_9}{I_{C,9} 2n_p U_T^2 K_{P,p}} = 4.84\mu m = W_{10}. \tag{4.61}$$

Differential pair finalization-Current source

In order to determine the differential's pair size we choose a small $L_1 = 200nm = L_2$, so we can now compute W_1,

$$W_1 = L_1 \frac{W_1}{L_1} = 5.18\mu m = W_2. \tag{4.62}$$

Transistors M_{B1} and M_9, M_{10} usually need to be matched to avoid the current mismatch, so as we know that $I_{C,9} = I_{C,B1}$ and $I_{d,1} = \frac{I_{BIAS}}{2}$ then,

$$\frac{W_{B1}}{L_{B1}} = \frac{2W_9}{L_9} \tag{4.63}$$

So,

$$L_{B1} = L_9 = 162.5nm \tag{4.64}$$

and

$$W_{B1} = 2W_9 = 9.68\mu m. \tag{4.65}$$

Sizing of other design bias transistors-sizing of the "ideal" CMFB transistor

Besides the theoretical calculation we have seen so far, here we have to size some extra transistors in the Cadence simulation. In order to size M_{20}, M_{21} PMOS transistors we choose $I_{C,20} = I_{C,21} = 1$, in moderate inversion as the other PMOS bias transistor and also $L_{20} = L_{21} = 162.5nm$. As we know that $I_{d,20} = I_{d,21} = 5\mu A$, we can find $W_{20}$and W_{21} from the following equation,

$$I_{C,20} = \frac{I_{d,20}}{2n_p U_T^2 K_{P,p} \frac{W_{20}}{L_{20}}} \Longrightarrow W_{20} = 4.84\mu m = W_{21}. \tag{4.66}$$

So we have to size also the M_{11} transistor of the "ideal" CMFB circuit in the Cadence simulation. In order to size M_{11} NMOS transistor we choose $I_{C,11} = I_{C,3} = 10$, in strong inversion as the other NMOS transistor of the current mirror and also $L_{11} = L_3 = 325nm$. As we know that $I_{d,11} = I_{dc} = 5\mu A$, we can find W_{11} from the following equation,

$$I_{C,11} = \frac{I_{d,11}}{2n_n U_T^2 K_{P,n} \frac{W_{11}}{L_{11}}} \Longrightarrow W_{11} = 320nm. \tag{4.67}$$

We also have to demonstrate in brief the **65nm PDK** but we will we simply record the results as it follows exactly the same procedure.

Bias currents-Differential pair

Following the same procedure as in 90nm PDK and from the equations 4.39, 4.40, 4.41, 4.42, 4.43, we have that,

$$I_{BIAS} = I_0 = 10\mu A,$$

$$g_{m,1} = 94.24\mu S,$$

$$\frac{g_{m,1}}{I_{d,1}} = 18.84V^{-1},$$

$$I_{C,1} = 1.08,$$

and

$$\frac{W_1}{L_1} = 27.4.$$

Folded cascoded current mirrors

For the reasons analyzed in detail in the 90nm PDK sizing procedure, knowing that $I_{d,5} = I_{d,7} = I_{d,9} = \frac{I_{BIAS}}{2} = 5\mu A$ and from the equation 4.43 we have that,

$$I_{C,5} = I_{C,6} = 1 \Longrightarrow \frac{W_5}{L_5} = 11.9,$$

$$I_{C,7} = I_{C,8} = 1 \Longrightarrow \frac{W_7}{L_7} = 29.6,$$

$$I_{C,9} = I_{C,10} = 1 \Longrightarrow \frac{W_9}{L_9} = 29.6,$$

and as we now that $I_{d,3} = I_{d,1} + \frac{I_{BIAS}}{2} = 10\mu A$ then,

$$I_{C,3} = I_{C,4} = 10 \Longrightarrow \frac{W_3}{L_3} = 2.4.$$

After that, if we analyze the output resistance R_{OUT} in the same way as in 90nm technology and convert the specified open-loop gain from dB to $\frac{V}{V}$ using the equation 4.47 we conlude that,

$$A_V = 316.22\frac{V}{V},$$

$$R_{OUT} = 3.35M\Omega$$

and

$$g_{m,5} = g_{m,7} = 96.4\mu S.$$

Here, we as we have a slight differentiation in the relation of NMOS and PMOS early voltages $U_{a,p} = 1.2U_{a,n}$ and $L_5 = 1.2L_7$,$L_3 = 2.4L_9$ converting the equations 4.54, 4.56 we have that ,

$$L_7L_9 = 0.011\mu m^2$$

and

$$L_7 = L_9 = 105nm = L_8 = L_{10}.$$

Also,

$$L_3 L_5 = 0.033\mu m^2,$$

$$L_3 = 2.4L_9 = 2.4L_7 = \frac{2.4}{1.2}L_5 = 2L_5,$$

$$L_3 = \sqrt{2(L_3 L_5)} = 254nm = L_4,$$

and

$$L_5 = \frac{L_3}{2} = 127nm = L_6.$$

Therefore, we can compute the width of all current mirrors transistors from the equations 4.58, 4.59, 4.60, 4.61 as follows,

$$W_3 = \frac{I_{d,3}L_3}{I_{C,3}2n_n U_T^2 K_{P,n}} = 604nm = W_4,$$

$$W_5 = \frac{I_{d,5}L_5}{I_{C,5}2n_n U_T^2 K_{P,n}} = 1.5\mu m = W_6,$$

$$W_7 = \frac{I_{d,7}L_7}{I_{C,7}2n_p U_T^2 K_{P,p}} = 3.1\mu m = W_8,$$

and

$$W_9 = \frac{I_{d,9}L_9}{I_{C,9}2n_p U_T^2 K_{P,p}} = 3.1\mu m = W_{10}.$$

Differential pair finalization-Current source

In order to determine the differential's pair size we choose a small $L_1 = 150nm = L_2$, so from the equation 4.62, we can now compute W_1,

$$W_1 = 4.1\mu m = W_2$$

Transistors M_{B1} and M_9, M_{10} usually need to be matched to avoid the current mismatch as we have already referred, so as we know that $I_{C,9} = I_{C,B1}$ and $I_{d,1} = \frac{I_{BIAS}}{2}$ and from the equations 4.63, 4.64, 4.65 then,

$$\frac{W_{B1}}{L_{B1}} = \frac{2W_9}{L_9}$$

So,

$$L_{B1} = L_9 = 105nm$$

and

$$W_{B1} = 2W_9 = 6.2\mu m.$$

Sizing of other design bias transistors-sizing of the "ideal" CMFB transistor

As we have already explained in 90nm PDK sizing procedure except for the theoretical calculation we have seen so far, here we have to size some extra transi stors in the Cadence simulation. In order to size M_{20}, M_{21} PMOS transistors we choose $I_{C,20} = I_{C,21} = 1$, in moderate inversion as the other PMOS bias transistor and also $L_{20} = L_{21} = 105nm$. As we know that $I_{d,20} = I_{d,21} = 5\mu A$, we can find $W_{20}$and W_{21} from the equation 4.66,

$$W_{20} = 3.1\mu m = W_{21}.$$

Moreover, we have to size also the M_{11} transistor of the "ideal" CMFB circuit in the Cadence simulation. In order to size M_{11} NMOS transistor we choose $I_{C,11} = I_{C,3} = 10$, in strong inversion as the other NMOS transistor of the current mirror and also $L_{11} = L_3 = 254nm$. As we know that $I_{d,11} = I_{dc} = 5\mu A$, we can find W_{11} from the equation 4.67,

$$W_{11} = 302nm.$$

For the reasons described in detail in the previous section, we follow an universal design optimization and choose to double the width and length of the input differential pair transistors M_1, M_2 and also the width and the length of the NMOS current mirror M_3, M_4.

Transistors	W/L ratio-90nm PDK pre-opt	W/L ratio-90nm PDK opt	W/L ratio-65nm PDK pre-opt	W/L ratio-65nm PDK opt
M_{B1}	$9.68\mu m/162.5nm$	$9.68\mu m/162.5nm$	$6.2\mu m/125nm$	$6.2\mu m/125nm$
$M_1 - M_2$	$5.18\mu m/200nm$	$10.4\mu m/400nm$	$4.1\mu m/150nm$	$8.2\mu m/300nm$
$M_9 - M_{10}$	$4.84\mu m/162.5nm$	$4.84\mu m/162.5nm$	$3.1\mu m/105nm$	$3.1\mu m/105nm$
$M_7 - M_8$	$4.84\mu m/162.5nm$	$4.84\mu m/162.5nm$	$3.1\mu m/105nm$	$3.1\mu m/105nm$
$M_5 - M_6$	$1.6\mu m/162.5nm$	$1.6\mu m/162.5nm$	$1.5\mu m/127nm$	$1.5\mu m/127nm$
$M_3 - M_4$	$640.3nm/325nm$	$1.2\mu m/650nm$	$604nm/254nm$	$1.2\mu m/508nm$

Table 17: Aspect ratios for FDFC OTA transistors for both 90nm and 65nm PDKs.

Finally, as in the previous section if we consider as the non-ideal metric the product of the width and the length of the transistors, then we can draw two very basic conclusions before running our simulations. So, if we assume that A is the transistor area for the 90nm technology and $\bar{A}$ is the area for the 65nm technology and also A_{opt} and $\bar{A_{opt}}$ the optimized versions respectively then we have the following results.

For **90nm PDK,**

$$A_{B1} = L_{B1}W_{B1} = 1.57\mu m^2, \tag{4.68}$$

$$A_{1-2} = 2(L_1W_1) = 2.072\mu m^2, \tag{4.69}$$

$$A_{3-4} = 2(L_3W_3) = 0.41\mu m^2, \tag{4.70}$$

$$A_{5-6} = 2(L_5W_5) = 0.52\mu m^2, \tag{4.71}$$

$$A_{7-8} = 2(L_7W_8) = 1.57\mu m^2, \tag{4.72}$$

$$A_{9-10} = 2(L_9W_9) = 1.57\mu m^2, \tag{4.73}$$

$$A = A_{B1} + A_{1-2} + A_{3-4} + A_{5-6} + A_{7-8} + A_{9-10} = 7.73\mu m^2. \tag{4.74}$$

Also, from the above equations 4.69, 4.70, 4.71,4.72, 4.73, 4.74 after optimization we have that,

$$A_{B1-opt} = 1.57\mu m^2,$$

$$A_{1-2-opt} = 8.28\mu m^2,$$

$$A_{3-4-opt} = 1.66\mu m^2,$$

$$A_{5-6-opt} = 0.52\mu m^2,$$

$$A_{7-8-opt} = 1.57\mu m^2,$$

$$A_{9-10-opt} = 1.57\mu m^2,$$

$$A_{opt} = 15.1\mu m^2.$$

So, can easily observe that after the optimization we have an increase 95.34% in the total transistor area which a an important increase and we have to examine if it is value for the results that produce.

For **65nm PDK** respectively from the above equations 4.69, 4.70, 4.71, 4.72, 4.73, 4.74 we have that,

$$\bar{A_{B1}} = 0.65\mu m^2,$$

$$\bar{A_{1-2}} = 1.23\mu m^2,$$

$$\bar{A_{3-4}} = 0.31\mu m^2,$$

$$\bar{A_{5-6}} = 0.38\mu m^2,$$

$$\bar{A_{7-8}} = 0.65\mu m^2,$$

$$\bar{A_{9-10}} = 0.65\mu m^2,$$

$$\bar{A} = 3.89\mu m^2.$$

and as we follow the same procedure after the optimization we have,

$$\bar{A_{B1-opt}} = 0.65\mu m^2,$$

$$\bar{A_{1-2-opt}} = 4.92\mu m^2,$$

$$\bar{A_{3-4-opt}} = 1.22\mu m^2,$$

$$\bar{A_{5-6-opt}} = 0.38\mu m^2,$$

$$\bar{A_{7-8-opt}} = 0.65\mu m^2,$$

$$\bar{A_{9-10-opt}} = 0.65\mu m^2,$$

$$\bar{A_{opt}} = 8.5\mu m^2.$$

Therefore, we can observe that after the optimization procedure we have an approximately $\approx 118\%$ increase like in 90nm PDK which is reasonable as we we applied exactly the same technique. Finally, it is important to note that before every simulation performed there is a fact that we have remarkably smaller transistor area in 65nm PDK sizing for this topology with a difference with a variety of about 77.64%.

4.3.3 Results and Analysis

AC Analysis

Open-loop gain-Gain Bandwidth-Phase Margin

The open loop gain, the gain bandwidth and the phase margin were calculated and verified via simulation to provide a reference for simulation validity for both 90nm and 65nm PDKs in the same way. The theoretical circuit simulation test configuration that was used is shown in Figure 4.25 and the schematic of the circuit used to derive these results is depicted in Figure 4.47(b). Also, the Figure 4.26 is showing the gain and phase response vs. frequency on pre-optimized and optimized versions for both 90nm and 65nm, bulk CMOS technologies and in Figure 4.27 we can see the comparative results of FDFC OTA gain and phase response vs. frequency on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Finally, the summary of the results are found and in the table below.

Parameter	Simulation-90nm PDK pre-opt	Simulation-90nm PDK opt	Simulation-65nm PDK pre-opt	Simulation-65nm PDK opt	Unit
Open-loop gain	43.88	45.33	44.74	47.11	dB
GBW	166	183	131	142	MH_Z
Phase margin	86.66	83.42	87.73	85.57	$^\circ$

Table 18: AC analysis results for both 90nm and 65nm PDKs.

In order to derive the above results we used the theoretical analysis as defined in section 4.1 and from the equations 4.1, 4.2, 4.5 we can specify for this FDFC OTA structure,

$$A_0 = g_{m1,2} R_{OUT}, \tag{4.75}$$

where we know from the equations 4.44, 4.45, 4.46 that $R_{OUT} = R_{UP} || R_{DOWN}$

$$GBW = \frac{g_{m1,2}}{2\pi C_L}, \tag{4.76}$$

$$PM = PM = 180^\circ - \arctan(\frac{f_{GBW}}{f_{dp}}) - \sum \arctan(\frac{f_{GBW}}{f_{ndp}}). \tag{4.77}$$

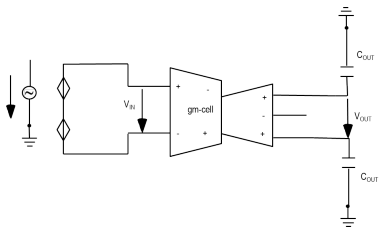


Figure 4.25: AC analysis test circuit configuration [37].

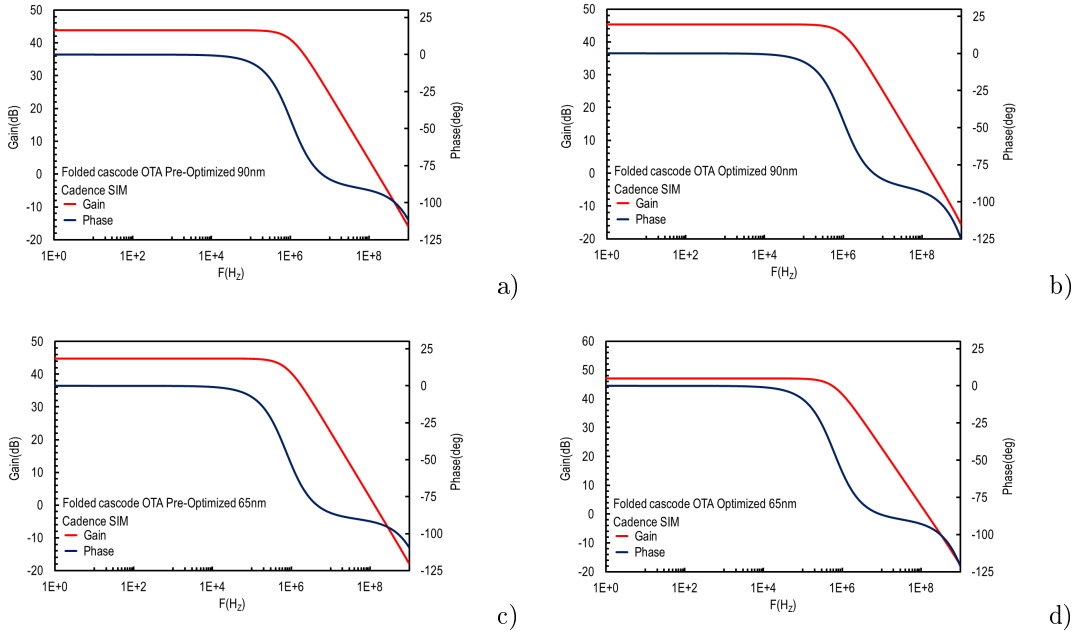


Figure 4.26: Simulated fully differential folded cascode OTA Gain/Phase response vs. frequency on pre-optimized and optimized versions for (a), (b) 90nm and (c), (d) 65nm, bulk CMOS process.

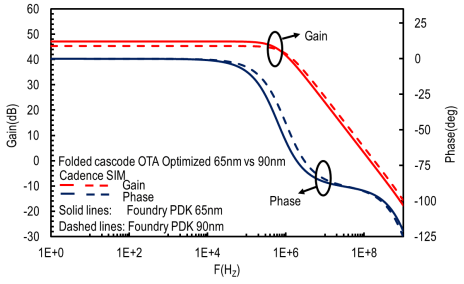


Figure 4.27: Comparative results of fully differential folded cascode OTA Gain/Phase response vs. frequency on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Solid lines: Foundry PDK 65nm, Dashed lines: Foundry PDK 90nm.

We firstly observe that results indicate mediocre improvements in the open loop gain, gain bandwidth and the phase margin as a result of the optimization in both technologies. In terms of gain, which is a criterion we are particularly interested in, we see a slightly better response in 65nm PDK and if we take into account the fact that the transistor's area is much smaller and the minor differencies in the other values then we can easily conclude that in this particular analysis 65nm technology has a little better results. Finally, is should be mentioned that this topology has better response than in simple OTA topology.

Transient analysis

Slew rate

The slew rate was calculated and verified via simulation to provide a reference for simulation validity for both 90nm and 65nm PDKs in the same way. The theoretical circuit simulation test configuration that was used is shown in Figure 4.28 and the schematic of the circuit used to derive these results is depicted in Figure 4.50(b). Also, the Figure 4.29 is showing transient response on pre-optimized and optimized versions for both 90nm and 65nm, bulk CMOS technologies and in Figure 4.30 we can see the comparative results of FDFC OTA transient response on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Finally, the summary of the results are found and in the table below.

Parameter	Simulation-90nm PDK pre-opt	Simulation-90nm PDK opt	Simulation-65nm PDK pre-opt	Simulation-65nm PDK opt	Unit
Slew rate	$+100/-99$	$+100/-97$	$+74.95/-97.48$	$+80.3/-97.73$	$\frac{V}{\mu s}$

Table 19: Transient analysis results for both 90nm and 65nm PDKs.

In order to derive the above results we used the theoretical analysis as defined in section 4.1 and from the equation 4.9, we can specify for this FDFC OTA structure,

$$SR = \frac{I_{BIAS}}{C_L}. \tag{4.78}$$

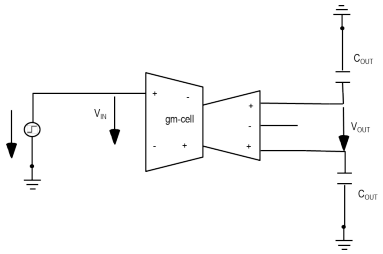


Figure 4.28: Transient analysis test circuit configuration [37].

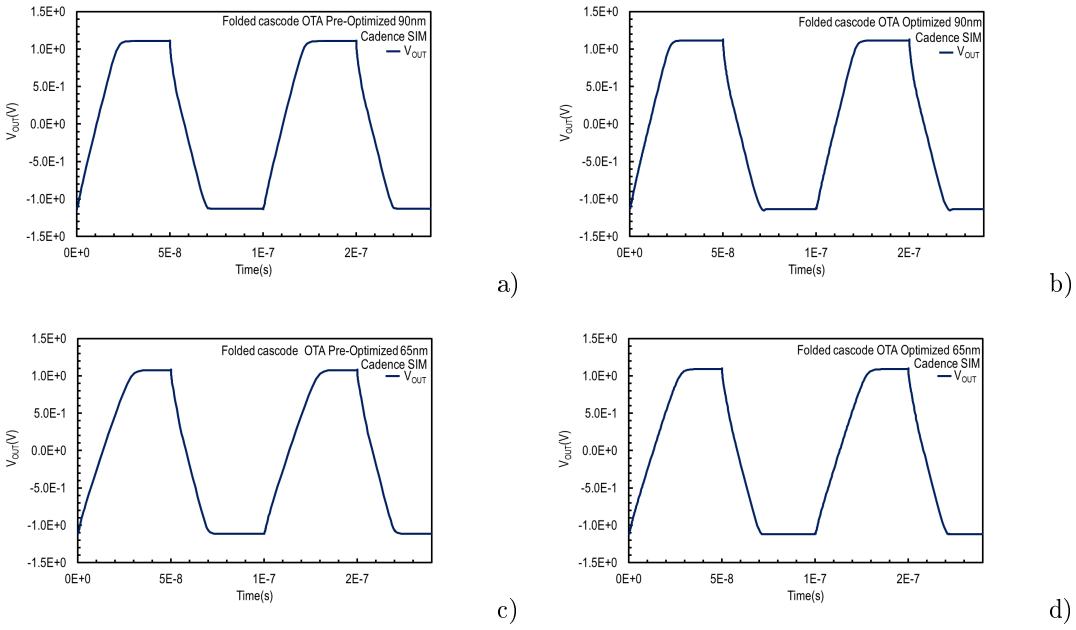


Figure 4.29: Simulated fully differential folded cascode OTA slew rate on pre-optimized and optimized versions for (a), (b) 90nm and (c), (d) 65nm, bulk CMOS process.

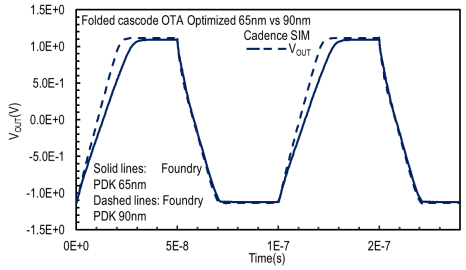


Figure 4.30: Comparative results of fully differential folded cascode OTA slew rate on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Solid lines: Foundry PDK 65nm, Dashed lines: Foundry PDK 90nm.

We can easily observe that we almost meet up the given specification for both technologies. Also, we could observe that after the implementation of the optimized structures we have slightly worse results in 90nm PDK and slightly better results in 65nm PDK. Finally, as in AC analysis we conclude that as the results in optimized version are similar, we may prefer 65nm PDK as it has lower area cost besides the fact tha 90nm PDK has slightly better response. Finally, is should be mentioned that this topology has better response that in simple OTA topology.

DC Analysis

Input common-mode range (CMR)

The input common-mode range was calculated and verified via simulation to provide a reference for simulation validity for both 90nm and 65nm PDKs in the same way. The theoretical circuit simulation

test configuration that was used is shown in Figure 4.31 and the schematic of the circuit used to derive these results is depicted in Figure 4.48(b). Also, the Figure 4.32 is showing common-mode input range vs. power supply voltage on pre-optimized and optimized versions for both 90nm and 65nm, bulk CMOS technologies and in Figure 4.33 we can see the comparative results of FDFC OTA common-mode input range vs. power supply voltage on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Finally, the summary of the results are found and in the table below.

Parameter	Simulation-90nm PDK pre-opt	Simulation-90nm PDK opt	Simulation-65nm PDK pre-opt	Simulation-65nm PDK opt	Unit
Input common mode range	$+0.092$ $/-0.337$	$+0.129$ $/-0.343$	$+0.167$ $/-0.357$	$+0.184$ $/-0.345$	V

Table 20: Input common mode range analysis results for both 90nm and 65nm PDKs.

In order to derive the above results we used the theoretical analysis as defined in section 4.1, and we transform the equation 4.7, for our topology. The maximum common-mode input voltage for the FDFC OTAs shown in Figure 4.23, like the maximum input voltage for the simple OTAs, corresponds to the input voltage where the drain–source voltage of the M_1 and M_2 input pair devices is equal to their drain–source saturation voltage [7]. The maximum common-mode input voltage is then given by

$$V_{INCMR}^{+} = V_{DD} - V_{Dsat,B11} - V_{GS,1}. \tag{4.79}$$

The minimum common-mode input voltage for the FDFC OTA shown in Figure 4.23, like the minimum input voltage for the simple OTA, corresponds to the input voltage where the drain–source voltage of the input pair current source is equal to its drain–source saturation voltage [7]. The minimum common-mode input voltage is then given by

$$V_{INCMR}^{-} = V_{SS} + V_{Dsat,3} + V_{Dsat,1} - V_{GS,1}. \tag{4.80}$$

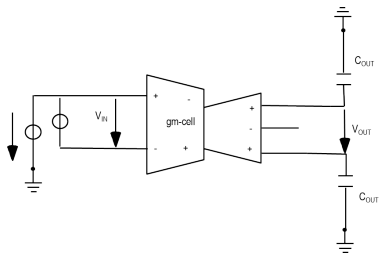


Figure 4.31: Input common mode range analysis test circuit configuration [37].

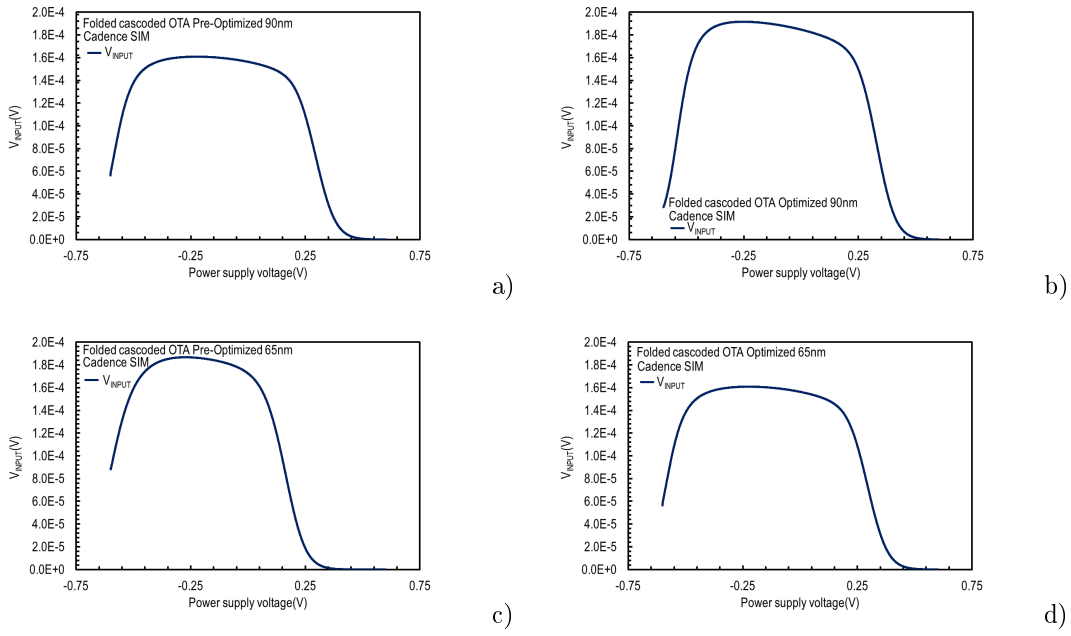


Figure 4.32: Simulated fully differential folded cascode OTA common-mode input range vs. power supply voltage on pre-optimized and optimized versions for (a), (b) 90nm and (c), (d) 65nm, bulk CMOS process.

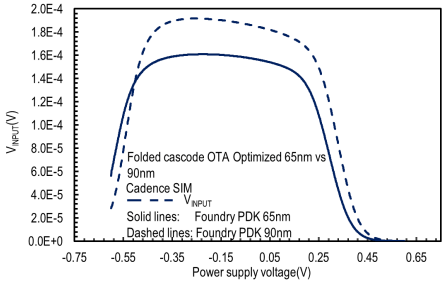


Figure 4.33: Comparative results of fully differential folded cascode OTA common-mode input range vs. power supply voltage on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Solid lines: Foundry PDK 65nm, Dashed lines: Foundry PDK 90nm.

We firstly observe that results indicate mediocre improvements in the common-mode input range as a result of the optimization in both technologies. We could also see a slightly better response in 65nm PDK and if we take into account the fact that the transistor's area is much smaller in 65nm PDK then we can easily conclude that in this particular analysis 65nm technology has a little better results. Finally, is should be mentioned that this topology has better response that in simple OTA topology and it is possibly influenced by the CMFB circuit.

Output voltage range

The output range was calculated and verified via simulation to provide a reference for simulation validity for both 90nm and 65nm PDKs in the same way. The theoretical circuit simulation test

configuration that was used is shown in Figure 4.34 and the schematic of the circuit used to derive these results is depicted in Figure 4.49(b). Also, the Figure 4.35 is showing output voltage range vs. input voltage on pre-optimized and optimized versions for both 90nm and 65nm, bulk CMOS technologies and in Figure 4.36 we can see the comparative results of FDFC OTA output voltage range vs. input voltage on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Finally, the summary of the results are found and in the table below.

Parameter	Simulation-90nm PDK pre-opt	Simulation-90nm PDK opt	Simulation-65nm PDK pre-opt	Simulation-65nm PDK opt	Unit
Output range	$+0.325$ $/-0.316$	$+0.297$ $/-0.289$	$+0.187$ $/-0.178$	$+0.172$ $/-0.162$	V

Table 21: Output range analysis results for both 90nm and 65nm PDKs.

In order to derive the above results we used the theoretical analysis as defined in section 4.1, and we transform the equation 4.8, for our topology. The maximum output voltage for the cascoded OTAs shown in Figure 4.23, like the maximum output voltage for the simple OTAs, corresponds to the output voltage where the drain–source voltage of the positive-side output device is at its drain–source saturation value [7]. The maximum OTA output voltage is then given by

$$V_{OUT}^{+} = V_{DD} - V_{Dsat,7} - V_{Dsat,9}. \tag{4.81}$$

The minimum output voltage for the cascoded OTAs shown in Figure 5.2, like the minimum output voltage for the simple OTAs, corresponds to the output voltage where the drain–source voltage of the negative-side output device is at its drain–source saturation value [7]. The minimum output voltage is then given by,

$$V_{OUT}^{-} = V_{SS} + V_{Dsat,4} + V_{Dsat,6}. \tag{4.82}$$

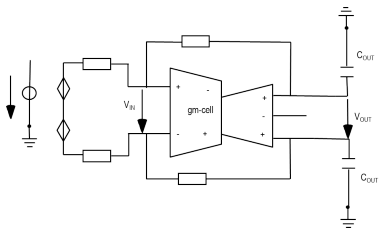


Figure 4.34: Output range analysis test circuit configuration [37].

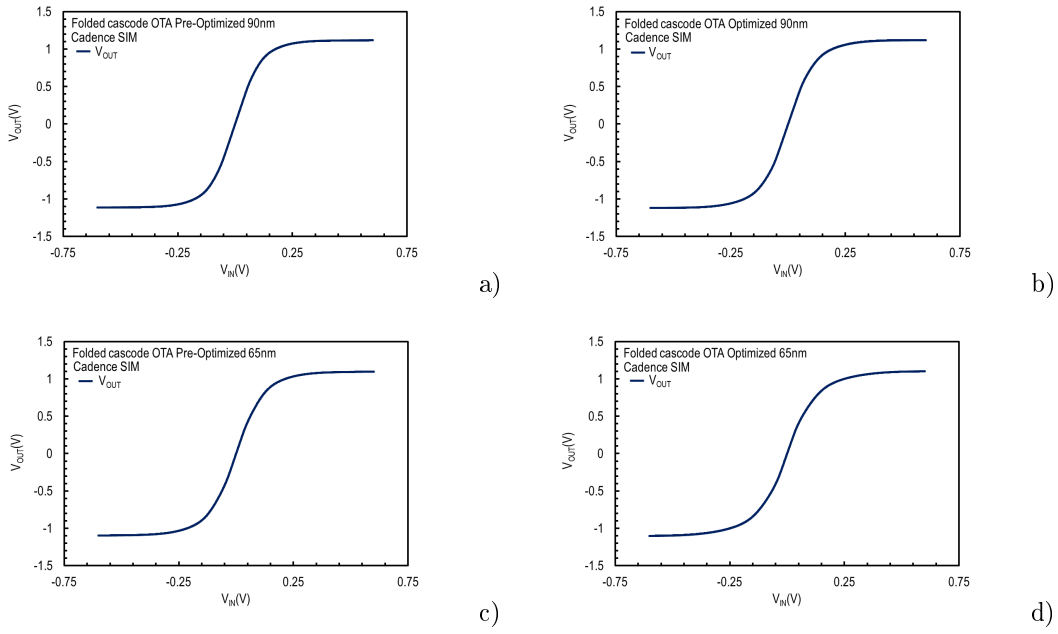


Figure 4.35: Simulated fully differential folded cascode OTA output voltage range vs. input voltage on pre-optimized and optimized versions for (a), (b) 90nm and (c), (d) 65nm, bulk CMOS process.

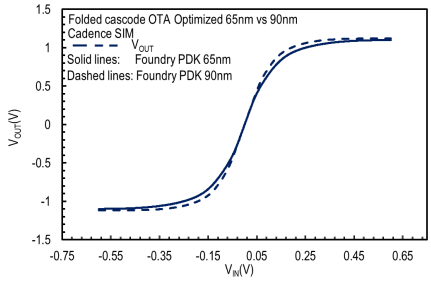


Figure 4.36: Comparative results of fully differential folded cascode OTA output voltage range vs. input voltagee on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Solid lines: Foundry PDK 65nm, Dashed lines: Foundry PDK 90nm.

An observation here is the fact that in both technologies and in both cases for which we ran the simulations the differencies after the optimization are minor, slightly better response in 90nm PDK is noticed. However, a remarkable output voltage headroom is observed in both PDKs. Finally, is should be mentioned that this topology has better response that in simple OTA topology and it is possibly influenced by the CMFB circuit.

Static power dissipation

As we have already referred in section 4.1, the static power dissipation is the product of the sum of the currents flowing through the current sources or sinks with the power supply voltages, in our case we have the current sources and supply voltages for both 90nm and 65nm PDKs and as a result the circuit's power comsumption in both cases is given by the equation 4.6 as follows,

$$P_{STATIC} = (V_{DD-}V_{SS})(I_{BIAS} + 2I_{d,1}) = 1.2V(10 + 10)\mu A = 24\mu W. \tag{4.83}$$

Parameter	Simulation- 90nm,65nm PDKs	Unit
Static power dessipation	24	μW

Table 22: Power comsumption analysis results for both 90nm and 65nm PDKs.

Results indicate equal static power dissipation for single ended and fully differential architectures, the power comsumption in this circuit is low enough for a lot of applications and as it has overall better performance from simple OTA structure, this parameter is even more important.

Basic operating points and current matching

In order to examine the theoretical results and to analyze FDFC OTA performance in detail, we print the basic operating points as they are shown below,

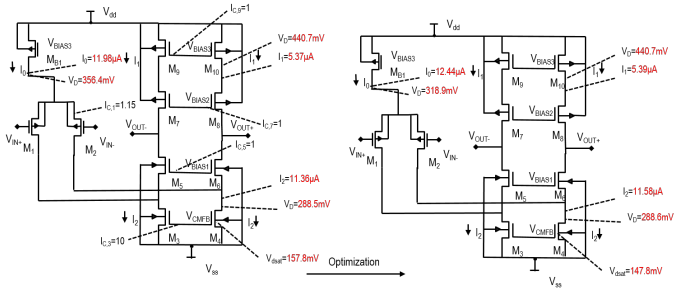


Figure 4.37: Basic operating points and current matching of simple one FDFC OTA of 90nm PDK.

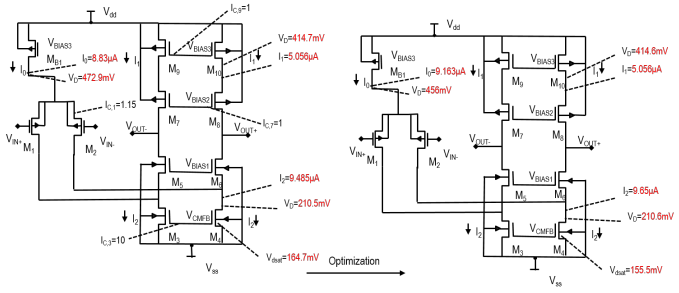


Figure 4.38: Basic operating points and current matching of simple one stage FDFC OTA of 65nm PDK.

It is important to note here that due to the structure of topology in both technologies we observe that there is no remarkable current mismatch in pair devices, however it exists some deviation in the other values of the circuit, nevertheless are greatly improved after the optimization technique is implemented.

Noise simulation

The total input noise was calculated and verified via simulation to provide a reference for simulation validity for both 90nm and 65nm PDKs in the same way. The theoretical circuit simulation test configuration that was used is shown in Figure 4.39 and the schematic of the circuit used to derive these results is depicted in Figure 4.51. Also, the Figure 4.40 is showing voltage noise (rms)/ Power spectral density (PSD) vs. frequency on pre-optimized and optimized versions in both bulk CMOS technologies and in Figure 4.41 we can see the comparative results of FDFC OTA OTA voltage noise (rms)/ Power spectral density (PSD) vs. frequency on optimized versions for both 90nm and 65nm technologies. Finally, the summary of the results are found and in the table below.

Parameter	Simulation-90nm PDK pre-opt	Simulation-90nm PDK opt	Simulation-65nm PDK pre-opt	Simulation-65nm PDK opt	Unit
Total input noise (rms)	0.544	0.418	0.464	0.374	mV

Table 23: Noise analysis results for both 90nm and 65nm PDKs.

In order to derive the above results we used the theoretical analysis as defined in section 4.1, and we transform the equation 4.10, for our topology,

$$V_n^2 = 2V_{n,1,2}^2 + 2(\frac{g_{m,3,4}}{g_{m1,2}})V_{n,3,4}^2 + 2(\frac{g_{m,9,10}}{g_{m1,2}})V_{n,9,10}^2. \tag{4.84}$$

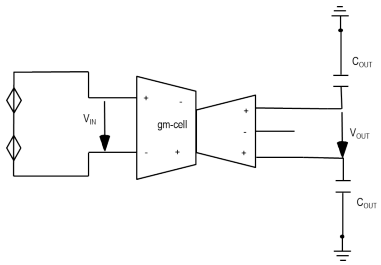


Figure 4.39: Noise analysis test circuit configuration [37].

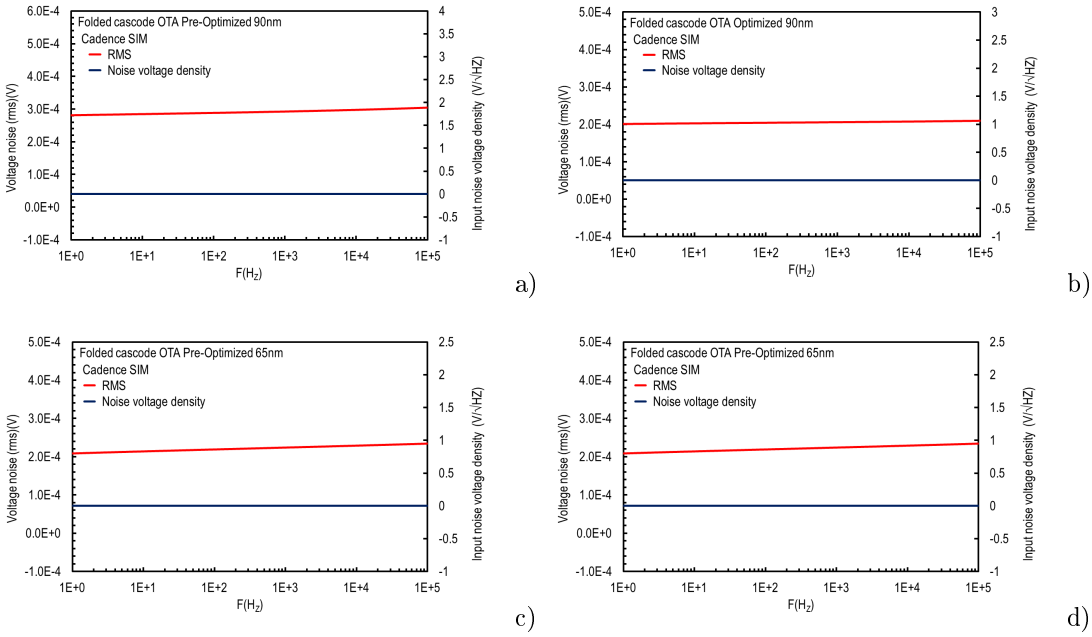


Figure 4.40: Simulated fully differential folded cascode OTA voltage noise (rms)/ Input noise voltage density vs. frequency on pre-optimized and optimized versions for (a), (b) 90nm and (c), (d) 65nm, bulk CMOS process.

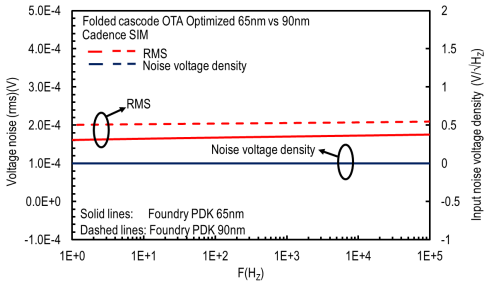


Figure 4.41: Comparative results of fully differential folded cascode OTA voltage noise (rms)/ Input noise voltage density vs. frequency on optimized versions for 65nm vs. 90nm bulk CMOS technologies. Solid lines: Foundry PDK 65nm, Dashed lines: Foundry PDK 90nm.

We could observe that optimized values are better for both PDKs, nevertheless 65nm PDK has better response. Also, input noise results plots show a decrease in noise as a result of the addition of common mode feedback circuit.

Input offset voltage

The input offset voltage was calculated and verified via simulation to provide a reference for simulation validity for both 90nm and 65nm PDKs in the same way. The theoretical circuit simulation test configuration that was used is shown in Figure 4.42 and the schematic of the circuit used to derive these results is depicted in Figure 4.52, the most frequently used distribution is Gaussian which was also used here but the method is appropriate for any kind of distribution [34], so, for this thesis we used a special simulator tool (Cadence Virtuoso IC 6.15-ADEXL) in order to extract our results. Also, the Figure 4.43 FDFC OTA input offset voltage distribution on pre-optimized and optimized versions for 90nm and 65nm, bulk CMOS process. Finally, the summary of the results are found and in the table below.

Parameter	Simulation-90nm PDK pre-opt	Simulation-90nm PDK opt	Simulation-65nm PDK pre-opt	Simulation-65nm PDK opt	Unit
Mean value (μ)	0.264	0.027	0.083	0.204	mV
Standard deviation (σ)	13.79	8.37	12.77	7.35	mV
Maximum value (3σ)	41.37	25.11	38.31	22.05	mV

Table 24: Noise analysis results for both 90nm and 65nm PDKs.

In order to derive the above results we used the theoretical analysis as defined in section 4.1, and we transform the equation 4.11, for our topology,

$$V_o^2 = \sigma(\delta V_{G,1,2}) + 2(\frac{g_{m,3,4}}{g_{m1,2}})\sigma(\delta V_{G,3,4}) + 2(\frac{g_{m,9,10}}{g_{m1,2}})\sigma(\delta V_{G,9,10}). \tag{4.85}$$

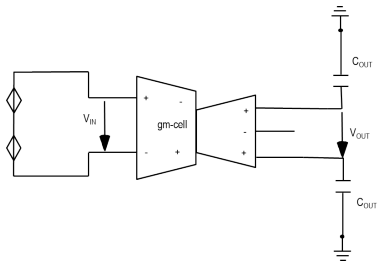


Figure 4.42: Input offset voltage analysis test circuit configuration [37].

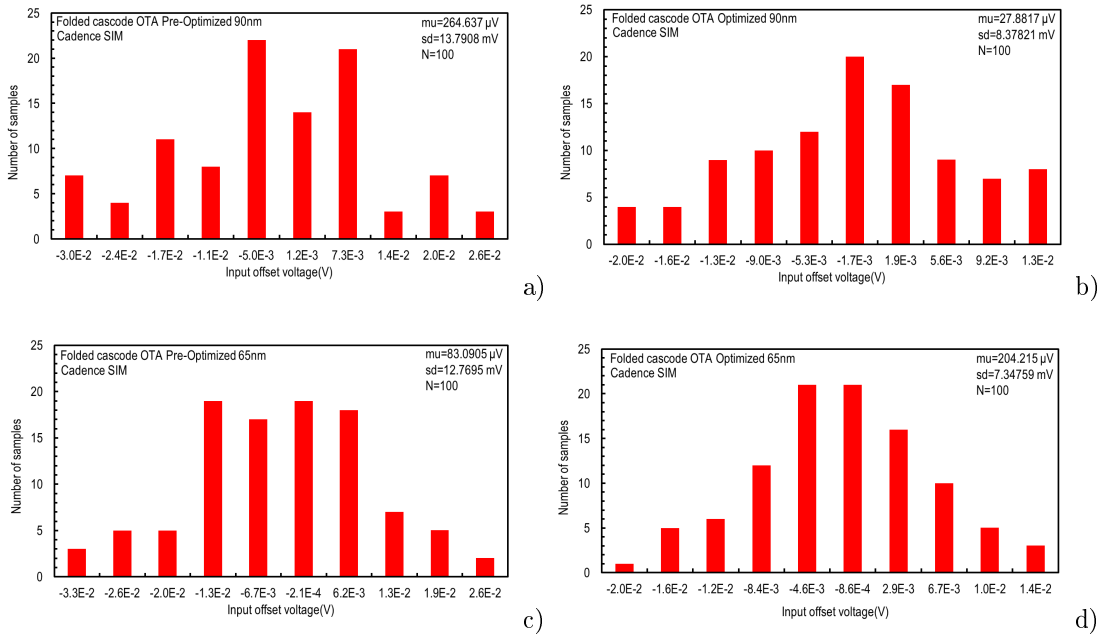


Figure 4.43: Simulated fully differential folded cascode OTA input offset voltage distribution on pre-optimized and optimized versions for (a), (b) 90nm and (c), (d) 65nm, bulk CMOS process.

We could see that the optimization is very important for both PDKs for this parameter also, 65nm PDK has slightly better performance and overall results indicate a reduction in the offset voltage which is supposed due to the CMFB circuit.

4.4 Comparative results of the technology parameters

The Table 5 and the Table 6 show in detail the results of the implementation of the different OTA parameters for the simple and the FDFC OTAs of the two technologies 65nm and 90nm respectively.

Parameter	Simulation-90nm PDK pre-opt	Simulation-90nm PDK opt	Simulation-65nm PDK pre-opt	Simulation-65nm PDK opt	Unit
Open-loop gain	25.2	25.77	27.5	31.05	dB
GBW	142	150	116	131	MH_Z
Phase Margin	89.2	84.33	90.01	85.92	$^\circ$
Slew Rate	$+76.1/-104$	$+65.1/-90$	$+67.3/-93$	$+66.1/-85.37$	$\frac{V}{\mu s}$
Input CMR	$+0.219/-0.119$	$+0.240/-0.155$	$+0.084/-0.214$	$+0.108/-0.219$	V
Output range	$+0.242/-0.142$	$+0.217/-0.190$	$+0.231/-0.195$	$+0.254/-0.235$	V
Power dessipation	24	24	24	24	μW

Table 25: Simple OTA design parameters.

Parameter	Simulation-90nm PDK pre-opt	Simulation-90nm PDK opt	Simulation-65nm PDK pre-opt	Simulation-65nm PDK opt	Unit
Open-loop gain	43.88	45.33	44.74	47.11	dB
GBW	166	183	131	142	MH_Z
Phase margin	86.66	83.42	87.73	85.57	$^\circ$
Slew rate	$+100/-99$	$+100/-97$	$+74.95/-97.48$	$+80.3/-97.73$	$\frac{V}{\mu s}$
Input CMR	$+0.092/-0.337$	$+0.129/-0.343$	$+0.167/-0.357$	$+0.184/-0.345$	V
Output range	$+0.325/-0.316$	$+0.297/-0.289$	$+0.187/-0.178$	$+0.172/-0.162$	V
Total input noise (rms)	0.544	0.418	0.464	0.394	mV
mean value (μ) (offset)	0.264	0.027	0.083	0.204	mV
Power dessipation	24	24	24	24	μW

Table 26: FDFC OTA design parameters.

4.5 Cadence simulation schematics

All the schematic simulations (Cadence Virtuoso IC 6.15) used to extract the design parameters of the circuits analyzed above are presented below.

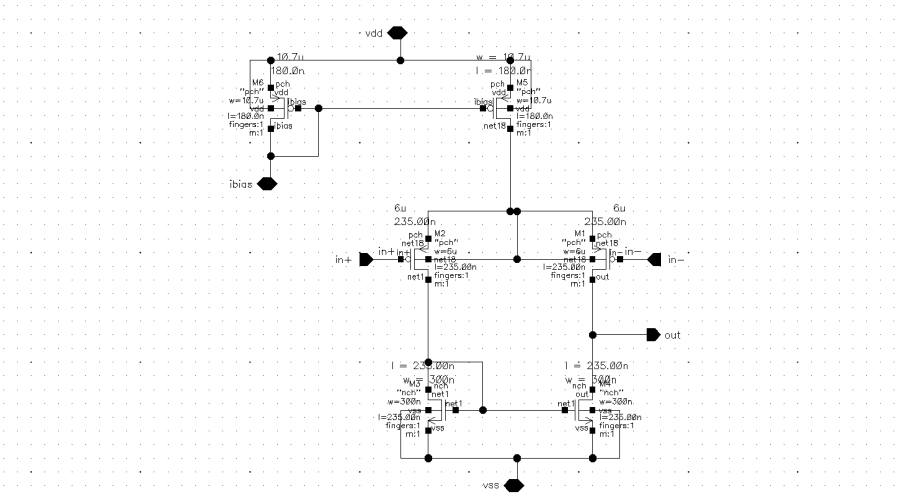


Figure 4.44: Simple OTA schematic for 90nm and 65nm, bulk CMOS technologies [37].

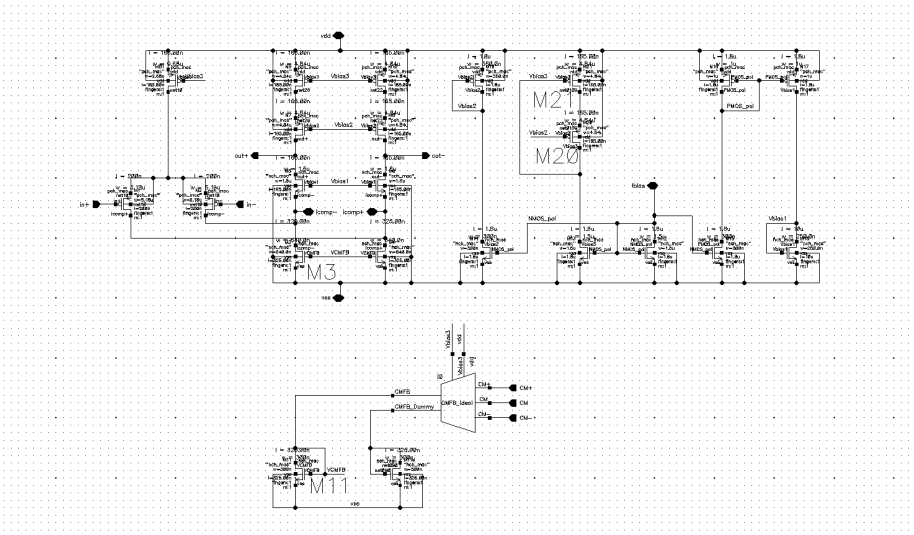


Figure 4.45: Fully differential folded coscode OTA schematic for 90nm and 65nm, bulk CMOS technologies [37].

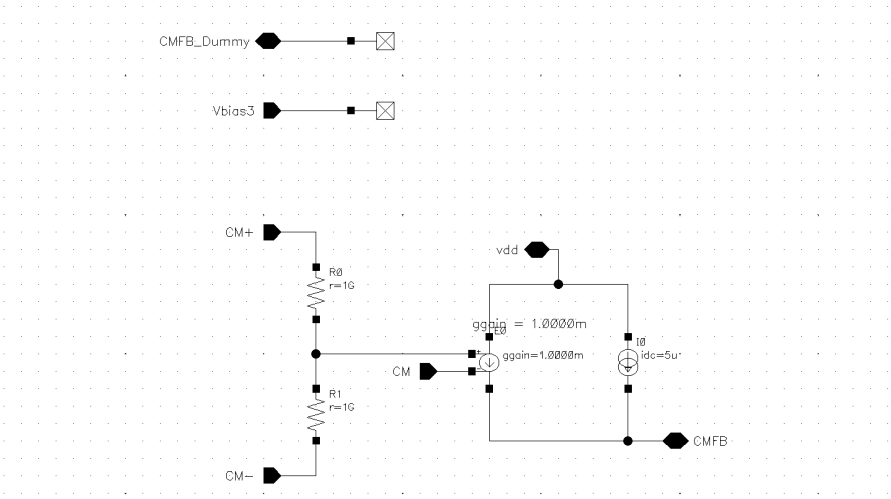


Figure 4.46: Ideal Common Mode Feedback Circuit (CMFB) schematic for 90nm and 65nm, bulk CMOS technologies [37].

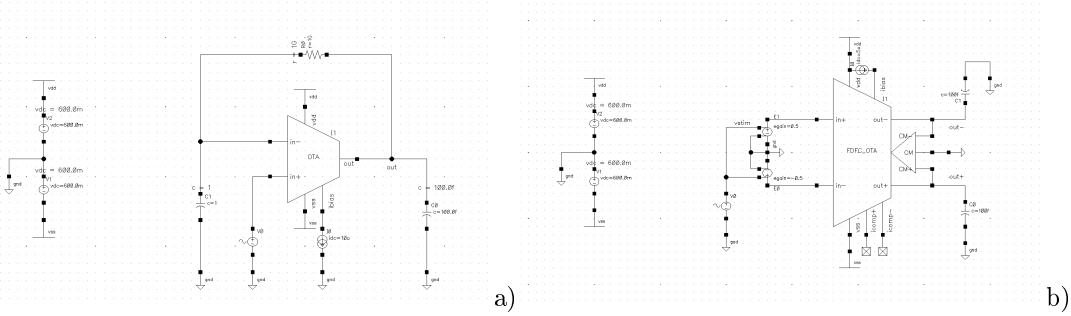


Figure 4.47: AC analysis schematics of (a) simple OTA and (b) fully differential folded coscode OTA for 90nm and 65nm, bulk CMOS technologies [37].

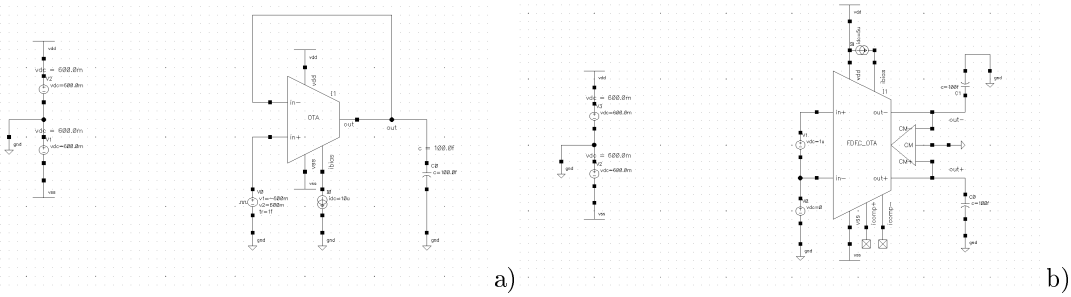


Figure 4.48: Input CMR schematics of (a) simple OTA and (b) fully differential folded coscode OTA for 90nm and 65nm, bulk CMOS technologies [37].

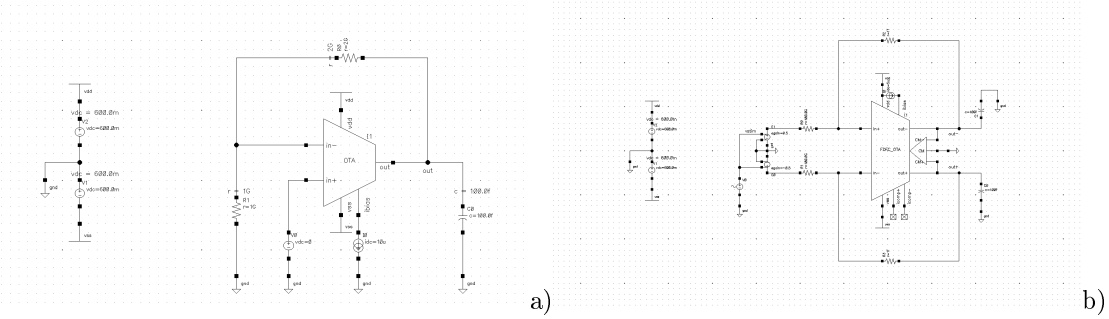


Figure 4.49: Output voltage range schematics of (a) simple OTA and (b) fully differential folded coscode OTA for 90nm and 65nm, bulk CMOS technologies [37].

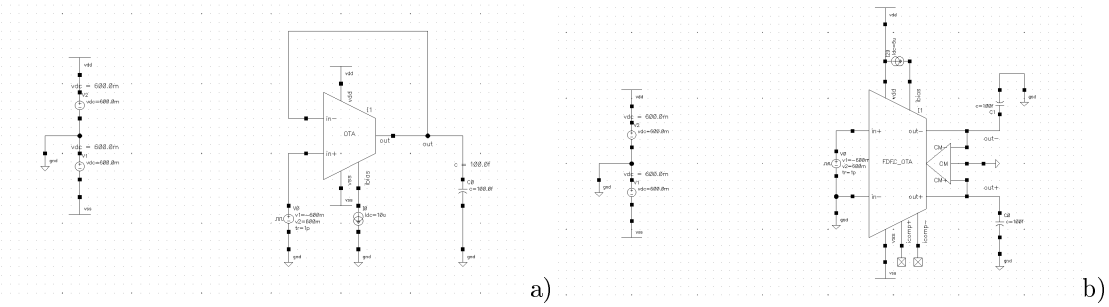


Figure 4.50: Transient analysis schematics of (a) simple OTA and (b) fully differential folded coscode OTA for 90nm and 65nm, bulk CMOS technologies [37].

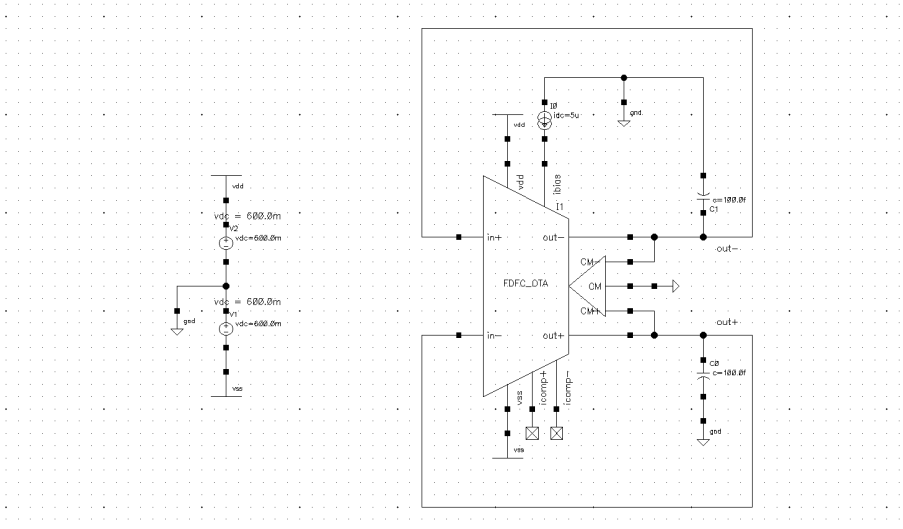


Figure 4.51: Noise analysis schematic of fully differential folded coscode OTA for 90nm and 65nm, bulk CMOS technologies [37].

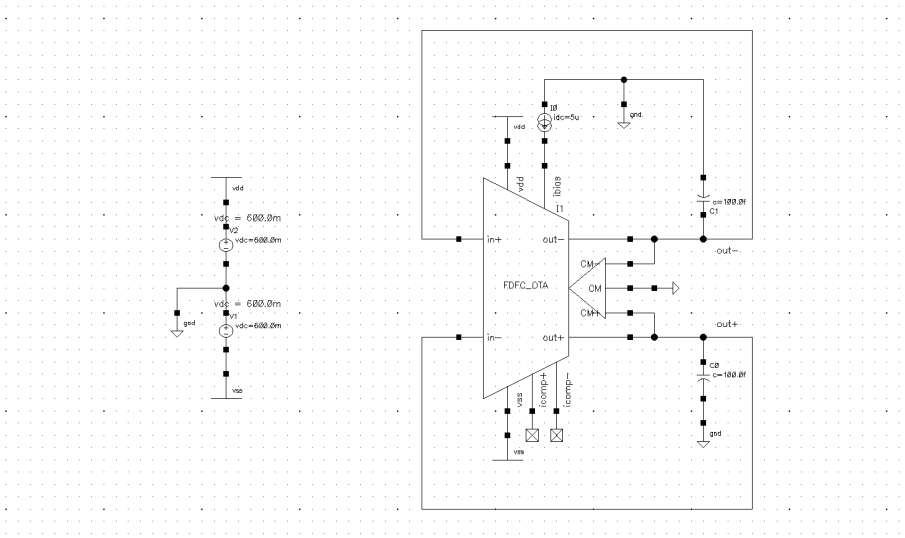


Figure 4.52: Input offset voltage schematic of fully differential folded coscode OTA for 90nm and 65nm, bulk CMOS technologies [37].

A Appendix

A.1 Matlab codes

The simple OTA was sized step-by-step, for our convenience we have used matlab code in order to calculate the basic equations in the proposed order as in the theoretical section above, for both 65nm, 90nm bulk cmos technologies.

```
%%%%% THESIS SIMPLE OTA SIZING-90nm-25dB %%%%%%


clc ;
clear all;
close all;


%%%% Physical constants

k=1.38*10^(-23);   % Boltzmann constant
q=1.602*10^(-19);  % Coulomb's constant
Tc=27;             % Temperature (C)
Tk=273.15+Tc;      % Temperature (K)

%%%% Normalization quantities

Ut=(k*Tk)/q;       % Thermal voltage

%%%% Specifications

sr=100*10^6;      % Slew Rate
cl=100*10^(-15);  % Load Capacitance
GBW=150*10^6;     % Gain Bandwith
AV0=25;           % Open-loop gain given >25db

%%%% Technology parameters

nn=1.24;           % Technology Parameter n (slope factor) for nmos
   transistor
np=1.22;           % Technology Parameter n (slope factor) for pmos
   transistor
Kpn=306*10^(-6);   % Normalized trasconductance Kpn for nmos
   transistor
Kpp=102.9*10^(-6); % Normalized trasconductance Kpp for pmos
   transistor
Uan=8.057*10^6;    % Early Voltage for nmos transistor
Uap=8.049*10^6;    % Early Voltage for pmos transistor
Lmin=90*10^(-9);   % Technology L minimum value

%%%% OTA sizing

% Bias (Pmos)

IF5=1;      % Moderate inversion
IF4=IF5;
L5=2*Lmin;  % Increase the speed (bigger Ft)
```

```
L6=L5;
IBias=sr*cl;
Io=IBias;
W5=(Io*L5)/(2*np*(Ut^2)*Kpp*IF5); % Solved for w5 the equation IF=
    IDsat/(2*n*ut^2*Kp*(W5/L5) as IF5 we assume 1--> WI and IDsat=Io=
    IBias
W6=W5;

% Differential pair (Pmos)

gm2overid2=4*((pi*GBW)/sr);  %% gm2/id2*2=2*pi*GBW/sr

% we create these 2 methods in order to take a very good aproximate
    value
% of IF2 in a range of values of IF2

% flag=0;
% IF2=0.001;
% gm2overid2=0;
% while flag~=1;
% gm2overid2=(1/(np*Ut))*(1/(0.5+sqrt(IF2+0.25)));
% if gm2overid2==18.84;
%   flag=1;
% end
% IF2=0.001+0.001;
% end
% IF2;

% IF2=0.0001:0.0001:1;
% gm2overid2=(1/(np*Ut))*(1/(0.5+sqrt(IF2+0.25)));
% plot(IF2,gm2overid2);
% IF2=0.913;
% gm2overid2=(1/(np*Ut))*(1/(0.5+sqrt(IF2+0.25)));

%
% IF2_TABLE=[0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 3 5 7 9 11 20 40 60
    80 100]
% for i=1:20
%     gm2overid2(i)=(1/(np*Ut))*(1/(0.5+sqrt(IF2_TABLE(i)+0.25)))
% end
% range_values=(0.1:0.1:100);
% IF2=interp1q(IF2_TABLE(9),gm2overid2(9),range_values)
% IF2

% The best approximation methot in order to find the IF2 is to use
    Linear
% interpolation

% IF2_TABLE=[0.0001 0.001 0.01 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1
    1.1 1.2 1.3 1.4 1.5 2 2.5 3 3.5 4 4.5 5 7 9 11 20 40 60 80 100 120
    140]
% for i=1:35
%     gm2overid2(i)=(1/(np*Ut))*(1/(0.5+sqrt(IF2_TABLE(i)+0.25)))
% end
```

```
%
%
% IF2=1.1
%
% for i=1.1:0.001:1.2
% gm2overid2_aprox=18.6027+(i-1.1)*((19.0758-18.6027)/(1.2-1.1))
% if gm2overid2_aprox==18.84
%     IF2
% end
% IF2=IF2+0.001
% end
% plot (IF2_TABLE,gm2overid2,'-o',IF2,gm2overid2_aprox);
% title ('gm2/id2 plot to IF2');
% xlabel ('IF2 [-]');
% ylabel ('gm2/id2 [1/V]');
% legend ('gm2/id2=(1/(np*Ut))*(1/(0.5+sqrt(IF2+0.25)))','location','
   southwest');
% set (gca,'XScale','log')
% hold on;
% grid on;


IF2=1.15;
gm2overid2=(1/(np*Ut))*(1/(0.5+sqrt(IF2+0.25)));
Id2=Io/2;
W2overL2=Id2/(IF2*2*np*(Ut^2)*Kpp); % We compute W2overL2 from this
   equation where we put as IDsat=I0/2 and IF2 with above value 0.931
AV=10^(AV0/20);     % To convert dB the open-loop gain parameter given
    >25db in specifications,approximate this in order to achieve the
   correct W2 & L2
% Ispec2=2*n*(Ut^2)*Kpp*W2overL2;   % It is computed by the expression
    IF2=Id2/Ispec
% Id2=IF2*Ispec2;   % It is computed by the expression IF2=Id2/Ispec
gm2=gm2overid2*Id2;
Rout2=AV/gm2;       % It is computed by AV0=gm2*Rout
gds2=2/Rout2;       % Given
L2=Id2/(gds2*Uap);  % It is computed by gds=IDsat/(2*Uap)
L2=L2*4;            % In order to achive gm in op's cadence
L1=L2;
W2=W2overL2*L2;
W1=W2;

% L=AV/(gm2overid2*Uap) % This computes the L od all the differential
   pair

% Active Load (nmos)

% The best approximation methot in order to find the IF4 is to use
   Linear
% interpolation

% IF4_TABLE=[0.0001 0.001 0.01 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1
   1.1 1.2 1.3 1.4 1.5 2 2.5 3 3.5 4 4.5 5 5.5 6 6.5 7 7.5 8 9 11 20
   40 60 80 100 120 140]
```

```
% for i=1:40
%     gm4overid4(i)=(1/(nn*Ut))*(1/(0.5+sqrt(IF4_TABLE(i)+0.25)))
% end
%
%
% IF4=7.5
%
% for i=7.5:0.001:8
% gm4overid4_aprox=9.2491+(i-7.5)*((9.4981-9.2491)/(8-7.5))
% if gm4overid4_aprox==9.42
%     IF4
% end
% IF4=IF4+0.001
% end
% plot (IF4_TABLE,gm4overid4,'-o',IF4,gm4overid4_aprox);
% title ('gm4/id4 plot to IF4');
% xlabel ('IF4 [-]');
% ylabel ('gm4/id4 [1/V]');
% legend ('gm4/id4=(1/(nn*Ut))*(1/(0.5+sqrt(IF4+0.25)))','location','
   southwest');
% set (gca,'XScale','log')
% hold on;
% grid on;

IF4=7.65;
Id4=Id2;
% gm4overid4=(1/(nn*Ut))*(1/(0.5+sqrt(IF4+0.25)));
gm4overid4=0.5*gm2overid2;  % In order to minimize the noise
   contribution
W4overL4=Id4/(IF4*2*nn*(Ut^2)*Kpn); % we compute W2overL2 from this
   equation where we put as IDsat=I0/2 and IF4 with above value 7.5
% Ispec4=2*n*(Ut^2)*Kpn*W4overL4;   % It is computed by the expression
    IF4=Id4/Ispec
% Id4=IF4*Ispec4; % It is computed by the expression IF4=Id4/Ispec
gm4=gm4overid4*Id4;
Rout4=AV/gm4; % It is computed by AV0=gm4*Rout
gds4=2/Rout4; % Given
L4=Id4/(gds4*Uan); % It is computed by gds4=IDsat/(2*Uan)
L4=L4*2; % In order to achive gm in op's cadence
L3=L4;
W4=W4overL4*L4;
W3=W4;


% We compute the area of each pair of transistors

A1_2=2*(L1*W1);
A3_4=2*(L4*W4);
A5_6=2*(L5*W5);


% We compute the total OTA Area

A=A1_2+A3_4+A5_6;
```

```
% % First optimization to reduce the total area
% We change the widths and the lengths of "big" devices (Pmos)
% W1_new=480*(10^(-9));
% W2_new=W1_new;
% W4_new=360*(10^(-9));
% W3_new=W4_new;
% W5_new=9.48*(10^(-6));
% W6_new=W5_new;
% L1_new=75*(10^(-9));
% L2_new=L1_new;
% L4_new=180*(10^(-9));
% L3_new=L4_new;
% L5_new=130*(10^(-9));
% L6_new=L5_new;
%
%
%
% % We re-compute the area of each pair of transistors
%
% A1_2_new=2*(L1_new*W1_new);
% A3_4_new=2*(L4_new*W4_new);
% A5_6_new=2*(L5_new*W5_new);
%
%
% % We re-compute the total OTA Area
%
% A_new=A1_2_new+A3_4_new+A5_6_new;
%

% Second optimization to increase the open loop gain & also to reduce
   the
% mismatch

% For the open-loop gain

W1_new_1=2*W1;
L1_new_1=2*L1;

W2_new_1=W1_new_1;
L2_new_1=L1_new_1;


W3_new_1=2*W3;
L3_new_1=2*L3;

W4_new_1=W3_new_1;
L4_new_1=L3_new_1;

% For the mismatch
W5_new_1=2*W5;
L5_new_1=2*L5;

W6_new_1=W5_new_1;
```

```
L6_new_1=L5_new_1;

% We re-compute the area of each pair of transistors

A1_2_new_1=2*(L1_new_1*W1_new_1);
A3_4_new_1=2*(L3_new_1*W3_new_1);
A5_6_new_1=2*(L5_new_1*W5_new_1);

% We re-compute the total OTA Area

A_new_1=A1_2_new_1+A3_4_new_1+A5_6_new_1;

%%%%% THESIS SIMPLE OTA SIZING-90nm-25dB %%%%%%


clc ;
clear all;
close all;


%%%% Physical constants

k=1.38*10^(-23);   % Boltzmann constant
q=1.602*10^(-19);  % Coulomb's constant
Tc=27;             % Temperature (C)
Tk=273.15+Tc;      % Temperature (K)

%%%% Normalization quantities

Ut=(k*Tk)/q;       % Thermal voltage

%%%% Specifications

sr=100*10^6;      % Slew Rate
cl=100*10^(-15);  % Load Capacitance
GBW=150*10^6;     % Gain Bandwith
AV0=25;           % Open-loop gain given >25db

%%%% Technology parameters

nn=1.24;           % Technology Parameter n (slope factor) for nmos
   transistor
np=1.22;           % Technology Parameter n (slope factor) for pmos
   transistor
Kpn=306*10^(-6);   % Normalized trasconductance Kpn for nmos
   transistor
Kpp=102.9*10^(-6); % Normalized trasconductance Kpp for pmos
   transistor
Uan=8.057*10^6;    % Early Voltage for nmos transistor
Uap=8.049*10^6;    % Early Voltage for pmos transistor
Lmin=90*10^(-9);   % Technology L minimum value

%%%% OTA sizing
```

```
% Bias (Pmos)

IF5=1;      % Moderate inversion
IF4=IF5;
L5=2*Lmin;  % Increase the speed (bigger Ft)
L6=L5;
IBias=sr*cl;
Io=IBias;
W5=(Io*L5)/(2*np*(Ut^2)*Kpp*IF5); % Solved for w5 the equation IF=
   IDsat/(2*n*ut^2*Kp*(W5/L5) as IF5 we assume 1--> WI and IDsat=Io=
   IBias
W6=W5;

% Differential pair (Pmos)

gm2overid2=4*((pi*GBW)/sr);  %% gm2/id2*2=2*pi*GBW/sr

% we create these 2 methods in order to take a very good aproximate
   value
% of IF2 in a range of values of IF2

% flag=0;
% IF2=0.001;
% gm2overid2=0;
% while flag~=1;
% gm2overid2=(1/(np*Ut))*(1/(0.5+sqrt(IF2+0.25)));
% if gm2overid2==18.84;
%   flag=1;
% end
% IF2=0.001+0.001;
% end
% IF2;

% IF2=0.0001:0.0001:1;
% gm2overid2=(1/(np*Ut))*(1/(0.5+sqrt(IF2+0.25)));
% plot(IF2,gm2overid2);
% IF2=0.913;
% gm2overid2=(1/(np*Ut))*(1/(0.5+sqrt(IF2+0.25)));

%
% IF2_TABLE=[0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 3 5 7 9 11 20 40 60
    80 100]
% for i=1:20
%     gm2overid2(i)=(1/(np*Ut))*(1/(0.5+sqrt(IF2_TABLE(i)+0.25)))
% end
% range_values=(0.1:0.1:100);
% IF2=interp1q(IF2_TABLE(9),gm2overid2(9),range_values)
% IF2

% The best approximation methot in order to find the IF2 is to use
   Linear
% interpolation

% IF2_TABLE=[0.0001 0.001 0.01 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1
```

```
   1.1 1.2 1.3 1.4 1.5 2 2.5 3 3.5 4 4.5 5 7 9 11 20 40 60 80 100 120
   140]
% for i=1:35
%     gm2overid2(i)=(1/(np*Ut))*(1/(0.5+sqrt(IF2_TABLE(i)+0.25)))
% end
%
%
% IF2=1.1
%
% for i=1.1:0.001:1.2
% gm2overid2_aprox=18.6027+(i-1.1)*((19.0758-18.6027)/(1.2-1.1))
% if gm2overid2_aprox==18.84
%     IF2
% end
% IF2=IF2+0.001
% end
% plot (IF2_TABLE,gm2overid2,'-o',IF2,gm2overid2_aprox);
% title ('gm2/id2 plot to IF2');
% xlabel ('IF2 [-]');
% ylabel ('gm2/id2 [1/V]');
% legend ('gm2/id2=(1/(np*Ut))*(1/(0.5+sqrt(IF2+0.25)))','location','
   southwest');
% set (gca,'XScale','log')
% hold on;
% grid on;


IF2=1.15;
gm2overid2=(1/(np*Ut))*(1/(0.5+sqrt(IF2+0.25)));
Id2=Io/2;
W2overL2=Id2/(IF2*2*np*(Ut^2)*Kpp); % We compute W2overL2 from this
   equation where we put as IDsat=I0/2 and IF2 with above value 0.931
AV=10^(AV0/20);     % To convert dB the open-loop gain parameter given
    >25db in specifications,approximate this in order to achieve the
   correct W2 & L2
% Ispec2=2*n*(Ut^2)*Kpp*W2overL2;   % It is computed by the expression
    IF2=Id2/Ispec
% Id2=IF2*Ispec2;   % It is computed by the expression IF2=Id2/Ispec
gm2=gm2overid2*Id2;
Rout2=AV/gm2;       % It is computed by AV0=gm2*Rout
gds2=2/Rout2;       % Given
L2=Id2/(gds2*Uap);  % It is computed by gds=IDsat/(2*Uap)
L2=L2*4;            % In order to achive gm in op's cadence
L1=L2;
W2=W2overL2*L2;
W1=W2;

% L=AV/(gm2overid2*Uap) % This computes the L od all the differential
   pair

% Active Load (nmos)

% The best approximation methot in order to find the IF4 is to use
   Linear
```

```
% interpolation

% IF4_TABLE=[0.0001 0.001 0.01 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1
   1.1 1.2 1.3 1.4 1.5 2 2.5 3 3.5 4 4.5 5 5.5 6 6.5 7 7.5 8 9 11 20
   40 60 80 100 120 140]
% for i=1:40
%     gm4overid4(i)=(1/(nn*Ut))*(1/(0.5+sqrt(IF4_TABLE(i)+0.25)))
% end
%
%
% IF4=7.5
%
% for i=7.5:0.001:8
% gm4overid4_aprox=9.2491+(i-7.5)*((9.4981-9.2491)/(8-7.5))
% if gm4overid4_aprox==9.42
%     IF4
% end
% IF4=IF4+0.001
% end
% plot (IF4_TABLE,gm4overid4,'-o',IF4,gm4overid4_aprox);
% title ('gm4/id4 plot to IF4');
% xlabel ('IF4 [-]');
% ylabel ('gm4/id4 [1/V]');
% legend ('gm4/id4=(1/(nn*Ut))*(1/(0.5+sqrt(IF4+0.25)))','location','
   southwest');
% set (gca,'XScale','log')
% hold on;
% grid on;

IF4=7.65;
Id4=Id2;
% gm4overid4=(1/(nn*Ut))*(1/(0.5+sqrt(IF4+0.25)));
gm4overid4=0.5*gm2overid2;  % In order to minimize the noise
   contribution
W4overL4=Id4/(IF4*2*nn*(Ut^2)*Kpn); % we compute W2overL2 from this
   equation where we put as IDsat=I0/2 and IF4 with above value 7.5
% Ispec4=2*n*(Ut^2)*Kpn*W4overL4;   % It is computed by the expression
    IF4=Id4/Ispec
% Id4=IF4*Ispec4; % It is computed by the expression IF4=Id4/Ispec
gm4=gm4overid4*Id4;
Rout4=AV/gm4; % It is computed by AV0=gm4*Rout
gds4=2/Rout4; % Given
L4=Id4/(gds4*Uan); % It is computed by gds4=IDsat/(2*Uan)
L4=L4*2; % In order to achive gm in op's cadence
L3=L4;
W4=W4overL4*L4;
W3=W4;


% We compute the area of each pair of transistors

A1_2=2*(L1*W1);
A3_4=2*(L4*W4);
A5_6=2*(L5*W5);
```

```
% We compute the total OTA Area

A=A1_2+A3_4+A5_6;

% % First optimization to reduce the total area
% We change the widths and the lengths of "big" devices (Pmos)
% W1_new=480*(10^(-9));
% W2_new=W1_new;
% W4_new=360*(10^(-9));
% W3_new=W4_new;
% W5_new=9.48*(10^(-6));
% W6_new=W5_new;
% L1_new=75*(10^(-9));
% L2_new=L1_new;
% L4_new=180*(10^(-9));
% L3_new=L4_new;
% L5_new=130*(10^(-9));
% L6_new=L5_new;
%
%
%
% % We re-compute the area of each pair of transistors
%
% A1_2_new=2*(L1_new*W1_new);
% A3_4_new=2*(L4_new*W4_new);
% A5_6_new=2*(L5_new*W5_new);
%
%
% % We re-compute the total OTA Area
%
% A_new=A1_2_new+A3_4_new+A5_6_new;
%

% Second optimization to increase the open loop gain & also to reduce
   the
% mismatch

% For the open-loop gain

W1_new_1=2*W1;
L1_new_1=2*L1;

W2_new_1=W1_new_1;
L2_new_1=L1_new_1;


W3_new_1=2*W3;
L3_new_1=2*L3;

W4_new_1=W3_new_1;
L4_new_1=L3_new_1;
```

```
% For the mismatch
W5_new_1=2*W5;
L5_new_1=2*L5;

W6_new_1=W5_new_1;
L6_new_1=L5_new_1;

% We re-compute the area of each pair of transistors

A1_2_new_1=2*(L1_new_1*W1_new_1);
A3_4_new_1=2*(L3_new_1*W3_new_1);
A5_6_new_1=2*(L5_new_1*W5_new_1);

% We re-compute the total OTA Area

A_new_1=A1_2_new_1+A3_4_new_1+A5_6_new_1;
```

Here there are demonstrated the Matlab Figures of $\frac{g_m}{I_d}$ vs. I_C used in order to compute $I_{C,2}$and $I_{C,4}$ in simple OTA in both 90nm and 65nm PDKs,

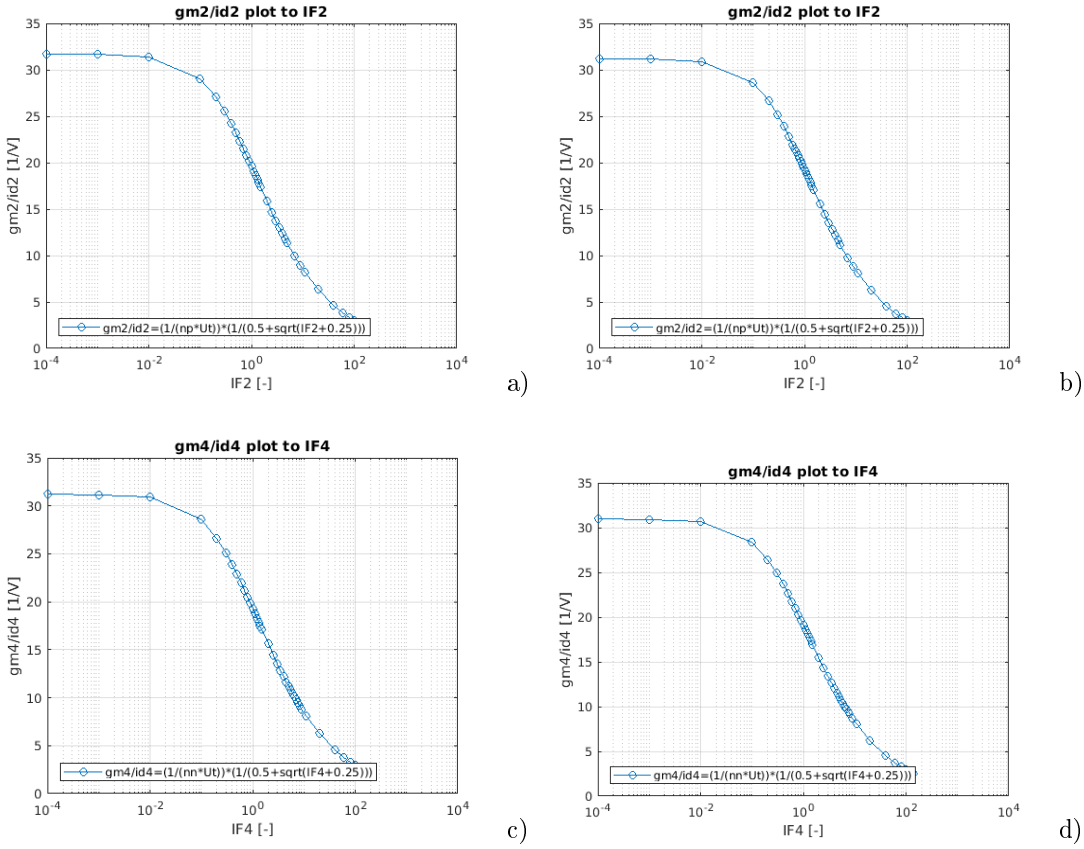


Figure A.1: Simulated transconductance-to-current-ratio $\frac{g_m}{I_D}$ vs. inversion coefficient I_C used to compute $I_{C,2}$ and $I_{C,4}$ for (a), (c) 90nm and (b), (d) 65nm, bulk CMOS process.

In the same way, we have used the following matlab codes in order to size the fully differential folded cascode (FDFC) OTA also,

```
%%%% THESIS FULLY DIFFERENTIAL FOLDED CASCODE OTA SIZING-90nm-50dB
    %%%%


clc ;
clear all;
close all;

%%%% Physical constants

k=1.38*10^(-23);
q=1.602*10^(-19);
Tc=27;
Tk=273.15+Tc;

%%%% Normalization quantities

Ut=(k*Tk)/q;

%%%% Specifications of the circuit

GBW=150*(10^6);     % Gain Bandwith
sr=100*(10^6);      % Slew Rate
cl=100*(10^(-15)); % Load Capacitance
nn=1.24;            % Technology Parameter nn (nmos transistors)
np=1.22;            % Technology Parameter np (pmos transistors)
Kpp=102.9*10^(-6); % Normalized trasconductance Kpp for pmos
    transistor
Kpn=306*10^(-6);    % Normalized trasconductance Kpn for nmos
    transistor
Uap=8.049*10^6;     % Early Voltage for pmos transistor
Uan=8.057*10^6;     % Early Voltage for nmos transistor

%%%% Sizing of OTA

%%%% Bias current-Differential pair

% Calculation of currents I0 and I1 and also we determine the
    transconductance,the inversion factor,and the W1/L1 ratio of the
    differential pair

% Calculate the Bias currents I0 and I1 in order to achieve the
    specified slew rate

I0=sr*cl;
I1=I0/2;
gm1=2*pi*cl*GBW;     % We calculate the transconductance gm1
Id1=I0/2;
gm1overid1=gm1/Id1; % We can calculate the gm1 over id1 value so we
    can find with linear interpolation method the IF1 value

% The best approximation method in order to find the IF1 is to use
    Linear
% interpolation
```

```
%  IF1_TABLE=[0.0001 0.001 0.01 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9
   0.95 1 1.1 1.2 1.3 1.4 1.5 2 3 5 7 9 11 20 40 60 80 100]
%  for i=1:30
%     gm1overid1(i)=(1/(np*Ut))*(1/(0.5+sqrt(IF1_TABLE(i)+0.25)))
%  end
%
%  IF1=1.1
%
%  for i=1.1:0.001:1.2
%  gm1overid1_aprox=18.6027+(i-1.1)*((19.0758-18.6027)/(1.2-1.1))
%  if gm1overid1_aprox==18.8496
%      IF1
%  end
%  IF1=IF1+0.001
%  end
% plot (IF1_TABLE,gm1overid1,'-o',IF1,gm1overid1_aprox);
% title ('gm1/id1 plot to IF1');
% xlabel ('IF1 (-)');
% ylabel ('gm1/id1 (1/V)');
% legend ('gm1/id1=(1/(np*Ut))*(1/(0.5+sqrt(IF1+0.25)))','location','
   southwest');
% set (gca,'XScale','log')
% hold on;
% grid on;


IF1=1.15;
% gm1overid1=(1/(np*Ut))*(1/(0.5+sqrt(IF1+0.25))) % best approximation
    of IF1 is 1.15

W1overL1=Id1/(IF1*2*np*(Ut^2)*Kpp); % We compute the W1/L1 ratio

%%%% Folded cascoded current mirrors

% We calculate the W/L of the 8 transistor composing the folded
   cascode stage
% We choose moderate inversion for transistors m5-m6,m7-m8,m9-m10 to
   keep the saturation voltage small and also to have small area
   consumption
% We choose strong inversion for transistors m3-m4 to reduce noise
   contribution

IF9=1;
IF7=1;
IF5=1;
IF10=IF9;
IF8=IF7;
IF6=IF5;
Id9=I1;
Id7=I1;
Id5=I1;

% Same current mirror
```

```
Id10=Id9;
Id8=Id7;
Id6=Id5;

W9overL9=Id9/(IF9*2*np*(Ut^2)*Kpp); % Pmos current mirror
W7overL7=Id7/(IF7*2*np*(Ut^2)*Kpp); % Pmos current mirror
W5overL5=Id5/(IF5*2*nn*(Ut^2)*Kpn); % Nmos current mirror

% Same W/L ratio in the same current mirrors

W10overL10=W9overL9;
W8overL8=W7overL7;
W6overL6=W5overL5;

% We choose strong inversion for these transistors

IF3=10;
IF4=IF3;
I2=(I0/2)+I1;
Id3=I2;

% Same current mirror

Id4=Id3;
W3overL3=Id3/(IF3*2*nn*(Ut^2)*Kpn); % Nmos current mirror

% same W/L ratio in the same current mirrors
W4overL4=W3overL3;

% Here we calculate the output resistance

A0=50;          % Open-loop gain>50 dB
AV=10^(A0/20);
Rout=AV/gm1;

% Negleting the conductance of the differential pair we compute the
   gm5=gm7

gm5=(1/(np*Ut))*(Id5/(0.5+sqrt(IF5+0.25)));
gm7=gm5;

% As we can choose gds5=gds7,gds3=gds9,Id3=2*Id9,Id5=Id7,L7=L9,L5=2*L3
    and Uan almost equal to Uap we can compute the following

Rup=2*Rout;
Rdown=Rup;
L7multL9=(Rup*Id7*Id9)/(gm7*(Uap^2));   % We solve the equation of Rup
L3multL5=(Rdown*Id3*Id5)/(gm5*(Uan^2)); % We solve the equation of
   Rdown

L7=sqrt(L7multL9);
L9=L7;;
L3=sqrt(2*L3multL5); % We know that L3=2*L9 and L5=L7
```

```
L5=L3/2;

% They are the same transistors

L10=L9;
L8=L7;
L6=L5;
L4=L3;


% We can calculate the width of all cascode transistors

W9=(Id9*L9)/(2*np*(Ut^2)*Kpp*IF9); % solved for W9 the equation IF=
    IDsat/(2*np*ut^2*Kpp*(W9/L9)
W7=(Id7*L7)/(2*np*(Ut^2)*Kpp*IF7); % solved for W7 the equation IF=
    IDsat/(2*np*ut^2*Kpp*(W7/L7)
W5=(Id5*L5)/(2*nn*(Ut^2)*Kpn*IF5); % solved for W5 the equation IF=
    IDsat/(2*nn*ut^2*Kpn*(W5/L5)
W3=(Id3*L3)/(2*nn*(Ut^2)*Kpn*IF3); % solved for W3 the equation IF=
    IDsat/(2*nn*ut^2*Kpp*(W3/L3)

% They are the same transistors

W10=W9;
W8=W7;
W6=W5;
W4=W3;

%%%% Find the length and the width of the differential pair and
    current source

% We choose a small L1=200nm

L1=200*10^(-9);
W1=L1*W1overL1;
W2=W1;
L2=L1;

% To determine LB1 and WB1 we know that IF9=IFB1 and I1=I0/2 and if we
     do
% the maths we end up to this

WB1=2*W9;
LB1=L9;

%%%% Design verification & Performance simulation (sizing of
    transistors m20,m21)

IF20=1; % we choose moderate inversion as in the other pmos
    transistors
IF21=IF20;
L20=LB1; % We choose a L~=162.5nm as in the other bias Pmos transistor
L21=L20;
Id20=I1; % Id20=I1=5*10^(-6)
```

```
Id21=Id20;
W20=(Id20*L20)/(2*np*(Ut^2)*Kpp*IF20);
W21=W20;

% Sizing of the transistor m11 of the cmfb

L11=L3;
IF11=IF3;
Id11=I1; % Id11=I1=5*10^(-6)
W11=(Id11*L11)/(2*nn*(Ut^2)*Kpn*IF11);

%%%% We compute the area of whole circuit

% We compute the area of each mirror

A3_4=2*(L3*W3);
A5_6=2*(L5*W5);
A7_8=2*(L7*W7);
A9_10=2*(L9*W9);

% We compute the total cascode area

A=A3_4+A5_6+A7_8+A9_10;

% We compute the area of the bias transistor

A_B1=(LB1*WB1);

% We compute the area of the input differential pair

A1_2=2*(L1*W1);

% We compute the total FC_OTA area

A_Total=A_B1+A1_2+A3_4+A5_6+A7_8+A9_10;

% Optimazation to achieve Av=50 dB
% In order to optimize we double the size of transistors m3,m4,m11,m1,
   m2

L1_new=2*L1;
L2_new=2*L2;
W1_new=2*W1;
W2_new=2*W2;
L3_new=2*L3;
L4_new=2*L4;
W3_new=2*W3;
W4_new=2*W4;
L11_new=2*L11;
W11_new=2*W11;

% We re-compute the area of whole circuit
AB1_new=(LB1*WB1);
A1_2_new=2*(L1_new*W1_new);
```

```
A3_4_new=2*(L3_new*W3_new);
A5_6_new=2*(L5*W5);
A7_8_new=2*(L7*W7);
A9_10_new=2*(L9*W9);

A_new=A3_4_new+A5_6_new+A7_8_new+A9_10_new+A1_2_new+AB1_new;

%%%% THESIS FULLY DIFFERENTIAL FOLDED CASCODE OTA SIZING-65nm-50dB
    %%%%


clc ;
clear all;
close all;

%%%% Physical constants

k=1.38*10^(-23);
q=1.602*10^(-19);
Tc=27;
Tk=273.15+Tc;

%%%% Normalization quantities

Ut=(k*Tk)/q;

%%%% Specifications of the circuit

GBW=150*(10^6);     % Gain Bandwith
sr=100*(10^6);      % Slew Rate
cl=100*(10^(-15)); % Load Capacitance
nn=1.25;            % Technology Parameter nn (nmos transistors)
np=1.24;            % Technology Parameter np (pmos transistors)
Kpp=102*10^(-6);    % Normalized trasconductance Kpp for pmos
    transistor
Kpn=252*10^(-6);    % Normalized trasconductance Kpn for nmos
    transistor
Uap=12.53*10^6;     % Early Voltage for pmos transistor
Uan=10.37*10^6;     % Early Voltage for nmos transistor

%%%% Sizing of OTA

%%%% Bias current-Differential pair

% Calculation of currents I0 and I1 and also we determine the
    transconductance,the inversion factor,and the W1/L1 ratio of the
    differential pair

% Calculate the Bias currents I0 and I1 in order to achieve the
    specified slew rate

I0=sr*cl;
I1=I0/2;
gm1=2*pi*cl*GBW;     % We calculate the transconductance gm1
```

```
Id1=I0/2;
gm1overid1=gm1/Id1; % We can calculate the gm1 over id1 value so we
    can find with linear interpolation method the IF1 value

% The best approximation method in order to find the IF1 is to use
    Linear
% interpolation

% IF1_TABLE=[0.0001 0.001 0.01 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.85
    0.9 0.95 1.05 1.1 1.15 1.2 1.25 1.3 1.35 1.4 1.45 1.5 2 3 5 7 9 11
    20 40 60 80 100]
% for i=1:35
%     gm1overid1(i)=(1/(np*Ut))*(1/(0.5+sqrt(IF1_TABLE(i)+0.25)))
% end
%
% IF1=1.05
%
% for i=1.05:0.001:1.1
%     gm1overid1_aprox=18.7681+(i-1.05)*((19.0166-18.7681)/(1.1-1.05))
%     if gm1overid1_aprox==18.8496
%         IF1
%     end
%     IF1=IF1+0.001
% end
% plot (IF1_TABLE,gm1overid1,'-o',IF1,gm1overid1_aprox);
% title ('gm1/id1 plot to IF1');
% xlabel ('IF1 (-)');
% ylabel ('gm1/id1 (1/V)');
% legend ('gm1/id1=(1/(np*Ut))*(1/(0.5+sqrt(IF1+0.25)))','location','
    southwest');
% set (gca,'XScale','log')
% hold on;
% grid on;


IF1=1.08;
% gm1overid1=(1/(np*Ut))*(1/(0.5+sqrt(IF1+0.25))) % best approximation
     of IF1 is 1.08

W1overL1=Id1/(IF1*2*np*(Ut^2)*Kpp); % we compute the W1/L1 ratio

%%%% Folded cascoded current mirrors

% We calculate the W/L of the 8 transistor composing the folded
    cascode stage
% We choose moderate inversion for transistors m5-m6,m7-m8,m9-m10 to
    keep the saturation voltage small and also to have small area
    consumption
% We choose strong inversion for transistors m3-m4 to reduce noise
    contribution

IF9=1;
IF7=1;
IF5=1;
```

```
IF10=IF9;
IF8=IF7;
IF6=IF5;
Id9=I1;
Id7=I1;
Id5=I1;

% Same current mirror

Id10=Id9;
Id8=Id7;
Id6=Id5;

W9overL9=Id9/(IF9*2*np*(Ut^2)*Kpp); % Pmos current mirror
W7overL7=Id7/(IF7*2*np*(Ut^2)*Kpp); % Pmos current mirror
W5overL5=Id5/(IF5*2*nn*(Ut^2)*Kpn); % Nmos current mirror

% Same W/L ratio in the same current mirrors

W10overL10=W9overL9;
W8overL8=W7overL7;
W6overL6=W5overL5;

% We choose strong inversion for these transistors

IF3=10;
IF4=IF3;
I2=(I0/2)+I1;
Id3=I2;

% Same current mirror

Id4=Id3;
W3overL3=Id3/(IF3*2*nn*(Ut^2)*Kpn); % Nmos current mirror

% same W/L ratio in the same current mirrors
W4overL4=W3overL3;

% Here we calculate the output resistance

A0=50;          % Open-loop gain >50 dB
AV=10^(A0/20);
Rout=AV/gm1;

% Negleting the conductance of the differential pair we compute the
   gm5=gm7

gm5=(1/(np*Ut))*(Id5/(0.5+sqrt(IF5+0.25)));
gm7=gm5;

% As we can choose gds5=gds7,gds3=gds9,Id3=2*Id9,Id5=Id7,L7=L9,L5=2*L3
    and Uan almost equal to Uap we can compute the following

Rup=2*Rout;
```

```
Rdown=Rup;
L7multL9=(Rup*Id7*Id9)/(gm7*(Uap^2));   % we solve the equation of Rup
L3multL5=(Rdown*Id3*Id5)/(gm5*(Uan^2)); % we solve the equation of
    Rdown

L7=sqrt(L7multL9);
L9=L7;
L3=sqrt(2*L3multL5); % we know that L3=2.4*L9 and L5=1.2*L7 so, L3=2*
    L5
L5=L3/2;

% They are the same transistors

L10=L9;
L8=L7;
L6=L5;
L4=L3;


% We can calculate the width of all cascode transistors

W9=(Id9*L9)/(2*np*(Ut^2)*Kpp*IF9); % solved for W9 the equation IF=
    IDsat/(2*np*ut^2*Kpp*(W9/L9)
W7=(Id7*L7)/(2*np*(Ut^2)*Kpp*IF7); % solved for W7 the equation IF=
    IDsat/(2*np*ut^2*Kpp*(W7/L7)
W5=(Id5*L5)/(2*nn*(Ut^2)*Kpn*IF5); % solved for W5 the equation IF=
    IDsat/(2*nn*ut^2*Kpn*(W5/L5)
W3=(Id3*L3)/(2*nn*(Ut^2)*Kpn*IF3); % solved for W3 the equation IF=
    IDsat/(2*nn*ut^2*Kpp*(W3/L3)

% They are the same transistors

W10=W9;
W8=W7;
W6=W5;
W4=W3;

%%%% Find the length and the width of the differential pair and
    current source

% We choose a small L1=150nm

L1=150*10^(-9);
W1=L1*W1overL1;
W2=W1;
L2=L1;

% To determine LB1 and WB1 we know that IF9=IFB1 and I1=I0/2 and if we
    do
% the maths we end up to this

WB1=2*W9;
LB1=L9;
```

```
%%%% Design verification & Performance simulation (sizing of
   transistors m20,m21)

IF20=1; % we choose moderate inversion as in the other pmos
   transistors
IF21=IF20;
L20=LB1; % We choose a L~=162.5nm as in the other bias Pmos transistor
L21=L20;
Id20=I1; % Id20=I1=5*10^(-6)
Id21=Id20;
W20=(Id20*L20)/(2*np*(Ut^2)*Kpp*IF20);
W21=W20;

% Sizing of the transistor m11 of the cmfb

L11=L3;
IF11=IF3;
Id11=I1; % Id11=I1=5*10^(-6)
W11=(Id11*L11)/(2*nn*(Ut^2)*Kpn*IF11);

%%%% We compute the area of whole circuit

% We compute the area of each mirror

A3_4=2*(L3*W3);
A5_6=2*(L5*W5);
A7_8=2*(L7*W7);
A9_10=2*(L9*W9);

% We compute the total cascode area

A=A3_4+A5_6+A7_8+A9_10;

% We compute the area of the bias transistor

A_B1=(LB1*WB1);

% We compute the area of the input differential pair

A1_2=2*(L1*W1);

% We compute the total FC_OTA area

A_Total=A_B1+A1_2+A3_4+A5_6+A7_8+A9_10;


% Optimazation to achieve Av=50 dB
% In order to optimize we double the size of transistors m3,m4,m11,m1,
   m2

L1_new=2*L1;
L2_new=2*L2;
W1_new=2*W1;
W2_new=2*W2;
```

```
L3_new=2*L3;
L4_new=2*L4;
W3_new=2*W3;
W4_new=2*W4;
L11_new=2*L11;
W11_new=2*W11;

% We re-compute the area of whole circuit

AB1_new=(LB1*WB1);
A1_2_new=2*(L1_new*W1_new);
A3_4_new=2*(L3_new*W3_new);
A5_6_new=2*(L5*W5);
A7_8_new=2*(L7*W7);
A9_10_new=2*(L9*W9);

A_new=A3_4_new+A5_6_new+A7_8_new+A9_10_new+A1_2_new+AB1_new;
```

Here there are demonstrated the Matlab Figures of $\frac{g_m}{I_d}$ vs. I_C used in order to compute $I_{C,1}$ in FDFC OTA in both 90nm and 65nm PDKs,

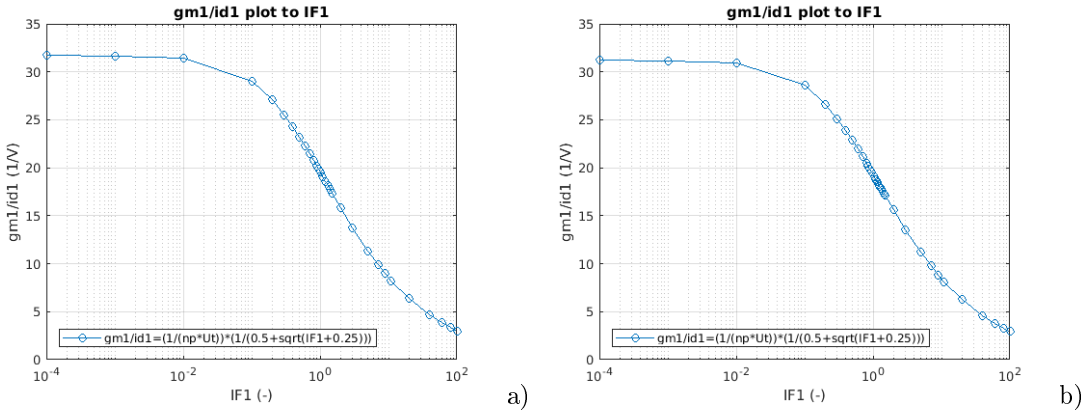


Figure A.2: Simulated transconductance-to-current-ratio $\frac{g_m}{I_D}$ vs. inversion coefficient I_C used to compute $I_{C,1}$ for (a) 90nm and (b) 65nm, bulk CMOS process.

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