Characterization and Compact Modeling of Low Frequency Noise and Ionizing Radiation Effects in Bulk Silicon MOSFETs

MSc Diploma Thesis

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Abstract

This work is divided in two main parts, both representing challenges in two distinct fields of semiconductor applications, the field of high-energy physics experiments, as a hostile operating environment for deep sub-micron MOSFETs and the field of high-precision, low-noise analog design with its requirements for detailed and accurate MOSFET noise models.

In the first part, analysis is presented on MOS devices irradiated to ultrahigh radiation doses (500Mrad), as part of the viability study conducted at CERN in cooperation with TUC for the upcoming LHC upgrade due in 2025-2027. Our part was to analyze, characterize and model the damage inflicted on a specific commercially available 65nm bulk CMOS technology, in order to allow designers at CERN to properly use it for the predicted ten year lifespan of the experiment. To this end, we have presented in this work selected operational parameters of interest to designers, which were extracted for both MOS polarities (n- and p-type), multiple device types (low, standard and high V_{TH}), at three different temperatures (-30°C, 0°C and 25°C), at four different irradiation levels (pre irradiation, 100, 200 and 500Mrad). Multiple device geometries were studied and are presented. A short analysis closes this chapter, correlating our findings with the published literature.

The second part deals with measurement and analysis of the noise response of a commercially available 110nm bulk CMOS technology. The system and methodology for on-wafer noise measurements is presented along with our efforts in extracting and analyzing usable data from our measurements. The EKV3 parameter extraction approach using the two distinct incorporated noise models is also described. Our resulting measurements are presented for the three different MOS polarities provided for this task (n-, p-type and intrinsic/native). Output as well as input referred noise spectra are presented, fitted with an analytical flicker noise model. Afterwards a short discussion of the results follows.

Περίληψη

Αυτή η εργασία χωρίζεται σε δύο βασικά τμήματα, που και τα δύο αντιπροσωπεύουν προκλήσεις σε δύο διαφορετικά πεδία εφαρμογών των ημιαγωγών, το πεδίο πειραμάτων φυσικής υψηλών ενεργειών, ως ένα πολύ εχθρικό περιβάλλον λειτουργίας για τρανζίστορ $MOSFET$ υπο-μικρομετρικών διαστάσεων και το πεδίο της αναλογικής σχεδίασης υψηλής ακριβείας και χαμηλού θορύβου με τις απαιτήσεις του για λεπτομερή και ακριβή μοντέλα θορύβου για τρανζίστορ $MOSFET$.

Στο πρώτο τμήμα παρουσιάζεται ανάλυση πάνω σε διατάξεις MOS που ακτινοβολήθηκαν σε υπερυψηλές δόσεις ακτινοβολίας ($500Mrad$), ως μέρος της μελέτης καταλληλότητας που διεξήχθη στο $CERN$ σε συνεργασία με το Πολυτεχνείο της Κρήτης για την επερχόμενη αναβάθμιση του LHC κατά τα έτη 2025-2027. Δική μας εργασία ήταν το να αναλύσουμε, χαρακτηρίσουμε και μοντελοποιήσουμε τη ζημία που επέρχεται σε μια συγκεκριμένη εμπορικά διαθέσιμη τεχνολογία $65nm\ bulk\ CMOS$, ώστε να επιτραπεί στους σχεδιαστές στο $CERN$ να την αξιοποιήσουν κατάλληλα για όλη τη δεκαετή προβλεπόμενη διάρκεια του πειράματος. Προς το σκοπό αυτό παρουσιάσαμε σε αυτή την εργασία συγκεκριμένες λειτουργικές παραμέτρους που ενδιαφέρουν τους σχεδιαστές, οι οποίες εξήχθησαν για τις δύο πολικότητες MOS (τύπου $n-$ και $p-$), τους διαφορετικούς τύπους διατάξεων (χαμηλής, κανονικής και υψηλής τάσης κατωφλίου), σε τρεις διαφορετικές θερμοκρασίες ($-30°C$, $0°C$ και $25°C$), σε τέσσερα διαφορετικά επίπεδα δόσης (προ ακτινοβόλησης, 100, 200 και $500Mrad$). Πολλές διαφορετικές γεωμετρίες μελετήθηκαν και παρουσιάζονται. Μία σύντομη ανάλυση κλείνει αυτό το κεφάλαιο, συσχετίζοντας τα ευρήματά μας με τη δημοσιευμένη βιβλιογραφία.

Το δεύτερο τμήμα ασχολείται με την μέτρηση και ανάλυση της απόκρισης θορύβου μιας εμπορικά διαθέσιμης τεχνολογίας $110nm\ bulk\ CMOS$. Παρουσιάζεται το σύστημα και η μεθοδολογία για την διεξαγωγή μετρήσεων θορύβου πάνω σε δισκία πυριτίου ($wafers$), μαζί με τη διαδικασία που ακολουθήσαμε για να εξαγάγουμε αξιοποιήσιμα δεδομένα από τις μετρήσεις μας καθώς και να τα αναλύσουμε. Περιγράφεται επίσης η προσέγγιση του ζητήματος εξαγωγής παραμέτρων μοντέλου $EKV3$, με τα δύο διαφορετικά ενσωματωμένα μοντέλα θορύβου. Οι μετρήσεις θορύβου παρουσιάζονται για τις τρεις πολικότητες που είχαμε διαθέσιμες για αυτόν το σκοπό (τύπου $n-$, $p-$ και ενδογενή). Παρουσιάζονται φάσματα θορύβου αναφερόμενου στην έξοδο καθώς και στην είσοδο, στα οποία έχει εφαρμοστεί ένα αναλυτικό μοντέλο θορύβου χαμηλής συχνότητας ($flicker$). Έπειτα ακολουθεί μια σύντομη συζήτηση των αποτελεσμάτων.

Contents

1 Introduction

Deeply scaled MOSFET transistors are the backbone of our modern technological life. As devices have progressively shrunk in the past decades, peculiarities in their behaviour have been magnified and multiplied, necessitating ever more detailed and involved understanding of their functions in order to permit their utilisation and ensure their long-lasting service. Integrated circuit designers build on foundations of sturdy and well-behaved models, thus the industry has to be able to provide them with these refined tools.

At CERN the hardware upgrade of the Large Hadron Collider experiment to the High Luminosity LHC has been in planning stages for the past decade. After the upgrade, detectors closest to the collision sites are expected to accumulate unprecedented doses of ionizing radiation over the projected decade-long lifetime of the experiment, due to the ten-fold increase over the initial design's luminosity. Aerospace and nuclear power engineering has up to now considered devices utilizing specialized processes and tested up to 1Mrad as "radiation hardened". In the HL-LHC the expected doses will reach Grad levels, so circuits will have to be fit for purpose and designed ab initio for reliability, with these extreme operating conditions in mind. To this end, radiation hardness by design is the paradigm for the innermost circuits and more modern technologies were essential for the application, compared to the 250nm and 130nm used before. A commercially available 65nm technology has been under investigation for its suitability and the electronics laboratory at TUC undertook the task of electrically characterizing and extracting model parameters for multiple transistor types, which were rapidly irradiated at CERN to doses of up to 500Mrad, at varying temperatures. In this work, part of this characterization endeavour is presented.

Noise can be a limiting factor on the performance of electronic integrated circuits. It can make the signal harder to detect, or outright drown it out. As transistor sizes scale down, low frequency noise becomes more apparent, as it scales inversely proportional to the gate area. Encountered in digital and analog electronics alike, it is a factor to consider during design of a wide range of circuits, from amplifiers to SRAMs. And as frequency of operation increases and smaller transistors are preferred, LFN can be upconverted and encountered as phase noise in RF circuits as well. Since the phenomenon is related to trapping along the semiconductor-oxide interface, optimization and tight control of the fabrication process is essential to minimize its occurrence. The electronics laboratory at TUC was tasked with measuring, characterizing and extracting EKV3 model parameters for the noise response of a commercially available 110nm technology. An analytical approach to LFN modeling of these devices is presented in this thesis.

Thesis structure

This work is a product of research on two distinct subjects, namely TID and noise characterization of MOSFET devices. As such, the most appropriate form to present it was chosen as follows. After this brief introductory part (ch.1), three main chapters are presented.

The first chapter (ch.2) is divided into three sub-sections, each briefly dealing with theoretical background knowledge on the subjects of the following chapters. Initially the basic mechanisms behind the interaction of ionizing radiation with semiconductor oxides are explained, with emphasis on the specific types of damage pertaining to this work. Afterwards basic theory on low frequency noise is presented along with the noise models integrated in the EKV3 MOSFET model. Closing this chapter are the brief demonstrations of the methods used to extract the basic operation parameters used throughout the rest of the thesis.

In the second chapter (ch.3), our focus is the damage inflicted by ionizing radiation on specific 65nm transistors. After a short report on the state of the art and the events necessitating this research endeavour, a more targeted theoretical description is given, based on the response to TID of the specific 65nm technology used, as has been recorded in recent literature produced by collaborating researchers in this field. The experiment conditions are then highlighted and our data is documented in the form of scaling plots for multiple device types (n-, p-MOS, low, standard and high V_{TH}) and temperatures ($-30°C, 0°C, 25°C$), with accompanying commentary. We have elected to organize our data according to the two main recorded damage mechanisms, those related to the channel length becoming shorter and those to the channel width becoming narrower. The chapter ends with a discussion pointing out interesting observations and correlating the previous plots with our theoretical expectations.

In the third chapter (ch.4) the whole procedure and methodology for measuring low frequency noise in our laboratory is presented. We showcase the algorithms used for data acquisition and analysis as well as the thought process behind our actions. The EKV3 parameter extraction procedure is described for both incorporated noise models. Subsequently we introduce the analytical model we fitted on our data and present our measured noise data with this model. We then conclude with discussion on our findings.

Closing the thesis, additional plots regarding the TID study are appended, followed by a list of the author's publications and the referenced bibliography.

2 Theory

2.1 Ionizing radiation interaction with MOSTs

Semiconductors have always exhibited degraded performance or uncharacterized behaviour after exposure to ionizing radiation, so their interaction has been a field of study since the integration of semiconductors in aerospace engineering, nuclear science or other applications where electronics need to be able to withstand adverse radiation conditions. Ionizing radiation is an umbrella-term that usually encompasses particles (α *and* $\pm\beta$ radiation, protons, neutrons or other heavy particles) or photons (high energy UV, X-rays, γ-rays), and often times a mixture of the previous. Two main kinds of ionizing radiation issues are commonly studied, one-time events (usually called *"Single Event Upsets"*, such as random byte flips in digital circuits, random glitches or at worst even catastrophic latch-ups, and accumulated damage induced through long term exposure. The second type falls under the acronym *"TID"* which stands for *"Total Ionizing Dose"* and is the subject of this work. Specifically, damage inflicted on Metal Oxide Semiconductors under very high levels of photon (X-ray) TID, normally not encountered in most applications (aerospace and nuclear). The total absorbed dose is measured in grays (Gy), an SI unit defined as the absorption of one Joule of energy into one kilogram of matter. An older unit of absorbed dose is the rad, equivalent to one erg of energy into one gram of matter, also equivalent to 10mGy. In this work rads have been used. As matter absorbs radiation differently, based on the type of radiation as well as the type of matter, when referring to an absorbed dose, the type of matter (i.e. SiO_2) should also be specified. In this work we will only be examining the TID effects on SiO_2 and thus omit the specification. In the following paragraphs we will present a short description of the interaction between high energy photons and semiconducting materials.

As described by [9], three main mechanisms exist for high energy photons to interact with matter. With increasing photon energy, these are the photoelectric effect, Compton scattering and pair production. In the energy levels involved in the X-rays used in the experiments for this work (tens of keV) the photoelectric effect is dominant, with photons interacting with silicon and silicon dioxide atoms ($Z_{Si} = 14$ and $Z_O = 8$). Of interest to us is the ionization of one of the innermost electrons (K shell) which is ejected from the atom. Following, an electron belonging to the L shell drops to fill the vacant state and leaves behind a hole (while also emitting a lower frequency photon). Thus an initial $e^- - h^+$ pair is created. The ejected electron can collide with and ionize neighbouring atoms as well, thus producing more pairs. Damage in MOS devices occurs from charges becoming trapped in the oxides or in the oxide interfaces. As technology progresses and the gate oxide becomes thinner, the ancillary oxides prove to be more important sites for such charge generation and trapping.

A small percentage of the generated e-h pairs recombines, however a larger percentage does not, owing to the large mobility of electrons in the oxide relative to the holes. The percentage that does not recombine is termed *"charge yield"*. As electrons in the oxides can have mobility values orders of magnitude larger than holes, they can more easily (and quickly) travel to the channel interface and be removed, thus the holes become more important when discussing the long term effects of TID. Acted on by the electrical field, holes migrate through "polaron hopping" [1] towards the negative electrode, the gate/SiO_2 interface in the case of PMOS and the SiO_2/channel interface in the case of NMOS. Temperature and oxide thickness as well as the external electric field play a part in the speed of the hole migration. Along their movement, holes can take the place of hydrogen atoms trapped in the oxide lattice, thus also freeing protons in the oxide. Hydrogen is a remnant from the semiconductor fabrication process and can be trapped inside the oxides in small but considerable quantities.

[1] polarons are quasi-particles, i.e. more complex systems which can be examined as single particles. Specifically, polarons have been used to study charge conduction through a dielectric crystal, as is the case for SiO_2 here, and manifest as the effect of electrons moving through the crystal lattice, while the electron clouds around neighboring atoms deform due to the electron's electric field. This local lattice deformation travels along with the mobile electron, giving it a larger effective mass.

Amorphous silicon dioxide (as is the case of the oxide resulting from deposition or thermal oxidation used in semiconductor manufacture) consists of a lattice of interconnected silicon and oxygen atoms, with each silicon atom forming a bond with four oxygen atoms around it. Each oxygen is shared between two neighboring silicon atoms thus each silicon atom is bonded to four "halves" of oxygen atoms, leading to the SiO_2 chemical formula. This is schematically represented in the following figure.

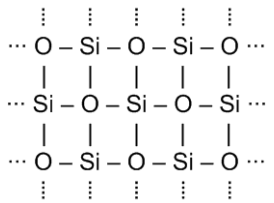


Figure 1: Schematic (2D) representation of amorphous silicon dioxide crystal

When an oxygen is missing from the lattice (defect), a weak bond is formed between two adjacent silicon atoms sharing their unpaired electrons in an energy state just above ($\sim 0.5 - 1eV$) the valence band. This bond can be broken by a hole (in our case generated by radiation as explained before), leading to a silicon atom with a net positive charge (trapped positive charge) and the second silicon atom with an unpaired electron. Depending on the spatial position of this trapped state, i.e. its proximity to the silicon substrate, it may be easy for an electron to tunnel from the substrate and pair with the previously unpaired electron. The traps nearest to the oxide (in the range of 3nm from the interface) are called border traps and are the most probable to recombine with electrons from the substrate in this way. This is a neutralized state which can evolve in two ways, either with the electron tunneling again back towards the substrate thus vacating the trap and regenerating the intermediate $Si^+ - Si^-$ state, or with the two electrons becoming shared between the two Si atoms returning the system to its initial state with the Si-Si bond and annealing the trap. The deeper traps can be annealed in a much longer time-frame, thus surviving for greater periods of time.

Previously in this chapter we mentioned hydrogen being released from trapped states in the SiO_2. To elaborate on the presence and abundance of H atoms in the MOS oxides, we must consider the fabrication process. After the amorphous thin gate oxide is deposited, due to the lattice constant mismatch between Si and SiO_2, Si atoms are left with unbonded electrons on the oxide side, usually referred in the literature as "dangling bonds". In order to passivate these unpaired electrons, the whole semiconductor is flushed with hydrogen gas. The hydrogen additionally passivates similar states in the outer surface of the oxide, providing lower leakage. This is inconsequential to the mechanisms described here but highlights the multiple benefits this treatment provides and its ubiquity in semiconductor manufacturing. Atomic H permeates thin oxides preferentially to molecular H_2 [2] and thus can be found trapped in the oxide (unintended side-effect) or can be found in the $Si - SiO_2$ interface terminating the unpaired electrons and "dangling" towards the channel (intended effect). This procedure is unsurprisingly termed *"passivation"* in the semiconductor manufacture community.[37] Returning to the way ionizing radiation damages MOS oxides, in the literature the mechanism is usually named *"depassivation"* and refers to the liberation of the trapped H atoms (as H^+ ions, namely protons) by migrating holes, which then slowly themselves migrate towards the oxide interface under the influence of the electric field. At the interface they break the passivated Si-H bond, forming molecular H2 and leaving behind the dangling Si electron. The trapping sites formed which are usually named *"interface traps"* can be either donor-like or acceptor-like depending on their energy level in the band structure which is determined by the external biasing. Effectively, in NMOS this results in the majority of interface traps being negatively charged while in PMOS the majority is positive. In contrast, the traps in the bulk of the oxide are always positive. Together they provide the parasitic electric fields that destabilise TID affected MOSFET operation. Owing to the much lower H^+ oxide mobility, the interface traps need much longer to accumulate (and conversely, anneal) leading to an interesting

interplay between the oppositely charged trap types in NMOS devices, during the evolution of the TID experiments, as well as the aggravated damage observed in PMOS devices, all of which we will exhibit in a following chapter. This whole mechanism can be summarized in the following simplified schematic representation in an NMOS transistor.

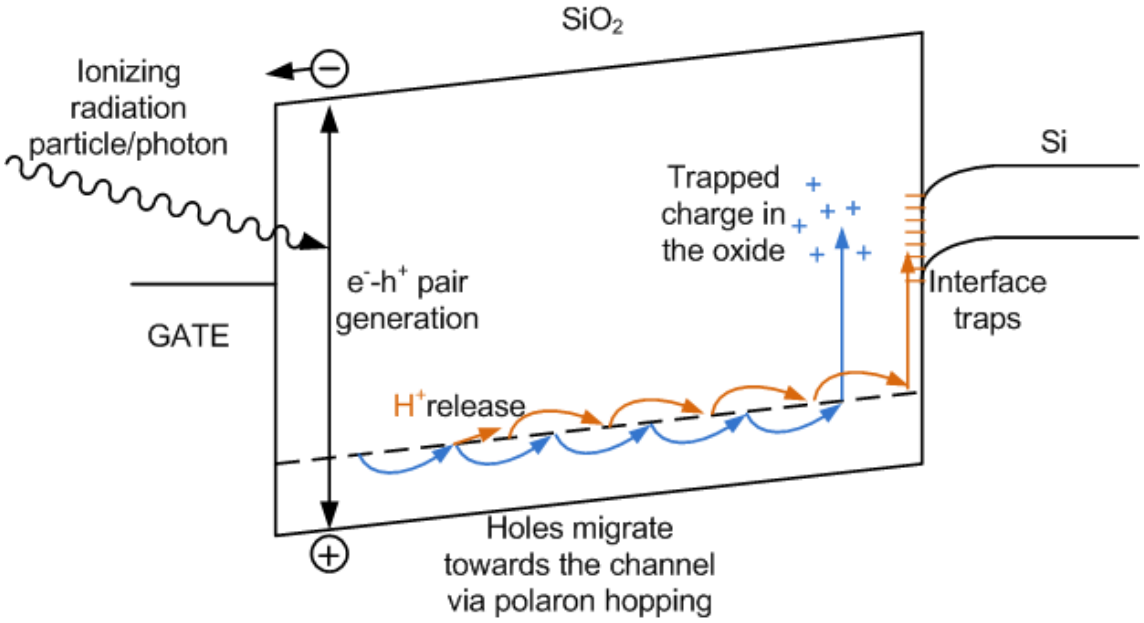


Figure 2: Schematic representation of the mechanism for oxide and interface trap creation in N-type device under TID

2.2 Flicker Noise in MOSTs

Noise signals in semiconductors are the random fluctuations in current or voltage that can degrade SNR. Several types of noise have been observed and studied in semiconductors, such as thermal noise, shot noise, random telegraph noise/signal (RTN/RTS) and flicker (or 1/f noise). The mechanisms behind the different types have been studied since the dawn of electronic components, even before the advent of semiconductors, and have been understood and described to a greater or lesser extent. In this work we will be analyzing flicker noise in MOSFETs, thus this will be the center of our attention in this following chapter.

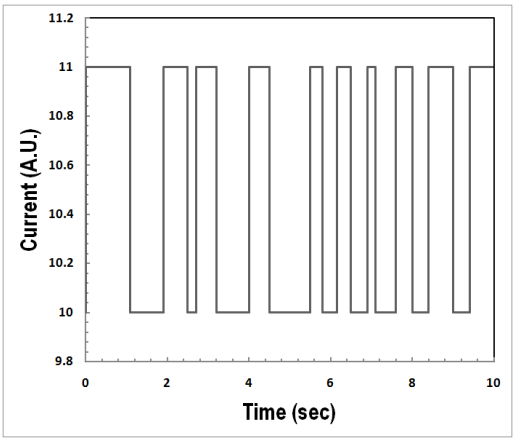
Noise signals are by nature truly random, which means one cannot predict their evolution in time given their history. As described by [26], in semiconductors the fluctuating current or voltage is recorded over a longer time period and then represented in the frequency domain, usually by means of the power spectral density, i.e. the noise power contents at specific frequencies. The average power of a noise signal is given by:

$$P_{AV} = \lim_{T\to\infty} \frac{1}{T} \int_0^T x^2(t)\, dt$$

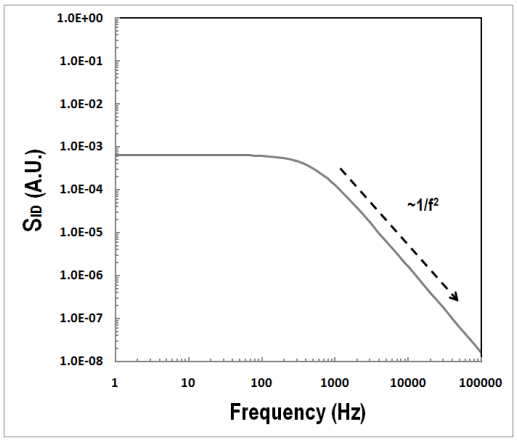
where x(t) is the measured noise signal in the time domain, during a time period of T. P_{AV} can be measured in V^2 or A^2, whereby the actual power consumed by a load can be calculated by dividing or multiplying with the load resistance. Converting this to the frequency domain, through a fourier transform of the time-domain signal, here represented by X(f), we can get the PSD in $\frac{V^2}{Hz}$ or $\frac{A^2}{Hz}$, which is in itself a valuable tool used to visualize and analyze noise responses. The PSD is given by:

$$S(f) = \lim_{T\to\infty} \frac{|X(f)|^2}{T}$$

The presence of traps along the $Si - SiO_2$ interface is unavoidable despite efforts to optimize fabrication processes. These trapping sites can have varying energy depths, far below the Fermi potential, in which case they are considered to be mostly occupied, or far above, making them empty. The ones closest to the Fermi potential (by a factor of some kT) are those that contribute actively to the trapping (and subsequent de-trapping) of channel carriers. These traps can capture and release carriers with different time constants, related to the trap's energy level. De-trapping is caused by the thermal vibrations of the crystal lattice, explaining the stochastic nature of the phenomenon. When a carrier is trapped, the current through the channel decreases infinitesimally with the reverse happening when the carrier is re-emitted. Macroscopically this is observed as random fluctuations in the channel current (output-referred noise) or fluctuations in the gate voltage (input-referred noise). If a single trap was active in the channel, the effect would be a fluctuation between two levels in the output current (or conversely in gate voltage), one for the trap being empty and another for the trap being occupied. In the time domain, this results in a signal reminiscent of telegraph signals (pulses of shorter or longer duration with spaces inbetween) with a random nature, hence the name RTN or RTS. When this single trap noise signal is converted from the time to the frequency domain, the result is a lorrentzian spectrum, with a flat plateau up to a certain frequency and then a $\frac{1}{f^2}$ drop in power.



(a) Representation of RTS noise produced by a single trap in time domain.



(b) Representation of Lorrentzian PSD produced by single trap in frequency domain.

As more and more traps are added to this simplified approach, assuming that they are uncorrelated and have time constants distributed over a wide range of frequencies, their resulting PSD tends to the $\frac{1}{f}$ trend characteristic of flicker noise. [14]. As each trap removes a carrier from the channel it not only causes a fluctuation in the number of carriers but also introduces a static point charge which repels carriers (a process called Coulomb scattering), thus locally modulating the channel effective mobility.

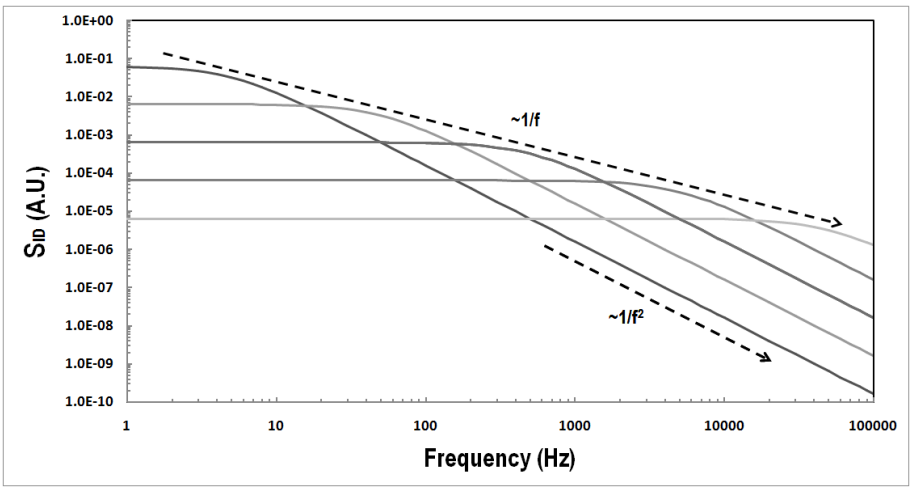


Figure 4: Multiple Lorrentzians approximate a 1/f (flicker) PSD. Here the effect is demonstrated with just five.

2.2.1 EKV3 Noise Modeling

The EKV3 MOSFET model incorporates two different approaches towards modelling of flicker noise. The parameter "lfnoi" is used as a flag to switch between the two. For a value of "0" the basic model is active while for a value of "1" the more advanced is used instead. The basic model functionality is the industry standard approach [15] of calculating the output-referred noise (S_{ID}) as follows:

$$S_{ID} = \frac{K_F g m^{E_F}}{C_{OX}^2 W L f^{A_F}}$$

with the S_{VG} coming from the division of S_{ID} by gm^{E_F}. In theory A_F equals to 1 and E_F to 2. In practice, however A_F can vary between 0.8 and 1.2 in most cases, depending on the actual noise-frequency slope and E_F can vary slightly around the value of 2, therefore they are given as parameters to ensure better fitting of the model. K_F is strongly process dependent and governs the general noise levels.

If the lfnoi flag is set to "1" the more complex model is enabled and parameters K_F and E_F are ignored. The parameter A_F retains the same functionality as before. For the actual noise model, a more complex mechanism has been incorporated in the model code [25, 27, 29], based on physical phenomena, namely the McWorther model, describing the carrier number fluctuation [14], the Hooge model concerning the carrier mobility fluctuation [22], as well as the access resistance contribution. A short explanation of each parameter's function follows:

- "nt" is the total number of traps.
- "alphac" is the Coulomb scattering coefficient.
- "ecn" is the critical field value, involved in the effect of velocity saturation on 1/f noise in shorter channels.
- "alphah" is the Hooge mobility fluctuation model parameter.
- "sdr" is the series resistance noise parameter.

The three first parameters are associated with the McWorther model which successfully describes the strong inversion noise response, while the Hooge effect parameter comes into play for weak inversion operation as can be seen in the following plot.

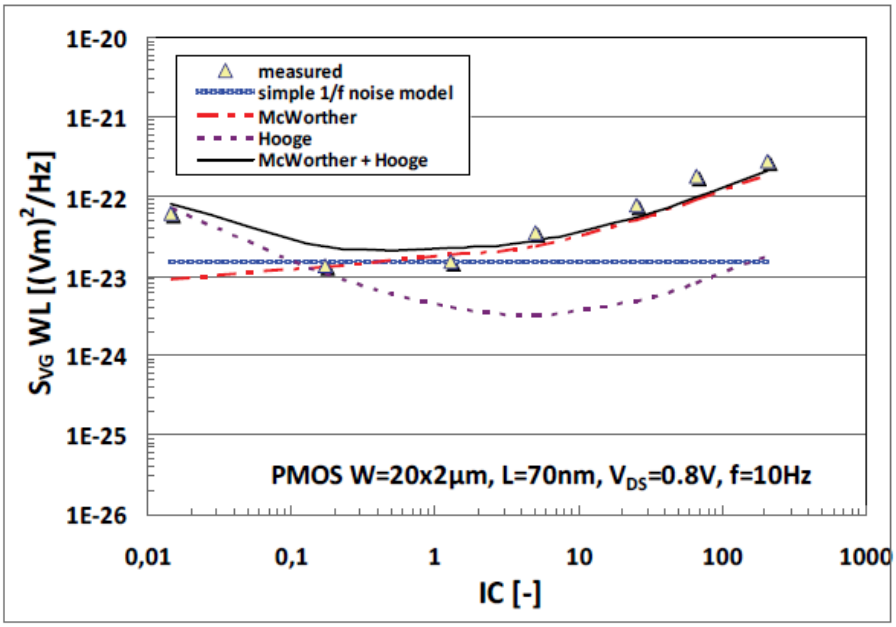


Figure 5: S_{VG} plot demonstrating the superior performance of the more complex EKV3 flicker noise model, as demonstrated in [27]

2.3 Extraction methods for operation parameters

Some device operation parameters are of importance to a model engineer or designer. As such, methodologies have been published on how to extract these from measurements. Here we present some of the most useful methodologies that have been applied throughout the course of data acquisition and analysis as part of this work.

2.3.1 Weak inversion slope factor, n

The WI slope factor can be easily calculated by the plateau displayed by the $\frac{g_m U_T}{I_D}$ when plotted versus I_D. The value of said plateau is equal to $\frac{1}{n}$

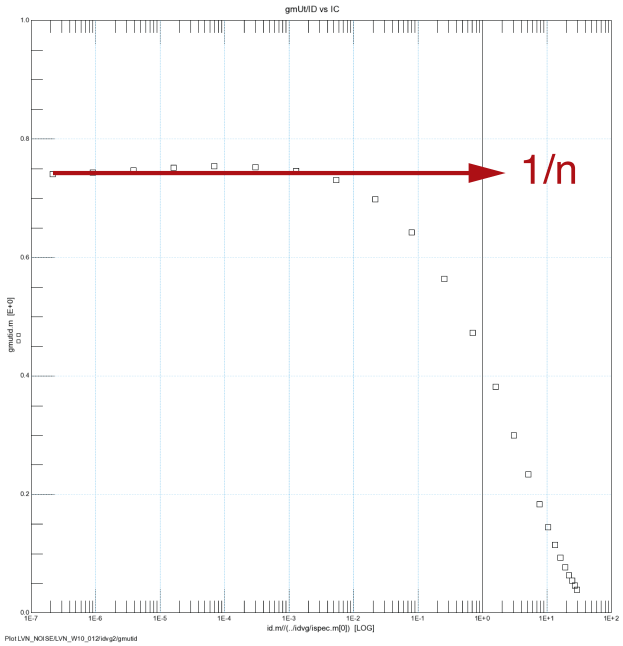


Figure 6: $\frac{g_m U_T}{I_D}$ vs IC

2.3.2 Mobility (maximum)

Using the strong inversion and saturation assumptions, the MOS drain current is given by:

$$I_D = \frac{n\beta}{2}(V_P - V_S)^2$$

$$where\ V_P = \frac{V_{GS} - V_{T0}}{n}$$

$$\sqrt{I_D} = \sqrt{\frac{n\beta}{2}}(V_P - V_S)$$

$$\frac{d\sqrt{I_D}}{dV_{GS}} = \sqrt{\frac{n\beta}{2}}\frac{d}{dV_{GS}}(\frac{V_{GS}}{n} - \frac{V_{T0}}{n} - V_S)$$

assuming V_{T0}, n, V_S constant, and knowing $\beta = \mu C'_{OX}\frac{W}{L}$

$$\frac{d\sqrt{I_D}}{dV_{GS}} = \sqrt{\frac{n\beta}{2}}\frac{1}{n} = \sqrt{\frac{n\beta}{2n}} = \sqrt{\frac{\beta}{2n}}$$

$$(\frac{d\sqrt{I_D}}{dV_{GS}})^2 = \frac{\beta}{2n} = \frac{\mu C'_{OX} W}{2nL}$$

$$\text{therefore } \mu = \frac{2n}{C'_{OX}}\frac{L}{W}(\frac{d\sqrt{I_D}}{dV_{GS}})^2$$

Obviously μ has a maximum at the maximum of the $(\frac{d\sqrt{I_D}}{dV_{GS}})^2$ term, which can be easily calculated from measured data. If C'_{OX} is not available, this method can still be used to calculate the $\mu C'_{OX}$ quantity

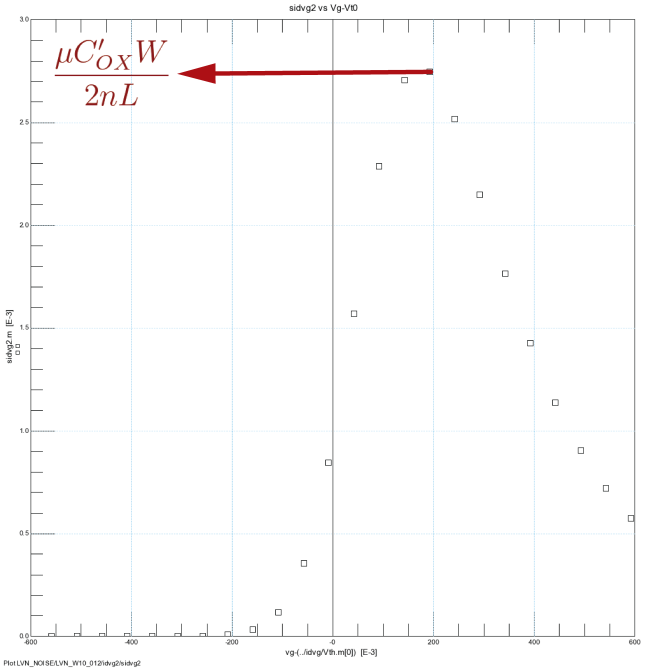


Figure 7: $(sqrt\frac{dI_D}{dV_G})^2$ vs $V_G - V_{T0}$

2.3.3 Specific current, I_{SPEC}

I_{SPEC} is the normalization factor for the Drain current of a MOS transistor. The inversion coefficient is the normalized version of I_D and thus is defined as $IC = \frac{I_D}{I_{SPEC}}$ I_{SPEC} is defined as:

$$I_{SPEC} = 2nU_T^2\beta$$

where $\beta = \mu C'_{OX}\frac{W}{L}$ and n is the weak inversion slope factor.

Utilizing the above formula for $\mu C'_{OX}$ and substituting, we can calculate

$$I_{SPEC} = 4n^2 * U_T^2 * max[(\frac{d\sqrt{I_D}}{dV_{GS}})^2]$$

2.3.4 Threshold Voltage, V_{T0}

The term V_{T0} implies zero back-bias ($V_B = V_S = 0$). As this was almost always the case in this work, this will be presented here and terms V_{T0} and V_{TH} will be used interchangeably.

The easiest way to extract the threshold voltage in saturation is with a constant current criterion. A threshold current I_{TH} is set, often arbitrarily, close to the moderate inversion part of an I_D versus V_G curve. Then, by finding the precise V_G which corresponds to the chosen I_{TH} on I_D versus V_G we have the threshold voltage. As it is almost impossible for the chosen current value to correspond to one specific measured V_G, most often an interpolation between two data points has to be used. The same criterion for saturation can be applied to the linear region, resulting however in an overestimation of the linear V_{T0} and subsequently the DIBL factor.

In this work, for accuracy, we have followed the *"adjusted constant current"* methodology, as described in [3]. The current criterion is thus defined as $I_{TH} = \alpha * I_{SPEC}$, with the value of the α parameter is solely dependent on V_D and is calculated by the following:

$$\alpha = q^2_{S|V_P=V_S} + q_{S|V_P=V_S} - q^2_{D|V_P=V_S} - q_{D|V_P=V_S}$$

$$\text{where } q_{S|V_P=V_S} = \tfrac{1}{2}F^{-1}(2e^0) \text{ and } q_{D|V_P=V_S} = F^{-1}\tfrac{1}{2}(2e^{\frac{-V_D}{U_T}})$$

$$\text{and } F^{-1} \text{ is the Lambert-W function}$$

The above is the simplified outcome of the basic voltage-charge relationship:

$$2q_x + lnq_x = u_p - u_x$$

(expressed for an arbitrary point x along the channel)

and solved under the specific conditions that $V_B = 0$, $V_S = 0$ and $V_P = V_S = 0$, as the V_{TO} is defined as the V_G at which the lowest potential point of the channel needs to be at least above pinch-off. In our case this is the Source end of the channel, thus the requirement that $V_P = V_S$. The value of α asymptotically approaches the value of 0.608 for saturation operation. This method is much more accurate when used to estimate the DIBL effect compared to simpler constant current methods.

While the most precise results would be given by calculating the specific current for each device, we can instead calculate the specific current for a large device and geometrically scale it (by multiplying with $\frac{W}{L}$) for the specific geometries of interest. This way we introduce some degree of inaccuracy for the smaller dimensioned transistors, by disregarding the I_0 decrease due to velocity saturation, but we gain a large simplification in our data analysis efforts. Additionally, as this work pertains to the degrading effects of radiation on CMOS transistors and their relationship to device dimensions, more self consistent results are guaranteed by using the geometrical scaling method extracted from a larger device.

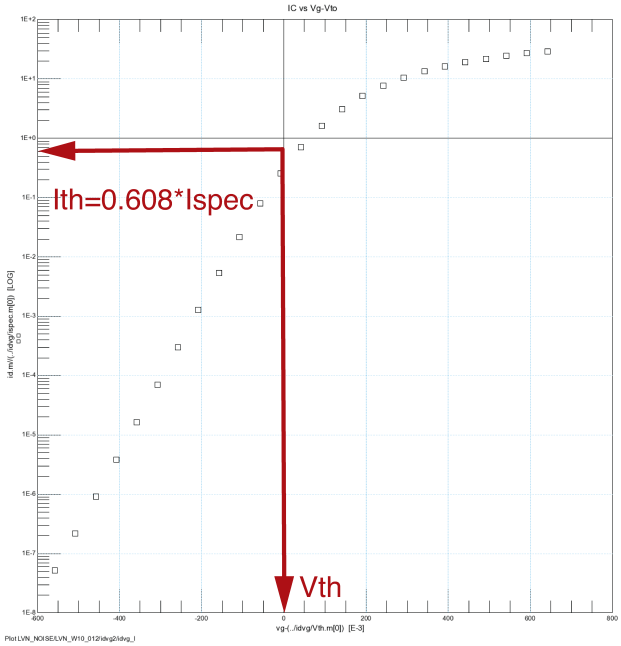


Figure 8: IC vs $V_G - V_{T0}$ for saturation operation. The IC corresponding to the V_{TH} is shown relative to the IC=1 horizontal line. The results

3 Total Ionizing Dose effects and characterization in 65nm CMOS technology

This part of the thesis pertains to the characterization of a commercially available 65nm CMOS technology intended for the proposed upgrades to the Large Hadron Collider (LHC) at CERN. This was a group effort on the part of the Electronics Laboratory at TUC in the span of 2017-2019. The LHC is scheduled for a hardware upgrade during a long machine shutdown that will take place in the years 2023-2025 with the goal of being operational by the end of 2027. The upgrade has been termed the HL-LHC (High Luminosity LHC) and is designed to increase the luminosity of the beam tenfold. For this reason radiation hard electronics are being investigated for use within the detectors, situated closest to the collision-event sites, thus being subjected to the highest levels of ionizing radiation. According to simulations, the expected Total Ionizing Dose (TID) in the useful lifetime of the experiment is expected to reach 1Grad (SiO_2), 1000 times over the rating of contemporary military and aerospace rad-hard devices.

The first two phases of the LHC experiment were designed using 250nm and 130nm electronics respectively. By 2011, in view of the future update, investigation of the radiation resistance, as well as operational trade-offs of a 65nm technology began [5]. Such investigations continued over the years [31, 30, 23] and by 2015, rudimentary modifications involving the V_{TH} and mobility parameters were implemented in the models provided by the foundry, to account for the TID effects and give designers a feel for the performance degradation induced by the ionizing radiation. In the summer of 2017 the Electronics Laboratory team at TUC undertook the task of extracting DC model parameters for various TID levels, at three different operating temperatures ($-30°C$, $0°C$, $25°C$), for devices of standard[34, 35, 16] and enclosed layout[13, 33, 32, 35], ranging from low- to standard- to high-V_{TH}, of N- and P-type. In the next sections the devices and measurement conditions will be presented, followed by the analysis of the data for the extraction of figures-of-merit valuable in analog IC design [35]. The section concludes with a discussion of the results.

3.1 TID degradation mechanisms observed in 65nm bulk CMOS

As technology nodes continue to scale down into the deep sub-micron level, the traditional source for incurring TID damage, namely the gate oxide, has shrunk to such low thickness that it no more contributes to performance degradation. Instead, the main source for performance drop-off has been narrowed down to two main contributors: The sidewall STI (Shallow Trench Isolation) oxide as well as the thicker ($\sim 20nm$) oxide and nitride (Si_3N_4) spacers used as masks for the LDD (Lightly Doped Drain) extensions play parts in complex mechanisms involving the generation and migration of charges that ultimately impair device performance. This multifaceted phenomenon has been the subject of much study in the last decades as it manifests differently for a multiplicity of variable conditions including but not limited to the manufacturing process[19, 11], biasing[11, 38], temperature [10, 16], dose rate [10] and more factors. Even though it is not part of this work, it should be mentioned that similar exploratory work has been carried out in 65nm bulk CMOS of different manufacturers [11] as well as smaller technology nodes such as a commercially available 28nm bulk CMOS process [39, 8, 38] that is being considered as an alternative to the 65nm process investigated here and even emerging MOS technologies [21, 12]. In addition to static DC characterisation, work is also been done on the noise response of such devices and its susceptibility to TID [36, 7, 21].

Returning to the specific 65nm process that lies at the center of this work, the two oxides mentioned before have been studied at length [20, 18, 6, 11] and the main mechanisms for device impairment will be shortly presented here. The two contributions seem to become more evident as device dimensions are scaled down and can be analysed by device type and the dimension being made smaller.

3.1.1 RISCE

The term RISCE stands for Radiation Induced Short Channel Effect and is observed mainly as the device length becomes shorter. It is mainly attributed to the effect of charge-trapping in the spacer oxides and nitrides over the LDD extensions and at the oxide-channel interface. These oxides are deposited, resulting in lower crystal quality with many lattice defects. Additionally the nitrides require hydrogen gas during their deposition, in the form of ammonia gas, which decomposes under high temperature to provide the nitrogen. Even in highly optimised processes the resulting nitride can be contaminated with several percent hydrogen, which remains trapped in the resulting oxide/nitride in addition to the quantity already present in the oxides due to their passivation. During irradiation electron-hole pairs are created as well as H^+ ions are liberated in the spacers. In the presence of high electrical fields, such as in the experiments of this work, these charged species are either trapped in the oxides becoming a fixed positive charge or migrate (at differing rates, dependent on type and temperature) towards the gate oxide and channel interface, creating traps. In PMOS devices these charges are positive and create an electric field repelling mobile carriers away from the LDD p^- regions, thus decreasing the available carrier number and thus the current carrying capability of the device overall. This can be interpreted as an increase in the series resistance, or as has been done in this work, a reduction of the effective mobility. The trap activation energy makes their effect bias dependent and difficult to characterize, as the specific biasing conditions determine the severity of the mobility reduction. In NMOS devices the n^- LDD regions become slightly more inverted owing to the electric field produced by the also positive trapped charge in the oxide, however this is inconsequential, as the LDD regions already have a lower conductivity than the rest of the device. Instead the damage observed is more akin to hot carrier injection, which the effective dopant concentration in the LDD, disturbed by the extra charges, was engineered to avoid. This is further supported by the observed bias dependence of the degradation in N-type devices, having a relationship with bias very similar to the conditions resulting in HCI. The migration of charges towards the interface results in both types in an increase (in absolute value) of the V_{TH}, which also affects the current handling of the device. In PMOS, charges seem to be less mobile, with V_{TH} shifts appearing at higher temperatures or after annealing, while in NMOS the shifts happen at the same time as the irradiation and are generally larger. In PMOS these interface traps are of positive sign and synergize with the fixed charge, while in NMOS they are of negative sign and to a degree negate the effects of the positive fixed charge, resulting in a smaller current reduction (also attributed to the increased V_{TH}) than in equivalent PMOS transistors.

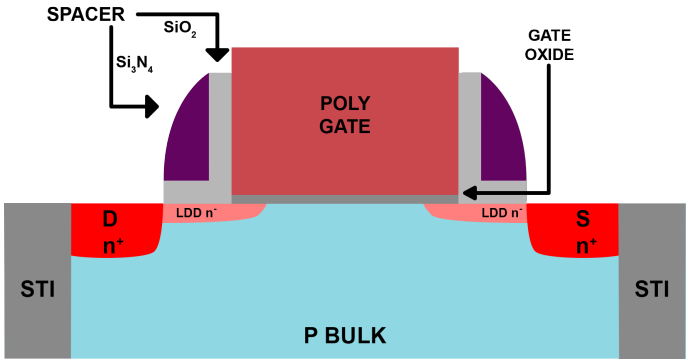


Figure 9: N-MOSFET side-view. Visible are the spacer oxides and nitrides that contribute to the RISCE. Also shown are the lightly doped drain and source extensions whose function becomes compromised with TID as described above. Damage cannot be easily depicted schematically. Only NMOS is shown.

3.1.2 RINCE

Narrow channel transistors are also very susceptible to TID through a mechanism named RINCE (Radiation Induced Narrow Channel Effect). Here the oxide involved is the STI oxide, used for device separation as well as stress engineering of mobility, a technique in which the larger volume of the SiO_2 is used to laterally compress the crystal and increase the effective carrier mobility in the direction of the compressive stress. Again, N and P types respond differently, to the fixed positive charges that accumulate in the bulk of the oxide. NMOS respond by becoming leaky, as the positive charge along the channel sidewall provides an inverting electrical field, attracting charge and providing leakage paths along the edge of the channel. As this charge is ever-present, its largest contribution is seen at a gate voltage $V_G = 0$, where instead of the channel being shut off, the parasitic edge channels continue to weakly conduct, thus increasing the leakage current (I_{OFF}) and consequently, the power dissipation even with the device off. The extreme case of this effect are devices that effectively cannot be turned off. In contrast, the failure mode in PMOS devices is the opposite. The fixed positive charge makes the channel more difficult to invert and control via the gate, effectively decreasing the channel width and increasing the series resistance (or again, lowering the effective channel mobility). Again charges that migrate due to the fields present, create interface traps at the oxide-channel interface, positive in PMOS and negative in NMOS. As with RISCE this lessens the effects in NMOS devices while it adds-up and concludes with the PMOS devices acting like high value resistors, with their current drive severely limited. As these effects are limited to the channel area neighboring the STI sidewall, it should be easily understood that they are of similar magnitude in wide and narrow devices, thus when overall width is small, they affect a larger percentage of the effective channel area, making their contribution more important.

While the above analysis is by no means highly detailed, it provides the two basic axes along which ultrahigh doses affect bulk CMOS transistors. It should be obvious then, that in devices where both dimensions are designed to be small simultaneously, RISCE and RINCE effects can be detrimental to device longevity and operation. It also highlights a design practice that has been utilised for the previous generations of electronics at CERN as well, radiation hardness by design, meaning that specific geometries and layouts are employed to minimise or avoid some effects. More specifically, enclosed gate transistors (alternate name: edgeless transistors) have been designed, in which the drain is placed at the center and the gate and source form annular rings around it. This all but eliminates RINCE effects, as the charge trapped in the STI does not affect the channel. Instead the source terminal electrically shields the channel and does not permit the STI charge electric field to penetrate inside. This leaves only RISCE effects to contend with, at the cost of a larger device footprint.

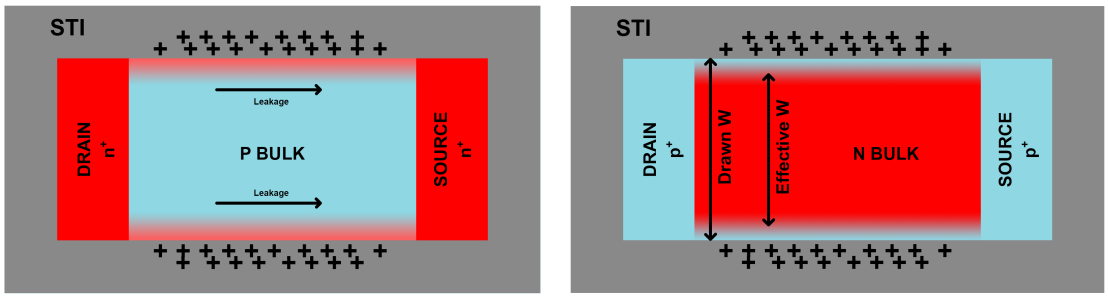


Figure 10: N- (left) and P-MOSFET (right) top view, with gate structure removed. NMOS device is depicted under $V_{GS} = 0$, $V_{DS} \neq 0$ (device should be shut-off) with the parasitic leakage paths visible along the length of the device. PMOS device is depicted under operating conditions, $V_{GS} < 0$, $V_{DS} < 0$ and the sides of the channel unable to form an inversion layer are visible.

3.2 Devices and measurement conditions

The test chips provided to us for TID characterization were fabricated as arrays containing multiple geometries, with shared Source, Bulk and Gate electrodes and individual Drain terminals. Gate anti-static protection circuitry was included. Irradiation and measurements were carried out at CERN, using their 50kV 3kW X-ray generator (SEIFERT RP149) at a dose rate of 9Mrad/h. Initially a measurement of all devices in the array was performed before irradiation (pre-rad) and afterwards at TID levels of 100, 200 and 500Mrad. During irradiation the devices were constantly diode-biased at what is considered "worst-case" (with regards to TID damage) for this technology, $|V_{GS}| = |V_{DS}| = 1.2V$, the maximum allowed voltage. During measurement the X-ray source was turned off and DC output and transfer curves with and without back bias were recorded. As temperature plays a major role in the extent of the degradation, for each temperature a fresh array was irradiated and measured.

In the following section we will be presenting NMOS and PMOS devices belonging to the Standard V_{TH} variety and comparing the TID effects at three different temperatures, -30°C, 0°C and 25°C as well as devices belonging to Low, Standard and High V_{TH} varieties, irradiated at 0°C and comparing their individual response to TID. The geometries presented are part of length scaling arrays with a device width of $W = 1\mu m$ and width scaling arrays of device length L=60nm. The length scaling arrays serve to illustrate the RISC effects while the width scaling arrays the RINC effects. The short L array was preferred over a longer L one because of larger availability and variety of data as well as a means to directly showcase the absolute worst case scenario of short and narrow devices, in which RISCE and RINCE both become important. The analog design parameters we extracted and present in the following sections are (in the order presented):

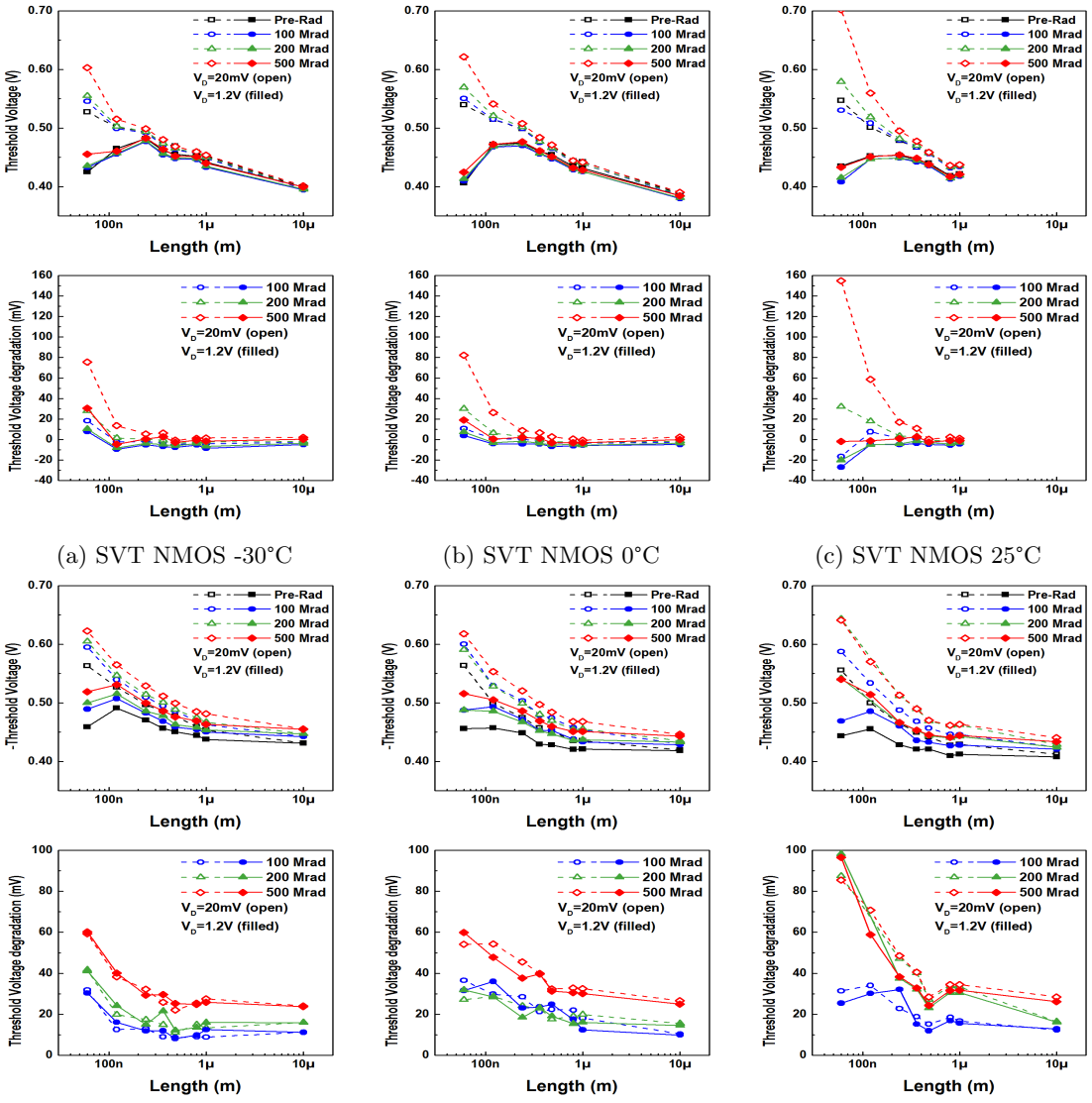
- Threshold Voltage for linear ($|V_{DS}| = 20mV$) and saturation ($|V_{DS}| = 1.2V$) operation in a common graph
- DIBL factor
- Weak inversion slope factor (n)
- On-Current, normalized for device geometry
- Transconductance factor (KP), as a measure of the effective mobility, normalized for device geometry
- Off-Current (leakage current), normalized for device width

We chose to normalize the on-state current and the transconductance factor (itself a measure of device effective mobility) with an $\frac{L}{W}$ factor to be better able to observe the phenomena regardless of device geometry. For the same reason the leakage current was normalized with a $\frac{1}{W}$ factor, as device length does not play a role in leakage. For each parameter's scaling plot, a companion graph is also presented showing the percentage degradation from the pre-irradiation value. These degradation graphs provide an immediate and easily perceivable image of the TID response and help in the interpretation of our results. In the appendix we have also made available similar plots for the following:

- Width scaling array comparisons between Standard V_{TH} devices with $L = 10\mu m$, at -30°C, 0°C and 25°C
- Width scaling array comparisons between Low, Standard and High V_{TH} devices with $L = 10\mu m$, at 25°C (with the highest TID level being 400Mrad for Low and High V_{TH} devices)
- Length scaling array comparisons between Standard V_{TH} devices with $W = 20\mu m$, at -30°C, 0°C and 25°C

3.3 Length Scaling, Width=1μm

3.3.1 Threshold Voltage Length Scaling, SVT, at -30,0,25 °C



(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

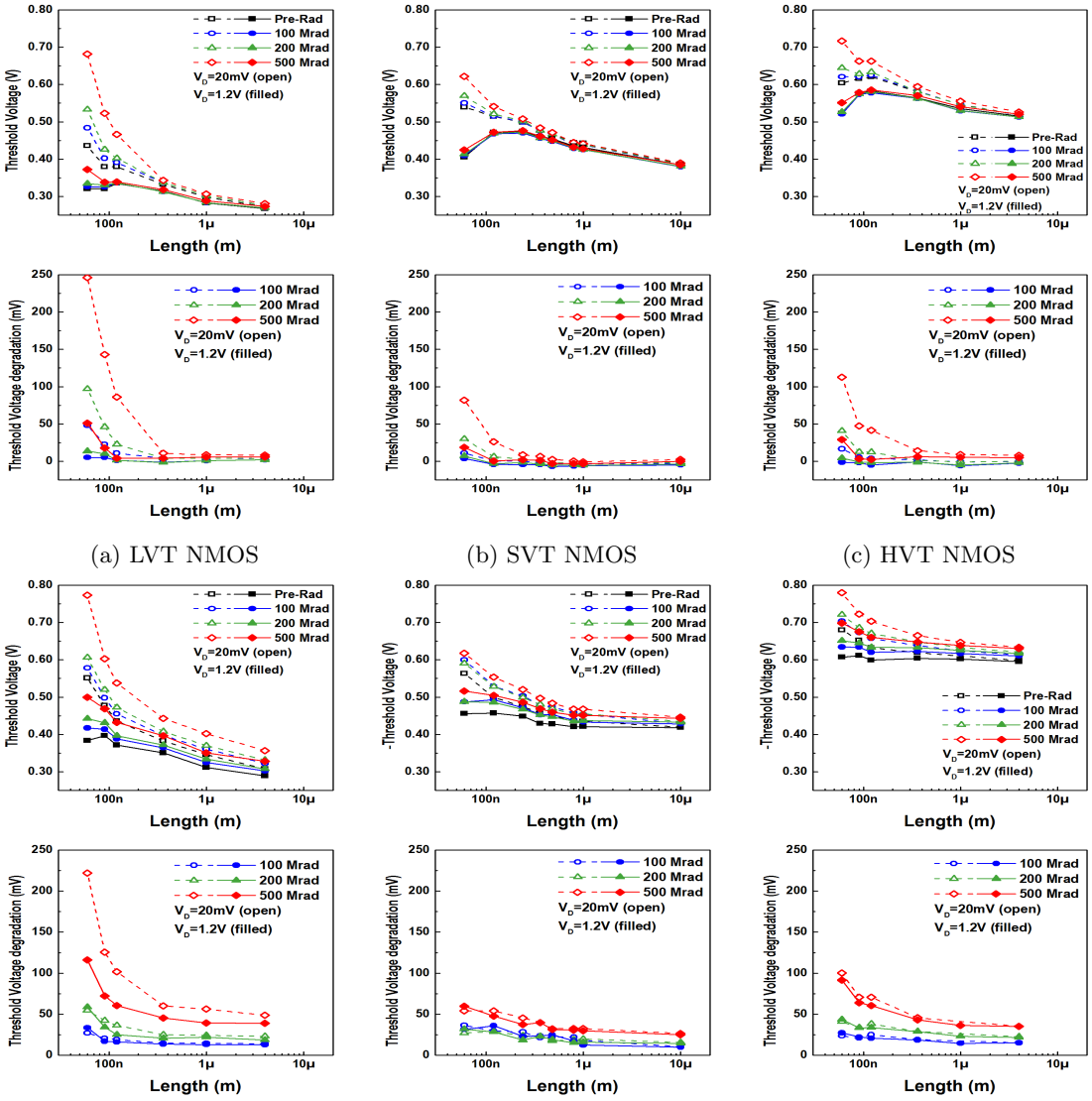
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 11: V_{TH} and degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

In standard V_{TH} NMOS, the threshold voltage does not exhibit significant degradation for longer channel lengths (L), in either linear or saturation operation, at all temperatures. Changes become evident as L becomes shorter, showing the effects of charge trapping in the spacer oxides [20, 18, 11] with temperature playing a significant role in exaggerating the phenomenon, namely the initial lowering of the V_{TH} with TID, followed by a marked increase, as can be observed in fig. 11c. On the contrary, PMOS devices exhibit a monotonical increase in $|V_{TH}|$ in direct relation to TID, for all device lengths with the effect being amplified by temperature. Interestingly whereas in NMOS linear region operation seems more affected, in PMOS practically the same degradation is observed in both linear and saturation operation, as evidenced by figs 11d,e,f. While NMOS devices show a larger increase in V_{TH} for the shortest L, for devices of the same L, at the same

TID levels, PMOS transistors show in all cases a much larger increase in V_{TH}.

3.3.2 Threshold Voltage Length Scaling at 0°C, LVT, SVT, HVT devices



(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

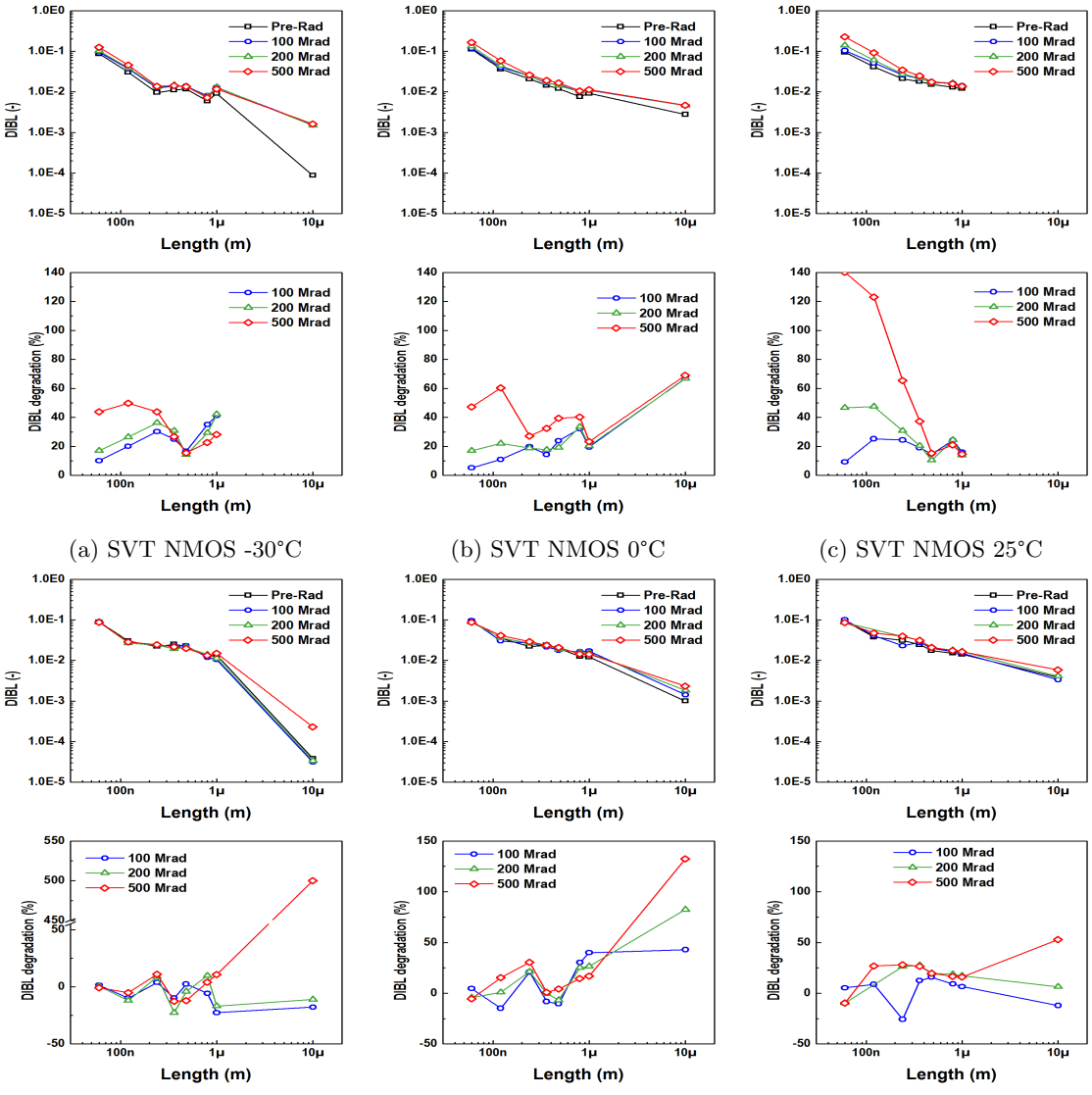
(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 12: V_{TH} and degradation, scaling vs channel Length at 0°C for N and P type devices of low, standard and high threshold voltage

As can be expected from the doping concentrations used to modify the threshold voltage, in all cases, with exceptions being the high V_{TH} NMOS in linear operation at the highest TID level as well as their PMOS counterparts, lower dopant concentration leads to more sensitive devices. This is more than obvious in figs 12a,d with both N and P devices ending up with a more than two hundred mV increase in V_{TH} for the shortest devices in linear mode. Saturation V_{TH} is not as severely impacted. This has the interesting effect of increasing the V_{TH} of the shortest low V_{TH} devices to approximately the same level as the high V_{TH} ones for both N and P types for linear operation. Regarding the peculiarity of the HVT transistors being more affected than their SVT counterparts, we can only assume that this is an artifact of our single device analysis. If multiple

devices were analysed per type, we would normally expect high V_{TH} devices to show the greatest robustness with regards to TID degradation.

3.3.3 DIBL Factor Length Scaling, SVT, at -30,0,25 °C



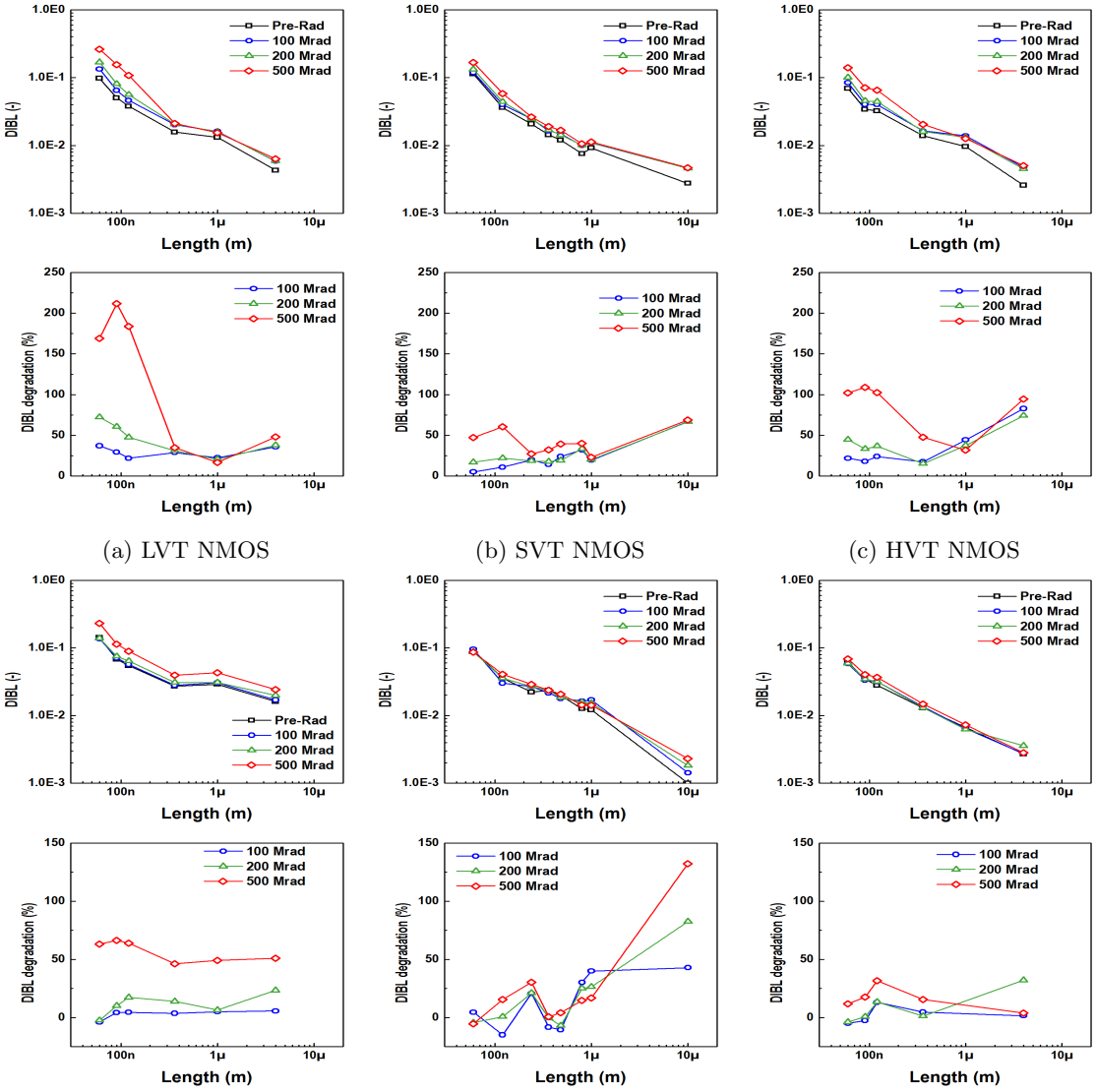
(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 13: DIBL and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

Following the previous observations on V_{TH} it is not surprising to see them reflected on the DIBL factor, where N type devices show a larger increase in DIBL with TID and temperature, inversely proportional to device L. P types show some weak dependency on temperature but since linear and saturation V_{TH} levels seemed to increase in tandem, their DIBL behaviour is much tamer. As the DIBL factor is very sensitive to the calculation of the threshold voltage, as P type devices show a seemingly random ±25% fluctuation with negligible TID dependence, it could be argued that the actual DIBL fluctuation is close to zero.

3.3.4 DIBL Factor Length Scaling at 0°C, LVT, SVT, HVT devices



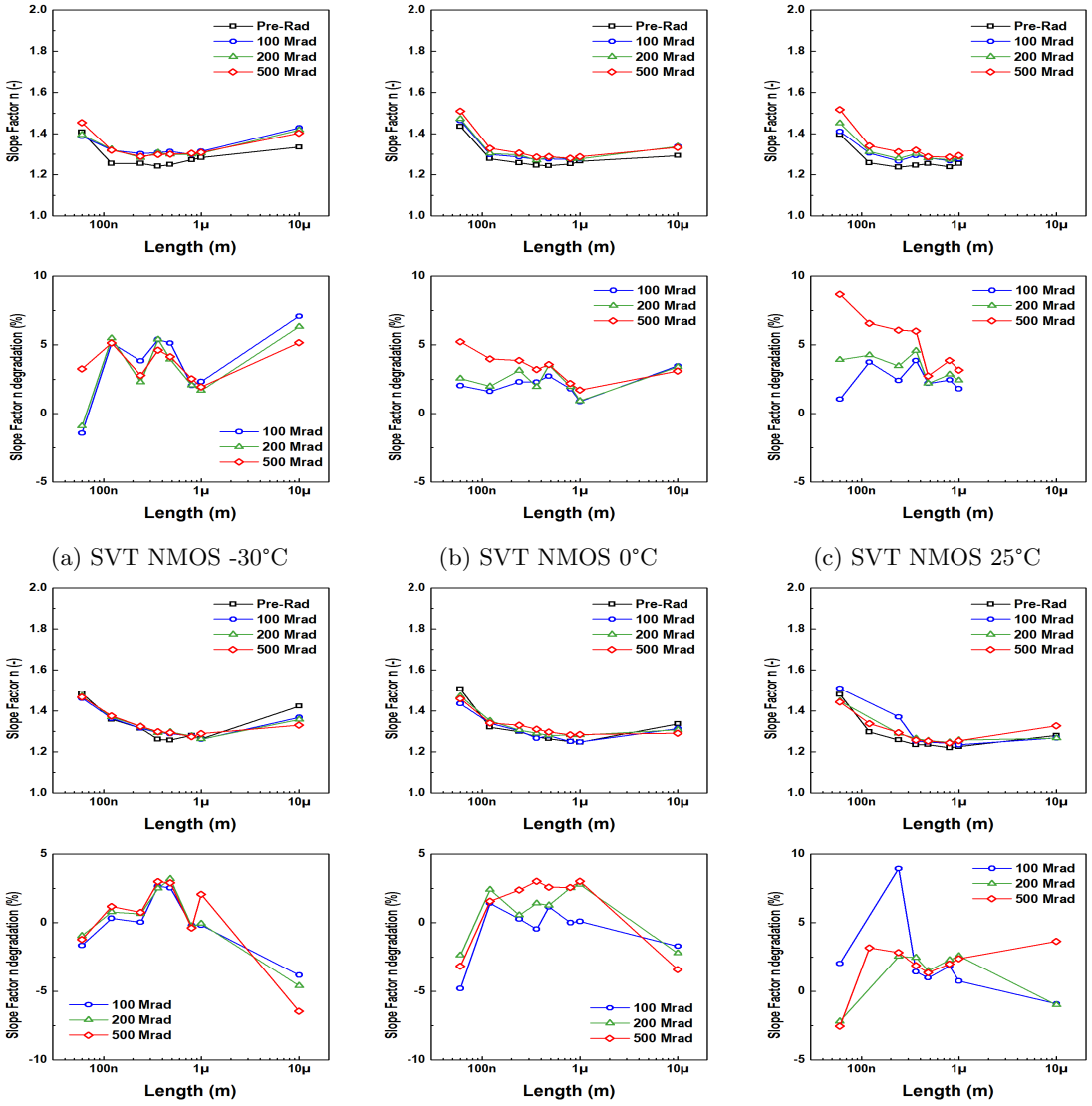
(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 14: DIBL and relative degradation, scaling vs channel Length at 0°C for N and P type devices of low, standard and high threshold voltage

As for the different device types, low V_{TH} devices again show greater sensitivity to TID effects, with an unmistakable monotonous increase in P type devices, in contrast to their standard V_{TH} counterparts seen previously. Interestingly in their case, we do not observe any significant length dependence, as can be seen in fig. 14d. Again high V_{TH} NMOS show an unexpected greater degradation than standard V_{TH}, but this has already been attributed to the non-statistical nature of our analysis sample.

3.3.5 WI Slope Factor Length Scaling, SVT, at -30,0,25 °C



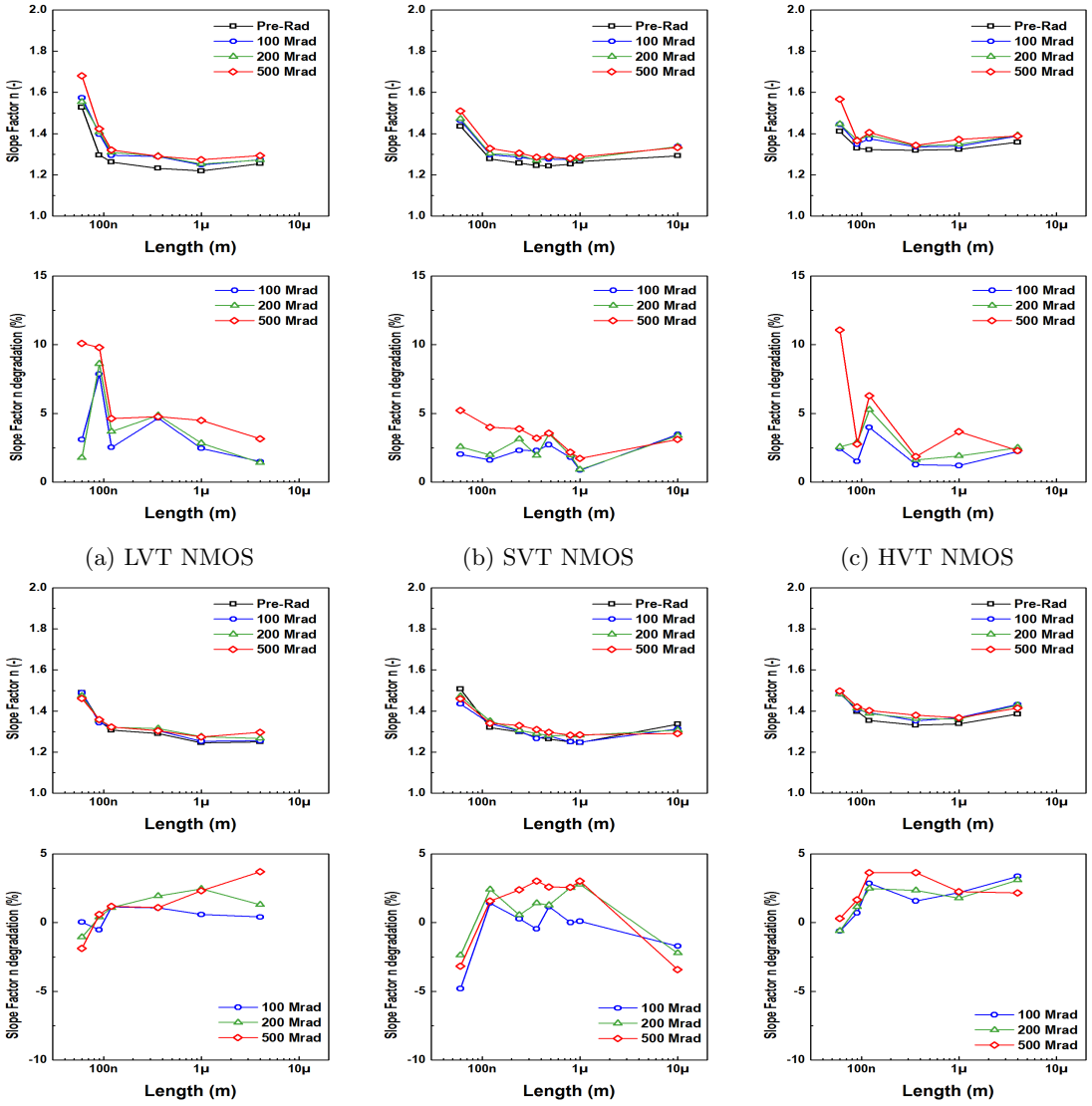
(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 15: Weak inversion slope factor and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

The saturation weak inversion slope factor shows a limited sensitivity to TID in wider devices, predominantly of N type. While P type transistors do not show almost any significant worsening with TID, being bounded between ±5% with little dependence on temperature, N type transistors nearly always exhibit an increase in their slope factor, which becomes more pronounced with temperature. Starting from a value of approximately 1.4 in pre-irradiation measurements, it increases to around 1.55 for the shortest devices after a dose of 500Mrad, a small increase, on the order of 10%, considering the severity of the dose but a significant worsening of device performance overall. Interestingly, this increase points out that slope factor degradation is not a component of the V_{TH} degradation (measured in the moderate inversion region) shown before, as an increase in n would result in a lower V_{TH}, if a constant current criterion was used, as is the case in this work.

3.3.6 WI Slope Factor Length Scaling at 0°C, LVT, SVT, HVT devices



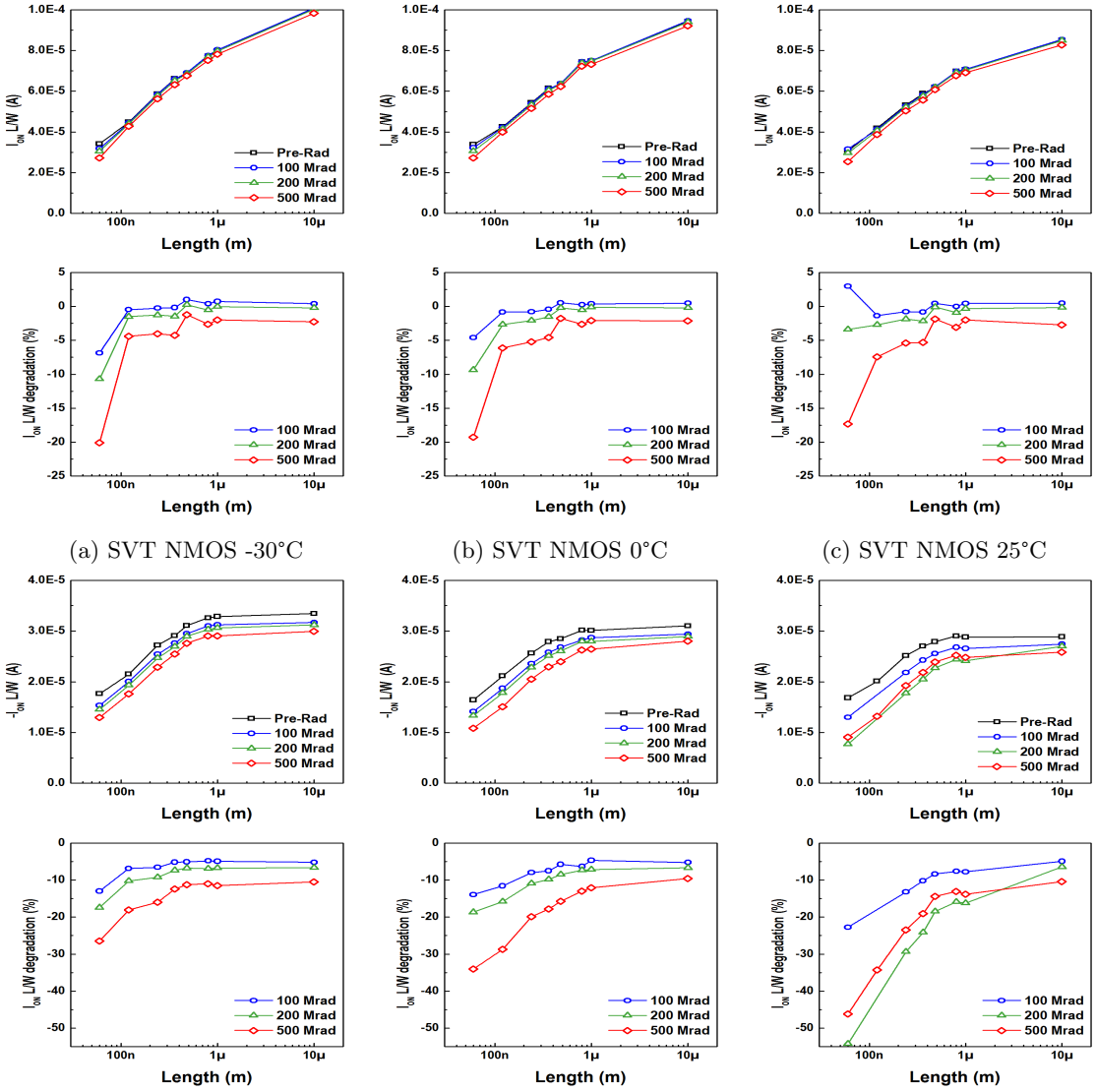
(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 16: Weak inversion slope factor and relative degradation, scaling vs channel Length at 0°C for N and P type devices of low, standard and high threshold voltage

Again PMOS show a better overall response. Not only all low, standard and high V_{TH} devices start at a comparable n, they exhibit a similar response to TID. Regarding NMOS on the contrary, differences between the three types are evident from pre-irradiation conditions. While high V_{TH} longer devices have a worse n than standard V_{TH} and those in turn are worse than low V_{TH}, this trend is rapidly overturned for the shortest devices, with low V_{TH} transistors starting out with an n above 1.5 and ending up with an n of 1.7 (fig. 16a), a significantly bad outcome. Interestingly for most devices we observe a degradation on the order of 5% in all three types with only the shortest ones approaching a 10% increase.

3.3.7 On-Current Length Scaling, SVT, at -30,0,25 °C



(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

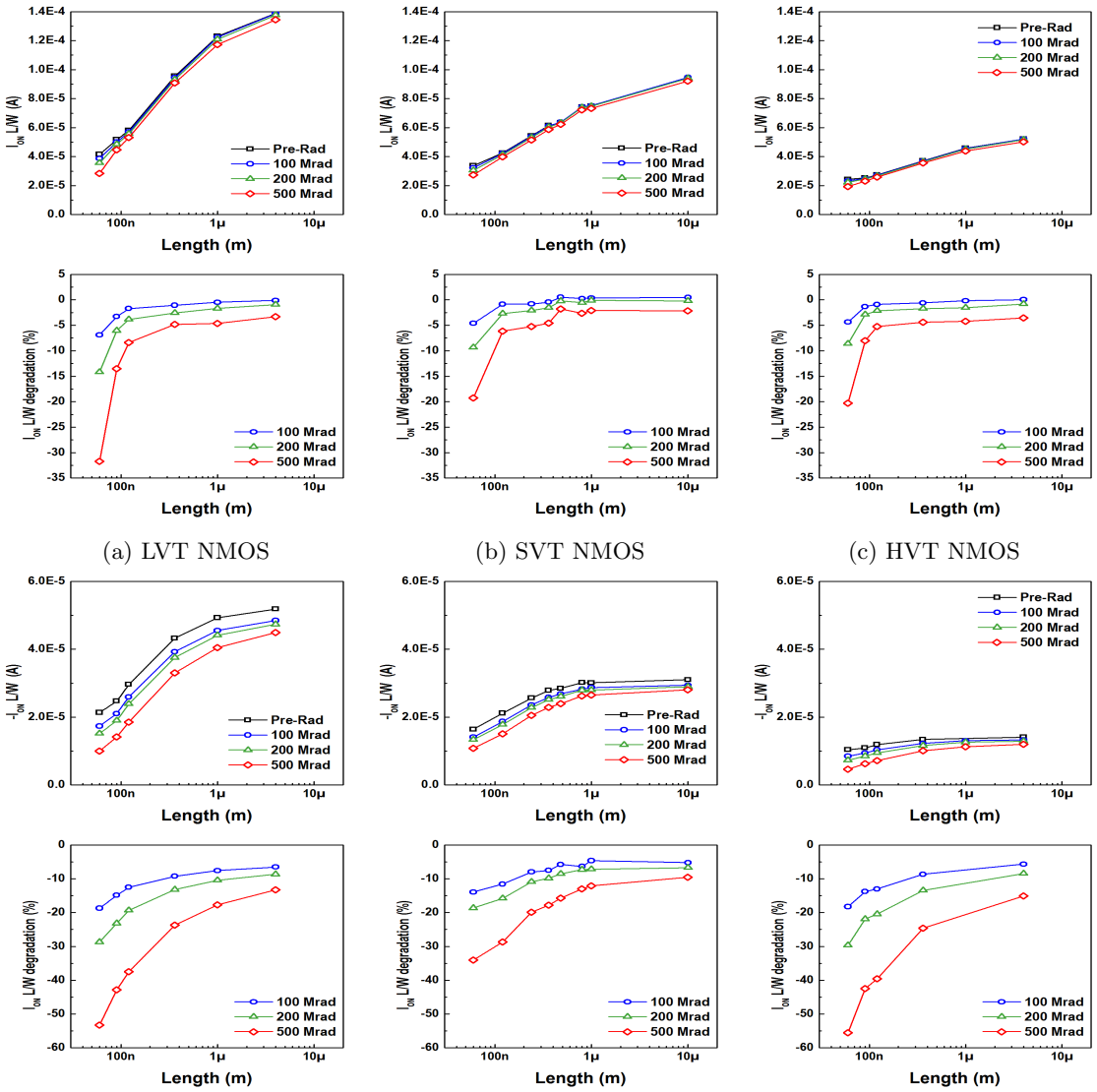
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 17: On-state current normalised by $\frac{L}{W}$ and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

When viewing the normalised on-state current, the results are more clear-cut, though no less interesting. We can immediately see that the current capabilities of all devices irrespective of type, length or temperature are impaired. However we can also note that NMOS not only are less hampered overall but also with a different sensitivity to TID. Specifically, NMOS show only minor current reduction for most device lengths up to 200Mrad with effects being prominent only for the highest dose, with the exception of the shortest devices, which begin degrading immediately and end up operating at 80% of their initial capability. Also worthy of note is the fact that where the effect is most prominent (i.e. 25°C, shortest device), we initially observe an initial increase in current, as the interplay between the fixed positive trapped charge and the more mobile negative interface traps [20, 18], while for all other geometries at 100Mrad there is zero to almost positive change, further indicating the progression of the phenomenon. PMOS degradation on the other hand is strongly dependent on both TID and temperature, with the TID affected devices outputting

close to half their original current. Overall we can observe that temperature not only plays a role on the total device degradation but also on the rate at which different length devices are affected. This can be seen with NMOS devices but becomes even clearer with PMOS, where for -30°C the lines are approximately straight and successively get a more pronounced slope as temperature increases. Finally we must mention the unexpected result that 200Mrad PMOS at 25°C exhibit a worse degradation than at 500Mrad. This cannot be explained at the time this work is written, nor is it accounted for in the bibliography we consulted.

3.3.8 On-Current Length Scaling at 0°C, LVT, SVT, HVT devices



(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

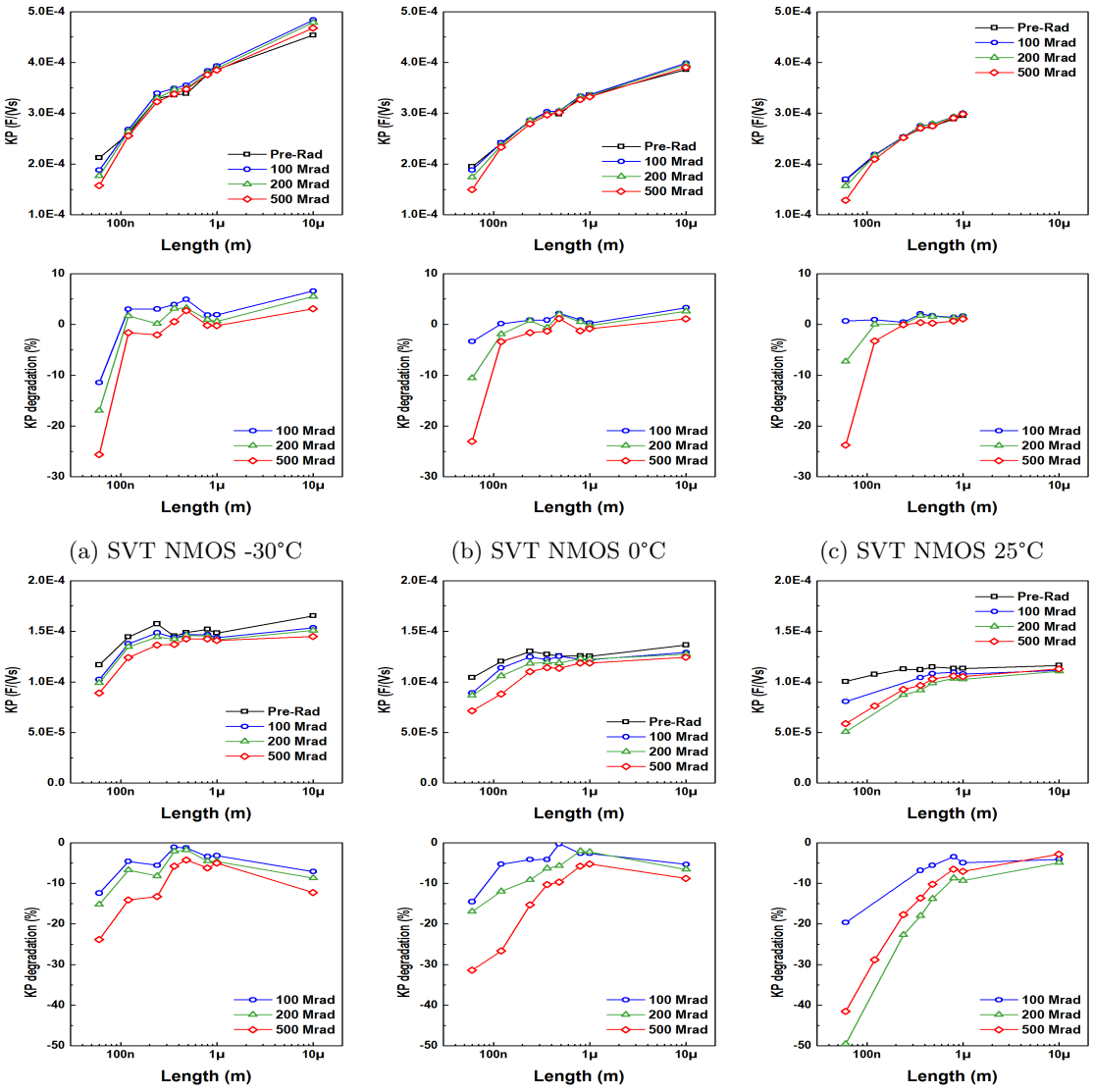
(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 18: On-state current normalised by $\frac{L}{W}$ and relative degradation, scaling vs channel Length at 0°C for N and P type devices of low, standard and high threshold voltage

The trend of low V_{TH} devices being more susceptible to TID effects continues with the on current with the surprising results however, of high V_{TH} devices. In the case of NMOS devices we notice that the degradation scaling is very similar with the standard V_{TH} ones, while for PMOS

more perplexingly, high V_{TH} devices have a greatly exaggerated degradation, more akin to the low V_{TH} ones. In any case, PMOS devices are again observed to suffer a great reduction in their current drive capabilities, far exceeding their equivalently sized NMOS devices.

3.3.9 KP Length Scaling, SVT, at -30,0,25 °C



(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

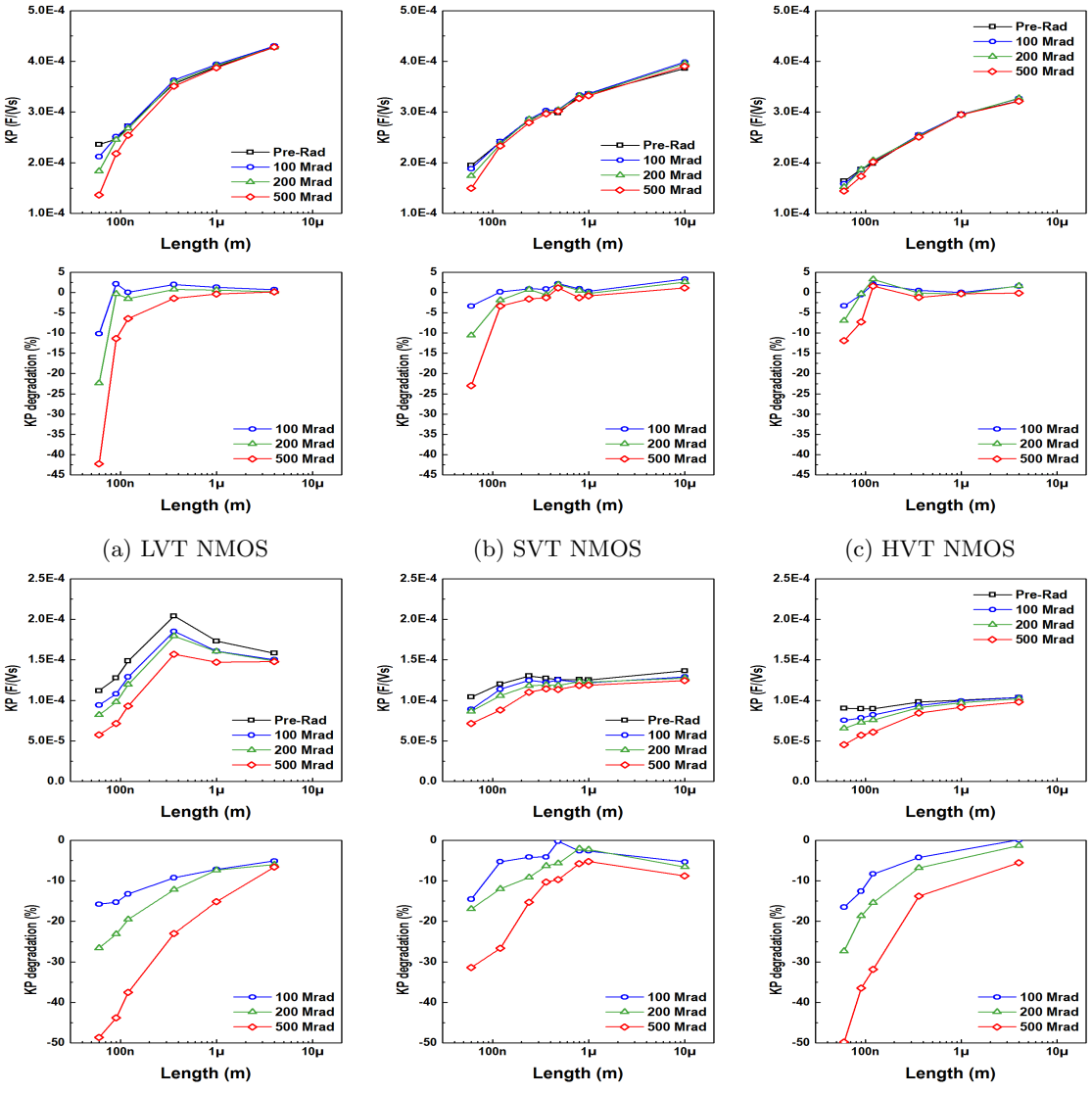
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 19: Transconductance factor ($KP = \mu * C'_{OX}$) and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

Mobility results help paint a larger picture when correlated with the corresponding on-current plots presented previously. While on-current tends to a near zero degradation for most N type devices at 100Mrad with a subsequent increase, here mobility is shown to increase even at 500Mrad for the longest devices. This is also mostly true for P types, with mobility being relatively less degraded than the current drive. This changes for the shortest devices where for N types mobility has a larger degradation and for P types it is equal to the on-current degradation. This points to the conclusion that the recorded drop in current capability is not a function of effective mobility

alone and that other other factors, such as the V_{TH} increase are at play. The inexplicable behaviour of 200Mrad degradation surpassing that of 500Mrad for 25°C is repeated here as well.

3.3.10 KP Length Scaling at 0°C, LVT, SVT, HVT devices



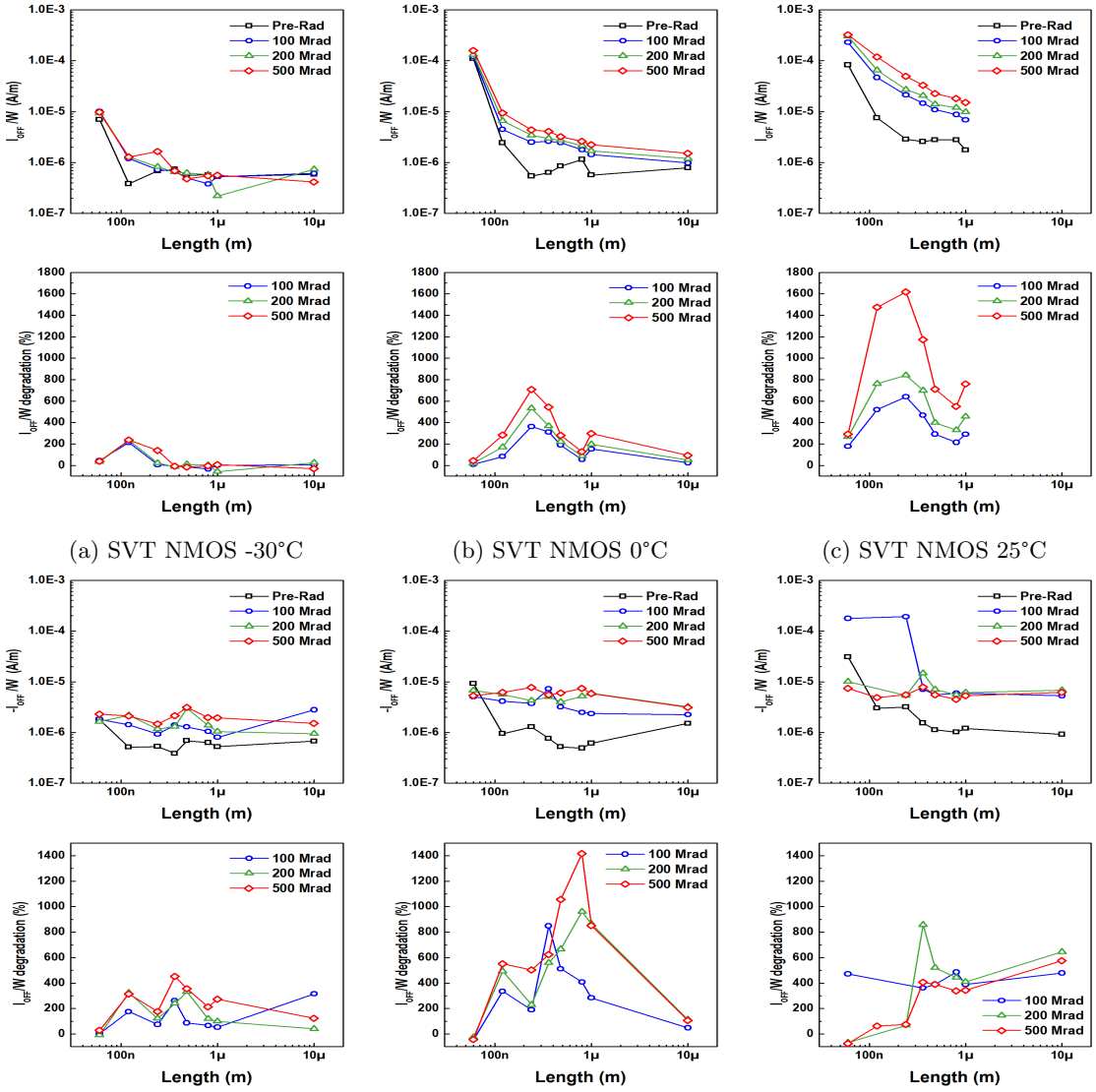
(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 20: Transconductance factor ($KP = \mu * C'_{OX}$) and relative degradation, scaling vs channel Length at 0°C for N and P type devices of low, standard and high threshold voltage

The same observations can be made for the three different transistor types. N types show a mostly positive or close to zero variation with a rapid drop towards the shorter channel length and P types are less degraded as well for all device lengths. As for the peculiarities we mentioned on the on-current degradation, while high V_{TH} P type transistors exhibit the same aggravated degradation as the low V_{TH} ones, in accordance to the on-current observations, here the high V_{TH} N type devices are less affected than the standard V_{TH} ones, as we would expect based on the dopant concentration differences used during fabrication.

3.3.11 Leakage Current Length Scaling, SVT, at -30,0,25 °C



(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

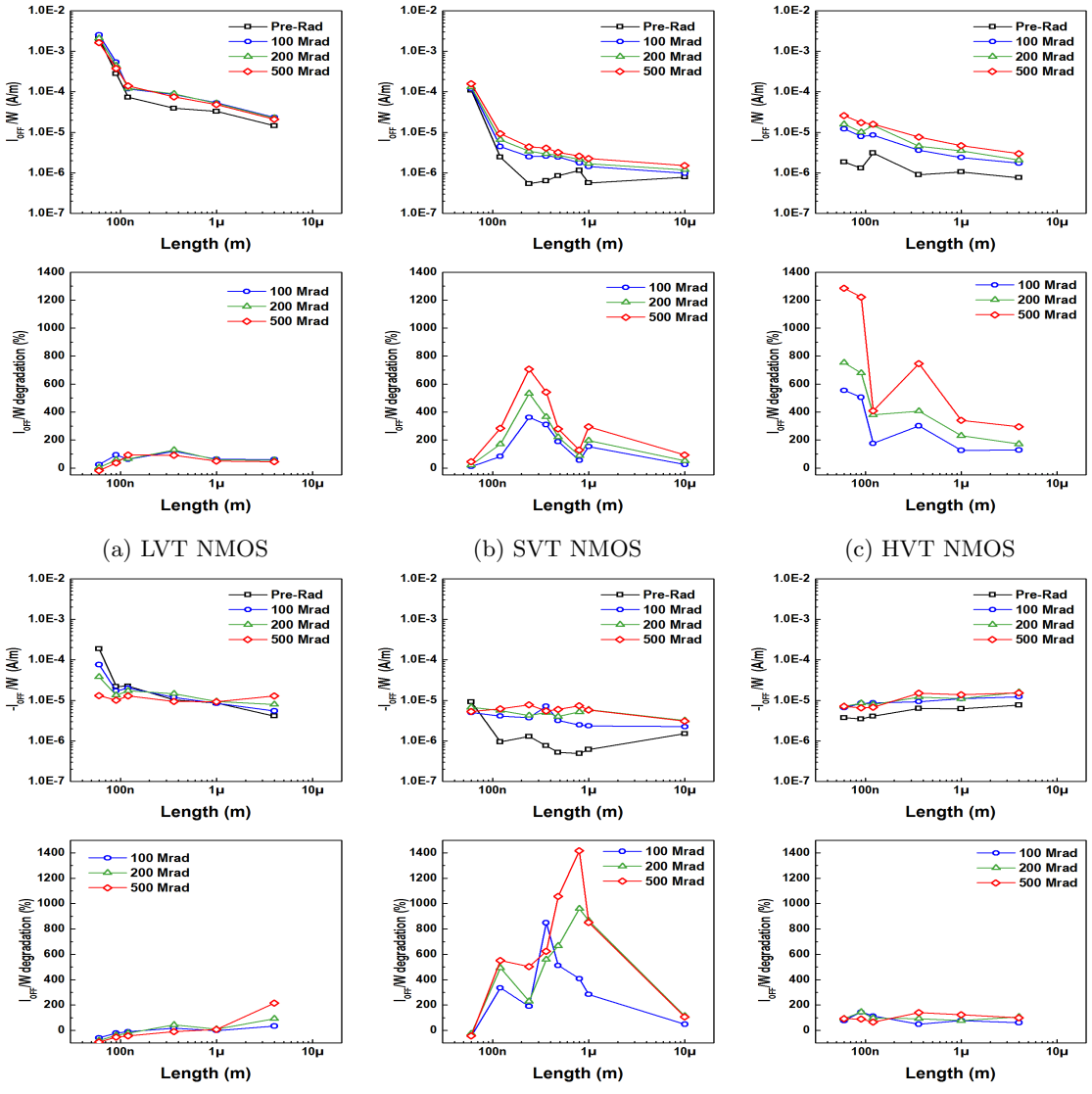
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 21: Leakage current normalised by $\frac{1}{W}$ and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

The increase in leakage currents associated with TID exposure is one of the main factors limiting the useful lifespan of devices in high TID experiments. While both N and P type devices suffer from TID exposure, this particular damage mechanism seems to be more problematic for N type devices. While pre irradiation base leakage levels are known to increase with temperature, it is also shown here that the degradation rate and thus also the total leakage current increase is strongly temperature dependant. Specifically in figs 21a,b,c this progression is evident, with degradation at -30°C being close to negligible, becoming 6 to 8 times for 0°C and reaching 10 to 16 times for 25°C experiments (always after the maximum dose). It is noteworthy that the maximum in the relative degradation curves is not observed at the shortest channel length devices but rather in more intermediate lengths. PMOS devices have a milder response, without a very pronounced dependence on temperature or device L. The final leakage levels are similar at all three temperatures across the whole L range. Of note is the observation that while the pre irradiation

leakage is comparable, the relative degradation seems worse at 0°C, highlighting again the difficulty in interpreting patterns due to the analysis being based on a single array per temperature point.

3.3.12 Leakage Current Length Scaling at 0°C, LVT, SVT, HVT devices



(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

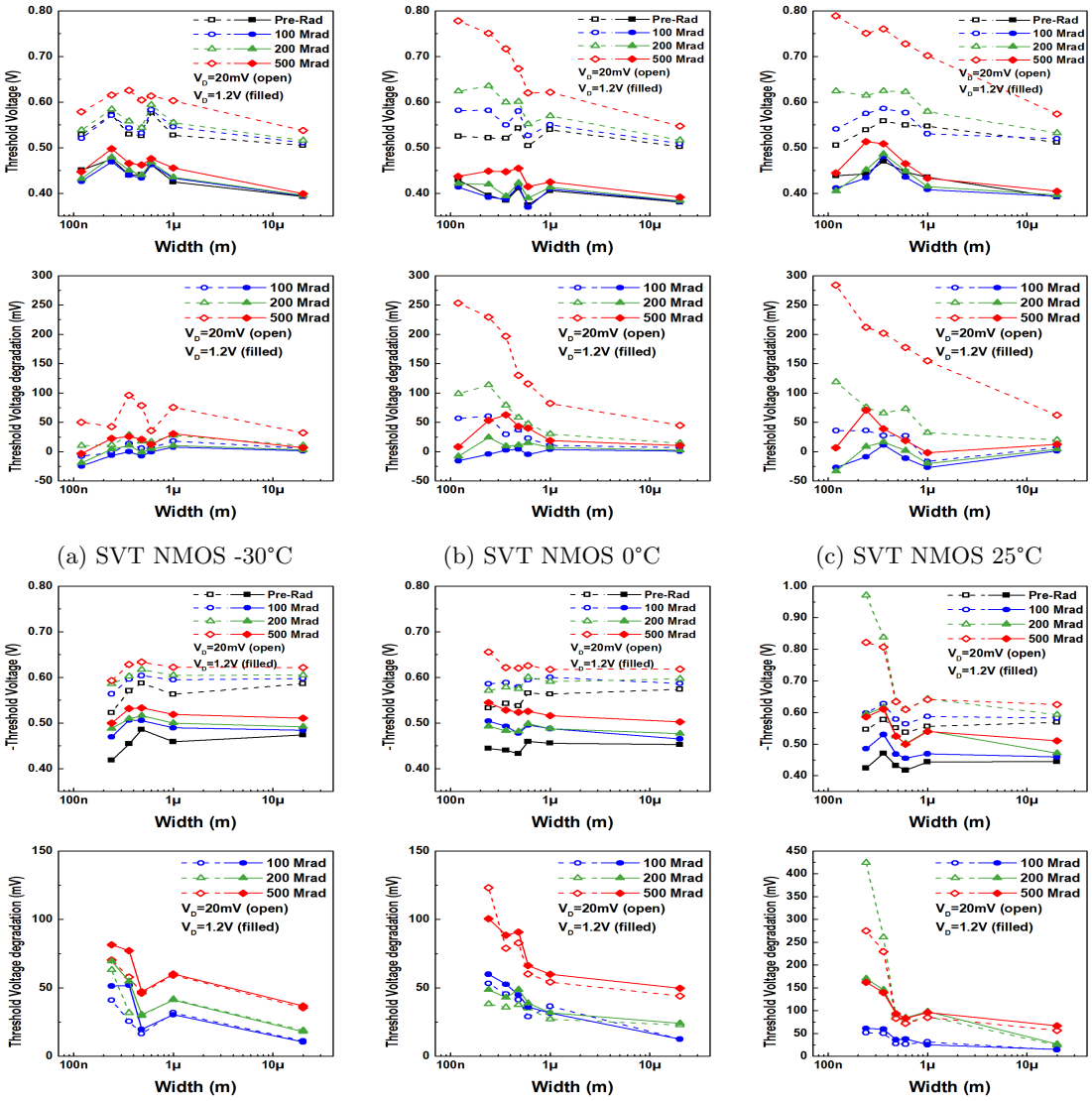
Figure 22: Leakage current normalised by $\frac{1}{W}$ and relative degradation, scaling vs channel Length at 0°C for N and P type devices of low, standard and high threshold voltage

Moving on to the three different types of devices available, the results are yet again difficult to interpret. While, as expected, low V_{TH} NMOS have an elevated initial leakage level, their sensitivity to TID is almost negligible, with the inverse being true for high V_{TH} ones, which show maximum sensitivity, reversing the notion of high V_{TH} devices being hardier in such experiments. For PMOS our observations are again puzzling. Low V_{TH} transistors have the highest initial leakage as well but their response to TID shows a counter-intuitive decrease in leakage current for the shortest device lengths, in contrast with the increase recorded in longer devices. Moreover, high V_{TH} transistors show non-zero but still very low sensitivity, in stark contrast to their NMOS

counterparts. Standard V_{TH} devices have the highest degradation, however as this dataset is already considered suspect, after the comparisons between figs 21d,e,f this might be an example of an overly damaged array that should not be considered typical for the phenomenon.

3.4 Width Scaling, Length=60nm

3.4.1 Threshold Voltage Width Scaling, SVT, at -30,0,25°C



(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

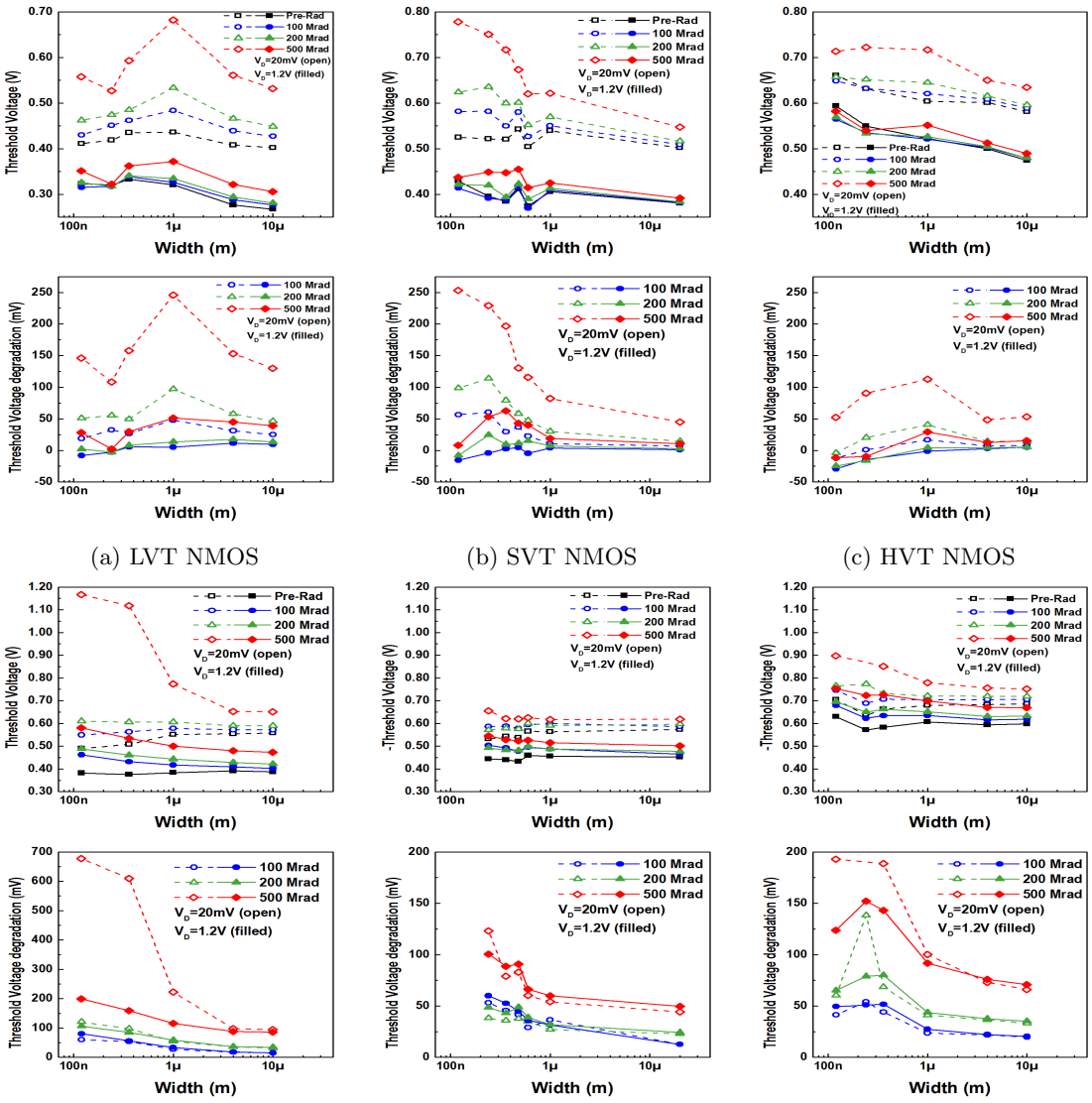
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 23: V_{TH} and degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

At this point of the analysis, short channel TID response is further compounded by the channel Width (W) becoming progressively narrower, leading to the most affected devices in this work. This is immediately obvious from the above presented graphs a,b,c showcasing a direct relationship between the damage and the total dose, which exhibits also a direct dependence on temperature and an inverse dependence on W. These effects, while observable in saturation operation, are more clear in linear operation, with the worst cases presented for the 25°C irradiation, where short and wide NMOS see an increase of 200mV in their V_{TH}, with that increase becoming 400mV for the short and narrow device. In figs 11a,b,c we had pointed out the relative insensitivity of the saturation V_{TH} to TID in all but the shortest devices. Here we are examining these short devices and see that this (relatively) low sensitivity is more or less constant for all device widths, in stark

contrast to their excessive sensitivity in linear mode. On the other hand PMOS do not exhibit any greater sensitivity in linear mode or insensitivity in saturation; in fact, with the exception of two devices, we can see that linear and saturation V_{TH} operation is practically equally impacted by TID, with temperature and W having the same qualitative relationship as before.

3.4.2 Threshold Voltage Width Scaling at 0°C, LVT, SVT, HVT devices



(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

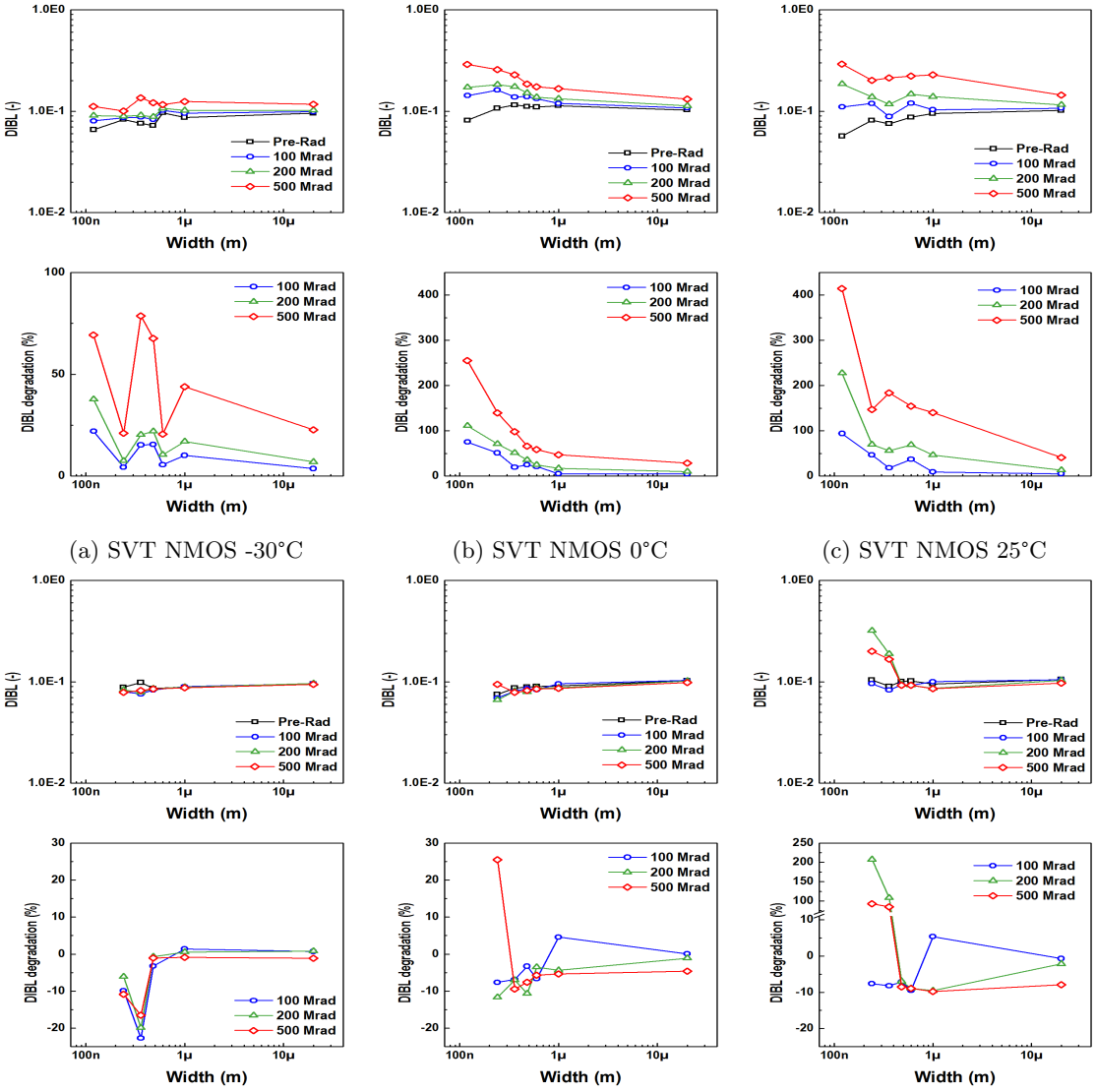
(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 24: V_{TH} and degradation, scaling vs channel Length at 0°C for N and P type devices of low, standard and high threshold voltage

High V_{TH} NMOS again show more resilience, however, interestingly low V_{TH} devices show comparable overall damage with those of standard V_{TH} while their maximum degradation peaks at intermediate device widths rather than narrower. The behaviour of similar degradation between linear and saturation observed with standard V_{TH} PMOS devices can also be seen repeated here at lower TID levels, with notable divergence though occurring at the highest TID in narrow devices for high and low V_{TH} devices but not for standard V_{TH} ones. This is not so easy to interpret; while

low V_{TH} are more than three times more affected than standard V_{TH}, high V_{TH} are also noticeably more affected as well, perhaps indicating that in this case standard V_{TH} devices happened to be unusually resilient. This is contrasted though by our previous observations in figs 23d,e,f where three independent arrays exhibited similar degradation thus indicating that the specific high V_{TH} array studied perhaps happened to be *less* resilient.

3.4.3 DIBL Factor Width Scaling, SVT, at -30,0,25°C



(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

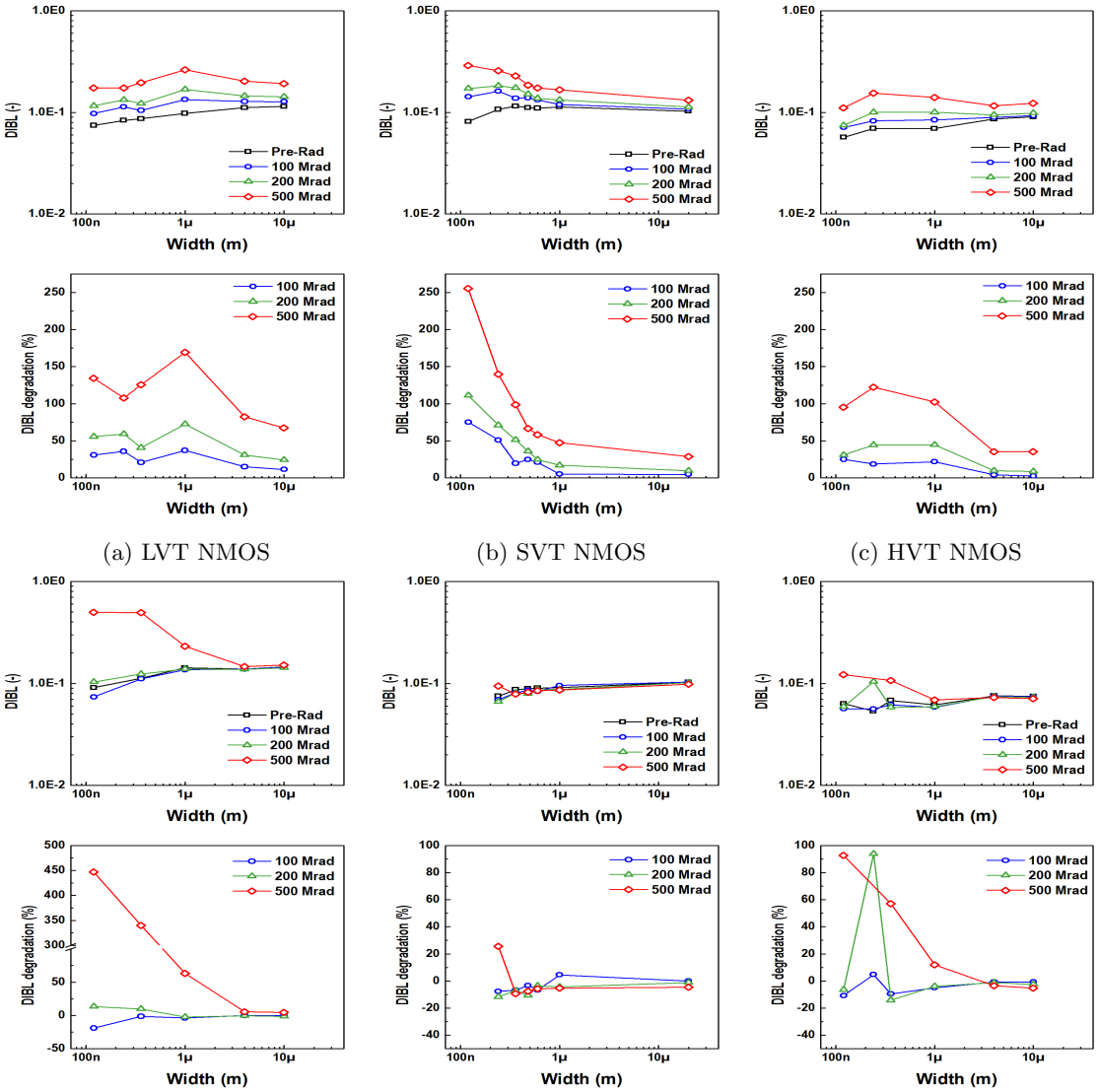
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 25: DIBL and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

As before, our observations on DIBL come as a direct consequence of the observations made on the V_{TH} response. As such, due to the large increase in linear mode V_{TH} in NMOS devices, we expect to see an analogous behaviour in DIBL, which is corroborated by the figs 25a,b,c above. In direct relation to the V_{TH} plots, we again see that the 25°C irradiation shows the largest degradation, beginning from a doubling in wide devices and ending in a quadrupling of the DIBL

factor in the narrowest ones. Following that, we again affirm the temperature dependence, with progressively lower degradation at lower temperatures. In all cases we can also discern the width dependence of the phenomenon. PMOS devices on the contrary exhibit minimal to no degradation (with the exception of the narrowest devices at 25°C), however this comes as a result of the commensurate increase in the (absolute) threshold voltage between linear and saturation regime, instead of an overall limited TID response.

3.4.4 DIBL Factor Width Scaling at 0°C, LVT, SVT, HVT devices



(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

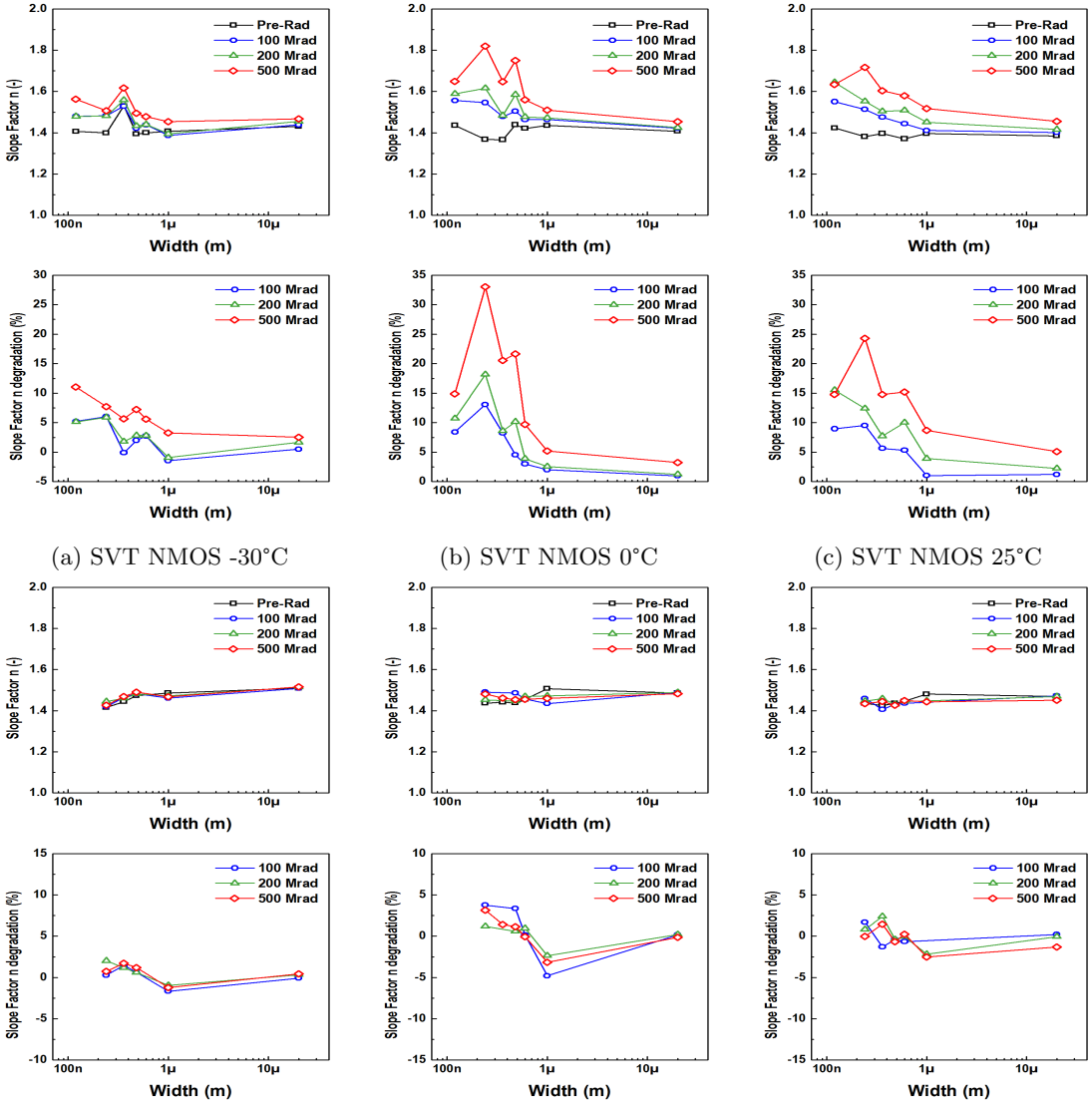
(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 26: DIBL and relative degradation, scaling vs channel Length at 0°C for N and P type devices of low, standard and high threshold voltage

For the different V_{TH} types, more or less the same can be said as with their V_{TH} analysis. For NMOS, again, the relative high V_{TH} insensitivity is observed along with the unexpected lower-than-expected degradation of the low V_{TH} devices which was highlighted in the corresponding subsection previously. For PMOS, as observed before, low V_{TH} devices show the expected higher

degradation and high V_{TH} show the unexpected higher than their standard V_{TH} counterparts degradation. So we can again remark that for low and high V_{TH} devices there exists a definite width dependence which is not recorded in standard V_{TH} ones.

3.4.5 WI Slope Factor Width Scaling, SVT, at -30,0,25$^{\circ}C$



(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

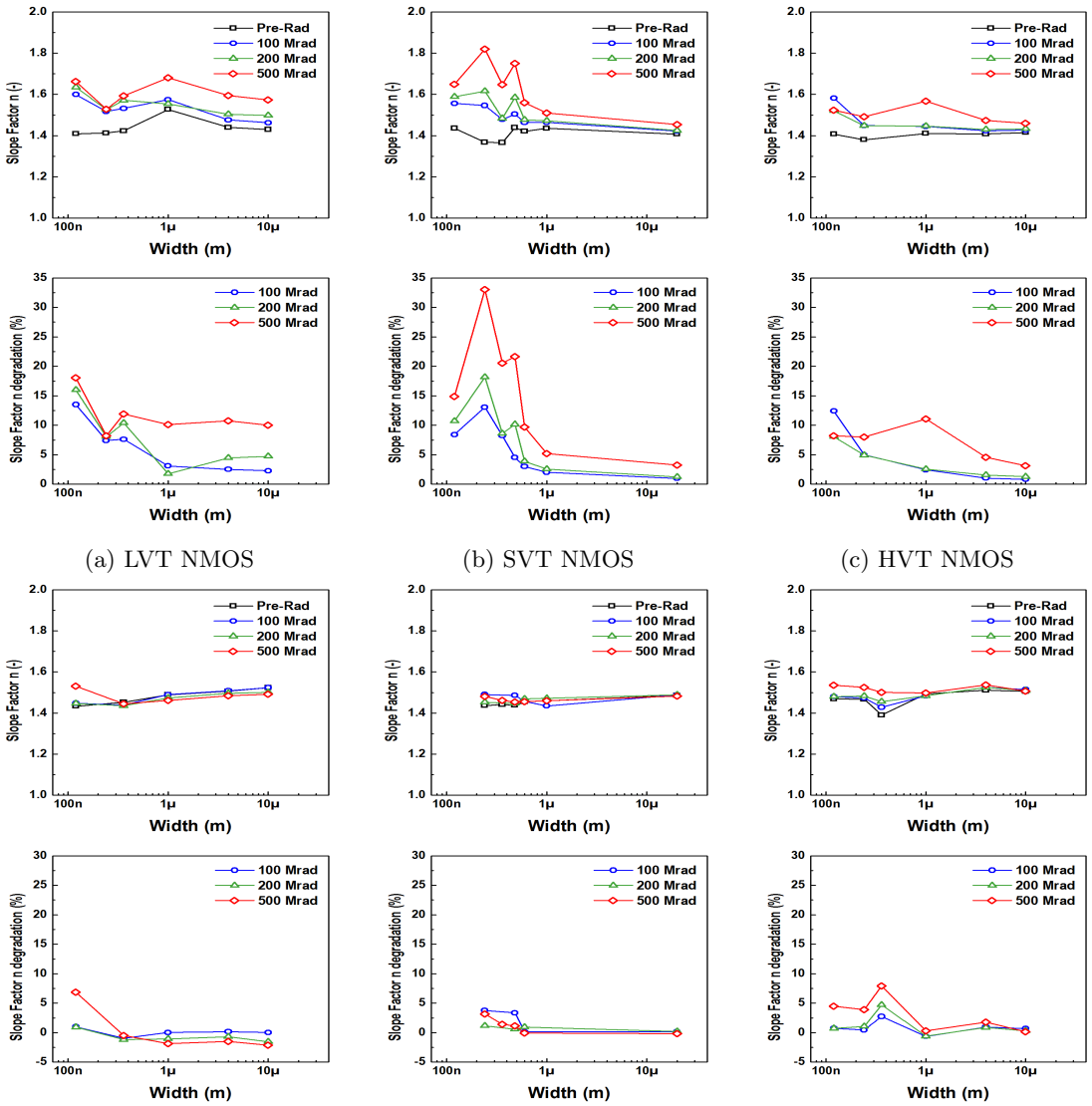
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 27: Weak inversion slope factor and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

As with the previous observations on the length scaling array, small to zero degradation is recorded in PMOS devices, pointing out a possible overall insensitivity of the weak inversion slope factor to TID effects, regardless of device geometry. On the other hand, just as we recorded a stronger impact on short NMOS devices, now that we examine the effects of narrower device widths we can also see that the n degradation in NMOS devices is strongly geometry dependent, with an inverse relationship to both device length and width. The dependence on temperature can also be observed, though narrow devices at 0°C seem to be somewhat more degraded than at 25°C.

The difference however is rather small and could be explained by the stochastic nature of the TID degradation on each device. What is noteworthy is the fact that these short and narrow devices emerge from the irradiation severely impaired, as their 1.6-1.8 slope factor value indicates.

3.4.6 WI Slope Factor Width Scaling at 0°C, LVT, SVT, HVT devices



(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

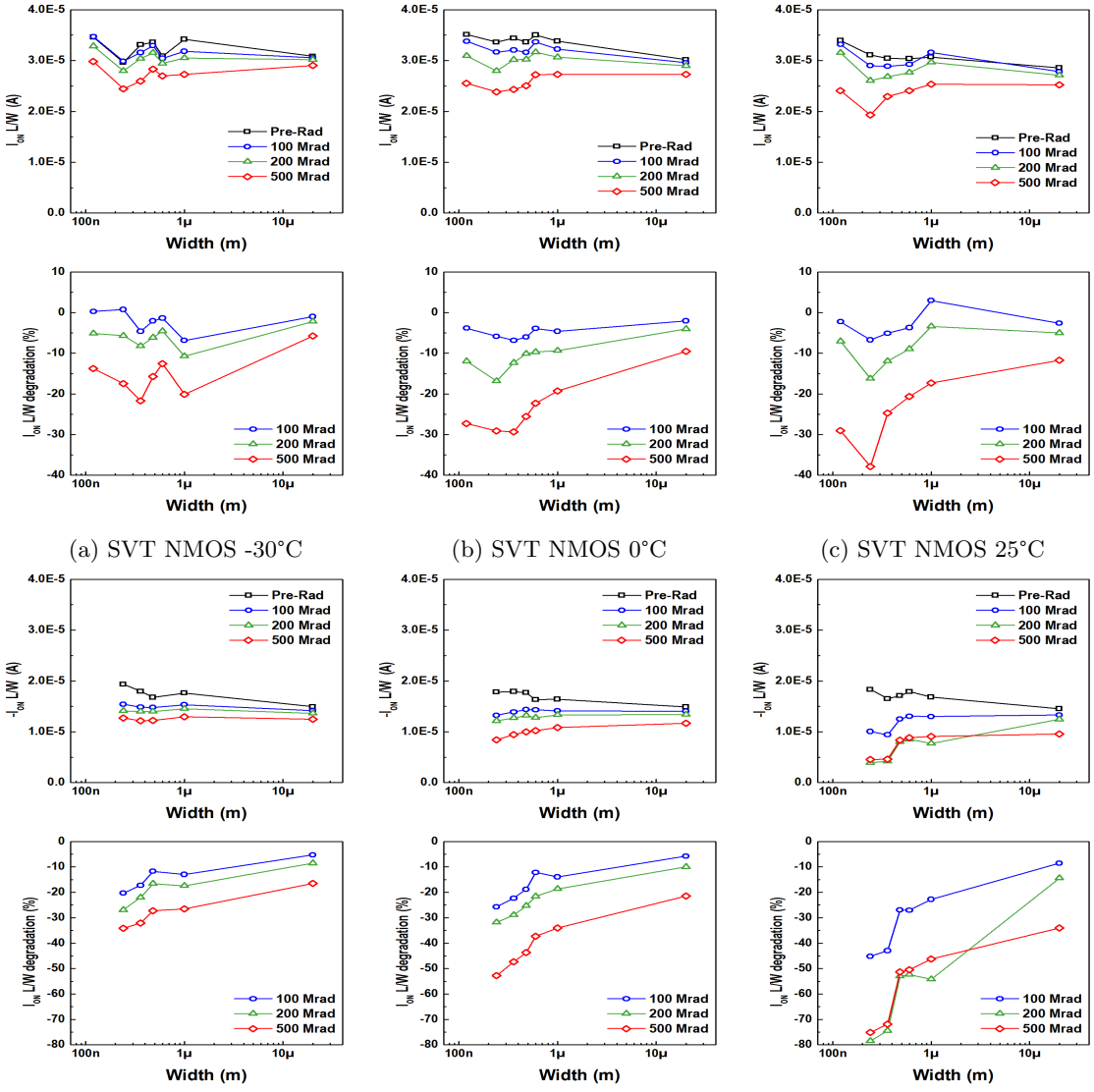
(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 28: Weak inversion slope factor and relative degradation, scaling vs channel Length at 0°C for N and P type devices of low, standard and high threshold voltage

When examining the response of the different V_{TH} NMOS types, what is immediately evident is that there appears to be little dependence on device width for the low V_{TH} transistors, in contrast to the standard and high V_{TH} ones. High V_{TH} devices exhibit an overall subdued response and interestingly standard V_{TH} NMOS show equal and even higher degradation than their low V_{TH} counterparts. This can probably be attributed to the specific array used for the 0°C standard V_{TH} experiment having suffered unexpectedly more, which is also supported by the figs 27b,c and the corresponding observations. PMOS devices exhibit the same overall insensitivity, with the

interesting yet small increase in the slope factor of the high V_{TH} narrowest devices.

3.4.7 On-Current Width Scaling, SVT, at -30,0,25$^{\circ}C$



(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

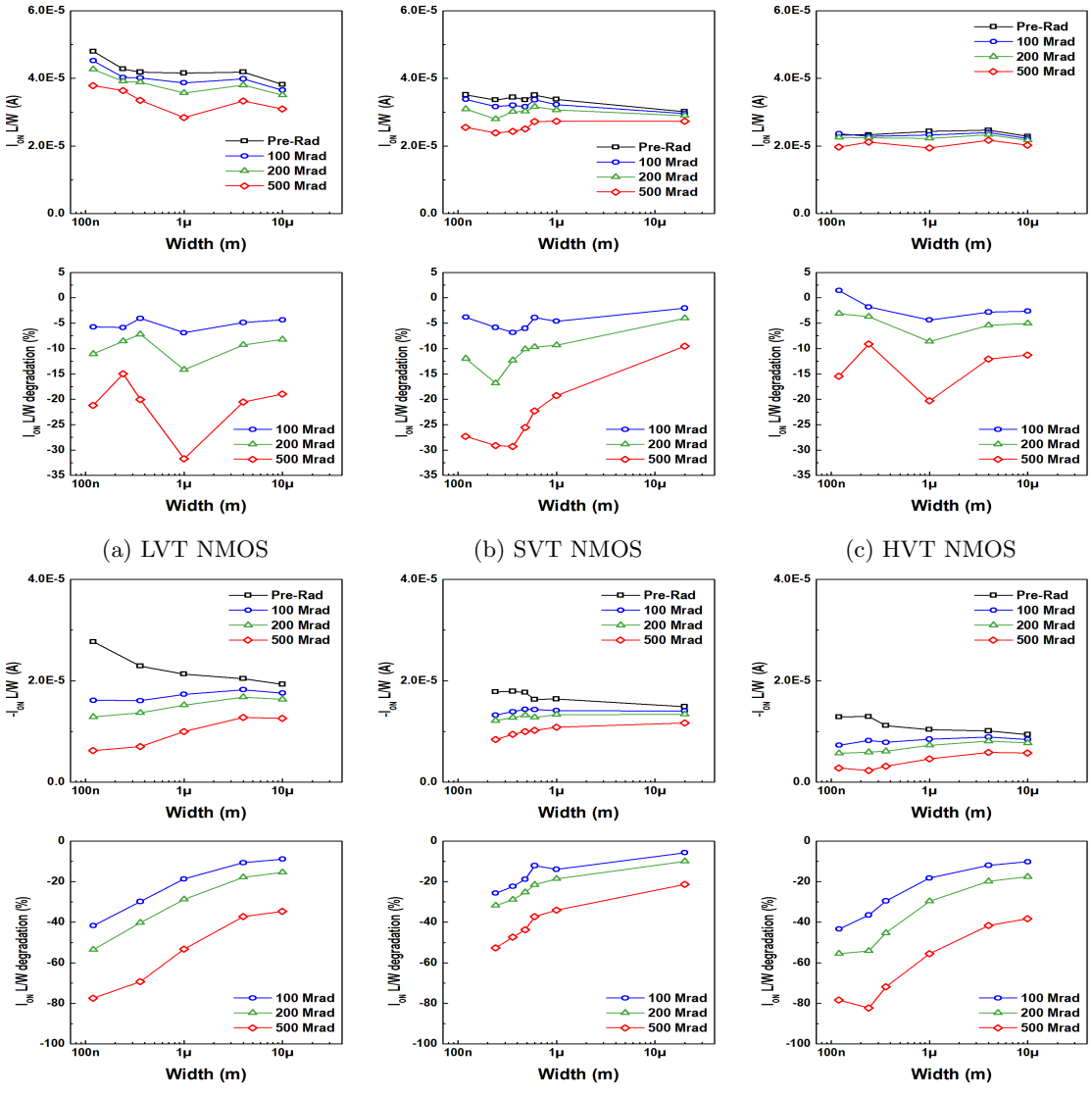
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 29: On-state current normalised by $\frac{L}{W}$ and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

Both N and P type devices are impaired by exposure to ionizing radiation, however it is clearly obvious from the above plots that P types are in all cases almost twice worse off than the equivalent N type ones. Starting from N types, we immediately observe the role that increased temperature plays in the scale of the phenomenon. Secondly we see the device width dependence which is however heavily linked to temperature. So, in the -30°C experiment the width dependence is less prominent than in 0°C and 25°C, with the latter dropping to a 60-70% of the initial current drive capability for the most affected devices. In P type devices the outcome is more dramatic, with current drive falling precipitously with increasing temperature and decreasing width. Even at intermediate temperatures, narrow transistors emerge at less than half of their initial capability,

with higher temperatures leaving the narrowest devices barely functional at a 20% of their initial current drive and the widest at a very impaired 50%.

3.4.8 On-Current Width Scaling at 0°C, LVT, SVT, HVT devices



(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

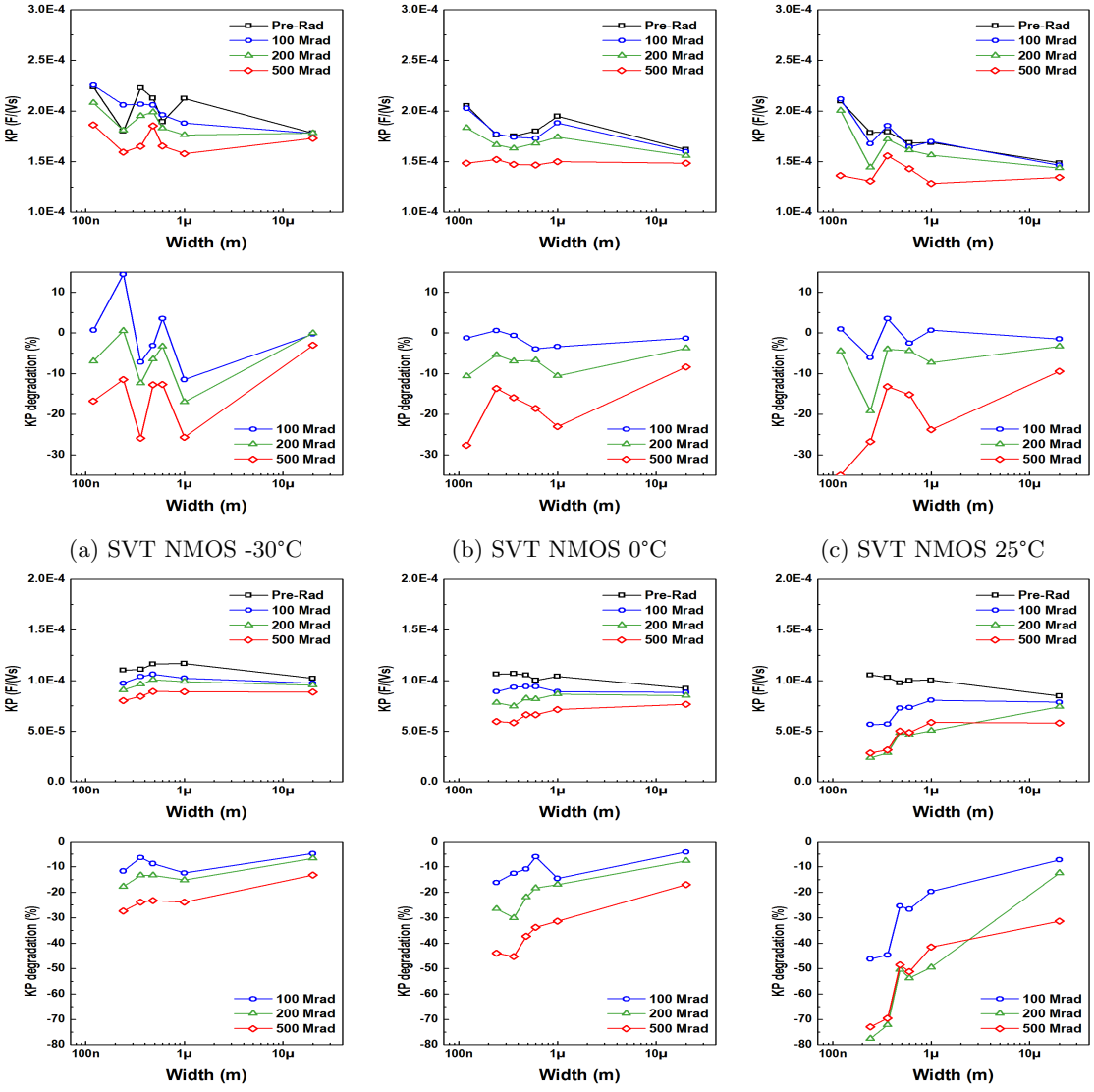
(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 30: On-state current normalised by $\frac{L}{W}$ and relative degradation, scaling vs channel Length at 0°C for N and P type devices of low, standard and high threshold voltage

The low and high V_{TH} NMOS transistors do not exhibit a very pronounced width-dependent degradation. Instead, with the exception of the $1\mu m$ device, all geometries seem to be almost equally impaired. As for the $1\mu m$ geometry, in both low and high V_{TH} cases, we see that it shows a greater susceptibility to TID than the other devices but this is an artifact of the irradiation experiments being carried out on different device arrays, with the $1\mu m$ device being part of the $W = 1\mu m$ length scaling array analysed in the previous sections of this work. While high V_{TH} transistors again prove more resilient, standard and low V_{TH} ones exhibit a very comparable degradation. As for the PMOS devices, the recurring result is one of extreme reduction in the

current capabilities of the devices. What can be arguably expected is that low V_{TH} devices are degraded to the point reached by their standard V_{TH} counterparts reach at higher temperatures. Unexpected, however is that high V_{TH} devices *also* exhibit s=the same relative degradation as the low V_{TH} ones, resulting in a worse outcome than the standard V_{TH} ones. This, coupled with their already low pre-irradiation current drive leaves these devices in a very compromised state.

3.4.9 KP Width Scaling, SVT, at -30,0,25°C



(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

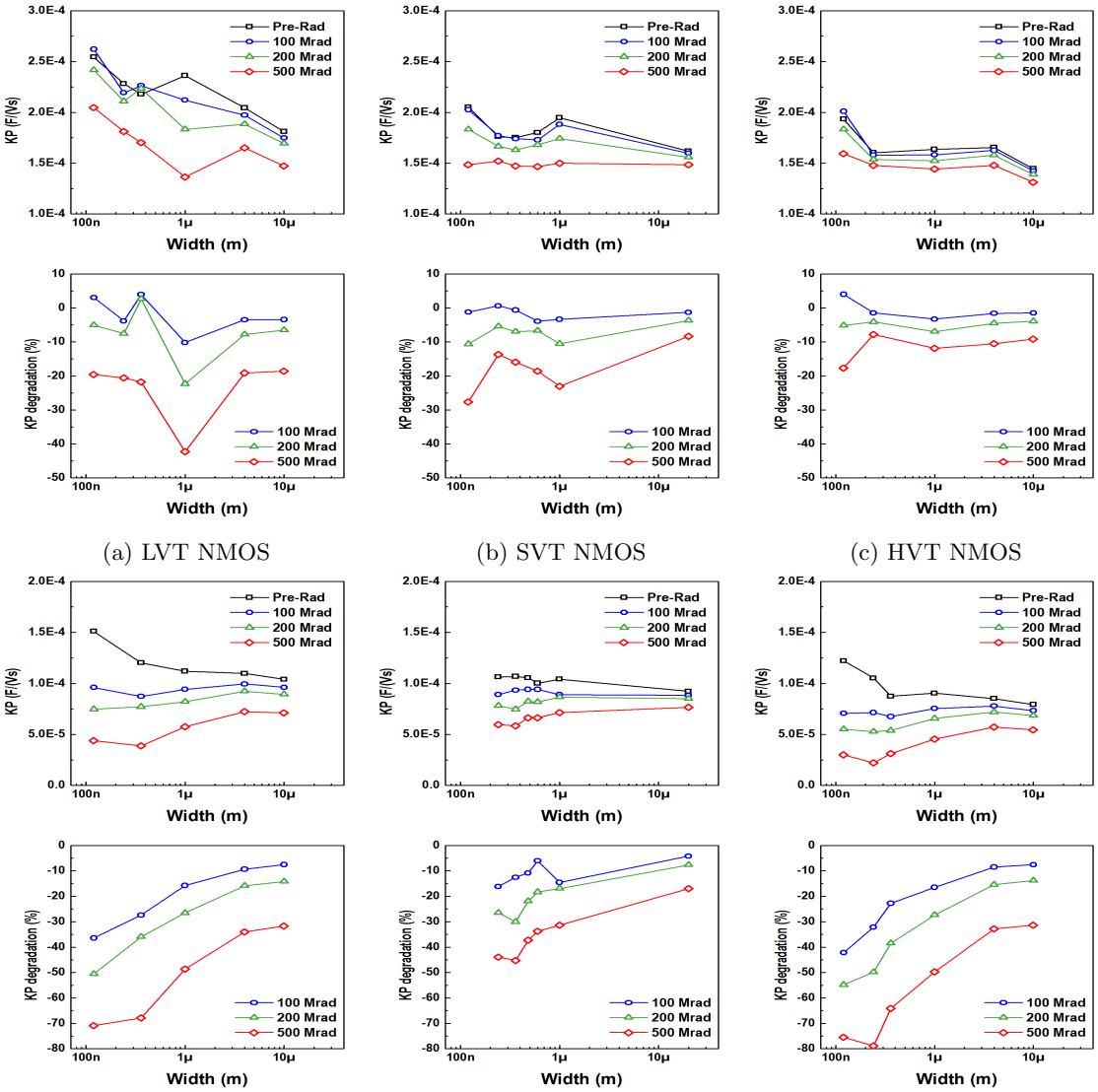
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 31: Transconductance factor ($KP = \mu * C'_{OX}$) and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

Comparing the KP plots with the normalised on-current presented previously we can observe certain parallel behaviours. In the length scaling array of wider devices we had highlighted that NMOS mobility seemed to differ from the I_{ON} response by first increasing with TID. While in some devices this is still true, in most NMOS transistors of this array, mobility degrades in tandem with the current, both qualitatively and quantitatively, with very similar percentages degradation

percentages being recorded between figs 29 & 31 a,b and c. The qualitative parallelism is also obvious for the PMOS devices, however KP degradation at -30°C and 0°C is noticeably more restrained than the equivalent I_{ON} drop. This indicates that the current drive decrease in PMOS is not only attributed to a reduced mobility but to more factors, most probable being the increase in V_{TH} (which was not observed to the same degree in similar NMOS geometries) as illustrated in figs 23d,e,f.

3.4.10 KP Width Scaling at 0°C, LVT, SVT, HVT devices



(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

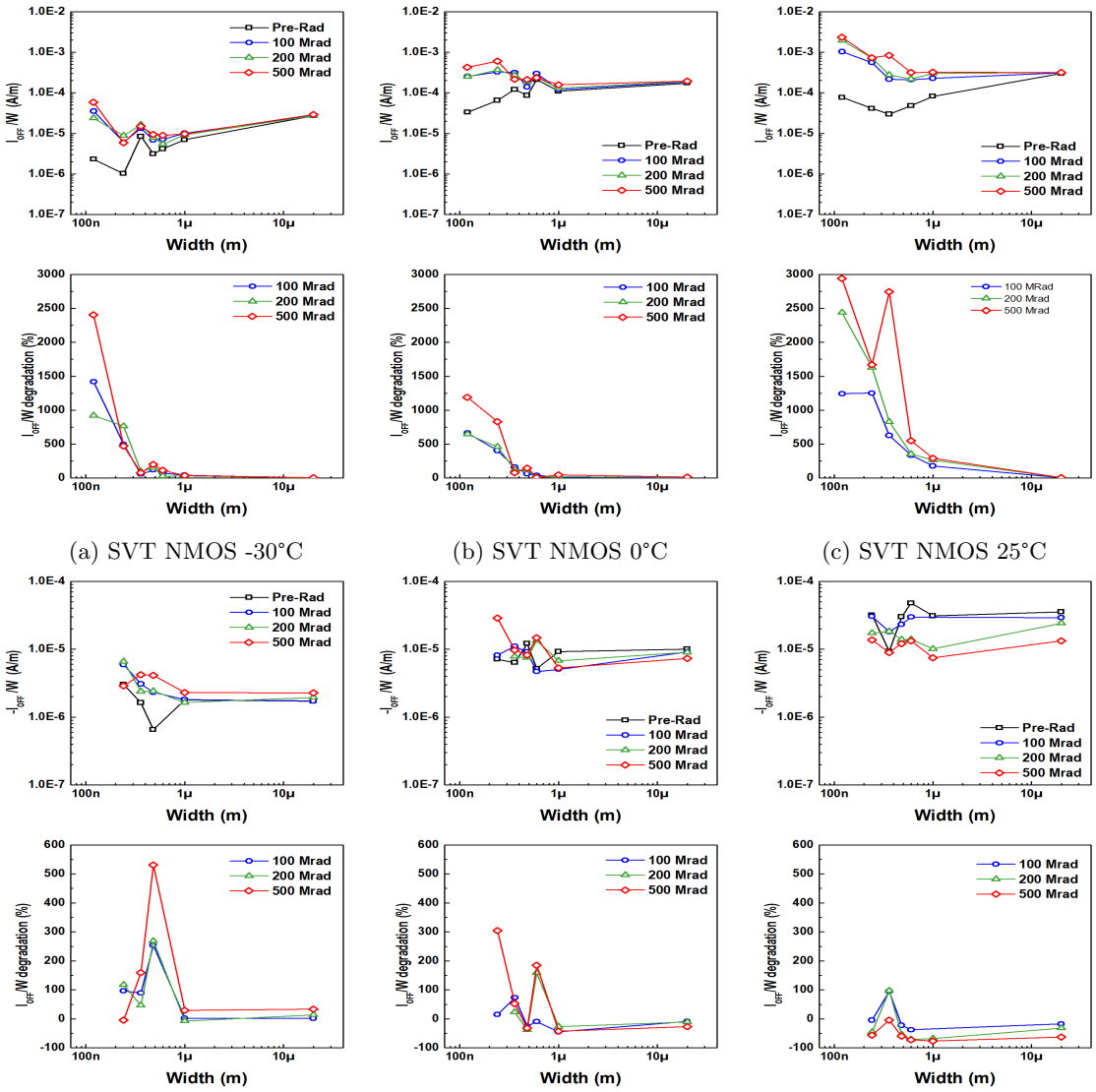
(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 32: Transconductance factor ($KP = \mu * C'_{OX}$) and relative degradation, scaling vs channel Length at 0°C for N and P type devices of low, standard and high threshold voltage

Initially we can highlight that the same observations made for the standard V_{TH} devices can be repeated for the low and high V_{TH} ones, of both N and P types. Namely the similarity of I_{ON} and KP degradation in NMOS and the lower KP degradation in PMOS. Afterwards though, we can also add that the interplay between the different pre-irradiation KP levels and the irradiation

sensitivity of the different types, leads to the interesting result; after a 500Mrad dose, most NMOS devices of all types end up with the same levels of effective mobility, as can be seen in figs 32 a,b,c in red. Most interesting is the high V_{TH} PMOS result, which exhibits very similar post-irradiation effective mobility but also more importantly, very similar radiation sensitivity. This mirrors our I_{ON} observations for these specific devices and cannot be readily explained by a dopant concentration argument. Again random defects or over-sensitivity of the specific array could be to blame for this counter-intuitive behaviour.

3.4.11 Leakage Current Width Scaling, SVT, at -30,0,25°C



(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

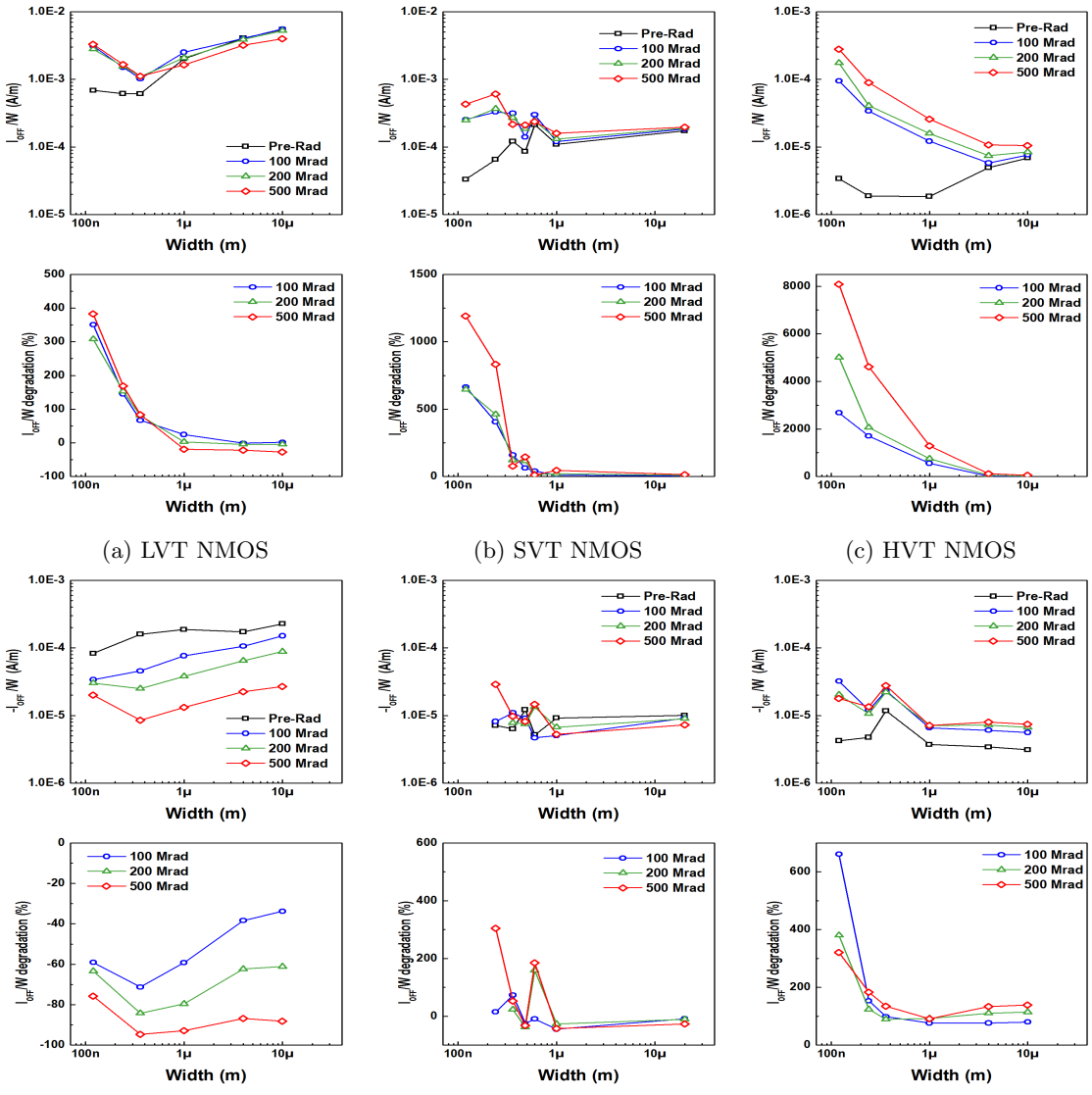
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 33: Leakage current normalised by $\frac{1}{W}$ and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

As has been remarked in a previous section where the leakage currents were examined as a function of device length, NMOS devices suffer much more from increased leakage as an irradiation effect ([20]). In this section where short length meets narrow width this outcome is magnified

greatly and made plain to see. NMOS devices with small L and W emerge from the irradiation process with a 10 to 30 times increase in the leakage current levels. This effect may be a compounding factor in the larger increase observed the NMOS n factor, compared to the PMOS devices, as highlighted in the previous corresponding section. PMOS on the other hand exhibit a much more controlled increase in leakage current, rising up to a 3 to 6 times increase at most. Since in P types degradation is more restrained, we might be able to observe the effect described in [10], that increased temperature facilitates the diffusion and dissipation of the charges responsible for the leakage increase. This is supported by figs 33d,e,f where contrary to most cases reviewed so far in this work, at -30°C we expect and record worse device behaviour than at room temperature.

3.4.12 Leakage Current Width Scaling at 0°C, LVT, SVT, HVT devices



(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 34: Leakage current normalised by $\frac{1}{W}$ and relative degradation, scaling vs channel Length at 0°C for N and P type devices of low, standard and high threshold voltage

The leakage current plots produced for the different V_{TH} types provide us with very intriguing results. We can observe in both N ant P type devices that higher-dopant concentrations seem to incur more leakage degradation with radiation. In N types this is relatively straightforward, with high V_{TH} transistors exhibiting a very significant leakage current increase with a distinct inverse relationship to width. In P types on the other hand, we see the low V_{TH} transistors becoming an order of magnitude *less* leaky after irradiation. N type low V_{TH} transistors also exhibit an improvement in their leakage current but only in the wider devices and to a far lesser extent. The fact that NMOS devices suffer greater damage to their leakage after irradiation continues to hold.

3.5 Discussion

3.5.1 RISCE

From the preceding graphs in par.3.3 we can clearly see evidence of the phenomena described in par.3.1.1. From our starting point of Standard V_{TH} transistors we can confirm the differences between N- and P-type devices as described by our colleagues in the referenced literature, pertaining to the effects of TID on the LDD parts of the device. Specifically, NMOS are expected to sustain hot carrier injection damage, which is mostly observed in shorter channel devices. True to that, we have shown that devices of shorter L are proportionally much more affected than longer ones. On the other hand PMOS were expected to show performance degradation for longer channels as well and this is also consistent with our data. There are more interesting observations to be made though, for example pertaining to DIBL and its different behaviour between the two types. By only looking at the DIBL graphs, one could be led to the wrong conclusion that PMOS do not exhibit radiation induced DIBL, whereas NMOS do. This is not the entirety of the phenomenon, however, as by considering the V_{TH} plots one can come to the realisation that in PMOS, linear and saturation V_{TH} is impacted to the same extent. Moreover, DIBL is associated with the V_{TH} shifting at elevated V_{DS}. On NMOS however, TID has the effect of not only slightly lowering the saturation V_{TH}, but also greatly increasing the linear mode one. This last observation on the linear mode V_{TH} has not been made before in the relevant literature and warrants further investigation. In the initial decrease in V_{TH}, followed by its increase in NMOS and the monotonous increase only in PMOS we are witnessing the effects of the opposite charges accumulating in the spacers and the interface in NMOS and the single (positive) type in PMOS, as described in par.3.1.1.

From an inversion level standpoint, regarding strong inversion saturation operation, we are again in good agreement with the literature. The trapped charge and interface trap interplay just mentioned in the V_{TH} response is also evident in the I_{ON} graphs, with an initial increase (with TID) in the device's current in NMOS which is also mirrored in the effective mobility. The same is *not* observed for PMOS, where from the beginning of the irradiation, current only decreases. This is too the case with the mobility. Continuing on, we again have evidence of the different mechanisms of degradation between the two types, as seen by the severity of the current drive decrease in PMOS for all device lengths and the impact being more obvious in shorter L NMOS only. Here the temperature comparison enables interesting observations as well. It has been mentioned in section 3.1.1 that elevated temperature helps the trapped charges to migrate more easily in PMOS, while their mobility is sufficient in NMOS even at lower temperatures. As a result the almost equal degradation recorded at all temperatures in NMOS is contrasted to the obviously amplified damage that PMOS suffer at 25°C versus 0°C and -30°C.

In the weak inversion region, we have presented graphs pertaining to the slope factor (n) and the leakage current. For the former not much can be said, apart from the fact that in PMOS it shows little to no impact by TID, whereas in NMOS a low sensitivity is recorded, becoming stronger with temperature and decreasing channel L. In the literature PMOS are expected to show a degree of subthreshold slope shift after annealing, which was not considered in this work. On the topic of leakage current, NMOS devices exhibit a much stronger response than PMOS, with the exception of 0°C PMOS, which however may be disregarded as suspect when compared with similar Low and High V_{TH} devices. Thus while PMOS show a ~ 5 times increase in I_{OFF}, NMOS show a 15 times increase, which is very substantial. For the leakage current plots, we normalized the values by $\frac{1}{W}$ so the fact that we observe a maximum not in either extreme of the L scale is very interesting. However we do not yet have an explanation for the mechanism behind the large leakage increase in larger W devices apart from the charge trapped in the sidewall STI (as described in par.3.1.2 we expected TID induced leakage to become more evident in narrower devices).

Pertaining to the comparison between the three different "flavours" of the technology, Low, Standard and High V_{TH} devices, we had the preconceived notion that TID damage should have an inverse relationship to the dopant level used to engineer the device's characteristics. It would be

a logical conclusion to assume that the lower dopant concentration employed in Low V_{TH} devices would make them more susceptible to the external parasitic fields produced by the trapped charges, with the reverse being true for High V_{TH} ones. While Low V_{TH} transistors do indeed suffer more under TID, High V_{TH} ones in general do not (at least given our limited data sample) prove more resilient. On the contrary, at times their relative degradation reaches that of the Low V_{TH} ones and given their pre-irradiation (by design) high threshold voltage and lower subsequent current capability, these devices are left lacking. More specifically, Low V_{TH} devices of both N- and P-type exhibit a greater relative degradation of their threshold voltage, weak inversion slope factor and current drive and by consequence DIBL and KP as well, when compared with their Standard V_{TH} equivalents. As we already mentioned, we were taken by surprise at the relative degradation that High V_{TH} transistors exhibit, both to their Standard V_{TH} counterparts, often having worse degradation but also to their Low V_{TH} counterparts with degradation at times equally as high. An impressive example of this is the PMOS Low and High V_{TH} devices which both show a 55% drop in their current drive, contrasted to the 35% drop recorded in standard V_{TH}. Other examples are the threshold voltage plots, in which both N- and P-type High V_{TH} transistors exhibit a larger (absolute) increase in V_{TH} than the Standard V_{TH}. Finally special mention is warranted for the leakage current plots produced by our data. Contrary to all expectations and all other characteristics studied, here Low V_{TH} devices show the best TID performance in N-types with High V_{TH} being the worst. Remarkably, in P-type Low V_{TH} devices, a *decrease* of leakage current is recorded for the shorter ($L < 1\mu m$) devices, with High V_{TH} ones showing minimal degradation as well. As stated in the previous paragraphs, this very low sensitivity to TID in Low and High V_{TH} devices, points to the suspect nature of the large degradation recorded in Standard V_{TH} devices. This effect has not been examined in the literature, to the best of our knowledge, and we believe should be tested for repeatability and if found statistically important, characterised further.

3.5.2 RINCE

In order to study the RINC effect we have used width scaling arrays of the shortest L (60nm) dimension. This has been a deliberate choice, despite the simultaneous action of the RISC effect we have been describing up to now and has the added effect of showing the worst damage that prolonged exposure to ionizing radiation can do to devices widely used in analog and digital circuits alike, namely devices of smaller geometry. Following a similar flow as before, beginning with the Standard V_{TH} temperature comparisons, we again observe that N-type devices show an exaggerated response in the linear mode threshold voltage relative to the saturation values, with P-types having both linear and saturation operation affected at the same rate. Again the effect of opposing trapped charges, in the STI this time, in NMOS is visible with the V_{TH} shift being negative for lower TID levels and becoming positive as TID increases. The extreme linear V_{TH} shift of NMOS can be seen in fig.35. This showcases that a similar mechanism of charge trapping, migration and (in the case of NMOS) equalisation is underway and that this mechanism is not replicated in PMOS where the V_{TH} shift is always positive (in absolute value). As expected from the RINCE theory, device W plays a central role in the amount of degradation, with temperature also aggravating the results, as charges in the oxide can more easily migrate. As expected, the DIBL plots reflect the above observations with the width and temperature dependencies becoming easily noticeable. Again the PMOS response is evidence of the same degradation of linear and saturation V_{TH}, with the exception of the narrowest devices at 0°C and 25°C, where linear mode damage is significantly higher.

In the strong inversion region we have recorded the anticipated difference in behaviour between the two device types. The main failure mode mode of PMOS transistors becomes now evident; with current handling capabilities becoming 20% of their original value, the significance of low temperature operation is highlighted for PMOS of small dimensions to be even remotely viable in the long term. It also emphasizes the meaning of the phrase that "PMOS turn into high value resistors", which has been used to describe their resulting state, as fig.35 shows the output characteristic of such a device becoming almost linear. Other than that, we record a roughly half

relative degradation in equivalent NMOS devices, with the slight initial increase now manifesting only as a delayed onset of symptoms, after the first 100Mrad dose. These observations also hold for the effective device mobility, which as with the previous arrays we analysed, for both N- and P-types has a similar trend as the on-state current but shows 10-20% less relative degradation. We surmise therefore that other factors, most probably the V_{TH} shift, account for the total current decrease we observe.

For sub-threshold operation we have presented graphs demonstrating a significant increase in the sub-threshold slope factor in N-type devices and practically no degradation in P-types. This is not directly attributable to the RINC effect but to the RISCE [20], which has been described before. What we recorded as an increased response in the short channel tail-end of the length scaling plots is now evident as a common characteristic of all the N-type devices belonging to the width scaling array. However in addition to the short channel sensitivity we also clearly see a W-dependent trend in NMOS, not reported elsewhere in the literature. Leakage-wise we have observed the failure mode of N-type devices under TID, that is a large off-state current increase, as depicted in fig.35. It is to be expected that with ever increasing total dose (the expected end-of-life maximum for the HL-LHC after 10 years is projected to be in the 1Grad range), these small geometry devices do not effectively turn off. It is not very clear from our data if a lower operating temperature can shield against this effect, as we record a larger relative degradation in both NMOS and PMOS at -30°C versus at 0°C. While according to [10] this might be expected in PMOS, as charge diffusion and dissipation is facilitated by higher temperatures, in NMOS this should be already happening even at lower temperatures.

From our comparative analysis between Low, Standard and High V_{TH} devices we again see that by almost all criteria Low V_{TH} transistors have the worst response, which again was expected. What was hinted at by the Length arrays before is repeated in the PMOS devices of the Width arrays in this part, pointing to the fact that there may indeed be a reason for the High V_{TH} transistors responding worse than the Standard V_{TH} ones or that at least further investigation is needed. These arrays are physically separate and have been irradiated independently from each other, so common trends can either be coincidental, due to the very limited sample size (one of each array for each type and temperature) or pointing to actual trends that warrant more attention. As this seems to be evident in PMOS, where High V_{TH} devices *always* exhibit larger degradation but not in NMOS, where the degradation follows our initial assessment of higher dopant concentration leading to more resilience, we cannot make a conclusive statement. It must again be stressed that the leakage response is of great interest in these width arrays as with the length arrays examined before (and the extra arrays included in the appendix), as Low V_{TH} devices always have the best response and High V_{TH} ones the worst. This is true again here with the extremes being High V_{TH} NMOS devices whose leakage increases eighty-fold and Low V_{TH} PMOS, whose leakage actually *decreases* with TID by more than 80%.

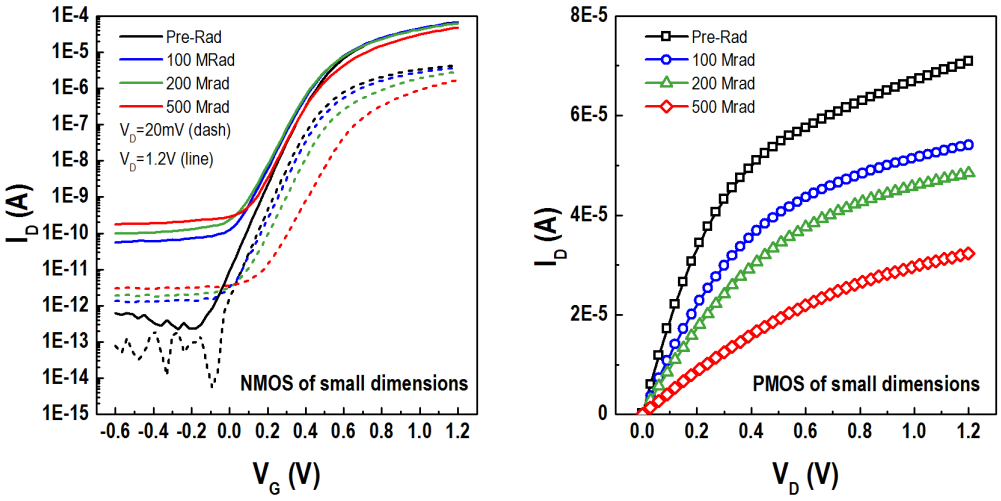


Figure 35: TID damage progression for short and narrow N- and P- devices. Drain current versus Gate Voltage for NMOS (left) and Drain current versus Drain Voltage for PMOS (right). PMOS device is depicted for a drain bias of $V_{GS} = 1.2V$.

3.6 Conclusions and ongoing work

A good way to summarise our observations from this chapter is to view the previous analysis from the perspective of the ASIC designers at CERN, for whom this work was originally undertaken. Knowing that this 65nm technology is being considered for implementation with both analog sensors and digital logic circuits close the collision sites, we can give specific advice towards the longevity of the HL-LHC experiment. In our understanding, the circuits will be kept at -30°C or even lower temperatures and we can conclude from our data that this is most certainly for the best. However, regarding the devices used we have to advise against the utilisation of smaller geometries, even though they are in many applications preferred for both faster speed and lower power consumption. At the very least, the smallest allowed geometries should be avoided entirely, as the TID experiments show that they do not easily survive the harsh radiation conditions. This might be a problem specifically for digital circuits, where small devices are prized for the aforementioned reasons. A solution can be found in utilising "hardness by design" principles such as edgeless transistors, on which our team has performed similar analysis, not presented in this work. Another condensed piece of advice is that Standard V_{TH} transistors seem to be at the crossroads of acceptable degradation and performance. While Low V_{TH} devices are again utilised in digital circuit design for the same reasons as above, their sensitivity to TID negates this, and as shown in the comparisons, many times leaves these devices in similar condition to their standard V_{TH} counterparts after irradiation. Furthermore the jump from the pre-irradiation conditions is much larger than in equivalent Standard V_{TH} transistors as evidenced by out degradation plots necessitating IC designs that will be functional over a much wider spread of operating points. Finally, we would have to advise against High V_{TH} types as not only are their pre-irradiation characteristics similar or worse to the Standard ones but as we have discussed previously, there may exist reasons for heightened TID sensitivity that have not yet been thoroughly studied.

This leads us to the plans for the possible continuation of this work. It should be noted that while the investigation of the DC characteristics was already a huge undertaking, it is but a part of the complete electrical response of a MOSFET. Device capacitance response to TID is a logical next step in the characterisation of this technology as is 1/f noise response, which is certainly impacted, as we know that trap states at the oxide interface are part of the TID degradation. Moreover interesting observations made in this work can be followed up on, such as the counter-intuitive sensitivity exhibited in many High V_{TH} devices or the inverse (in relation to all other

characteristics) relationship of the leakage sensitivity to device type (LVTs by far less sensitive than SVTs and those in turn less than HVTs). The field of MOSFET response to ultrahigh levels of ionizing radiation is a vast one and our team can continue to play a part in its exploration.

4 Noise measurement and characterization in 110nm CMOS technology

This part of the thesis pertains to the measurement, characterization and parameter extraction of 1/f noise produced by MOSFETs of a commercial 110nm CMOS technology. The measurements were conducted on-wafer, at the Electronics Laboratory at TUC. The wafer was provided by a semiconductor foundry for this express purpose, as were the specifications for the geometries and conditions to be measured. In the next sections the measurement specifications will be presented followed by the measurement setup, the measurement strategy and procedure as well as the analysis of the produced data. The section concludes with a discussion of the results.

4.1 Measurement specifications

The measurements were performed on a single undiced wafer (fig.36) containing multiple copies of the same test die, produced specifically for quality testing and characterization purposes. The devices were organized in arrays, each containing multiple geometries, in matched pairs as shown in fig.37. Of these we were interested in the following types and geometries shown in table 1. The arrays used common Gate, Source and Bulk terminals and separate pads were available for connecting with each transistor's Drain terminal.

- LV Low leakage N-type MOSTs
- LV Low leakage P-type MOSTs
- LV Low leakage Native N-type MOSTs

NMOS	**PMOS**	**Native NMOS**
W=10μm L=120nm	W=10μm L=120nm	W=10μm L=500nm
W=150nm L=10μm	W=150nm L=10μm	W=500nm L=500nm
W=5μm L=2μm	W=5μm L=2μm	W=5μm L=2μm
W=2μm L=1μm	W=2μm L=1μm	W=2μm L=1μm

Table 1: List of DUTs

All geometries were measured at room temperature (25°C). Additionally the W=2μm L=1μm geometry was measured at 125°C as well. Four geometries of NMOS, PMOS and Native NMOS transistors were measured on 5 physically distant sites of one wafer. Frequency spectra for the drain current noise (S_{I_D}) were measured and will be presented. The accompanying DC characterization was also carried out, covering the DC operating points of the noise measurements ($V_D = 0.9V$ and V_G variable, so as to cover device operation from weak to strong inversion) but will not be included in this work.

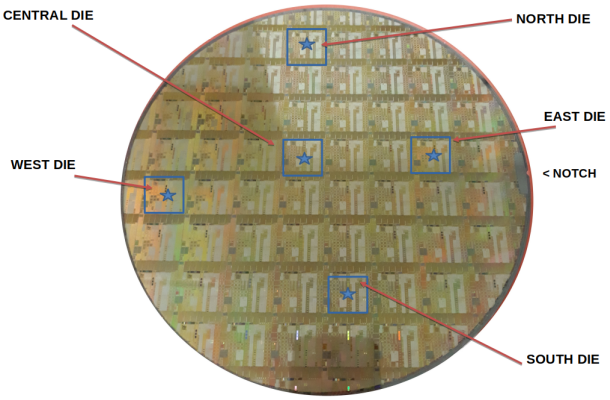


Figure 36: Test wafer with chosen measurement sites. Notch highlighted to provide orientation

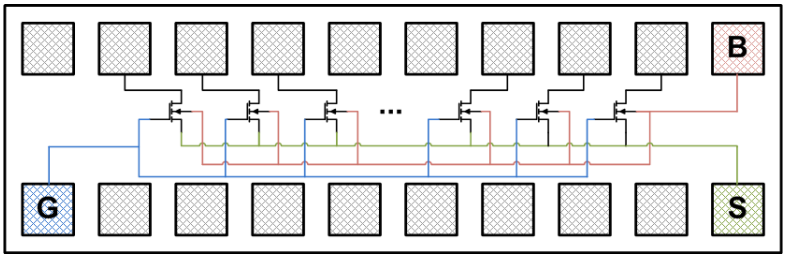


Figure 37: Schematic representation of measured arrays. Unnamed pads represent Drain terminals.

4.2 Measurement setup and operation

For the measurements, the following noise measurement set-up was assembled and used. The equipment and software used are part of the array of instruments utilized at the Electronics Laboratory at TUC.

1. Cascade Microtech probe station, equipped with four micro-manipulators, thermally controlled chuck and faraday cage microchamber.
2. Temptronic TP3000A, active temperature controller for the chuck.
3. 1Hz switchable filter.
4. HP/Keysight 4142B Modular DC Source/Monitor, equipped with three SMUs and one Ground unit for DUT biasing.
5. Stanford Research SR570 configurable low noise current amplifier, used as a preamplifier front-end.
6. HP/Keysight 35670A dynamic signal analyzer for noise frequency spectrum measurements.
7. Various interconnecting cables for signal (triaxial, coaxial), data (GPIB, RS232) and assorted adapters (triax-to-bnc)
8. Computer running ICCAP 2012 for instrument control and data acquisition.

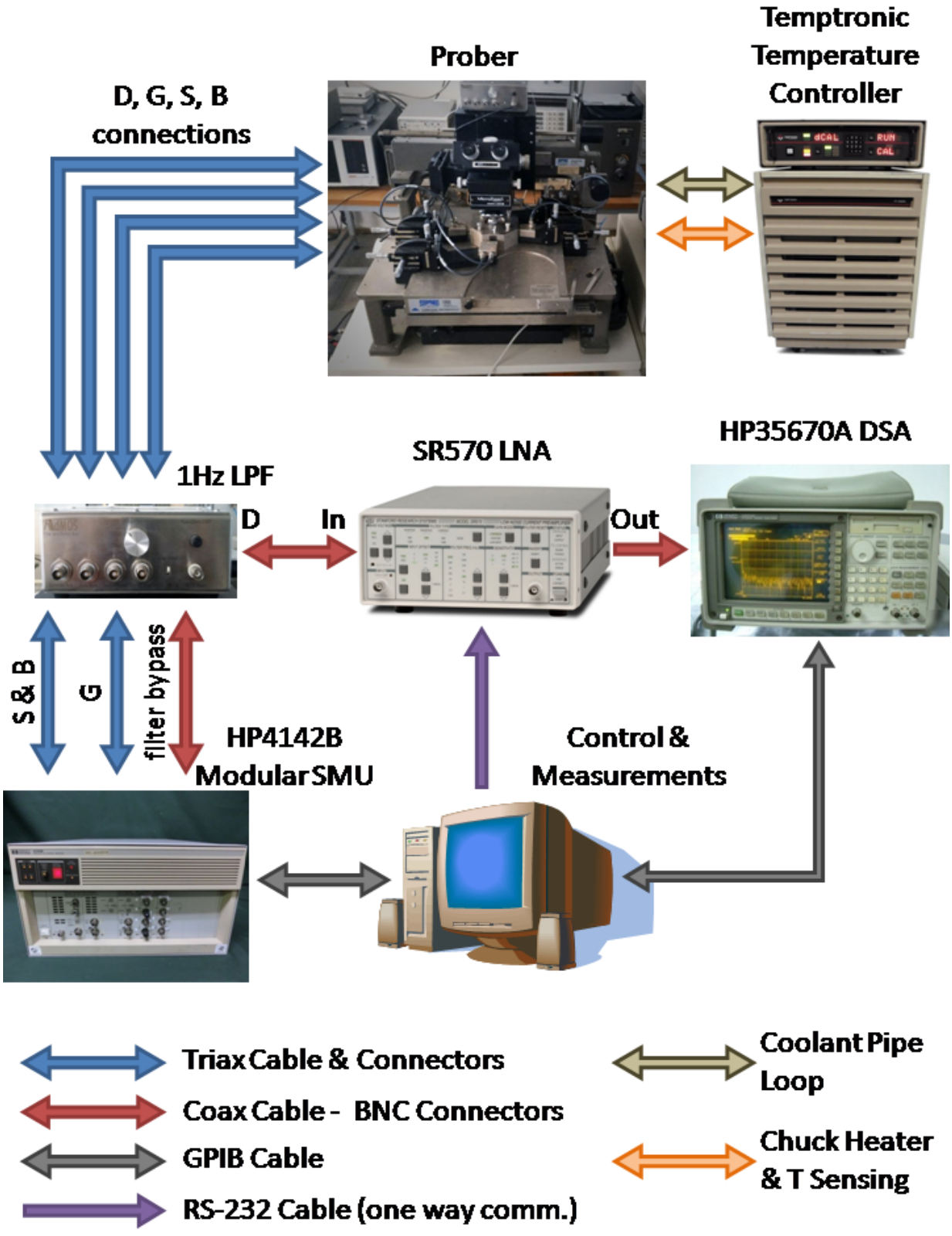


Figure 38: Schematic representation of the measurement setup

The core of the above system is comprised of the DUT biased by the SR570 amplifier. This is depicted in fig.39 below:

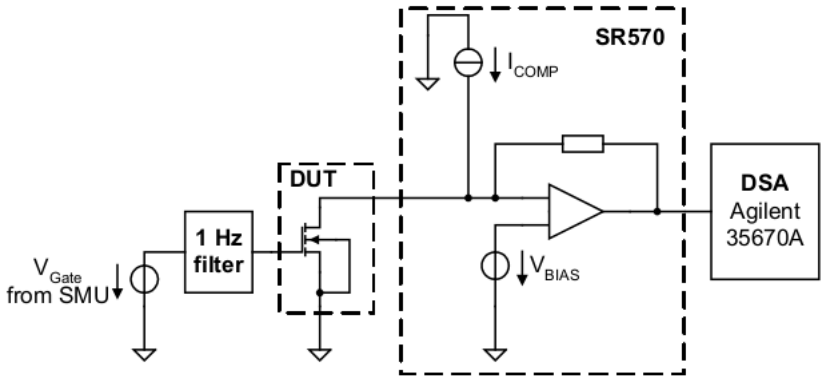


Figure 39: Measurement system core

The DUT is biased by a voltage and current stimulus provided by the SR570 through the I_{COMP} and V_{BIAS} sources. The V_{BIAS} source sets the operating voltage (-5V up to 5V) and the I_{COMP} source provides the current (in the range of -5mA to 5mA), so that the power load is not placed on the sensing transimpedance amplifier, something that would lead to heating and inaccurate measurements. The amplifier can thus sense and amplify the minute variations in the transistor drain current, the noise we are interested in, and output a proportional voltage which is then read by the DSA and recorded. Gate biasing comes from one of the 4142 SMUs and is filtered through a switchable 1Hz 3^{rd} order filter. The filter is mandatory so that the SMU's intrinsic noise, as well as the mains 50Hz noise, are not added to the DUT's intrinsic noise. It also needs to be able to be switched out entirely, in order for high speed DC measurements to be carried out without the need for rearranging the setup or waiting for the filter to settle. Switching is controlled via a second 4142 SMU as needed.

The above is the simplified operation description. In reality many more unwanted noise intrusion paths have to be blocked for sensitive measurements to be possible. A good star ground is important to avoid ground loops and to provide a good rejection point for radiated noise that could be picked-up by either the DUT, the cables or the instrument chassis. The star point is in the back of the 1Hz filter box and ground return is completed through the HP 4142B chassis ground. Also imperative is a clean power supply for the SR570 amplifier. This was thought of by the manufacturer and internal rechargeable lead-acid batteries are used so that the amplifier can be unplugged from the mains to provide better isolation to the sensitive front-end from mains noise. The wafer is placed on top of the chuck (electrically floating), inside a sealing Faraday cage and the whole prober chassis is grounded to the star grounding point.

Biasing and sensing is done through triaxial cables up to the prober needle. These use the center conductor for the signal, the outer braid conductor is used as a shield and internally connected to system ground and the intermediary "guard" braid is actively driven to the same level as the center conductor. This way any voltage difference between signal and shield cannot cause a current to flow (as would be the case in a simple coaxial cable) between signal and shield and contaminate the measurement, instead that current is absorbed by the low-impedance guard driver. Dry graphite lubricant is used between the plastic insulator layers of the cable to dissipate any static electricity due to cable movement and friction of the plastic layers. The system (mainly the 1Hz filter box) does not allow for Kelvin type (force-sense) measurements, although in our case currents are rather low and this does not pose much of an issue.

The 1Hz filter serves multiple purposes. Most important is the low-pass filtering of the gate electrode bias. It also acts as the center of the star grounding scheme as mentioned above and as the interconnect between the cables coming from the SMUs, the cables going to the prober needles

and the cable going to the amplifier. It is a commercially available solution for low frequency noise measurements provided by AdMOS and comes with a custom written ICCAP GUI. This GUI provides a user friendly interface that coordinates and controls all the above mentioned instruments so that DC transfer and output measurements can be carried out, followed by noise measurements without the need to change the hardware setup. It also provides a means of calibrating the SR570 (which is a "listen-only" instrument without the capability to relay information back to the controller PC) using the sensing capabilities of the HP 4142B as well as calibrating the setup as a whole by providing specific routines to measure and correct for the system noise floor at the various amplifier gain levels.

4.3 Measurement strategy and procedure

Low frequency noise measurements are time-consuming due to the long intervals needed to sample the needed frequency ranges, a fact compounded by the need for multiple measurement averaging done by the DSA as a first step to acquire usable, unwanted-noise-free noise measurements. Therefore a precise measurement strategy has to be established up front, for the least wasted time and the most useful data. First of all a series of DC transfer measurements were carried out on two diametrically opposed dies (not ones that would be used in the final measurement run, so as not to damage them) and used established techniques [3] to calculate the threshold voltage "V_{TO}" as well as the specific current of the technology "I_{SPEC}", for every geometry belonging to the three types of transistors mentioned in section 4.1. From this knowledge we could then calculate approximate gate bias voltages that would cover the chosen inversion levels. We decided on a set of 8 V_G offsets that when added to the V_{TO} and applied to the gate, should result in inversion levels very close to the designated ones. The relationship among inversion coefficient IC and inversion charge at the source, q_s, in saturation is $IC = q_S^2 + q_S$. The inverse relationship is, $q_S = \sqrt{\frac{1}{4} + IC} - \frac{1}{2}$. Knowing that $v_P - v_S = 2q_S - \ln q_S$ and $V_P = v_P U_T = \frac{V_G - V_{T0}}{n}$ and assuming V_S and n to be constant, we can derive a formula which takes IC as an input and produces a voltage offset with respect to the V_{T0} that when added to it and applied to the gate terminal, will result in the required level of inversion. Going through a few iterations we can thus calculate rounded ΔV_G values to come close to our IC requirements (always respecting the maximum V_{GS} of 1.2V) as shown in the table below. This is a necessary step in cases like this where measurements at specific inversion levels are needed instead of specific gate biases. Obviously for P-type devices the sign should be inverted.

IC	**ΔV_G**
0.01	-150mV
0.04	-100mV
0.18	-50mV
1.6	+50mV
10	+200mV
29	+350mV
57	+500mV
97	+650mV

Table 2: V_G Offsets for specific IC

It is known that V_{TO} can exhibit device variability, to an extent dictated by how tightly controlled the fabrication process is. In the end the V_{TO} proved to be rather well-behaved with small variations in the order of no more than $\pm 50mV$, however this was an unknown factor at the beginning, that would have to be accounted for, by setting the bias points on a per-DUT basis, to account for the V_{TO}, further increasing the time per measurement while increasing the possibility for user error. To combat this, we manipulated the GUI-generating code that we generally use in ICCAP for noise measurements, in order to add extra functionality. Checkboxes were added so the user can select the type (N, P or native N) as well as the geometry from a list of

available ones. Moreover a constant current V_{TO} extraction routine was integrated, so that after measuring the IV characteristics of each DUT, the program would automatically calculate and set for itself the V_G bias voltages used for noise measurement. This highly streamlined procedure is implemented for the first time at our laboratory and has the potential to greatly simplify the whole measurement process. In the past, the V_{T0} of all devices to be measured had to be calculated in a preliminary measurement run, the bias points for each device would have to be calculated and stored and would have to be manually entered at the time of the noise measurement. Our approach manages to reduce the overall time needed per device and more importantly reduce the user-error parameter to a minimum. What's more, the code written for this purpose is easily adaptable and should provide such simplification to future projects similar to this one, so it is a tool added to the laboratory's arsenal.

In the end we concluded that we would measure output characteristics for a V_D range of 0 to 1.1V with a 50mV step at a V_G range from -0.15 to 1.2V with a step of 50mV as well.
As for transfer characteristics, the gate voltage would be swept from -0.6 to 1.2V with as step of 50mV, at 6 drain voltage biases, from 0.1 to 1.1V with a step of 200mV. The measurement algorithms require that the noise measurement operating conditions should be present amongst the IDVG and IDVD measurements. So after covering this bare minimum, we added more measurement points, with a small time cost, to the overall measurement protocol, which will aid in future analysis and characterization of the produced data. The above allow for enough data points for a good validation of the DC operation, while still not adding much to each DUT's overall measurement time.

Once the DC measurement protocol had been fixed, we then had to come to specific conditions for the noise measurements. The frequency range in our system has its lower and upper bounds set by the following factors:

- LPF corner frequency (1Hz).
- DSA maximum bandwidth (25kHz for our model).
- Amplifier gain.

Our lower bound was set by the filter. We decided that with the roll-off present at 1Hz, 2Hz should provide a usable lower frequency stop. As for the upper bound, it is widely known that an amplifier's gain and bandwidth product has a fixed value. By going through a number of measurement test runs, we concluded that 200nA/V transimpedance amplifier gain was a good trade-off for sensitivity at lower current levels as well as lower system noise floor. The system's upper corner frequency would then be 2kHz, giving us just enough room to extract the measurements requested in the end of section 4.1. At higher currents (larger ICs) when the amplifier's output becomes saturated, the measurement algorithm detects this condition and automatically lowers the gain, thus pushing our upper corner frequency higher.

Next, we had to consider the way our DSA splits the frequency spectrum. It can split its bandwidth in segments, each subsequently split into 400 frequency bins. The DSA then measures the power density in each bin. Given also the technical limitation that the step for each bin has to be an exponent of 2, we had to strike a balance between the necessity for accurate low frequency ($< 100Hz$) measurements, the time needed and the resulting available bandwidth. As a best compromise of the previous, we arrived at the following scheme:

- 2-402Hz with a 1Hz step.
- 402-1202Hz with a 2Hz step.
- 1202-4402Hz with an 8Hz step.

all the above at 40 averages per range, at 8 different gate bias voltages. The resulting complete measurement protocol amounted to ca. 30 minutes per DUT.

Before commencing with the measurement campaign though, the system needs to be calibrated first. While the HP4142 programmable SMU and the HP35670A DSA run their own self-check and calibration routines at startup, we had to run the routines to measure and correct for intrinsic errors in the V and I sources of the SR570 amplifier, as well as measure and record the complete system's noise floor. These, although time consuming would only have to be done once and, provided the system set-up did not change, would be stored and corrected for by the measurement program. While the I and V source calibration is self explanatory (force a set I or V and measure the actual value) the noise floor measurement was more involved, as bandwidth and noise floor are dependent on the amplifier's gain as well as the I source's current range. For this reason the amplifier's input was terminated using precision resistances and its output noise was recorded by the measurement program. Both results are shown below. As with standard measurements, instruments were allowed to warm-up to operating temperature for around 30 minutes before the procedure. Also for the noise-floor measurements, more averages (50) were used for smoother curves.

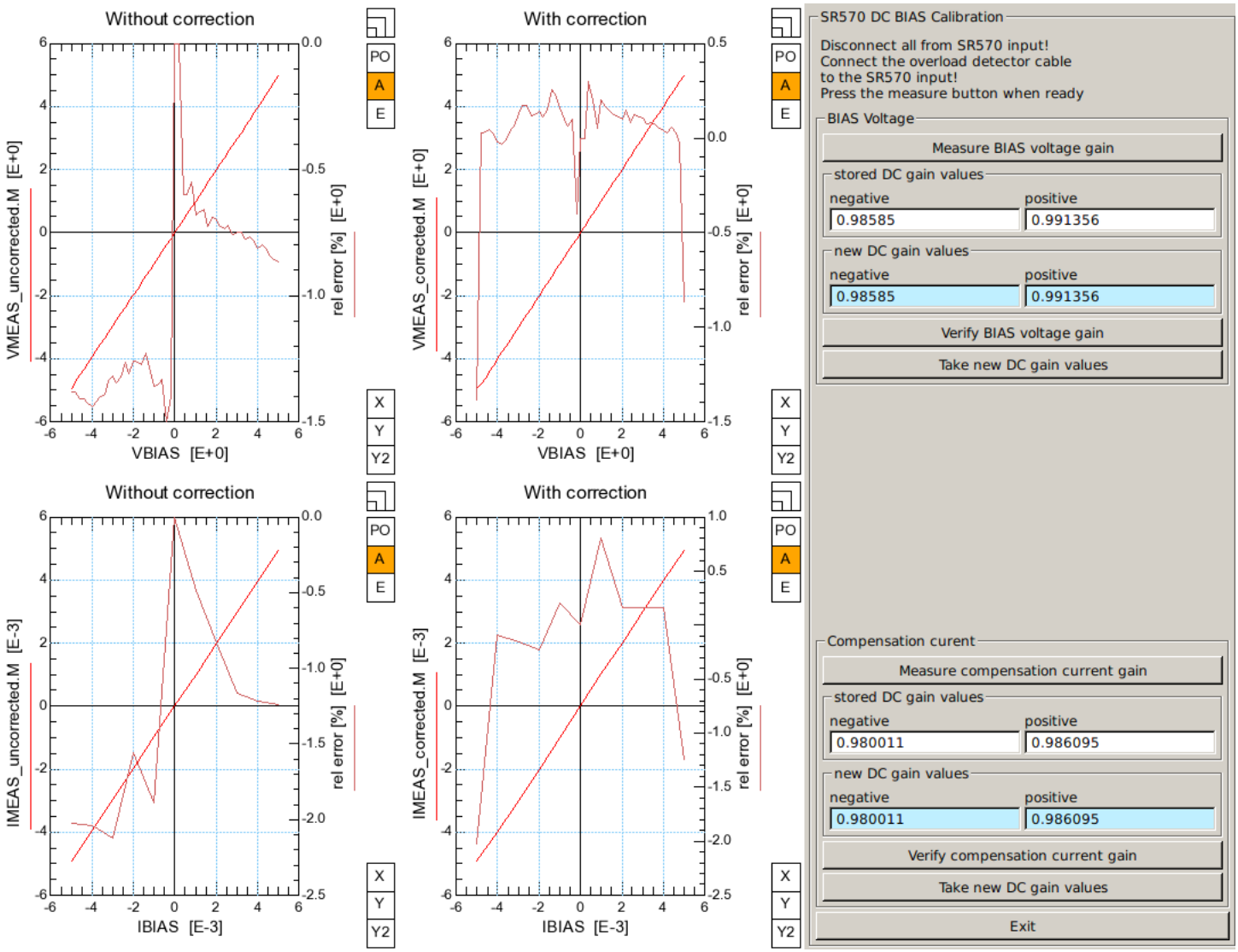


Figure 40: SR570 DC calibration

Output voltage and current are shown before and after correction.

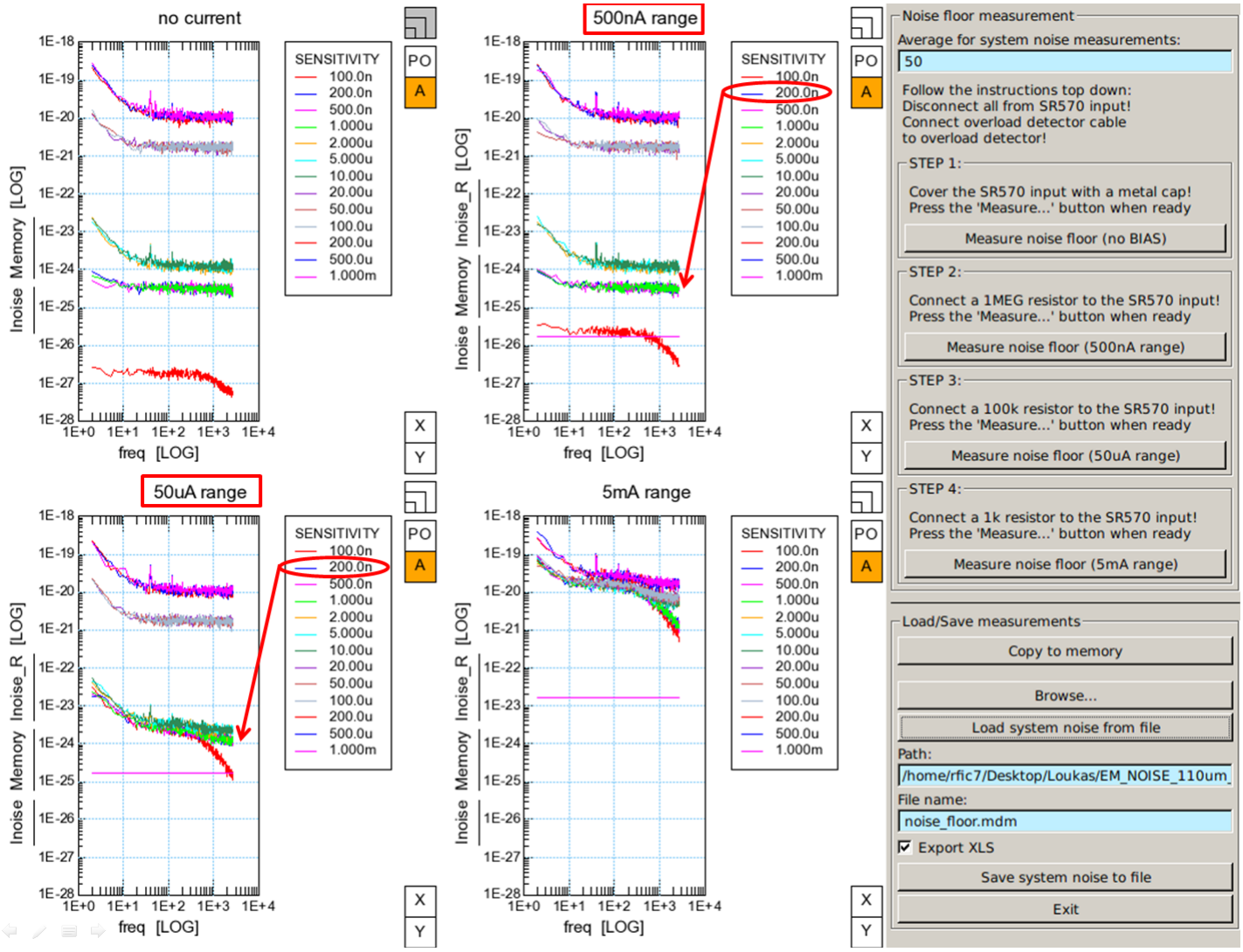


Figure 41: SR570 noise floor calibration

Since we had decided on 200nA/V gain (termed "sensitivity" by the program), and comparing with the DC currents needed for device operation, we can see that our measurement S_{I_D} noise floor could not go below $10^{-24}\frac{A^2}{Hz}$

After all the foundations had been laid, it was time to begin the actual measurements, which took place over the course of approximately twenty days. Depending on ambient electrical noise (most students carry WiFi and 4G enabled laptops and cellphones) as well as mechanical noise (heavy footsteps, doors slamming shut) specific measurements could potentially be rendered unusable, at which point (at times even preemptively) we would have to manually stop and restart the measurement. In conclusion, we ended up with ten measured DUTs per geometry, belonging to 5 different dies, for a total of 120 DC+noise data-sets in room temperature plus another 20 at elevated (125°C) temperature.

4.4 Analysis

As is, the system can output I_D vs V_G, I_D vs V_D and S_{I_D} measurements. Using ICCAP it is relatively easy to apply a multitude of custom-written algorithms (in the form of "transforms" or "macros" in ICCAP terms) to multiple similar data-sets. This way we were able to analyse our data efficiently and produce the mean values needed for model fitting and parameter extraction.

One of the first actions after loading our noise measurement data is to clean-up the noise spectra. Sadly, even with all the precautions taken, we still had considerable spikes at 50Hz (mains frequency), 100Hz (mains frequency after rectification in power supplies), their harmonics, as well as higher frequency spikes of unknown origin, attributed to power supply switching noise. Since our frequency binning was rather dense, rejecting these spikes, which would often appear on a single frequency bin, was easy. The measurement value was simply replaced with the previous bin value without qualitative degradation of data, which is demonstrated below.

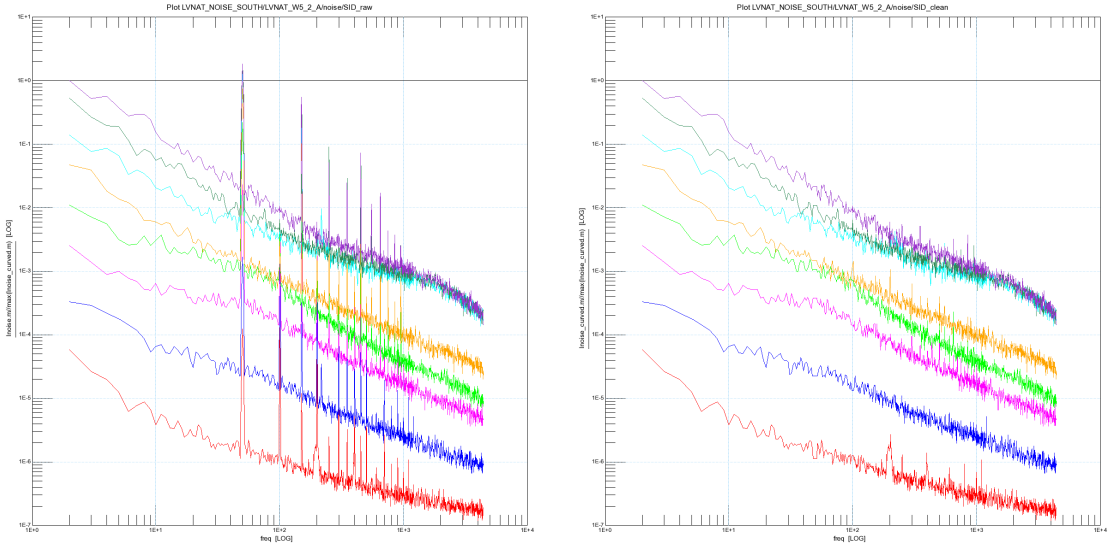


Figure 42: Raw and cleaned S_{I_D} data

Other important steps in the analysis are to produce the output transconductance (g_{DS}) from IDVD measurements, the gate transconductance (g_m) and transconductance efficiency from IDVG measurements. From these, we can then extract important device parameters such as the weak inversion slope factor (n), specific device current (I_{SPEC}), which in turn allows us to extract the threshold voltage (V_{T0}) [3] and to normalize the drain current to the inversion coefficient IC. The g_m as well as I_D values at the specific bias conditions chosen for the noise measurements should now be calculated, as they will be needed next.

Moving on to the noise data, we first calculate and plot the $S_{I_D} \cdot frequency$ product, which easily allows us to judge whether our noise spectrum contains 1/f noise, as in that case the spectra should assume an approximately horizontal appearance, at least in the frequency range where 1/f noise is present. Afterwards, the previously calculated g_m values at the bias points are now used to produce the noise voltage spectrum referred to the gate, S_{V_G} as follows:

$$S_{V_G} = \frac{S_{I_D}}{g_m^2}$$

We can now calculate the value of S_{I_D}, the value of S_{V_G} and the value of $\frac{S_{I_D}}{I_D^2}$ at a specific low frequency, close to 10Hz. Since noise data tends to be itself noisy, it is generally preferred to calculate the mean of the measured value at more than one frequency bin (normalizing by multiplying by the frequency first) and assigning the resulting mean to the median frequency of

the range chosen. The range is chosen depending on the availability and quality of 1/f noise. For example, in the geometry shown in fig.42 the range was set between 6 to 12Hz, and the result was assigned to 9Hz.

For all of the above, custom code was written to perform each function and macros were used to apply those code snippets to each and every measured device recursively. The noise calculations are mathematically straightforward, it should be noted however, that due to the dynamic range of the noise signal, a log-mean was used for the calculations. All the code used for this project was written in "PEL" (Parameter Extraction Language, ICCAP's integrated programming language) and was developed specifically for the needs of this endeavor. Care was taken to hard-code as little as possible, even though this makes code more complicated and time consuming to compose, to allow for code reuse in future projects of this kind, as this is a niche area of expertise that the laboratory covers.

The next step after all measurements were complete, loaded in ICCAP and the aforementioned extractions were applied to all of them, was to produce the mean value of our measurements, to be used as a basis for the model parameter extraction. Again, it was obvious that for signals with such dynamic range, it would be imperative to use a log-mean approach. In a normal mean operation, the sum of measurements is divided by their number. In the log-mean approach, the sum of the logarithm of every measurement is divided by their total number, and the result is given as an exponent of the outcome. The logarithm's function is to compress very large signals and lift very low ones, so as to avoid measurements that deviate too much from the rest dominating over all others. The procedure was as follows and was implemented in PEL code for automation and streamlining.

1. Create the log-mean of IDVD measurements. I_D and V_D data-sets are log-means. Produce the g_{DS} data-set from the mean.
2. Create the log-mean of IDVG measurements. I_D and V_G data-sets are log-means. Produce the g_m, $\frac{g_m U_T}{I_D}$, $(\frac{d\sqrt{I_D}}{dV_{GS}})^2$ data-sets.
3. Calculate the I_{SPEC}, n, V_{T0} values from the I_D and V_G means. At this time the I_C data-set is also produced.
4. Copy the frequency data-set and create the biasing (V_G) data-set, which has to be a mean value per bias point. As it was mentioned before, noise was measured at specific ICs, which means that the V_G bias points for the measured devices could be different per device. Create the S_{I_D} and S_{V_G} data-sets as log-means, per bias point.
5. As the noise V_G bias points are now known, we have to return to the IDVG data-sets and calculate via interpolation the precise g_m, I_D and IC values that correspond to each bias point DC operation. The resulting values are stored as tables.
6. Returning to the mean noise data-sets we can now extract the noise level at a set low frequency close to 10Hz. This frequency coincides with the one used for all the individual measurements per geometry. These data-sets are the levels of S_{I_D}, S_{V_G} and $\frac{S_{I_D}}{(I_D)^2}$ at the aforementioned frequency. The I_D mentioned here is the above calculated at the bias point operation condition.
7. Create all the relative plots.

The procedure described above is automated by means of a 1000 line piece of custom written PEL code. Doing it manually has been done in the past, however the possibility for errors increases and the endeavor is tedious. The automation additionally means that if a correction needs to be made, or if a device exhibits unconventional behaviour and needs to be measured again, the mean values can be computed in a matter of seconds.

4.5 Simulation and EKV3 parameter extraction

At this point EKV3 noise parameters can be extracted. For this purpose the base DC EKV3 model was provided by the manufacturer. We first had to confirm that the DC model provided a good fit of our measurements (from this point-onward "measurements" will refer to the log-mean of the measurements as described in section 4.4). For this reason we described our devices with the following simple SPICE-type statement:

```
include "path_to_model_card" section="tt"
nmos (D G S B) ekvnmos
model ekvnmos n12
```

With the above statement:

- The modelcard is called by its direct path, and the typical (tt) case is used.
- A device instance name "nmos" is chosen (arbitrary name).
- This instance has four nodes, (D,G,S,B) the four electrical terminals of a MOS device
- This device is electrically described by a model named "ekvnmos" (arbitrary name).
- The simulator is informed that the model named "ekvnmos" has the "n12" modelcard behind it.
- Having included the modelcard path, the simulator searches inside for matches to the name "n12" and once it finds a match, gains access to the model parameters and simulations are possible.

Even though the fabrication process has advanced since the last model silicon validation, the model was certainly good enough for DC simulations. However, we elected to modify certain central parameters that would provide even better model fitting, which would also result in better noise model behaviour. Such parameters were "vto", "kp", "gamma", "wedge" as well as some parameters governing scaling phenomena, such as "ka" "qwr" and others [4]. It must be noted that modifications were small and intended as tuning of the model to better represent our measurements. Especially for scaling parameters, great care was taken to keep modification to a minimum, as the device set we had was not adequate for a complete scalable model extraction. In cases, less optimal model fit was preferred instead of modifications to parameters that could wreak havoc to the model, without us noticing. For this stage, the modelcard was called inside ICCAP and parameters were hand tuned inside the (plain-text) model card file. This was the most time-conserving route, as the modifications were easy to perform. After all this we now had enough confidence in the model to proceed with noise simulations, using the basic flicker noise model incorporated in EKV3 [4].

Simulating a device's S_{I_D} spectrum is not as straightforward as it is with DC simulations. The following subcircuit (in Spectre language) has to be used to simulate each device:

```
subckt noise_circ (D G IN OUT)
N (9 6 0 0) EKV3_model L=10u W=10u NF=1
L2 (6 G) inductor  l=1000000
C2 (IN 6) capacitor c=1000000
V1 (D 9) vsource type=dc dc=0
H1 (OUT 0) pccvs m=1 probes=[V1] coeffs=[0 1] gain=1
ends
```

This subcircuit is based on one of the examples for noise simulation provided with ICCAP. By using *"sufficiently"* large values for the capacitor and inductor, it becomes transparent to DC simulations, while allowing for AC noise simulation. The key points are:

- "EKV3_model" refers to the MOS transistor modelcard as described previously.
- C and L act as DC and AC blocking components, respectively.
- The AC current noise component is read through a DC voltage source with zero output, as is standard practice in SPICE-like simulators.
- ICCAP's noise probe expects a "voltage" type input. For this reason a Current Controlled Voltage Source (H1) monitors the noise current and relays it 1:1 as a voltage output.
- The simulation result is the $\sqrt{S_{I_D}}$ and so it has to be squared to be compared to the measurements.

Apart from the subcircuit, one can not use the same exact set-up for measuring and simulating noise. As stated previously, our DSA needs to have its bandwidth separated in segments, something that ICCAP does not support for noise simulations. Thus a new "simulation" setup has to be created for each device bearing the same V_G bias points as the measurement and a single (preferably logarithmic) frequency sweep instead of the segments. An AC source with zero voltage magnitude also has to be connected to the subcircuit so that the simulator can perform the frequency sweep. At this point, of course, the same extractions have to be produced for the simulated data as were produced for the measured, namely S_{V_G}, $S_{I_D} \cdot frequency$ and the level of S_{V_G}, S_{I_D} and $\frac{S_{I_D}}{(I_D)^2}$ at the low reference frequency. These then have to be plotted against the measurements in the same graphs, for parameter extraction to proceed. After all the above are set-up correctly, the user may finally begin to tune the noise model, through iterations of modifying a parameter value, simulating and observing changes in the simulated curves. This can be accomplished by direct access to the modelcard, however it is a tedious process. It is much easier to work from within ICCAP, using the integrated manual parameter tuner. To this end, the following modifications were done to the instance statement, to allow ICCAP to "see" the following parameters:

```
    nmos (D G S B) ekvnmos
model ekvnmos n12
+ af=1
+ kf=1.5e-24
+ ef=2
+ lfnoi=0
```

Only giving ICCAP the parameters, however would be of no meaning; these parameters already exist within the modelcard and any duplicates would be discarded by the simulator. The modelcard was modified as well, to treat these parameters as "instance parameters", to be provided by ICCAP and relayed to the core of the model. The last obstacle was the fact that the ICCAP integrated manual tuner would not cooperate, since the measured noise spectrum and the simulated one were of different types and sizes (i.e. the measured spectrum had its frequency in segments, while the simulated in a single sweep and the frequency steps of the simulation need not be as fine, as the resulting curve is smooth). The solution to this came in the form of more PEL code, essentially recreating the manual tuner, under our full control. Again, the following was custom written for this work and these capabilities of PEL code had not been exploited before at our laboratory.

```
NumParams = 3

params = "ICCAP_ARRAY["&VAL$(NumParams)&"]"
```

```
mins   = "ICCAP_ARRAY["&VAL$(NumParams)&"]"
inits  = "ICCAP_ARRAY["&VAL$(NumParams)&"]"
maxs   = "ICCAP_ARRAY["&VAL$(NumParams)&"]"
logscale=1
immediate=0

!set variables
params[0]= "af"
mins[0]  = 0.5
maxs[0]  = 2
inits[0] = af

params[1]= "kf"
mins[1]  = kf//100
maxs[1]  = kf*100
inits[1] = kf

params[2]= "ef"
mins[2]  = 1
maxs[2]  = 3
inits[2] = ef

!store current model parameter set
ICCAP_FUNC("../../ParameterSet", "Memory Store")

!call the TUNER feature
!-----------------------------------------------------
TUNER params,mins,inits,maxs,logscale,immediate,"sim"
!-----------------------------------------------------

GET_STRING "Do you want to KEEP the new model parameters or reset to previous values?  [y/n]",
"y",answer$
IF answer$<>"y" THEN
ICCAP_FUNC("../../ParameterSet", "Memory Recall")
ICCAP_FUNC("sim","Execute")
END IF

!clean-up arrays
params="ICCAP_ARRAY[0]"
mins="ICCAP_ARRAY[0]"
inits="ICCAP_ARRAY[0]"
maxs="ICCAP_ARRAY[0]"
```

While understanding PEL is useful, with a few explanations it should be obvious what the above piece of code does.

- We initialize temporary local variable arrays (ICCAP_ARRAY) with the number of desired variables.
- "logscale=1" will make the tuner use a logarithmic slider scale.
- "immediate=0" will make the tuner simulate only after the user has released the slider.
- The desired parameters are written to the variable arrays, as well as their min/max and initial values.
- The current parameter values are stored

- The "TUNER" function is called and given the set parameters, to create the tuner GUI. The last parameter("sim") is the name of the function called when the mouse click is released.
- After the tuner is exited, the user is asked whether they choose to keep or discard changes. Should they choose to discard, the previous values are retrieved, restored and the simulation is run again to restore the model to its previous state.

And the result is:

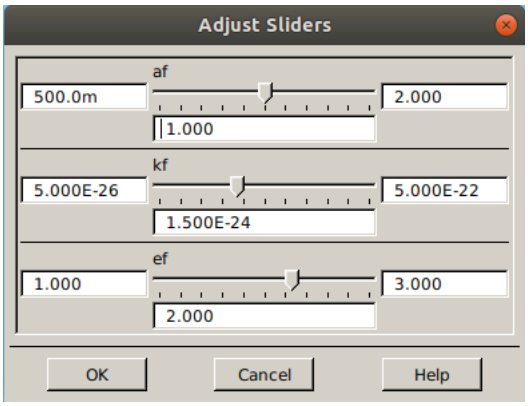


Figure 43: Custom created ICCAP parameter tuner

The ability to manipulate a user-friendly and intuitive slider, instead of typing parameter values in a modelcard, coupled with the fact that simulation begins as soon as the slider is released means that the time per simulation is *more than halved*.

As demonstrated in [24] by plotting the values of $WLC_{OX}S_{I_D}$ at a set low frequency versus g_m in logarithmic scales, the EKV3 "ef" parameter value can be calculated from the slope of the linear part of the resulting curve. This was easily achieved, as all the required data was already at hand. The value produced by this method (the mean of the values for all four devices) was then used as a starting point for the "ef" parameter. The "af" parameter can be easily extracted by fitting the model slope to the measurement, which only left "kf" as a free parameter, to be adjusted so that model noise levels matched the measured.

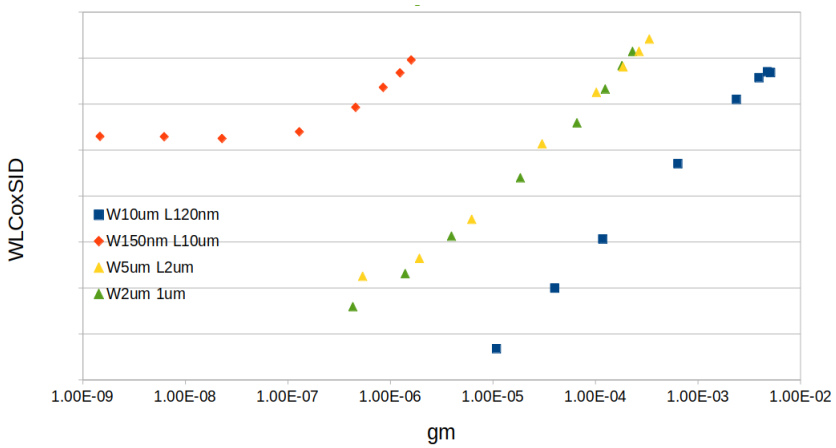
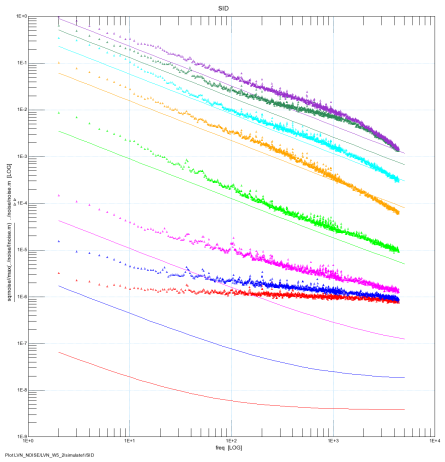


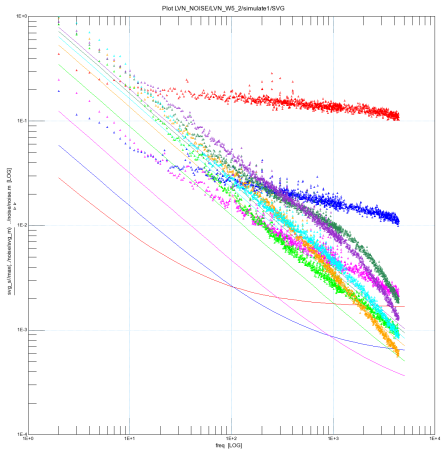
Figure 44: Methodology demonstrated by Martin and Ghibaudo to extract EKV3 "ef" parameter

This method was repeated for all three device types and specific "af", "kf", "ef" parameter values were extracted for the LVN, LVP and LVN native devices. We were not satisfied, however

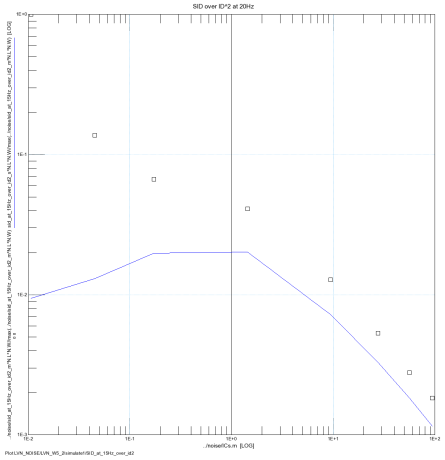
with how the resulting model fit the measurements, despite our best efforts. In weak inversion our measurements seem to increase in value, as can be seen in the following plots, to an extent that the basic model cannot follow.



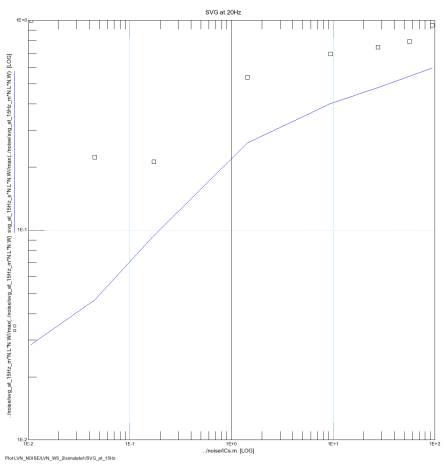
(a) S_{I_D} versus frequency



(b) S_{V_G} versus frequency



(c) $\frac{S_{I_D}}{I_D^2} \cdot f$ at 20Hz



(d) $S_{V_G} \cdot f$ at 20Hz

Figure 45: LVN W5μm L2μm basic noise model behaviour

That behaviour is to be expected, up to a degree. The basic model is mainly targeting moderate and strong inversion, so some deviation from the measurements was expected in weak inversion. Due to this behaviour manifesting itself in all geometries however, we decided to pursue a better model fit by activation of the more complex 1/f noise model present in EKV3 as of version 301.06 [25, 27, 26, 4]. To this effect the core MOS instance statement was modified to the following:

```
    nmos (D G S B) ekvnmos
model ekvnmos n12
+ af=1
+ kf=1.5e-24
+ ef=2
+ lfnoi=1
+ nt=1E14
+ alphac=1E5
+ alphah=1E-20
```

```
+ ecn=1E4
```

Using a similar PEL algorithm as above (not repeated for brevity) that included the new parameters, tuner sliders were again used to extract the parameter values for best model fit. As the noise model does not have its own scaling parameters, our choice was to prioritise best larger device fit (W5μm L2μm and W2μm L1μm) and ICs in the range of 1-10.

4.6 Analytical model

In order to protect the manufacturer's IP as well as provide a more concise view of the phenomena without the overcomplication of the integrated noise model, we will present the result of using the analytical equations, as they have been documented in [17, 28] to model the noise measurements. The S_{I_D} spectrum, of each device was modelled with the following equations and from that, the methodology explained above was used to calculate the S_{V_G} spectrum, as well as the $S_{I_D} \cdot f$, $\frac{S_{I_D}}{ID^2} \cdot f$, $S_{V_G} \cdot f$ at a reference frequency close to 10Hz.

The dominant noise component was used in the analytical approach, namely the McWorther carrier number fluctuation, apparent from weak to strong inversion. The Hooge model (mobility fluctuations) as well as the access resistance contributions were not included. Furthermore, although the equations provide for it by use of the λ_C parameter, short channel effects on noise were not modelled ($\lambda_C = 0.$)

$$\mathbf{S_{\Delta I^2_{nD}}|_{\Delta N} = I^2_D \cdot S_D|_{\Delta N} \cdot K_D(q_s, q_d)|_{\Delta N}}$$

$$where:$$

$$S_D|_{\Delta N} = \frac{q_e \lambda N_T}{kTWLn^2 C_{ox}^2 f^{af}}$$

$$K_D(q_s, q_d)|_{\Delta N} = S_{IC^2}(q_s, q_d, \lambda_C) + \frac{a\mu}{1 + q_s + q_d} + \left(\frac{a\mu}{2}\right)^2$$

$$S_{IC^2}(q_s, q_d, \lambda_C) = \frac{1}{2IC^2} \frac{(q_s^2 + q_s) - (q_d^2 + q_d)}{(1 + \lambda_C(q_s - q_d))^3} ln \left(\frac{q_s + 0.5 - \frac{\lambda_C((q_s^2+q_s)-(q_d^2+q_d))}{2(1+\lambda_C(q_s-q_d))}}{q_d + 0.5 - \frac{\lambda_C((q_s^2+q_s)-(q_d^2+q_d))}{2(1+\lambda_C(q_s-q_d))}} \right)$$

$$q_s = \sqrt{0.25 + IC} - 0.5$$

$$q_d = 0.01 \cdot q_s \ (we\ are\ always\ in\ saturation)$$

- q_e is the elementary charge
- λ is the tunneling attenuation distance (=0.1nm)
- f is the frequency
- k is Boltzmann's constant
- T is the temperature in K
- n is the weak inversion slope

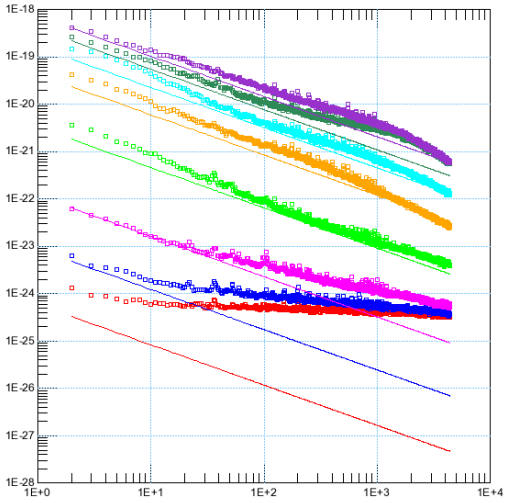
- μ is the mobility
- af is the noise frequency dependence parameter
- N_T is the oxide volumetric trap density parameter, in $eV^{-1}m^{-3}$
- a_c is the Coulomb scattering coefficient parameter, in VsC^{-1}
- $a = a_c \cdot Q_{SPEC} = a_c 2nU_T C_{ox}$

The parameters used to to fit the analytical model are presented below.

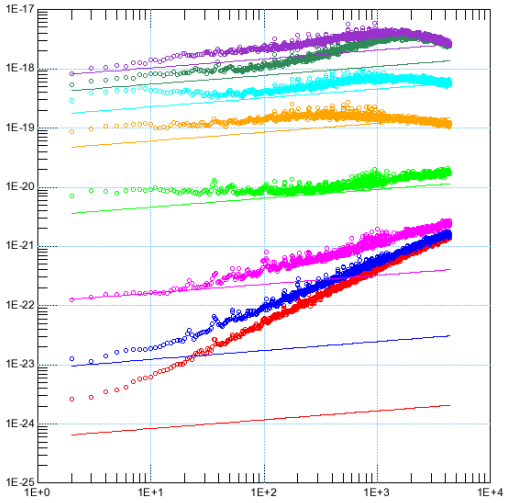
	LVN	**LVP**	**LVN native**
af	0.85	0.95	0.85
$\mathbf{a_c}$	$1.5 \cdot 10^3$	$1.2 \cdot 10^5$	$1.0 \cdot 10^3$
$\mathbf{N_T}$	$6.0 \cdot 10^{41}$	$8.0 \cdot 10^{41}$	$2.1 \cdot 10^{41}$

Table 3: Analytical model parameters.

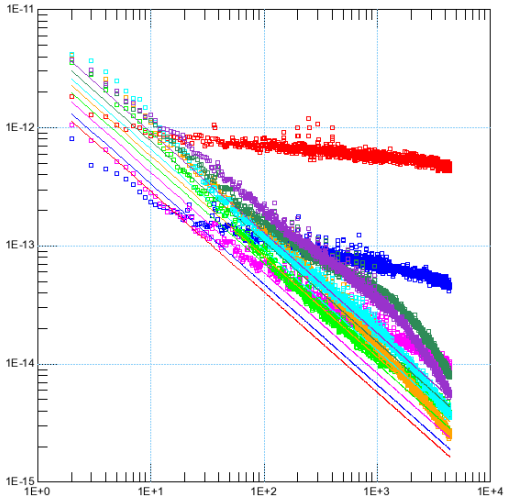
The analytical model is presented below (lines), plotted against our measurements (markers).



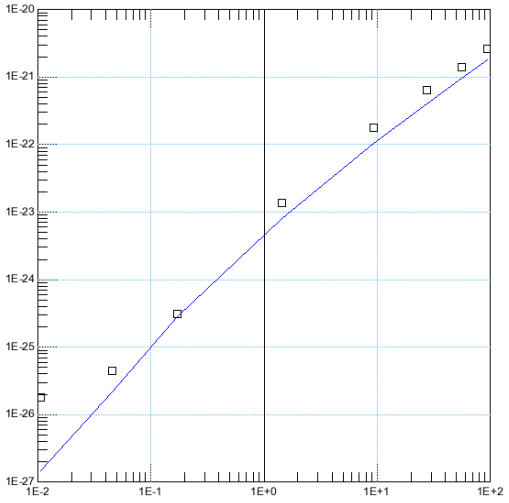
(a) S_{I_D} vs frequency



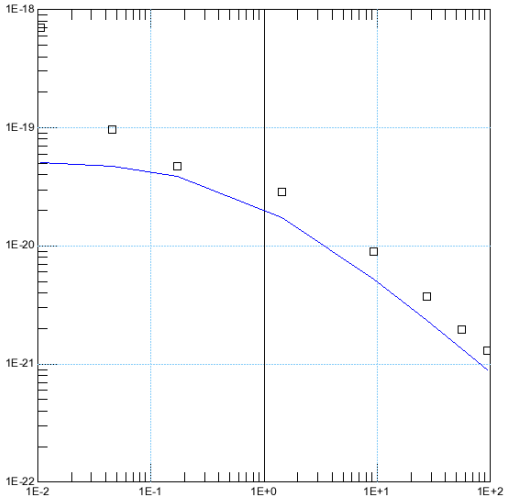
(b) $S_{I_D} \cdot f$ vs frequency



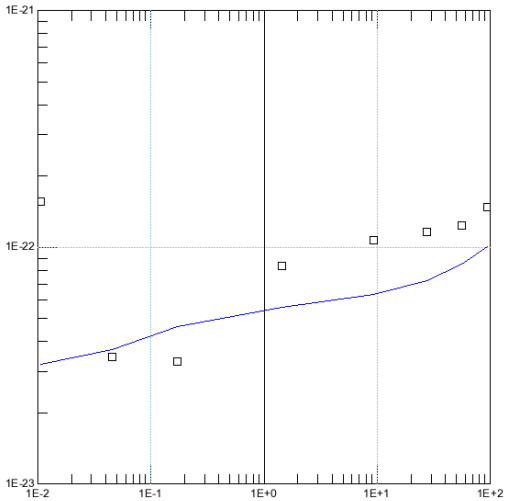
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 20Hz vs IC

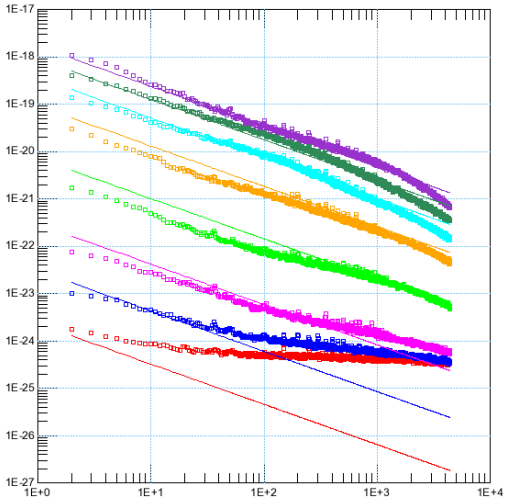


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 20Hz vs IC

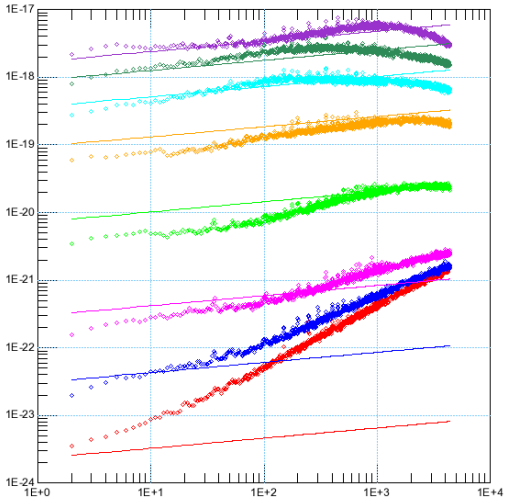


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 20Hz vs IC

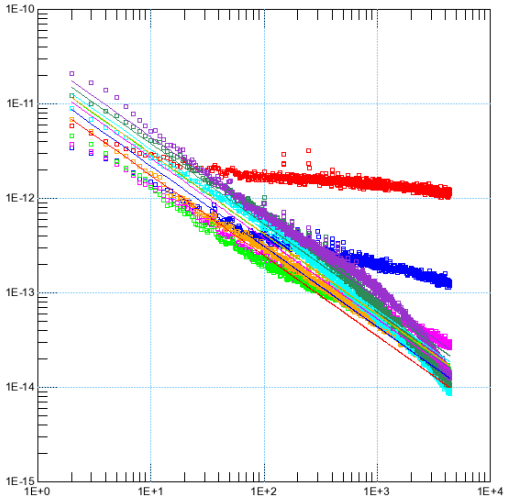
Figure 46: LVN W5μm L2μm at 25°C



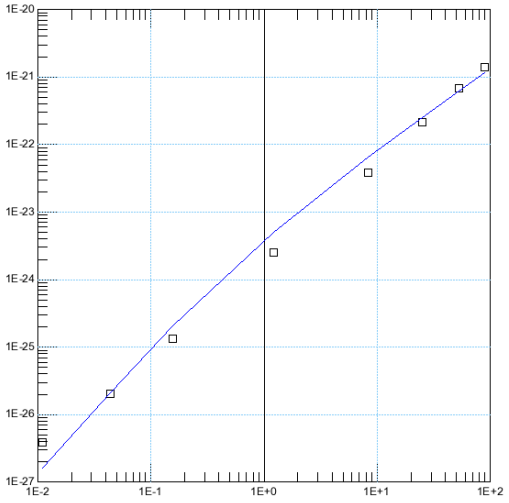
(a) S_{I_D} vs frequency



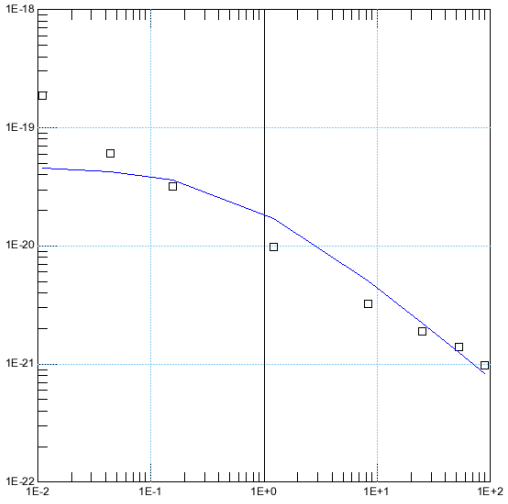
(b) $S_{I_D} \cdot f$ vs frequency



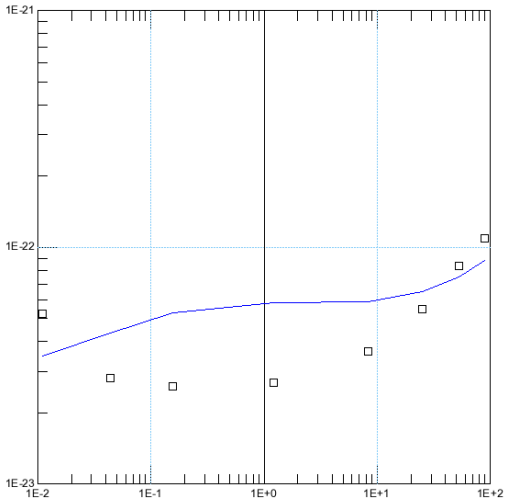
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 9Hz vs IC

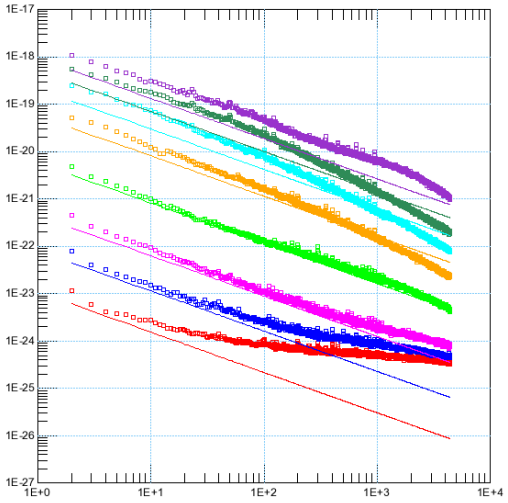


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 9Hz vs IC

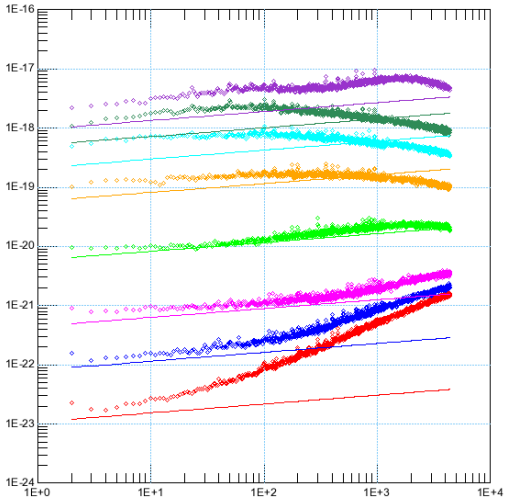


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 9Hz vs IC

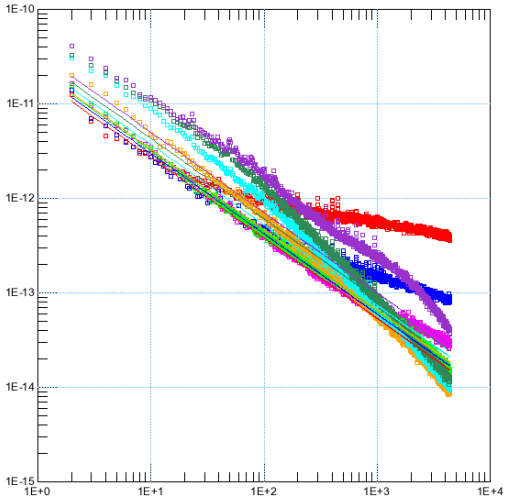
Figure 47: LVN W2μm L1μm at 25°C



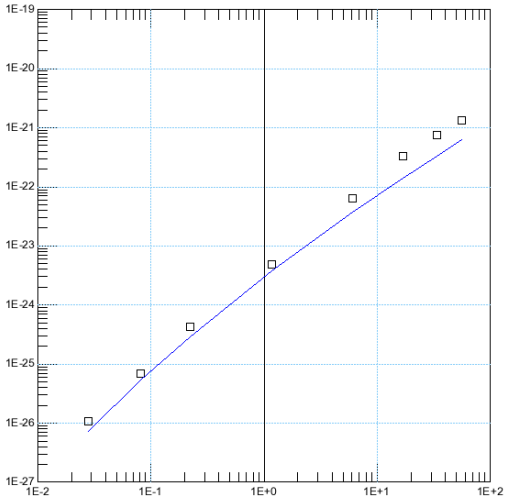
(a) S_{I_D} vs frequency



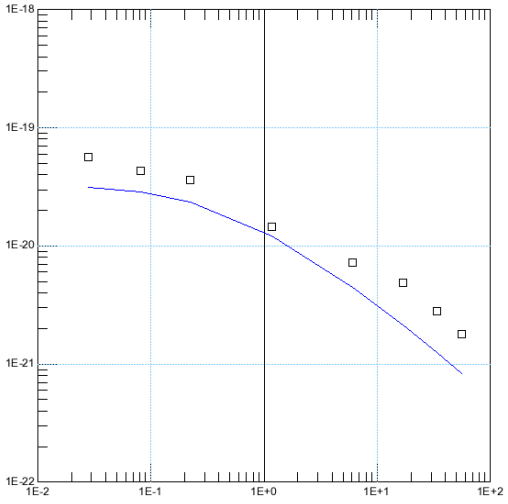
(b) $S_{I_D} \cdot f$ vs frequency



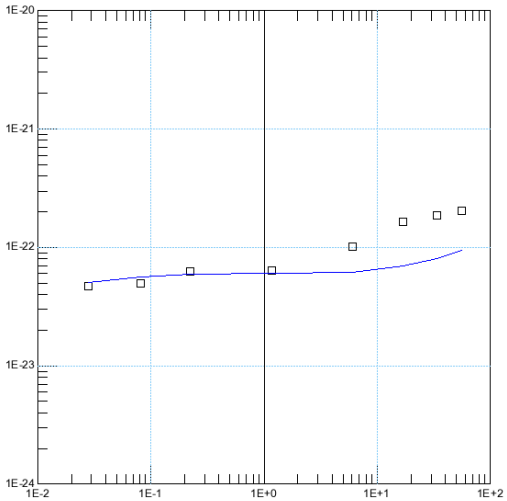
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 6.5Hz vs IC

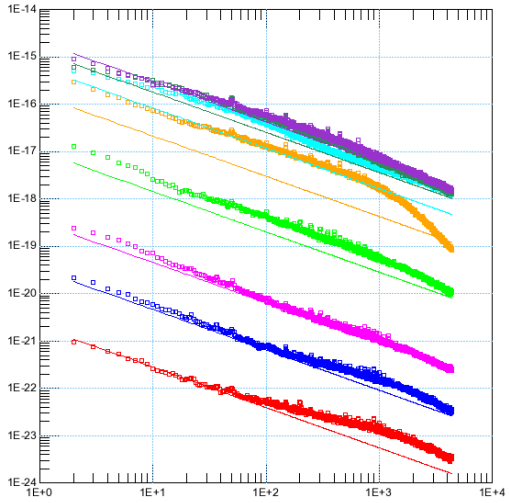


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 6.5Hz vs IC

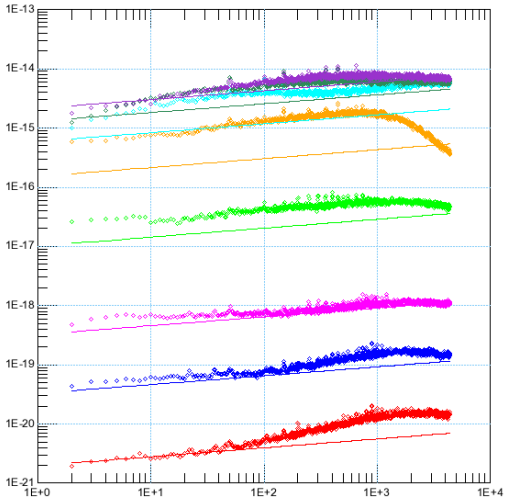


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 6.5Hz vs IC

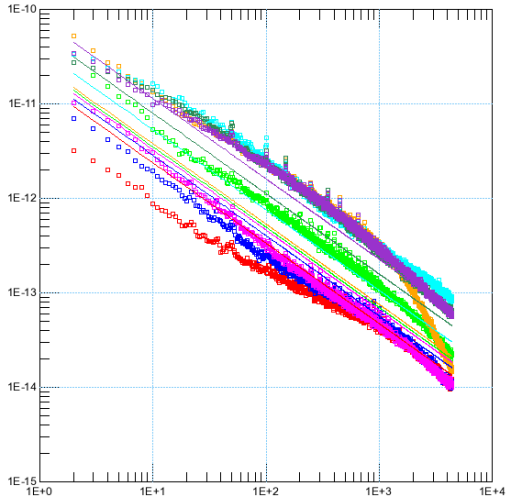
Figure 48: LVN W2μm L1μm at 125°C



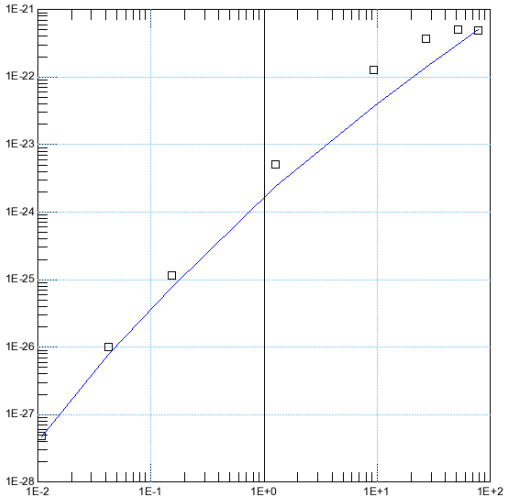
(a) S_{I_D} vs frequency



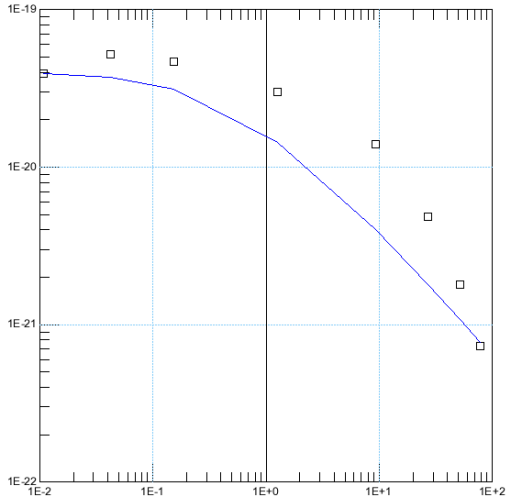
(b) $S_{I_D} \cdot f$ vs frequency



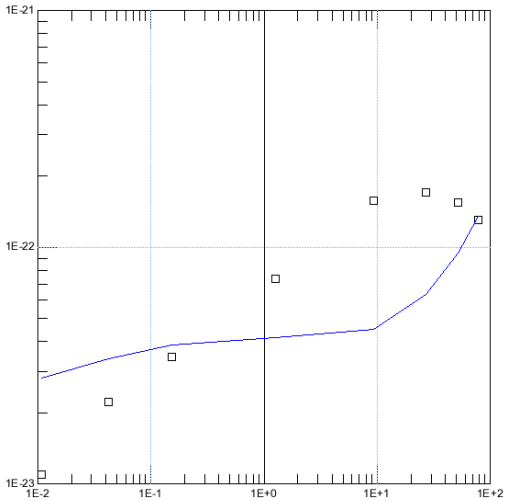
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 9Hz vs IC

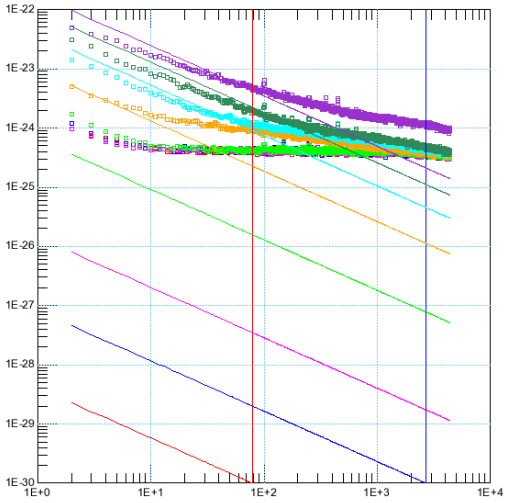


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 9Hz vs IC

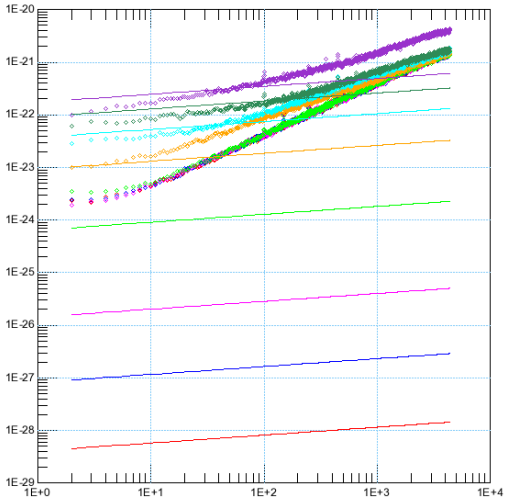


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 9Hz vs IC

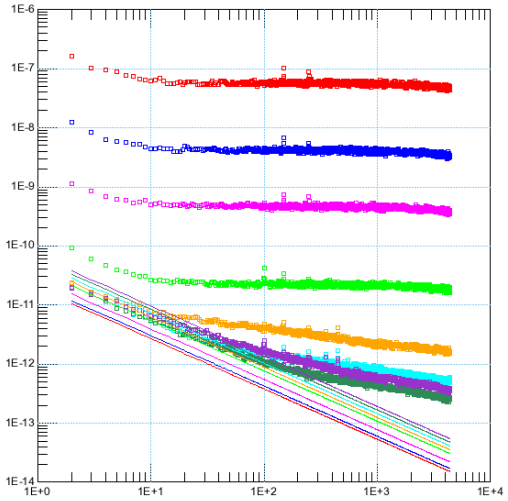
Figure 49: LVN W10μm L120nm at 25°C



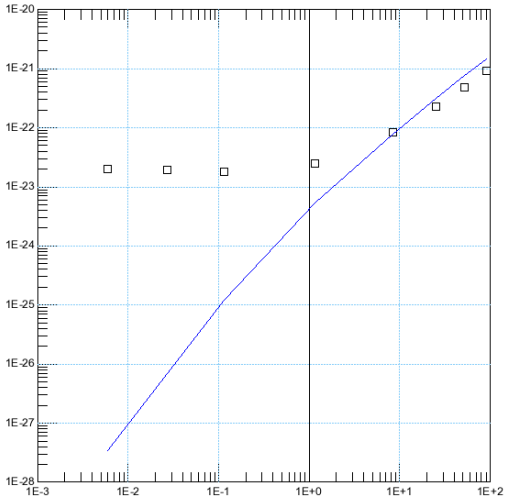
(a) S_{I_D} vs frequency



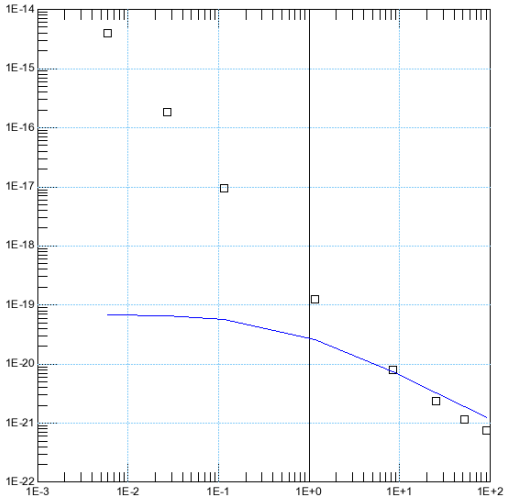
(b) $S_{I_D} \cdot f$ vs frequency



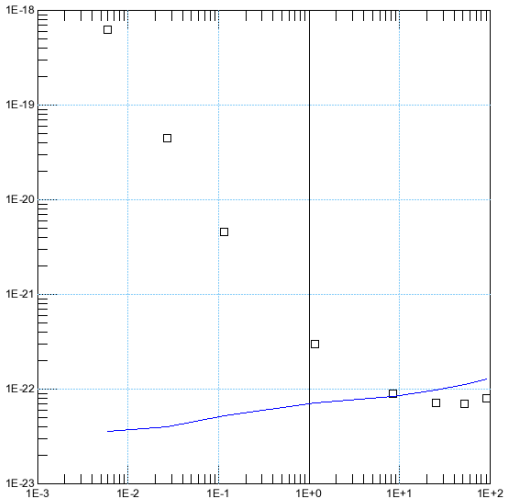
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 5Hz vs IC

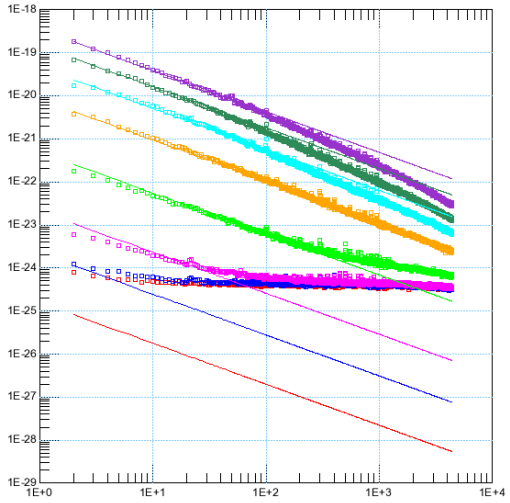


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 5Hz vs IC

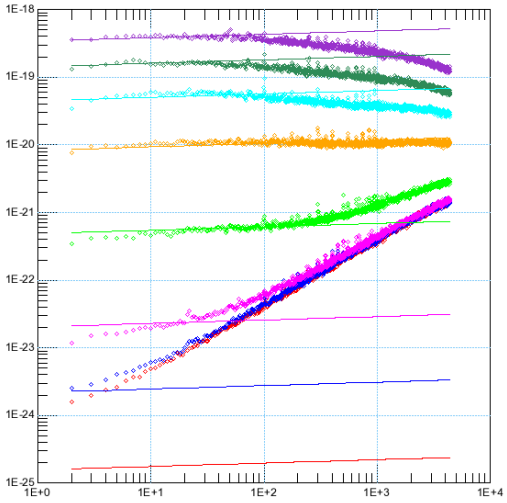


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 5Hz vs IC

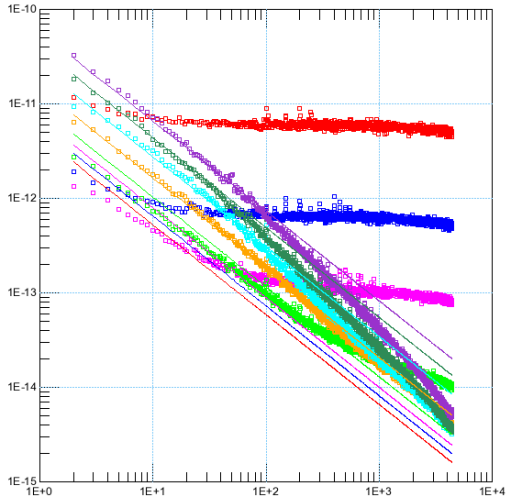
Figure 50: LVN W150nm L10μm at 25°C



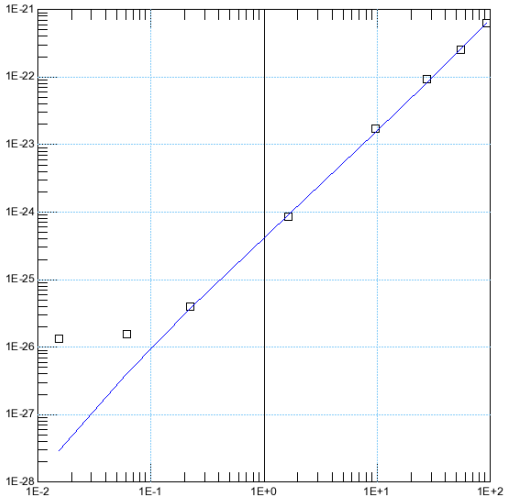
(a) S_{I_D} vs frequency



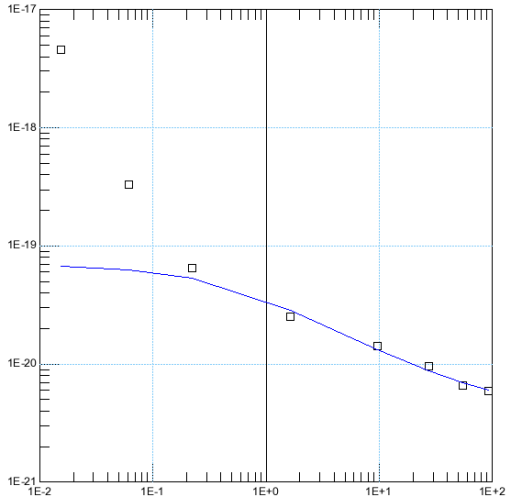
(b) $S_{I_D} \cdot f$ vs frequency



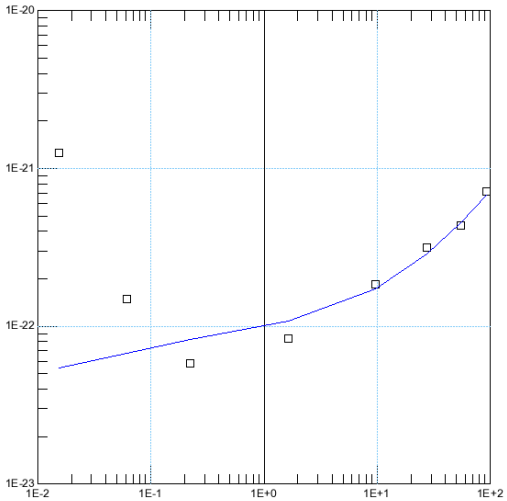
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 20Hz vs IC

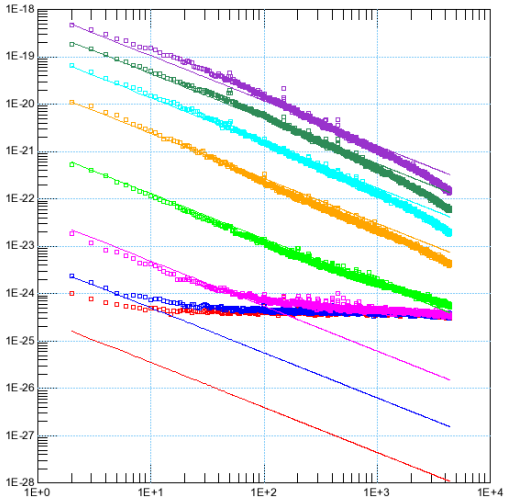


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 20Hz vs IC

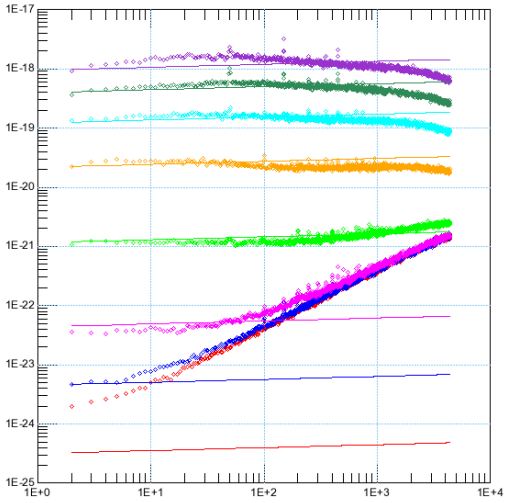


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 20Hz vs IC

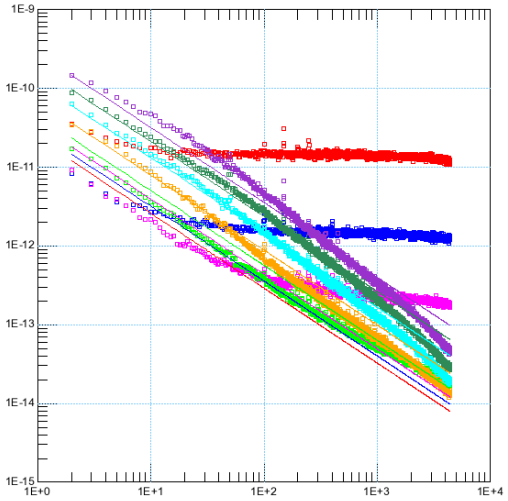
Figure 51: LVP W5μm L2μm at 25°C



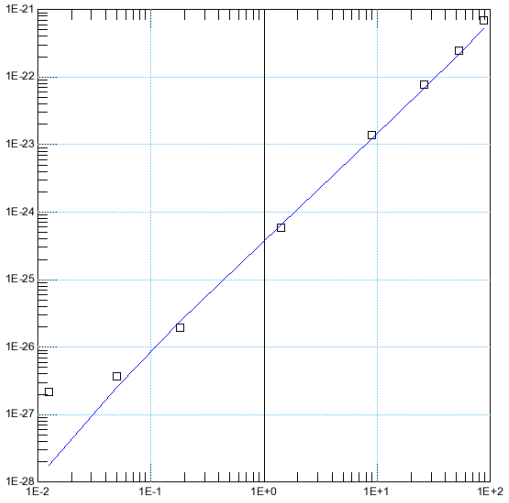
(a) S_{I_D} vs frequency



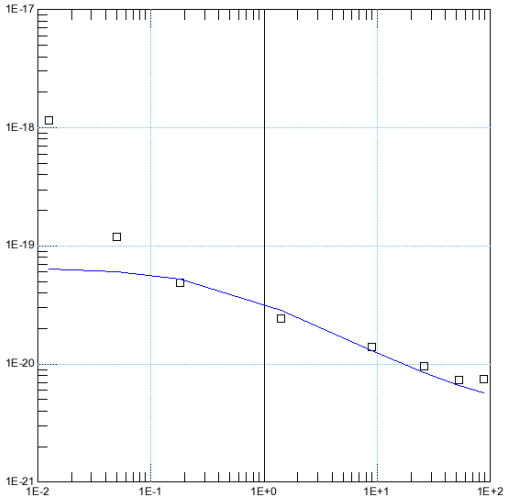
(b) $S_{I_D} \cdot f$ vs frequency



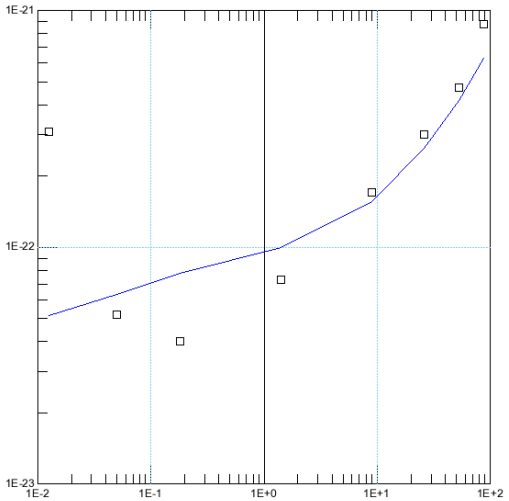
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 9Hz vs IC

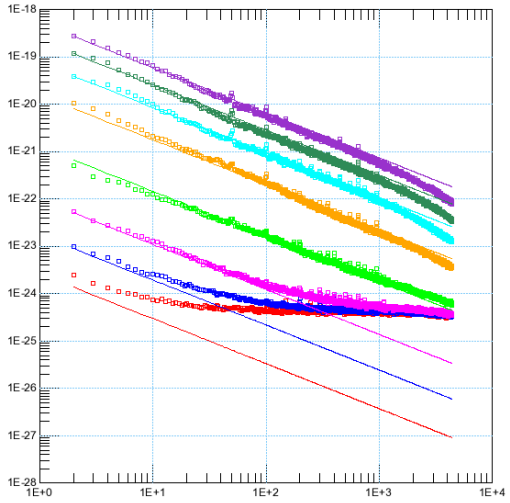


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 9Hz vs IC

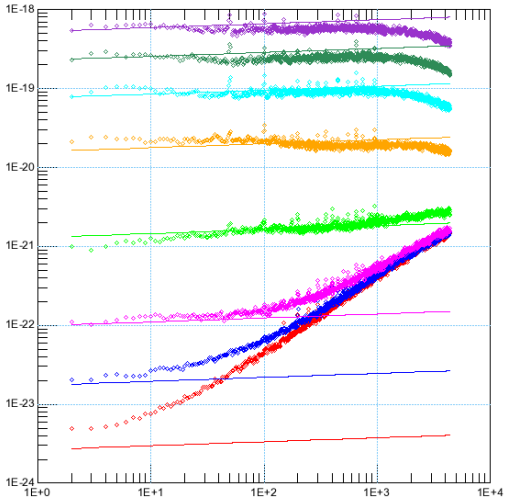


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 9Hz vs IC

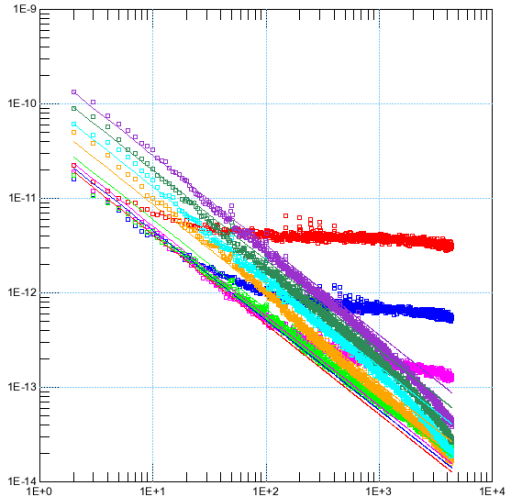
Figure 52: LVP W2μm L1μm at 25°C



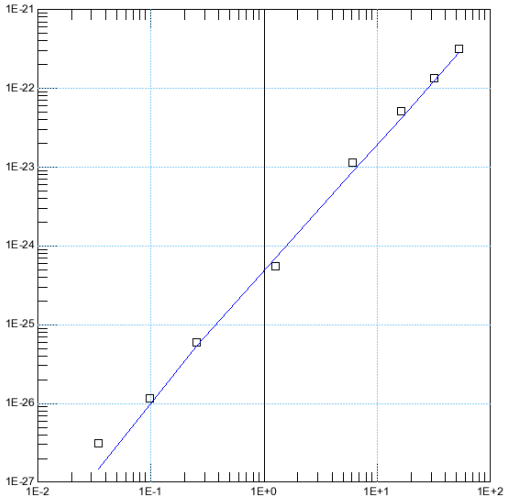
(a) S_{I_D} vs frequency



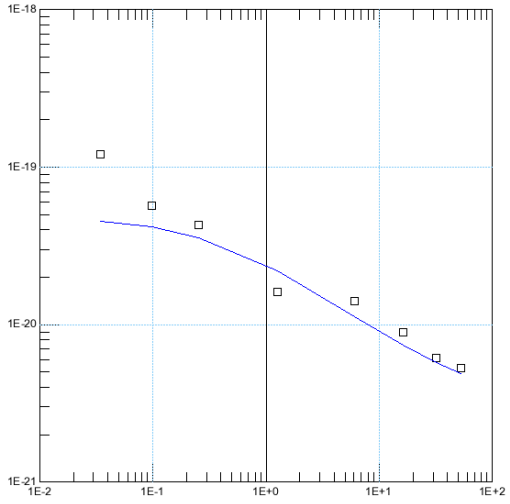
(b) $S_{I_D} \cdot f$ vs frequency



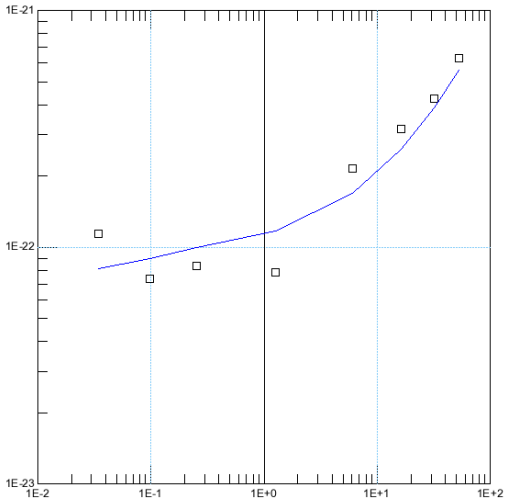
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 6.5Hz vs IC

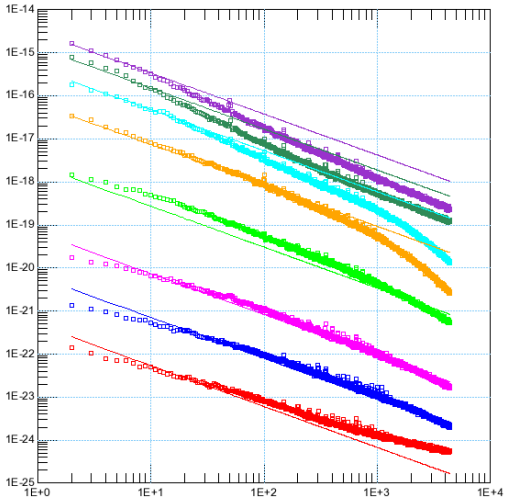


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 6.5Hz vs IC

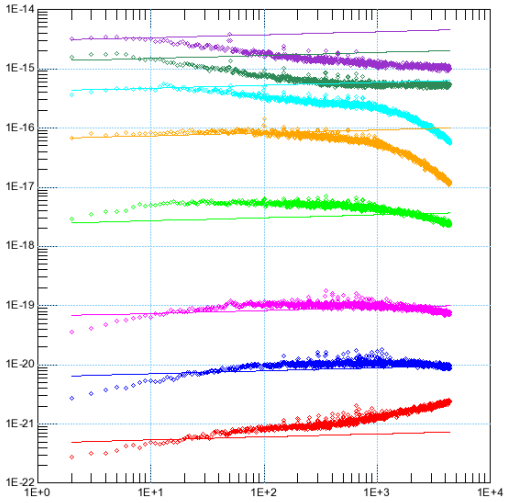


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 6.5Hz vs IC

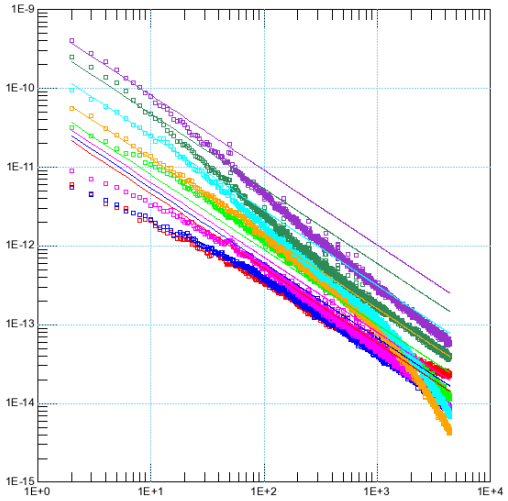
Figure 53: LVP W2μm L1μm at 125°C



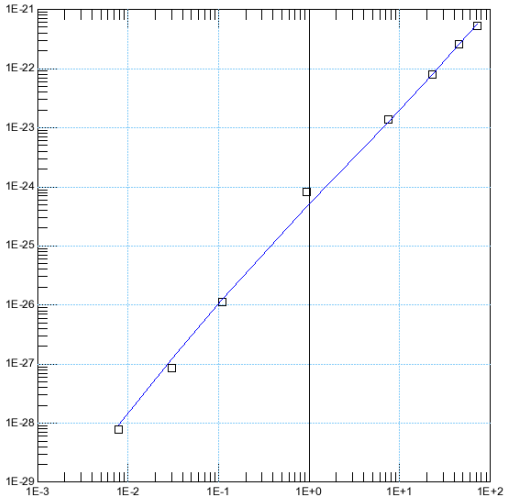
(a) S_{I_D} vs frequency



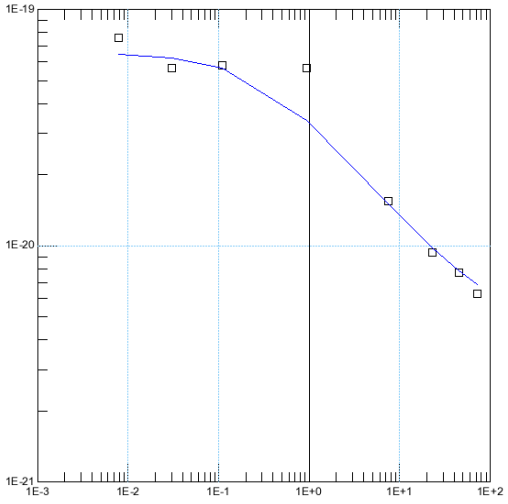
(b) $S_{I_D} \cdot f$ vs frequency



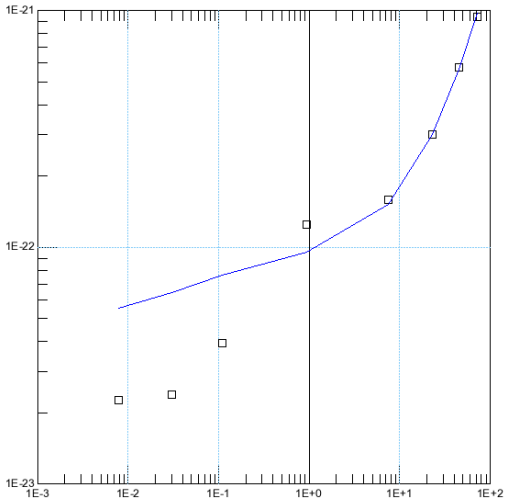
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 9Hz vs IC

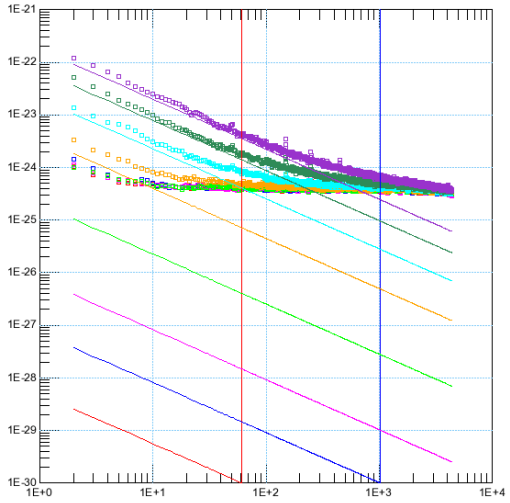


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 9Hz vs IC

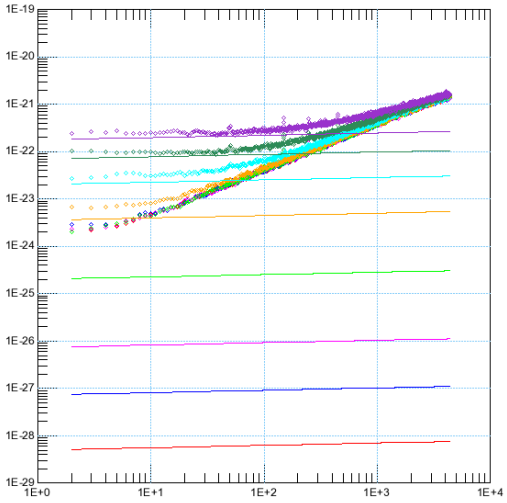


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 9Hz vs IC

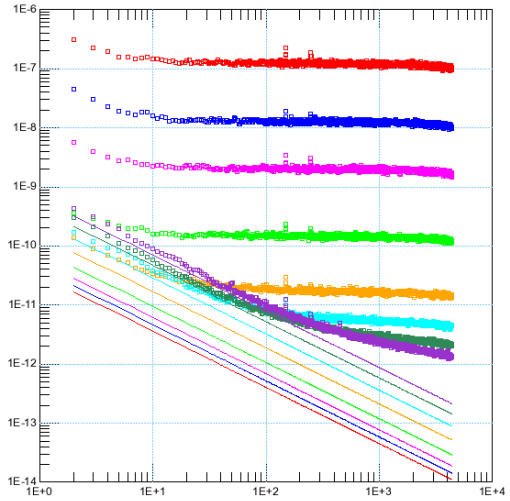
Figure 54: LVP W10μm L120nm at 25°C



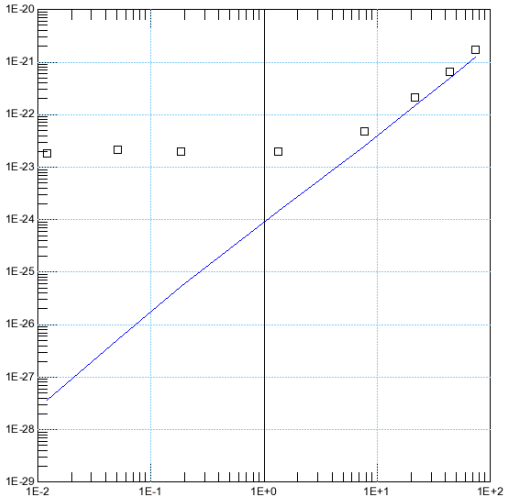
(a) S_{I_D} vs frequency



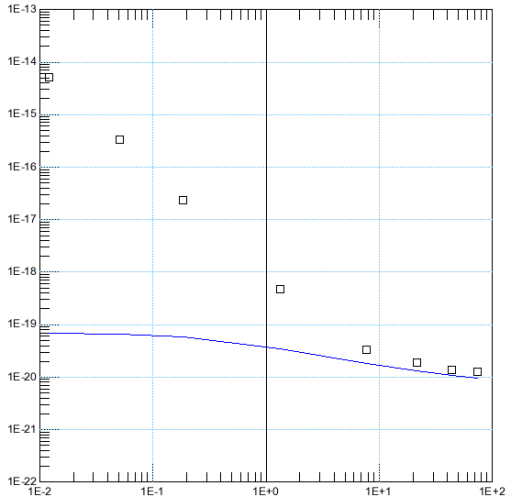
(b) $S_{I_D} \cdot f$ vs frequency



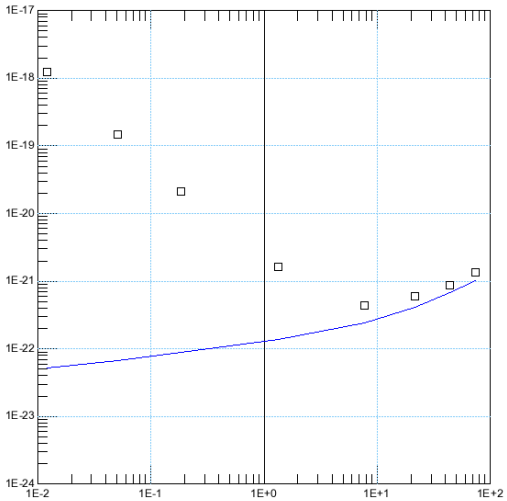
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 5Hz vs IC

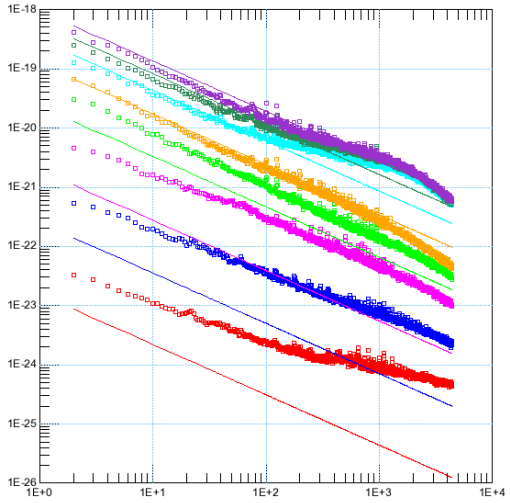


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 5Hz vs IC

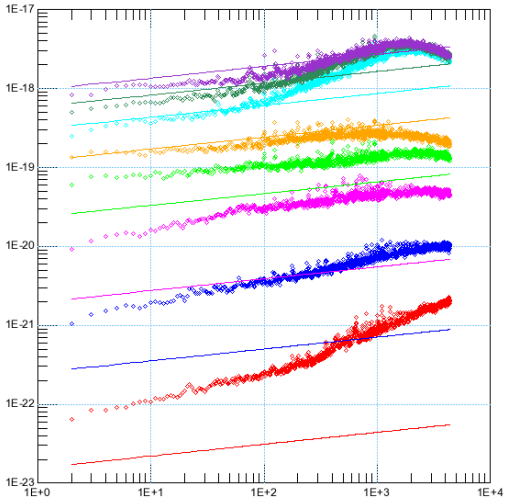


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 5Hz vs IC

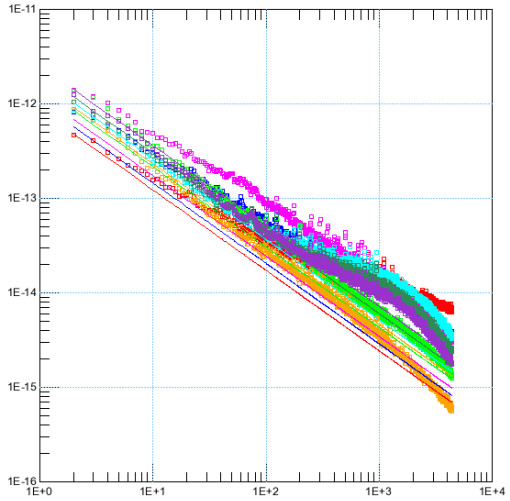
Figure 55: LVP W150nm L10μm at 25°C



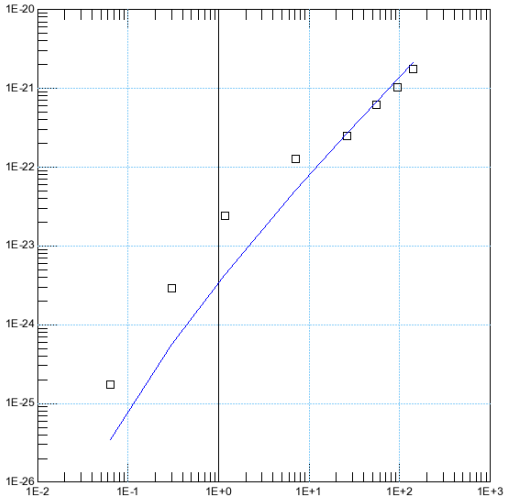
(a) S_{I_D} vs frequency



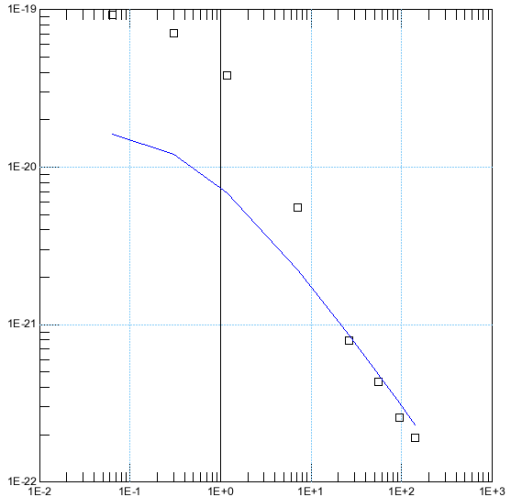
(b) $S_{I_D} \cdot f$ vs frequency



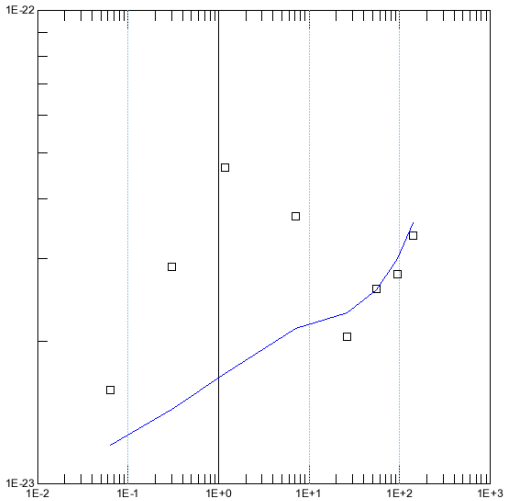
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 9Hz vs IC

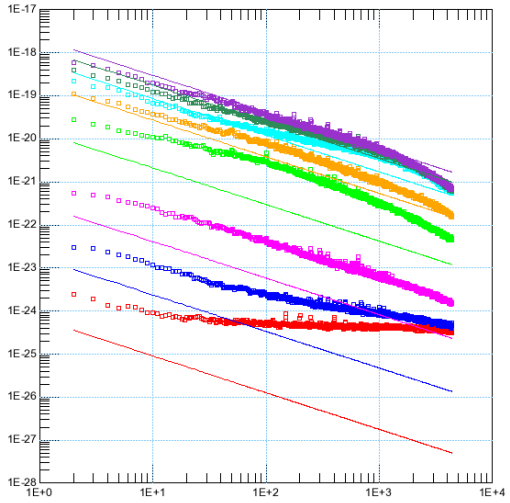


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 29Hz vs IC

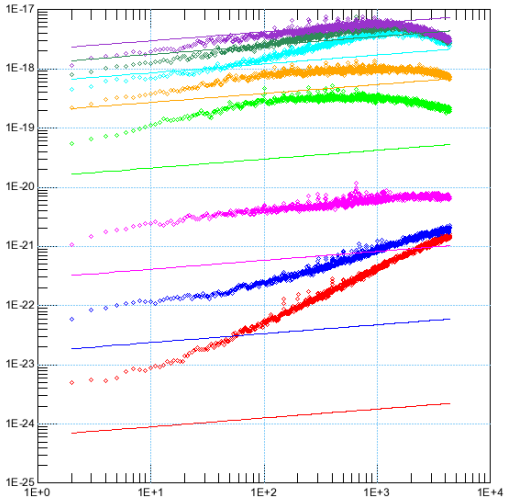


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 9Hz vs IC

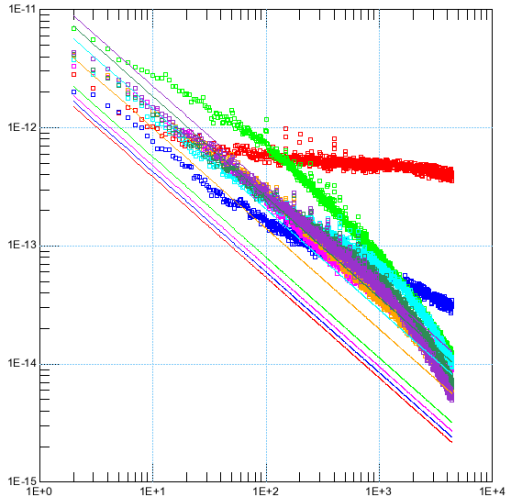
Figure 56: LVN Native W5μm L2μm at 25°C



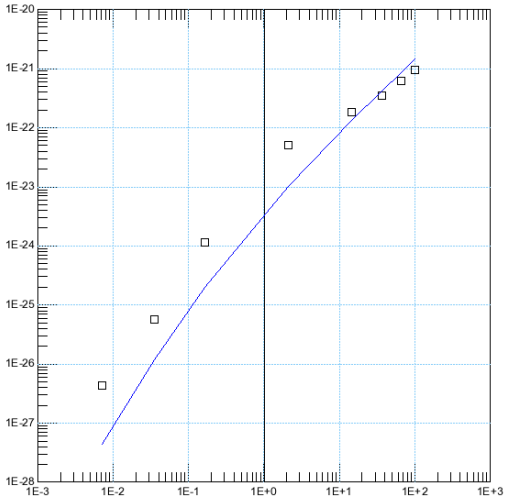
(a) S_{I_D} vs frequency



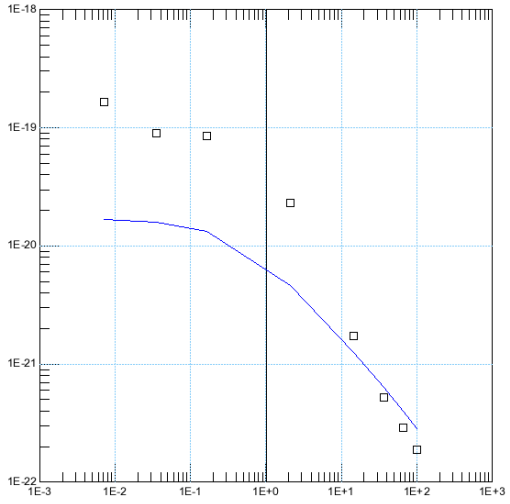
(b) $S_{I_D} \cdot f$ vs frequency



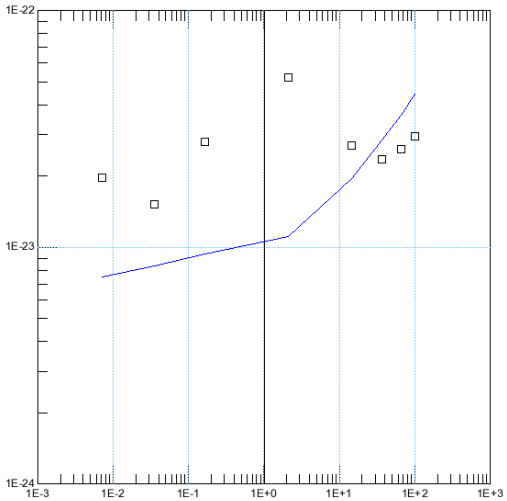
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 9Hz vs IC

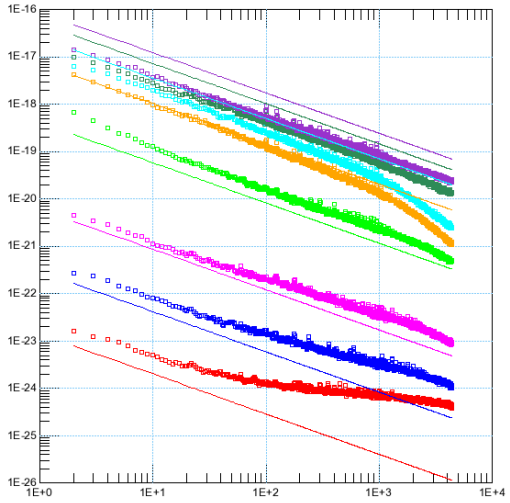


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 9Hz vs IC

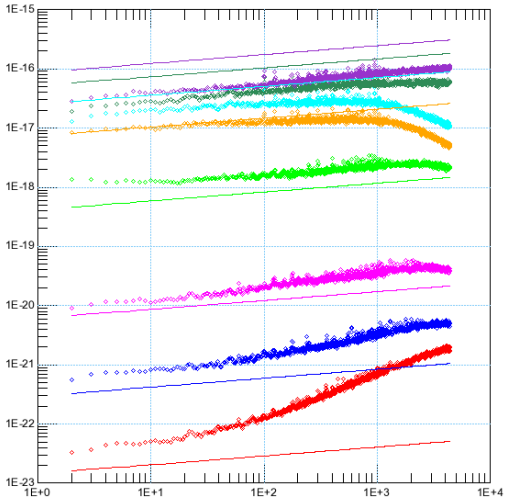


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 9Hz vs IC

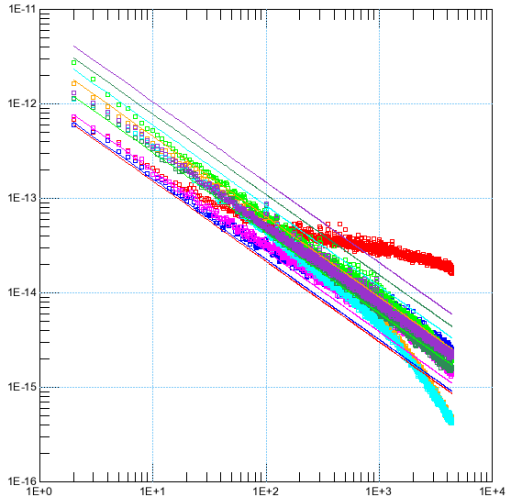
Figure 57: LVN Native W2μm L1μm at 25°C



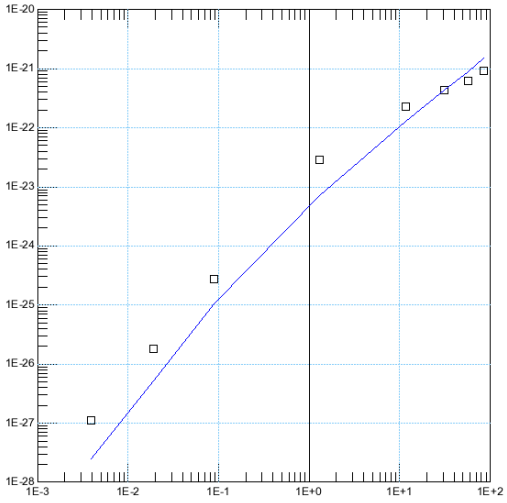
(a) S_{I_D} vs frequency



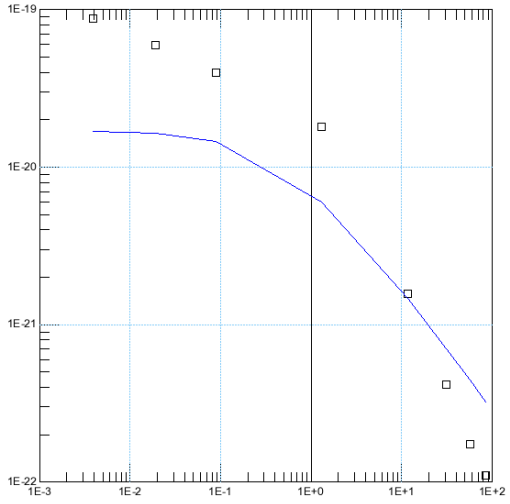
(b) $S_{I_D} \cdot f$ vs frequency



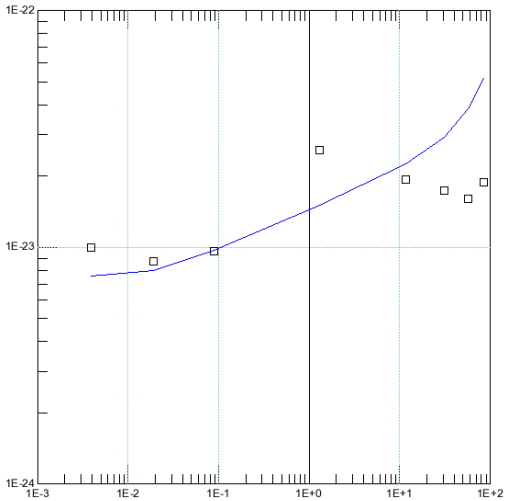
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 9Hz vs IC

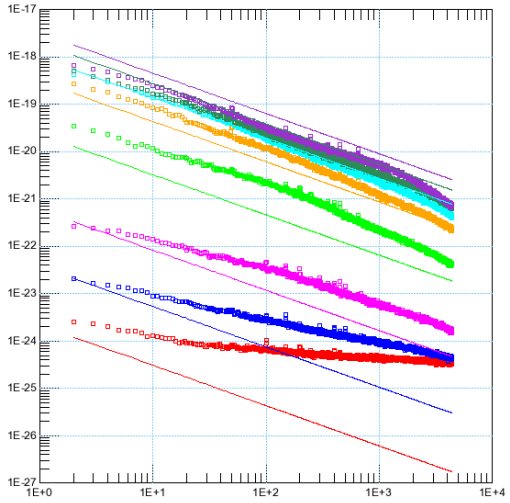


(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 9Hz vs IC

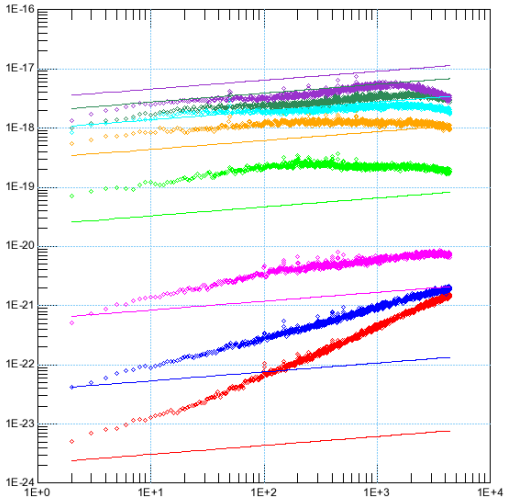


(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 9Hz vs IC

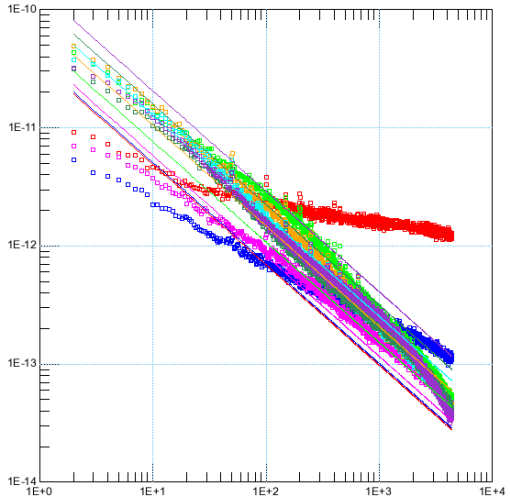
Figure 58: LVN Native W10μm L150nm at 25°C



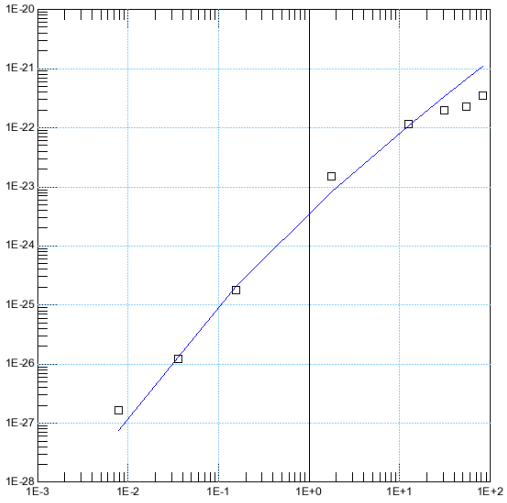
(a) S_{I_D} vs frequency



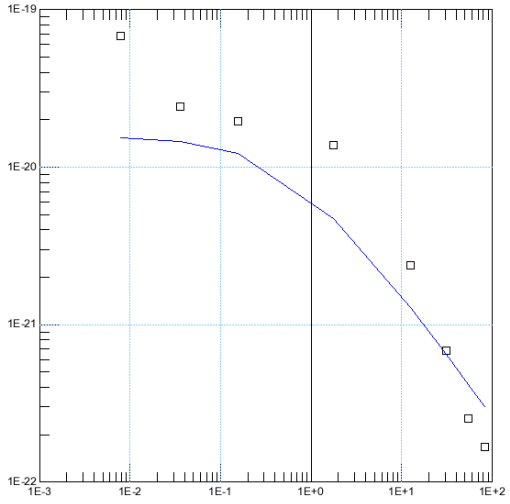
(b) $S_{I_D} \cdot f$ vs frequency



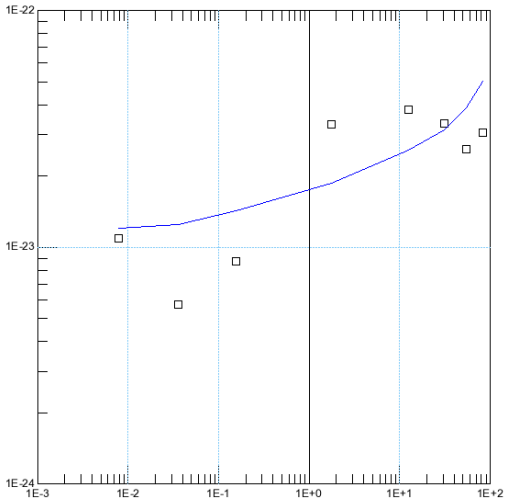
(c) S_{V_G} vs frequency



(d) $S_{I_D} \cdot f \cdot \frac{L^3}{W}$ at 9Hz vs IC



(e) $\frac{S_{I_D}}{I_D^2} \cdot f \cdot W \cdot L$ at 9Hz vs IC



(f) $S_{V_G} \cdot f \cdot W \cdot L$ at 9Hz vs IC

Figure 59: LVN Native W500nm L500nm at 25°C

4.7 Discussion

From the analytical approach, one can glean basic information about the measured devices. Some first observations confirm the theoretical predictions, i.e. P-type devices have lower noise levels than N-type, with native devices coming in between, closer to the standard N-type. We can also confirm that the dominant noise source is the trapping-detrapping of channel current carriers (number fluctuation) as the measurements can be satisfactorily modelled by using only this effect. A definitive Hooge effect is not apparent in any of the devices, hence the omission of its contribution in the analytical model. If such an effect was present, the telltale signature would be that the $\frac{S_{I_D}}{I_D^2}$ vs IC plots (plots "e") would have an upward trend for the lower inversion levels. It should be noted that this *appears* to be the case for some devices, however the reason for this is the noise floor of the measurement system preventing us form having reliable data at the lowest inversion levels, which becomes readily apparent from the S_{I_D} spectrum (plots "a"). By examining the extracted parameters we can also confirm that P-type devices have a more textbook 1/f noise response, as their "af" parameter is closer to unity than for N-type devices. The other two parameters, a_c and N_T appear to have values in the expected range, $N_T \approx 10^{41}$ and $a_c \approx 10^5$ for P-type and $\approx 10^4$ for N-type, though for the latter, the extracted parameter value is rather low. As a_c and N_T work together, a direct comparison can only be made for the N-type and native devices that have similar a_c parameters. There the lower N_T parameter value for the native devices directly reflects the lower noise levels recorded. The P-type devices seem to be closer to the behaviour expected by the model than their N-type counterparts, as can be seen by the better model fit.

Focusing on the short device geometry (W10μm L120nm in LVN and LVP, W10μm L500nm in LVN Native) we can observe that the N-type devices exhibit a downward trend towards the higher inversion levels, which the model cannot follow accurately. P-type devices on the contrary do not exhibit this behaviour. This is easily attributed to the carrier velocity saturation effect which is mostly apparent in short devices. NMOS are known to suffer more from it than PMOS and that is also evident in our noise measurements. Since the λ_C parameter for the channel length modulation and velocity saturation effects was not used, the model's response is not expected to match the measurements precisely. Due to these effects, the parameters were extracted for a better fit of the larger devices (W5μm L2μm and W2μm L1μm), trading-off performance at the shorter geometries. Two more observations can be made, as well. Native N-type devices exhibit less strong short channel effects, with lower overall noise levels (also attributed to the halo implants, which will be discussed on their own) and also the form of the $\frac{S_{I_D}}{I_D^2}$ plot resembles most the theoretical curve form, which is the form of the $\frac{g_m}{I_D}$ curve, while in all other geometries, such behaviour is not observed.

Regarding the narrow devices (W150nm L10μm in LVN and LVP) not much can be observed, apart from a good model fit at strong inversion, owing to the absence of usable measurements for LVN and LVP. The native device (W500nm L500nm), having a shorter channel however, has increased noise levels, allowing us to observe a different frequency dependence ("af" parameter bias dependence) for lower inversion levels, which reverts to the longer and wider channel value above moderate inversion.

By examining the noise response of the W2μm L1μm device at $25°C$ vs $125°C$ we can discern that noise levels increase only for the weaker inversion levels, while for strong inversion they remain the same for LVN, even dropping a little for LVP. As for the model, it is in good agreement at the elevated temperature for both LVN and LVP that were measured.

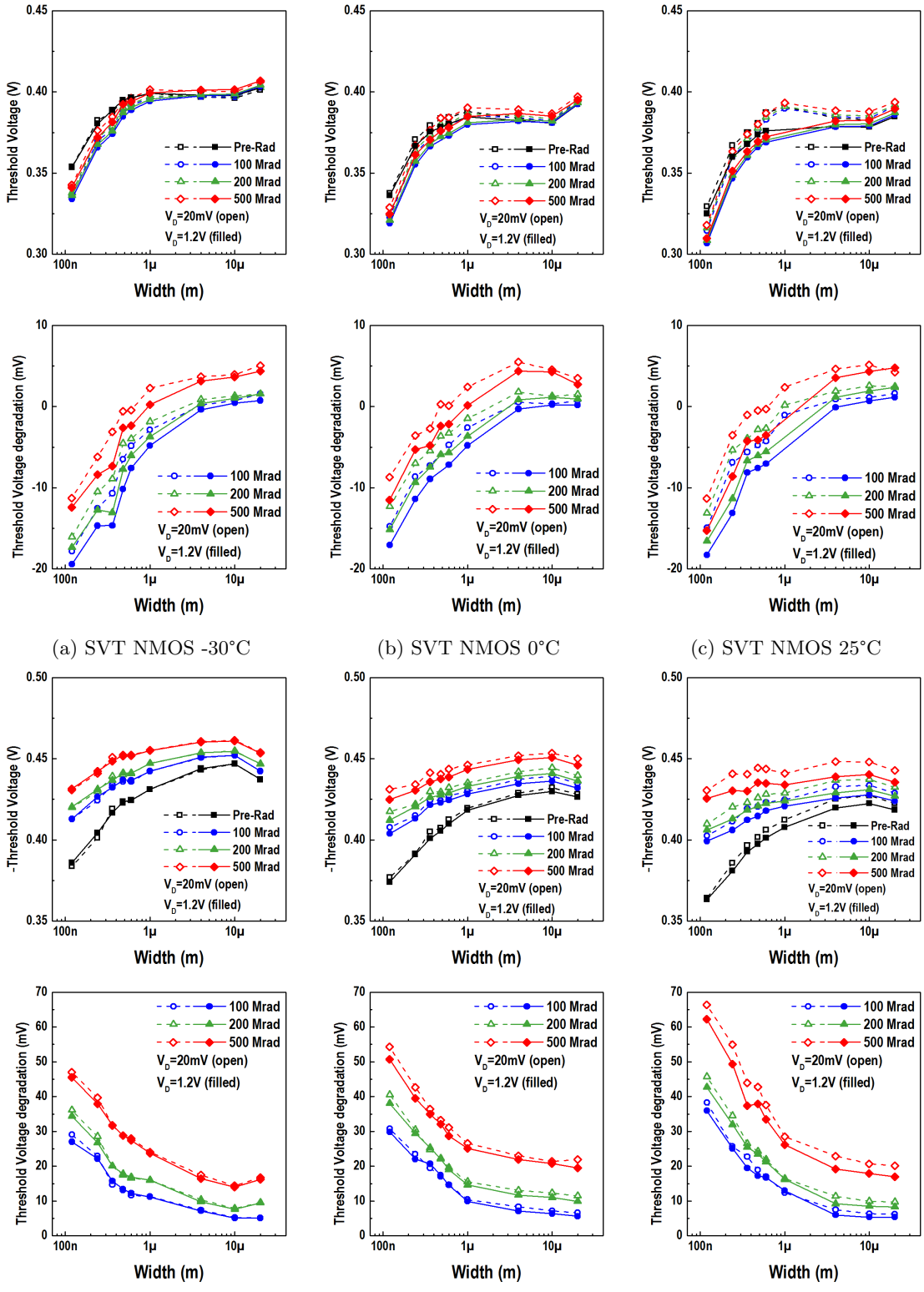
Finally, we seem to have uncovered a very interesting behaviour, linked to the effect of halo (or "pocket") implants as described in [1]. This can be observed in all our Native devices but most clearly in the W5μm L2μm and W2μm L1μm geometries. For the W10μm L500nm device, it is probable that with such a short channel length, the halo implants come very close, probably even overlap, thus hiding this effect. Morphologically, it can be summed up as a sort of step in the $S_{I_D} \cdot f$ vs IC plot. For lower inversion levels the curve exhibits a fixed slope, which at the onset

of strong inversion suddenly changes to a lower value and then reverts back, close to its original value, resulting in an inverted "S" shaped curve. This has been considered to be a signature of the halo implantation, as halo regions exhibit higher trap density, resulting in non-uniform noise production along the length of the channel. As these devices have otherwise no channel doping, this phenomenon becomes readily apparent.

A Additional TID scaling plots

A.1 Width Scaling, Length=10μm, at -30°, 0°, 25°C, SVT devices

A.1.1 Threshold Voltage Width Scaling

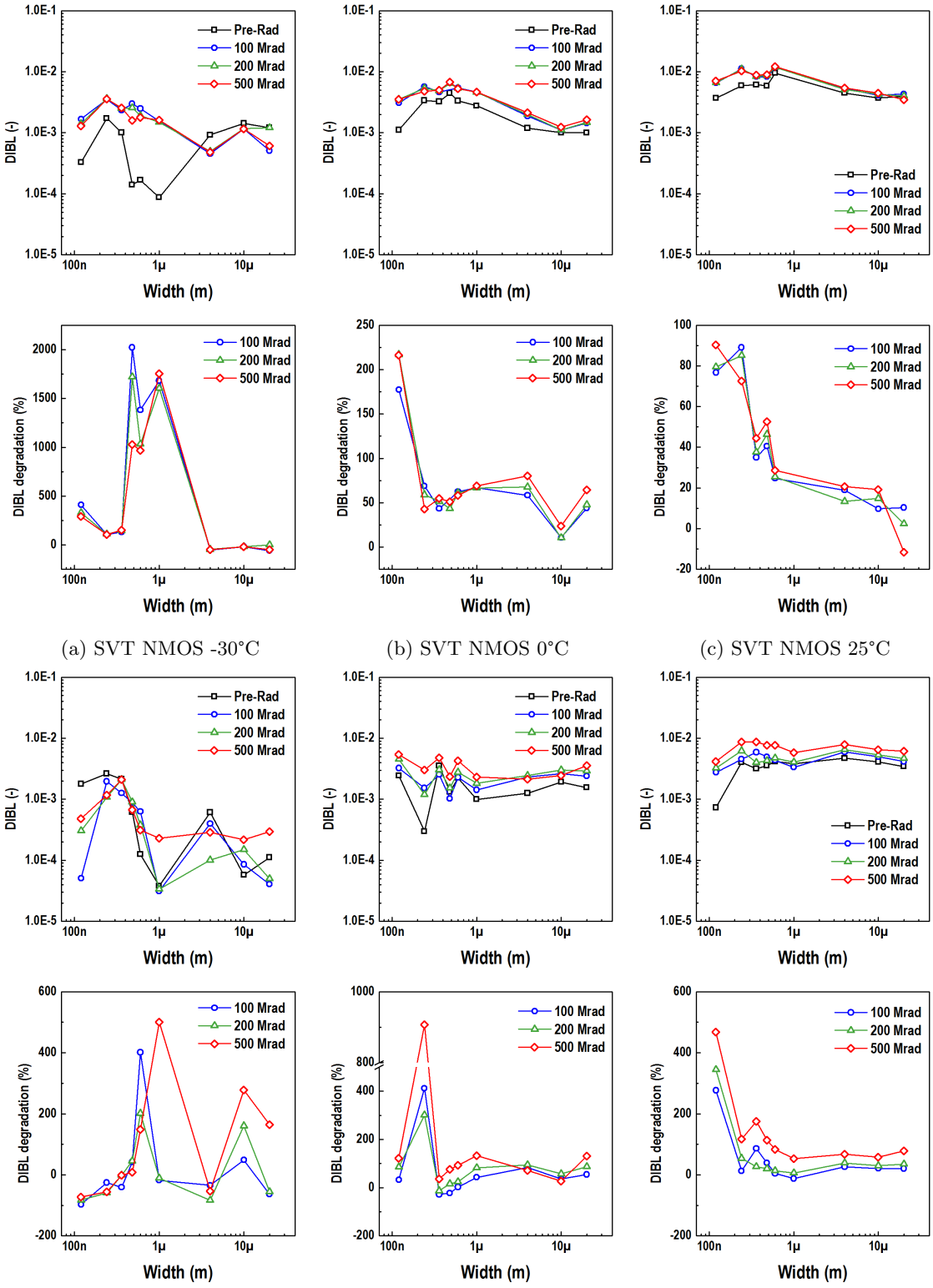


(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 60: V_{TH} and degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

A.1.2 DIBL Factor Width Scaling

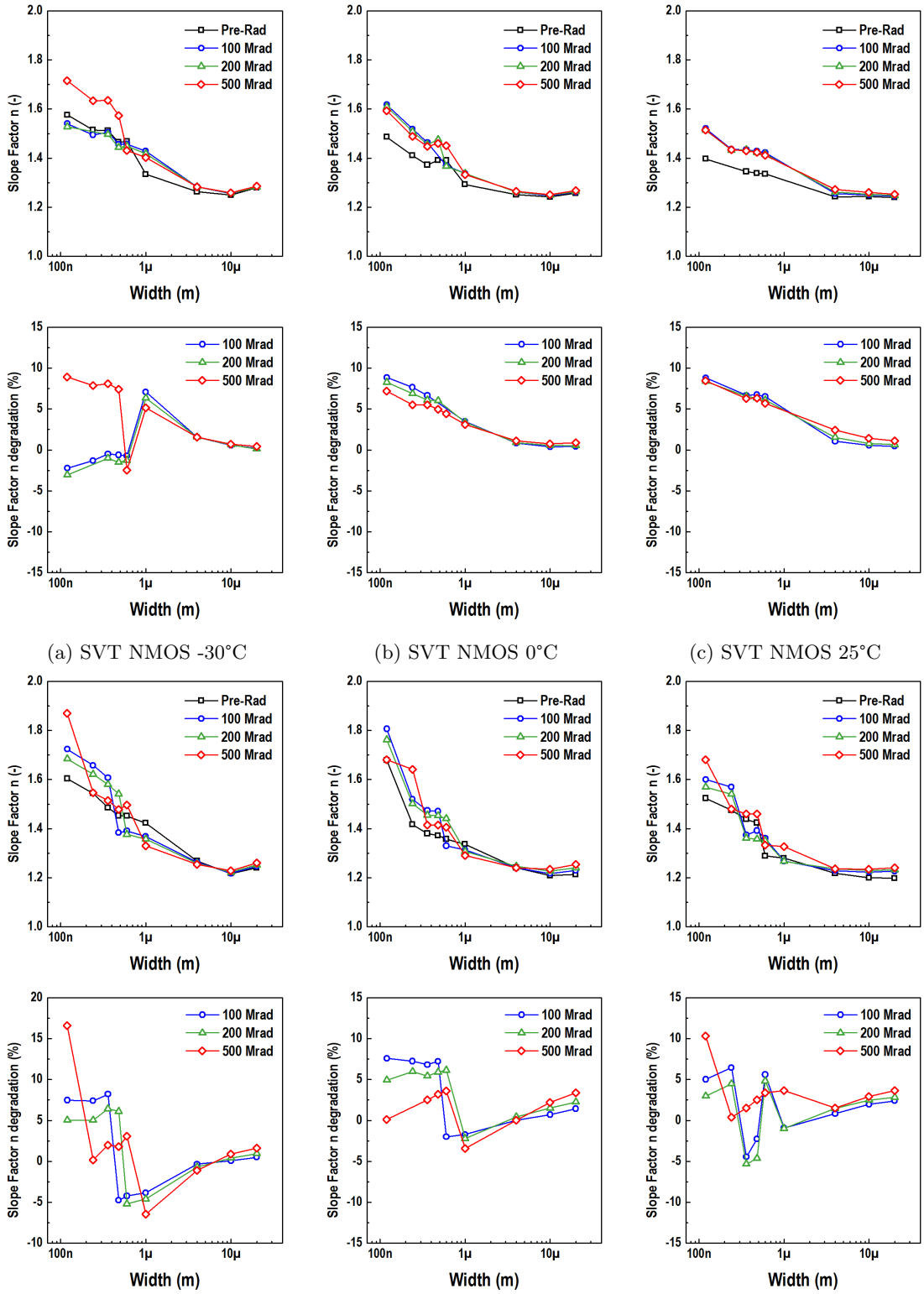


(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 61: DIBL and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

A.1.3 WI Slope Factor Width Scaling

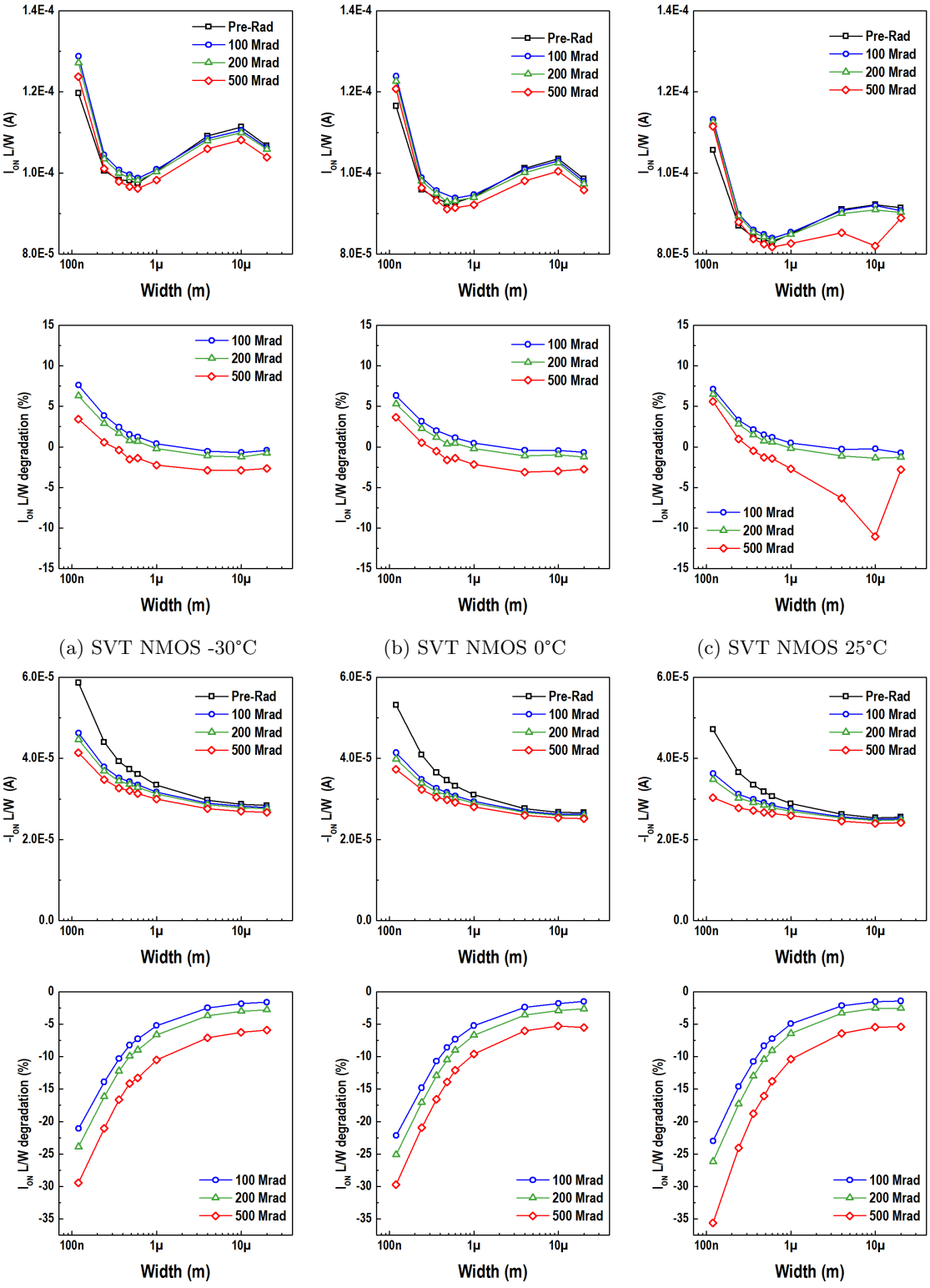


(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 62: Weak inversion slope factor and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

A.1.4 On-Current Width Scaling

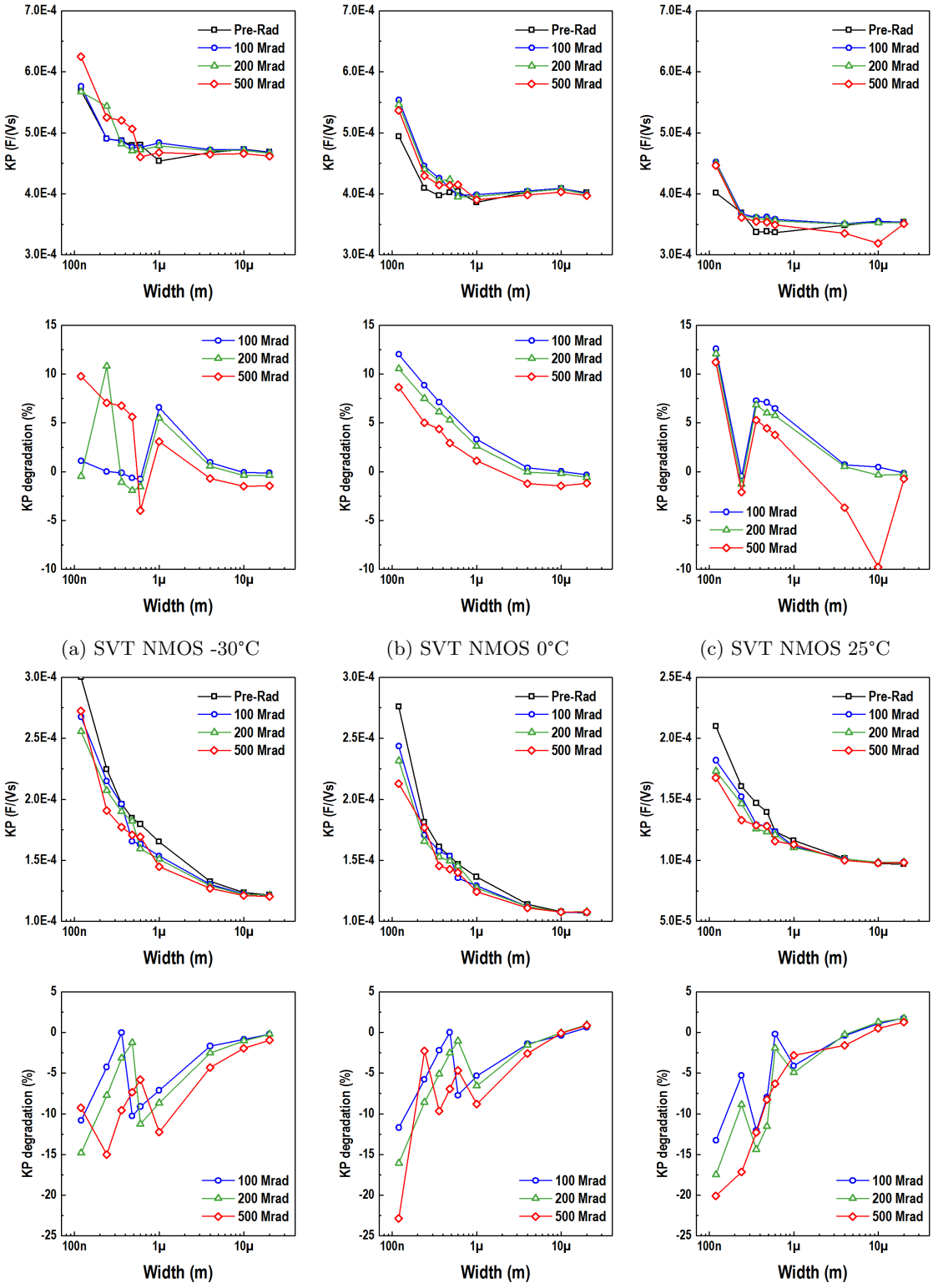


(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 63: On-state current normalised by $\frac{L}{W}$ and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

A.1.5 KP Width Scaling

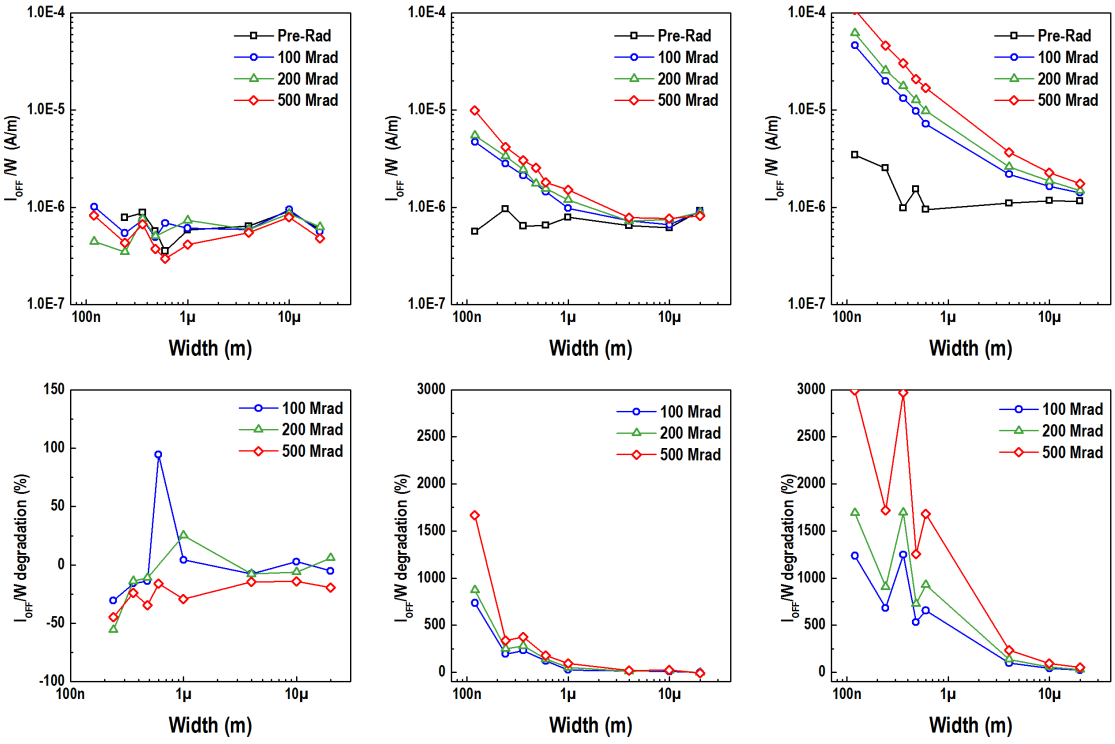


(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

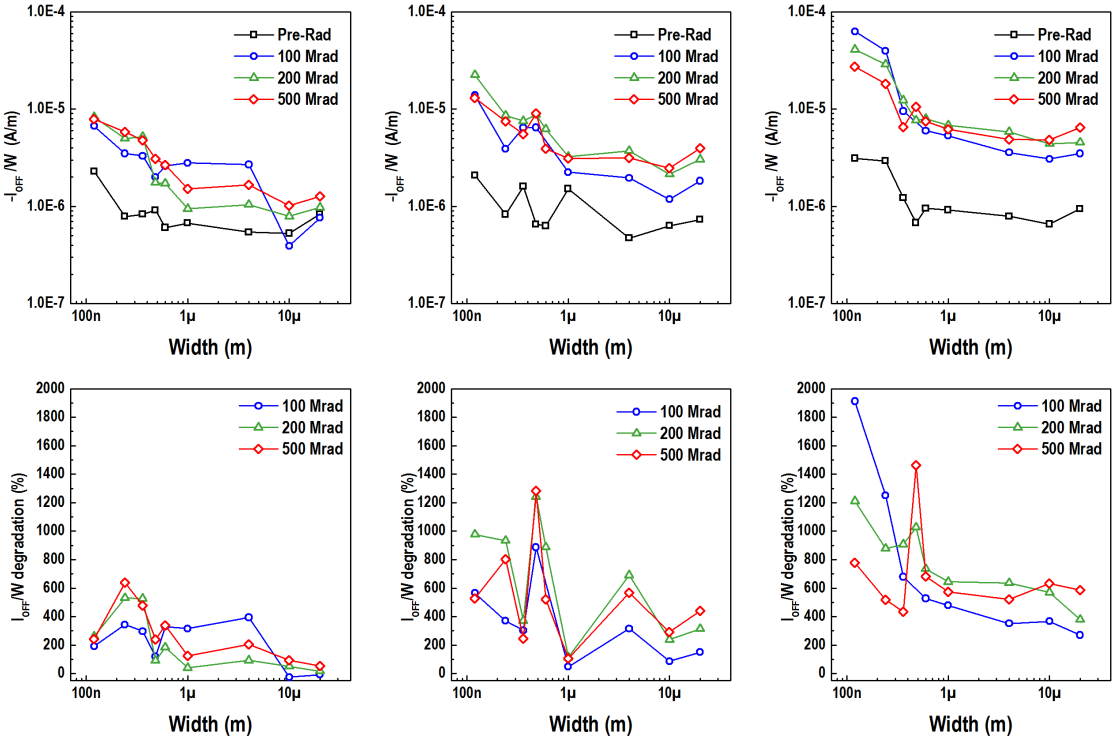
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 64: Transconductance factor ($KP = \mu * C'_{OX}$) and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

A.1.6 Leakage Current Width Scaling



(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

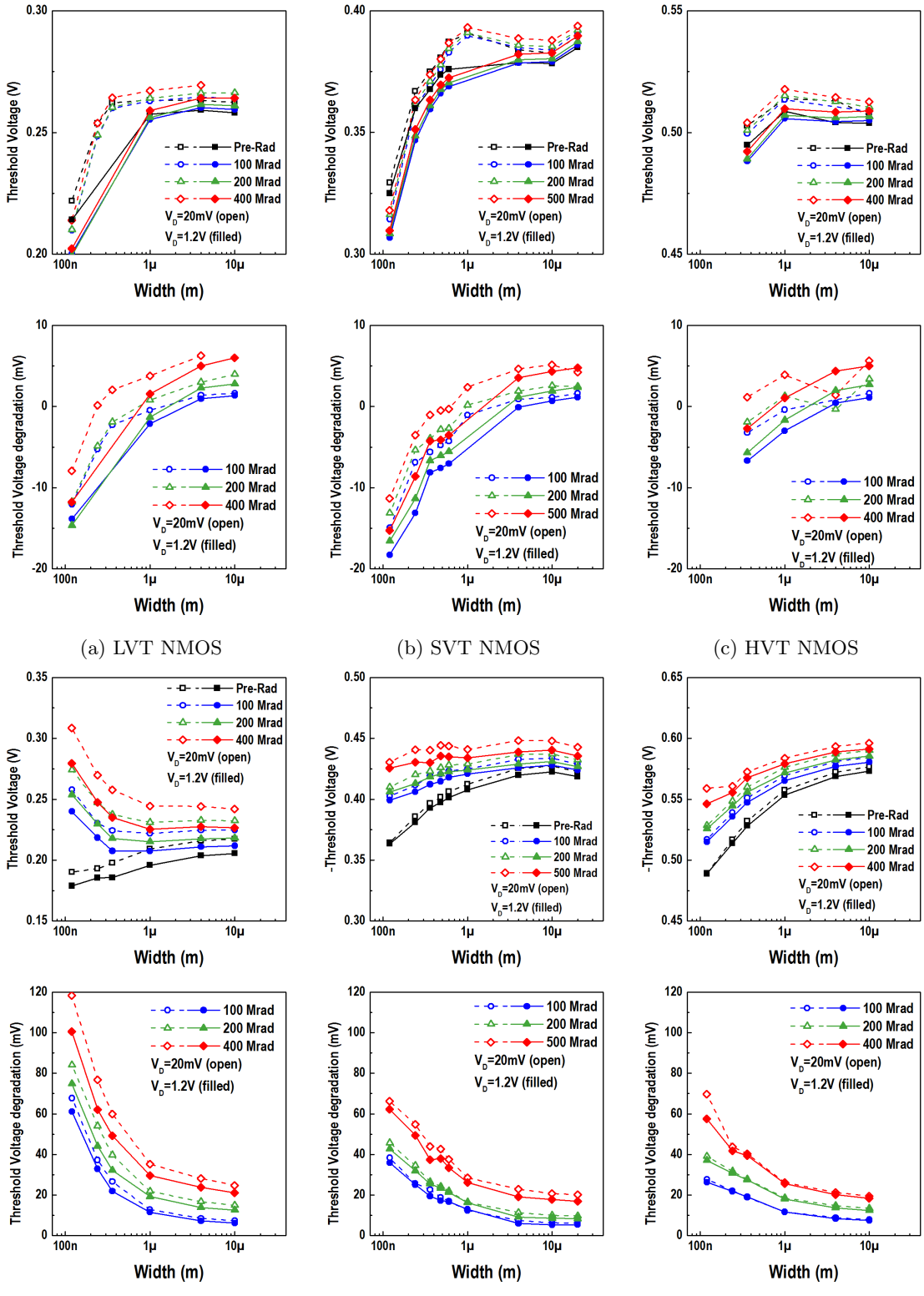


(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 65: Leakage current normalised by $\frac{1}{W}$ and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

A.2 Width Scaling, Length=10μm, at 25°C, LVT, SVT, HVT devices

A.2.1 Threshold Voltage Width Scaling

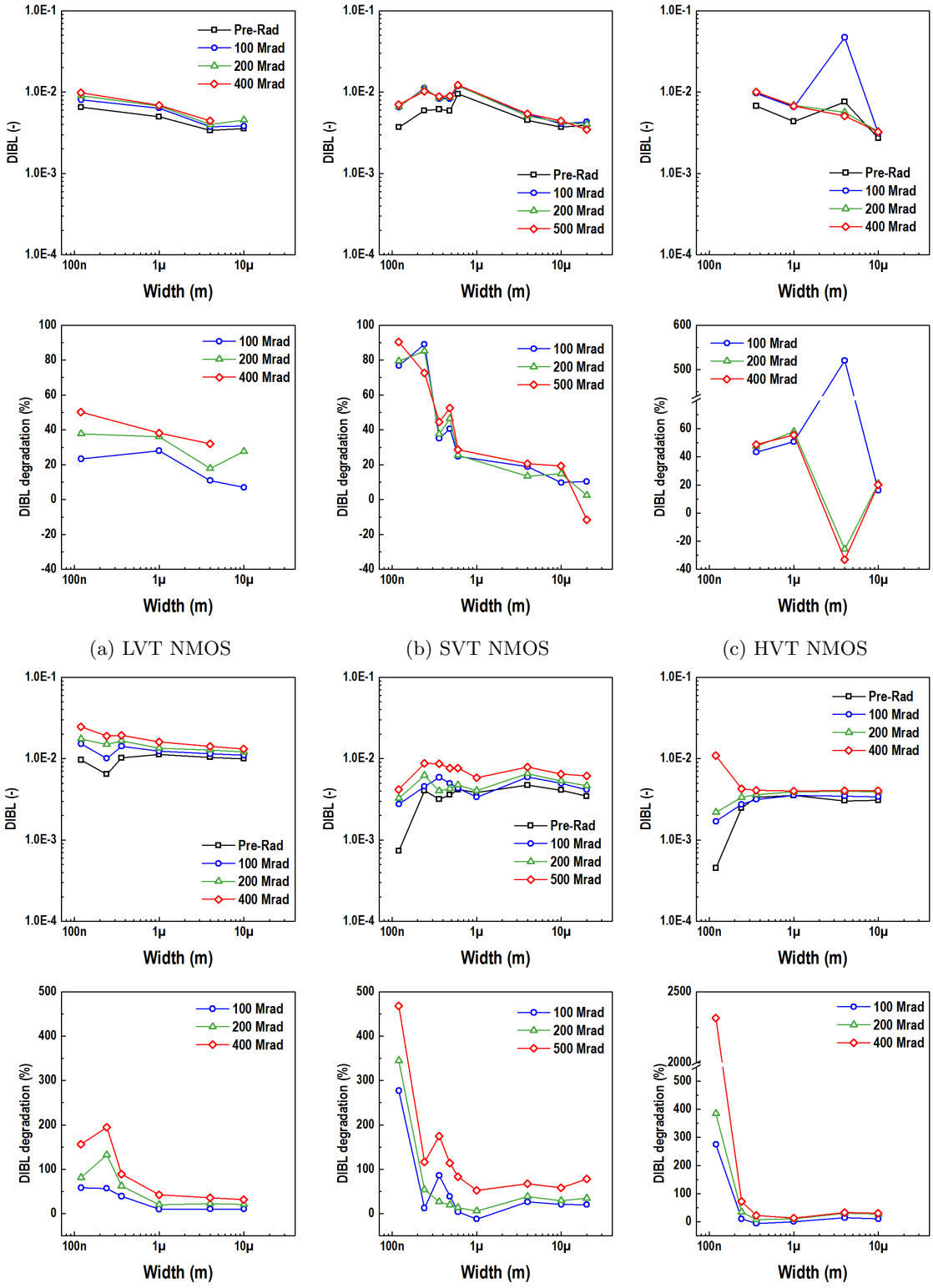


(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 66: V_{TH} and degradation, scaling vs channel Length at 25°C for N and P type devices of low, standard and high threshold voltage

A.2.2 DIBL Factor Width Scaling

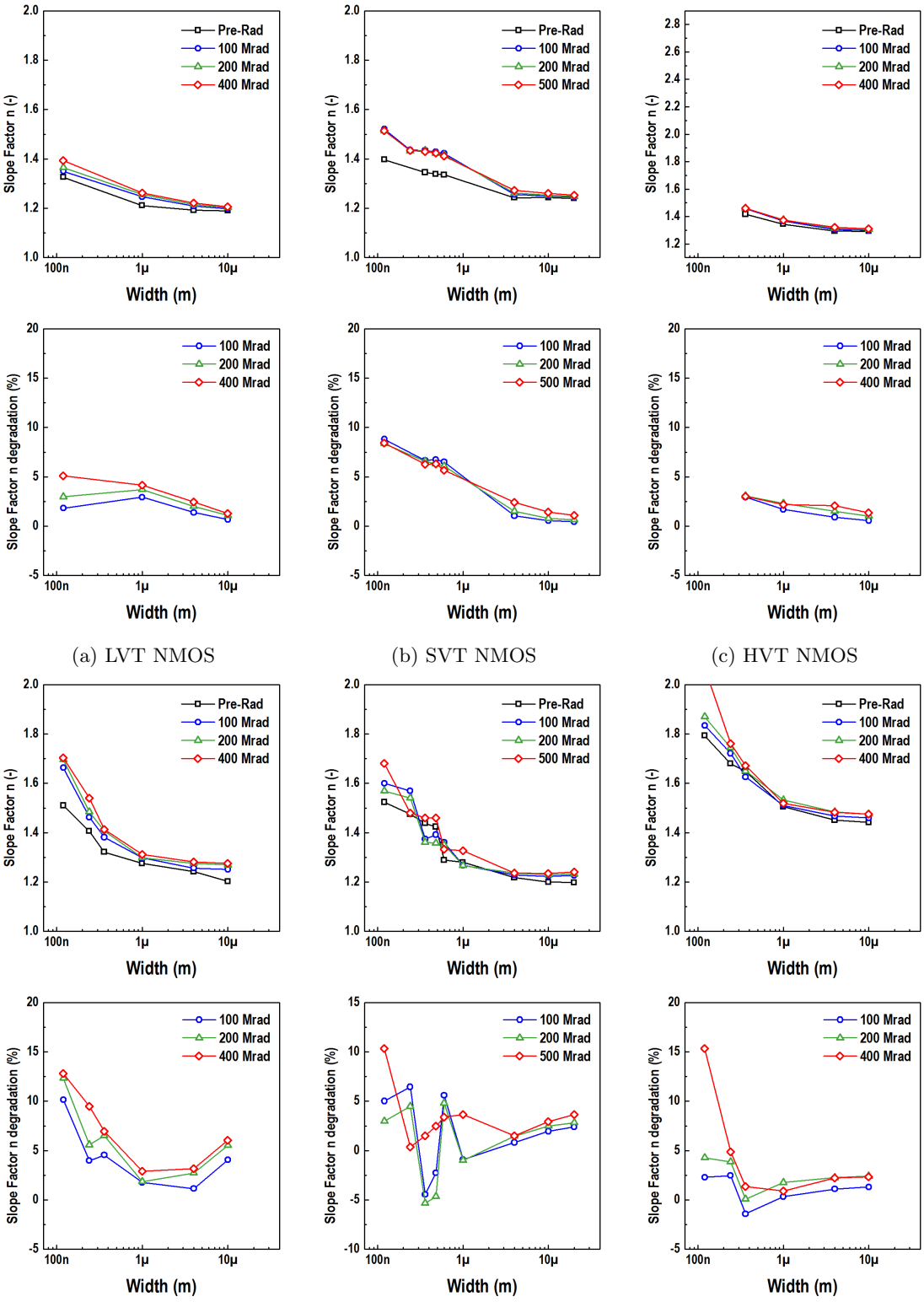


(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 67: DIBL and relative degradation, scaling vs channel Length at 25°C for N and P type devices of low, standard and high threshold voltage

A.2.3 WI Slope Factor Width Scaling

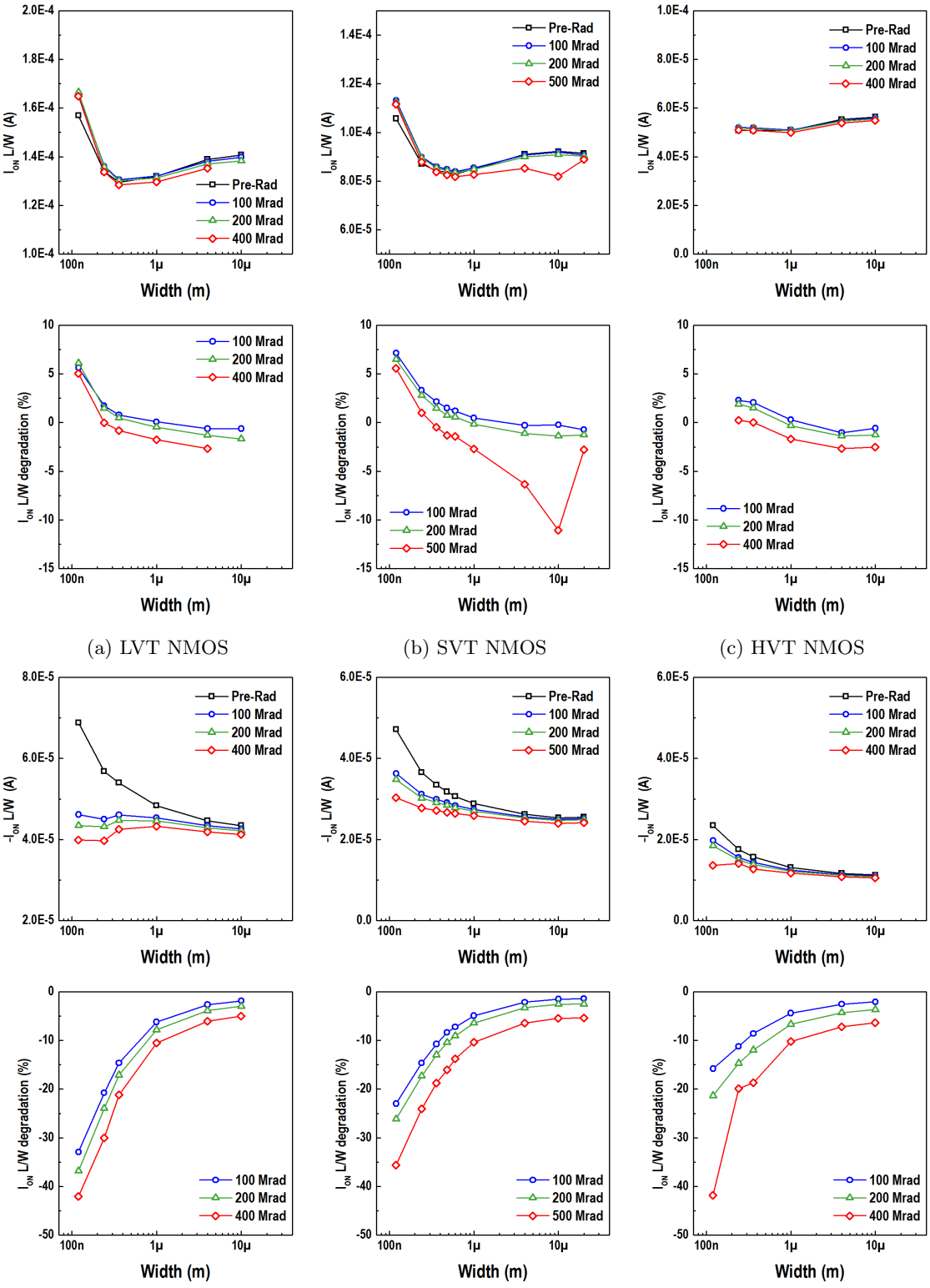


(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 68: Weak inversion slope factor and relative degradation, scaling vs channel Length at 25°C for N and P type devices of low, standard and high threshold voltage

A.2.4 On-Current Width Scaling

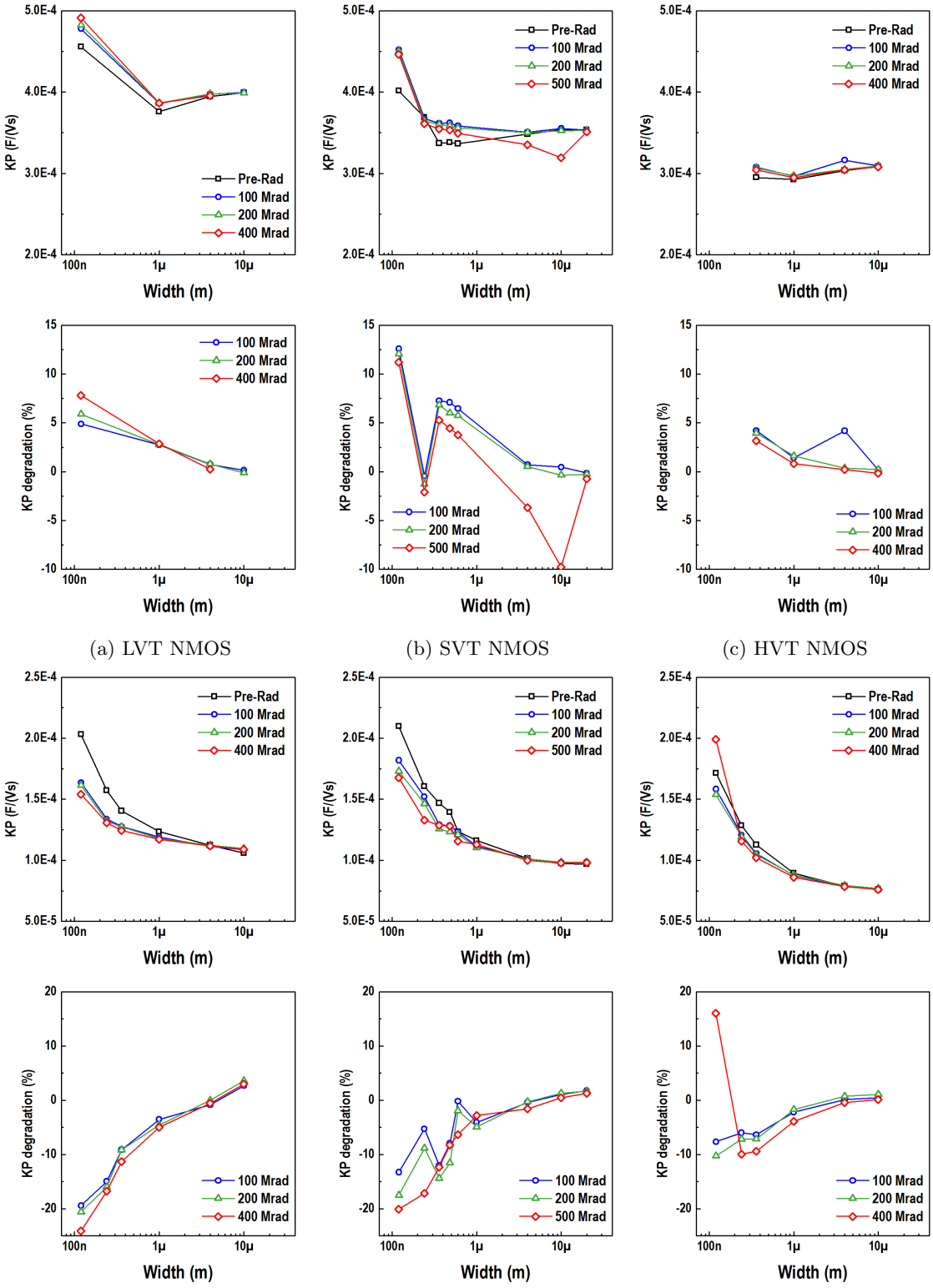


(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 69: On-state current normalised by $\frac{L}{W}$ and relative degradation, scaling vs channel Length at 25°C for N and P type devices of low, standard and high threshold voltage

A.2.5 KP Width Scaling

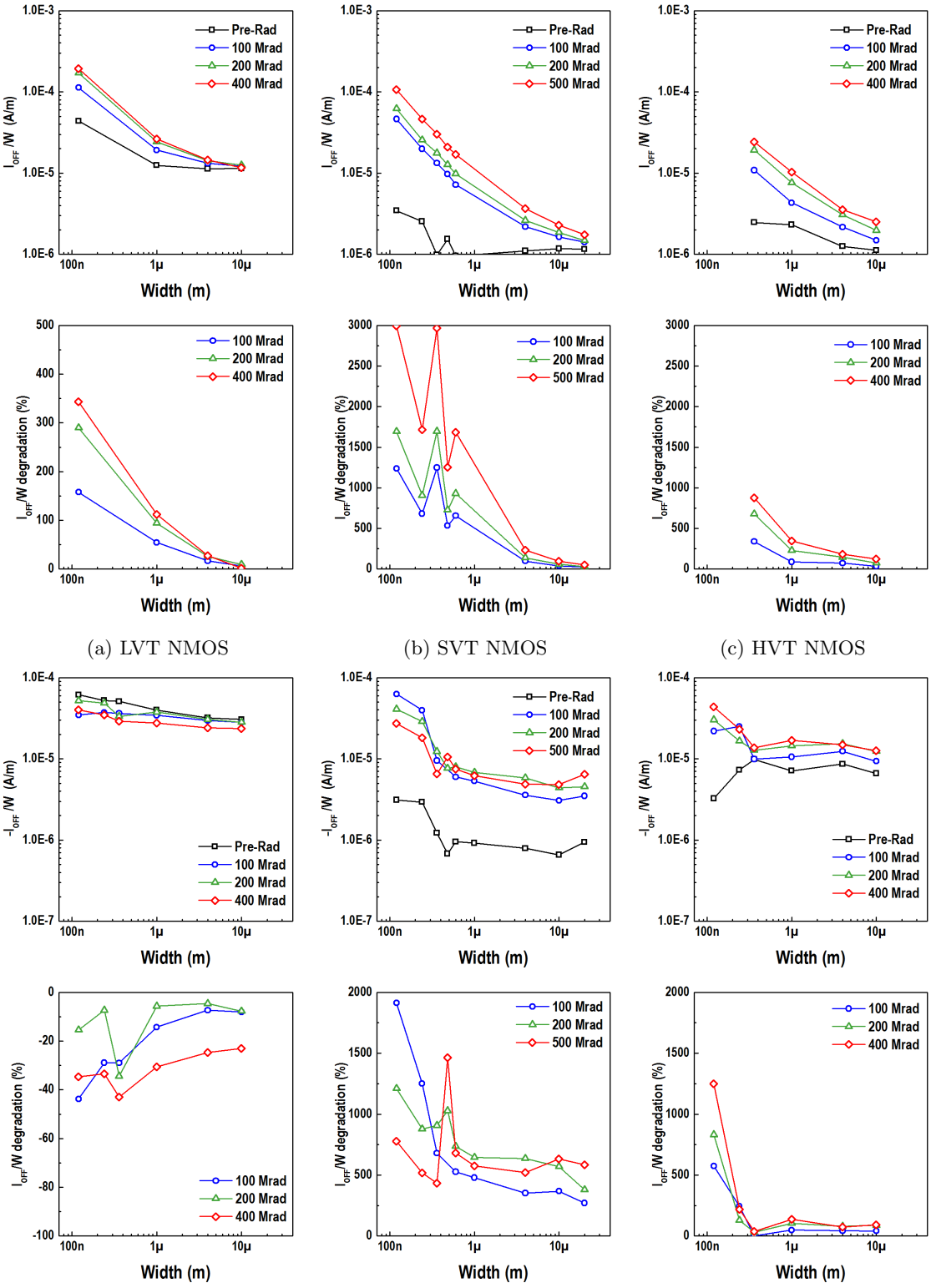


(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 70: Transconductance factor ($KP = \mu * C'_{OX}$) and relative degradation, scaling vs channel Length at 25°C for N and P type devices of low, standard and high threshold voltage

A.2.6 Leakage Current Width Scaling



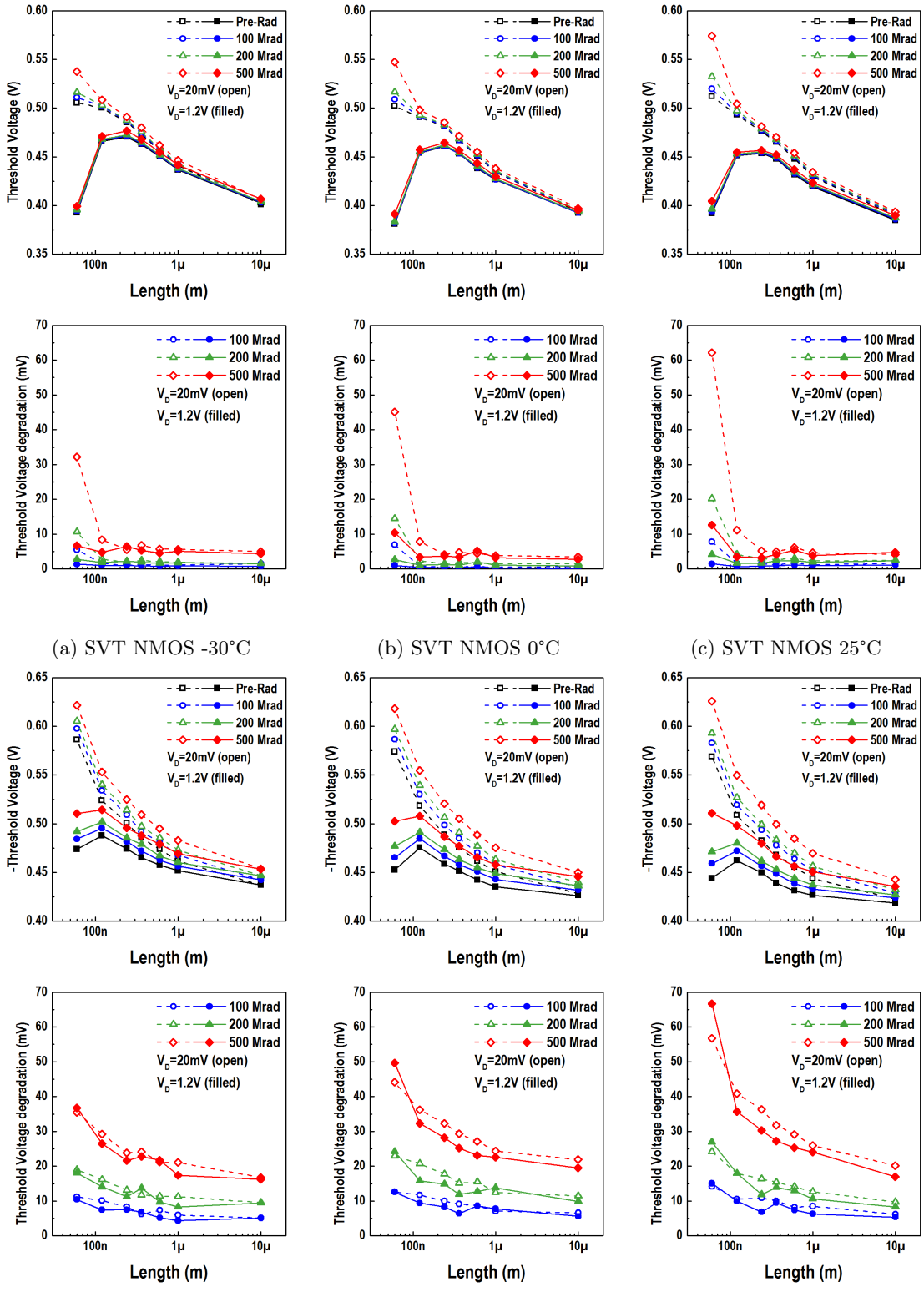
(a) LVT NMOS (b) SVT NMOS (c) HVT NMOS

(d) LVT PMOS (e) SVT PMOS (f) HVT PMOS

Figure 71: Leakage current normalised by $\frac{1}{W}$ and relative degradation, scaling vs channel Length at 25°C for N and P type devices of low, standard and high threshold voltage

A.3 Length Scaling, Width=20μm, at -30°, 0°, 25°C, SVT devices

A.3.1 Threshold Voltage Length Scaling

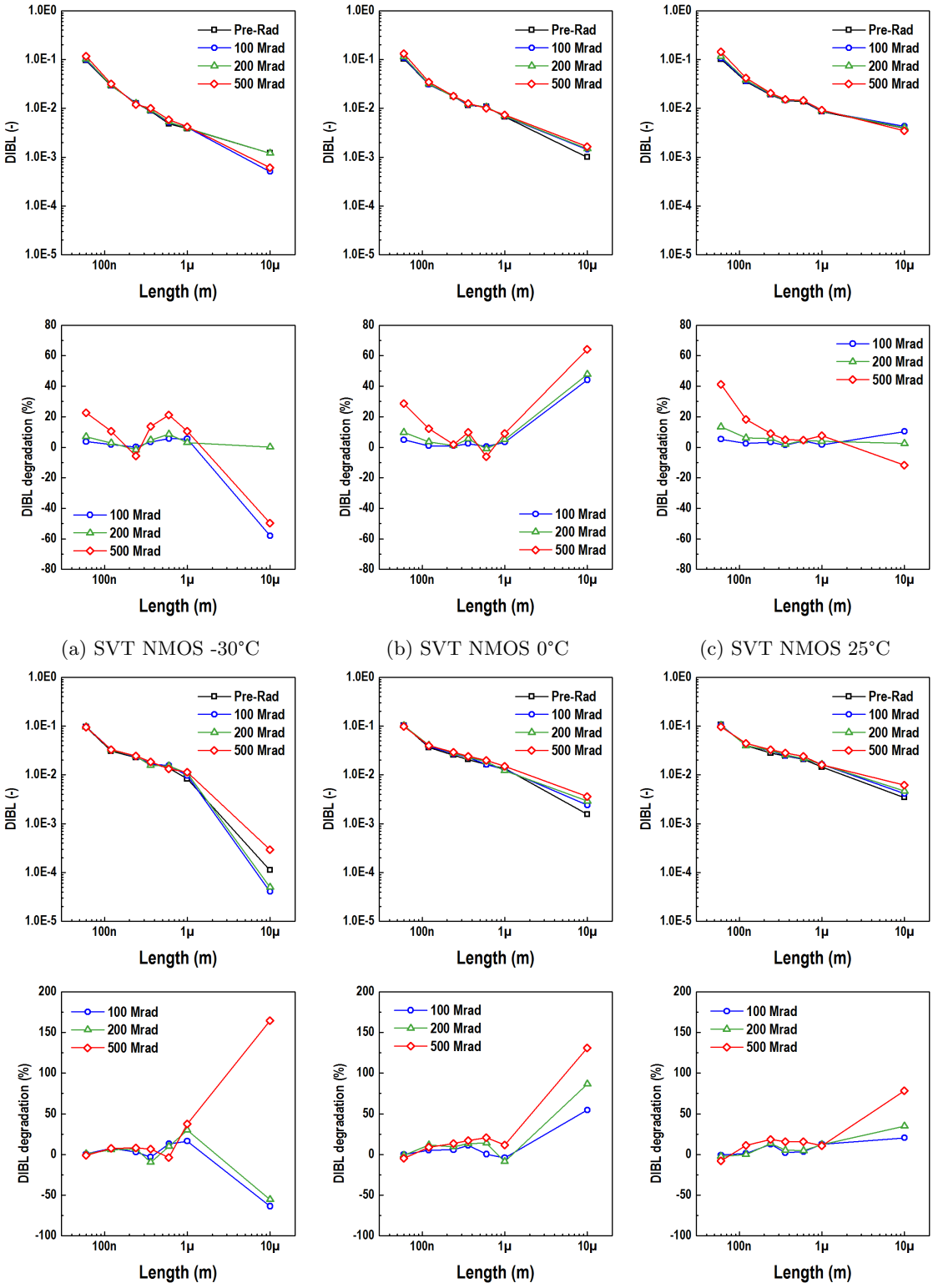


(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 72: V_{TH} and degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

A.3.2 DIBL Factor Length Scaling

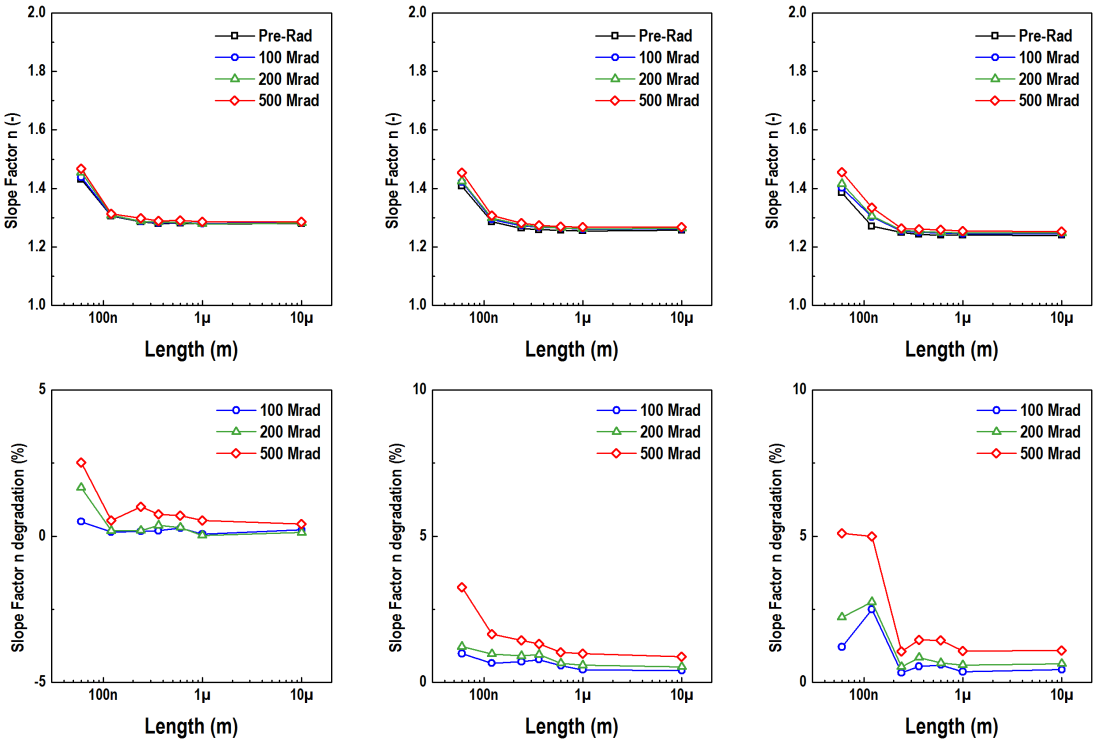


(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

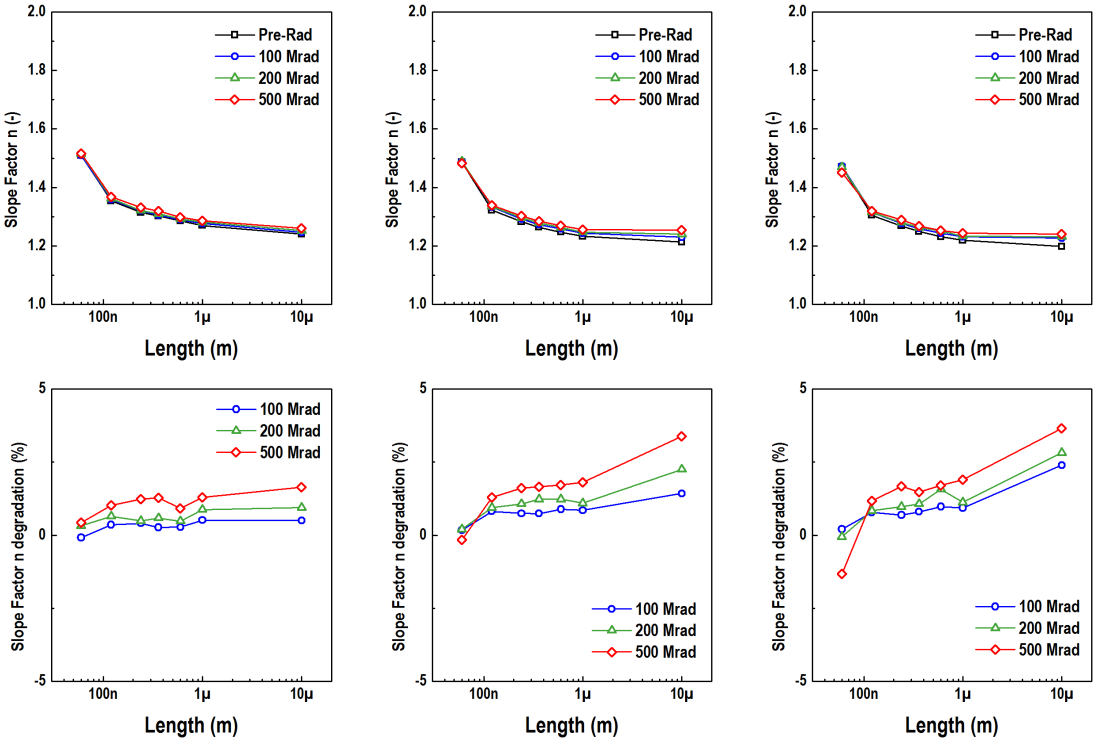
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 73: DIBL and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

A.3.3 WI Slope Factor Length Scaling



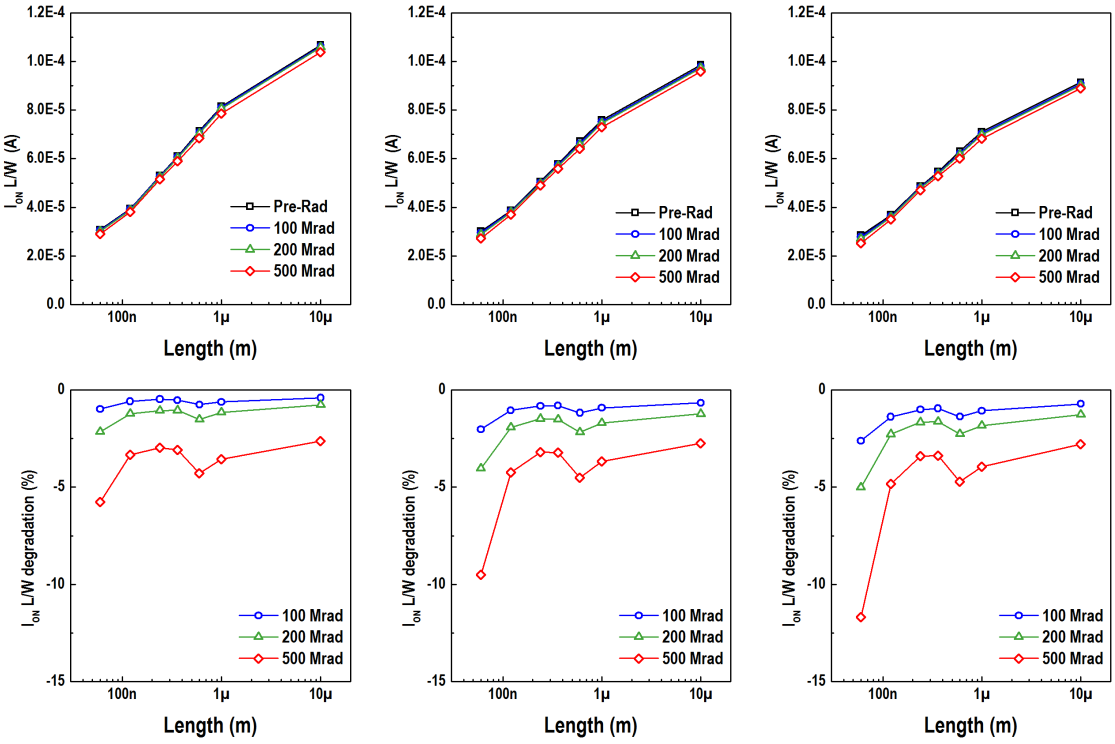
(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C



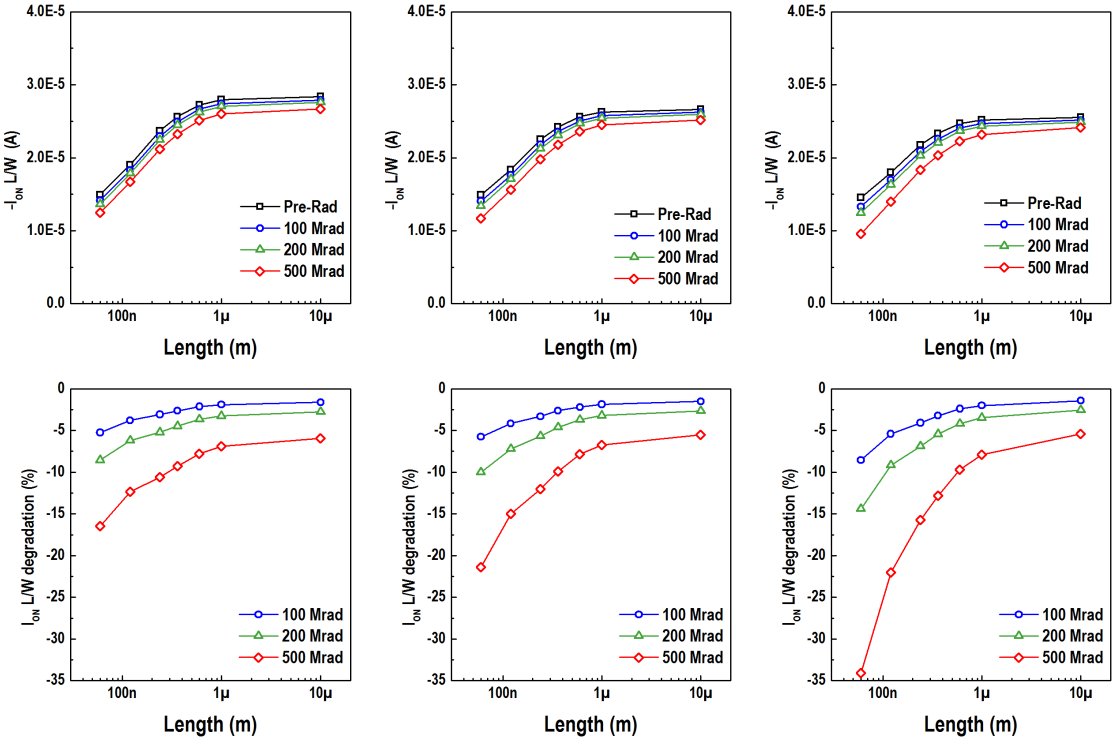
(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 74: Weak inversion slope factor and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

A.3.4 On-Current Length Scaling



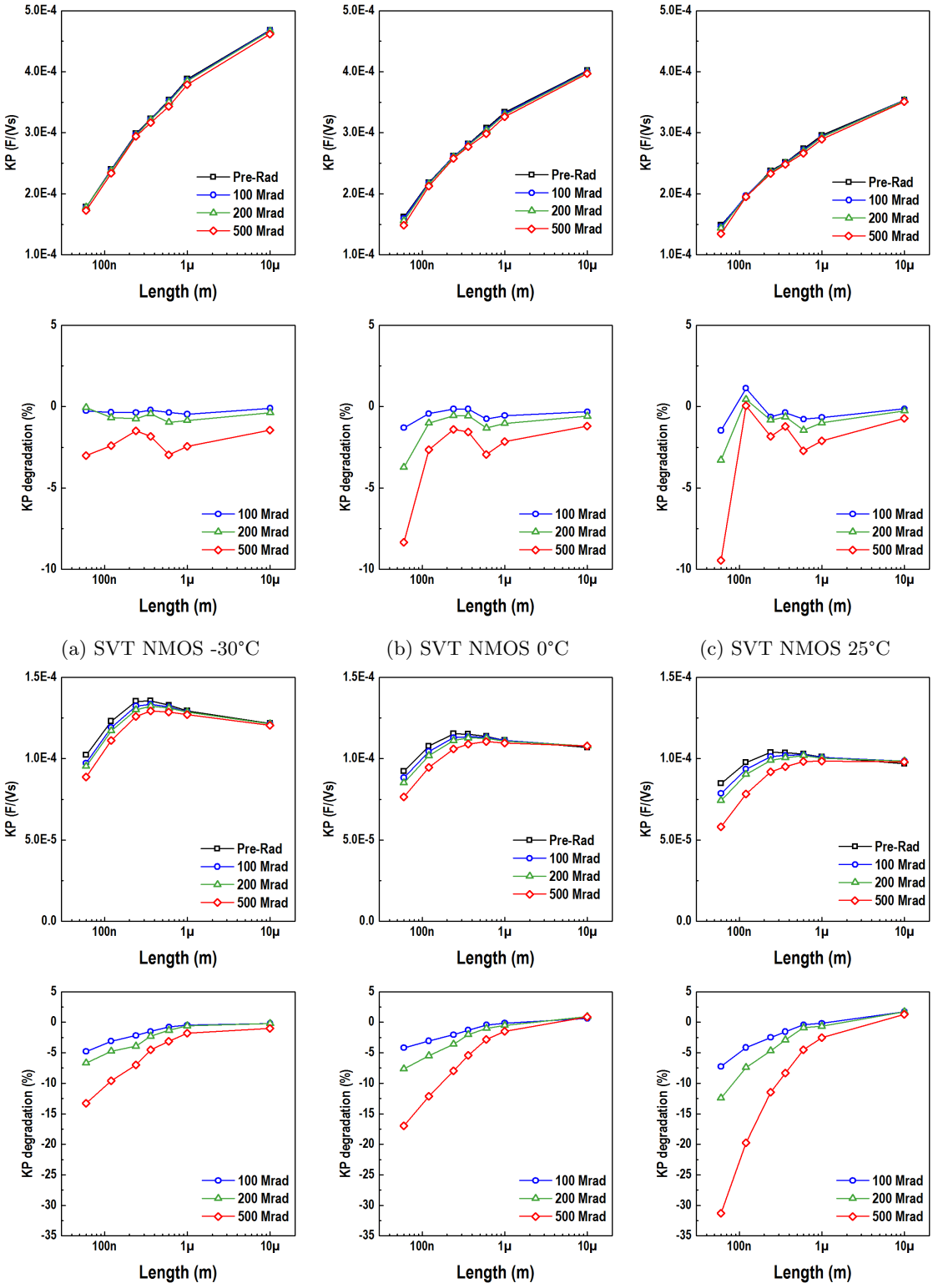
(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C



(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 75: On-state current normalised by $\frac{L}{W}$ and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

A.3.5 KP Length Scaling

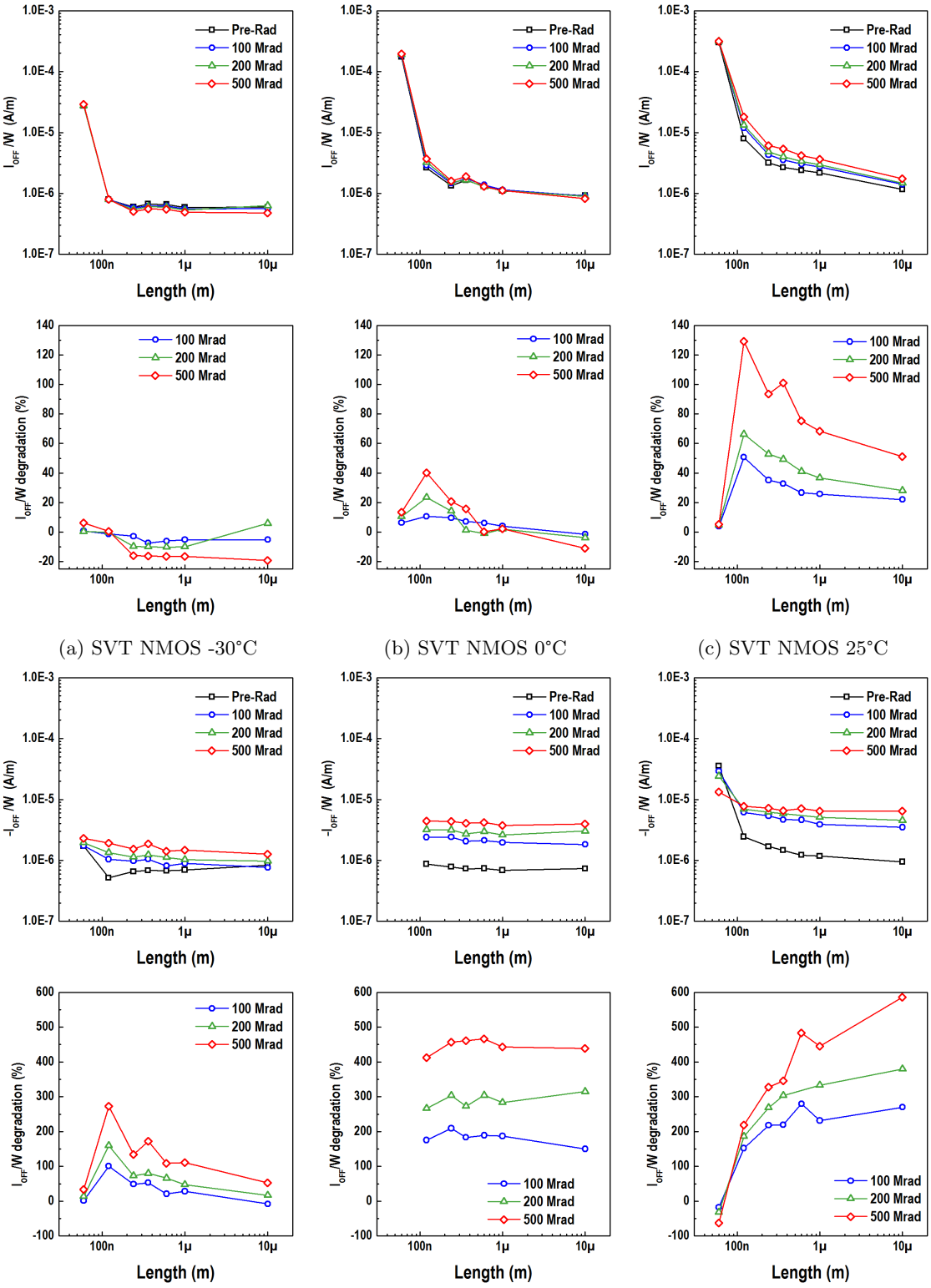


(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 76: Transconductance factor ($KP = \mu * C'_{OX}$) and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

A.3.6 Leakage Current Length Scaling



(a) SVT NMOS -30°C (b) SVT NMOS 0°C (c) SVT NMOS 25°C

(d) SVT PMOS -30°C (e) SVT PMOS 0°C (f) SVT PMOS 25°C

Figure 77: Leakage current normalised by $\frac{1}{W}$ and relative degradation, scaling vs channel Length for N and P type devices of standard threshold voltage, at -30°C, 0°C and 25°C

B Author's Publications

International peer-reviewed journals:

1. N. Makris, M. Bucher, **L. Chevas**, F. Jazaeri, J.M. Sallese, "Free Carrier Mobility, Series Resistance, and Threshold Voltage Extraction in Junction FETs," in IEEE Transactions on Electron Devices, vol. 67, no. 11, pp. 4658-4661, Nov. 2020.
2. M. Bucher, N. Makris, **L. Chevas**, "Generalized Constant Current Method for Determining MOSFET Threshold Voltage," in IEEE Transactions on Electron Devices, vol. 67, no. 11, pp. 4559-4562, Nov. 2020.

International peer-reviewed conferences, full-text:

1. N. Makris, **L. Chevas**, M. Bucher, "Compact Modeling of Low Frequency Noise and Thermal Noise in Junction Field Effect Transistors," ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC), 2019, pp. 198-201, Cracow, Poland, Sept. 23-26, 2019.
2. A. Nikolaou, **L. Chevas**, A. Papadopoulou, N. Makris, M. Bucher, G. Borghello, F. Faccio, "Forward and Reverse Operation of Enclosed-Gate MOSFETs and Sensitivity to High Total Ionizing Dose," 2019 MIXDES - 26th International Conference "Mixed Design of Integrated Circuits and Systems", pp. 306-309, Rzeszow, Poland June 27-29, 2019.
3. A. Papadopoulou, N. Makris, **L. Chevas**, A. Nikolaou and M. Bucher, "Design of Micropower Operational Transconductance Amplifiers for High Total Ionizing Dose Effects," 2019 8th International Conference on Modern Circuits and Systems Technologies (MOCAST), pp. 1-4, Thessaloniki, Greece, May 13-15, 2019.
4. **Best Paper Award**, A. Nikolaou, M. Bucher, N. Makris, A. Papadopoulou, **L. Chevas**, G. Borghello, H. D. Koch, F. Faccio, "Modeling of High Total Ionizing Dose Effects for Enclosed Layout Transistors in 65 nm Bulk CMOS", 41st IEEE Int. Semiconductor Conf. (CAS), pp. 1-4, Sinaia, Romania, Oct. 10-12, 2018.
5. **L. Chevas**, A. Nikolaou, M. Bucher, N. Makris, A. Papadopoulou, A. Zografou, G. Borghello, H.D. Koch, F. Faccio, "Investigation of Scaling and Temperature Effects in Total Ionizing Dose (TID) Experiments in 65nm CMOS", 25th Int. Conf. Mixed Design of Integrated Circuits and Systems (MIXDES), Gdynia, Poland, June 21-23, 2018.
6. A. Nikolaou, M. Bucher, N. Makris, A. Papadopoulou, **L. Chevas**, G. Borghello, H. D. Koch, K. Kloukinas, T. S. Poikela, F. Faccio, "Extending a 65 nm CMOS Process Design Kit for High Total Ionizing Dose Effects", IEEE Int. Conf. on Modern Circuits and Systems Technologies (MOCAST), pp. 1-4, Thessaloniki, Greece, May 7-9, 2018.
7. M. Bucher, A. Nikolaou, A. Papadopoulou, N. Makris, **L. Chevas**, G. Borghello, H. D. Koch, F. Faccio, "Total Ionizing Dose Effects on Analog Performance of 65 nm Bulk CMOS with Enclosed-Gate and Standard Layout", 31st IEEE Int. Conf. on Microelectronic Test Structures (ICMTS), pp. 166-170, Austin, Texas, Mar. 19-22, 2018.

International peer-reviewed conferences, abstract:

1. **L. Chevas**, M.I. Iosifidis, N. Makris, M. Bucher, "Electrical Behavior of Commercial Discrete Power VDMOS Transistors and their Compact Modelling", 7th Int. Conf. on Micro-Nanoelectronics, Nanotechnologies and MEMS (Micro&Nano), Thessaloniki, Greece, Nov. 5-7, 2018.
2. A. Papadopoulou, **L. Chevas**, A. Nikolaou, N. Makris, M. Bucher, "Weak Inversion Ring Oscillator Design Study in 65nm CMOS Technology under Total Ionizing Dose Effects", 7th Int. Conf. on Micro-Nanoelectronics, Nanotechnologies and MEMS (Micro&Nano), Thessaloniki, Greece, Nov. 5-7, 2018.

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