Circuits, Sensors and Renewable Energy Sources Laboratory

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School of Electrical and Computer Engineering of Technical University of Crete

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Doctor of Philosophy

by **Mandourarakis Ioannis**

Electronic systems for energy management of photovoltaic cells

Advisory Committee

- Assoc. Prof. E. Koutroulis (Supervisor)
- Prof. S. Siskos (Physics Dept., Aristotle University of Thessaloniki)
- Prof. G. Stavrakakis

Examination Committee

- Assoc. Prof. E. Koutroulis (Supervisor)
- Prof. S. Siskos (Physics Dept., Aristotle University of Thessaloniki)
- Prof. G. Stavrakakis
- Prof. A. Dollas
- Prof. G. Karystinos
- Assoc. Prof. S. Ioannidis
- Assoc. Prof. F. Kanellos

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Abstract

Expanding the markets for advanced photovoltaic (PV) energy harvesting applications depends on the use of power management methods and electronic systems that implement efficient processes to maximize power generation. The research presented in this dissertation is the result of a response to such demands, presenting novel techniques which aim at facilitating the energy management in photovoltaic systems and electricity grids, in general.

The main target of this PhD thesis is to research a series of novel techniques which can work either as single approaches to serve the aforementioned purpose, but also to allow for their combination to create low-power, low-complexity, and low-cost devices dedicated to be embedded in a single power source (either a PV cell or a set of PV cells). The goal is to enhance the controllability of the overall system, to improve its power efficiency, and to increase the amount of status information received by every unit involved, rather than shared aggregated values of telemetry data. This also translates to a maintenance service upgrade by expediting any failure diagnosis, simplifying its serviceability and minimizing any out-of-order costs.

In this PhD thesis, novel electronic systems are presented for:

- the maximization of the power produced by photovoltaic cells,
- the management of the energy produced by photovoltaic cells,
- the addition of status monitoring capabilities to distributed DC power sources,
- the addition of operational controlling capabilities to distributed DC power sources.

Experimental prototypes of the proposed electronic energy management systems have been developed and their successful operation has been validated by experimental results.

Περίληψη

Ηλεκτρονικά συστήματα για τη διαχείριση ενέργειας φωτοβολταϊκών στοιχείων

Η επέκταση των αγορών για προηγμένες εφαρμογές συλλογής ενέργειας φωτοβολταϊκών στοιχείων (Φ/Β) εξαρτάται από τη χρήση μεθόδων διαχείρισης ενέργειας και ηλεκτρονικών συστημάτων που εφαρμόζουν αποτελεσματικές διαδικασίες για τη μεγιστοποίηση της παραγωγής ενέργειας. Η έρευνα που παρουσιάζεται σε αυτή τη διατριβή είναι το αποτέλεσμα ανταπόκρισης σε τέτοιου είδους ανάγκες, παρουσιάζοντας καινοτόμες τεχνικές που στοχεύουν στη διευκόλυνση της διαχείρισης ενέργειας στα φωτοβολταϊκά συστήματα και στα δίκτυα ηλεκτρικής ενέργειας, γενικότερα.

Κύριος στόχος αυτής της διατριβής είναι η ανάπτυξη μιας σειράς καινοτόμων τεχνικών που μπορούν να λειτουργήσουν είτε ως μεμονωμένες προσεγγίσεις για να εξυπηρετήσουν τον προαναφερθέντα σκοπό, είτε για να επιτρέψουν κατά τον συνδυασμό τους τη δημιουργία ολοκληρωμένων λύσεων χαμηλής κατανάλωσης, χαμηλής πολυπλοκότητας και χαμηλού κόστους, τροποποιημένες ώστε να επιτρέπουν την ενσωμάτωσή τους σε μια συμβατική πηγή ισχύος (είτε μία Φ/Β κυψέλη ή ένα σύνολο Φ/Β κυψελών). Σκοπός είναι να ενισχυθεί η δυνατότητα ελέγχου του συνολικού συστήματος, να βελτιωθεί η απόδοση ισχύος του και να αυξηθεί ο όγκος των πληροφοριών που λαμβάνονται από κάθε εμπλεκόμενη μονάδα, αντί να μοιράζονται συγκεντρωτικές τιμές δεδομένων τηλεμετρίας. Αυτό μεταφράζεται επίσης σε αναβάθμιση των υπηρεσιών συντήρησης επιταχύνοντας τη διάγνωση τυχόν αστοχιών, απλοποιώντας τη δυνατότητα επιδιορθώσεων και ελαχιστοποιώντας το κόστος που προκύπτει λόγω παύσης λειτουργίας του συστήματος.

Σε αυτή τη διδακτορική διατριβή παρουσιάζονται νέα ηλεκτρονικά συστήματα για:

- τη μεγιστοποίηση της ισχύος που παράγεται από τα Φ/Β στοιχεία,
- την διαχείριση της ενέργειας που παράγεται από Φ/Β στοιχεία,
- την προσθήκη δυνατότητας παρακολούθησης των κατανεμημένων DC πηγών ενέργειας,
- την προσθήκη ελέγχου της λειτουργίας των κατανεμημένων DC πηγών ενέργειας.

Έχουν αναπτυχθεί πειραματικά πρωτότυπα των προτεινόμενων ηλεκτρονικών συστημάτων διαχείρισης ενέργειας και η επιτυχής λειτουργία τους έχει επικυρωθεί από πειραματικά αποτελέσματα.

Foreword

For the preparation of this PhD thesis, first of all, I would like to express my deepest feelings of gratitude towards my supervisor and Professor of the School of Electrical and Computer Engineering of the Technical University of Crete (TUC), Dr. Eftychios Koutroulis, for his mentoring, inspiration, and academic guidance in all of the stages of my academic career.

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Published papers of this PhD thesis

The work presented in this PhD thesis has been published in the following scientific papers:

1. **I. Mandourarakis**, V. Gogolou, E. Koutroulis and S. Siskos, "Integrated Maximum Power Point Tracking System for Photovoltaic Energy Harvesting Applications," in *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 9865-9875, Aug. 2022.
2. **I. Mandourarakis**, E. Koutroulis and G. N. Karystinos, "Power Line Communication Method for the Simultaneous Transmission of Power and Digital Data by Cascaded H-Bridge Converters," in *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 12793-12804, Oct. 2022.
3. **I. Mandourarakis**, Z. Agorastou, E. Koutroulis, G. N. Karystinos and S. Siskos, "On-chip Power Line Communication for Cascaded H-bridge Power Converters," *2022 11th International Conference on Modern Circuits and Systems Technologies (MOCAST)*, 2022, pp. 1-5.
4. I**. Mandourarakis**, E. Koutroulis and G. N. Karystinos, "Transmission of Digital Data to Cascaded H-bridge Converters Through the Power Line," in *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, 2022, pp. 1-12
5. **I. Mandourarakis**, E. Koutroulis and G. N. Karystinos, "Control of Cascaded H-bridge Converters for Power Line Communication" in *IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society*, 2022, pp. 1-6.
6. S. Voutsinas, **I. Mandourarakis**, E. Koutroulis, D. Karolidis, I. Voyatzis, M. Samarakou, "Control and communication of smart photovoltaic arrays", *Pan-Hellenic Conference on Informatics (PCI)*, 2022, pp. 1-6

Table of Contents

1.Introduction

1.1. Renewable energy sources and photovoltaic cells

The term 'renewable energy' refers to energy sources that are replenished naturally, in a relatively short period of time, and that do not deplete as they are used. Renewable Energy Sources (RES) are used to generate electricity and output that power to the coupled grid and/or on AC/DC electrical loads. The main types of renewable energy sources are solar, wind, hydro, biomass, and geothermal.

Solar energy is the most widely used renewable energy source. The radiant light of the sun (electromagnetic energy) can be converted into electricity by PVs. All the other types require the use of an electric generator on their final stage, which turns the mechanical power into electricity. For example, wind energy is converted into electricity by the electric generators of wind turbines. Wind turbines are usually located in areas where there is a strong, consistent wind. Hydro energy is converted into electricity by hydroelectric power plants which are usually located near rivers or lakes and use the power of moving water to rotate a turbine that generates electricity. Biomass energy is converted into electricity by biomass power plants which turn the chemical energy into thermal energy through controlled burners and then the thermal energy into mechanical energy through steam pressure which activates the rotation of electric generators. Finally, geothermal energy is converted into electricity by geothermal power plants which include the final two stages of the biomass power plants.

Solar energy is the most abundant renewable energy source, making up nearly 73% of the renewable energy available on Earth. Wind energy is the second most abundant renewable energy source, making up about 25% of the renewable energy available on Earth. Hydroelectric energy is the third most abundant renewable energy source, making up about 2% of the renewable energy available on Earth.

PVs are the most common type of solar cell made of a material that absorbs sunlight and converts it into electricity. Other types of solar cells are used to capture the thermal energy of the sun. However, in this PhD thesis the word 'solar cell' will always refer to a PV cell. The most common type of PV cell is the silicon cell. Silicon cells are made of a silicon wafer that

is coated with a light-absorbing material, usually silicon dioxide, which absorbs photons from sunlight and releases electrons. These electrons flow through an external circuit and generate an electric current which can then be used to power electrical devices.

1.2. Energy management of photovoltaic cells

The energy management of photovoltaic cells is the process of regulating the amount of energy produced by the cells and how it is used. This can be implemented by controlling the amount of light the cells are exposed to, the amount of time that the cells are exposed to light, and the amount of electric power flowing through the cells. Since the most common need is to maximize the power that the PVs can yield, the first two of the aforementioned three methods are rarely used. The driving need towards power maximization is the fact that the PV cells are non-linear DC sources characterized by the power-voltage (P-V) curves shown in Fig. 1 which vary with solar irradiation and are susceptible to partial shading. The P-V curve of any solar cell presents all the possible operating points at a specific set of conditions (sunlight intensity, the plane array angle in respect to the sunlight beam, and the cell temperature).

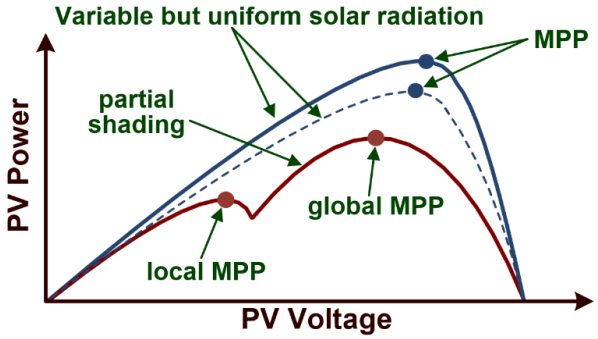


Fig. 1. Generic P-V characteristic of a PV array under direct sunlight (blue lines) and under partial shading (red line).

The Maximum Power Point (MPP) is the point on the power-voltage curve at which the output power of the PV array is maximized. The MPP of a PV array can be found on the peak of the blue curves shown in Fig. 1. The dotted curve in Fig. 1 is sketched to depict the trend that the operating points of the same PV array present when the incident irradiation in the PV array's plane is reduced. Since there is only one point where the power is being maximized for any array in any given circumstance, there needs to be a way to ensure that the PV array will be driven in a way that can guarantee its maximum power production. Such tracking methods are called Maximum Power Point Tracking (MPPT) methods and are used

to maximize the power output of a solar cell by matching the operating voltage of the PV cell/array to the corresponding MPP. When the PV cells are combined in series and/or in parallel sets on a PV module (panel) or array, the same curve format applies, unless some of the PV cells are shaded or malfunction. In that case, the PV array is said to be partially shaded (or malfunctioning) and the P-V curve is deformed by the emergence of various peaks, as shown in the red curve of Fig. 1. These peaks, also called local MPPs, may disorientate some of the MPPT algorithms as they may be stuck on a local MPP rather than the global MPP. Such a problem does not emerge in the case that the MPPT is dedicated to one cell only, which is also the case for the system to be developed in this PhD thesis.

All MPPT algorithm variations constantly monitor the power output of the PV structure and adjust the its operating voltage to maintain operation at the maximum power point. This allows the PV cell (or module/array) to operate at its maximum power output even when the incident light conditions are changing. This provides a significant advantage in applications where the PV cell is exposed to varying light conditions, such as cloudy weather, in a solar vehicle, a solar-powered aircraft, or in PV systems with malfunctioning PV elements.

The MPPT algorithms are also very useful in grid-tied solar power systems to maximize the power output of the PV array. This allows the PV array to operate at its maximum power output even when the grid voltage is changing.

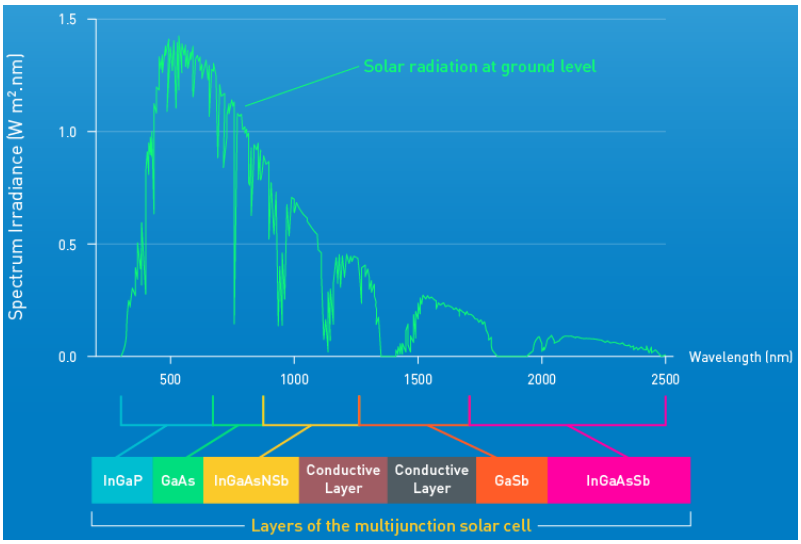


Fig. 2: Degree of utilization of direct solar radiation by the various gallium compounds and the wavelength of solar radiation where they yield the most (source: futurism.com)

The efficiency of a PV cell, i.e. the percentage of sunlight that is converted into electricity for commercial photovoltaic cells is about 22%. According to an article by the World

Economic Forum [1], a scientific team managed to create in July 2017 a PV multijunction which presented a combined (for the 5 layers used) efficiency of 41.2%, utilizing almost all frequencies of the available spectrum (Fig. 2) of direct solar radiation [2]. The innovation of the construction of this PV is twofold. On the one hand, a new printing technology of the individual layers was developed that increases manufacturing precision, on the other hand, gallium antimonide (GaSb) was used for the layers in order to make the most of the available spectrum of solar radiation directly incident on the material.

Although PV has been quite expensive to build, successes like this are proving vital in pointing out the limits of feasibility studies for solar technology, setting a positive precedent and reshaping the market and emerging products.

The lifetime of a photovoltaic cell is the number of years over which it produces a specified power output and it typically ranges from 20 to 30 years. The temperature coefficient of a photovoltaic cell is the change in the cell's power output per degree Celsius change in temperature. The temperature coefficient of a photovoltaic cell is typically -0.5% to -0.7%. The power density of a photovoltaic cell is the power output of the cell per unit area and it typically ranges from 100 to 200 watts per square meter. Finally, the energy density of a photovoltaic cell is the energy output of the cell per unit volume and typically ranges from 1 to 2 Watt-hours per cubic meter.

1.3. Purpose of the PhD thesis

The purpose of this PhD thesis is the design and development of electronic systems that will facilitate towards the energy management, monitoring and control of a set of distributed DC power sources. Although the elements of such a set can have diversifying DC source characteristics and in principle this system can allow for any type(s) of DC sources, the PhD thesis focuses on the sole use of conventional PV cells. However, even if similar cells, of the same brand and model are used, due to the effects that may arise during the partial shading in PV modules (i.e. sets of PV cells), each cell may be operating on a different point of its current-voltage (I-V) characteristic curve at given point in time. This suggests that each element of such a DC source set may yield different DC output voltage and/or present a different power production capacity, which in turn, shows that the use of PV cells as distributed DC sources can serve as a liable example, indicative enough to confirm the operability of the system in the general case that allows for diversified DC sources.

Fig. 3 presents a set of PV cells, connected in series, each of which is connected to a Power Converter Unit (PCU) where its power flow and voltage are managed by a Control Unit (CU). The PCU in this PhD thesis is a DC/DC converter with its output connected to a full-bridge operating as an AC inverter. The CU allows for the power management (MPPT and power regulation) of each PV cell by controlling the PCU. Using such a configuration, it is possible to compose PV array structures for PV power generation systems, by expanding the PV module shown in Fig. 3, which also allows for parallel connections as long as the edges of the modules develop the same potential.

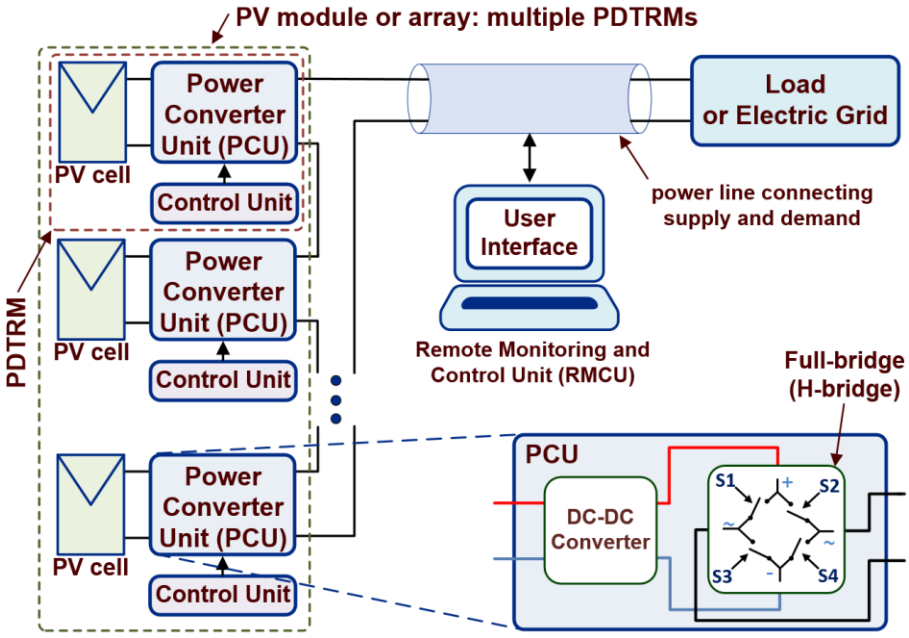


Fig. 3: The general diagram of the PV system investigated in this PhD thesis.

A Power Line Communication (PLC) technology has also been developed which allows for such a system to be remotely (via the Internet) monitored and controlled. This means, that this system is designed so that each one of the PV cell PCU/CU can provide telemetry data and/or be commanded accordingly, so that the system alters its operating status, in respect to the wishes of the remote user. As mentioned, the following chapters constitute parts of a step-by-step design and implementation of a novel PLC system. Each chapter includes various representations of its sub-systems, according to the level of detail, the nature of the implemented logic, the devices involved, and the design principles in focus. The core of this novel PLC design is based on the mixed-signal full-bridge blocks (see Fig. 3) which, from this point on, will be referred as Power and Data Transmission and Reception Modules, or PDTRMs in short. As explicitly shown on the lower right side of Fig. 3, the PCU can be further broken

down into two main parts, both of which can be controlled by the CU, a DC-DC converter and a full-bridge.

The PLC allows for a lower cost of implementation (when compared to the conventional substitutes for wireless data transmission) and, in principle, a more secure communication when this technology is used in public services.

The telemetry data and the commands are transmitted through the power line that connects the output of the PV module to the load or electric grid. In between these two ends, somewhere over the transmission line there is the magnetic coupling of the Remote Monitoring and Control Unit (RMCU). This unit is comprised of two main interfaces, with the first being dedicated to receiving the telemetry data (Uplink Receiver) and the second being dedicated to transmitting the user commands (Downlink Transmitter). In accordance, each one of the PV cell PCU/CU has two similar interfaces, one for receiving the parameterization commands (Downlink Receiver) and one for transmitting the telemetry data (Uplink Transmitter).

The subsystems that are presented in this PhD thesis can also be constructed within an Integrated Circuit (IC), as shown in Fig. 4, which can be embedded on the back-panel area of a conventional PV cell. The IC contains the circuits and the logic that is described in Fig. 3 as the PCU and the CU, respectively.

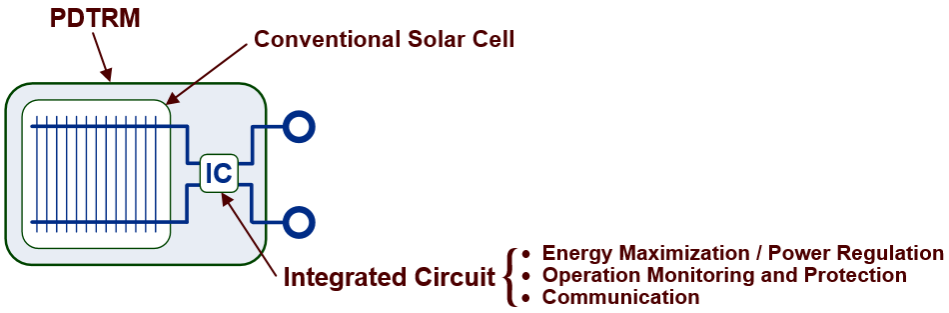


Fig. 4: Implementation of the PV cell PCU and the CU in an integrated circuit.

Fig. 5 presents the same content of Fig. 3, enriched with the MPPT/Power Regulation, and full-duplex communication components for the Uplink and Downlink channels. The load or electric grid includes a low-pass filtering stage to remove the communication noise and minimize any potential interference. The long power line is modelled, both in Fig. 3 and Fig. 5 as a blue tube that protects the two power cables of the system. The Uplink Receiver and the Downlink Transmitter can be placed at any point on this line although its more natural for

these to be placed close to the physical node that receives and transmits information to the RMCU either directly or through the internet.

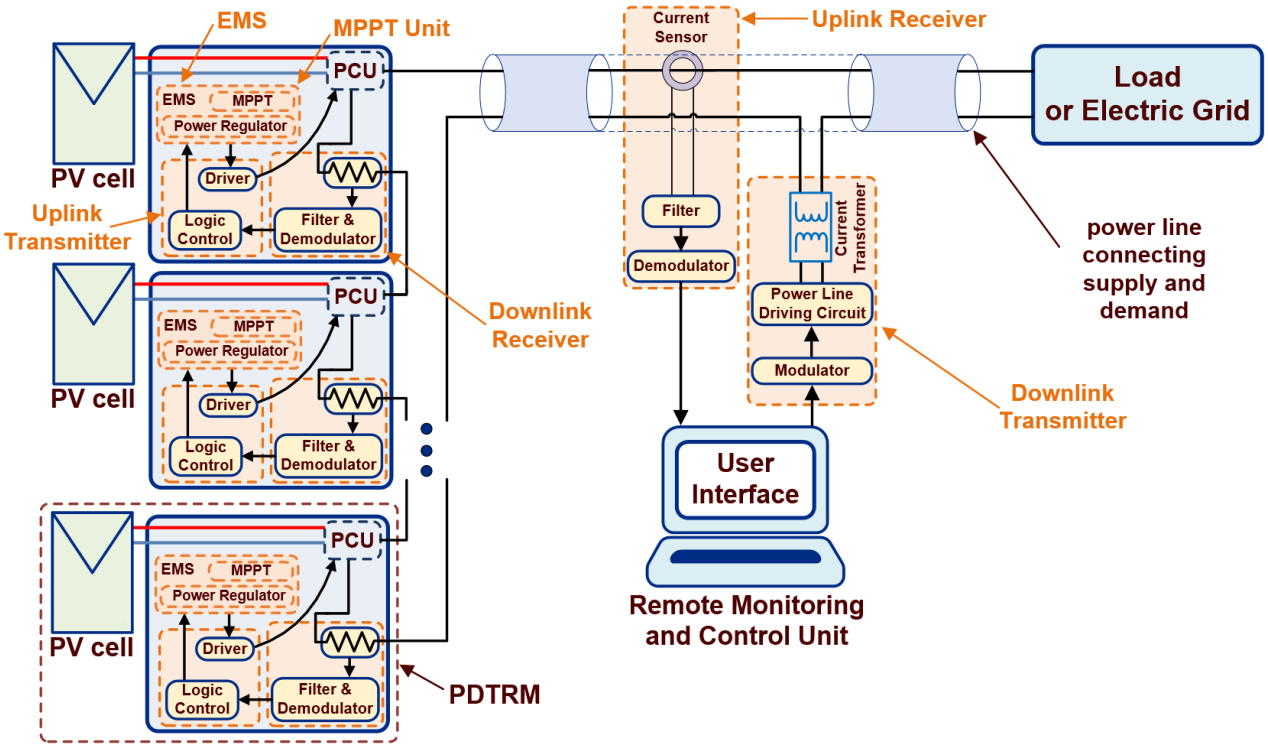


Fig. 5: The general diagram of the PV system investigated in this PhD thesis, expanded in order to present the Power Management Unit and the Uplink and Downlink interfaces.

As can be seen in the general diagram of Fig. 5, the PV cell PCU and CU developed in the context of this PhD thesis project consist of the following parts:

1) an MPPT execution unit for the continuous maximization of the power produced by the PV cell under the constantly changing conditions of solar radiation and ambient temperature.
2) an Energy Management Subsystem (EMS) to control the power generated by the PV cell and adapt it to the (time-varying) power requirements of the load supplied by the PV system or to a specific value pre-set by the user so that to support the corresponding function often required by modern smart electrical networks (Smart Grids). This system ensures that each PV cell can be connected in series and/or parallel with other PV cells, according to the technical requirements of the PV panel or array where these PV cells will be integrated in each application.
3) an electronic power converter whose circuit can be rearranged to act as either a DC/DC converter or a DC/AC converter and channel the power produced by the PV cell to the

desired type of electrical load depending on the end application (e.g. batteries, electrical network, etc.). In DC/AC mode, it is able to operate either autonomously (stand-alone mode) or in grid-connected mode. The PLC design, developed in the context of this PhD thesis project, allows for the remote user of the PV system to define the mode of operation (DC/DC or DC/AC) of the power converter through the communication interface.

4) an electronic subsystem which will act as a full-duplex communication node for: (a) monitoring the operation of the PV cell which allows the automatic detection and localization of faults in the individual PV cells of a PV array and (b) for controlling the PV array(s) parameterization.

   This means that the user will have the ability to remotely (via the internet) collect information on the correct or incorrect operation of each PV cell of the PV array through an appropriate interface (although this meta-processing of the transmitted data is out of the scope of this PhD thesis) and then he/she will be able to take proper actions, like shutting down or regulating the voltage and or the power of specific cells or group of cells, change from DC to AC or alter the AC frequency, etc.

   As regards the RMCU, the design of this PhD thesis is limited to the development of the communication and control hardware which, when enriched with the proper software on the RMCU it will support automatic and remote monitoring of the energy production of multiple PV systems of this type via the internet.

5) a microelectronic system that integrates the Downlink Receiver and the Uplink Transmitter to each one of the PV cell PCU and CU which are responsible for receiving parameterization commands and shape their power generation output, accordingly.

The main object of the chapters to follow is to present the design of the three main subsystems of the power control and communication units involved in this system, with most of the focus being paid on the PV cell side for:

- the MPPT and power regulation circuit intended for maximizing the electricity produced by the PV cell,
- the Uplink circuit that takes care of the transmission of information (uplink transmitter) from the PV cell – and to further complement this with its reception (uplink receiver) from the electronic circuit of the RMCU and

- the Downlink circuit that takes care of the (asynchronous to the Uplink) transmission of information (downlink transmitter) from the electronic circuit of the RMCU to each PV cell (downlink receiver) of the PV module/array.

The technologies that have been developed for the aforementioned subsystems can be used independently which suggests that, in principle, each one is unique and autonomous and thus can be utilized either alone or be integrated with the rest, in all possible combinations.

Also, these technologies can:

- be implemented either in an integrated circuit or in Field Programmable Gate Arrays (FPGAs)/microcontrollers/Digital Signal Processors (DSPs),
- be applied at a PV cell, PV module or PV array level and
- be extended to other non-PV-cell related applications [e.g. with thermoelectric generators (TEGs)], in distributed RES systems etc.

1.4. Structure of this PhD thesis

The rest of this PhD thesis is organized as follows:

- **Chapter 2** focuses on the novelty of the subsystem that is responsible for the proper MPPT of the power source. An elaborated analysis is describing the core digital components of this system including mentions on the soft-start sequence and its rules of operation, the properties of the sensors and the doubling of the duty cycle resolution, as well as discussing the various refinements and modifications the overall system. The chapter completes with the experimental results exercised upon two different setups, one with an FPGA and one on the fabricated ASIC, verifying its applicability and its successful dynamic operation under varying weather conditions.
- **Chapter 3** focuses on the energy management system of the design, which is responsible for controlling the generated power and adapting it to the (time-varying) load requirements. This system rearranges the power converter's final stage to act either as a DC/DC or DC/AC power generation source and/or to regulate its power and voltage, as instructed. The chapter proceeds by analyzing various features and subsystems, it provides information regarding the surveillance and protection requirements involved, it discusses the functionality of the various user inputs, and

completes by providing the experimental results that verify the proper operation of the operating state adjustment and the power/voltage regulation units.

- **Chapter 4** introduces the reader to the PLC concept, following an extensive prior art review of the existing methods for various architectures and applications and then focuses on the novelty of the proposed PLC method. Special emphasis is given on the power signal generation circuit, the digital transmitter design with its respective receiver and the main design parameters that are crucial for proper synching and a full-duplex channel implementation. The chapter proceeds by a brief analysis on estimations regarding the bit error rate for the required cabling and baud rate. Then, follows the description of the implemented experimental prototypes, one in an FPGA setup and one around a fabricated ASIC. The results of both experiments verify the correctness of the design and the applicability of the fabrication process. The chapter ends by the findings of a research around the total harmonic distortion of the proposed PLC system, providing useful insights on the best control schemes to minimize distortion on the load side, given the number of power modulation technique, the power sources involved and the bitstream length (i.e. the data transmission occupation percentage).
- **Chapter 5** begins with a thorough presentation of the methods used in point-to-point linking between distributed power production and consumption units. It then continues by analyzing the ways that the proposed design contributes to the addition of the remote controlling of the distributed power source networks, thus enriching the PLC concept that was described in the previous chapter. Although the design on the receiver in the power source side is topology agnostic in principle, the particular work focuses solely on H-bridge power converters. The concept is realized as an integrated framework of a digital data transmitter, receiver and communication protocol, that operate without using additional switching circuits or power amplifiers, and the chapter includes an extended explanation on how all these are utilized in a digital logic circuitry. There are extra sections that include the receiver's design parameters, its demodulation stages with the 3-layer encoding structure, and the interpretation of the synchronization and functional commands. The chapter proceeds by providing a series of simulations that clarify all of the concepts that are integrated in the protocol implementation, the full-duplex management and the synchronization units, in full

detail. Then it concludes, by presenting the experimental prototype and by discussing the experimental results which verify the feasibility of the design and the successful operation of all the systems involved.

- **Chapter 6** gathers all the design choices that were used throughout the implementation of the prototypes, which were proven to enhance the robustness of the system and to increase its verifiability. The chapter describes various practices which have proven to help debugging, to expedite development, to guarantee a flawless troubleshooting and a quick auditing procedure.
- Finally, the PhD thesis is concluded in **Chapter 7** which summarizes the contribution of this work and presents a series of useful conclusions and ideas for future work expansion.

2. Maximum power point tracking for PV cells

2.1. Introduction

In PV energy harvesting applications, integrated circuits must perform an efficient MPPT process to maximize the power production of the PV source under constantly changing atmospheric conditions. There are several alternative MPPT methods, but the Perturb and Observe (P&O) technique has the advantage of simplicity in operation and implementation. PV MPPT control systems are presented in this PhD thesis as a means of implementing the on-chip P&O MPPT method, which, in comparison to the existing MPPT systems, has the advantage of utilizing purely digital circuits without requiring complex devices like analog multipliers, Sample and Hold (S/H) units, or Analog-to-Digital (A/D) converters. The P&O MPPT technique can therefore be easily implemented with low design complexity and high performance. According to the experimental results, the PV MPPT control unit can operate successfully under a wide range of operating solar irradiation values and achieve high MPPT efficiency.

2.2. Prior art review

Solar, thermal, and piezoelectric energy harvesting systems have evolved significantly over the last decade. The technology aims to cover the energy demands of consumer-level smart devices in applications such as Internet-of-things (IoT) [3], wireless sensor networks (WSNs) [4] and wearable computing [5]. The current design of application-specific integrated circuits (ASICs), which serve as specialized peripheral circuits for managing the aforementioned sources of power generation, has also been influenced by these advancements. On the same silicon substrate, these ASICs may also be fabricated including integrated sensors, switching converters, and passive components like capacitors and inductors.

Numerous implementations have been made as a result of the study into energy harvesting systems that are intended to meet such commercial needs. Implementations that only rely on PV sources are the most conventional approach. Some of them concentrate on the PV string/panel level. However, single solar cell integrations have also been researched

since they are more suited for low-power and compact implementations. Fig. 6 shows the power-voltage curves of a PV generator under various incident sun irradiation and ambient temperature conditions [6]. The maximum power point (MPP) of a photovoltaic generator is dependent on sun irradiation and ambient temperature. In energy harvesting applications, a DC/DC converter is connected to the output of the PV source and it is controlled according to an appropriate MPPT process to ensure that the PV source always operates at the respective MPP despite the ever-changing meteorological conditions at the PV system installation site. This type of power management system is often required for PV energy harvesting applications to have low power consumption, high accuracy of tracking the MPP (i.e. MPPT efficiency), and minimal complexity and implementation cost.

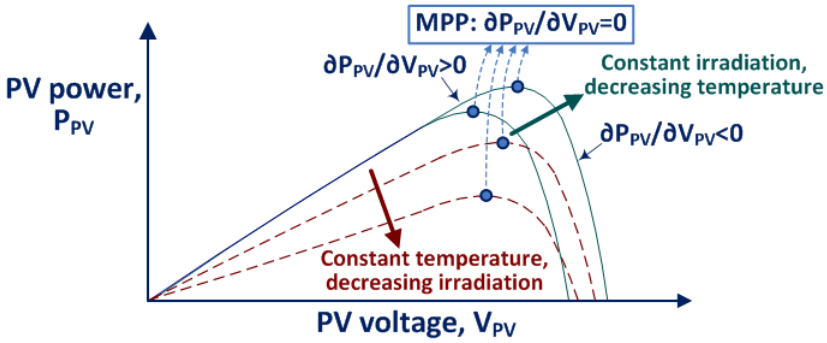


Fig. 6. The power-voltage curves of a PV power generator.

Until now, numerous on-chip implementations of MPPT systems have been presented. On-chip implementations of the Ripple Correlation Control (RCC) MPPT approach are described in [7, 8]. This MPPT technique relies on analog circuits and a high switching frequency to reduce the size and cost of the passive components necessary for its implementation. The on-chip implementations of the P&O, also known as "Hill-Climbing", MPPT algorithm reported in [9-11] aim to maximize the output power of charge-pump-based low-power DC/DC converters. By altering the switching frequency and conversion ratio depending on measurements of the charge-pump output voltage, a two-dimensional MPPT operation is performed. These methods, however, are inapplicable to switching DC/DC converters that operate at higher power levels. Numerous on-chip implementations influenced by the Fractional Open-Circuit Voltage (FOCV) approach are shown in [12-24]. The disadvantage of using the FOCV MPPT method in PV energy harvesting systems is that energy production is halted during measurement of the PV source open-circuit voltage, which affects the efficiency of energy production. In addition, it necessitates knowledge of

the open-circuit voltage of the PV source, which is dependent on both the manufacturing properties of the utilized solar cells and their configuration in series and/or parallel to form the PV generator for each application.

The MPPT technique of [25] has been implemented in an integrated circuit and is based on varying the duty cycle and switching frequency of a DC/DC converter to maximize the power conversion efficiency while simultaneously ensuring that the input impedance of the power converter settles close to its optimal value, which should be known a priori (i.e. impedance matching). In [26], the MPPT process is accomplished on-chip by altering the duty cycle of the power converter so that its input impedance equals a previously determined ideal value.

The MPPT approach described in [27] has also been implemented in an integrated circuit, however it is only suitable to converter-less energy harvesting systems with particular electrical and operational properties of the supplied electronic load. The MPPT method described in [28] for converter-free energy harvesting devices is based on a negative feedback control loop that follows a specified voltage-frequency curve. In time-based MPPT algorithms [29-31], input source power is estimated by measuring the charging time of a capacitor in the power converter circuit. However, despite the fact that this MPPT technology may be incorporated on-chip, it is only relevant to certain configurations of the power converter circuit and therefore cannot be applied to generic energy harvesting designs.

Analog circuit-based on-chip designs of the P&O MPPT approach are presented in [3, 32-37]. The MPPT circuit in [33] uses Sample and Hold (S/H) circuits, but the MPPT circuit in [36] is based on a mixed-signal multiplier (requiring several capacitors) and an A/D converter, hence increasing the ASIC footprint size and complexity. Similarly, [4, 38-39] necessitate an analog multiplier and S/H circuits. In [40], a variant of the P&O MPPT approach is implemented on-chip; nevertheless, robustness under low irradiance conditions requires the employment of an analog power metering circuit and a complex digital core. Lastly, the P&O methods of [34, 37, 41-43] are all based on analog and mixed-signal circuitry (multiplexers, comparators, integrators, and/or electronic circuits), which increases the design and implementation complexity of the MPPT chip due to the requirement of storing and processing the PV current and PV voltage measurements between consecutive sampling periods while maintaining a high dynamic range and a small chip footprint. Recent work [44] has proposed a mixed signal multiplier for the estimation of power to apply the P&O

approach. Internal analog circuits are utilized to generate pulse-signals with ON times proportionate and inversely proportional, respectively, to the multiplier input voltages. For the on-chip implementation of this MPPT approach, a particular multiplier design is necessary.

Among the numerous MPPT approaches outlined above for use in PV energy harvesting systems, the P&O methodology has the benefits of universality, operational simplicity, and ease of implementation. In addition, it does not need knowledge of the operating features of the PV source (such as PV source output impedance, location of MPPs, open circuit voltage, number of PV cells connected in series/parallel, etc.). Consequently, it can be easily incorporated into commercial PV energy harvesting products where the electrical specifications of the PV source are not known during the industrial manufacturing stage of the PV power management system because they are defined by the user based on the application and installation site meteorological conditions [6].

Existing on-chip implementations of the P&O MPPT technique are based on the use of complex electronic circuits such as analog PV current and voltage multipliers, S/Hs and A/D converters, which increases the implementation complexity and power consumption of the MPPT unit within an integrated circuit, as shown in the prior art review presented above (IC). Also, commercially available chips either require the connection of external analog current and voltage sensors to perform the MPPT process according to the P&O technique (e.g. SM72445 and LT8490) or contain a microprocessor (e.g. MPT612 and PowerPSoC) which increases the complexity of MPPT system implementation on-chip, or they cannot operate with PV sources consisting of a single PV cell (e.g. MAX20800). Alternately, the functioning of commercial MPPT chips is based on the FOCV MPPT approach (e.g. BQ24650, SPV1050, AEM10941, CN3801), which displays substantial limitations in PV energy harvesting applications, as described above.

In this PhD thesis, a unique MPPT control system for on-chip implementation of the P&O MPPT technique is described, which, in comparison to the on-chip MPPT solutions previously provided at both the scientific and commercial levels, has the following benefits:

1. the use of complex circuits such as multipliers, S/H units, A/D converters, or microprocessors is not required,
2. the MPPT algorithm is implemented based on purely digital circuits and, therefore, its operation and performance are not dependent on the chip fabrication technology,

3. no prior knowledge of the operational characteristics of the PV source is required for its operation, and
4. it is applicable across the entire spectrum of PV energy harvesting, utilizing power switch converters of both low- and high-power rating.

Consequently, the MPPT system described in this PhD dissertation may be easily built on-chip with low design complexity, occupying a small space, while keeping the excellent performance characteristics of the P&O MPPT approach. In addition, its performance is unaffected by system noise, which is crucial for managing switching power converters and impacts the performance of analog current and voltage sensing circuits.

The MPPT system presented in this dissertation has been experimentally evaluated in the field under real-world operational circumstances. The experimental findings that demonstrate the successful operation of the developed system and its capacity to manage the MPPT operation of a DC/DC power converter in a PV energy harvesting system in real time, are presented in § 2.6. Section in § 2.3 describes the MPPT system in terms of the circuit-level design of the PV current and voltage sensors and the operation of the digital MPPT unit.

2.3. The MPPT system design

As a reference, Fig. 7 highlights the position of the system to be described in this chapter, focusing solely on the MPPT system design. The same module highlighted in Fig. 7, along with the 'Logic Control' and 'Driver' blocks found in the same container block of a PDTRM cell are the ones containing the logic that will be analyzed in the next chapter, analyzing the EMS of the PDTRM PV cells.

The diagram of the PV energy harvesting system showcasing its interconnections with the 'Power Production Unit' block of Fig. 7, is shown in Fig. 8. A simplistic break down structure of the MPPT under study is depicted as the grey box on the lower part of the image. The power converter of this PhD thesis was designed as a DC/DC converter which is controlled by the MPPT algorithm.

Specifically, the MPPT system of this PhD thesis consists of a Boost-type (step-up) DC/DC power electronic converter, the PV source output current and voltage sensors that are assumed to output the respective values in a linear Pulse Rate Modulation (PRM), and the

MPPT circuit that generates the Pulse Width Modulation (PWM) signals for driving the power transistors of the DC/DC converter based on the P&O MPPT algorithm.

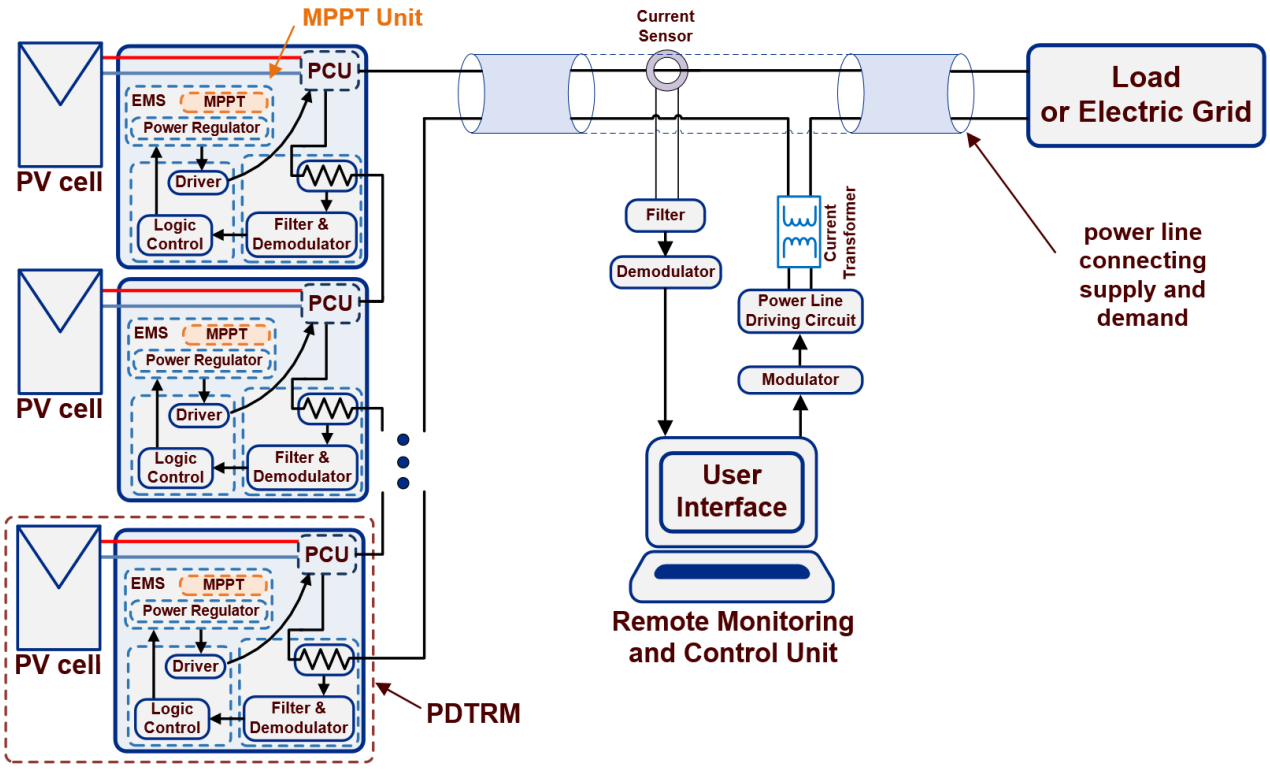


Fig. 7: The general diagram of the PV system investigated in this PhD thesis presenting the MPPT unit of the PV cells.

The optional AC capability for the current inversion is added by a full-bridge which is controlled through the 'Logic Control' and 'Driver' blocks. The AC inverter is the last stage of the 'Power Production Unit' and is fully analyzed in Chapters 3 and 4.

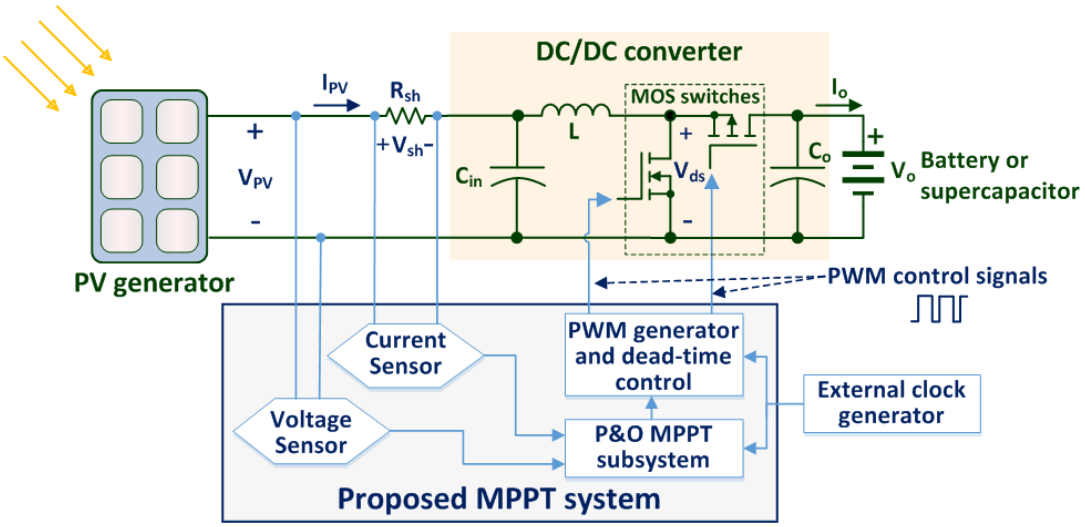


Fig. 8. Diagram of a PV energy harvesting system employing the MPPT control unit.

2.3.1. PRM sensors design

As previously stated, the voltage and current sensor design of the innovative MPPT system is expected to employ PRM, which proposes the usage of a Voltage-to-Frequency (V2F) Converter architecture (VFC) [45] to avoid the complexity and power consumption of Analog-to-Digital (AD) converters. To create the necessary input sensing signals for the digital MPPT block, the PV source output voltage is transformed to a pulse stream with a frequency $f_{V,PV}$ (Hz), that varies proportionately with the PV source output voltage (i.e. V_{PV} in Fig. 8), as follows:

$$f_{V,PV} = k_V \cdot V_{PV} \tag{1.1}$$

where k_V is the gain of the PV voltage sensor.

The voltage that is being fed to the PV current sensor is based on the shunt resistor R_{sh} depicted in Fig. 8. This voltage is equal to:

$$\Delta V_{shunt} = V_{in,1} - V_{in,2} = R_{sh} \cdot I_{PV} \tag{1.2}$$

where $V_{in,1}$ $V_{in,2}$ (V) are the voltages developed at the terminals of R_{sh} with respect to the ground level potential.

The output of this sensor drives the input of a voltage-to-current converter, therefore generating a pulse stream with a frequency, $f_{I,pv}$ (Hz), that fluctuates linearly with the PV source output current (i.e. I_{PV} in Fig. 8) according to the equation:

$$f_{I,PV} = k_I \cdot R_{sh} \cdot I_{PV} \tag{1.3}$$

where k_I is the respective PV current sensor gain.

2.3.2. Digital MPPT control unit design

The subsystem linkages and structural breakdown of the MPPT control unit are shown in Fig. 9. Each module in this MPPT unit is constructed using digital circuitry, and its clock is supplied by an external oscillator. The subsystems employ clock dividers based on digital counters to change the sampling time T_{S_CLK} (sec) and the shape of the DC/DC converter PWM control signal as explained in the next section and shown in Fig. 9.

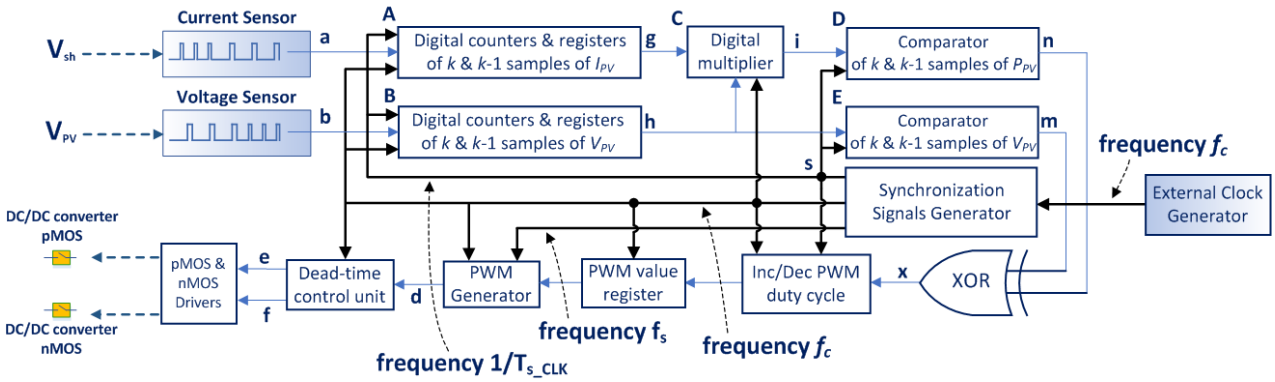


Fig. 9. Block diagram of the MPPT unit.

The operation of the MPPT digital circuit is based on the P&O algorithm. As illustrated in Fig. 6, the derivative of the PV source output power with respect to its output voltage is positive at the left side of the MPP and negative at its right, while the following condition holds at the MPP [6]:

$$\frac{\partial P_{PV}}{\partial V_{PV}} = 0 \tag{1.4}$$

where P_{PV} (W), V_{PV} (V) are the output power and voltage, respectively, of the PV cell/array.

If a Boost-type DC/DC converter operating in the continuous conduction mode is coupled to the PV source's output, the input V_{PV}, and output V_o, voltage levels are linked as follows [46]:

$$\frac{V_o}{V_{PV}} = \frac{1}{1-D} \tag{1.5}$$

where D is the duty cycle of the PWM control signal of the DC/DC converter's nMOS switch.

In addition, the DC/DC converter output is frequently coupled to an energy storage device in PV energy harvesting systems (i.e. battery or supercapacitor). Consequently, V_o stays constant over the brief time span necessary for the MPPT algorithm to converge. Consequently, it is possible to change the operating point of the PV source by adjusting the duty cycle of the PWM signal that drives the DC/DC converter, because according to (1.5), when the duty cycle is decreased, the operating point of the PV source shifts to the right side of the PV power-voltage curve (i.e. higher voltages are developed at the PV source), and otherwise it shifts to the left side of that curve. When the Boost-type DC/DC converter runs in the discontinuous-conduction mode, the nonlinear $D = g(V_{PV})$ characteristic equation given in [46] must be accounted for. In this scenario, because the current-voltage

characteristic of a PV source dictates that $\frac{\partial I_{PV}}{\partial V_{PV}}$ is less than zero and V_o is greater than V_{PV}, the following condition holds:

$$\frac{\partial D}{\partial V_{PV}} < 0 \tag{1.6}$$

Therefore, a similar operation with the continuous conduction mode, which has been described above, is also achieved in the discontinuous-conduction mode of the Boost converter.

According to (1.1) and (1.3), the number of pulses of the PV current and voltage sensors during a sampling period, $N_{I,PV}$ and $N_{V,PV}$, are proportional to I_{PV} and V_{PV}, respectively:

$$N_{I,PV} = f_{I,PV} \cdot T_{S\_CLK} \tag{1.7}$$

$$N_{V,PV} = f_{V,PV} \cdot T_{S\_CLK} \tag{1.8}$$

where T_{S_CLK} (sec) is the sampling period. Therefore, the product $N_{P,PV} = N_{I,PV} \cdot N_{V,PV}$ is proportional to P_{PV}. By measuring the values of $N_{P,PV}$ and $N_{V,PV}$ in the MPPT system, the condition for convergence to the MPP given by (1.4) is transformed as follows:

$$\frac{\partial P_{PV}}{\partial V_{PV}} = 0 \quad \Leftrightarrow \quad \frac{\partial N_{P,PV}}{\partial N_{V,PV}} = 0 \tag{1.9}$$

In this innovative P&O MPPT unit, the necessity for analog multipliers, S/Hs, A/D converters, and other analog circuitry has been eliminated. To manage the DC/DC power converter, the duty cycle, $D(k)$, of the PWM control signal for the DC/DC converter (with time step k) is adjusted as follows:

$$D(k) = D(k-1) - \alpha \cdot sign\left(\frac{\partial N_{P,PV}}{\partial N_{V,PV}}(k)\right) \tag{1.10}$$

where $\alpha > 0$ is a constant and the function $sign(\cdot)$ is defined as follows:

$$sign(x) = \begin{cases} 1 & if\ x > 0 \\ -1 & if\ x < 0 \end{cases} \tag{1.11}$$

The digital values of $N_{P,PV}$ and $N_{V,PV}$ in (1.7)-(1.10) are respectively stored in 40-bit and 20-bit registers. The value of T_{S_CLK} should be greater than the time necessary for the DC/DC power converter to achieve steady state after a duty cycle disturbance, as determined by the formula (1.10). On the basis of [46], the latter may be computed based on the power converter circuit design in each PV application of interest. A high value of α in (1.10) allows for a more rapid convergence to the MPP [47]. This is appropriate for PV applications in where the

incident solar irradiance varies regularly (e.g., owing to shade when the PV system is mounted in an urban setting, or on moving surfaces/vehicles, etc.). However, the amplitude of oscillations around the MPP is also enhanced following convergence of the tracking process.

In order to implement the MPPT control law described by (1.10), the pulse-rate modulated digital outputs of the PV output current and voltage sensors (signals **'a'** & **'b'** in Fig. 9) trigger the corresponding digital counters (blocks **A** and **B** in Fig. 9) which sum the received events per sampling period and produce the binary values of $N_{I,PV}$ and $N_{V,PV}$, respectively. The registers in blocks **A** and **B** store the samples of $N_{I,PV}$ and $N_{V,PV}$ during the sampling periods k and k-1. In block C, the corresponding values of $N_{I,PV}$ and $N_{V,PV}$ are digitally multiplied to obtain the values of $N_{P,PV}$ at the k and k-1 sampling periods, i.e. $N_{P,PV(k)}$ and $N_{P,PV(k-1)}$, respectively. Then, the pairs [$N_{P,PV(k-1)}$, $N_{V,PV(k-1)}$] and [$N_{P,PV(k)}$, $N_{V,PV(k)}$] are processed by digital comparators (blocks D and E), which raise their output to a logic "1" in case that $\Delta N_{P,PV(k)} = N_{P,PV(k)} - N_{P,PV(k-1)} > 0$ or $\Delta N_{V,PV(k)} = N_{V,PV(k)} - N_{V,PV(k-1)} > 0$, else, they output a logic "0". Therefore, since (1.10) is implemented through comparison of successive samples of $N_{P,PV}$ and $N_{V,PV}$, knowledge of the exact values of the sensors gains k_V and k_I in (1.1) and (1.3) is not required for the development (e.g. for adjustment of circuit parameters) and operation of the respective digitalized MPPT unit.

When $\Delta N_{P,PV(k)}$ and $\Delta N_{V,PV(k)}$ have the same polarity, the output will indicate a duty cycle decrease, , i.e. $0 \oplus 0 = 0$ and $1 \oplus 1 = 0$ according to equation (1.10), where '$\oplus$' is the Boolean symbol for the XOR operation. Similarly, when $\Delta N_{P,PV(k)}$ and $\Delta N_{V,PV(k)}$ have reversed polarity, the output will indicate an increase in the duty cycle (i.e. $1 \oplus 0 = 1$ and $0 \oplus 1 = 1$). The XOR output is routed to a digital subsystem that raises or reduces the digital output of a counter corresponding to the duty cycle value of the final PWM control signal of the DC/DC converter by an amount equal to α [as determined by (1.10)]. The output of the 'Inc/Dec PWM duty cycle' block is sent into the 'PWM Generator' module, which is constructed in accordance with [48] and contains the digital logic that generates a square-wave PWM control signal with the appropriate duty cycle for controlling the power switches of the DC/DC converter. The resultant PWM signal is then sent (by signal **'d'** in Fig. 9) to the dead-time control unit, which adds minor delays to prevent cross-conduction between the nMOS and pMOS power switches of the DC/DC converter, which have non-zero turn-on/off delay times.

In order to create twice as many different duty cycle values, a custom module was inserted into the 'PWM Generator' block that employs two counters, the first of which is activated on the rising edge of the clock and the second on the falling edge. The following equation describes the relationship between the PWM frequency of the DC/DC converter, f_s, the frequency of the global clock, f_c, and the duty cycle range, DR.

$$DR = 2 \cdot \frac{f_c}{f_s} \tag{1.12}$$

In order to implement a PV MPPT system using the proposed digital design, the value of f_s should initially be chosen by the designer of the DC/DC converter such that:

(i) the switching speed limit of the power switches employed [see Fig. 8, e.g. Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFETs), Insulated-Gate Bipolar power Transistors (IGBTs) etc.] is not exceeded and

(ii) the resulting switching power losses and volume of the inductive and capacitive components of the DC/DC converter satisfy the desired specifications, as described in [46].

In general, once this design is ready to be manufactured, the value of f_c needs to be selected according to the specifications of the chip fabrication technology used, such that the power consumption of the digital circuits is kept to a low level.

In conclusion, the MPPT unit presented in this PhD thesis is based on the application of the P&O approach in a digital subsystem, whilst the analog circuit design was limited to the initial stages of the PV current and voltage sensors. The primary benefit of this feature is that the digital P&O subsystem of this PhD thesis can be designed using a hardware description programming language (such as Very High Speed Integrated Circuit Hardware Description Language or VHDL) independent of the final fabrication technology of the chip, thereby requiring a low chip design effort. In contrast, its analog counterpart would require extensive circuit design (e.g., calculation of component values, adjustment of voltage thresholds, extensive simulations such as corner and/or Monte Carlo analyses, etc.), which is dependent on the target fabrication technology of the chip and would necessitate a redesign if a different chip fabrication technology is chosen. Additionally, in the MPPT unit given in this PhD dissertation, the integrated circuit noise does not influence the majority of the overall MPPT system since it is built on digital circuits, but in a purely analog MPPT system, the whole circuit would be susceptible to noise.

2.4. Implementational specifics regarding the MPPT logic design functionality

This paragraph describes a series of features including improvements that have been added to the logic design of the units involved in the MPPT circuit configuration. Since the basic operating principle and the main circuits of the MPPT subsystem have already been described in detail in the previous paragraphs, this paragraph is limited to the presentation of these additions specifically. The additions are realized with the design and implementation of extra inputs and outputs which are dedicated in providing external user functions and debugging results, respectively.

For example, one input is used to change the duty cycle stepping to either fast (4/128 % per sampling period) or slow (1/128 % per sampling period) in order to adjust the PWM feedback loop of the DC/DC converter response. Another input is added so that the user can intervene to the direction of the duty cycle, by selecting to either minimize it or leave it floating towards the direction that is being calculated by the algorithm. Also, one more input has been added allowing the user to invert the result calculated by the XOR, in case the user wants to use the same MPPT logic with a buck-boost DC/DC converter.

As to the additional outputs, part from the inverter signal of the PWM driver, there are two more debugging signals that indicate when the PWM duty cycle has reached its lowest and highest value (0 and 128, respectively) and one more output which is dedicated to toggling the current sensor operation as the latter may be consuming energy when operating. In this PhD thesis, the operational time of this current sensor was chosen to be at 50% and its activation triggering begins at each sampling period which means that it stays off for the second half of every sampling period.

During the implementation and the debugging of the MPPT design of this PhD thesis, a number of internal signals were used as inputs or outputs being fed directly with data, in an open-loop configuration, as the closed-loop design could only be verified at the last stage of the process which would include the response of the DC/DC converter and the V2F sensors. The need for simulating an open-loop system and the facilitation of polling by direct feed and debugging of the internal signals becomes more evident by the analysis complementing the illustration of the VHDL blocks in the following paragraph. These diagrams are provided as an example to present an early basic version of the MPPT design, displayed in the format of Register Transfer Level (RTL).

2.4.1. A basic review of the MPPT RTL design

Fig. 10 shows the first level of the hierarchical structure that implements the digital logic subsystems (white blocks presented in Fig. 9).

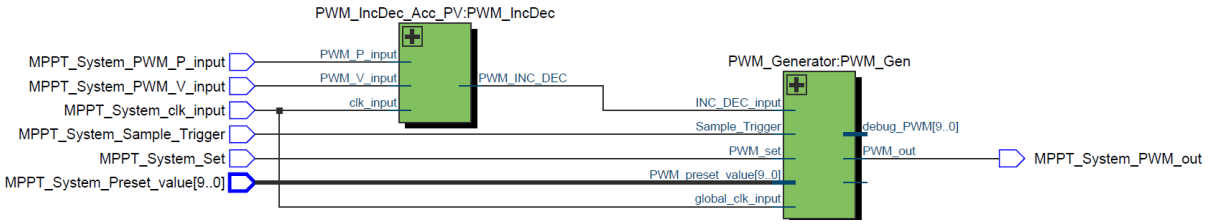


Fig. 10: The implementation of the digital subsystems in VHDL code (1st Level).

The PWM_IncDec block contains the logic for the first 2 digital logic stages of Fig. 9, i.e. the 'A', 'B', 'C', 'D', 'E', 'XOR' and 'Inc/Dec PWM duty cycle' blocks, and the PWM_Gen contains the next 2 digital logic stages of Fig. 9, i.e. the 'PWM value register' and the 'PWM Generator' block.

The 1st and 2nd inputs expect 1-bit signals in an PRM format. The 1st input receives the current sensing data but it is distinguished with distinctive letter 'P' as a reminder that it will later on be multiplied with the value of the 2nd input to represent the value of power rather than current. The 3rd input receives the digital clock pulses which here are supplied by a signal generator but in the actual on-chip realization they will be produced by a properly configured ring-oscillator. The 4th input triggers the sampling of the MPPT algorithm and in the final version it pertains to an internal signal. The 5th signal is dedicated to setting and re-setting the MPPT operation by forcing the generated PWM duty cycle to receive a specific value (when it becomes 1). The 6th input receives the 10-bit vector signal that holds the target duty cycle value to be set by the 5th input, when the user decides to do so (for debugging purposes). Fig. 11 expands the blocks of Fig. 10 in order to expose the reader to more details regarding the VHDL logic structure.

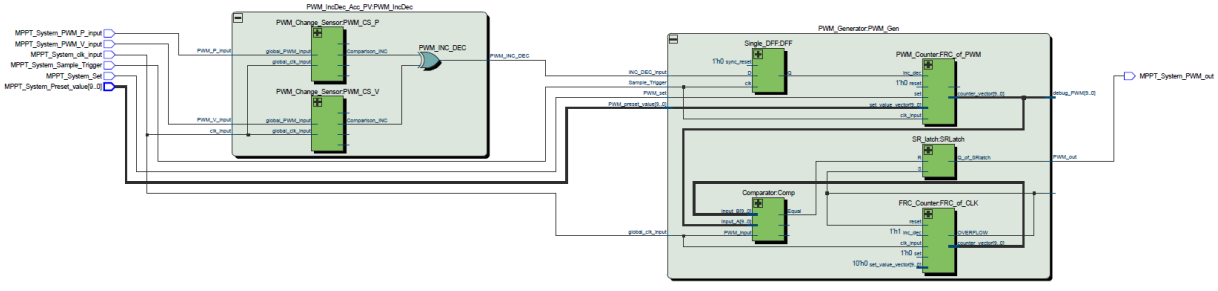


Fig. 11: Detail of Fig. 10 (2nd Level).

Fig. 12 shows an enlarged view of the left part of Fig. 11, which contains the subsystems of the 2 comparators as well as the XOR that receives its outputs and decides whether the value of the generated PWM should be increased or decreased. Excluding the clock input, this block has 2 inputs and one output.

Fig. 13 shows an enlarged view of the right part of Fig. 11, which takes care of incrementing or decrementing the counter (the 'FRC_of_PWM' in the upper right) which holds the value of the current PWM generated pulse and which changes value (through the DFF in the upper left) only when a rising pulse from 0 to 1 comes from the 'Sample_Trigger' input, which is the input that receives the signal of the Sampling and Hold (S&H) stage. The other 3 blocks in the bottom half of 'PWM_Gen' ('SRLatch', 'Comp' and 'FRC_of_CLK') take over the generation of the PWM pulse stream and essentially constitute the 7th digital logic stage ('PWM Generator' block) of Fig. 9.

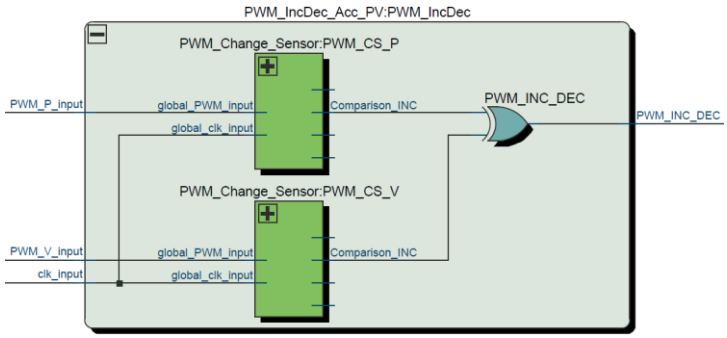


Fig. 12: Detail of Fig. 11 (2nd Level): the two comparators and the XOR that make up the first two digital processing stages of the MPPT.

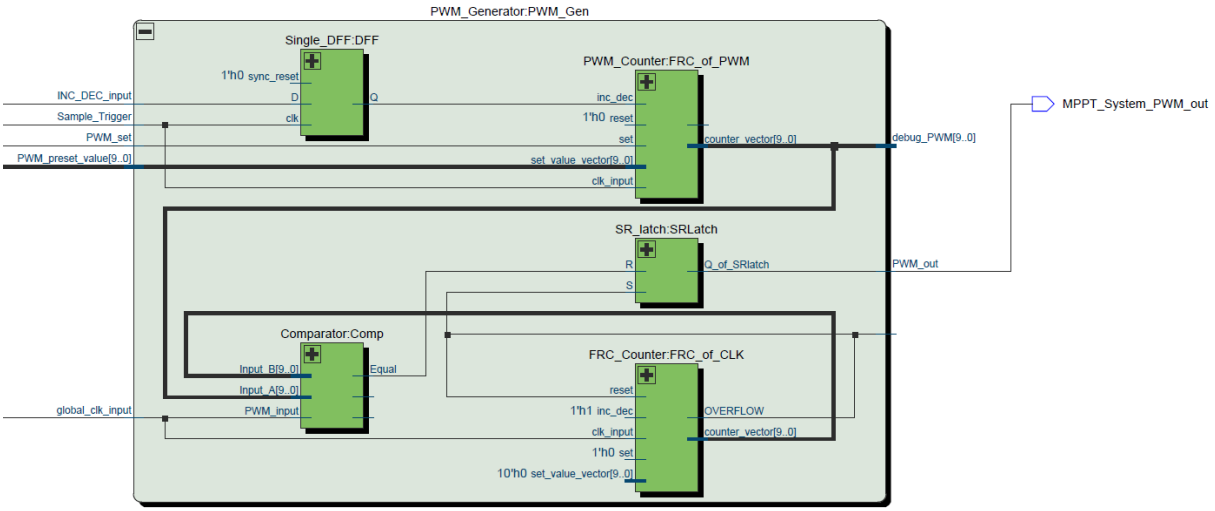


Fig. 13: Detail of Fig. 11 (2nd Level): the circuit for processing the PWM Inc/Dec decision and generating the appropriate pulse stream.

An important note regarding the proper operation of the digital logic shown in Fig. 13 concerns the final values that the 'FRC_of_PWM' and 'FRC_of_CLK' counters can take, namely, that the final value (ceiling) of 'FRC_of_PWM' be at least 1 less than the final value (ceiling) of 'FRC_of_CLK'.

In Fig. 14, the subsystem presented in Fig. 12 is further expanded to reveal the sub-blocks of the comparators (3rd Level) which are identical with each one of them consisting of the left block which controls the two rightmost blocks that implement a 10-bit comparator and a counter. The counter registers the clock cycles number that pass while the signals received from the last analog stage (PWM P and PWM V) remain in the 'on' state. This requires that the digital clock must have a high frequency so that the range of values that these counters can take (here 10-bit, i.e. 1024 clock pulses) is not exhausted within the time interval that the PWM pulses (P and V) are in 'ON' state.

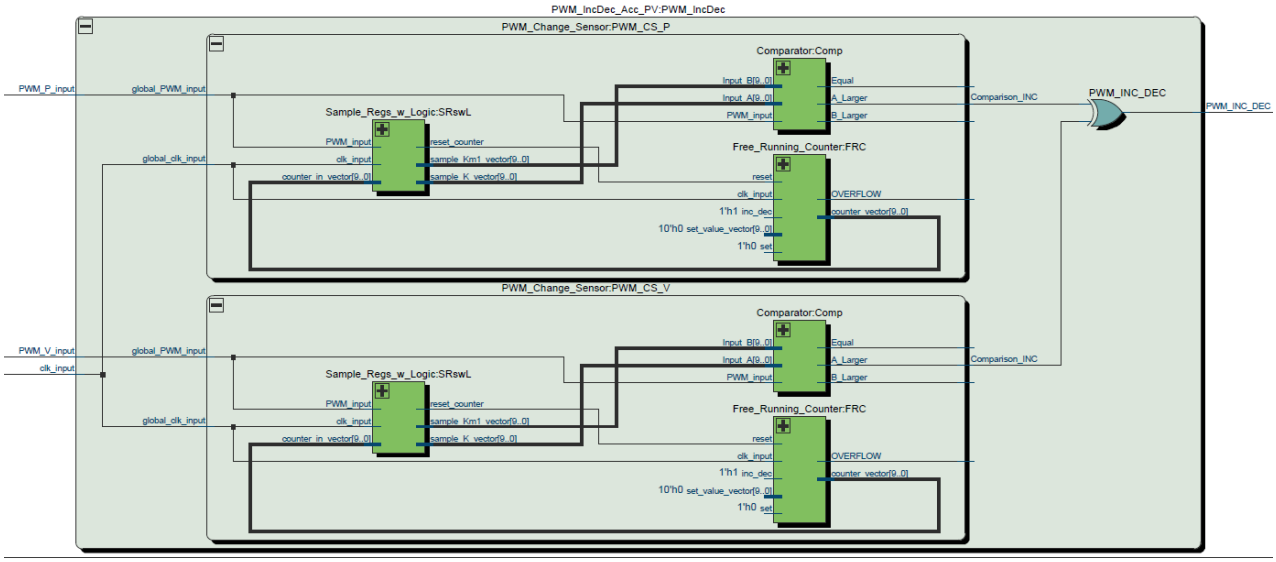


Fig. 14: Detail of Fig. 12 (3rd Level): the interior of the comparators.

The same design principles have been followed for the development of the VHDL code throughout the whole course of this PhD thesis. However, the rest of the implementations are far more complex and the illustration of the blocks in an RTL format will not serve as an informative medium for the reader. Instead, the design ideas, the parameterization choices, the features and functionalities of the modules that follow on the rest of this work will be described using specially prepared block diagrams enriched with the necessary explanatory semantics, as the ones found in Fig. 7, 8 and 9.

2.4.2. Soft start and control of the MPPT unit power consumption

The PV source (i.e. cell or array) may consume more power than it receives at a given time. Also, the same unit should start to modulate its MPPT duty cycle at a low rate as sudden changes during start-up can lead to large current values which, if leaked, can destroy the power switches and any other vulnerable circuitry, especially in case of on-chip implementation of the DC/DC power converter. For these two reasons, the circuit of Fig. 15 was designed where the additional digital logic is completed around the MPPT circuit as shown in Fig. 9.

The added digital logic takes over the control of the duty cycle values according to the received power. If the received power is lower than a given value (let this be called P_{min}) the circuit undertakes the management of the MPPT duty cycle at a slow rate as it enters the 'Soft Start' state. The slow rate of change of the duty cycle ensures that the current flowing through the power circuit will be limited to small values. The duty cycle rate of change resumes once the absorbed power exceeds P_{min}. From that point on, this rate will not decrease again unless the 'Soft Start' process is automatically re-engaged. This only happens if all relevant digital structure loses power and restarts at some point in time (also called a hard-reset).

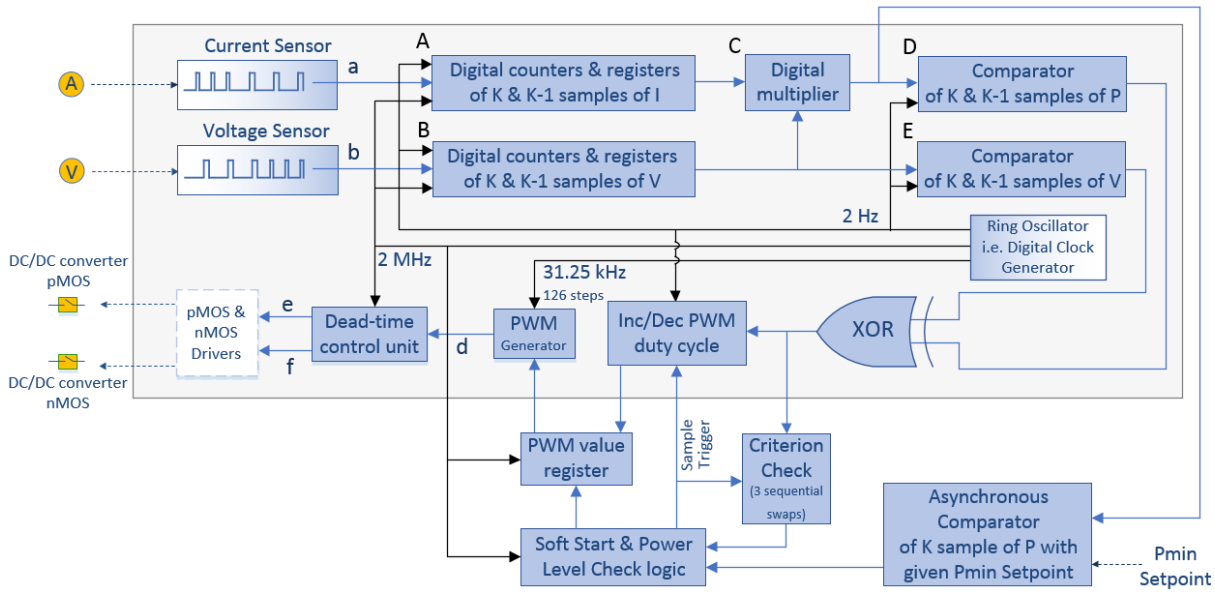


Fig. 15: The 'Intake Power Control and Soft Start' circuit as developed around an enriched alternative structure of the 'MPPT & PWM' module.

Given that the power has exceeded P_{min} and that the MPPT circuit is operating normally, when, at some point in time, the power becomes less than P_{min} once again (for example if there is deposition of dirt, or a cloud shading the PV cell, or as while it gets dark towards night

hours of the day), the circuit periodically freezes the detection process of the MPPT keeping the duty cycle constant at its most recent value. Freezing occurs only if the device is found to draw power less than P_{min} and only if the duty cycle is found to make more than a number (here 3) oscillations around an operating point, which implies that it is close to the MPP.

2.4.3. Sensing range

The sensing range of the PRM sensors is selected by taking into consideration the following factors: (a) the characteristic operating curves of two types of VF2 voltage and current sensors, and (b) the specification stating that each measurement (sampling rate) of the MPPT algorithm will be made in steps starting from 10 measurements per second to 1 measurement at 10 seconds (0.1 to 10 samples per sec). This meant that the corresponding digital counters need to be able to hold countable values ranging from 7 to 800,000 events per sample. In this PhD thesis, two different versions of voltage/current sensors, which were fabricated on-chip, have been considered:

Type 1:

- Output pulse frequency range f_{out} (corners) f_{min} ~20 kHz to f_{max} ~80 kHz
- Output pulse frequency range f_{out} (typical) f_{min} ~24 kHz to f_{max} ~53 kHz

Type 2:

- Output pulse frequency range f_{out} (corners) f_{min} ~0.07 kHz to f_{max} ~1.43 kHz
- Output pulse frequency range f_{out} (typical) f_{min} ~0.12 kHz to f_{max} ~0.88 kHz

For example, given that the system clock will be clocked at 1 MHz, when the sampling rate is every 1/10 of a second then 100.000 clock pulses will be intercepted between two consequent samples, while when the sampling rate is once per 10 seconds, then 10.000.000 clock pulses will be intercepted between two consequent samples. The clock cycles that mediate between two consecutive samples, both during 'Soft Start' mode and in MPPT mode, are provided as parametric inputs in the first implementation stages of the design. In the final version it was decided that these will reflect to a period of 1 and 2 seconds, respectively. The registers that receive these values need a 24-bit range (here 25-bit registers were used for the 2's complement safe margin). Accordingly, to count the 800,000 events, 18-bit registers are sufficient (so 20-bit registers were used) and to store the product of Current x Voltage (previous and current values) 40-bit registers were used.

2.4.4. Doubling the duty cycle range

As the design uses a single clock frequency source (e.g. a frequency generator, or a ring-oscillator), which is f_c = 3.2 MHz (which was later reduced to 2.0 MHz) and since the DC/DC converter needs to be driven to high frequencies (for proper component sizing and power consumption purposes), here f_s = 50 kHz, the duty cycle will be able to receive 64 discrete values. This means that the duty cycle (from 0 % to 100 %) will change in steps of 100/64 % since the available range is calculated as clock tick groups of f_c / f_s = 3.200.000/50.000 = 64.

To increase this range, an array of two counters was created so that each one of them will count the events either on the rising or the falling edge of the clock, respectively ('FRC_10bits_both_on_Rising_and_Falling'). This way, these events can be summed at twice the frequency of the clock. Thus, instead of 64 clock steps per PWM pulse, 128 clock steps (7-bit) are applied. This arrangement has been inserted into the 'PWM Generator' module shown in Figs. 10 and 11.

2.5. Simulation results and refinements

2.5.1. Duty cycle range doubling simulations

Fig. 16 illustrates the correct behavior of the duty cycle range doubling described in § 2.4.4. The actual clock ticks are set to 126, with the count ranging from 0 to 126, which translated into 127 distinct values and not 128. This is because of the way that the digital logic shown in Fig. 13 is operating. The simplistic design of Fig. 13 exploiting the functionality of the 'SRLatch' suggests that the final value (ceiling) of 'FRC_of_PWM' is at least 1 less than the final value (ceiling) of 'FRC_of_CLK'. The same ceiling is changed to 123 when a step of 4 is selected in the duty cycle stepping.

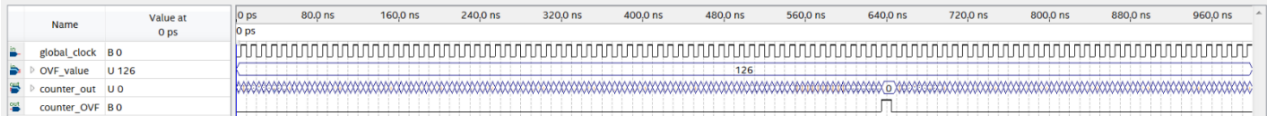


Fig. 16. Illustration of the correct operation of the composite counter that sums events on both the rising and falling clock pulses.

Various tests were performed to confirm that all the digital logic related to the counters that count on both the rising and falling edges of the clock can support this change. It was

necessary to add comparators that are correctly synchronized on the one hand, and dedicated checks for the proper rising and falling edges of the clock in respect to these comparators, on the other. Also, it was required to add delays and checks and an extra measurement of the double counting result, which was chosen to be for the past value to ensure the stability in the output results as the double counter changed values relative to the value of the counter changing sign (from 1 to 0) of the PWM. This concerned the comparators that control the double FRC counter (128 values) in relation to the PWM counter, as well as the logic that determines how and when to reset these counters.

2.5.2. Simulating the generic case

Fig. 17 depicts the simulated waveforms of the key MPPT logic signals seen in Fig. 9. This simulation contains the main clock, the output of the current sensor (signal 'a'), and the output of the voltage sensor (signal 'b'). The vector signals 'g' and 'h' are the outputs of the current and voltage registers, which store the counter values of the number of digital pulses per sampling period in decimal form. The 'i' vector signal corresponds to the product of 'g' and 'h' and contains input power samples. The sampling trigger pulses are included in signal's'. The signals 'm' and 'n' represent the outcomes of the comparators of two successive voltage and power samples, respectively. These comparators produce a logic 1 if $\Delta N_{V,PV(k)} > 0$ and $\Delta N_{P,PV(k)} > 0$, and a logic 0 otherwise. The signal 'x' is produced by applying the XOR technique to the signals 'm' and 'n'. Its waveform verifies the expected result, which is to raise the duty cycle when $\Delta N_{P,PV(k)} / \Delta N_{V,PV(k)} < 0$, and lower it otherwise.

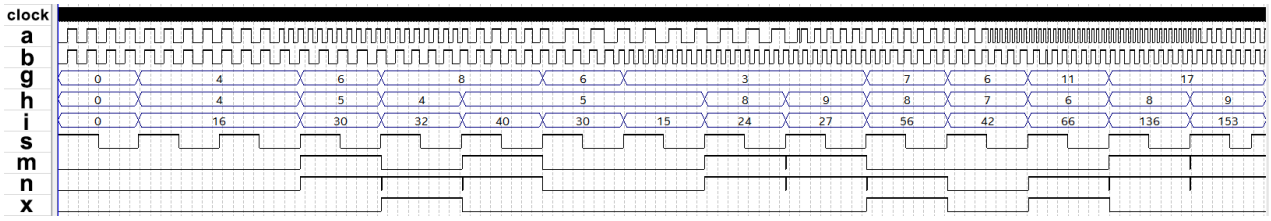


Fig. 17. Simulated waveforms of principal logic signals of the MPPT control unit.

2.5.3. Adding a duty cycle reset notification signal

To control the duty cycle level, two output signals were added to the PWM generator module. The first one becomes 1 (meaning that it is raised to the high-level state) when duty cycle = 0 and is called 'DC_IS_ZERO' and the second one becomes 1 when duty cycle = max and is called 'DC_IS_MAX'. Fig. 18(a) presents the 'PWM_out' signal which gradually reduces

its duty cycle up to the point that it reaches its minimum value around 1.14 μsec where the 'DC_IS_ZERO' flag output is triggered. Similarly, Fig. 18(b) presents the 'PWM_out' signal which gradually increases its duty cycle up to the point that it reaches its maximum value around 1.45 μsec where the 'DC_IS_MAX' flag output is triggered. The 'Max_DC_steps' denote that maximum duty cycle value which is 123 although the increment and decrements in this example happen with a stepping of 1, because the same simulations were used to test the stepping of 4. At the early stages of this implementation the setting point was 123 to cover both stepping. On a later version it was corrected so that it would change to 126 when the stepping was chosen to be 1.

Fig. 18. Confirming the correct operation of the MPPT, as well as the operation of: (a) DC_IS_ZERO and (b) DC_IS_MAX.

2.5.4. Adding duty cycle step selection signal (1 or 4 steps)

As already mentioned in § 2.4, an additional input signal was created in the PWM Generator module, which selects whether the duty cycle will change every one step (represented as logic 0) or every 4 steps (represented as logic 1). For reasons that relate to the fact that there needs to be an adequate difference between two consequent duty cycle outcomes in terms of current change and voltage change, it was decided that the minimum

value of the duty cycle range will be 2 for stepping = 1 and 6 for stepping = 4. The simulations to follow confirm that the duty cycle changes are kept within the intended value range and that the PWM can change its values in a linear manner, regardless of stepping, from 6 to 123. In the final version, the duty cycle range for step = 1 was converted from 2 to 125 and for step = 4 from 6 to 125, as the duty cycle must always start with a value greater than the step size. For duty cycle values less than 1 or 5, respectively, the PWM duty cycle was set to 0 % and for values greater than 124 the PWM duty cycle was set to 100 %. So when the duty cycle step = 1, the PWM output signal can change in a total of 122 steps, taking 1.6 % as the first non-zero value (increasing linearly by about 0.8 %), while when on duty cycle step = 4, the PWM output signal changes in a total of 29 steps, taking 5 % as the first non-zero value (increasing linearly by about 3.4 %).

2.5.5. Adding signals to control the MPPT result and/or the duty cycle direction

Additionally, as already mentioned in § 2.4, an input signal ('SEL_DEC_OR_DEC_INC') was included which forces the MPPT to stop and the duty cycle to be reduced by a constant step when it has a logic value of 0, or it just allows the MPPT to proceed uninterrupted when it has a logic value of 1. The same logic circuit ensures that if the duty cycle has reached 0 then the 'Soft Start' process reactivates before the MPPT begins.

Furthermore, again, as already mentioned in § 2.4, for both debugging reasons and to ensure that the same structure will be able to control both boost and buck converters, one extra signal was introduced which reverses the duty cycle fluctuation direction (the result of the ΔP/ΔV comparisons of the P&O algorithm).

Finally, an extra logic was implemented in the early designs, adding two extra internal signals where the 1st one would select whether the output of INC/DEC would be as is or whether it would be functioning as its complement (by introducing the 'SEL_XNOR_OR_XOR' and a 1-bit MUX). This was followed by a two-input AND gate, through which the 2nd additional signal ('SEL_DEC_OR_DEC_INC') was passed, to select whether the 'OUTPUT_INC_DEC' output will remain 0 as long as a low logic state (0) is applied or whether it will change values reflecting the 'Result_of_XNOR_OR_XOR_selection' signal values. This logic was added targeting to invert the effect that the input of the 'SEL_DEC_OR_DEC_INC' has when it is enabled, meaning to increase the duty cycle values bypassing the MPPT driver commands, instead of decreasing the duty cycle values (bypassing the MPPT driver commands). These

two extra signals were only used for debugging purposes and they were removed along with the accompanying logic on later stages of the design.

2.5.6. Proactive fix of INC/DEC and PWM output jitter

During early simulations it was found that the PWM output was presenting a jitter effect which soon was found to be caused by a software design choice that required the propagation of a signal for a single clock cycle, forcing the INC/DEC signal to be reset (and thus to reach the value of zero) every time there was a sample trigger event.

Also, since the duty cycle is limited to a range that does not allow its values to reach the 0 % or the 100 %, the actual PWM signal will never be a straight line either in a constant low logic state (0) or a high logic state (1), unless it is explicitly programmed to do so, when it reaches the minimum and maximum duty cycle setpoints. The addition of that VHDL code allowed for the PWM to reach the absolute 0 % and 100 % by forcing the signal to receive either the logic state 0 or 1, when the duty cycle was equal to its minimum or maximum value, respectively.

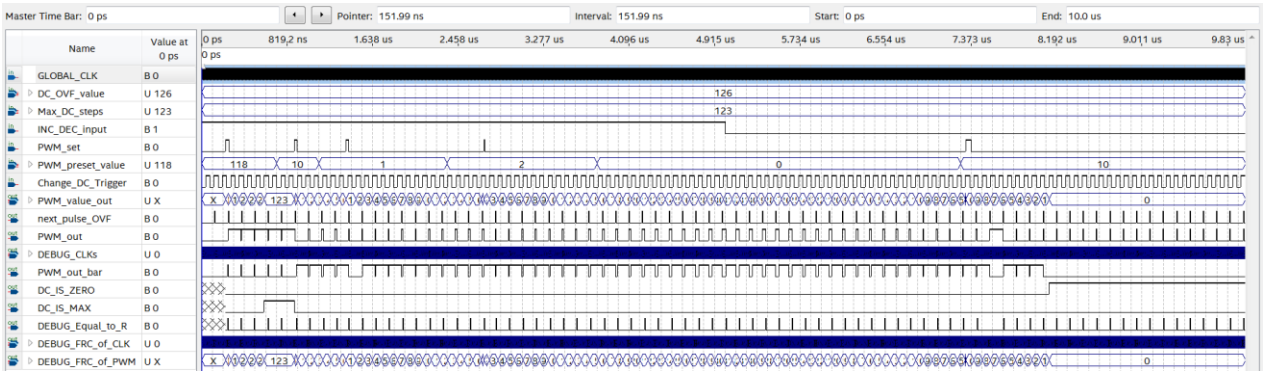


Fig. 19. Revealing the jitter of the PWM outputs when the duty cycle has reached maximum value and also, verifying the correct operation of the PWM presetting, the DC_IS_ZERO and DC_IS_MAX flags and the increment/decrement of the duty cycle in respect to INC/DEC.

The snapshot of Fig. 19 reveals this effect in the 'PWM_out' and 'PWM_out_bar' signals at the time that the 'DC_IS_MAX' = 1. In the simulations to follow this effect has been corrected and the 'PWM_out' is a smooth line in these cases. Also, Fig. 19 verifies the correct operation of the system when the INC/DEC signal is set to either 1 or 0, forcing the duty cycle to increment or decrement by one, accordingly. Also, the same figure verifies the proper setting of the 'PWM_preset_value' and 'PWM_set' inputs. In later versions, these two inputs are automatically controlled by the 'Soft Start' digital logic to ensure that the duty-cycle keeps its

last value when the circuit enters a low power state. This ensures that if an object shadows the PV cell, causing it to lose power, the latter will be protected from a duty-cycle value that would cause a sudden high-current flow once the object that created the shadow effect is removed.

2.5.7. Modifications to eliminate metastability issues

Two 2-stage DFF synchronizers were added to the 'Event Input' inputs of the improved counters that count the (asynchronous) events output of the two PRM voltage and current sensors, for the time duration among two samples.

Three more synchronizers were also added to the 'PWM_Generator' module, one to synchronize the 'Change_DC_Trigger' input, which changes whenever the duty cycle changes, one for the SR Latch output that generates the PWM signal, and one to synchronize the output signal that notifies the zeroing of the duty cycle (DC_IS_ZERO).

Also, three extra synchronizers were added to the 'IncDec_Acc_PV' module to protect the 'KEEP_CURRENT_SENSOR_OFF', 'SEL_XNOR_OR_XOR' and 'SEL_DEC_OR_DEC_INC' inputs, which (a) control the measurement of the PRM current sensor events, (b) change the polarity of the P&O algorithm and (c) provide the option to decrease the PWM duty cycle or control the PWM according to the MPPT results, respectively.

Finally, the RS latch in the 'PWM Generator' was rebuilt using a D-type flip/flop and appropriate combinational logic. This resulted in two versions, a 'DFF_with_XOR' and an 'SR_latch_Toggler', which was kept as the preferred solution. Finally, the use of a synchronizer at the output of the RS latch was chosen to further reduce the possibility of occurrence of metastability phenomena.

2.5.8. Checking the soft start and the current sensor duration of operation

To control how long it takes to measure all the required samples in each iteration of the MPPT control loop, a separate current sensor enable signal was added (0 enables the sensor and 1 disables it). The signal was added to the IncDec_Acc_PV module which is connected to the CLK input of the Event Counter to measure the current (with an OR) to pause the increment for as long as 1 is valid. The counter resets to zero on the next sample trigger signal. The signal is named 'KEEP_CURRENT_SENSOR_OFF' to indicate that a high-state (positive logic, or 1) disables the current sensor measurement circuitry.

The simulation results shown by Fig. 20 verify the correct operation of:

- the duty cycle stepping ('MPPT_System_DC_Step_1_or_4') as shown by the highlighted area **A**,
- the correct calculation of the 'MPPT_Power_Level_20bit' in respect to the values of the 'MPPT_MONITOR_Current' and the 'MPPT_MONITOR_Voltage' values
- the INC/DEC output signal presenting no jitter ('MPPT_IC_DEC_out'),
- the signal 'MPPT_System_SEL_DEC_OR_DEC_INC' that bypasses the MPPT results and decrements the duty cycle, as shown by the highlighted area **B**,
- the signal 'MPPT_System_SEL_DEC_OR_DEC_INC' in combination with the INC/DEC output signal, with the latter being ignored for the period of 6 sec to 7.5 sec, since the former has priority,
- the signal 'MPPT_System_Preset_Value' and the vector 'MPPT_System_Set' as shown by the highlighted area **C**,
- the logic that controls the power saving mode of the current sensor ('MPPT_System_KEEP_CURRENT_SENSOR_OFF') as shown by the highlighted area **D**,
- the 'MPPT_System_PWM_out' signal which follows the duty cycle values,
- the MPPT algorithm directing the duty cycle to increment since the values of the 'MPPT_System_FREQ_I_Input' and 'MPPT_System_FREQ_V_Input' are kept constant, and
- the 'MPPT_System_DC_IS_ZERO', which can be cross-checked by the values of the 'MPPT_PWM_value_out'.

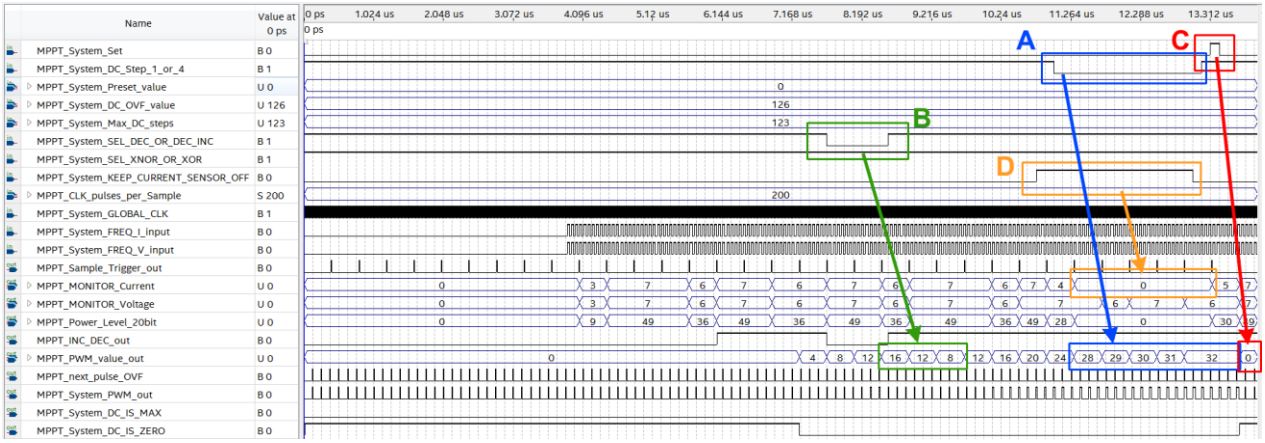


Fig. 20. Verifying the correct operation of various MPPT features.

The following two figures present the results of two simulations which were conducted by using realistic PRM signals (meaning the 'MPPT_w_SS_n_PLC_I_Input' and the 'MPPT_w_SS_n_PLC_V_Input') which change the frequency of their pulses either in similar or opposite directions. This forces the calculated INC/DEC to change the duty cycle either by increasing or decreasing it. The signal that represents the PWM signal ('MPPT_w_SS_n_PLC_PWM_out') is changing its duty cycle as expected, thus verifying the correct operation of the MPPT algorithm. It is worth noting the when the signal 'MPPT_w_SS_n_PLC_SEL_DEC_OR_DEC_INC') is set to 0, the MPPT algorithm stops its normal operation and decreases the duty cycle of the PWM output. Also, it is worth noting that the 'MPPT_w_SS_n_PLC_SET_SENSOR_OFF' becomes wider when the duty cycle is close to zero as indicated by the 'MPPT_w_SS_n_PLC_DC_IS_ZERO' signal.

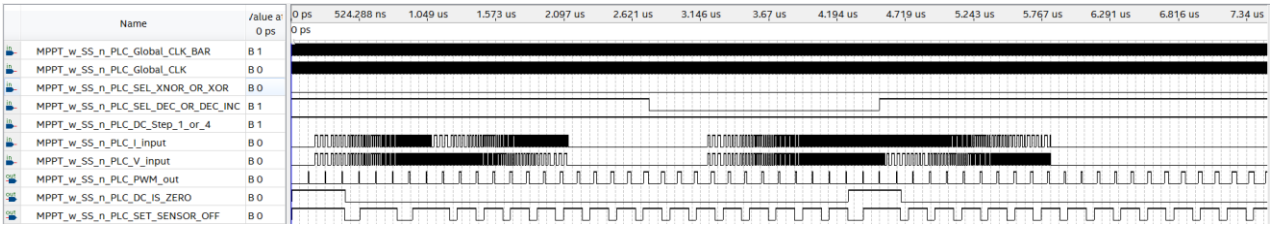


Fig. 21. Verifying the correct operation of the MPPT duty cycle changes under realistic PRM signals with varying frequencies.

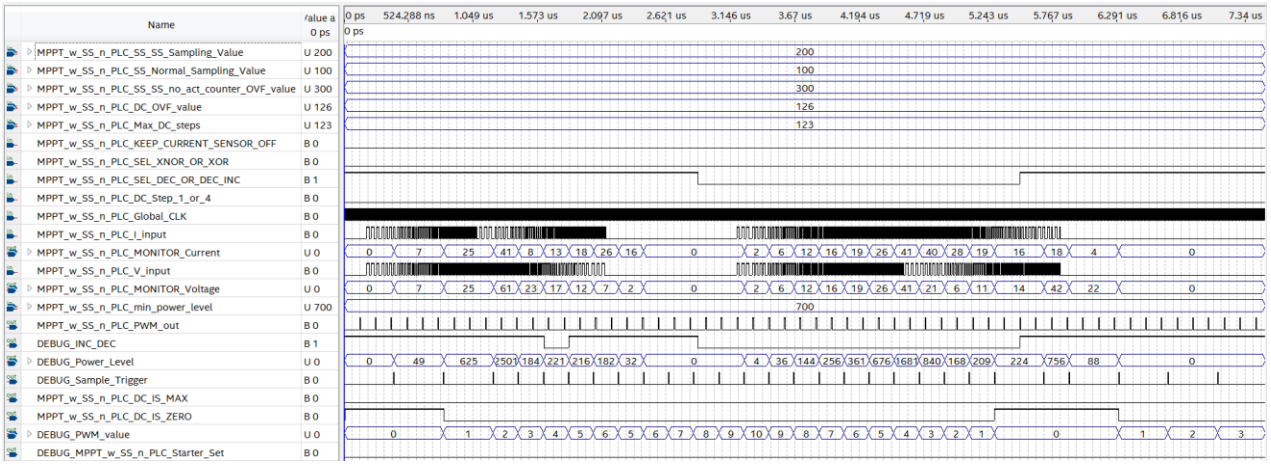


Fig. 22. Verifying the correct operation of the 'Soft Start' process.

The results of the simulation in Fig. 22 confirm the results of the previous simulation by providing a more elaborated view of the calculations regarding the PRM input signals ('MPPT_…_MONITOR_Current and 'MPPT_…_MONITOR_Voltage'), the DEBUG_PWM_value and the DEBUG_Power_Level which is compared against the 'MPPT_…_min_power_level'), that holds the P_{min} value for the proper operation of the 'Soft Start' process. The three dots of

the aforementioned labels substitute the phrase "w_SS_n_PLC", as shown in the names of all the signals of Fig. 22. The activation of the 'Soft Start' process can be identified by the wider pulses of the 'DEBUG_PWM_value' which happens either in the beginning of the simulation, since this is when the PDTRM cell is supposed to increase its current under a slow rate, or during any time that the power get lower than P_{min} after it has been higher than P_{min} and the duty cycle falls down to zero. If this happens, the system enters once again the 'Soft Start' state that forces the PWM duty cycle to increment in a slower rate. This second case can be observed after the 5.7 sec where the power was measured to be 756 (higher than P_{min}) and later falls down to 88 (lower than P_{min}) while the duty cycle is zero. The wider pulses of the 'DEBUG_PWM_value' signal from that point on, signify the activation of the 'Soft Start' process which will last for a preset amount of time. In the final version of the experimental implementation, this time was set to 8 seconds.

2.6. Experimental results

The MPPT circuit was originally developed (both analog and digital end to end sub-circuits) in Labcenter Electronics Ltd's Proteus Design Suite. Then, the digital part was developed (in VHDL code) in Quartus Prime and simulated in Intel's Modelsim, while in addition individual parts of the code have been confirmed through proper testing on Vivado Design Suite (Student edition) of Xilinx.

2.6.1. 1st experimental prototype

Next, the 1st experimental setup is presented, which was developed to certify the correct operation of the control and monitoring unit subsystems, including the MPPT, the voltage/power regulation and partially parts of the complementary control logic.

The two figures that follow, Fig. 23 and Fig. 24, present the experimental prototype in two different angles. These photos are provided in color at first, and later on, are presented in black and white (Fig. 26 and Fig. 27, respectively), including an augmented layer of colored boxes and explanatory labels so that the reader will be able to identify all the important components of the developed MPPT and power regulation system.

The same approach was applied with Fig. 25 which presents the prototype of a microcontroller-based boost DC/DC converter PCB. On the left of that figure is the original

color photo and on the right is the same photo in black and white enriched with an overlay of colored boxes and explanatory labels.

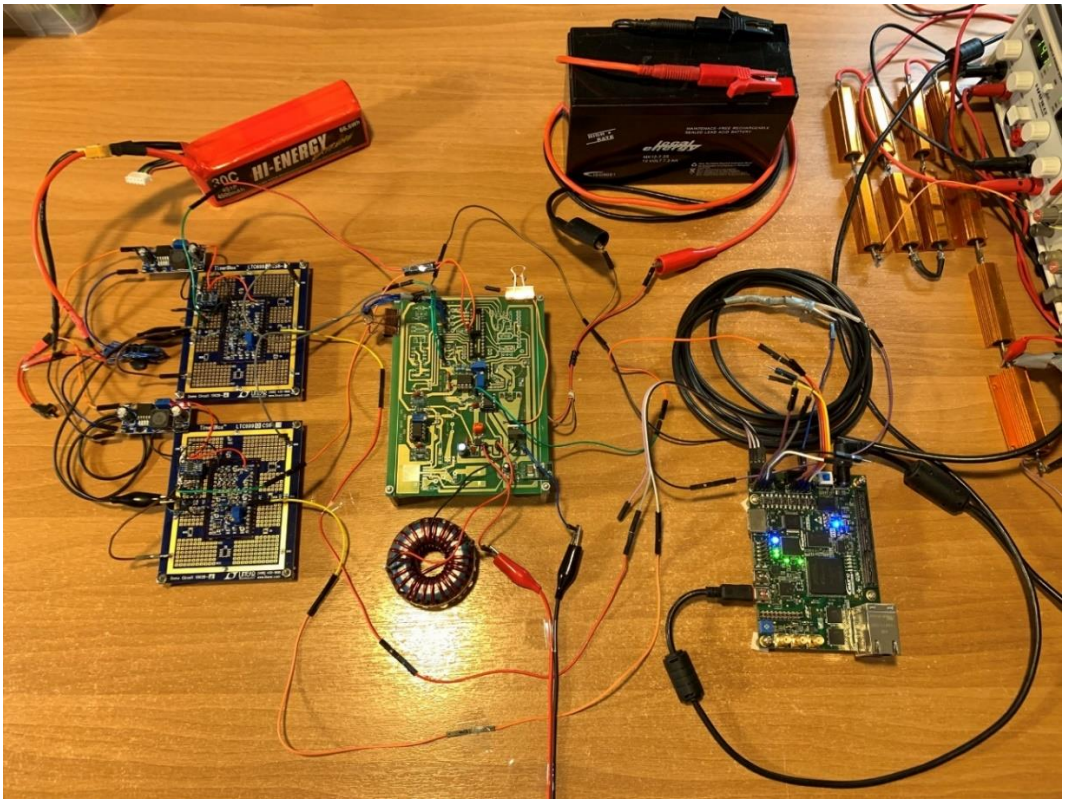


Fig. 23. The experimental prototype of the MPPT and power regulation unit (top view).

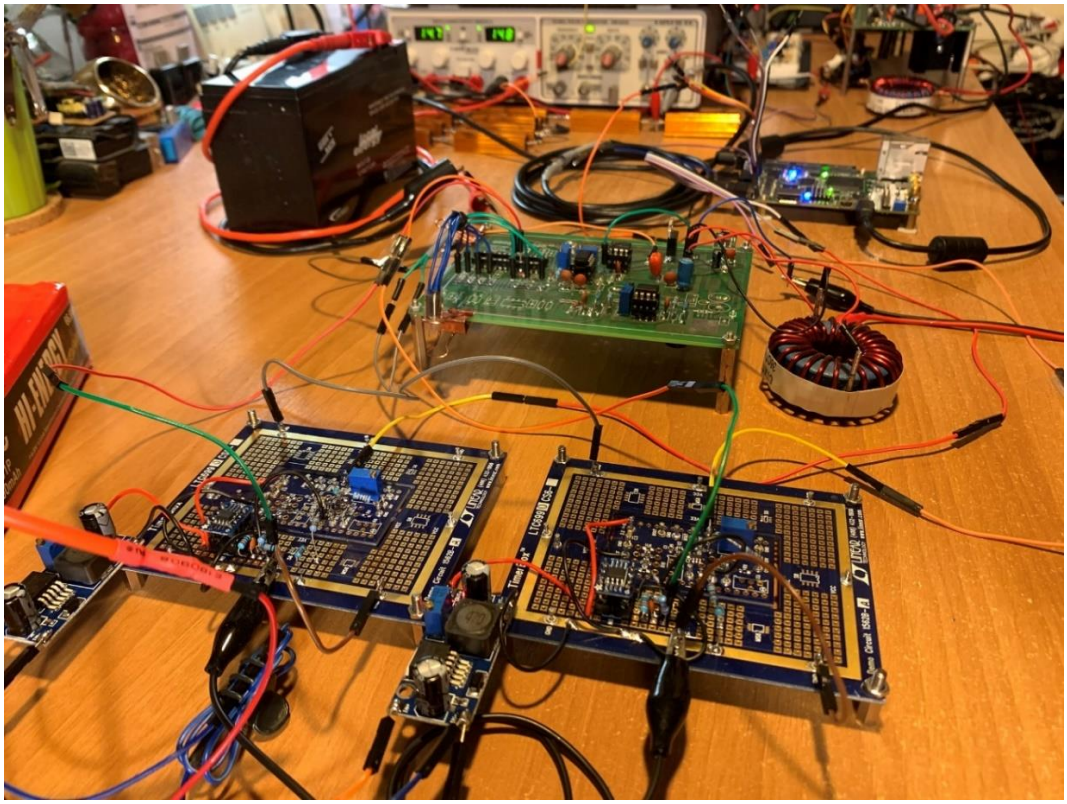
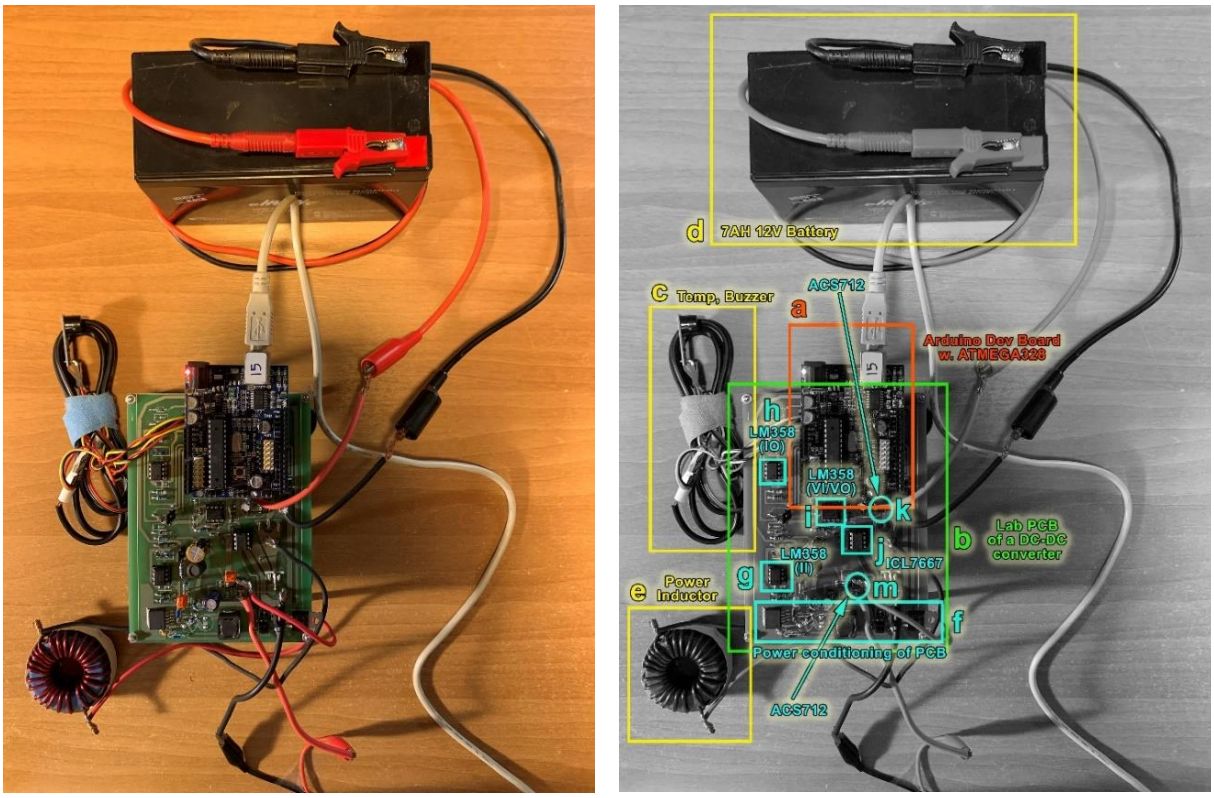


Fig. 24. The experimental prototype of the MPPT and power regulation unit (side view).

Then, Fig. 28 focuses on the Voltage Controlled Oscillators (VCOs) and the most important components of the boost DC/DC converter and the paragraph completes with Fig. 29 which highlights the main signals routing (for power and information) to further enlighten the interconnectivity and interoperability among the FPGA, the VCOs and the Boost-type DC/DC converter.

The role of the prototype PCB shown in Fig. 25 is twofold. On the one hand, this PCB includes extra components which enable its monitoring and control using a microcontroller-based interface, thus providing an off-the-shelf debugging solution in the lab that allows the characterization of the DC/DC converter properties and the PV cell to be connected. On the other hand, the DC/DC converter that can be integrated on its PCB can be used as a reference to compare and validate the experimental results of the system that will be implemented around the PCB shown in the center of Figs. 23, 24, 26 and 27.



(a) (b)

Fig. 25. The Arduino controlled Boost-type DC/DC converter.

In the right photo of Fig. 25, inside the bright orange colored box 'a' is the microcontroller development board based on the ATMEGA328 microcontroller. In this microcontroller there is code stored for the P&O MPPT control unit, as well as the system calibration and

monitoring of the DC/DC converter operation. This is used to compare and confirm the correct operation of the MPPT subsystem of the PV cell/array Control unit implemented in the FPGA array of the experimental prototype. It also includes additional logic for the various peripheral functions and control of the entire auxiliary experimental prototype via a suitable PC interface. The connection is achieved through the gray USB cable shown in the top of the picture frame (mentioning the virtual USB CDC address 15). This cable is used for programming the ATMEGA328 and to establish a connection between this PCB integrated system and a computer.

The green colored box 'b' encloses the PCB, which, apart from its 28-pin connection with the microcontroller-based development board, it carries the main power electronics, current and voltage sensors (component 'k' and 'm') as well as the analog calibration modules of input current (component 'g'), output current (element 'h'), input voltage (1st channel of component 'i') and output voltage (2nd channel of component 'i'). The power MOSFET and power diode of the DC/DC converter are not visible as they are laid on the back side of the PCB. The visible modules are the following: the integrated circuit driving the power MOSFET (component 'j'), the circuit that takes care of powering all the ICs on the board (component 'f'), and the main power inductor (component 'e'). The photo also shows a temperature sensor and a buzzer (component 'c') on the upper left frame, which are placed to alert and thus prevent the overheating of the ICL7667 power MOSFET driver (component 'j') or the overvoltage/undervoltage of the battery (component 'd'). Finally, the terminals shown at the bottom of the photo frame are the connection of the board to the PV panel which is connected to the input of the converter.

Fig. 26 shows the main modules of the 1st experimental setup. In this setup the information for: (a) the PV panel voltage, (b) the PV panel current and (c) the voltage at the output of the Boost-type DC/DC converter (DC-bus voltage), is entered as a digital pulse stream to the FPGA (component 'a') via the VCOs (components 'e' and 'f', for the input voltage and current, respectively). The frequency generator (components 's' and 'r') provides a square signal which emulates the pulse rate modulated signal produced by the sensor of the DC-bus voltage.

The DC/DC converter circuit (component 'b') is powered by the 12 V battery (component 'q') which also acts as an electric load. The battery is common in both the auxiliary (microcontroller-based) PCB board shown in Fig. 25 and this one and is charged by a PV panel

whose wiring is visible at the bottom (middle) of the image. It is apparent that the circuit of the DC/DC converter is based on the same PCB design as the one shown in the auxiliary prototype, carrying only the necessary electronics for the given application.

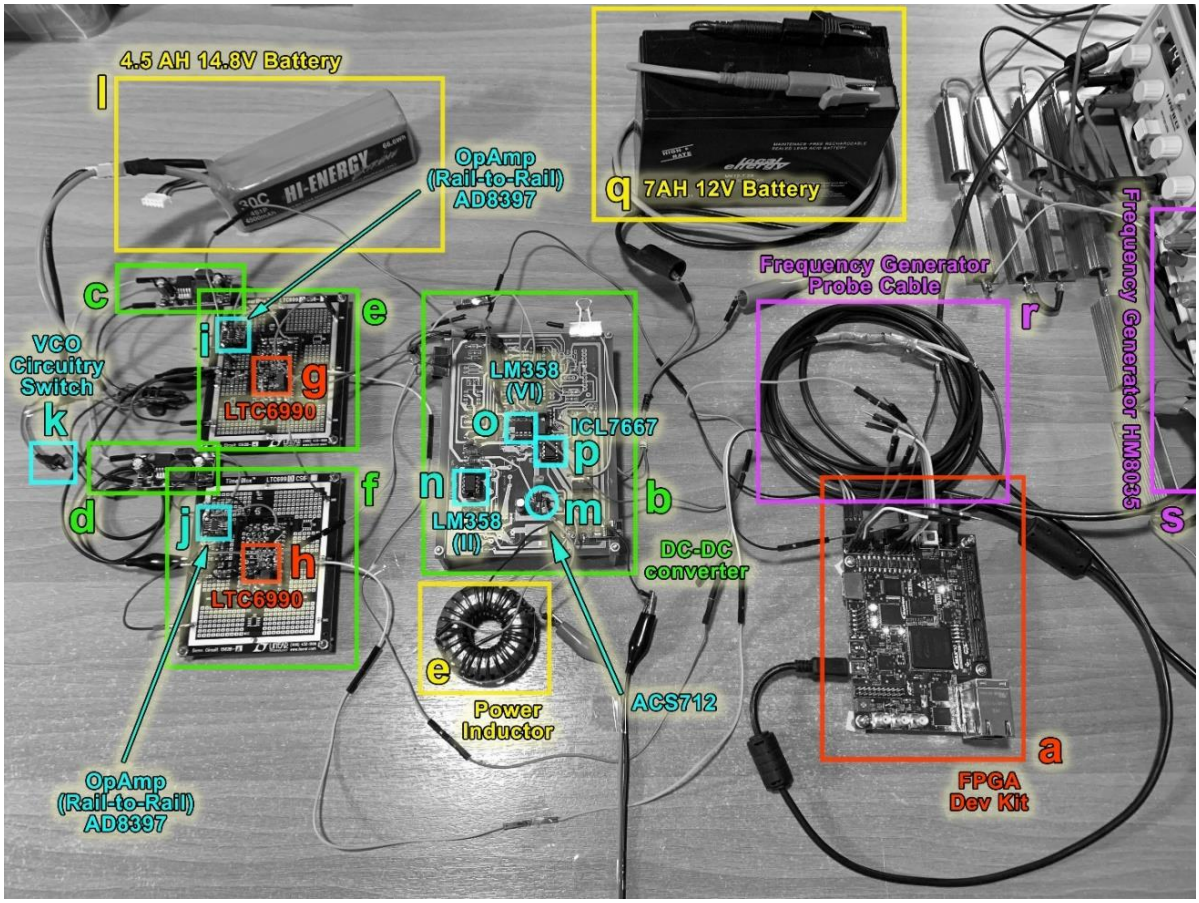


Fig. 26. Subsystems of the experimental prototype of the MPPT and Power Regulation Unit (top view).

These are the DC/DC converter input current sensor (component 'm', based on the ACS712 integrated Hall sensor), the converter input current and voltage calibration circuit (components 'n' and 'o') based on the LM358 operational amplifier, the MOSFET driver ICL7667 (component 'p'), the power inductor, the filtering capacitors and the power semiconductors located on the back of the DC/DC converter PCB.

The 14.8 V battery is responsible for powering the VCOs components 'e' and 'f', through the DC/DC buck converters (components 'c' and 'd', respectively), which supply 3.0 V to the VCOs. These VCOs simulate the operation of the output voltage and output current sensors of the PV cell. The circuit of the VCOs is switched off via the component 'k' switch. The development FPGA (component 'a') is powered through its power supply (an adapter from 230V AC to 12V DC). The HAMEG frequency generator (HM8035, component 's'), sends a positive square signal (the voltage of which alternates between 0V and 3.0V with duty cycle

50%) to one of the inputs of the FPGA device (component 'a'), through a coaxial cable (component 'r'). This signal has a suitable frequency to simulate the PRM information, i.e. to create pulses of a frequency proportional to the output voltage of the DC/DC converter (DC-Bus voltage) simulating the pulses to be produced by the corresponding sensors presented in the PDTRT system. The two Buck-type converters (components 'c' and 'd') are based on the integrated LM2596 chipset. The VCOs are based on the integrated LTC6990 chipset, around which a suitable circuit of passive and active elements has been developed (such as the rail-to-rail AD8397 amplifier, depicted in components 'i' and 'j'). These elements undertake the calibration and amplification of the generated signal (square pulses at 3.0V). The VCOs in this circuit are designed to output signals from 10 kHz to 100 kHz, which can increase linearly as the voltage to be modulated increases, from 0.4V to 4.0V, respectively. However, this range is divided into 8 – partially overlapping – regions, which means that the available bandwidth is approximately 14 kHz for each experiment. As a reference, the corresponding code in the FPGA development system is designed to handle pulses ranging from 0 kHz to 80 kHz.

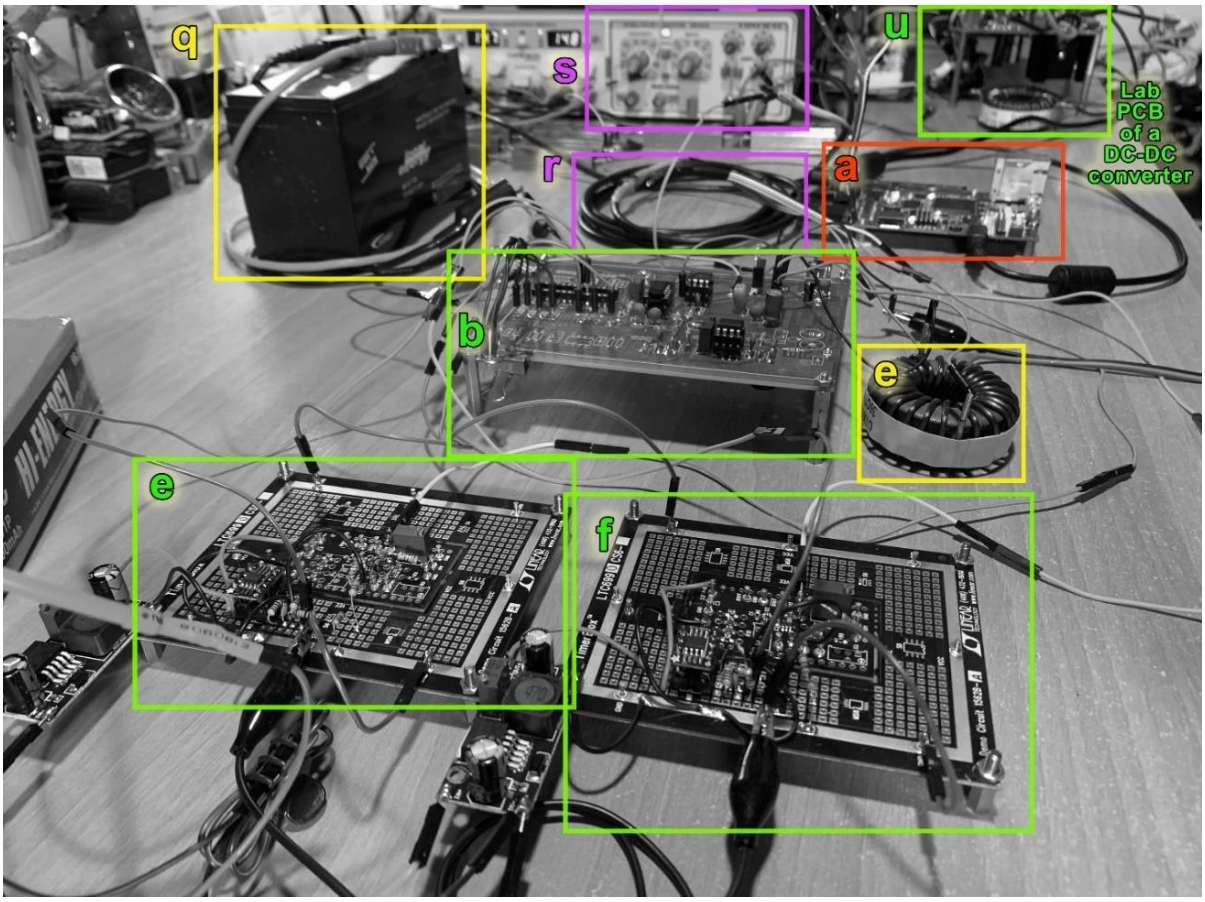
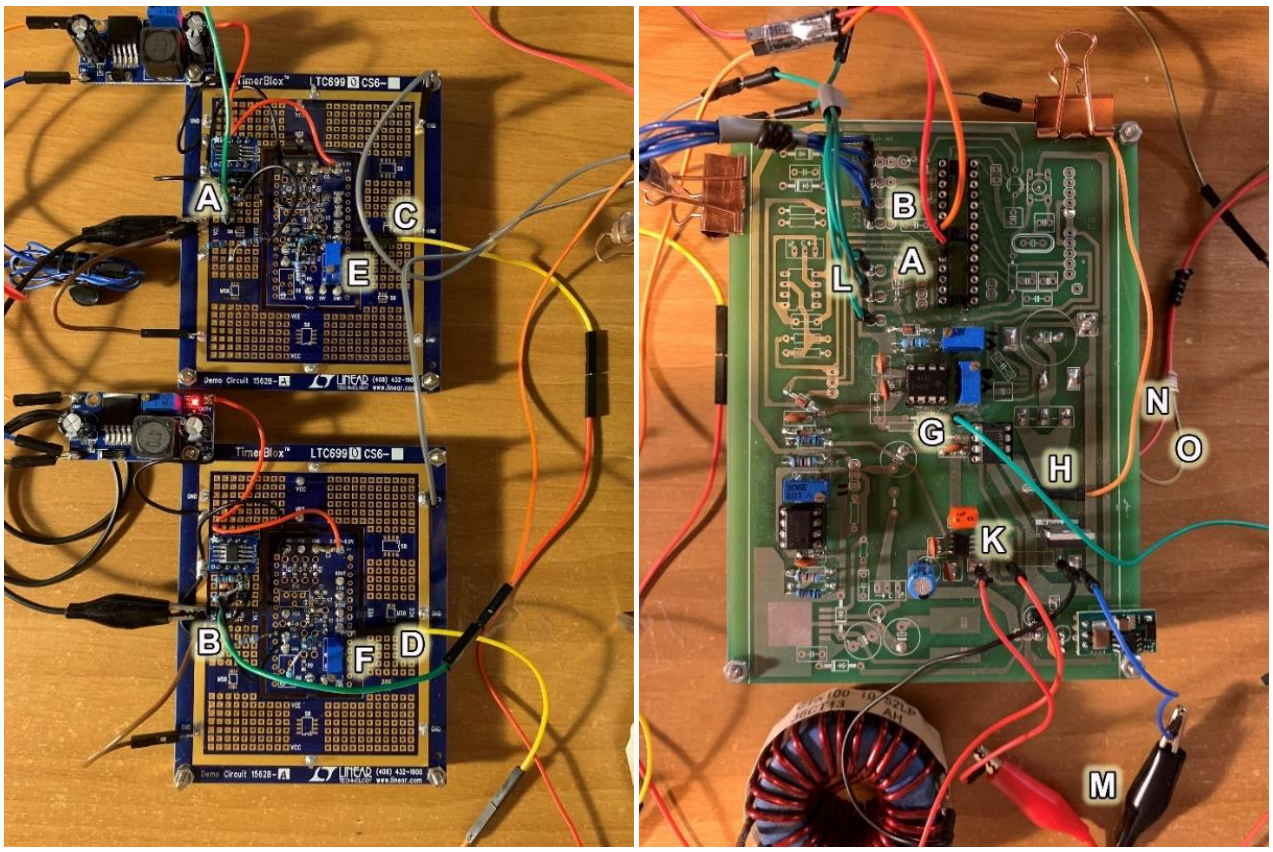


Fig. 27. Subsystems of the experimental prototype of the control and monitoring unit (side view).

In Fig. 27, the same color-coded boxes are kept for each of the sub-systems shown in Fig. 26. Here, the frequency generator is much more obvious, and the component 'u' is added framing the DC/DC converter board of the auxiliary (microcontroller-based) prototype.

Finally, on the left of Fig. 28 the TimerBlox boards are presented, in an enlarged view, showing details of the PCBs on which the VCO circuits were developed. Similarly, on the right of Fig. 28, the auxiliary boost DC/DC converter circuit in shown in an enlarged view. In the same context as before, the symbols 'A' to 'O' have been placed on a white background in these photos to facilitate useful mentions on some notable points.



(a) (b)

Fig. 28. (a): Enlargement of the VCOs PCB, (b): Enlargement of the DC/DC converter.

More specifically, in the left photo where the VCOs are visible, points 'A' and 'B' indicate the wiring of the analog input (voltage 0.4V to 4.0V), which starts from points 'A' and 'B' as indicated in the right photo, that is, from pins 24 and 23 of the 28-pin socket where the ATMEGA328 is usually placed. The wiring on points 'A' and 'B' sends to the analog inputs of the VCOs, the analog voltage and current information of the microcontroller-based DC/DC converter inputs, respectively. Points 'C' and 'D' are the respective outputs of the VCOs. The

8-range dividers – which implicitly define the operating frequency range per experiment – are programmed by the trimmers indicated on points 'E' and 'F'. The integrated chipset LTC6990 equalizes the divider to integer values 1 to 8, depending on the impedance range that the trimmer is located. The operating range of the VCO is configured in respect to the value of the trimmer divider. The two VCOs are implemented in a similar way, however each can have its own calibration depending on the value of the trimmer divider.

In the right photo, point 'G' indicates the PWM signal input that drives the integrated chipset ICL7667 (outputs an inverted logic signal), which in turn drives the power MOSFET (PSMN2R2-40PS). The wiring of point 'H' targets to debug the drive of the given MOSFET and thus it can indirectly examine the proper operation of the ICL7667 driver, as well. Point 'K' presents a clearer view of the integrated chipset ACS712 input current sensor. The input sockets, which connect the PV panel to the DC/DC converter are shown at point 'M'. The wiring at points 'O' and 'N' shows the connections to the negative and positive terminals of the 12 V battery, respectively.

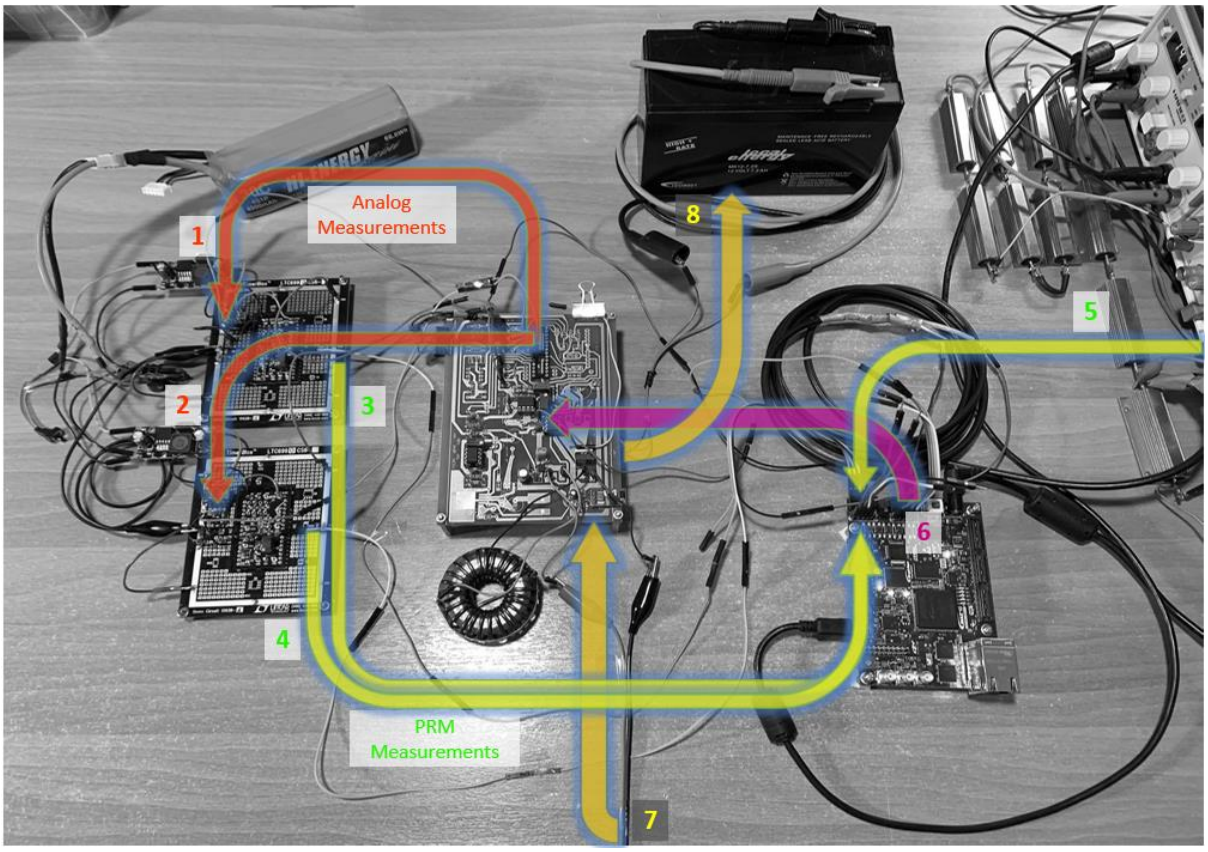


Fig. 29. Illustrating the information and power flow of the MPPT and Power Regulation Unit.

Finally, Fig. 29 shows the routing of the main control signals as well as the power channeling (using yellow arrows) from the PV panel (label 7), to the battery (label 8), according to the control applied by the DC/DC converter. The analog signals (labels 1 and 2) are highlighted in orange and the corresponding signals modulated with PRM (labels 3 and 4) are shown in green. Like the VCOs, the frequency generator produces a (user adjustable) variable frequency control and watchdog reference signal (label 5) with which it controls (like the other 2 PRM signals) the state of the PWM signal (label 6). The PWM is fed back into the DC/DC converter board, thus closing the control loop.

The experimental results that verify the successful operation of the MPPT subsystem of the 1st prototype are presented in § 3.3.2, along with the power regulation subsystem results.

2.6.2. 2nd experimental prototype

The proposed MPPT system was also manufactured using XFAB XH018 0.18m mixed-signal CMOS technology. The PV current/voltage sensors and the MPPT control unit were respectively constructed on two separate chips that were coupled during experimental validation, however this has no effect on the functioning of the MPPT system as a whole. The digital MPPT control unit was constructed using the VHDL programming language, while the final chip was synthesized using the Cadence Virtuoso digital implementation software package.

The performance of the synthesized chips including the MPPT and Power Regulation system was evaluated in the field under actual operating circumstances by synthesizing a PV array consisting of four parallel PV modules. Also, according to [46], a DC/DC converter operating with a PWM switching frequency of 31.25 kHz was constructed. Experiments were performed with the ASIC clocked at 2 MHz, although further clocking tests demonstrated that the MPPT logic was functional up to 8 MHz (the highest clocking frequency that the available function generator could provide at that time).

The experimental setup is shown in Fig. 30, and the characteristics of the PV modules under Standard Test Conditions (STC) and the DC/DC converter are reported in Table 2.1. Through a MOSFET driver IC, the PWM output of the MPPT IC drives the DC/DC converter circuit constructed from discrete electrical components.

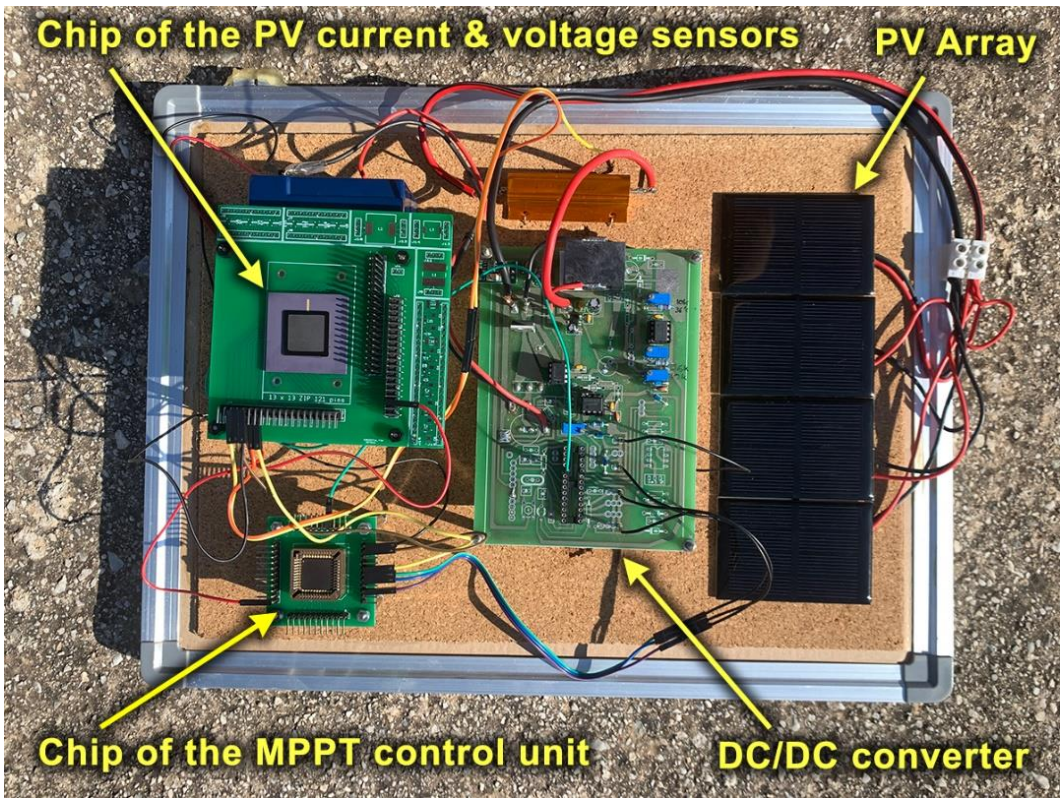


Fig. 30. The experimental setup used for evaluating the performance of the fabricated chips of the novel MPPT and Power Regulation system.

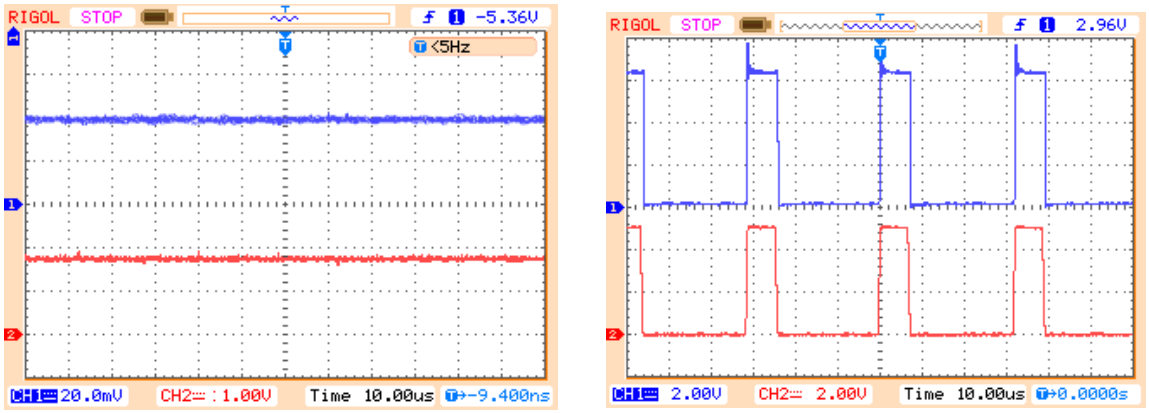
The output of the DC/DC converter is connected to a 6 V rechargeable battery, which provides power to the MPPT chip through a 2.4 V voltage regulator. Also, a shunt resistor of $R_{sh} = 0.1\ \Omega$ has been used for sensing the PV array output current, as analyzed in § 2.3.1.

Table 2.1. PV Module and DC/DC Converter Parameter values in the 2nd experimental setup.

PV Modules	
Short-circuit current under STC	**0.24 A**
Open-circuit voltage under STC	**2.4 V**
MPP power under STC	**0.4 W**
DC/DC Converter	
PWM switching frequency	**31.25 kHz**
Inductance, L	**150 μH**
Input capacitance, C_{in}	**1000 μF**
Output capacitance, C_o	**4700 μF**
Nominal output voltage, V_o	**6 V**

In order to experimentally test the operation of the fabricated chips, the values of f_s (DC/DC converter switching frequency), f_c (clock frequency), T_{S_CLK} (sampling period) and α were selected as described in § 2.3.2 and § 2.4.4. The switching frequency of the PWM control signals generated by the P&O MPPT unit has been adjusted at $f_s = 31.25$ kHz. in consideration of the DC/DC converter characteristics listed in Table 2.1. The $f_c = 2\ MHz$ clock pulses of the digital subsystems of the MPPT control unit are provided by a signal generator, which results in DR = 128 according to (12). Lastly, (10) is implemented with $\alpha = 4$ and $T_{S\_CLK} = 0.5\ sec$ to obtain appropriate performance in terms of MPPT convergence speed and accuracy for common PV applications, as described in section § 2.3.2.

Fig. 31(a) depicts the measured output voltage and current of the PV array during the operation of the digital MPPT chip when the incident solar irradiance intensity and ambient temperature are 1000 W/m^2 and 26 °C, respectively. For the specific PV operating point it holds that $V_{PV} = 1.75$ V and $I_{PV} = 800$ mA. Fig. 31(b) depicts the resultant waveforms of the pMOS transistor gate voltage generated by the PV MPPT system for PWM control in this test instance, as well as the drain source voltage of the DC/DC converter nMOS transistor (i.e. V_{ds} in Fig. 8).

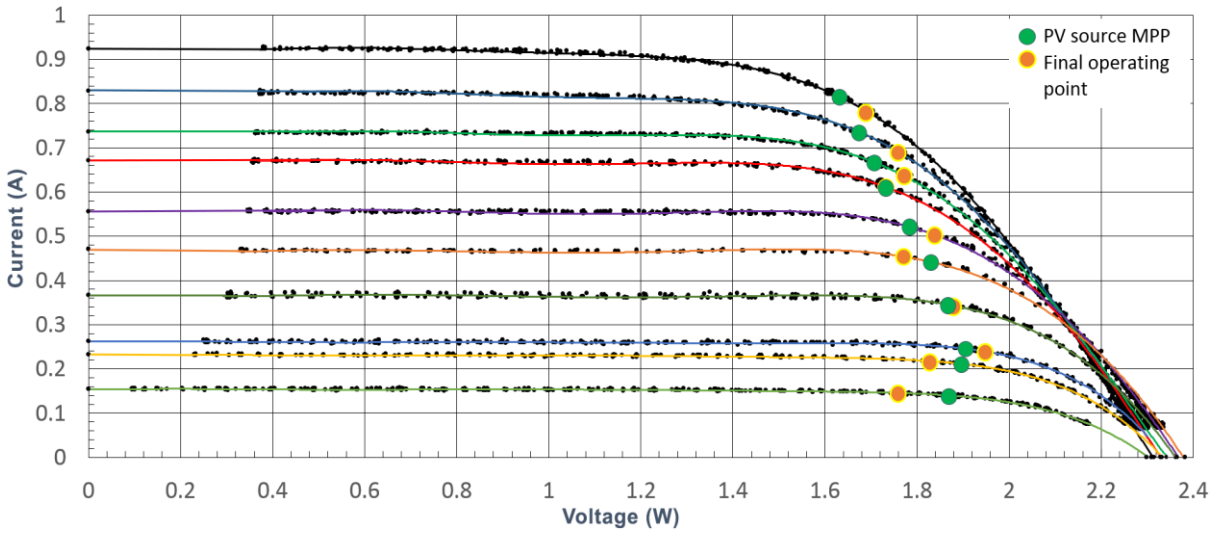


(a) (b)

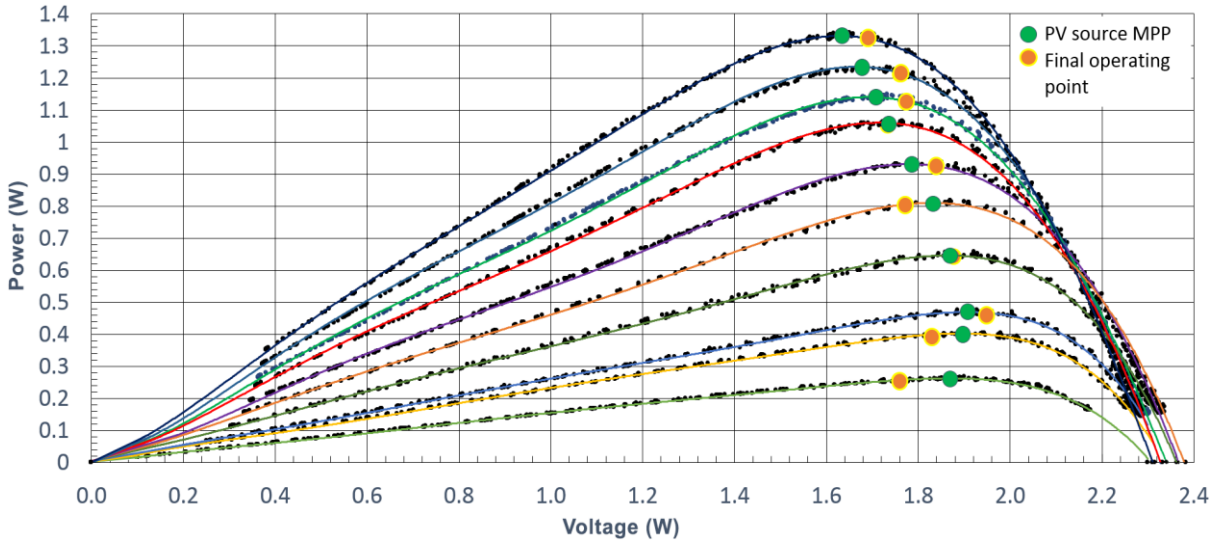
Fig. 31. Oscilloscope waveforms at 1000 W/m^2 and 26 °C of: (a) PV array output current (channel 1: 400 mA/div) and voltage (channel 2: 1V/div) and (c) DC/DC converter nMOS drain-source voltage (channel 1: 2V/div) and PWM control signal (channel 2: 2V/div).

It is observed that the PWM signal generated by the MPPT chip is able to regulate the switching behavior of the DC/DC converter as predicted for the MPPT process.

The performance of the designed MPPT system was assessed for incoming solar irradiation values between 100 and 1000 W/m^2. Fig. 32 depicts the experimentally determined current-voltage and power-voltage characteristics of the PV array.



(a)



(b)

Fig. 32. Experimental results for incident solar irradiance values in the range of 100-1000 W/m^2: (a) PV array current-voltage characteristics and (b) PV array power-voltage characteristics.

This image also depicts the matching MPP of the PV source and the final operating point following convergence of the P&O process done by the designed MPPT system. Due to the intrinsic oscillation of the operating point of the PV array around the MPP that is enforced by the P&O algorithm according to (10), the average power generated by the PV array after convergence of the MPPT system was computed for each solar irradiance value. To quantify the precision of convergence to the real MPP of the PV array, the MPPT efficiency, η_{MPP} (%), of the designed MPPT system was computed as follows:

$$\eta_{MPP} = \frac{P_{MPP,r}}{P_{MPP,a}} \cdot 100\% \tag{13}$$

where $P_{MPP,r}$ (W) is the average value of the PV-generated power after convergence of the MPPT system and $P_{MPP,a}$ (W) is the power at the actual MPP point of the PV source according to the experimental results displayed in Fig. 32.

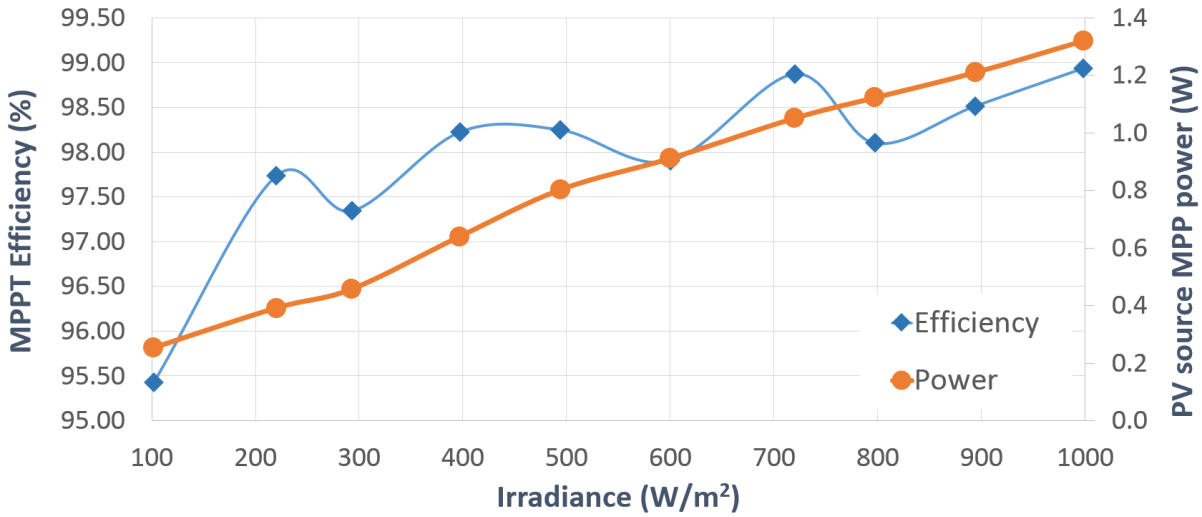


Fig. 33. The experimentally-measured MPP power of the PV array and the MPPT efficiency of the developed system for incident solar irradiance values in the range of 100-1000 W/m^2.

The values of η_{MPP} at different levels of incident solar irradiation are shown in Fig. 33, indicating that the on-chip MPPT control unit delivers a high MPPT efficiency over a broad range of solar irradiance values.

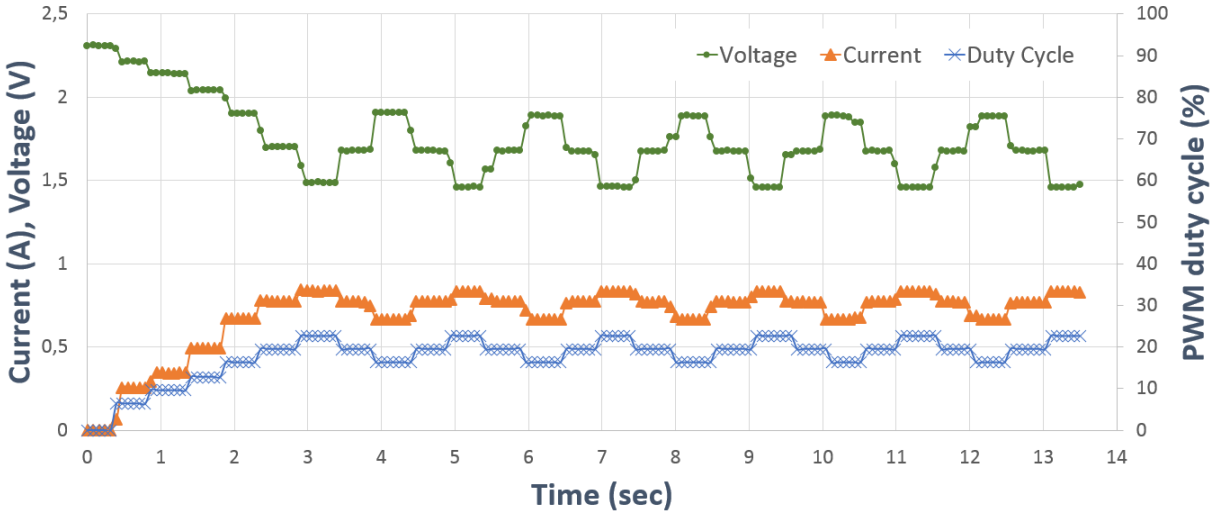


Fig. 34. Experimental waveforms of the PV source output current and voltage and the duty cycle of the DC/DC converter control signal, during operation of the developed MPPT system under transient conditions, when the incident solar irradiance is 1000 W/m^2.

The deviations from the actual MPP of the PV source are attributable to: (a) the small-scale offset and non-linearity exhibited by the PV array output voltage and current

sensing circuits on the fabricated chip; and (b) the magnitude of the duty cycle perturbation step [i.e., variable α in (10)]. Since the duty cycle calculation according to (10) is based on comparison of successive samples of $N_{P,PV}$ and $N_{V,PV}$ and not on their absolute values, as analyzed in § 2.3.2, these results demonstrate that any deviation of both the simulated and experimental values of k_V and k_I in (1) and (3) (e.g., due to the chip fabrication process) does not significantly impact the operation of the devised on-chip MPPT unit.

Fig. 34 illustrates the dynamic functioning of the proposed MPPT system, which depicts the change of the PV source output current and voltage as well as the duty cycle of the DC/DC converter control signal throughout the execution of the MPPT process when the incident solar irradiance is 1000 W/m^2 and the duty cycle value commences at 0 %. The amount of time necessary for the PV source to converge to its MPP under transient circumstances is dependent on the P&O algorithm's iteration period [i.e. parameter T_{S_CLK} in (7) and (8)], which must be longer than the reaction time of the DC/DC converter.

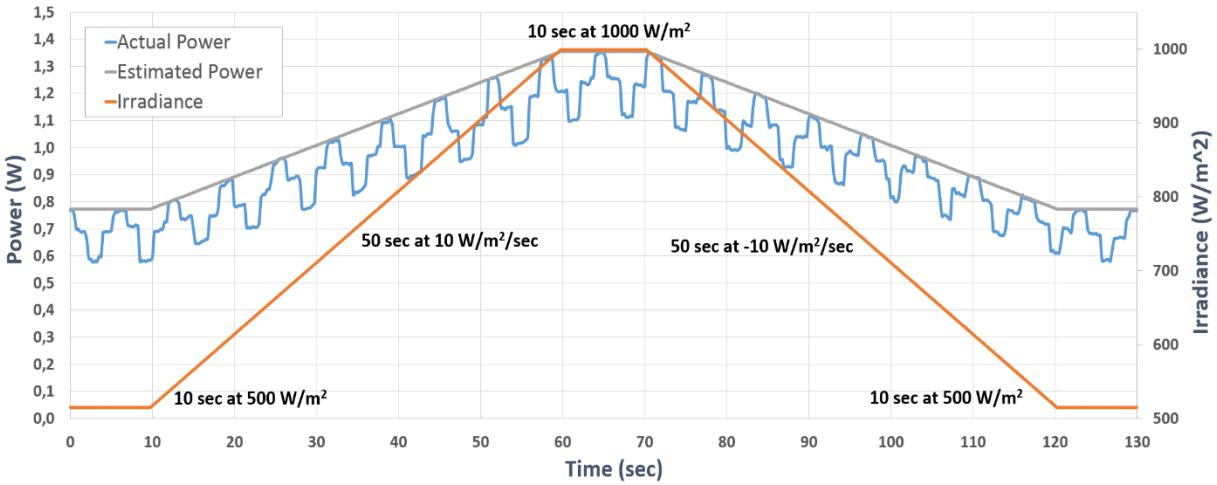


Fig. 35. The experimentally measured power produced by the DC input source during dynamic operation of the MPPT chip when the incident solar irradiance follows a sequential ramp.

Moreover, the dynamic operation of the manufactured MPPT chips was experimentally assessed by applying ramps of irradiance fluctuation, as studied in [49] in accordance with the EN 50530 standard. The incident solar irradiance was adjusted to follow a sequential ramp between 500 W/m^2 and 1000 W/m^2 at a rate of ±10 W/m^2/sec and a pause of 10 sec on each irradiance level, as seen in Fig. 35. This figure depicts the power generated by the PV array during operation of the MPPT chip under similar circumstances. Observations indicate that the MPPT system on-chip effectively tracks the variations in incoming solar irradiance that occur in typical PV systems and that its performance is unaffected by the internal digital

circuits' time delay. In addition, the power generated at each operating point conforms to the data shown in Figs. 32 and 34. According to (10), the observed power oscillations are an intrinsic property of the P&O MPPT algorithm.

Compared to the integrated MPPT system previously published in [44], the experimental findings reveal that the developed MPPT control unit performs satisfactorily using just digital units, without the need for analog circuitry. In addition, it is able to operate in conjunction with PV current and voltage sensors with a pulse-frequency modulated output that are connected externally to the chip of the MPPT control unit presented in this PhD thesis in order to meet the requirements of any PV energy harvesting system (e.g. in high-power PV systems).

3. Energy management system for PV cells

3.1. Introduction

The main goals of an energy management are the following: (a) to increase the electric efficiency of a system (by maximizing the energy that is being supplied to the load while minimizing the energy losses), (b) to minimize the cost of the total system (design, development and maintenance), (c) to regulate the balance of supply and demand, (d) to enhance robustness and fail tolerance and (e) to increase the time service of uninterruptible power supply, while providing additional services to the electric grid.

The PV Energy Management Systems (EMS), when connected to an electric storage device, are of vital importance as they can provide the lack of power either to the load and/or to the electric grid when the power supplied by the PV source (e.g. during the night, or due to a shading incident by clouds, or an unexpected power failure due to some fault) is not adequate to cover the respective needs. This way the EMS can protect the power supplied appliances by regulating the voltage level and the power flow fixed. Also, some EMSs that are connected to the electric grid can contribute to stabilize the frequency and the local voltage of the electrical network around them, given that they can provide the necessary power (either directly from the PVs or through the EMS storage device).

Thus, in case of PV systems, an EMS is responsible for the efficient and effective utilization of photovoltaic energy by monitoring and coordinating the proper interoperability of its four main processes which are: energy generation, energy storage, energy distribution and energy consumption (regardless of the variation in sources and/or in loads). At the same time, it needs to optimize the energy utilization of the PV cells (as it has already been established) and to monitor and control the system's response to avoid faults and to schedule its availability according to the consumer requirements and electricity prices.

Most of the EMSs found in today's commercial PV array systems are capable of conditioning their electricity storage units (usually a battery bank, supercapacitors and/or a fuel-cell stack), in order to maximize their life cycle and render them prepared and deployable for any power surges or extreme occurrences during the peak electricity demand

hours. The modern EMSs can also communicate with the user/operator by sending useful data about their state and the state of the power system, which are also called telemetry data. According to a study conducted by the authors of [50] the evolution of the smart grid has boosted the need for applications that will support bidirectional communication to facilitate the fine-grained metering, feedback and control of the involved systems in order to increase their manageability. Since such infrastructures are still quite new and immature, the authors of [50] identified a wide heterogeneity among the features of the available systems found in literature.

The summary of the respective results presented in their review, can be found in Fig. 36.

Evaluation criteria	Monitoring	Dis-aggregation	Availability and accessibility	Information intergration	Affordability	Control	Security & privacy	Intelligence
PERSON (Yang and Li, 2010)	Yes	Yes	Monitor and Control center available at user premises; no web or mobile interface	Aggregates usage information; Integrates temperature, humidity, luminance, and motion data	Low power and low cost consumption	Manual remote control of the switches and dimmers	No	Context-aware intelligent algorithm
WattDepot (Brewer and Johnson, 2010)	Yes	Possible to implement, separate sensors present	Web-based interface	Automatic interpolation	Freely available - Open Source	No	Limited Privacy model	No
ViridiScope (Kim et al., 2009)	Yes	Yes	Not discussed	Aggregates magnetic, acoustic, and light data	Indirect sensing requirement; no inline installation needed	No	No	No
Mobile feed-back (Weiss, et al., 2009)	Yes	Yes	Interactive; readily available feedback on smartphone	Integrates historical data	High availability through smartphone app.	No	No	No
DEHEMS (Sun-dramoorthy, et al., 2011)	Yes	Yes	Web-based user interface, real-time display unit	Integrated sensed information, electric supply and gas supply lines data	Sensing Requirement	No	No	(Not yet) Planned for 3rd phase
EnergyWiz (Petkov, et al., 2011)	Yes	No	Smartphone app.	Integrates historical usage, and user info from peers; social network friends, and EnergyWiz users	Requires smartphone app.	No	No	No
NOBEL (Karnouskos, 2011)	Yes	Yes	Smartphone app.	No	Requires smartphone app.	No	Yes	Limited (user behavior nalytics)
ALIS (Bartram, et al., 2010)	Yes	Yes	Web, Smartphone, Touch panel, art display	Integrates historical use, community usage data	Requires extensive installation - more costly	Yes	No	No

Fig. 36. Various EMS evaluation based on their main features according to [50].

The authors conclude their study by pointing out that the future EMSs will have to carefully address the privacy and security issues since they are still being handled quite poorly. They also add that the future EMS will need to offer some intelligence based on analytics and learning algorithms that will be able to provide insights into the consumer behavior and to automatically suggest plans of efficient operation to the electric grid subsystems (resources and loads).

Towards this call, the work of this PhD thesis enhances the interconnection and interoperability of the smart grid nodes by utilizing the available electric cabling, establishing PLC connections, which are – in principle – more robust, private and secure than the wireless ones. The protocol of the telemetry data that are broadcasted by the distributed PV cells or arrays is designed so that it can allow for embedding any data encryption required by the target application. Also, its breakdown structure can support the intelligent meta-processing of data in the server application of the remote user terminal (RMCU in Fig. 37). The status of the EMS of the designed system has very high granularity, as it can report for the state of every connected PV array down to the level of a single PV cell, if required.

3.2. The energy management system (EMS) design

As a reference, Fig. 37 highlights the position of the system to be described in this chapter, focusing on the subsystems that are closely related to the EMS design.

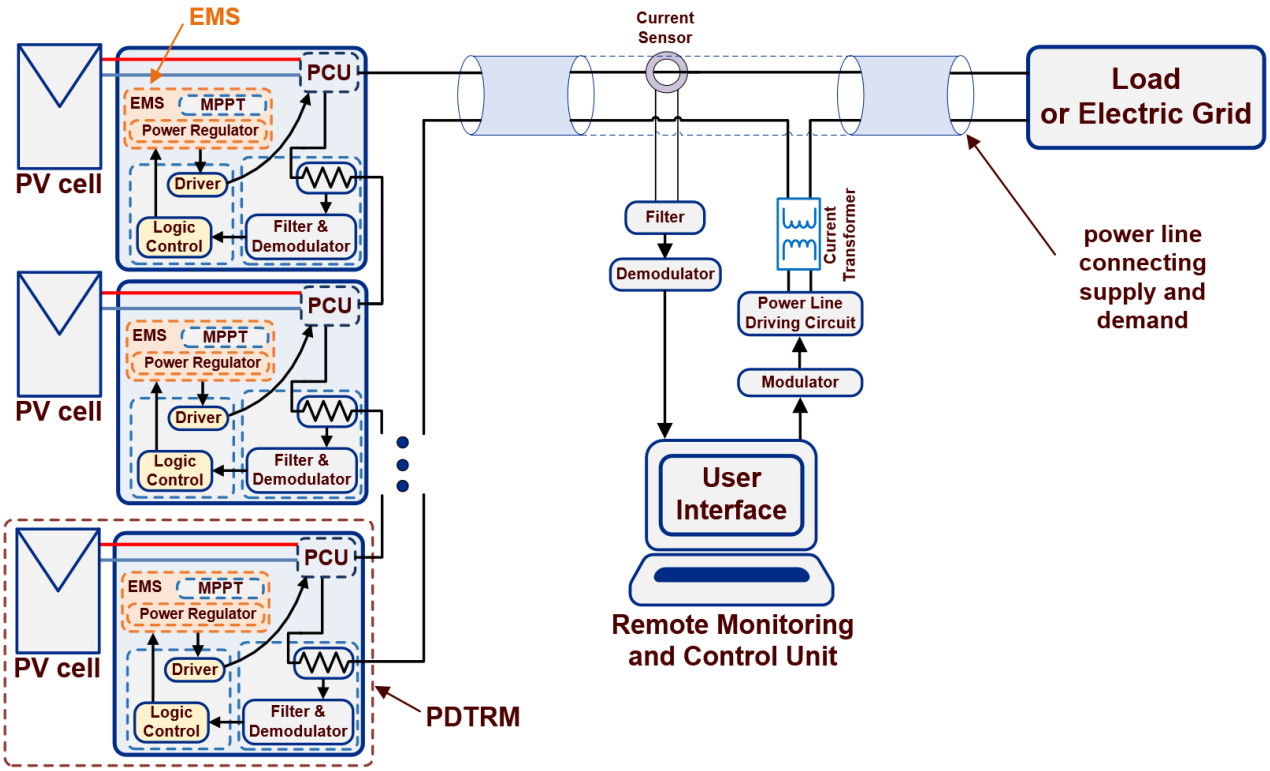


Fig. 37. The general diagram of the PV system investigated in this PhD thesis expanded in order to present the Energy Management System.

3.2.1. Power management features and subsystems

The energy management subsystem for controlling the generated power and adapting it to the (time-varying) load requirements was developed in conjunction with the power switch PWM control signal generation subsystem of the power converter. The power management subsystem rearranges the power converter to act as a DC/DC converter when a DC output voltage should be produced and as a DC/AC converter when an AC output voltage is to be supplied to the load. The DC/AC converter is based on a full-bridge of power switches which follow the taxonomy displayed in Fig. 3. In order to control the power produced by the PV cell and adapt it to the (time-varying) power requirements of the load supplied by the PV system or to a specific value pre-set by the user so as to support and the corresponding function often required by modern smart grids, the power management subsystem operates as follows:

- until a correct parameterization is obtained from the user-interface, the DC/AC bridge of the power converter is disabled (the upper 2 power switches of the full-bridge are turned ON and the lower two power switches of the full-bridge are turned OFF),
- to produce a DC output voltage the power converter is rearranged by the control signals so that one upper power switch of the DC/AC bridge turns ON and the diagonal power switch turns ON, so overall it operates as a DC/DC converter and: (a) if the DC/DC converter operates for maximum power production, then the MPPT process is executed until its output voltage reaches V_{DC_max}.Then, the DC/DC converter is turned off until its output voltage drops to V_{DC_reg} at which point it resumes MPPT operation, (b) if the DC/DC converter operates to produce a predetermined output voltage (based on the parameterization received from the user-interface via the Downlink subsystem), then the duty cycle of the DC/DC converter is controlled according to the P&O algorithm so that the output voltage of the DC/DC converter is constant at the pre-set value.
- in the case of stand-alone operation of the PV array and with AC output voltage generation, the MPPT function is not performed. In this case, the duty cycle of the DC/DC stage is controlled according to the P&O algorithm so that its output voltage is constant at a value of V_{DC_reg} and the control of the DC/AC bridge is activated for stand-alone operation (described below).
- in the case of interconnected operation of the PDTRM Arrays: (a) without setting the output power of the PV cells to a predetermined value: the MPPT function is performed

and the full-bridge control is activated for interconnected operation (described below) and (b) with setting the output power of the PV cells to a predetermined value: instead of MPPT for power maximization, a P&O algorithm is performed to set the output power of the PV cell to the desired value preset by the user (from the user-interface) through the Downlink subsystem.

3.2.2. Monitoring and protection subsystems

It is important to note that in order to implement the PV cell operation monitoring subsystem (Fig. 37), the Uplink transmitter is used to send the measurements of the voltage and current produced by the PV cell to the RMCU (the remote user-interface). These measurements are then stored in a database and subject to processing for the purpose of e.g. detecting and locating faults in the PV cells, implementation of energy management schemes in smart grids or microgrids etc.

Also, for the implementation of the protection subsystem of the PV cell, when a configuration command instructing for the PV cell disabling is received (e.g. during installation or maintenance, or for anti-theft protection), then the power converter is also disabled and the DC/AC bridge switches are toggled so that the 2 upper power switches of the full-bridge are in the ON state (activated) and the two lower power switches of the full-bridge are in the OFF state (deactivated).

3.2.3. Power supply subsystem

The power supply subsystem of the PV cell control unit is enriched at the system level with the following features:

a) four MOSFETs which are connected in a full-bridge topology, each one being controlled independently of the rest, to either pass the DC voltage as is to its output or to alternate it in order to create a pseudo sinusoidal AC component,
b) an optional circuit which includes a dead time option in the driving of the aforementioned full-bridge to avoid cross-conduction currents,
c) a cold-start circuit to progressively charge the output capacitor of the DC/DC converter to a voltage of V_{DC_cs} at the start-up operation of the PV cell,
d) the power supply stabilization circuit for the analog and digital circuits of the control and monitoring unit (LDO) which provides a constant voltage equal to V_{DC_LDO} to these

circuits regardless of the voltage fluctuations of the DC-DC converter output capacitor and

e) a DC Bus sensor and a 'Soft Start' digital logic that protects the PV cell circuitry from over currents, as explained in § 2.4.2.

3.2.4. Additional functionality-check inputs in the EMS module

In the EMS subsystem there are three different 1-bit inputs which are used for parameterization and debugging by appropriately changing the behavior of the given subsystem to adjust its mode of operation, to verify its design and operation and to facilitate towards any correcting action that may need to be applied, especially in the case that the control unit of the PV cell will be fabricated in an integrated circuit.

The first of these inputs is called 'SEL_XNOR_OR_XOR' and aims to change the calculated direction of the PWM output signal duty cycle changes. This is useful for checking the correct operation of the EMS subsystem's internal digital circuits that perform the P&O algorithm as described in § 2.3.2.

The second of these inputs is called 'SEL_DEC_OR_DEC_INC' and aims to ignore the duty cycle calculation direction and to set it (as long as the input is 0) to a fixed decreasing state. This is aimed to identify potential problems that are also related to the MPPT algorithm implementation circuits in the control and monitoring unit. It also serves to shift the duty cycle towards a known (and desired) value during the performance evaluation and the experimental tests to re-adjust proper operation. Also, it enables the linear scanning of the entire duty cycle value range to investigate the response of the MPPT and power regulation subsystem.

Finally, the third of the inputs is called 'SEL_DC_Step_1_or_4' and aims to define two different duty cycle stepping modes, as the optimal stepping is defined by quantities that are not precisely known during the design of the control unit and mostly depend on the target application. For example, it depends on the sampling frequency of the MPPT algorithm, its averaging time-window, which are both indirectly dependent on the switching frequency of the power converter and its response speed.

Also, it is dependent on the total noise entering the MPPT P&O algorithm calculations (e.g. through the sensors output signals), as well as the stability and speed of the MPPT algorithm's response to possible sudden external changes in the voltage and current

produced by the PV cell. The fine stepping can provide more accuracy in the duty cycle scan and less deviation from the optimal operating point of the PV cell, while the large stepping can avoid miscalculations in the feedback loop of the P&O algorithm, as it makes distinct the outputs routed from the corrective actions of the automation itself against random effects caused by noise. These issues in turn, may affect the power regulation response, its steady-state error level, etc. The presence of these three signals increases the controllability of the given system through the at-will transition (or absence of transition) to the corresponding states, at distinctively set user-selected time intervals, to serve for functionality checks and fault diagnosis of the related PDTRM subsystems.

3.3. Experimental results

3.3.1. Experimental results of the operating state adjustment unit (FSM control)

The experimental tests that follow, examine the logic that was developed as an enriched Finite State Machine (FSM), verifying the correct interpretation of the Downlink commands then the proper transition from one state to another. Fig. 38 depicts a snapshot of the 8-bit logic analyzer that examines whether the embedded transmitter's predefined commands are received correctly by the Downlink receiver (i.e., if they are read and demodulated correctly) and whether the FSM logic interprets each one of them appropriately, adopting the state that leads to the anticipated system parameterization.

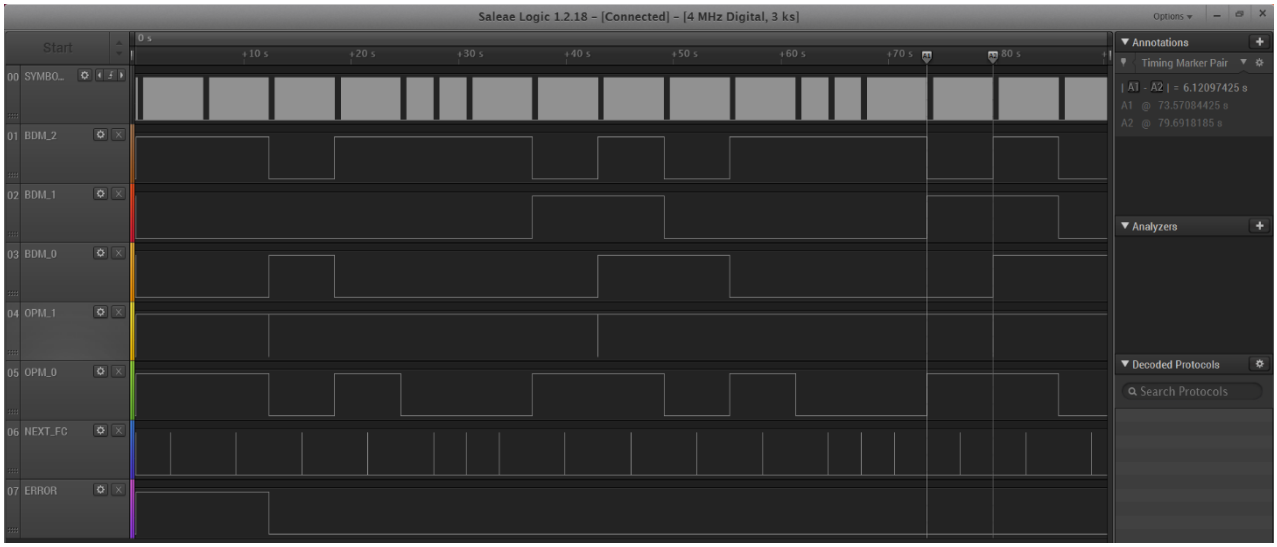


Fig. 38. Checking the FSM state transitions by observing the 3-bit full-Bridge Driving Mode, the 2-bit DC/DC Op Mode, the Synchronization Command and the ERROR detection flag.

The FSM state is defined as the value of the 7-bit vector, which consists of:

a) the value of the multiplexer [the 3-bit full-Bridge Driving Mode (BDM) assigned to channels 01,02,03 in the logic probe] for characterizing the state of the terminal full-bridge (where the ID of the parameterization refers to the ID of the first of the two full-bridges of the experiment),
b) the value of the multiplexer [2-bit DC/DC Operational Mode (OPM) assigned to channels 04 and 05 in the logic probe] that defines the driving mode of the DC/DC converter,
c) the bit that captures the successful recognition of a synchronization command (channel 06 in the logic probe) and finally,
d) the bit (channel 07 in the logic probe) that captures the ERROR that prevents the FSM from applying the indicated change.

In order to verify the proper operation of the FSM from end to end, a Downlink Transmitter module was implemented and placed inside the rest of the FPGA logic providing an extra output ('SYMBOLS_OUT') that broadcasts data as long as the FPGA circuit is considered to be powered on. This stream of square symbols, when connected to the Downlink Receiver input ('SYMBOLS_IN'), can excite the receiving logic, trigger the carrier locking mechanisms and successfully demodulate the signal. This demodulated signal is then interpreted to special commands that are sent to the FSM control circuit.

So, the first of the 8-bit signals (channel 00 in the logic probe) captures the bits of the 'SYMBOLS_OUT' output which is then routed to the 'SYMBOLS_IN' input of the FPGA. In total, the given experiment examines the automatic transition from one command to another, with the transmitter sending a total of 6 commands serially, which it then loops infinitely.

Although the following chapters will look into this in detail, it is good to note at this point that each of the first 5 commands consists of 10+10+31 = 51 bits (called synchronization commands) which prepare the receiver for locking and reading the command to follow. This command is comprised of 30 data bits followed by 21 Cyclic Redundancy Check (CRC) bits that verify the correct reception of all 30+21=51 bits of the functional command. The sixth command consists of 10+10+31 = 51 bits for a special syncing command called 'WAKE_UP_1K' and 30+21 = 51 bits of one last functional command. The synchronization commands contain

a small gap (a channel mute) at their beginning, which makes them easy to distinguish in Fig. 38. The ERROR (detected) signal is kept high until it recognizes the second functional command, while it does not become high again as it does not detect some error in transmission.

The indicators A1 and A2 in Fig. 38 allow the measurement of the time interval occupied by the transmission of a synchronization and a functional command. As it will be explained further in Chapter 5, this interval is equal to 51+51 x 60 msec = 6.12 sec as the transmission for these commands is undertaken by the built-in transmitter which, in the given experiment, is programmed to send the useful bits at the specific rate.

3.3.2. Experimental results of the MPPT module and voltage/power regulation

This paragraph presents the experiments that certify the correct operation of the subsystem that configures the MPPT algorithm, adjusts the output voltage of the DC/DC converter and regulates the output power of the PV source (cell, module or array). The experimental setup that has produces the results to follow has been presented in detail in § 2.6.1. The EMS system is capable of adjusting its operation depending on the parameterization of the control unit, as it is being simulated to be obtained from the user-interface via the downlink subsystem which is analyzed in Chapter 6.

In order to confirm the results, an auxiliary experimental prototype was initially used to connect to the computer so that the corresponding P-V and I-V characteristics of the connected PV panel with the given weather conditions are produced in the corresponding user-interface (RMCU). These characteristics then provided a reference for the results obtained by the MPPT process from the second, identical experimental prototype, which was connected to the same PV panel immediately afterwards, but was controlled by the FPGA-based unit.

The respective voltage design parameters were set to:

V_{DC_min} = 2.0 V, V_{DC_LDO} = 2.3 V, V_{DC_reg} = 2.5 V, V_{DC_cs} = 2.6 V, and V_{DC_max} = 3.0 V.

Fig. 39 shows the PV panel used (type PS-20W), with short-circuit current I_{sc} = 6.13 A, open-circuit voltage V_{oc} = 9 V, voltage at the maximum power point V_{mp} = 6 V and current at the maximum power point I_{mp} = 3.33 A. The operating voltage of the PV panel is higher than that of a single PV cell that is intended to be integrated into the PDTRM.

Fig. 39. The PV panel used in the EMS experimental verification process.

To confirm the operating principle of voltage regulation, the behavior of the duty cycle was examined for the case that the DC-bus voltage is different (sometimes higher and sometimes lower) than a predetermined value. The voltage value in the given experiment was chosen to be 2.6 V, which corresponds to the frequency of 13.5 kHz, leaving the measurements of the output voltage of the DC/DC converter in case of implementation within an integrated circuit to be carried out with a V2F sensor as designed in § 2.3.1.

Fig. 40 presents 4 snapshots, and two scenarios. The two on the top concern one scenario and the two on the bottom concern another one. The snapshots on the left are taken when the DC-bus voltage is slightly below the pre-programmed value and the snapshots on the right are taken when the DC-bus voltage is slightly above the pre-programmed value. The screenshots on top show on channel 2 the frequency and the duty cycle of the DC/DC converter (blue color) and on channel 1 the debug signal indicating the circuit selection for decrement/increment (yellow color). The screenshots on the bottom present the second scenario, where channel 2 (blue color) shows the frequency and the duty cycle of the DC/DC converter and channel 1 (yellow color) the respective frequency of the DC Bus voltage, i.e. the output voltage of the DC-DC converter. Finally, the frequency counters on the top snapshots show the frequency of the PWM signal while on bottom snapshots the frequencies of the DC Bus voltage PRM sensor which seem to be slightly lower (left snapshot) and slightly higher (right snapshot) than 13.5 kHz.

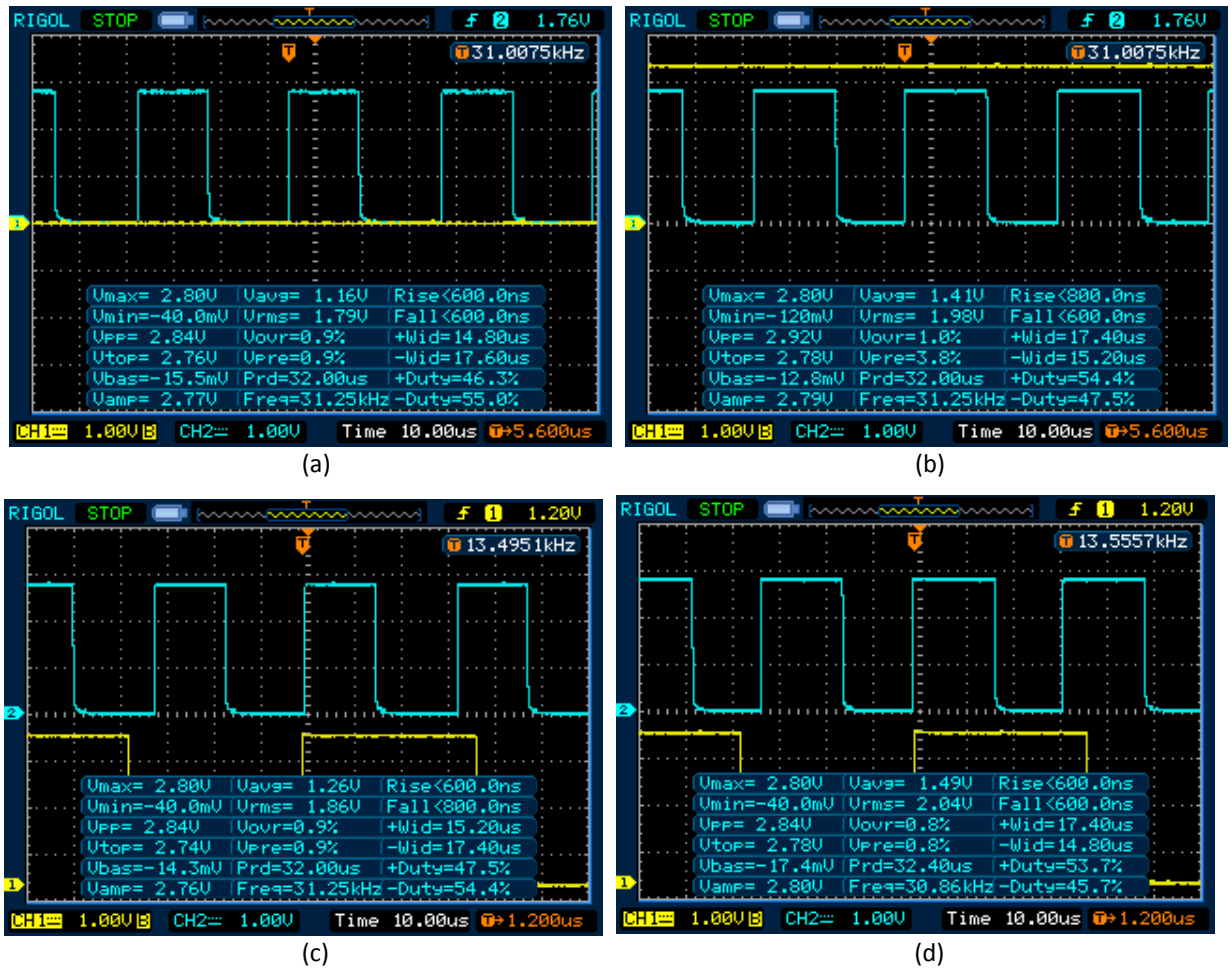


Fig. 40. The behavior of the duty cycle is shown for two scenarios (1st on top and 2nd on bottom snapshots) where the DC-bus voltage is lower (a),(c) than desired and higher (b),(d) than desired, respectively.

More specifically, the experiments start in both cases with the duty cycle set to 50 %. As it can be observed, for a frequency of 13.49 kHz, the duty cycle continuously decreases (in the snapshot for the given scenario it is 50 – 4 = 46 %) while for a frequency of 13.55 kHz, the duty cycle continuously increases (in the snapshot for the given scenario it is 50 + 4 = 54 %). The fluctuation direction changes after the ICL7667 driver used as it is inverting. The given behavior certifies that when the circuit is operated with a VCO and the control loop is closed, the system will adjust the voltage around the desired point on a case-by-case basis.

To confirm the correct functionality of the power regulation unit of the EMS system, the circuit of the 2nd experimental prototype – accompanied by a suitable power supply – was used, proving that the circuit stabilizes its current flow, properly, for various input voltages, and for two different preset power options.

In Fig. 41, the current values are presented sequentially, for input voltage values (from left to right) for 1.5 V, 1.7 V and 2.3 V. The programmed power value was 1.5 W. As can be seen

the duty cycle in each case is placed around the area that forms the appropriate current value, so that in each case the resulting power oscillates around 1.5 W. Likewise, in Fig. 42, the current values are presented successively, for input voltage values (from left to the right) for 2.3 V, 2.6 V and 3.0 V. The programmed power value was 2.0 W. As it can be seen from the snapshots, in each case, the duty cycle is placed around the region that translates to the appropriate current value, which will in turn result to power oscillations around 2.0 W.

Fig. 41. Scenario where various operating points were examined for 1.5 W preset.

Fig. 42. Scenario where various operating points were considered for 2.0 W preset.

To illustrate the correct operation of the DC-bus overvoltage protection circuit (i.e., voltage greater than 3.0 V) the channels 1 to 4 of the logic analyzer represent the following:

- the frequency generator output ('GEN_FR') which simulates the PRM sensor of the PV source, which produces a square frequency wave proportional to the DC-bus voltage,
- the PWM output of the DC/DC converter,
- a debug signal ('HT_3V') which goes high when the system detects a frequency from 'GEN_FR' corresponding to a voltage greater than V_{DC_max} = 3.0V,

- and a debug signal ('LT_2V5') which goes high when the system detects a frequency from 'GEN_FR' corresponding to a voltage lower than V_{DC_reg} = 2.5V.

As shown in Fig. 43, the PWM signal is interrupted for some time. The interrupt occurs when 'HT_3V' goes high, i.e. when the system senses that the DC-bus voltage is higher than V_{DC_max} = 3.0V, and then it remains to that state until the 'LT_2V5' signal goes high, i.e. when the system senses that DC-bus Voltage is lower than V_{DC_reg} = 2.5V.

Fig. 43. Scenario where DC-bus overvoltage protection (> V_{DC_max}=3.0V) and V_{DC_reg} = 2.5V is considered.

In Fig. 44, the moments in time where the two transitions mentioned above take place are presented enlarged. At the same time, the cursor is positioned to highlight the corresponding frequencies:

f_{DC_max} = 15.38 kHz for V_{DC_max} = 3.0 V and f_{DC_reg} = 12.9 kHz for V_{DC_reg} = 2.5 V.

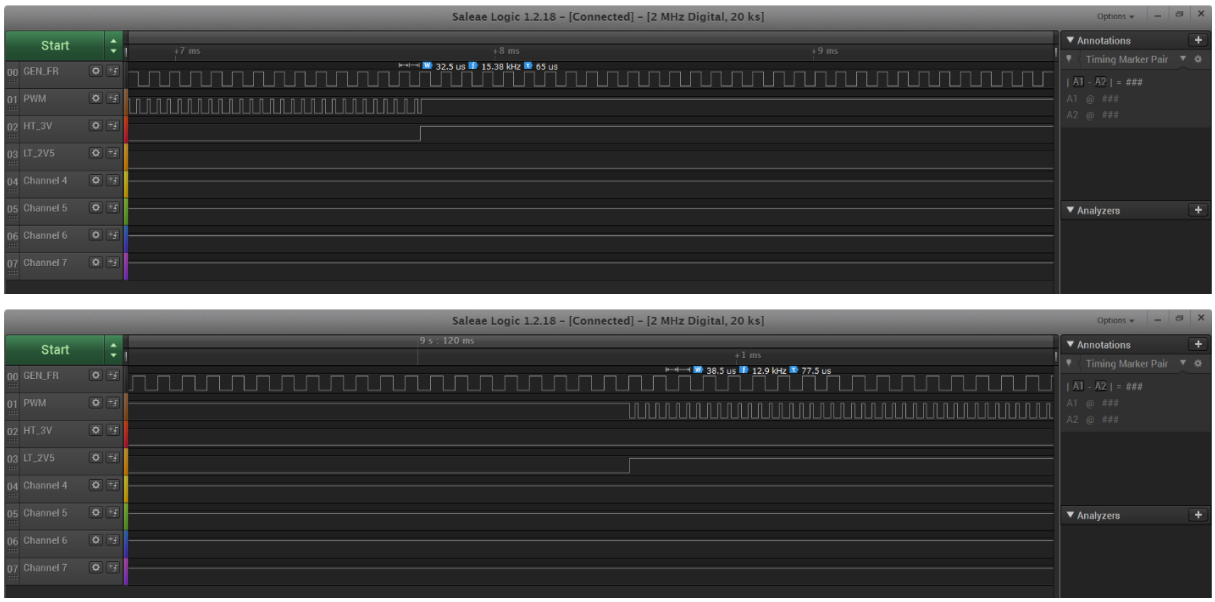


Fig. 44. Magnification of the transitions at a voltage greater than V_{DC_max} = 3.0 V (top) and at a voltage less than V_{DC_reg} = 2.5 V (bottom).

In Fig. 45, the power-voltage and current-voltage characteristics are presented, to verify the correct operation of the MPPT unit with the given PV panel in real operating conditions (outdoors, under clouds). The duty cycle on the MPPT at this time was in the region of 61%.

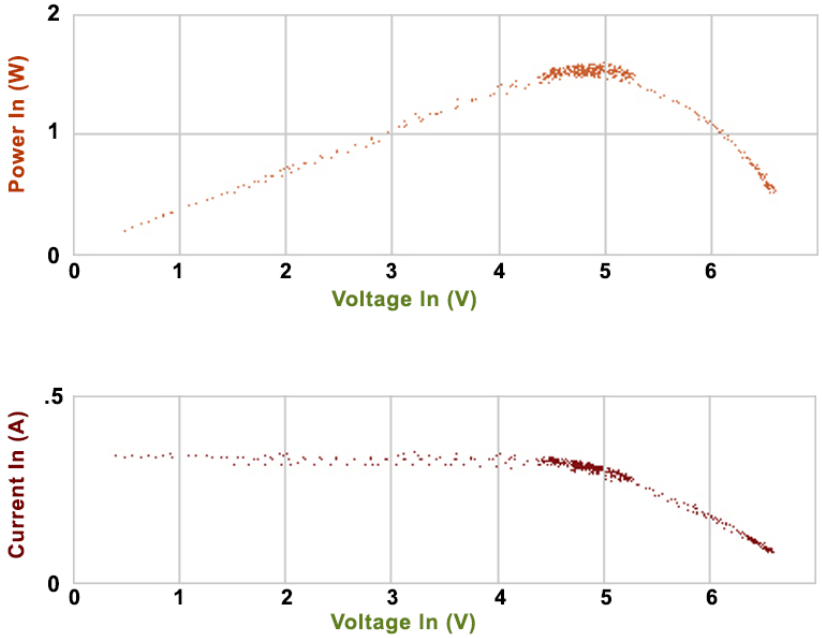


Fig. 45. P-V (top) and I-V (bottom) characteristics of the 1st experimental test of the MPPT module.

Fig. 46 presents a snapshot from the oscilloscope where channel 2 (blue color) shows the driving of the ICL7667 (inverting logic) and channel 1 (yellow color) shows the output of the ICL7667 driving the corresponding MOSFET of the power converter.

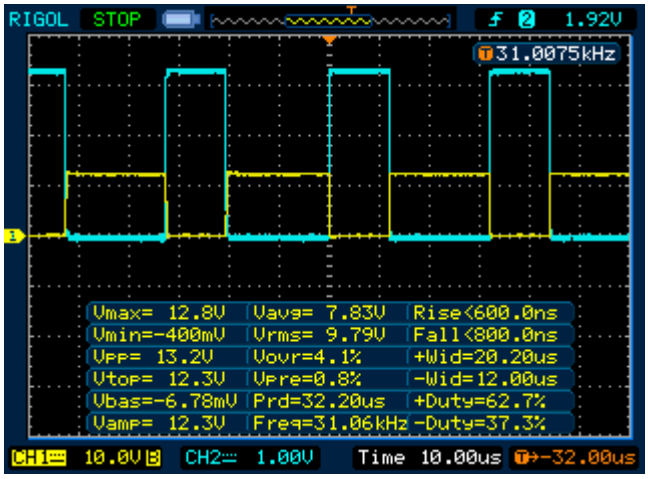


Fig. 46. The duty cycle of the DC/DC converter of the experimental prototype in the 1st test experiment of MPPT operation.

Fig. 47 presents the voltage and current measurements at the input of the DC/DC converter of the experimental prototype during the operation of the MPPT unit and finding the maximum power point of the PV array.

Fig. 47. The input voltage (left) and input current (right) to the DC/DC converter during operation of the MPPT unit and finding the maximum power point in the 1st MPPT experiment.

Fig. 48 presents the power-voltage and current-voltage characteristics of the PV panel during the experimental test of the MPPT unit in real operating conditions (outdoors, under clouds), but with different intensity of incident solar radiation. The duty cycle on the MPPT at this time was in the region of around 59%.

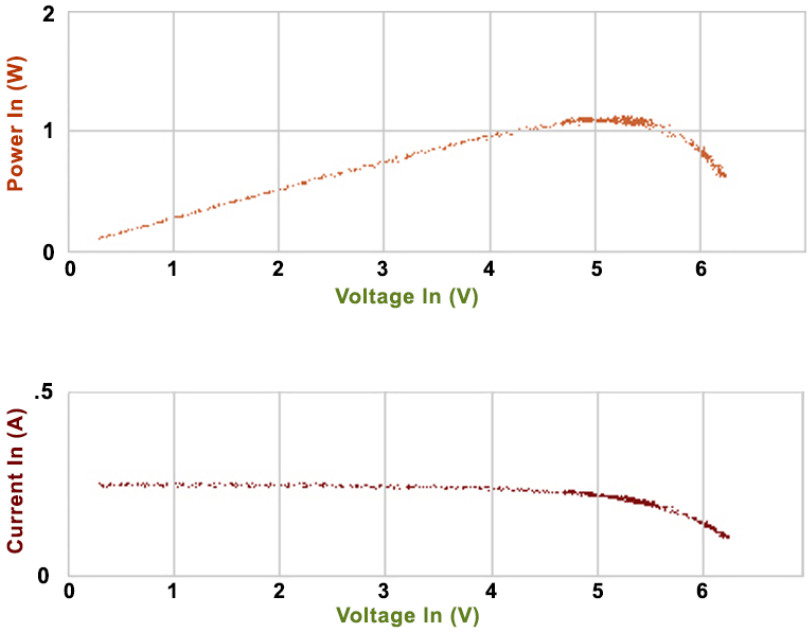


Fig. 48. P-V (top) and I-V (bottom) characteristics of the 2nd experimental test of the MPPT module.

Fig. 49 presents a snapshot from the oscilloscope where channel 2, as in the first experiment, shows the driving of the ICL7667 (inverting logic) and channel 1, the output of the ICL7667 driving the corresponding MOSFET.

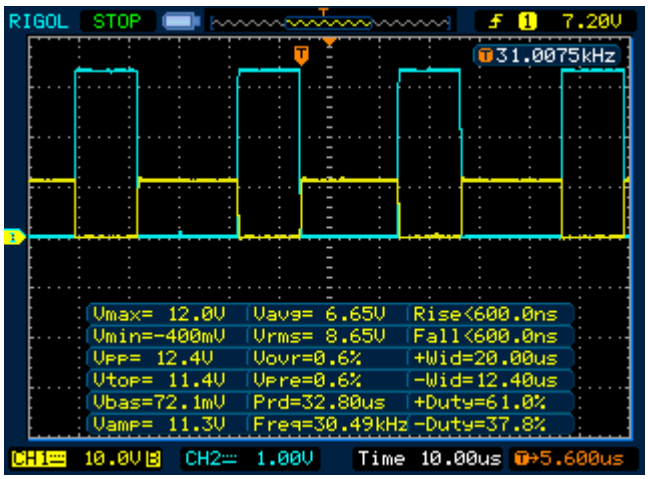


Fig. 49. The duty cycle of the DC/DC converter of the experimental prototype in the 2nd test experiment of MPPT operation.

Fig. 50 presents the voltage and current measurements at the input of the DC/DC converter of the experimental prototype during the operation of the MPPT unit and finding the MPP of the PV array in the 2nd MPPT experiment.

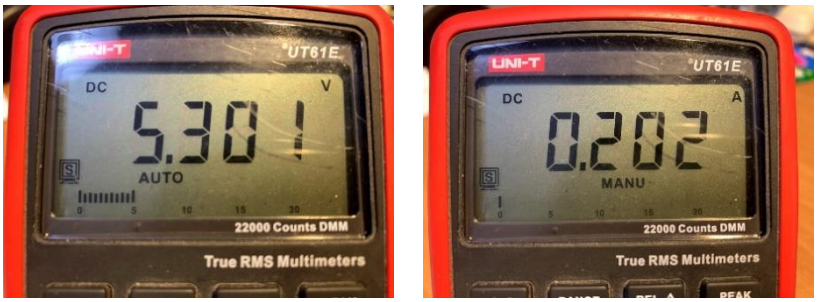


Fig. 50. The input voltage (left) and input current (right) in the DC/DC converter of the experimental prototype in the 2nd MPPT experiment.

4. Uplink PLC for monitoring PV cells

4.1. Introduction

The communications that exploit the power line networks enable the interconnectivity and interoperability of distributed power production units in smart grids and microgrids by using existing cabling to monitor and control the overall power system.

This part of the PhD thesis analyzes a unique uplink PLC approach for cascaded H-bridge converters based on the usage of the circuits of the individual PTDRMs for the transfer of both power and digital data. The DC energy sources of the power modules that synthesize the cascaded H-bridge converter may also be PV cells or arrays. As seen in Fig. 3, this chapter describes the design decisions taken to allow each PTDRM of the array to broadcast its status information to the RMCU. Compared to existing PLC approaches, the developed method combines the benefits of applicability to cascaded H-bridge structures with either a DC or an AC output, while avoiding the use of an additional power amplifier or coupling circuit for the transmission of information, making the system independent of the implementation scale and the type of the power supplied load. This chapter describes the design method followed for the proposed data transmitter and receiver modules using FPGA devices. The developed PLC system has been used to a two-cell cascaded H-bridge inverter experimental prototype. The experimental findings confirmed the successful transfer of telemetry data via the power converter circuit, their recovery by a receiver connected to the power loop, and the concurrent delivery of power to the load.

4.2. Prior art review

During the last years, the electricity industry is increasingly relying on power electronic technologies to meet the multi-scale driven demand for evolving building energy management systems [51], electric vehicles [52, 53], aircrafts [54], smart grids [55], and various commercial Internet of Things (IoT) platforms [56-59]. A key element that enables and supports such transformations is the extended informatics which acts as an interconnecting solution for monitoring and controlling, in a cost-efficient way, the generation, distribution, and consumption of energy. The PLC solutions are preferable when a cabling network, regardless of scale, is existent, and its topology can be exploited to support data-carrying

channels, as such an investment minimizes: (a) overall complexity, (b) failure incidents, (c) maintenance issues, and (d) cost.

In all applications mentioned above, interconnectivity and interoperability of the individual distributed power production units are essential attributes necessary for monitoring and controlling the overall power system. To cover these requirements, the nodes of such networks must establish proper data linking and adequate exchange of information with a central point of command without compromising security. In power systems with multiple distributed nodes, the actual power cable is often utilized as a physical layer for communication to attain such data links, resulting in the implementation of PLC schemes.

The interfacing of the PLC usually requires a separate communication coupling circuit [60], to induce the data in the shared medium. However, this increases the overall complexity of design and cost, especially for the network nodes that are spatially distributed (e.g., in microgrids, photovoltaic arrays, or electric vehicle batteries). Other industrial PLC solutions avoid this design implication by adopting an interfacing architecture that lies in the direct exploitation of a power converter circuit properties by taking advantage of a particular characteristic of its operating principle [61-62].

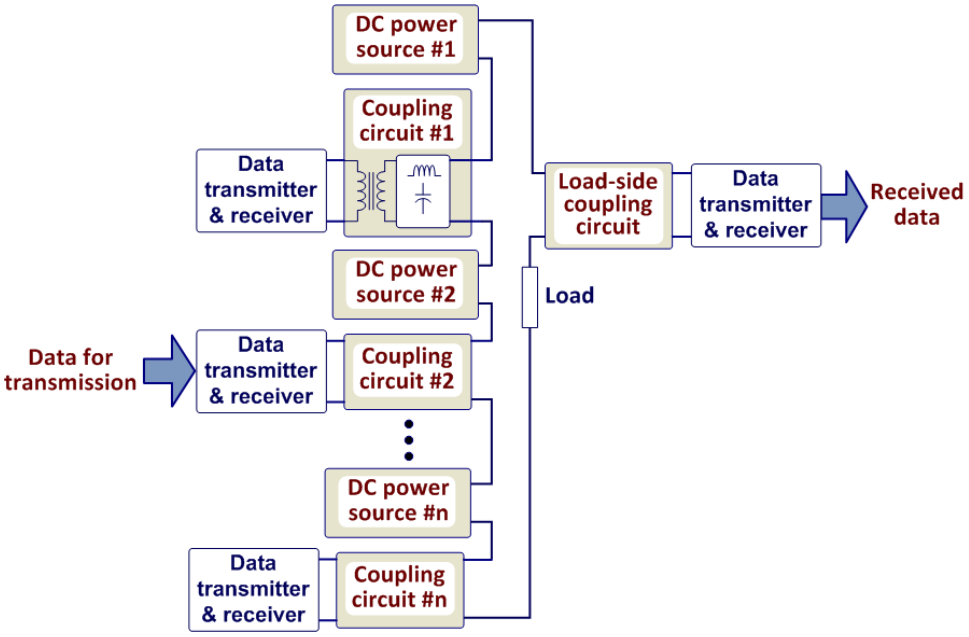


Fig. 51. PLC topology based on the use of separate coupling circuits in DC power sources.

As seen in Fig. 51, the designs of the current PLC topologies are divided into those needing a separate coupling circuit and those in which DC/DC converters connect through a shared DC input or output bus. In its simplest form, PLC is implemented by modulating the

data for transmission and injecting the resultant signal into the power lines through a separate coupling circuit composed of inductive and capacitive components coupled in series, as seen in Fig. 51 [60], [63-64]. According to [60], any modem connected in parallel to a shared two-wire communication line may affect the characteristics of a common carrier signal by changing the impedance it exhibits on the DC-bus linking DC/DC converters with a load. The impedance switching modifies the data according to the communication protocol of the Controller Area Network (CAN). A circuit for detecting envelopes demodulates the sent data. The PLC architecture shown in Fig. 51 has been implemented in [63], which proposes a PV monitoring system.

In the work of [63], a parallel resonant coupling circuit is utilized to inject the modulated signal into the DC power lines linking each PV string to a DC/AC converter. This circuit is coupled in series with each PV module. The digital voltage, current, and temperature readings of each PV module of [63] are modified using amplitude-shift keying (ASK). For demodulation, a parallel resonant coupling circuit linked in series to the DC/AC inverter input is used.

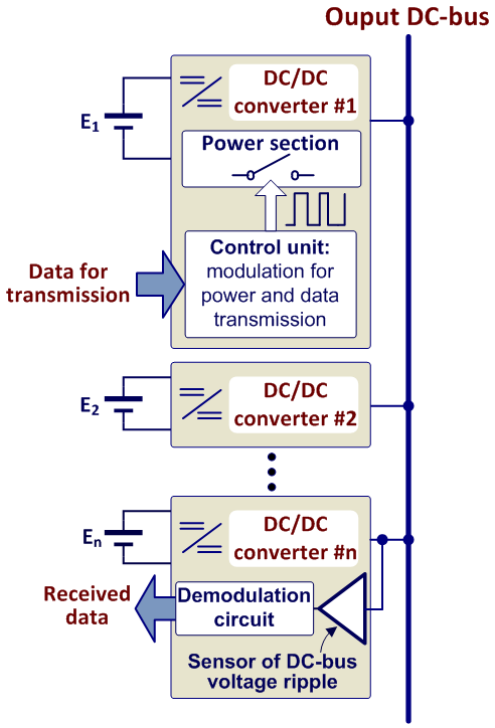


Fig. 52. PLC topology for DC/DC converters communication through a common DC output bus.

The paper of [64] presents a PLC frequency regulating strategy for microgrids. The information to be sent is modulated using an M-ary ASK method. Using an inductive coupling circuit, the resultant signal is injected into the power line. At the receiver end, an inductive

coupling circuit is also needed for signal extraction. The disadvantage of the aforementioned architectures, which are based on the topology of Fig. 51, is that separate coupling circuits must be used at each transmitter and receiver to isolate the communication units from the power lines, thereby increasing the complexity and cost of the overall power system.

Utilizing the power converters as both transmitters of information and producers of electric power is another method for achieving PLC. This strategy reduces the complexity and expense of implementing the power system as a whole. In this application, the PLC architecture shown in Fig. 52 connects the outputs of numerous DC/DC converters to a single DC-bus. The power switches of each power converter are regulated for the concurrent generation of power and modification of information in the DC-bus voltage ripple. This PLC architecture is used in [61-62], [65–69]. The PLC approach described in [65] utilizes the control loop of a DC/DC converter to modulate data using Phase Shift Keying (PSK) in the digital controller of the power converter switches. The study was performed using Buck-type DC/DC converters connected in series within a PV string.

Regarding the use of PLC methods to DC microgrids to improve their operational dependability, [66] proposes the use of Switching Frequency Modulation (SFM) of a power converter to utilize the voltage ripple of the DC-bus voltage. A dual active bridge DC/DC converter and the Fast Fourier Transform (FFT) analysis of the DC-bus voltage accomplish this task. The switching frequency may be recognized and utilized to determine the loading circumstances so that the correct energy management approach can be applied to the remaining converters. This PLC system was designed for the unique topology of the power converter.

In a similar work including full-bridge converters [67], the transmission signal was modulated with phase-shift over the signal for power management. Additionally, this method is only applicable to phase-shift full-bridge converters. In [68], the outputs of bidirectional half-bridge CLLC resonant converters are paralleled to a DC-bus. Spread-spectrum Binary Frequency Shift-Keying (BFSK) modulation is used for their switching frequency, and data transmission is accomplished by monitoring the ensuing DC bus voltage variation. A DC-bus to which AC/DC and DC/DC power converters of different power sources (electric grid, renewable energy sources, battery bank) and switching reluctance motors are linked is discussed in [61]. The operational data of a switching reluctance motor is conveyed to the DC-bus by modulating the turn-off angle of each phase of the motor through control of

the appropriate power converter, therefore exerting a low-frequency voltage ripple on the DC-bus voltage. The process of data demodulation is carried out by evaluating the DC-bus voltage ripple using the autoregressive power spectrum density technique. In [62], synchronous transmission of both power and data signals is achieved by varying the PWM switching frequency of a particular power switch in a power converter designed for switched reluctance generators between two alternative values (corresponding to logic bits 1 and 0). Thus, the DC output voltage ripple of the power converter is modulated based on the provided digital information. The receiver demodulates the transmitted signal using FFT on the resultant output voltage ripple. A similar system is described in [69], in which the turn-off angle of a switching reluctance generator linked to a wind turbine is controlled by the control signals supplied to the generator's power converter. Applying the maximum entropy spectrum estimation approach to the voltage ripple of the DC output voltage of the power converter demodulates the transmitted signal. However, these techniques of simultaneous power and data transfer are limited to applications using switching reluctance machines.

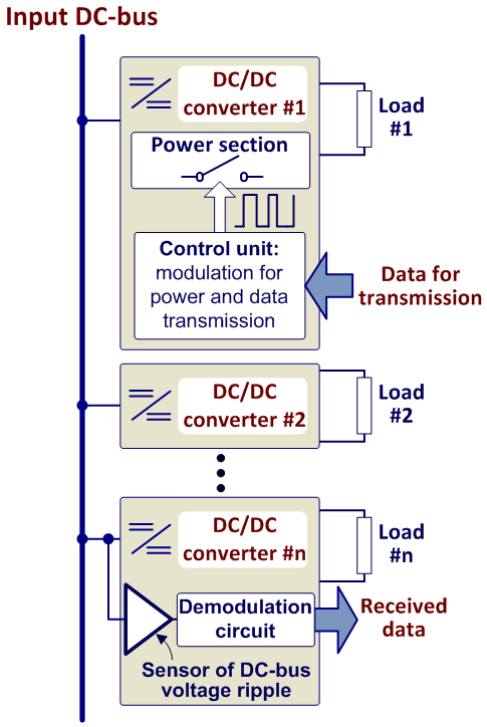


Fig. 53. PLC topology for DC/DC converters communication through a common DC input bus.

In Fig. 53's alternative PLC architecture, the inputs of numerous DC/DC are linked to a common DC-bus, and the communicated information is modulated in the voltage ripple of the DC-bus voltage [70-77]. In [70], the Frequency Shift Keying (FSK) and Pulse-Width Modulation (PWM) modulation techniques are merged. This implementation necessitates an

impedance stabilization network since the magnitude of the carrier must be steady, and the ElectroMagnetic Interference (EMI) generated by the communication ripple must also conform to the requirements. In [71-73], DC/DC converters communicate via FSK and duty-cycle modulation for data transmission, while data reception is achieved by detecting the switching signal on the common DC-bus voltage. All of these receiver solutions rely on band-pass filtering, peak detection, and accurate sampling. In [74], the same idea is implemented by changing a sawtooth oscillator in a normal PWM control circuit of a DC/DC converter to generate an FSK modulated signal. For data demodulation, this PLC method adds an extra analog circuit. To provide bidirectional communication, an information controller is also included, which may receive this information as it is delivered by other DC/DC converters linked in parallel to a shared bus. The research in [75] focuses on data transfer by using the high/low voltage patterns created on the power line by the on/off switching of the Point-of-Load (PoL) DC/DC converter power switches during output voltage regulation. Despite being confined to PoL DC/DC converters, this approach shows that such modules may transmit data by altering the duty cycle of the power switches, so accomplishing the simultaneous transmission of numerous signals to different loads. The control of a DC/DC power converter's switching frequency using a binary FSK technique is presented in [76] to modulate the information of the transmitted symbols (i.e. logic 0 or 1) in the ripple of the power converter's DC output voltage. FSK is also used in [77] to modify the PWM switching (i.e. carrier) frequency of the DC/DC power converter. The demodulation procedure is carried out by applying the discrete Fourier transform on the ripple of the DC input signal.

The authors of [78] describe a technique for the simultaneous transfer of power and data in Buck- and Boost-type DC/DC converters. The data to be communicated are modulated using a direct sequence spread spectrum based on an m-sequence and PSK into the triangular-wave carrier signal of a PWM generator, which generates the final control/drive signal for the power converter. Multiple power converters may exchange data using Code Division Multiple Access (CDMA) communication. The sent data may be recognized by a receiver analyzing the DC input or output voltage ripple. To boost the signal-to-noise ratio when DC/DC converters run in parallel, [79] uses frequency hopping–differential PSK to modulate the data transferred into the triangle signal, which serves as the carrier for the DC/DC converter PWM control process. In this method, the switching frequency varies during data transmission, and the sent data are modulated into the PWM carrier signal's phase.

Among the previously stated PLC approaches, those relying on power converters for the transfer of both power and data have been restricted to DC power architecture. Regarding AC power systems, [80] proposes a method for the communication between power converters in an AC microgrid. Each power converter is regulated in the d−q frame, in which the digital data are modulated using ON/OFF Keying (OOK) and a fractional harmonic carrier frequency. However, this technology was evaluated for the transmission of digital data with low bit rates via a microgrid through power converters.

The outputs of power converters may be coupled in series to construct structures such as cascaded H-bridges, AC-stacked inverters, and similar topologies [81] in order to maximize the efficiency of power generation. The works of [81] and [82] describe circuit-level physical layer models of the communication channel used to create power and convey data to the power converters of such structures (e.g., for synchronization). The transfer of information from the power converters (e.g., for operational monitoring reasons) to a central data acquisition/control unit has not been studied in these studies.

In this PhD thesis, a unique PLC methodology is presented that focuses on cascaded H-bridge converters and uses the circuits of individual power modules to transmit both power and digital information data. The novel suggested approach does this by using the driving signals of power switches on the output H-bridge of the power converter circuit.

Since the Cascaded H-Bridge (CHB) structure is frequently used in industrial networks, and the multilevel inverters (MLI) are a common subset, it seems imperative to consider the use of the CHB MLI in a PLC design that provides high power quality (i.e., low Total Harmonic Distortion, THD), reliable data transmission, and no additional cost to the system design. However, no power line communication systems for the transfer of digital data (for monitoring reasons) over the power circuit of a cascaded H-bridge converter to a remote-control station have been provided as of yet.

Therefore, it will be quite beneficial for the community to regard the findings of this PhD dissertation on alternative control schemes for cascaded H-bridge converters, where both the information signal and the power components are generated by the power circuits of the modules synthesizing a single-phase CHB-MLI to transmit both power and information through the power cable that interconnects the power converter with the load or electric grid. The sent information (data) is digital since transmission is performed by using the power switching patterns of a single CHB-MLI module at any given moment. In contrast to the

previous PLC strategies discussed above, the PLC approach provided in this PhD thesis succeeds to achieve simultaneously the benefits listed below:

(i) it does not require any additional circuit elements (e.g., power amplifiers, coupling circuits, etc.) for the injection of the communication signal into the power line,

(ii) it is applicable in cascaded H-bridge structures with either a DC or an AC output, and so it can be applied to conventional power switching circuits to implement communication schemes with either stacked or distributed power converters [83], and

(iii) it is scalable and can be applied to a wide range of power-supplied loads.

Therefore, the PLC approach described in this dissertation may be simply applied with little design complexity while preserving its great adaptability and scalability. The experimental findings demonstrate that the designed PLC approach operates successfully.

The rest of the chapter is organized as follows. The proposed PLC method in terms of the circuit-level design of both the transmitter and the receiver is described in § 4.3. The simulations analysis is presented § 4.4 and the experimental results are presented in § 4.5. Finally, section § 4.6 investigates issues regarding the THD on the mixed signal that reaches the load and discusses on refinements that can be applied in order to smooth any related considerations.

4.3. The developed uplink PLC method for PV cells telemetry data broadcasting

As a reference, Fig. 54 highlights the position of the system to be described in this chapter, focusing solely on the Uplink transmitting and receiving units.

To further enlighten the reader as to the subsystems involved in implementing the uplink channel of the designed PLC method, the block diagram in Fig. 55 presents an alternative view that focuses on the most preeminent properties and circuitry of the system. This sketch provisions multiple DC power sources, each connected to an H-bridge power converter, thus forming the elementary building blocks of the power system, with each PV cell or module (or the DC/DC converter connected at the output of the PV source) indicated as a “power and data transmission module” (PDTRM). The driving signals of the cascaded H-bridge converter power switches are controlled by a separate digital control unit that is built into each PDTRM, i.e. the digital transmitter shown in Fig. 56, which functions, as discussed

in § 4.3.1, to either create power or transmit information (e.g. DC source current and/or voltage, monitoring data of the PDTRM operation, etc.).

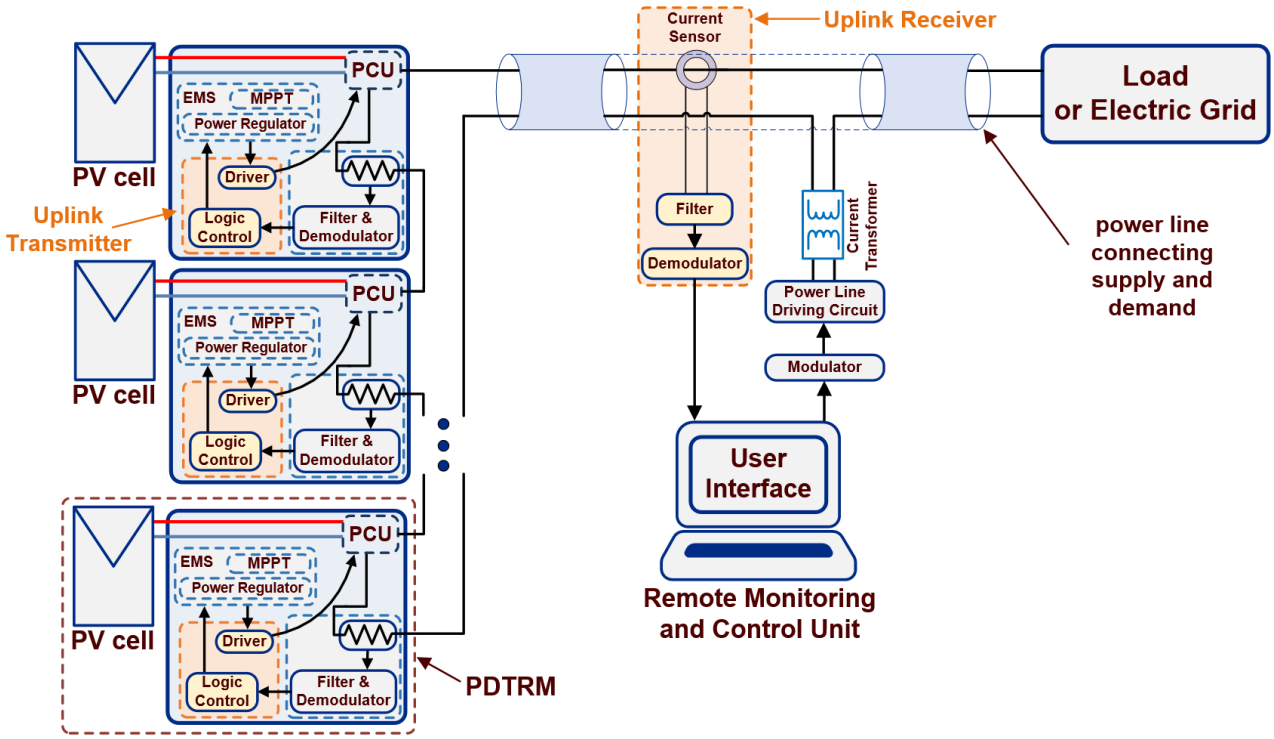


Fig. 54: General diagram of the PV system investigated in this PhD thesis presenting the Uplink PLC units.

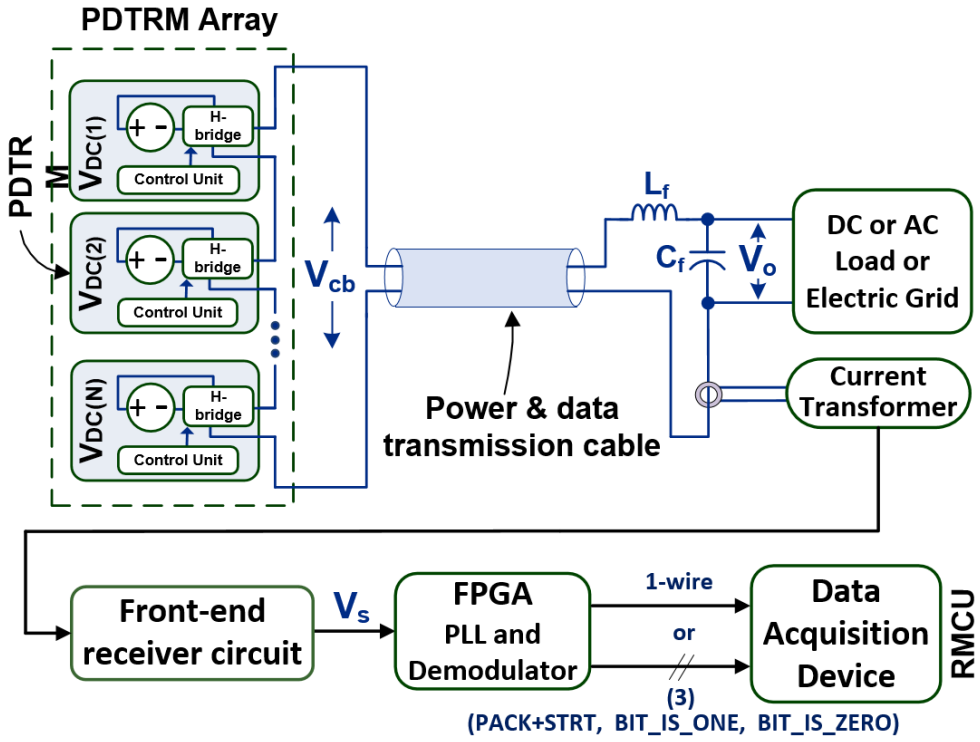


Fig. 55. Block diagram of the proposed PLC scheme for simultaneous generation of power and transmission of digital data.

The PDTRMs of the cascaded H-bridge converter successively broadcast their data. The information communicated by the PDTRMs is then received by a receiver connected to the power connection connecting the PDTRMs string to the DC/AC load or electric grid. The proposed PLC method is also applicable in case that alternative types of DC power sources (e.g. thermoelectric generators, batteries, supercapacitors etc.) are incorporated in the modules of the cascaded H-bridge converter.

As seen in Fig. 55, each H-bridge is power-supplied from a DC voltage source $V_{DC(i)}$. On the other end of the communication line, the receiver first detects the voltage created across a current transformer (alternatively, a Hall sensor may be used), therefore measuring the current developed in the power line. The signal being measured is sent via a high-pass filter and digitizer (front-end receiver circuit). The signal is then sent to a digital Phase Locked Loop and Demodulator (PLL&D), which are implemented in an FPGA unit to construct the bitstream of the information sent by the PDTRMs and send it to the final data-acquisition device (i.e., the aforementioned MCRU which can be realized as a terminal computer). At the load side (e.g., DC or AC load or the electric grid), a low-pass L-C filter is attached to filter the high-frequency harmonics of the composite power/information signal (i.e., V_{cb} in Fig. 55) created at the output terminals of the cascaded H-bridge structure.

Therefore, the power and digital information signals are dissociated, and the power signal is applied to the load while only the previously specified communication receiver acquires the digital information. A similar output filter is also used in cascaded H-bridge converters with PWM control (e.g. in [84]).

4.3.1. The uplink PLC digital data transmitter design

A block diagram of a PDTRM digital data transmitter is presented in Fig. 56. This transmitter functions by leveraging the power switch drivers of each PDTRM's inbuilt H-bridge (terminal full-bridge). The H-bridge driving logic modulates the signal for the transmission interface by creating the required pulses for the waveforms of both the power signal and the data bitstream.

In the context of this study, the digital information communicated by each PDTRM comprises of the DC source current and voltage; however, this may be modified to meet the needs of any specific application. Given that the power system contains numerous PDTRMs,

the transmitter circuit is provided with a 10-bit digital identification (ID) vector that distinguishes the information broadcast by each PDTRM.

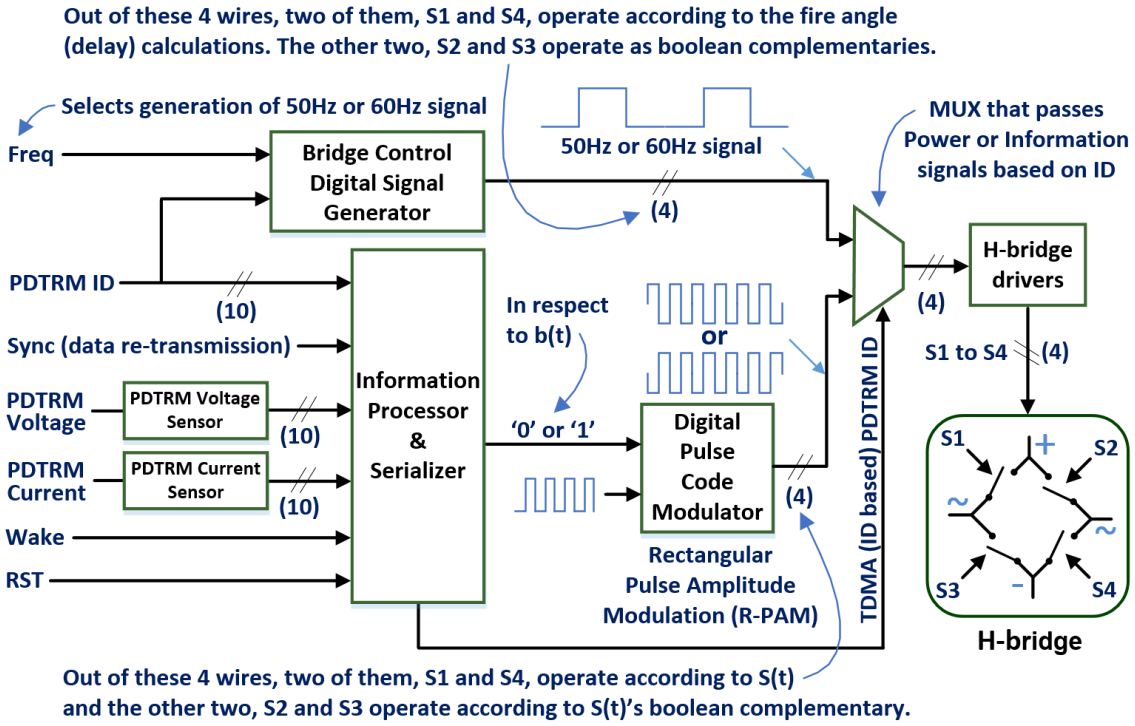


Fig. 56. Block diagram of the digital transmitter in each PDTRM.

This ID is defined in every PDTRM by a hardwired external connection of the appropriate input pins of its digital circuit to either V_{dd} Volts or 0 Volts (i.e. ground level) to represent logic bits 1 and 0, respectively. This ID permits two signal-generating operations, as indicated in Fig. 56, as:

(i) it shapes the output signal of the module 'Bridge Control Digital Signal Generator' (BCDSG), since the pulse width is dependent on the ID of the PDTRM, and

(ii) it dictates the period in which this output must be replaced by the information signal to be delivered.

The signal is created by the 'Digital Pulse Code Modulator' module (DPCM). The information symbol format is based on Rectangular Pulse-Amplitude Modulation (R-PAM), where the phase (0° or 180°) is dependent on the value of the bit to be sent (0 or 1, respectively). DPCM is based on a square-wave generator and digital logic that negates this digital signal based on the serial bits received by the 'Information Processor and Serializer' module (IP&S). To determine the checksum of the information to be sent, the IP&S block employs an embedded CRC polynomial [85]. In addition, it features a parallel to serial interface (P2SI)

allowing the transfer of the resultant bits (information and CRC checksum) in the correct timeslot.

According to the above, the square wave generator creates the sequence $S(t_k)$ at the H-bridge output terminals:

$$S(t_k) = V_{DC,i} \times sgn_a\big(b(t_k) \times \sin(2 \times \pi \times f_c \times t_k)\big) \tag{4.1}$$

where $V_{DC,i}$ is the amplitude of the DC source voltage (as shown in Fig. 55), t_k (sec) is the time instant of the k-th clock edge, f_c is the carrier frequency, $b(t_k)$ acts as a phase reversing switch by changing the sign of the square wave, thus producing the same effect as a 180° degrees shifting, according to:

$$b(t_k) = \begin{cases} -1, & \text{if bit to transmit is 0,} \\ 1, & \text{if bit to transmit is 1.} \end{cases} \tag{4.2}$$

and $sgn_a(x)$ extracts the sign of a real number, as follows:

$$sgn_a(x) = \begin{cases} -1, & \text{if } x < 0, \\ 0, & \text{if } x = 0, \\ 1, & \text{if } x > 0. \end{cases} \tag{4.3}$$

As illustrated in Fig. 56, $b(t)$ represents the binary data given to the first input of the DPCM module. The square wave carrier, illustrated as the second input of the DPCM module in Fig. 56, is transmitted to the output of the DPCM either in phase or 180° out of phase with regard to the reference oscillating signal, depending on the digital information generated by the IP&S module.

If T is the period time (given in the number of clock periods) during which all N PDTRMs of the string must transmit their data according to a Time Division Multiple Access (TDMA) scheme, then the timeslot of the PDTRM with ID n is between t_1 and t_2 where $t_1 = n \times T/N$ and $t_2 = (n+1) \times T/N - 1$.

The pseudo-sinusoidal voltage of the whole PDTRM string is comprised of the total of the digital signals generated by the BCDSG blocks of the individual PDTRMs. As an application case study, the PDTRM string is regarded to be a cascaded multilevel DC/AC converter in this work (C-MLI). As seen in Fig. 57, the firing angle (i.e., the delay that produces the pulse width of the power signal) is computed in clock cycles as follows:

$$delay = floor\left(\arcsin\left(\frac{n}{N}\right) \times \frac{F}{2 \times \pi \times f}\right) \tag{4.4}$$

where $n < N$ is the decimal number of the PDTRM ID, N is the total number of PDTRMs in series in the PDTRM string, F is the frequency of the clock of the digital system (here 2 MHz), and f is the frequency of the waveform to be produced (e.g., 50 or 60 Hz).

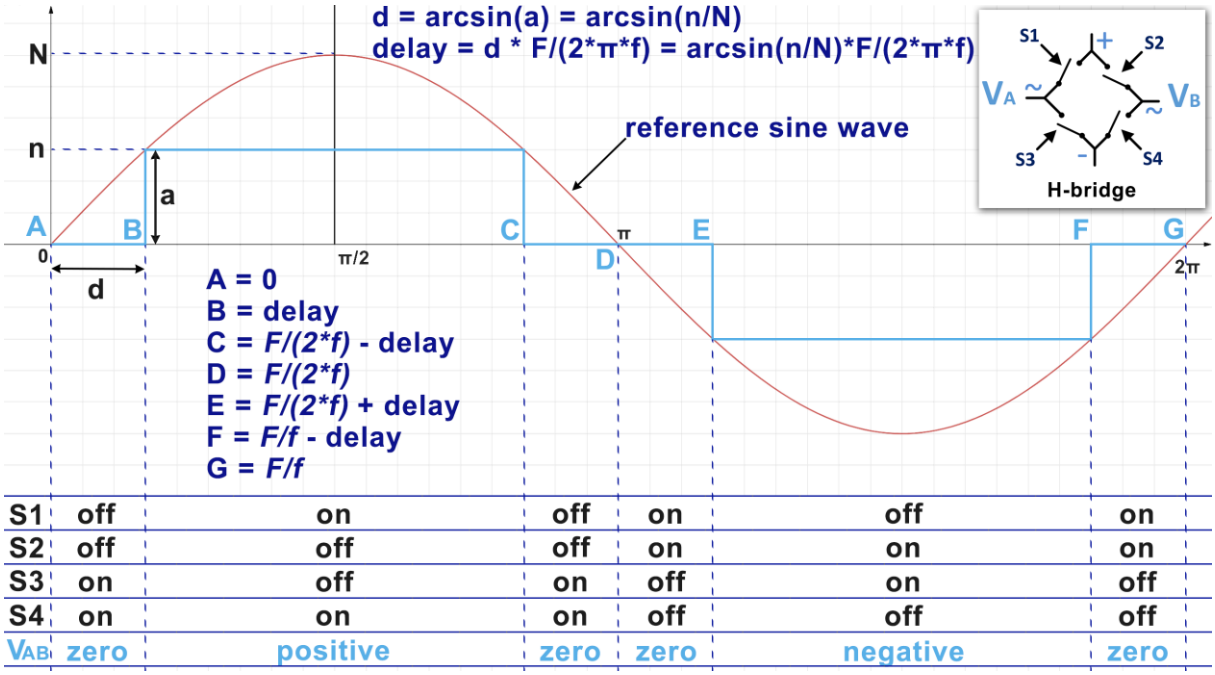


Fig. 57. Delay calculation and driving of the four signals of the nth H-bridge that generates the respective power signal component, for all n<N.

The delay d (in the range of 0-/2 radians) of the nth H-bridge is $d = asin(a)$, where $a = n/N$ (rads) given that the reference sine wave shown in Fig. 57 corresponds to the envelope of the PDTRM string output voltage V_{cb} (i.e., power signal) comprising N PDTRMs in series. This delay is converted into clock pulses by multiplying d by $F/(2 \times \pi \times f)$, as seen in (4.4). Since the clock frequency F is constant, the BCDSG block calculates the number of clock pulses for a quarter of the power signal's period as $F/(4 \times f)$, where f is 50 Hz or 60 Hz depending on the logic state (0 or 1, respectively) of the "Freq" input. As seen in Fig. 57, switches S1-S4 are switched to the ON/OFF state based on the outcome of the corresponding logic comparisons at time instants A-G and the clock counter, which is reset every F/f clocks.

In this study, the fundamental frequency switching modulation strategy described above was favored as it permits the fabrication of a virtually sinusoidal output voltage when the number N of cascaded PDTRMs is medium to high, hence substantially reducing the size of the output filter. By adjusting the PLC carrier frequency f_c in (4.1) to be greater than the PWM switching frequency, the proposed PLC approach may also be used to cascaded H-bridge converters controlled by low switching frequency PWM schemes (e.g. [86]).

In Fig. 56, the DC source current and voltage of each PDTRM are monitored using sensors providing 1-bit PRM signals, which are then transformed to 10-bit vectors by the digital modules 'PDTRM Current Sensor' and 'PDTRM Voltage Sensor'. When a PDTRM moves to a low power state in which it cannot function, its output driving signals (S1-S4) transform the H-bridge into a short circuit by setting the power switches S3 and S4 to the ON state.

This approach enables the continuous transfer of power and data signals between PDTRMs linked in series. S1 to S4 are powered so that the H-bridge operates as a short-circuit until a 'Wake' signal is received from the IP&S digital module of the PDTRM. The 'Wake' signal is utilized for synchronization reasons; hence, it must be sent to all PDTRMs from a single reference source (i.e., a common terminal node), the RMCU. The 'RST' signal is used to reset the control logic to its starting state and stop the S1-S4 as though a low power event had occurred.

4.3.2. The uplink PLC receiver design

The composite power/digital-data signal delivered by the PDTRMs across the power line has components at the carrier frequency f_c and the frequency of the power signal f_s, as well as harmonics caused by the modulation for the production of power and generated noise. Fig. 58 depicts the front-end circuit of the receiver hardware that processes the current transformer output signal (Fig. 55). It comprises of four stages for current sensing, passive differential filtering, differential amplification, and Schmitt-trigger comparator-based digitization.

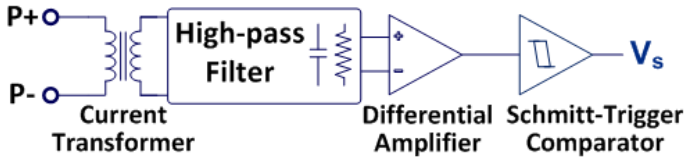


Fig. 58. The front-end circuit of the receiver in the PLC scheme developed in this PhD thesis.

The output signal of the receiver front-end (i.e., V_S in Fig. 58) is then processed by the digital part of the receiver that is shown in Fig. 59, producing the logic signal $R(t_k)$ which has a form similar to (4.1) and can be defined as:

$$\mathrm{R(t_k)} = \mathrm{sgn_b\big(b(t_k) \times \sin(2 \times \pi \times f_c \times t_k + \theta)\big)} \tag{4.5}$$

where θ is the phase shift which depends on the length of the power line from the transmitter to the receiver and the phase shift produced by the amplifiers of the front-end part of the receiver circuit, and $sgn_b(x)$ is defined as follows:

$$\mathrm{sgn_b(x)} = \begin{cases} 0, & \text{if } \mathrm{x} \leq 0, \\ 1, & \text{if } \mathrm{x} > 0. \end{cases} \tag{4.6}$$

The receiver back-end digital system shown in Fig. 59 comprises a Phase-Locked Loop (PLL) and demodulator for the application of a synchronous demodulation technique that requires the presence of a square-wave sequence generator module.

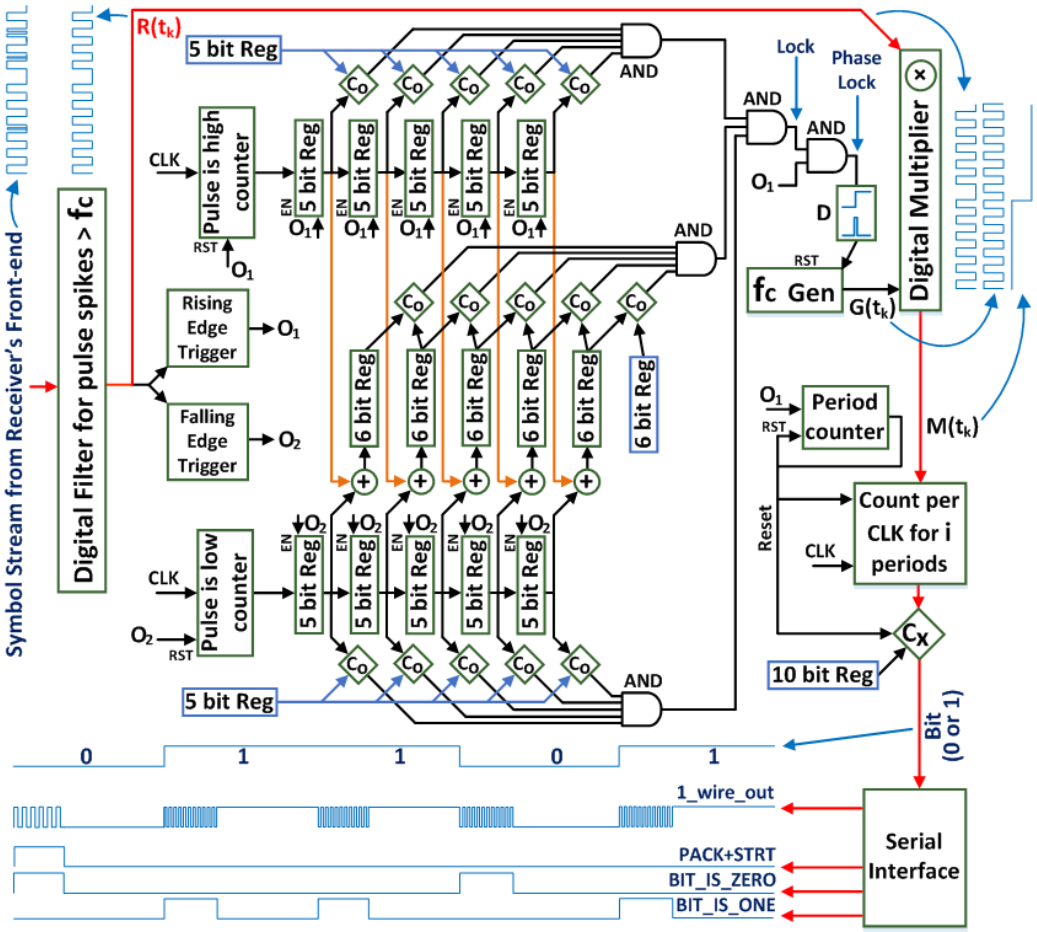


Fig. 59. Block diagram of PLL and demodulator in the proposed PLC receiver.

This module is depicted as the 'f_c Gen' block in Fig. 59, and it is dedicated to creating the following waveform:

$$G(t_k) = sgn_b\big(sin(2 \times \pi \times f_c \times t_k)\big) \tag{4.7}$$

which, once in phase with (4.5), it is digitally multiplied in order to extract the data of $b(t_k)$.

Since the phase shift may be susceptible to tiny variations and/or digital noise may still be present, the initial stage of the receiver's back-end incorporates a digital filter and a phase-locking mechanism to guarantee the best match of (4.5) and (4.7) so that their phase difference is zero. As seen in Fig. 59, the first step of the PLL&D module is a digital filter that eliminates any spikes with a duration of less than one-fourth of F/f_c clock periods. The subsequent step is the real PLL, which begins with two counters, one of which counts the processor clock ticks (CLKs) of the positive pulse peaks (the "pulse is high" counter) and the other counting the CLKs of the negative pulse peaks (the "pulse is low" counter). Each counter feeds a sequence of five registers that load the high and low CLKs of the most recent five periods. A set of five comparators (i.e., blocks "C_0" in Fig. 59) compares the values of the registers that record the subsequent low portions of the carrier periods to a register with a prefixed value (this is half the period of the carrier signal; here, 25 CLKs). A comparable structure records and compares the successive high portions of carrier periods. Finally, the sums of each period's high and low components are compared using a third structure comprised of registers and comparators. To account for any irregularities or glitches in the received signal, the threshold of all comparators is ± 2 clock periods. This structure permits the identification of any pattern resembling a square wave of frequency f_c, indicating the existence of the carrier signal. Proper phase locking is achieved by energizing the locking mechanism upon detection by resetting a square-wave generator with f_c frequency at the rising edge of the observed carrier signal period. Block 'D' in Fig. 59 assures that this triggering will only occur once. A delay will keep this reset signal low (i.e., inactive) until another mechanism detects no bit-change at the 'Serial Interface' block for an extended period of time (for example, one minute) and re-enables block 'D'. This logic locks the produced square pulses so long as the time-dependent phase drift is less than a few clock cycles. Any abrupt changes in phase are seen as intentional phase alterations by the carrier, thus no correction is necessary in this instance.

In the subsequent step, the 'Digital Multiplier' module in Fig. 59 multiplies the digitally filtered carrier with the produced carrier signal, therefore performing a digital down conversion (DDC) [87]. The signals to be multiplied are both digital, thus they may be multiplied by going through a single XNOR gate, as indicated in Equation (8), where is set to 0 since the previous step synchronized the waveforms $G(t_k)$ and $R(t_k)$.

$$M(t_k) = G(t_k) \odot R(t_k) = \\ = sgn_b\left(\sin(C_{t,k})\right) \odot sgn_b\left(b(t_k) \times \sin(C_{t,k} + \theta)\right) \quad (4.8)$$

where $C_{t,k} = 2 \times \pi \times f_c \times t_k$ (4.9)

Since θ=0, the sinusoidal terms can both be substituted with $C_{t,k}$. So, it holds that:

$$M(t_k) = G(t_k) \odot R(t_k) = sgn_b(C_{t,k}) \odot sgn_b(b(t_k) \times C_{t,k}) \quad (4.10)$$

which becomes either 1 when $b(t_k) = 1$ or 0 when $b(t_k) = -1$.

The next step is the integrator and sampler, which gather the logic ones and zeros and provide a more definitive conclusion based on a predetermined threshold. For this purpose, a counter accumulates the high logic samples for a time span equal to a symbol period throughout each processor clock cycle (here 47 x 50 clock periods). A symbol of zero phase is anticipated to create the length of a symbol period following the DDC (in CLKs). The comparator 'C_X' that follows the DDC unit compares the counter's total to a predetermined value equal to half a symbol period (here, this number is stored in a 10 bit register and equals 47 x 25 CLKs). Labeled as a bit equal to 0 if the total is less than this amount; otherwise, identified as a bit equal to 1.

In the last level of the PLL&D block, three digital serial-interface signals are generated to allow the terminal data-acquisition device to demodulate the sent information. The '1-wire' signal in Figs. 55 and 59 includes a Brief Square-Wave Oscillation (BSWO) of a few periods at the beginning of this output signal (at f_a = 20 kHz or f_b = 40 kHz) to indicate the beginning of a packet or a bit, respectively. This BSWO was adjusted at 1/3 of the bit transmission time to allow the tune detection circuit to notice it with ease. The terminal data collection device detects the frequency of the BSWOs using two PLL detectors set to 20 kHz and 40 kHz, respectively. Immediately after the activation of either of the two PLL detectors, the data-acquisition device samples the logic state of the signal with a delay of 1/3 of the bit transmission time. If the triggered PLL is the one that indicates the beginning of a packet, then the sampled bit is regarded as the first bit to be stored in the 51-bit register. If the triggered PLL indicates the beginning of the next bit, the sampled bit is stacked into the appropriate register. When the register is filled, the information is read. Each time the corresponding PLL detector indicates the reception of a new packet, the register is cleared. The '1-wire' signal implies that any bit transfer is preceded by a high frequency BSWO at either f_a or f_b. Consequently, a BSWO at f_a denotes the beginning of a 51-bit packet, and what

follows is the expected first bit of that new packet, whereas a BSWO at f_b indicates the beginning of the second bit of that packet. In Fig. 59, the signal 'PACK+STRT' contains the pulses that indicate the commencement of a packet, the signal 'BIT IS ONE' carries the pulses that indicate the reception of a bit equal to 1, and the signal 'BIT IS ZERO' carries the pulses that indicate the receipt of a bit equal to 0.

4.3.3. Parameters selection in the uplink PLC method

The PDTRM ID, current, and voltage are described by binary vectors of R_1, R_2, and R_3 bits of resolution, respectively. Also, a CRC checksum of C bits in length is added to these vectors to detect accidental errors during their transmission. This means that the information vector comprises $L = R_1 + R_2 + R_3 + C$ information bits. Each such vector will have to be transmitted with a rate of s vectors per second. Therefore, the available time timeslot for transmitting a vector of L bits for each PDTRM is $1/s$. In the case of a PDTRM array formed by PDTRM strings connected in parallel, thus comprising M PDTRMs in total, the vector transmission rate for the entire array will be $S = s / M$. Therefore, $s = S \times M$, where S is expressed in samples per second, and each sample includes the data of all PDTRMs of the array. For proper transmission through a cable conductor, the information needs to be modulated using a carrier of high frequency f_c. In order to exploit the switching operation of the power semiconductors in the terminal H-bridge of each PDTRM, the transmitted information is shaped into square-wave symbols, with each symbol having a duration of an integer number i of periods of that carrier, where each period lasts $T = 1 / \mathrm{f_c}$. The binary representation of bits 0 and 1 is performed by phase-shifting symbol 1 by 180° with reference to symbol 0. This suggests that the binary representation of these symbols can be reconstructed by applying a demodulation technique based on a simple DDC process at the data receiver. Thus, each symbol (or bit) has a duration $d = i \times T$. The total duration of all bits of information is $D = L \times d$. Since each PDTRM timeslot has a duration of $1/s$, the variables R_1, R_2, R_3, C, i, $\mathrm{f_c}$, and s need to be selected to satisfy the following condition:

$$\mathrm{D} \times \mathrm{s} = (\mathrm{R_1} + \mathrm{R_2} + \mathrm{R_3} + \mathrm{C}) \times \mathrm{i} \times \frac{1}{\mathrm{f_c}} \times \mathrm{s} \leq 1 \tag{4.11}$$

In a realistic scenario, the sampling rate S of the overall array, the number M of PDTRMs in that array, and the resolution of the data to be transmitted (i.e., R_1, R_2, R_3) will be imposed by the target application specifications. In turn, this allows for the design parameters i, $\mathrm{f_c}$, and C to be selected such that (4.11) is satisfied. For example, assuming that the specifications

apply to a PDTRM array which comprises 1000 PDTRMs, where each PDTRM can generate up to 10 Volts and 5 Amps (including sensors with a resolution of 1 mV and 2 mA, respectively) and that the required status sampling rate for the entire PDTRM array is once per minute, then it results that R_1=10 bits, R_2=14 bits, R_3=12 bits, S=1/60 samples per second and M=1000. If the designer selects a CRC polynomial of 24 bits and a carrier frequency of 50 kHz and each symbol comprises 50 periods, then (4.11) is satisfied. In case the application requires the addition of safety margins between the data transmission symbols or a proportion of the data transmission time slot to be committed to a communication channel from the terminal data-acquisition unit to the PDTRMs (for example, in the case of a half-duplex communication link), given that the specifications are kept the same, then the designer will need to change the values of i, f_c and C, accordingly. The baud rate of such a topology is f_c / i, where f_c is practically limited by the rising and falling time of the PDTRM H-bridge power switches, and i can be as small as allowed by the receiver sensitivity to distinguish between the two binary symbols.

4.3.4. Power signal generation control circuit

With reference to Fig. 54, the Uplink unit has the purpose of creating 4 signals that enter the drivers of the MOSFET transistors of the DC/AC full-bridge connected to each PV cell. To control the power signals that serve to generate the AC part of the full-bridge, two control units were implemented, each of which is activated depending on whether the PDTRM array is connected to the electrical grid or not. To increase the controllability of the power control circuit of the DC/AC bridges, as well as to examine the correctness of the parameterization, as above, an additional digital subsystem was implemented, which undertakes to drive the 4 signals that end up on the drivers of the MOSFET transistors of the DC/AC full-bridge circuit, according to the commands it receives. This subsystem is used for purposes of debugging and checking the correct design and operation of the other peripheral subsystems of the control and monitoring unit of the overall PV system (a PDTRM version). In Fig. 60, the main units for the production of the 4 signals for the drivers of the DC/AC full-bridge of the PDTRMs PCU ('DUT Stand Alone AC' and 'DUT Grid Tied AC') can be distinguished, as well as the alternative circuit to increase controllability as a 'Debug (Test AC)' section which is the 3rd of the 6 alternative options ('Bridge Control Digital Signal Sensors') which are the 'Debug AC' mode, the 'Stand Alone AC' mode, the 'Grid Tied AC' mode, the 'DC' mode, the 'Short Circuit' mode and the 'Disable All' modes, respectively. The multiplexer is added for selecting one of

the power generation schemes at a time, depending on the value of the 4-bit 'Bridge Control Mode' vector.

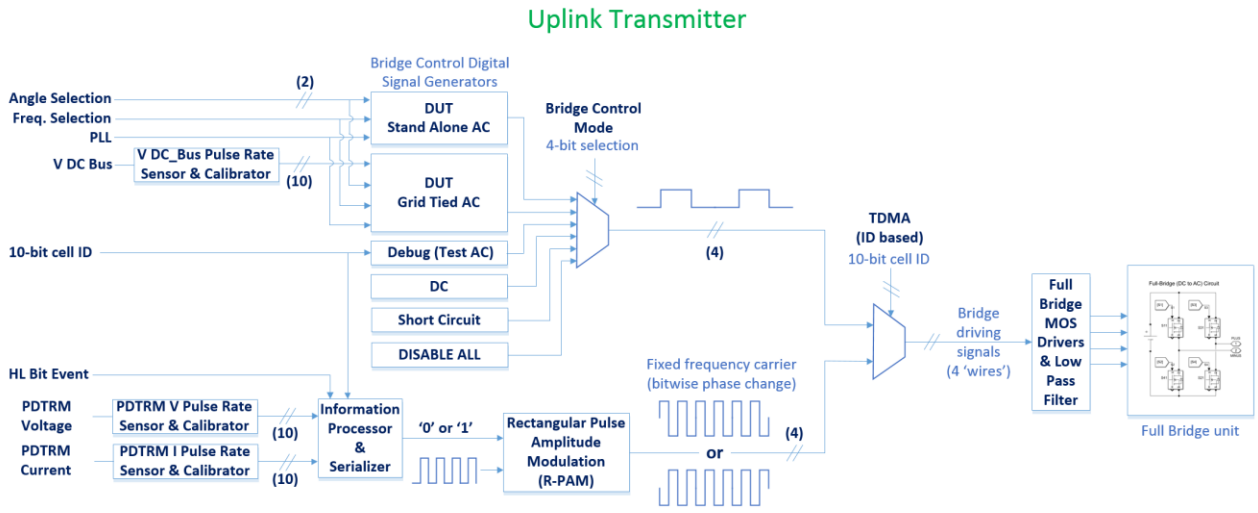


Fig. 60. The general diagram of the Uplink module showing the additions for driving the DC/AC full-bridge of the PV cell PCU and the 'Debug (AC)' section for improved controllability.

The same controllability enhancing logic was applied to one of the inputs of the 'DUT Stand Alone AC' and 'DUT Grid Tied AC' units. The input is called 'Angle Selection', it is common to both modules, and it was implemented to control the behavior of the DC/AC full-bridge at various 'firing' angles of the MOSFET transistors of the PV cell PCU.

4.4. Simulation results

The various versions of digital parts of the Uplink communication circuits design of this PhD thesis has been all set up by programming in VHDL software code on Quartus Prime 18.1, while the VHDL coding was tested and simulated on ModelSim. Their most complex parts were initially tested in Intel's Modelsim and then in Questa Sim-64 by applying specially designed workbenches that covered all operational cases. The back-end of the receiver was implemented on an FPGA development board based on an Altera chipset by Intel (10M50DAF484ES). The computer interface of an 8-channel Logic Analyzer was used for monitoring and capturing the PLC system I/O signals in real-time.

The simulation waveforms in Fig. 61 present the expected behavior of the PDTRM outputs S1 to S4 when a falling-edge trigger pulse is applied on input 'Sync'. When a similar pulse is applied on 'RST', the system operates into the halt mode as mentioned in § 4.3.1. Once a negative-edge 'Wake' pulse is applied, the MSTM begins to control the H-bridge to create a square power component at 50 Hz or 60 Hz, according to the state of the 'Freq' input.

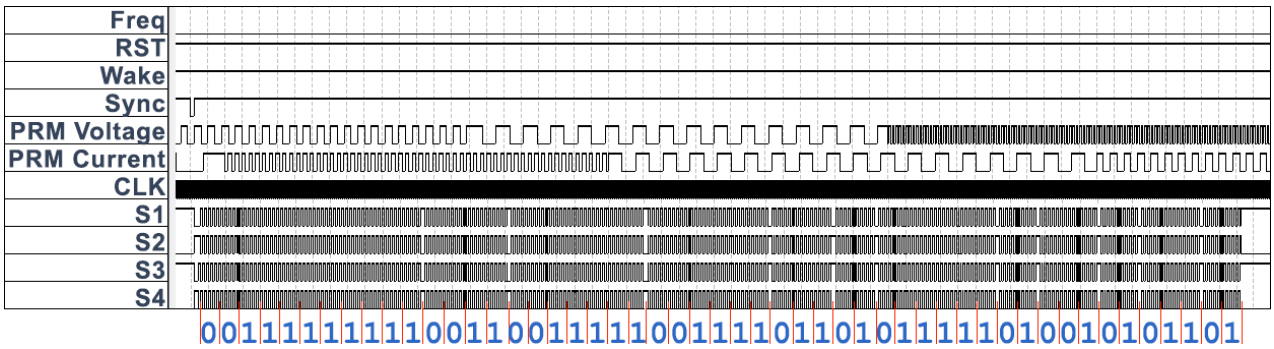


Fig. 61. Screenshot from Quartus testing that focuses on packet's phase changes.

The image capturing rendering of the S1 to S4 reveals the symbol phase-changes as extra thick- or light-colored stripes. Fig. 62 presents a test-bench of the Uplink VHDL code to be synthesized, certifying the unit's proper functioning. As designed, the 'Wake' pulses enable the H-bridge control circuitry and have no effect thereafter other than resetting the internal timeslot estimator. The 'Sync' pulses trigger data transmission. For 'Freq'=1, the power component frequency changes from 50 Hz to 60 Hz, proportionally narrowing the S1 to S4 square waves (Fig. 62).

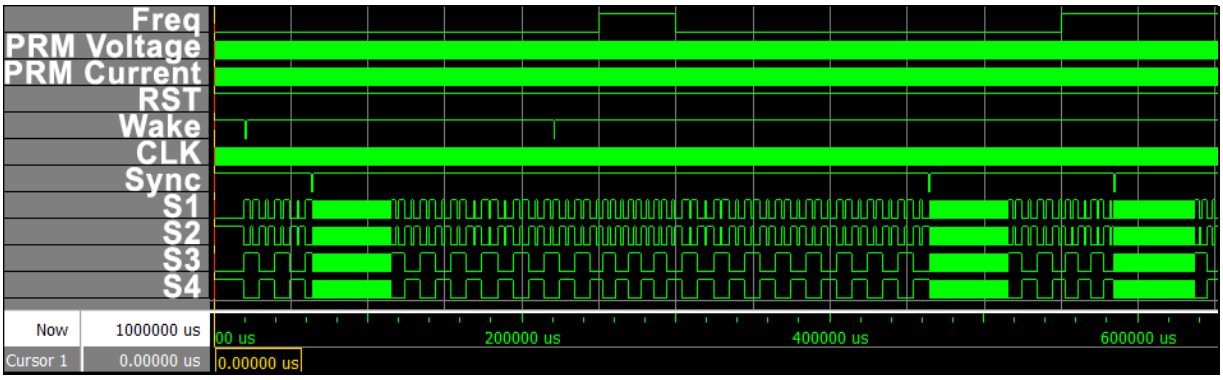


Fig. 62. Testbench screenshot from ModelSim.

4.4.1. Baud rate and bit-error-rate (BER) estimations

The baud rate (symbols per sec) of the Uplink signal is calculated as:

$$Baud\ Rate = f_b = \frac{f_{clock}}{i \cdot P_{CLKs}} = \frac{f_{carrier}}{i} \tag{4.12}$$

where f_{clock} is the clock frequency of the chipset (2 MHz), $f_{carrier}$ is the carrier frequency (40 kHz), i is the carrier periods per symbol (which is formed as a square-wave oscillation by the H-bridge power switches) and P_{CLKs} (50) is the period clock ticks dedicated to form a period of the symbol. So, for the given design it is calculated as follows:

$$f_b = \frac{2 \cdot 10^6}{47 \cdot 50} = 851 \text{ bps} \quad (4.13)$$

The modulation of the signal is using the simplest form of PSK, also called BPSK (binary PSK) or PRK (phase reversal keying) or 2PSK. This modulation was selected as it can handle the highest noise level or distortion before the demodulator reaches an incorrect decision which makes it the most robust of all the PSKs. It is, however, only able to modulate at 1 bit/symbol and so is unsuitable for high data-rate applications.

As to the channel bandwidth B, according to IEEE Std 1901-2010, which is a standard for high speed transmission frequencies over power lines, i.e. broadband over power lines (BPL), the physical medium can deliver robust results for frequencies up to 100 MHz (although in practice the occupied band ranges from 30 to 86 MHz). It is used for the last mile connection (less than 1500m to the premises) to internet access services as well as BPL devices used within buildings for local area networks, smart energy applications, transportation platforms (vehicle), and other data distribution applications (<100m distance between the communicating devices). More specifically, the IEEE P1909.1 is the recommended practice for smart grid communication equipment, test methods and installation requirements. It is a mid-frequency standard (less than 12 MHz) which uses types of Orthogonal Frequency-Division Multiplexing (OFDM), can use TDMA or Carrier-Sense Multiple Access (CSMA), and modulates up to four bits per symbol in Quadrature Amplitude Modulation (16-QAM). So, for the applications to be examined in this PhD thesis, a value of B = 10 MHz =10^7Hz will be assumed, as it is safe to consider pro rata, that the cabling used for a fraction of the last mile connections of such applications will be able to handle this channel bandwidth.

The Carrier-to-Noise Ratio (CNR) is defined as the ratio of the received modulated carrier signal power C to the received noise power N after the receiver filters. With respect to the power of carrier to power of noise, when both carrier and noise are measured across the same impedance, this ratio can equivalently be given as [88]:

$$CNR = \frac{C}{N} = \left(\frac{V_C}{V_N}\right)^2 \quad (4.14)$$

where V_C is the RMS voltage of the carrier signal and V_N is the RMS voltage of noise, i.e. the sum of non-information bearing signals, for the general case.

For an application where the uplink carrier signal has an RMS voltage of V_C= 2.3 V and the C-MLI generates a total RMS voltage of approx. V_N= 230 V, the CNR is equal to:

$$\frac{C}{N} = \left(\frac{2.3}{230}\right)^2 = \left(\frac{1}{100}\right)^2 = 10^{-4} \quad (4.15)$$

Assuming the use of BPSK modulation under Additive White Gaussian Noise (AWGN), the BER, which is also the symbol error rate since in BPSK there is only one bit per symbol, can be calculated as [89]:

$$P_b = Q\left(\sqrt{\frac{2 \cdot E_b}{N_0}}\right) \quad \text{or} \quad (4.16)$$

$$P_e = \frac{1}{2} erfc\left(\sqrt{\frac{E_b}{N_0}}\right) \quad (4.17)$$

where $Q(x)$ gives the probability that a single sample taken from a random process (with zero-mean and unit-variance Gaussian probability density function) will be greater or equal than x, E_b/N_0 is an entity which is closely related to the CNR of the received signal, after the receiver filter but before detection and $erfc(x)$ being the complementary error function, i.e. $erfc(x) = 1 - erf(x)$.

The error function (also called the Gauss error function), often denoted by $erf(x)$, is a complex function of a complex variable x defined as [90]:

$$erf(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt \quad (4.18)$$

For non-negative values of x, the error function has the following interpretation: for a random variable Y that is normally distributed with mean equal to 0 and standard deviation $\frac{1}{\sqrt{2}}$, then $erf(x)$ is the probability that Y falls in the range $[-x, x]$.

In digital communication or data transmission, Eb/N0 (energy per bit to noise power spectral density ratio) is a normalized signal-to-noise ratio (SNR) measure, also known as the "SNR per bit". Eb/N0 directly indicates the power efficiency of the system without regard to modulation type, error correction coding or signal bandwidth (including any use of spread spectrum) [91]. This also avoids any confusion as to which of several definitions of "bandwidth" to apply to the signal.

The relation of E_b/N_0 to CNR (C/N) is shown by [91]:

$$\frac{E_b}{N_0} = \frac{C}{N} \cdot \frac{B}{f_b}, \quad (4.19)$$

where B is the channel bandwidth and f_b is the channel data rate (net bit rate). So,

$$\frac{E_b}{N_0} = 10^{-4} \cdot \frac{5 \cdot 10^7}{2 \cdot 851} = 2.938 \quad (4.20)$$

Subsequently, the anticipated probability of 1 bit of error in an application with the aforementioned specifications is calculated as follows:

$$P_e = \frac{1}{2} \cdot erfc\left(\sqrt{\frac{E_b}{N_0}}\right) = \frac{1}{2} \cdot erfc\,(1.714) = \frac{1}{2} \cdot 15 \cdot 10^{-3} = 0.768\ \% \quad (4.21)$$

This suggests one bit of error every 130 bits of transmitted information.

4.5. Experimental results

The experiments were conducted into two separate stages. The first stage covers the steps followed to verify the operational principle of the developed PLC method on an FPGA-based setup. The second phase was conducted directly onto a fabricated ASIC chipset to test its response to various conditions and verify the proper integration of all subsystems.

4.5.1. 1st stage of experiments (FPGA-based)

The experimental prototype depicted in Fig. 63 has been constructed according to the specifications shown in Table 4.1.

Table 4.1. Specifications of the FPGA experimental prototype.

Parameter of the communication system	Symbol	Value
PDTRMs ID digital representation	$\boldsymbol{R_1}$	10 bits
PDTRM voltage resolution	$\boldsymbol{R_2}$	10 bits
PDTRM current resolution	$\boldsymbol{R_3}$	10 bits
Sampling rate of PDTRM array status	**S**	1 / min
Number of PDTRMs in the array	**N**	2
CRC polynomial length	**C**	21 bits

The FPGA development board (10M50DAF484ES), which is based on an Intel Altera chipset, has the synthesis of the VHDL-developed software code that implements the digital circuit of the PDTRM control logic for the data transmission and reception units.

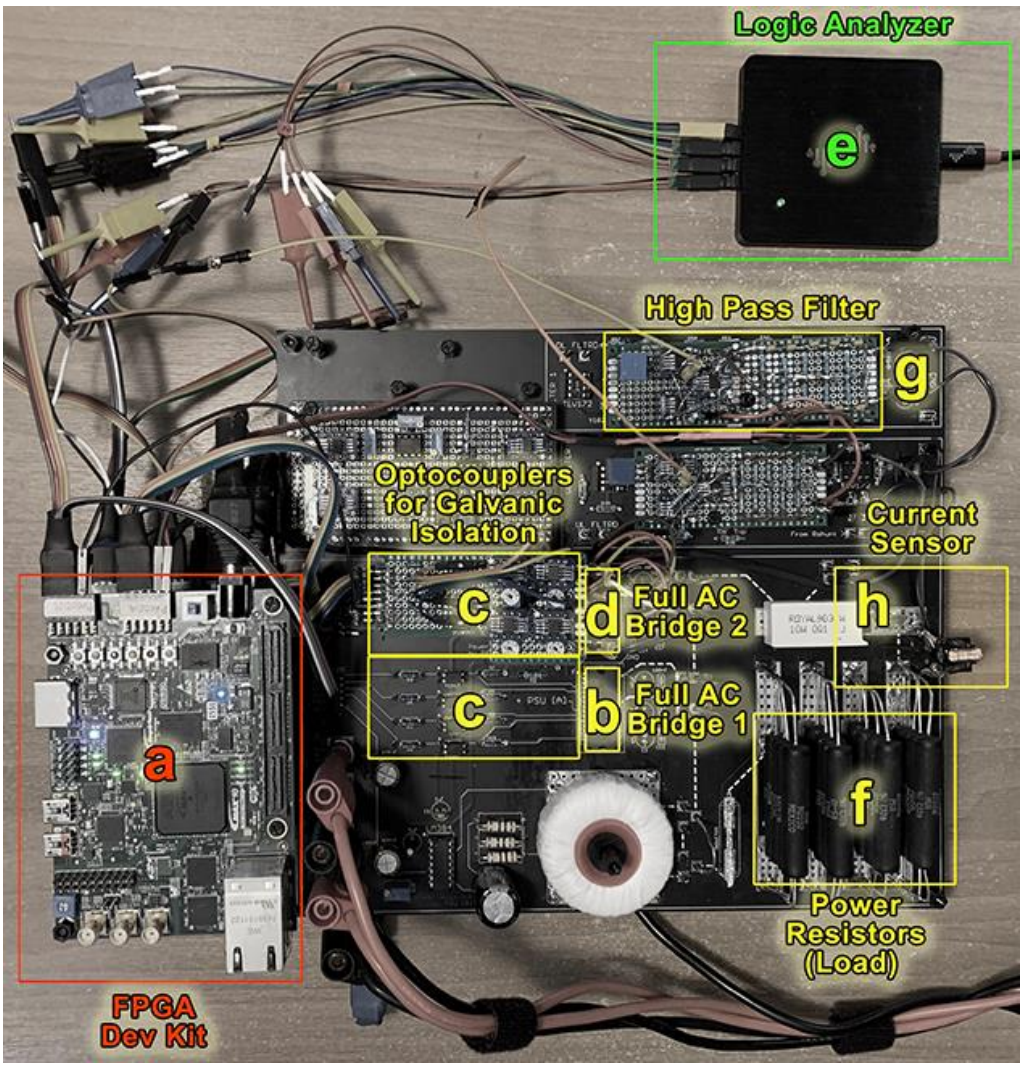


Fig. 63. The experimental prototype developed to verify the operation of the proposed PLC method.

A 16-channel Logic Analyzer and a 2-channel digital oscilloscope were used to monitor the individual signals in real time and assess the functionality of the whole system. The output of the PDTRM string is linked to a 40 Ω resistive load. The PDTRM string comprises of two PDTRM H-bridges. The H-bridges are comprised of IGBTs and were constructed using STGIPQ5C60T-HL chips. The receiver includes a current transformer (turns ratio = 1/100) and a high-pass active differential RC filter of 5th order. This filter, whose layout is seen in Fig. 58, consists of a voltage follower at each input, a differential amplifier, and a comparator stage, all of which are based on MCP6022 operational amplifiers, and it has a cut-off frequency of 284.2 Hz.

Cell ID										Voltage										Current										CRC Checksum											
MSB									LSB	MSB									LSB	MSB									LSB	MSB										LSB
9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	20	19	18	...					1	0

Fig. 64. Breakdown structure of the information in a data transmission packet.

According to the specifications of Table 4.1, each PDTRM unit's data transmission to the data-acquisition device (Fig. 55) consists of 30 + 21 = 51 bits of information. Fig. 64 depicts the breakdown structure of the 51-bit packet. Each packet's least significant bit (LSB), which is also the LSB of the CRC checksum, is always equal to logic 1. The MSB of the PDTRM ID is sent before any other bits. The first 30 bits are the ID (10 bits), measured voltage (10 bits), and measured current (10 bits) of the PDTRM, whereas the final 21 bits are the CRC checksum of the first 30 bits. Under the assumption of a low constant random independent bit error rate, the selected 21-bit CRC polynomial has the greatest Hamiltonian distance (BER). On a 40 kHz carrier, the 51-bit stream is sent as square pulses modulated by R-PAM. Each symbol consists of 47 periods, each of which lasts 25 μsec. Consequently, the period of each symbol (bit 1 or 0) is 47 x 25 = 1175 μsec. Although symbol 1 is built similarly to symbol 0 (having the same number of periods and period length), it exhibits a 180° phase shift relative to symbol 0.

The chosen design parameters indicate that the PLC system can handle the operation of an array including up to M=1000 PDTRMs (e.g. employing the individual PV cells of a PV array). Since all M PDTRM units must transmit one data packet per minute, each minute is split into M=1000 equal time intervals (timeslots) and each interval is numbered and allocated to a PDTRM based on its ID. Consequently, each PDTRM has a predetermined timeslot during which it is anticipated to send its information packet via TDMA, with each timeslot lasting 1/s = 1 / (S x M) = 60 / 1000 = 60 msec. In this experimental arrangement, the data transmission time is 51 x 1.17 = 59.925 milliseconds, which satisfies the formula (4.11). Each PDTRM transmitter has a counter that overflows to indicate the end of a timeslot, which is then supplied to a counter that monitors these occurrences. Based on the PDTRM ID, this method estimates the timeslot available for the serial transmission of 51 bits of information. Due to the consistent TDMA method, each of the M (total) PDTRM units is intended to communicate its status information on a specified timeslot, based on its ID value, in the general scenario. This implies that at any one moment, precisely one PDTRM is providing its status information (the one with an ID corresponding to the specified timeslot), while the other M-1 PDTRMs are committed to generating the power signal. This dissertation's PLC technique may be used for:

a) the routine transmission of a few bits of digital data for synchronization and control during energy management processes, or alerts regarding the operational status of

the individual PDTRMs (for example, diagnostics about operational faults of the power switches in a PDTRM in accordance with [92]), and

b) the transmission of lengthier information messages (such as 51 bits in our experimental arrangement) with a repeat rate on the order of many tens of seconds to satisfy the needs for grid energy management [93], grid energy monitoring [63], and other requirements.

In this experimental configuration, 1 bit of information must be sent by each PDTRM in 1.175 msec, which is much less than the transmission repetition rate in the aforementioned applications. Therefore, the influence of the utilized TDMA technique on the total power output capabilities of the cascaded H-bridge converter is insignificant. It offers data transmission capabilities to the individual PDTRMs of the cascaded H-bridge converter. Each PDTRM of the cascaded H-bridge inverter contributes one component to the overall power signal vector. Keeping the firing angle constant and dependent on the ID means that one of these vector components will be replaced by data transmission at any given moment. In this situation, the reduced THD will be obtained by ensuring that the sequence of the PDTRM transmission is identical to the sequence of their power generating components, with their firing angles computed according to (4.4) and assessed in section § 4.3.1.

To further reduce the THD, an additional rule is included. It is believed that the PDTRMs broadcast in a sequential (round-robin) manner, with the PDTRM with ID=1 transmitting first and the PDTRM with ID=M transmitting last. This additional rule requires the PDTRM with ID=X to take over the creation of the power vector component of the following PDTRM ('X+1') as soon as it completes its transmission and to continue operating according to this concept until the round-robin sequence is restarted. As seen in Fig. 65, such a disposition is applied to every successive pair at the appropriate moment.

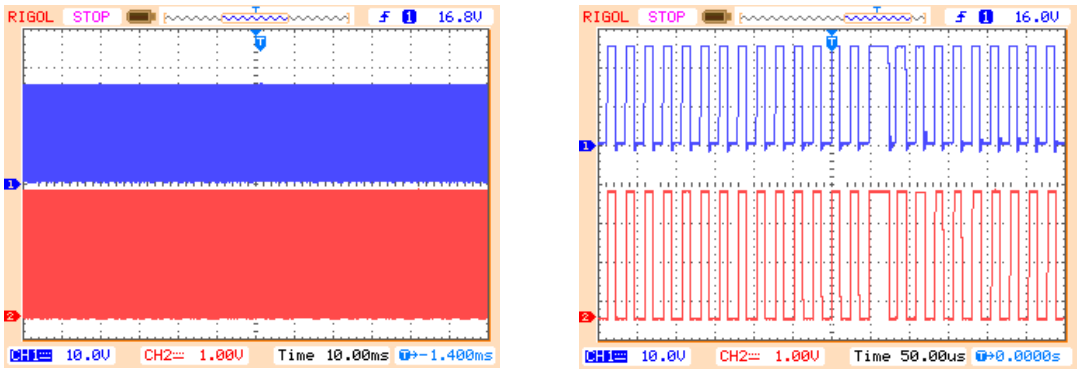
The modulation of each PDTM during M+2 sequential timeslots

Timeslot number	1	2	3	4	...	M-1	M	1	2	...
PDTM with ID 1	**DTr 1**	Cmp A	Cmp A	Cmp A	...	Cmp A	Cmp A	**DTr 1**	Cmp A	...
PDTM with ID 2	Cmp A	**DTr 2**	Cmp B	Cmp B	...	Cmp B	Cmp B	Cmp A	**DTr 2**	...
PDTM with ID 3	Cmp B	Cmp B	**DTr 3**	Cmp C	...	Cmp C	Cmp C	Cmp B	Cmp B	...
PDTM with ID 4	Cmp C	Cmp C	Cmp C	**DTr 4**	...	Cmp M-1	Cmp M-1	Cmp C	Cmp C	...
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
PDTM with ID M-1	Cmp M-1	Cmp M-1	Cmp M-1	Cmp M-1	...	**DTr M-1**	Cmp M	Cmp M-1	Cmp M-1	...
PDTM with ID M	Cmp M	Cmp M	Cmp M	Cmp M	...	Cmp M	**DTr M**	Cmp M	Cmp M	...

"Cmp 1" to "Cmp M" refer to the AC power vector component X, where X is 1 to M
"DTr 1" to "DTr M" stand for 'Data transmission of the PDTM with ID = X', where X is 1 to M

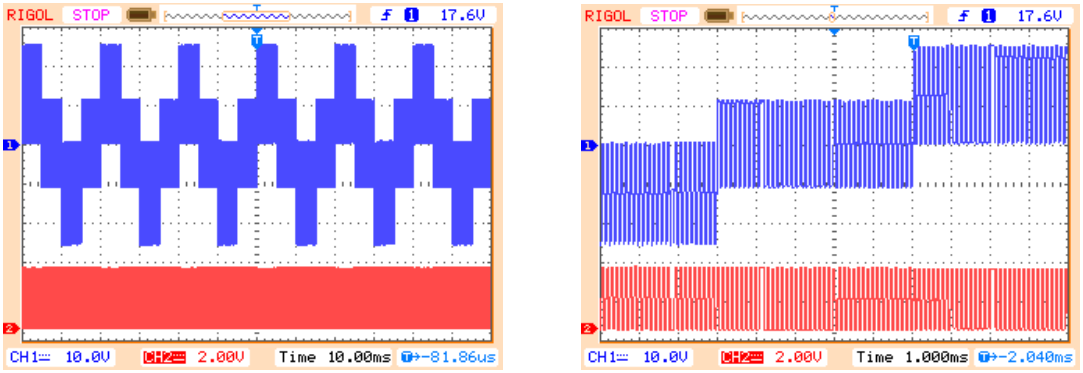
Fig. 65. The modulation of each PDTRM during M+2 sequential timeslots.

This rule ensures that all M-1 PDTRMs will generate the same power signal at all times. As an application example in this experimental setup, N=2 H-bridges are employed to transmit their status data interchangeably.



(a) (b)

Fig. 66. Oscilloscope waveforms of V_o (channel 1, 10V/div) and V_s (channel 2, 1V/div) when the two PDTRM units are set to create DC and they interchangeably transmit their data packets (R-PAM at 40 kHz, for 59.925 msec): (a) at 10ms/div, (b) zoom-in view at 50us/div.



(a) (b)

Fig. 67. Oscilloscope waveforms of V_o (channel 1, 10V/div) and V_s (channel 2, 2V/div) when the two PDTRM units are set to create AC and they interchangeably transmit their data packets (R-PAM at 40 kHz, for 59.925 msec): (a) at 10ms/div, (b) zoom-in view at 1ms/div.

Initially, the L-C filter at the output of the power line (Fig. 55) was not connected and therefore $V_{cb} = V_o$. The experimental oscilloscope waveforms in Fig. 66 present V_o and V_s (shown in Fig. 55) when the PDTRM units are set to produce a DC output voltage, and one of them is triggered to transmit a 51-bit packet of information. Fig. 67 depicts the same voltages when the PDTRM units are set to produce an AC output voltage and transmit their data packets interchangeably, illustrating the superimposition of the information signal on top of the power signal.

Figs. 68 and 69 depict the equivalent spectrum diagrams for the two PDTRM units when data is delivered over DC and AC, respectively. Both graphs depict the fundamental carrier frequency of f_c=40 kHz and its V_o and V_s harmonics.

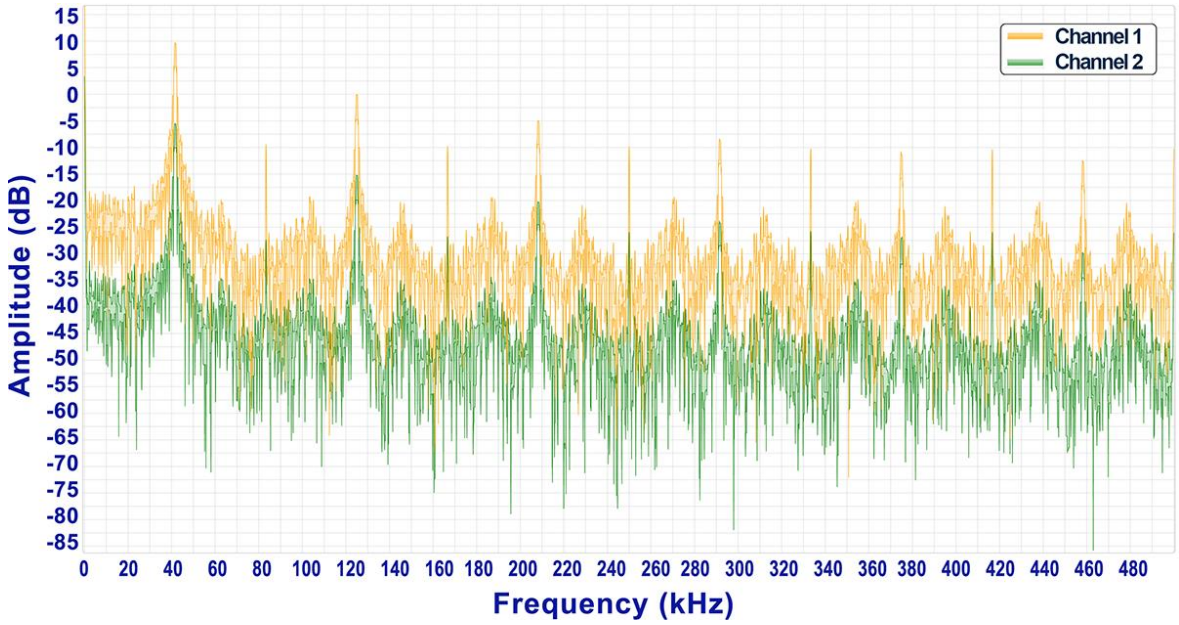


Fig. 68. The experimentally measured spectrum analysis of V_o (channel 1), and V_s (channel 2) when data is transmitted over DC.

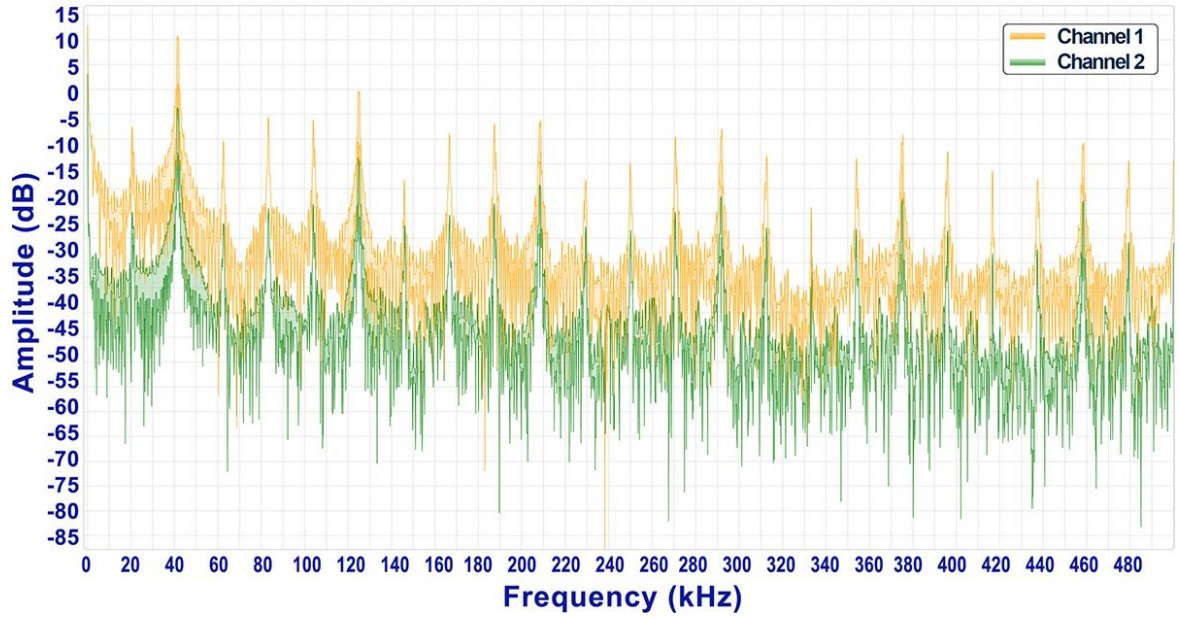
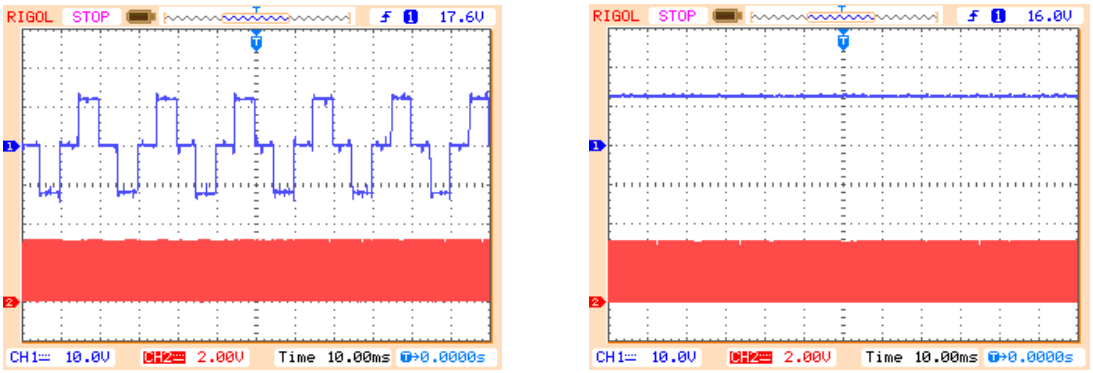


Fig. 69. The experimentally measured spectrum analysis of V_o (channel 1) and V_s (channel 2) during the simultaneous AC power and data transmission.

The switching frequency value f_c=40 kHz is consistent with that utilized in current cascaded H-bridge systems (e.g., [94]), in which other modulation methods are employed only

for power transmission. Thus, the intended PLC approach may be implemented using ordinary design methods for cascaded H-bridge converters, without putting any extra restrictions on the switching speed capacity of the power semiconductors. However, this technique has the added advantage of transmitting both power and digital information over the power circuit of the PDTRMs.



(a) (b)

Fig. 70. Oscilloscope waveform of V_o (channel 1, 10V/div, 10ms/div) and V_s (channel 2, 2V/div, 10ms/div) when an L-C filter is used to filter the transmitted data over the: (a) AC and (b) DC power signal.

The voltage V_o recorded on the load side after the LC stage filtering according to Fig. 55, with L_f =400 μH and C_f =19.7 μF. is shown in Fig. 70. In the design of the L-C filter, these values of L_f and C_f were chosen so that only the harmonics of the cascaded H-bridge output voltage (i.e. V_{cb} in Fig. 55) caused by the transmission of digital data using the PLC technique were filtered. In both situations (AC and DC power generation), as seen in Fig. 70, the digital data signal is effectively eliminated, leaving just the power signal component to be supplied to the output load.

In order to demodulate the sent information, the PLC receiver simultaneously isolates the data transmission signal from the composite signal of the power connection, as explained below. In this instance, the amplitude of V_o is less than in Fig. 67(a) because, for demonstration reasons in this experimental configuration, the two PDTRMs of the cascaded H-bridge converter were configured to send digital data constantly and alternately.

As discussed before, the transmission duration of each PDTRM relies on the length of the broadcast bit stream and the repetition rate of the data transmissions, both of which are chosen by the designer to meet the requirements of the intended application. Due to the interlacing effect, Fig. 71 depicts the differentiation of transmitted symbols as a color grading flip, which facilitates the detection of places where the R-PAM signal phase is changing.

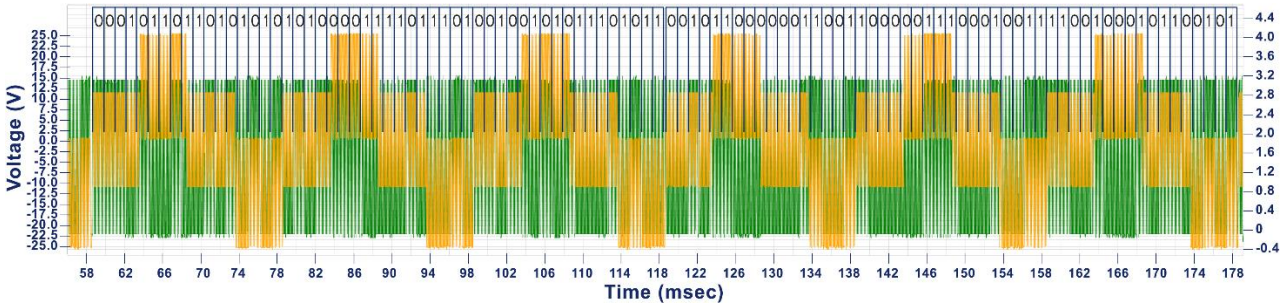


Fig. 71. Distinction of the actual transmitted symbols in the oscilloscope waveforms of V_o (channel 1) and V_S (channel 2) during the transmission of the two 51-bit packets of information of each one of the two PDTRM units. The interlacing effect facilitates towards the distinction of the symbols since every phase-change flips the color grading of the square waves.

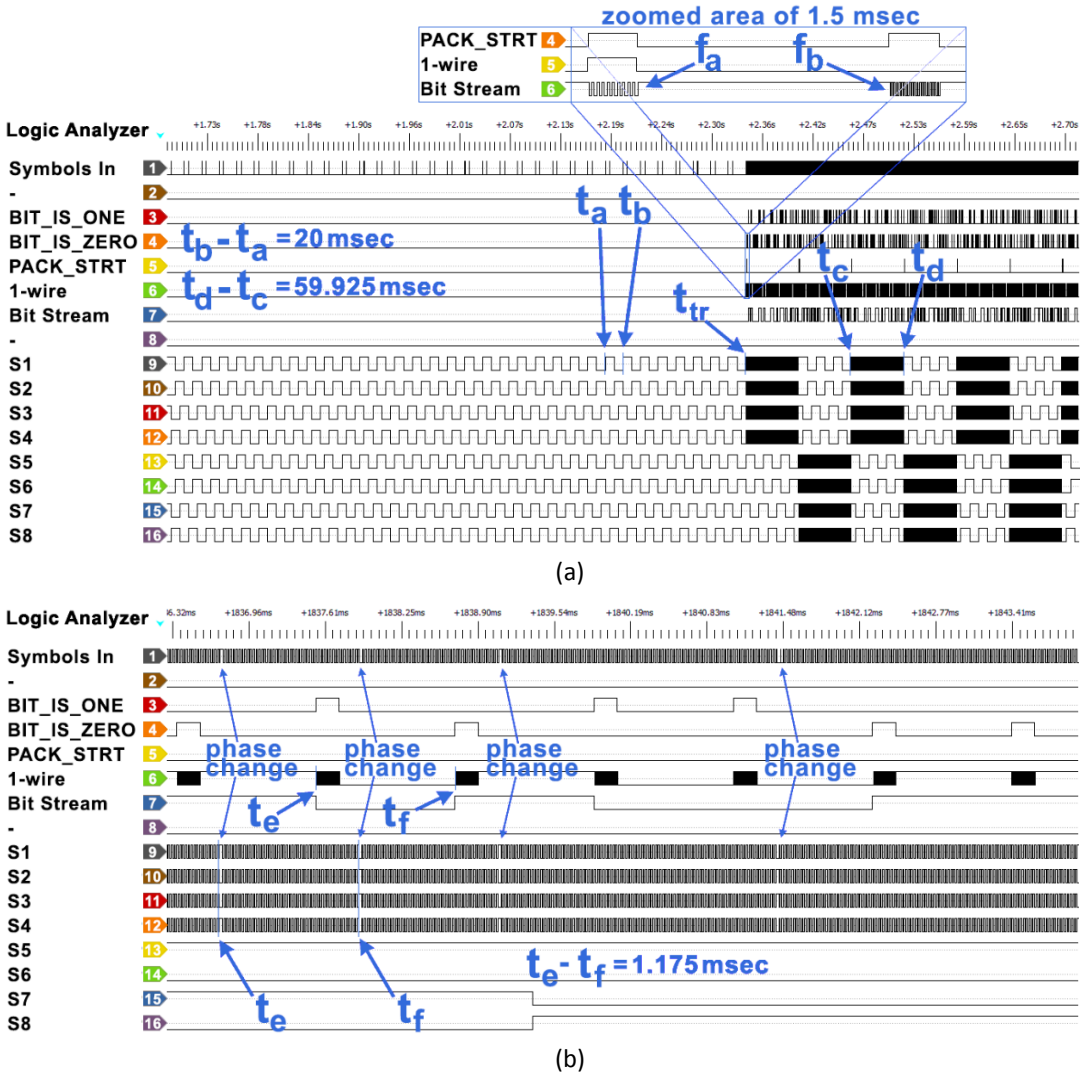


Fig. 72. Logic analyzer experimental waveforms of the transmitter principal signals: (a) presenting the interchanging transmission of two 51-bit packets of data, (b) a zoomed interval depicting the symbols corresponding to bits “0101100”.

The driving signals of the two H-bridges (S1-S4 and S5-S8, respectively) are displayed in Fig. 72. It is apparent that after the t_{tr} time instant the two units begin to transmit their

information interchangeably. The timing markers t_a and t_b on Fig. 72(a) emphasize the interval of one period of the power signal.

The timing markers t_c and t_d show that the information transmitted (i.e. the 51-bits sequence) requires approximately 59.925 msec. The zoomed area of Fig. 72(a) shows the expression of the BSWOs described in § 4.3.2, i.e. f_a and f_b on the '1-wire' signal. The 'Symbols In' signal presents the information that the current sensor intercepts as current fluctuations caused by the transmission of data, which are forwarded to the receiver, and the result of the process is displayed on the 'Bit Stream' signal to confirm the successful reception. Fig. 72(b) presents a zoomed plot, focusing on phase changes of the information signal. The timing markers t_e and t_f show the duration of one bit (or one symbol) of information, which is 1.175 msec. The waveforms S1 to S4 in Fig. 72(b), begin with the bit 0 (on the left), followed by a phase change to bit 1, then to bit 0, then to two bits of 1, and finally to two bits of 0, thus transmitting the symbols that correspond to the sequence "0101100".

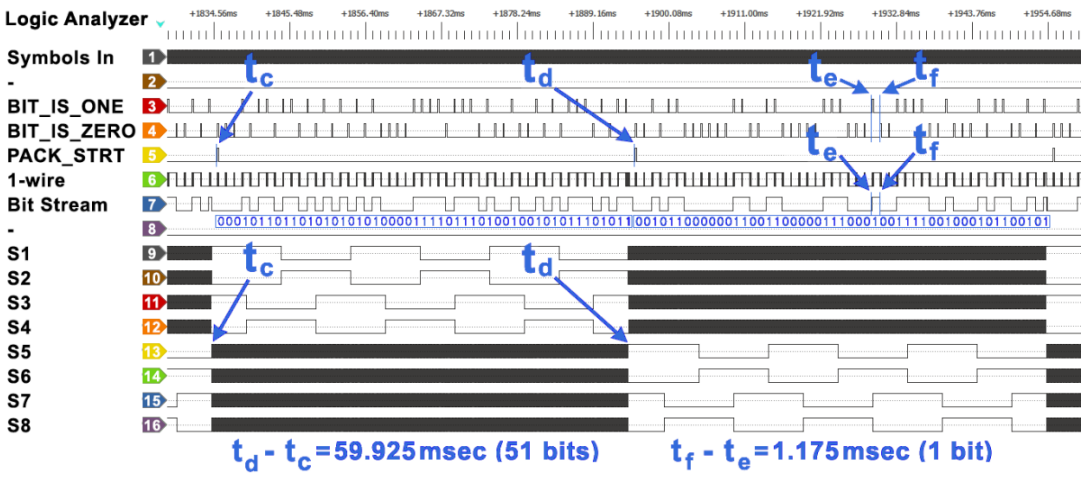


Fig. 73. Logic analyzer experimental waveforms that focus on the interchanging between the power components of the two PDTRMs (which alternate but - in total - preserve the anticipated power wave sequence) and the transmission of their respective packets of information.

Fig. 73 focuses on the two alternating packets of information. These have been acquired by the PLC receiver and the demodulation result is presented by the 'Bit Stream' digital signal. The digital signals produced for the demodulation of the transmitted information at the remote data-acquisition computer interface shown in Fig. 55, as analyzed in § 4.3, are also presented in Fig. 73 in channels 3 to 5. As it can be observed, the pulses of the signals 'BIT_IS_ONE' and 'BIT_IS_ZERO' in Fig. 73 are alternating in the same order as the symbols shown in Fig. 71. The demodulated bitstream is also shown in channel 7 of Fig. 73 and is also

quoted with actual digits on the designated space for the waveform of channel 8 of the same figure. A comparison between the bitstreams of Fig. 71 and Fig. 73 confirms that the transmitted telemetry data have been successfully received.

The power conversion efficiency of the overall cascaded H-bridge structure was measured experimentally to drop by 0.04-2.15% for transmission rates of digital data in the range of 60-1500 msec and a switching frequency value of f_c=40 kHz. This can be reduced further if either the value of f_c is reduced or high-frequency power devices are employed in the H-bridge circuits.

Experimental tests were conducted for a length of 0 to 30 meters of the power and data transmission cable that interconnects the cascaded H-bridge converter with the filter and load in Fig. 55 when using a NYAF HO5V-K 0.75mm^2 cable. The resulting number of bit errors of the data transmission and reception process was measured to be zero since any information loss was recovered by the CRC checksum embedded in the data packets as analyzed in § 4.3. Depending on the target specifications imposed in each application (e.g., type of interconnection cable, transmission distance, etc.), the impact of noise on the bit error rate can be evaluated using the circuit-level communication line models presented in [81] and [82].

4.5.2. 2nd stage of experiments (ASIC)

A number of arrangements and parametric designs have been tested apart from the ones that produced the experiments of the above arrangement via FPGA, all yielding very promising results. The final design of the Uplink system was also fabricated using the XFAB XH018 0.18μm mixed-signal CMOS technology. The chip has already been presented in Fig. 30, since it is the same chip which was tested in the experimental validation process of the MPPT system. So, similar to the MPPT design, the digital Uplink control unit has been built using the VHDL language, and the Cadence Virtuoso digital implementation software suite has been used for the synthesis of the final chip.

The manufactured chipset was proven to run flawlessly when overclocked up to 8 MHz, which increased the confidence for a smooth operation at 2 MHz. The time interval that is occupied by the transmission of the uplink data was further reduced in order to increase the safe margins between the receiving time window dedicated on the downlink and the transmitting time window dedicated on the uplink. The switching rate of the DC/AC bridge

MOSFETs was chosen to be reduced from 100 kHz to 40 kHz during data transmission, to ensure the emission of a clean signal that is can be produced by most of the industry's power MOSFETs and that the harmonics of the two frequencies used for the downlink channel (100 kHz and 66.6 kHz) will not coincide with the ones on the uplink channel. The modulation format was left unchanged, i.e. R-PAM but each symbol (chip) is now 550 μsec long (versus 1000) and occupies 550 / 25 μsec = 22 periods of the carrier signal. So, the full 51-bit bit-stream now has a duration of 28.05 msec. The fabricated PLC ASIC was designed according to the specifications presented in Table 4.2.

Table 4.2. Specifications of the fabricated ASIC prototype.

Parameter of the communication system	Symbol	Value
PDTRMs ID digital representation	$\boldsymbol{R_1}$	10 bits
PDTRM voltage resolution	$\boldsymbol{R_2}$	10 bits
PDTRM current resolution	$\boldsymbol{R_3}$	10 bits
Sampling rate of PDTRM array status	**S**	1 / min
Maximum number of PDTRMs in the array	**M**	1000
CRC polynomial length	**C**	21 bits
Carrier Frequency	$\mathbf{f_c}$	40 KHz
Number of periods per binary symbol (chip)	**i**	22

In order to verify the operability of the fabricated chip, the one of the two FPGA development boards of Fig. 63 was used to demodulate the information it will receive from the ASIC and to forward it (using two serial formats) to the remote user-interface. For that purpose, one of the signals S1 to S4 is directly connected to the receiver's back-end input. The two PRM sensory inputs of the MSTM are connected to two voltage-controlled oscillators (VCOs) to emulate the generation of voltage and current measurements by the DC source of the PDTRM (e.g. PV cell). The 'CLK' is supplied by an external generator, and the 'RST', 'Freq', 'Wake', 'Sync' inputs are controlled by a microcontroller board, which provides valuable low-frequency user feedback for debugging and demonstration purposes. Each symbol is divided into 22 periods of 25 μsec each. The symbol duration is 22 x 25 = 550 μsec, and the baud rate is 1818.2 bps. Since a data packet includes 51 bits of information, the packet duration is 51 x 550 = 28.05 msec.

Enlarged parts of the four H-Bridge driving signals (S1 to S4) are shown in the experimental waveforms depicted in Figs. 74 to 76. In Fig. 74, the falling event of the 'Sync' signal triggers twice the transmission of the MSTM telemetry data. The signals 'RST' and 'Wake' are fixed to logic 1, suggesting a disable state for both. The timing markers show that the packet to be transmitted requires approximately 28.05 msec.

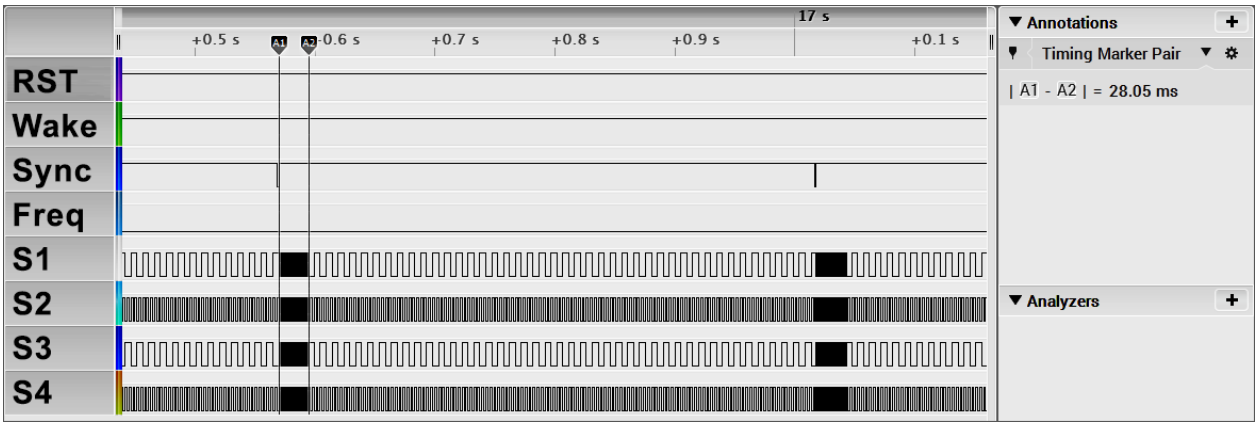


Fig. 74. Logic analyzer experimental waveforms: transmission of two 51-bit data packets, triggered by a 'Sync' falling-edge event.

Fig. 75 presents a zoomed snapshot of the area focused on the phase change of the information signal. The waveforms start by a 0 bit followed by a 1 bit, followed by two 0 bits, followed by a 1 bit, transmitting the symbols corresponding to the bit sequence '01001' i.e., the bits 40 to 44, also shown in Fig. 61. Fig. 76 reveals the full-bridge driving signals that produce the ID-specific power component in detail.

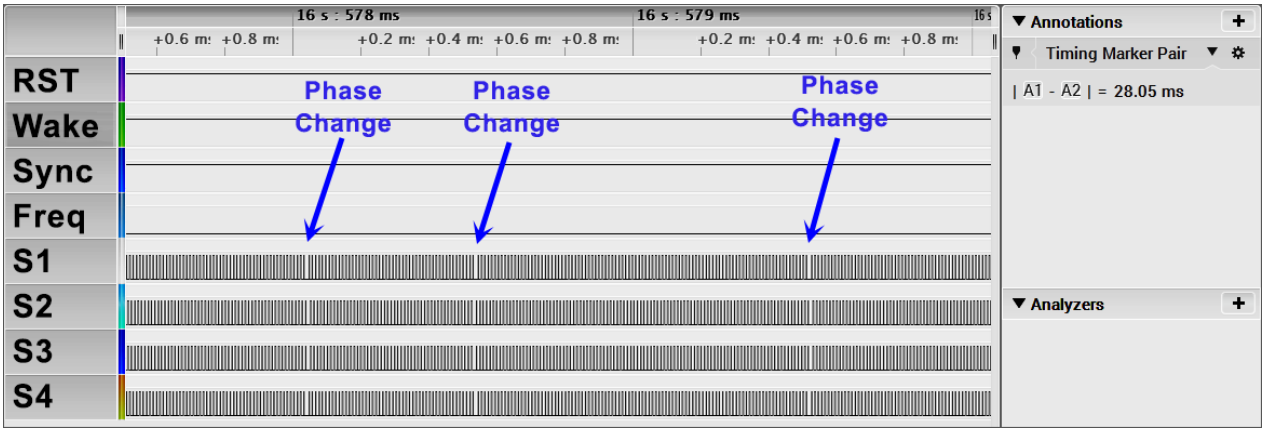


Fig. 75. Logic analyzer experimental waveforms depicting five symbols that correspond to bits '01001'.

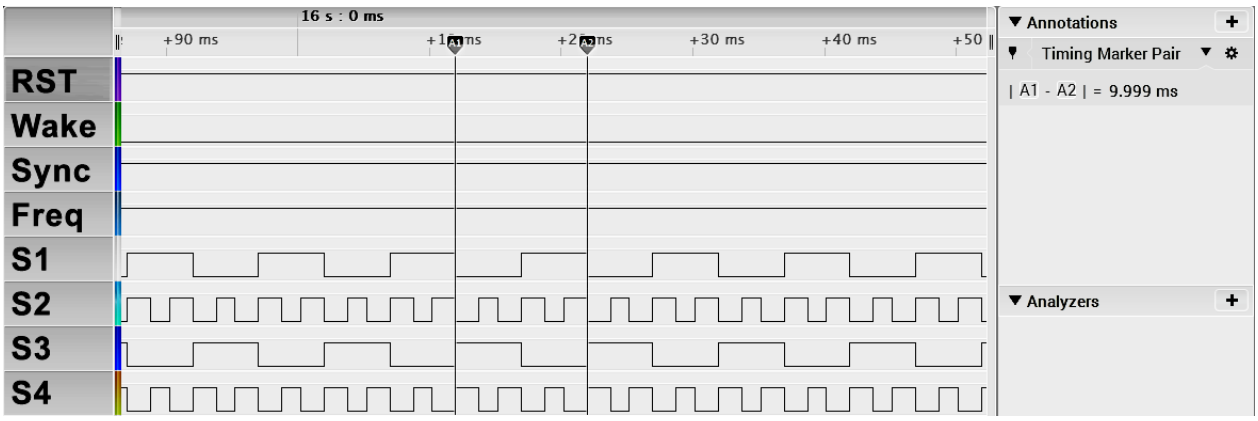
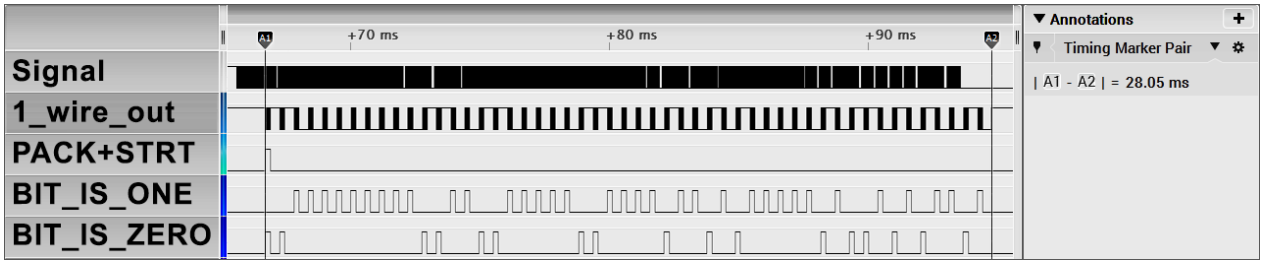
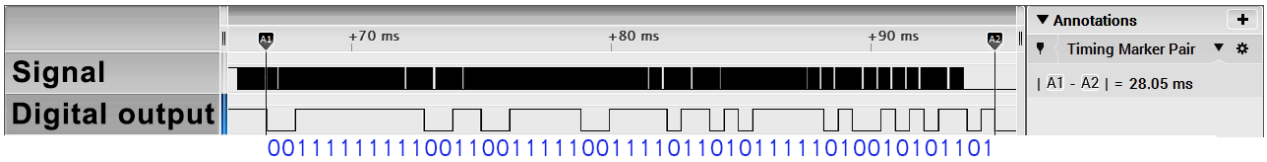


Fig. 76. Logic analyzer experimental waveforms: transmission of H-bridge driving signals to produce a component of the power signal of 50Hz with 60° degrees firing angle.



(a)



(b)

Fig. 77. (a) Logic analyzer experimental waveforms that reveal an enlarged part of the signals that the digital logic of the PLC receiver is demodulating, (b) the demodulated bitstream.

Fig. 77(a) depicts the logic analyzer experimental waveform of the bitstream that has been sent by the uplink transmitter (indicated as 'Signal') against the received data by the RMCU. The acquired bitstream 'Digital Output', shown in Fig. 77(b), changes logic states in the same order as the symbols shown in Fig. 61, simulated for the same VCO frequencies. Also, three extra experiments were conducted verifying that, for the given 21-bit CRC polynomial (i.e. 101100101011101010001) that is embedded in the fabricated ASIC, the received 20 last bits (checksum) have been identical to the anticipated ones, in all cases. Three indicative cases are the following;

- a preset (fixed) 30-bit vector that bypasses the chip measurements and sends a fixed vector instead (this is done by raising the 'SN_FX' pin shown in Fig. 5, to logic 1):

  Fixed Value: *00111 11111 01010 10101 00001 11101*

  CRC checksum: ***11110000011111000011***

- when both sensors are sensing no pulses:
  Sensing Zero: *11111 00000 00000 00000 00000 00000*
  CRC checksum: ***11101000000011100 1101***
- for a random sensing value:
  Sensing Random: *11111 00000 01000 00101 11100 00111*
  CRC checksum: ***00000111010110000000 1***

The result of the comparison between the bitstreams of Fig. 61 and Fig. 77(b) and the three verified CRC checksums confirm that the data have been successfully received and that the Uplink module operates as intended.

4.6. Considerations and research on the CHB converter THD with uplink PLC

4.6.1. Introduction

In this section, alternative control schemes are analyzed and compared for the simultaneous transmission of power and digital data through the power circuits of the modules synthesizing a single-phase cascaded H-bridge multilevel inverter, with the ultimate goal to reach a small THD footprint. So, the topic of this research pays special focus to the control schemes applied to the H-bridge driving circuits to produce a low THD without compromising the reliability of data communication. Various parametric simulation models are designed and tested using time-division multiplexing with two variations over the assignment technique for the PLC communication task. The results suggest that the low-bandwidth PLC design described in this PhD thesis is robust enough to provide the required communication fidelity and capable of successfully transmitting the mixed-signal (i.e., power and data) through the power cable under various operating conditions.

The researched control schemes are evaluated in terms of the resulting THD of the cascaded H-bridge converter output voltage as a function of the size of digital information transmitted and the number of the cascaded H-bridge converter modules. The comparison of the results can reveal valuable insights for realizing the most appropriate technique as a step toward efficient power delivery with minimal to no communication errors. This section of the PhD thesis focuses on the properties of the PDTRMs which are combined in a CHB Multi Level Inverter (CHB-MLI) (§ 4.6.3), raising considerations on the resulting THD of the cascaded H-bridge converter output voltage per case. The discussion analyses the implementation of

the various control schemes (§ 4.6.4) of the PDTRM blocks that comprise the CHB-MLI and presents its findings in numerous illustrative examples (§ 4.6.5).

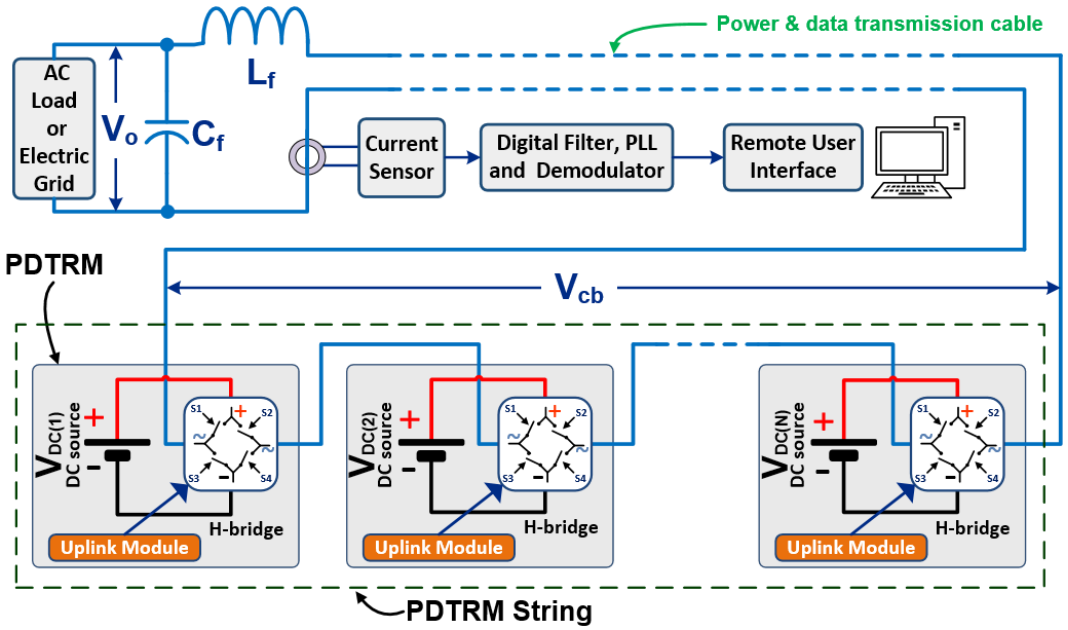


Fig. 78. Block diagram of the CHB-MLI structure for PLC.

4.6.2. Towards a low THD uplink PLC method for cascaded H-Bridge converters

The main electric element of the PLC system under study is presented in Fig. 78 as a block diagram that shows an array of mixed-signal (i.e., power and data) H-bridges (PTDRMs) that deliver AC power (to a load or the electric grid) and at the same time, they broadcast information to the Remote User-interface (RUI) of a terminal computer or Remote Monitoring and Control Unit (RMCU). The figure shows the PDTRMs (modules) connected in series to form the cascaded topology. The design can be asymmetric in principle [95], i.e., consisting of DC power sources of various voltages; however, here, it is assumed that each one of the PDTRMs includes a DC power source of voltage $V_{DC(i)}$, where i is the ID of the M modules in total. Thus, the pseudo-sinusoidal AC peak voltage equals $V_{cb}(pp) = V_{DC} \times M$. Each PDTRM includes a digital switch-control unit ('Uplink Module', Fig. 78) and an H-bridge structure. The 'Uplink Module' drives the terminal H-bridge by applying the proper switching patterns on S1 to S4.

Shared medium access and multiplexing

As analyzed in § 4.3, in this PLC scheme, at any given time instant, there is precisely one PDTRM dedicated to either producing an AC power component of the V_{cb} voltage or

generating digital pulses that will form binary symbols of data. Binding exactly one of the string's PDTRMs to the communication task is performed by applying a Time-Division Multiplexing (TDM) technique, where each PDTRM is allowed to transmit in specific preset timeslots according to the identification number (ID) that uniquely characterizes the specific module. So, if an array consists of M PDTRMs and T is the time period during which all of them are required to transmit their data, then, assuming an even timeslot distribution, each timeslot will occupy $T_S = T/M$ of time-space. In the simplest case, the n^{th} PDTRM is allowed to broadcast between t_1(n) and t_2(n) where $t_1(n) = (n\text{-}1) \times T_S$ and $t_2(n) = n \times T_S$. It occupies this time-space with data pulses rather than power pulses if and only if it is triggered to transmit. This process is executed for as long as required, given that the transmission duration does not exceed T_S. Subsequently, the available timeslot occupation can vary from 0 % to 100 % in the general case. In this work, the T_S was designed to occupy the time-space of exactly 3 periods of the AC current (f_0 = 50 Hz), so T_S is 60 msec.

Although all of the string's PDTRMs are identical and share the same transmission capabilities, it is assumed here that only one of them is allowed to broadcast information at any given time. However, this concept can be extended to include frequency-, polarization- or code-division multiplexing.

Format of the modulated signal extracted by the H-bridges

The distribution of the communicational task to each one of the PDTRMs, in various patterns of assignment (control schemes) provides the following benefits:

(i) helps to spread the effort of the high-frequency switching to all modules evenly,

(ii) enhances the transmission system's fault tolerance to electric stresses, since it avoids any single point of failure issues by enabling coverage extension and replication of vital information, and

(iii) allows shaping the resulting AC power signal in order to minimize the overall THD of the output signal. The latter can be achieved by controlling the succession of the IDs of the PDTRMs that are dedicated to transmit information.

The effects that the PLC assignment sequences have on the AC current generated as the summation of the AC components of the rest of the PDTRMs in terms of THD reduction is examined in the following paragraphs of this chapter.

Each PDTRM is broadcasting digital data by directly exploiting the module's integrated terminal full-bridge (H-bridge) power switch drivers. The H-bridge acts as the transmission interface to the common AC bus of the PDTRM string. Its signal formation is based on the digital pulses, which create the waveforms of either the AC power component or the data bitstream on the H-bridges' output. Due to the switching nature of the H-bridge, the expression of information is based on the R-PAM. The selected modulation is the BPSK technique, where the phase of the square-waved symbols (chips) takes exactly one of two values (i.e. phase 0° or 180°) depending on the desired bit to be transmitted (either 0 or 1, respectively).

This modulation was selected among various available digital modulations for the demonstration purposes of this work, and in principle, any of them can effectively be applied in this PLC design.

Table 4.3. Design Parameters of the Transmission Modulation.

Parameter	Symbol	Value
Carrier frequency	f_c	20 kHz
Number of periods per binary symbol	P	47

As shown in Table 4.3, the carrier frequency of the square pulse BPSK signal is f_c=20 kHz and forms bit-presenting symbols of P=47 periods each. The symbol's phase inversion is performed by negating the respective carrier generator according to the state of each bit of information that is next to transmission. The sensory data processor, the information data registers, the parallel to serial interface, the power component generator, the data signal generator, and the multiplexer that selects the driving signal among the two latter are all digital parts of the 'Uplink Module' depicted in Fig. 78.

The AC power component pulses are patterns expressed as a function of the PDTRM IDs. The current work uses two such functions; equation (4.22), described in § 4.6.4.A that implements a Nearest Level Control (NLC) method and the one derived by the Phase Disposition Sinusoidal Pulse Width Modulation (PD-SPWM) technique, where the level-shifting of the comparable triangular carrier is a direct function of the PDTRM's ID [96]. The same is true for the calculations of the available timeslots, as shown in § 4.6.4.B where t_1(n) and t_2(n) (i.e., the limits of the available timeslot) are a function of the PDTRM's ID.

4.6.3. The uplink PLC control schemes under investigation

This work includes two main PLC assignment sequences (i.e., two disposition variations) of the communication task over the PDTRMs, as shown by the top and bottom charts in Fig. 79, which is an enrichment of the diagram shown in Fig. 65.

1st assignment sequence (for the control schemes A and D)

Timeslot #	1	2	3	4	...	M-1	M	1	2	...
PTDRM 1	**DTr 1**	Cmp A	Cmp A	Cmp A	...	Cmp A	Cmp A	**DTr 1**	Cmp A	...
PTDRM 2	Cmp B	**DTr 2**	Cmp B	Cmp B	...	Cmp B	Cmp B	Cmp B	**DTr 2**	...
PTDRM 3	Cmp C	Cmp C	**DTr 3**	Cmp C	...	Cmp C	Cmp C	Cmp C	Cmp C	...
PTDRM 4	Cmp D	Cmp D	Cmp D	**DTr 4**	...	Cmp D	Cmp D	Cmp D	Cmp D	...
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
PTDRM M-1	Cmp M-1	Cmp M-1	Cmp M-1	Cmp M-1	...	**DTr M-1**	Cmp M	Cmp M-1	Cmp M-1	...
PTDRM M	Cmp M	Cmp M	Cmp M	Cmp M	...	Cmp M	**DTr M**	Cmp M	Cmp M	...

2nd assignment sequence (for the control schemes B and C)

Timeslot #	1	2	3	4	...	M-1	M	1	2	...
PTDRM 1	**DTr 1**	Cmp B	Cmp B	Cmp B	...	Cmp B	Cmp B	**DTr 1**	Cmp B	...
PTDRM 2	Cmp B	**DTr 2**	Cmp C	Cmp C	...	Cmp C	Cmp C	Cmp B	**DTr 2**	...
PTDRM 3	Cmp C	Cmp C	**DTr 3**	Cmp D	...	Cmp D	Cmp D	Cmp C	Cmp C	...
PTDRM 4	Cmp D	Cmp D	Cmp D	**DTr 4**	...	Cmp M-1	Cmp M-1	Cmp D	Cmp D	...
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
PTDRM M-1	Cmp M-1	Cmp M-1	Cmp M-1	Cmp M-1	...	**DTr M-1**	Cmp M	Cmp M-1	Cmp M-1	...
PTDRM M	Cmp M	Cmp M	Cmp M	Cmp M	...	Cmp M	**DTr M**	Cmp M	Cmp M	...

"Cmp 1" to "Cmp M" refer to the AC power vector component X, where X is 1 to M
"DTr 1" to "DTr M" stand for 'Data transmission of the PTDRM X', where X is 1 to M

Fig. 79. An example of the communication assignment schemes (A, D and B, C) applied on the CHB-MLI PDTRMs during M+2 sequential timeslots.

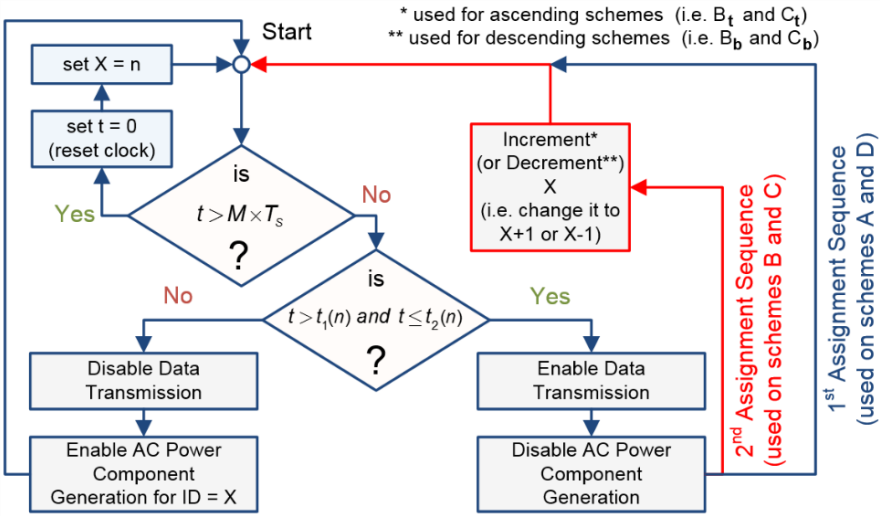


Fig. 80. Flowchart of the 1st and 2nd assignment sequences.

The two wireframe charts are horizontally split evenly in M+2 timeslots and vertically split into the AC power components ('Cmp A' to 'Cmp M') of the overall AC attributed to each one of the M modules in total. Each of the PDTRMs executes one of the two algorithms presented in the flowchart of Fig. 80.

These algorithms are embedded in the control logic of the 'Uplink Module' of every PDTRM. The difference of the 2nd PLC sequence over the 1st is the added manipulation of the internal register X, which changes right after t_2(n) (which marks the end of the data transmission availability timeslot of the respective PDTRM) forcing the PDTRM to behave as if its ID value was the one of the next (or the previous) PDTRM in line. This new ID assignment makes the PDTRM to generate the next (or previous) AC power component, as shown in the bottom chart of Fig. 79.

The 1st of the PLC assignment sequences suggests that the IDs of the PDTRMs that transmit information will comply with a succession (either ascending or descending), following the respective timeslot numbering (ascending in the bottom chart of Fig. 79), ensuring that the PDTRM transmission succession is similar to the succession of their power generation components. However, this leads to the replacement of a particular AC power component (e.g., 'Cmp A') at any given time by data transmission pulses (e.g., 'DTr 1') since the respective PDTRM (e.g., 'PDTRM 1') is dedicating its power switching patterns to the digital data transmission rather than power generation. This AC component omission is different for every one of the M timeslots, reflecting a deviation from the anticipated AC voltage V_{cb} and subsequently the LC-filtered output voltage V_0 applied to the load (Fig. 79).

A. Control scheme based on ID rotation and NLC

In this control scheme (i.e., 'control scheme A'), the value of d(n), which is the time that the output of H-bridge of module n needs to produce an output voltage of 0 V, is calculated as follows:

$$d(n) = floor\left(arcsin\left(\frac{n+1}{M}\right) \times \frac{f}{2 \times \pi \times f_0}\right),\ \forall\ n \geq 0,\ n \in N$$

$$delay(n) = (d(n-1) + d(n))\ /\ 2,\quad \forall\ n > 0,\ n \in N \tag{4.22}$$

where $n \leq$ M-1 is the number of the PDTRM ID, f is the digital system's clock frequency (here 1 MHz), and delay(n) is the time (in the range of 0-π/2 rads) that the H-bridge of the nth PDTRM needs to output zero voltage while in all other cases it outputs V_{DC} which is the voltage of the DC power source included in each PDTRM. If the PDTRMs directly applied the d(n) calculation

then the resulting pseudo-sinusoidal signal would be contained inside the reference sinusoidal signal that it approaches (for significant numbers of M). The calculation of delay(n) creates a simple compensational correction that reduces the NLC deviation from the reference sinusoidal signal resulting in a fast and adequate approximation.

The graphical expression of delay(n), which can be regarded as a 'firing angle' setting, is shown in Fig. 81 for the case of M = 5. It presents the reconstruction of an 11-level AC power signal (created by 5 PDTRMs), where one of the modules is responsible for the creation of the superimposed digital data signal. Due to the symmetry that every quarter of a pseudo-sinusoidal signal possesses against the π/2 axis and the y (voltage) axis, the calculated d(n) for all n are adequate for rendering all n periodic square waveforms.

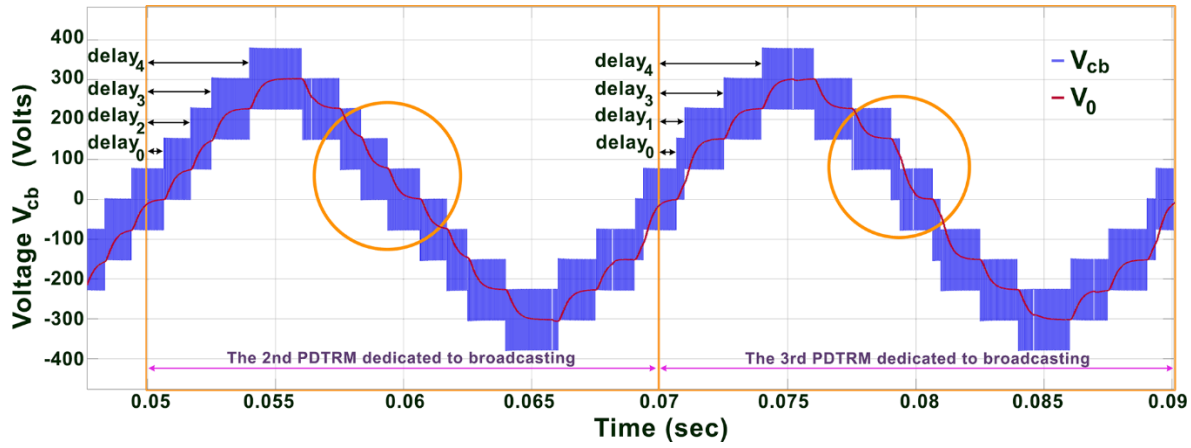


Fig. 81. Control Scheme A: voltage V_{cb} superimposed with data and V_0 after the data filtering (uses ID rotation and NLC).

This control scheme results in the omission of an AC component in every timeslot, here the 2nd AC power component in the generation of the left pseudo-sinusoidal period, and the 3rd AC power component in the generation of the correct pseudo-sinusoidal period. The respective effect on the load-side voltage V_0, for the case of Fig. 81, is pointed by comparing the content of the two circles in that figure. Another distortion exists a few milliseconds later (at 0.0825 sec compared to 0.0625 sec). Also, distortions exist in the symmetrical points of those mentioned (i.e., when voltage level is similar but increases).

B. Control scheme based on ID rotation with power component substitution and NLC

In control scheme B, the PLC assignment sequence avoids periodic deformation issues by ensuring that the AC vector component to be replaced (by the data transmission) at any given time is the same. The PDTRMs follow a round-robin transmission policy similar to the

one previously described (either ascending or descending). However, in this scheme the PDTRM with ID=X is forced to change its power generation pattern to the next in line (either X+1 or X-1) as soon as its transmission is complete. The PDTRM keeps this new setup of operation (acting as the 'X+1' module, for the case shown in the bottom chart of Fig. 79) up until the restart of the sequence, which occurs after M timeslots. This guarantees that all M-1 PDTRMs produce the same AC power signal at all times.

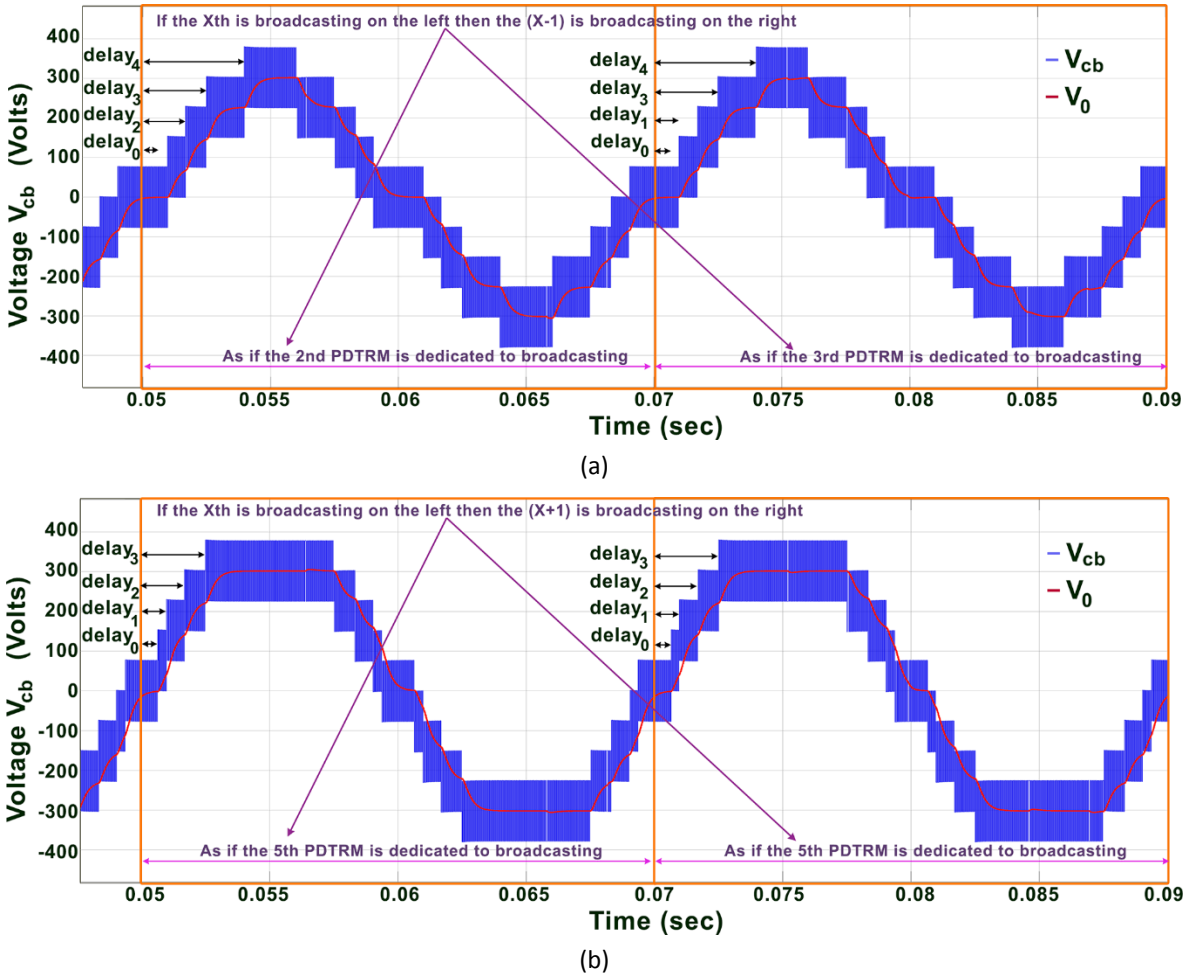


Fig. 82. Control Scheme B - voltage V_{cb} superimposed with data and V_0 after the data filtering for: (a) an ascending sequence and (b) a descending sequence (uses ID rotation with power component substitution and NLC).

The result of this added rule is presented in the examples of Fig. 82. The difference between the two cases is that the ascending sequence results in the omission of the base power component ('Cmp A', which is missing from the bottom chart of Fig. 79). The descending sequence results in the omission of the top power component. The cases where the bitstream length does not cover the entirety of the available timeslots are examined (for each one of the control schemes) in § 4.6.5.

C. Control scheme based on ID rotation with power component substitution and PD-SPWM

The two control schemes (B and C) are the realizations of the 2nd PLC assignment sequence. This control scheme differs from B, because the AC power generation components are created according to the PD-SPWM technique rather than NLC. The control scheme C has been introduced in this point to examine if it can drastically reduce the THD as anticipated by its performance in conventional single-phase CHB-MLI multi-carrier topologies [97]. The result of this concept for the case of M=5 is presented in Fig. 83.

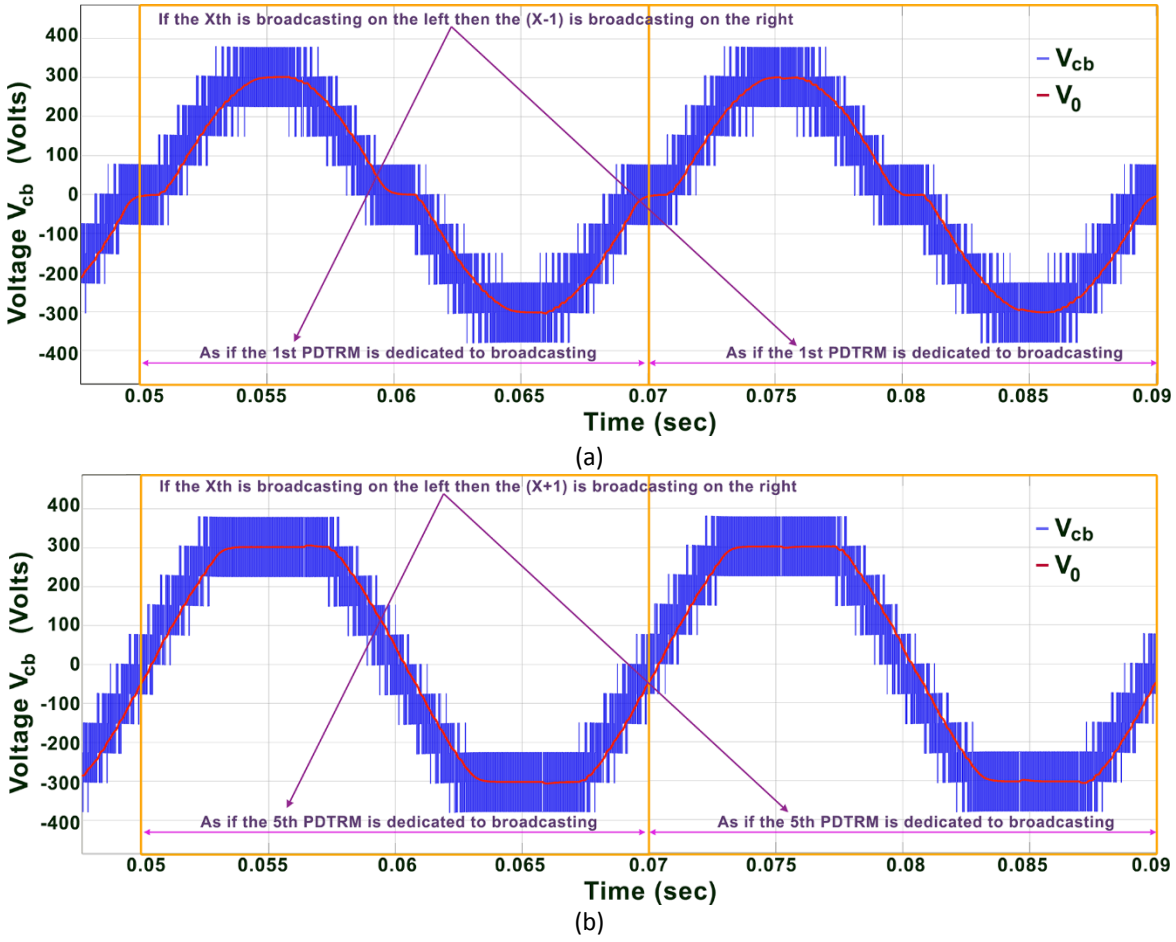


Fig. 83. Control Scheme C - voltage V_{cb} superimposed with data and V_0 after the data filtering for: (a) an ascending sequence and (b) a descending sequence (uses ID rotation with power component substitution and PD-SPWM).

This one presents smoother transitions when visually compared to Control Scheme B, as anticipated.

D. Control scheme D based on ID rotation and PD-SPWM

Control Scheme D is the second realization of the 1st PLC assignment sequence (the first one was in Control Scheme A). Its difference from Control Scheme A is similar to the

difference of Control Scheme C in respect to B, i.e., the introduction of the PD-SPWM technique. The result is the smoothening of the step transitions in the presence of the wave distortions (similar to the ones presented in Fig. 81), as shown in Fig. 84. However, any conclusive remarks will be safely obtained after the quantitative THD analysis in § 4.6.5.

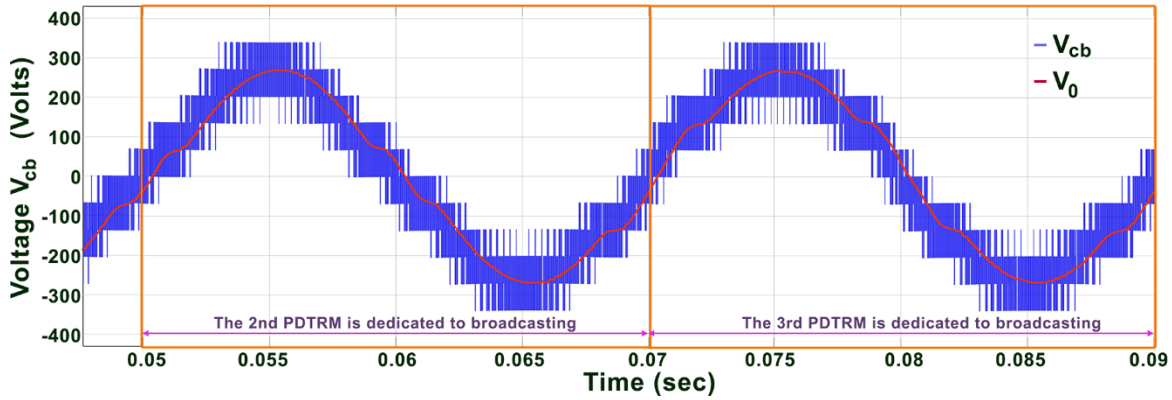


Fig. 84. Control Scheme D: voltage V_{cb} superimposed with data and V_0 after the data filtering (uses ID rotation and PD-SPWM).

4.6.4. Simulation results

The impact of the alternative control schemes presented in § 4.6.4 on the CHB-MLI output voltage THD was evaluated. The described PLC design was modeled in MATLAB Simulink R2018a with the SimScape plug-in. The electric characteristics of the elements used (common to all models) are shown in Table 4.4.

Table 4.4. Specifications of the CHB-MLI.

Electrical Parameter of the System	Symbol	Value
Frequency of the AC current	f_0	50 Hz
Frequency of the SPWM carrier	f_{SPWM}	4 kHz
Voltage (RMS) across the load	V_0	230 V
Output filter inductance	L_f	15 mH
Output filter capacitance	C_f	2 μF
Electrical load resistance	R_L	40 Ω

The power switches of the H-bridges comprised power MOSFETs with an ON-resistance R_{ON}= 100 mΩ. All four control schemes (A, B, C, and D) were simulated using the parameters of Table 4.5.

Table 4.5. Design Parameters of the PLC Interface.

Parameter	Symbol	Values
PDTRMs number	M	5, 10, 15 or 20
Bitstream length	B_l	Steps of 20%
Control scheme	C_S	A, B_t, B_b, C_t, C_b, D

In all cases, the data to be transmitted were successfully received, requiring no post-processing for recovering any lost information. The receiver's design was based on a Finite-Impulse Response (FIR) high-pass filter with a stopband edge frequency at 8 kHz, a passband edge frequency at 12 kHz, and a stopband attenuation at 18 dB, followed by a Schmitt trigger comparator for level shifting.

The quality of the received information is depicted in Fig. 85 (as the bottom symbol-stream). It can be seen that it is identical to the transmitted information (the top symbol-stream), with a minor transfer delay. This indicates that a lower stopband attenuation or a higher bandwidth communication is possible if required. The arrows pinpoint the carrier phase changes, which suggest the swapping of the binary information logic level. The arrows were also added as they facilitate to visually compare the two symbol streams. At the top of the figure lays the actual transformation of each symbol to the respective binary value of the information.

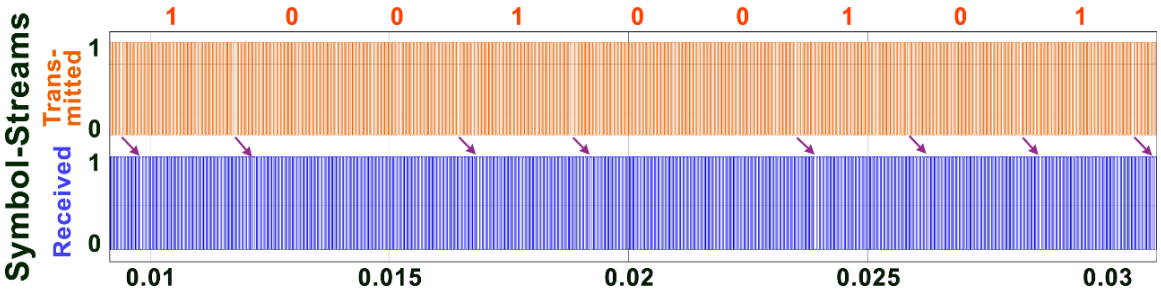
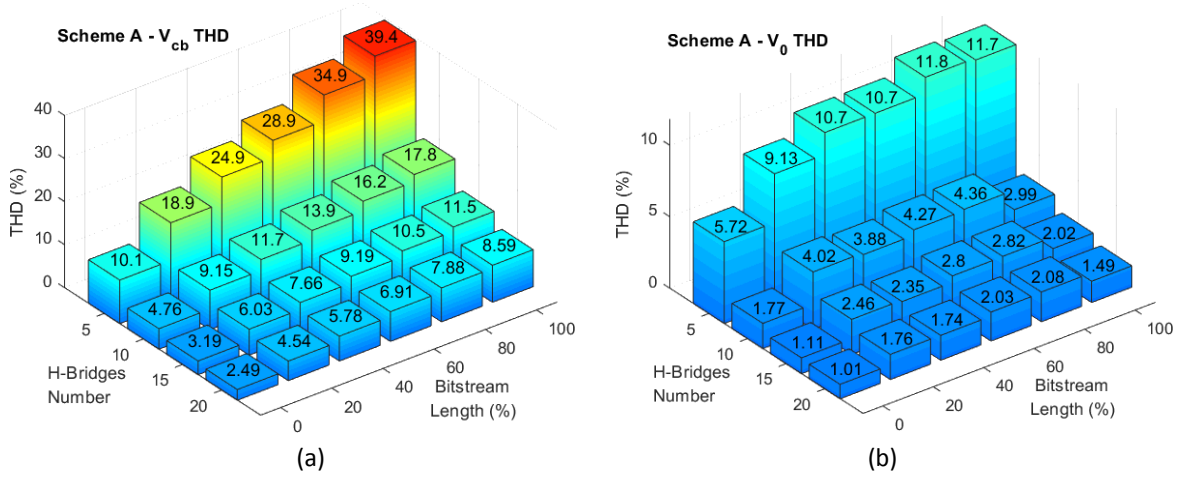


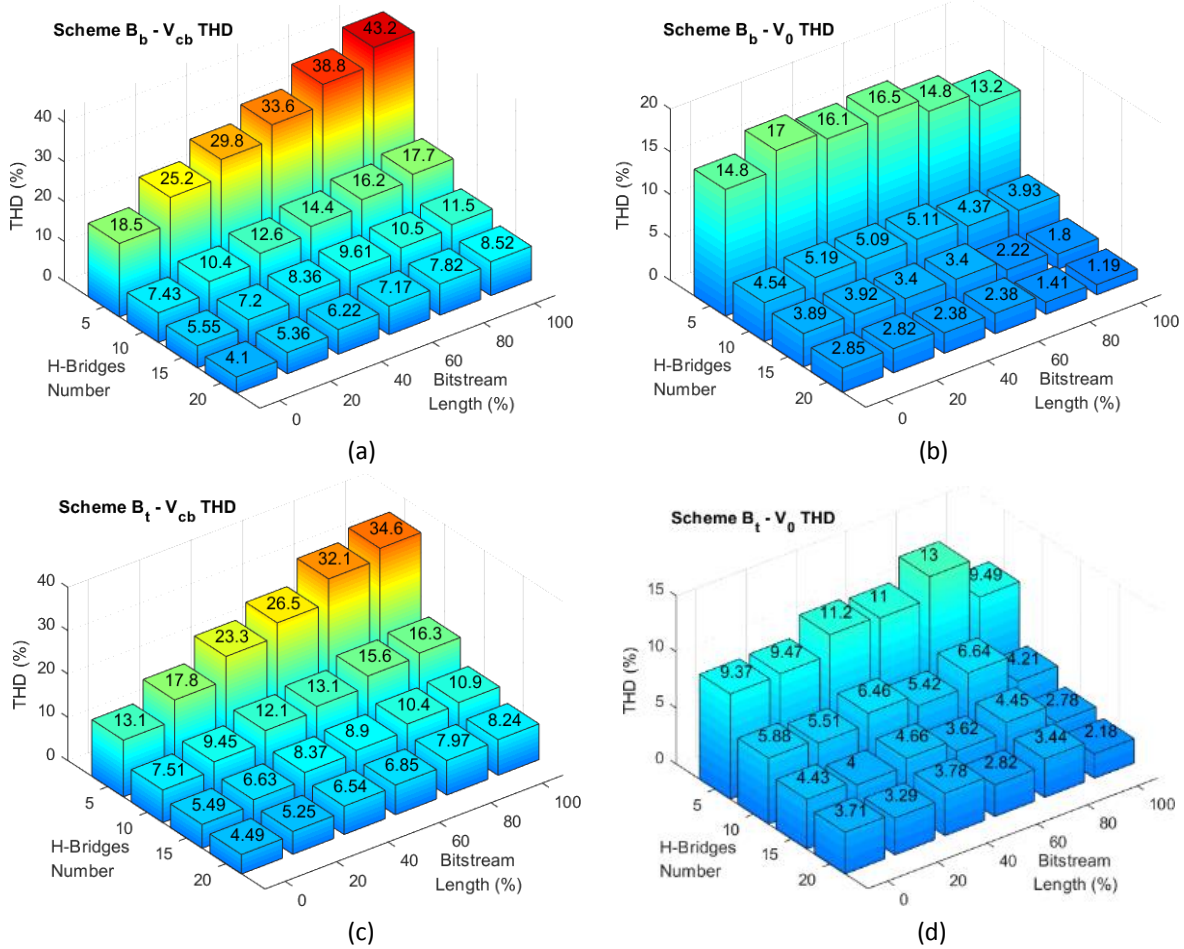
Fig. 85. Comparison of the transmitted and received symbol bitstreams.

The case to be depicted in Fig. 85 was chosen from the simulations of 'Control Scheme C' as it utilizes PD-SPWM switching, which poses an extra challenge to the PLC channel. Figs. 86 to 89 present the calculated THD for both V_{cb} and V_0, per scenario.



(a) (b)

Fig. 86. Control Scheme A simulation results - THD vs. bitstream length and H-bridges number of the 1st assignment sequence for: (a) V_{cb} and (b) V_0.



(a) (b)

(c) (d)

Fig. 87. Control Scheme B simulation results - THD vs. bitstream length and H-bridges number of the 2nd assignment sequence for: (a),(c) V_{cb} and (b),(d) V_0 with (a),(b) ascending and (c),(d) descending succession.

Parameter M shows the number of PDTRMs in series. Parameter B_l shows the information coverage percentage of the timeslots (bitstream length %). The two assignment

sequences (1st and 2nd) are the two PLC techniques used to disposition the data transmission task from one PDTRM to another in time steps of T_S. In all cases, the THD was higher for the V_{cb} in respect to V_0, which is a result to be expected due to the filtering of the data that exist in a frequency much higher than the fundamental (f_0).

Similarly, for the control schemes B and C, which are both based on the 2nd assignment sequence, the THD values of the descending schemes (i.e., B_t and C_t) are -in general- smaller than the ones of the ascending schemes (i.e., B_b and C_b). This is because the bottom AC power component holds a higher percentage of power at the fundamental frequency than the top one. A demonstration of this effect is shown in Figs. 87 and 88, where the bottom charts have lower values and subsequently a favored THD over the respective ones on the top.

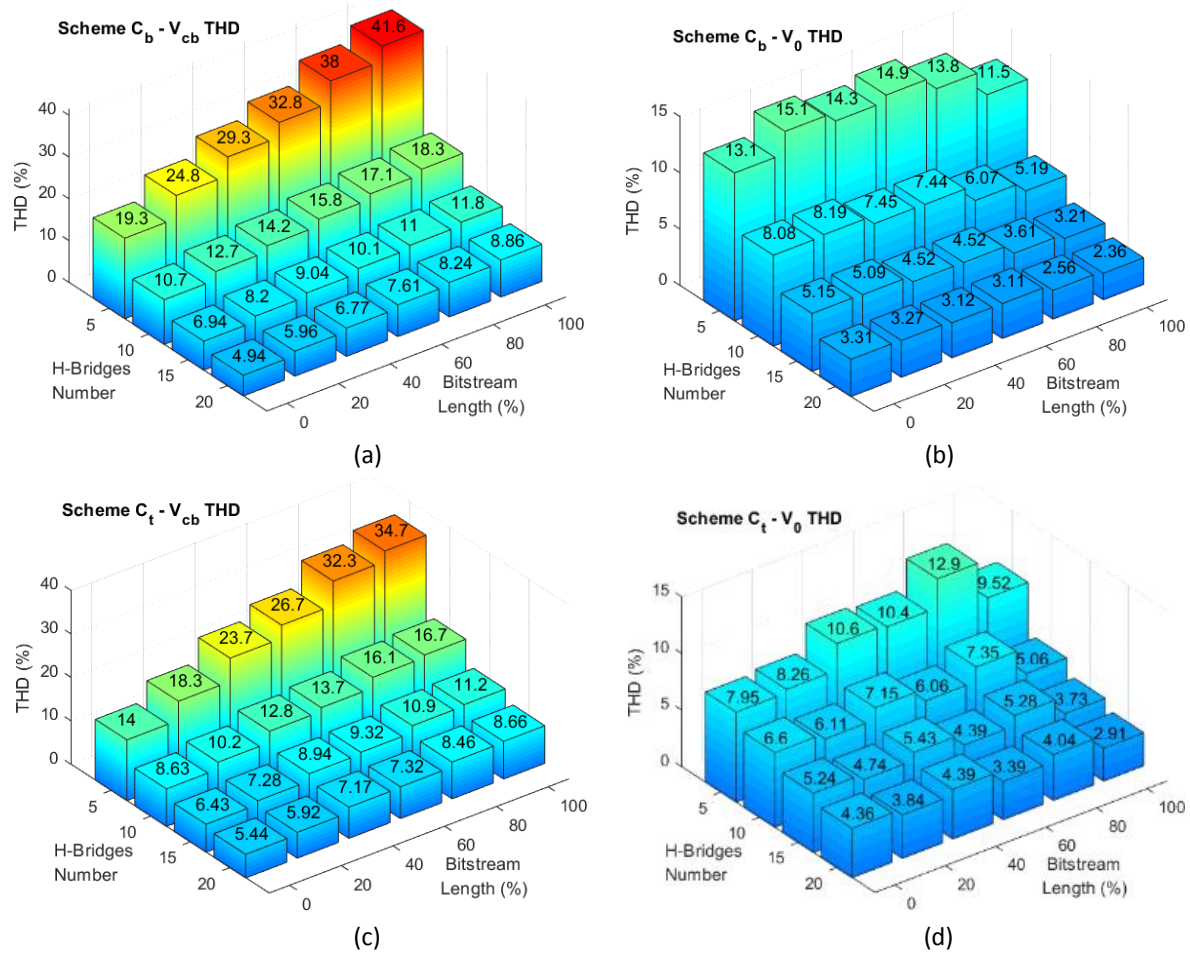


Fig. 88. Control Scheme C simulation results - THD vs. bitstream length and H-bridges number of the 2nd assignment sequence over a PD-SPWM for: (a),(c) V_{cb} and (b),(d) V_0 with (a),(b) ascending and (c),(d) descending succession.

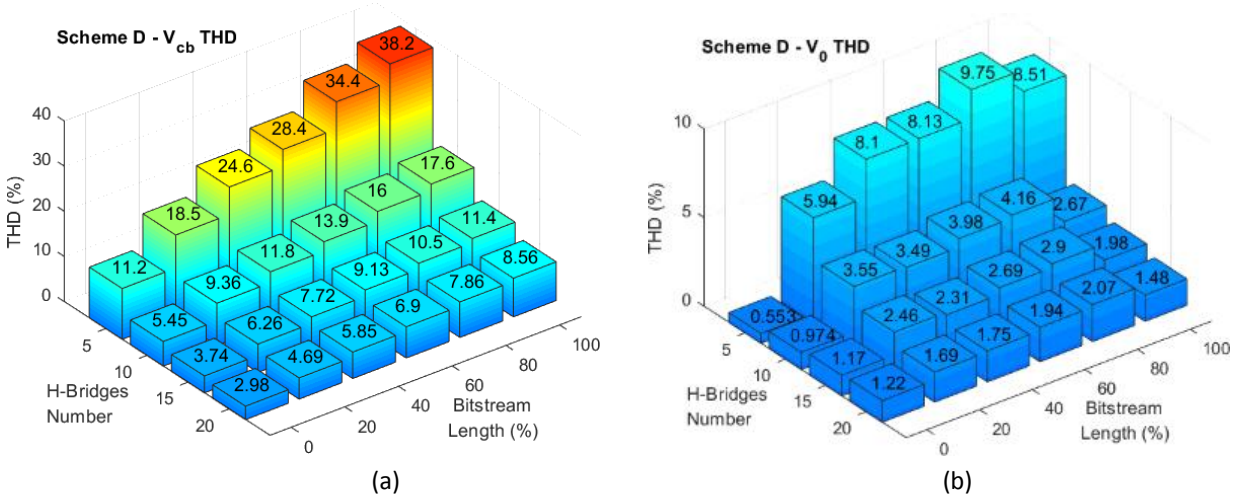


Fig. 89. Control Scheme D simulation results - THD vs. bitstream length and H-bridges number of the 1st assignment sequence over a PD-SPWM for: (a) V_{cb} and (b) V_0.

Regarding the control schemes A and D, which are both based on the 1st assignment sequence, D outperforms A in many cases, which is expected, as it benefits from the PD-SPWM technique. The exception is located in the corner of a high number of H-bridges (M=15, M=20) when no information is broadcasted. This is because the harmonic at f_{SPWM}, in this case, holds a decent percentage of high-frequency power, in all AC modules. In contrast, control scheme A holds a lesser amount as the scenario does not require broadcasting high-frequency information. Comparing control schemes B and C, which differ only in the fact that scheme C uses the PD-SPWM technique, scheme C is marginally better for the cases that M=5, i.e., a small number of modules, and worse in all other cases. Also, scheme C is worse when compared to all other control schemes for M>5. This demonstrates that the induced PD-SPWM switching that spans across all modules' operation is outperformed by the power quality improvement that a higher number of modules can offer in NLC.

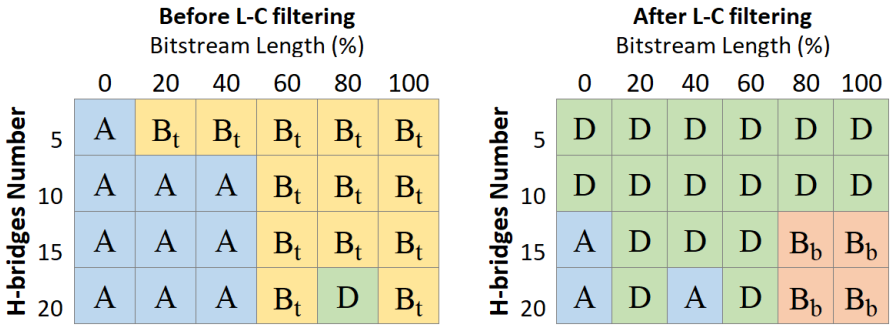


Fig. 90. Presentation of the best control schemes per case.

A detailed view of the applicability of the control schemes concerning the existence of an L-C filter, the bitstream length, and the H-bridge number available is presented in Fig. 90.

Control scheme D offers a THD of V_0, which is less than 4.2 % and covers the power quality requirements of various applications. In case an L-C filter is not used, then the next best choice is the control scheme B using descending succession. When the information load is relatively small (e.g. bitstream length < 60 %) a generally safe choice is Control Scheme A.

5. Downlink PLC for the control of distributed PCUs

5.1. Introduction

The PLC technologies enable the point-to-point linking between distributed power production and consumption units, thus overlaying enhanced monitoring and control capabilities to the overall power system.

A novel PLC method primarily focusing on CHB converters is presented in this chapter, which enables the transmission of digital data by a remote terminal computer to the individual power modules synthesizing a cascaded H-bridge power converter through their power circuits and the power cable that is also used to simultaneously transmit power. In such a case, the individual power modules of the cascaded H-bridge converter may also comprise PV cells or arrays as DC energy sources.

The basic principle can serve the general case where the PLC method is applied to any distributed network of power sources, as long as this network is electrically valid, similarly to the design that has been presented in Figs. 3 and 5. This method can enable the reception of the data broadcasted by the RMCU shown in Figs. 3 and 5 and allow for the parameterization of their power generation operation.

The downlink PLC method developed in this PhD thesis comprises an integrated framework of a digital data transmitter, receiver, and communication protocol, without using additional coupling circuits or power amplifiers and independently from the implementation scale and the type of the power-supplied load. Its operation has been tested using an experimental prototype consisting of a two-module cascaded H-bridge inverter and an FPGA device hosting the digital transmitter and receiver units.

The experimental results verify the successful transmission of digital parameterization commands from a central terminal computer to the individual power modules of the cascaded H-bridge converter, along with the simultaneous transmission of AC power to the load over the common power cable.

5.2. Prior art review

In recent years, there has been an increase in interest in the simultaneous transmission of power and information via PLC systems. These technologies target applications in smart grids, the Internet of Things (IoT), and electric cars [98-100] because they reduce the complexity and expense of total communication system deployment.

The conventional method of implementing PLC schemes utilizing the power converter circuit introduces low-cost transmission options by manipulating the DC/DC converter's control loop [65], [101]. The selection of simple modulation techniques, such as two-state PSK and FSK, respectively, the use of a sinusoidal carrier in [65], the inclusion of an isolating line impedance stabilization network in [101], and the absence of encoding in both of these studies enable the development of low-cost demodulation receivers. Therefore, [65] utilizes a down-conversion receiver, while [101] uses a DSP with discrete Fourier transformation (DFT) and an A/D conversion unit. Similarly, in [102], the DC/DC converters broadcast data using binary FSK (BFSK), and the reception is achieved using an analog band-pass filter (BPF), an envelope detector, and a hysteresis comparator, plus an inductive sensor circuit.

The authors of [60] suggest a controller area network (CAN) protocol implementation in which binary data are transferred by varying the impedance that a modem provides on a DC-bus connecting the DC/DC converters' loads. A circuit for detecting envelopes demodulates the sent data. The research presented in [66] focuses on controlling power flow and load sharing data, although this method is constrained by power range and communication dependability. Similar constraints on the type of the load and the power supply are imposed on the works [61], [62], and [69], where the emphasis is placed on switched-reluctance for motors [64] and generators [62], [69]. Using PSK on full-bridge inverters, [103] improves the operational dependability of DC microgrids. For demodulation, the units that function as receivers use a sliding DFT method. The control of distributed DC/DC power converters in [76] is implemented using BFSK modulation and demodulation is accomplished with a digital correlation receiver. BFSK modulation is also used in [77] for DC/DC converters in microgrids, with a DFT method used for demodulation. For the transmission and receiving of ASK-modulated signals, the PV monitoring system described in [63] employs parallel resonant coupling circuits. In [104], where an M-ary ASK approach is employed for microgrid frequency control, coupling circuits are required. In [79], frequency hopping–differential PSK is implemented for parallel DC/DC converters such that the transmitted data are modulated

into the phase of the PWM control signal. The receiver comprises a DSP and an ADC for digital data output. In order to eliminate switching harmonics, [78] implements a direct-sequence spread spectrum modulation with a m-sequence and PSK in the PWM control signal of the DC/DC converter. A DSP circuit does the DFT computations to get a phase representing the transmitted binary information during demodulation.

All of the above-mentioned literature on PLC implementation through the power circuit has concentrated on DC-bus linkages and/or the exploitation of the operating principles of DC/DC power converters. Concerning DC/AC power converters, [80], [81], and [82] address the PLC implementation in series connections of DC/AC power converters, such as AC-stacked inverters and cascaded H-bridge converters. However, the works of [81] and [82] transmit basic synchronization pulses as opposed to actual digital data. In addition, as indicated in [80], attaining a high bit rate necessitates sophisticated signal processing, which puts a simpler receiver decoder and protocol management as significant issues requiring more study.

In addition, none of these studies have examined the transmission of digital data from a remote-control station to individual DC/AC power converters via the same power connection used to carry electricity from the power converter to the load or the electric grid. Nonetheless, this feature is essential for cascaded H-bridge converters used in distributed PV and energy storage systems, Static Synchronous Compensators (STATCOMs) for grid voltage regulation, etc. [105-107], as it enables parameterization and control of the operation of the individual power modules of the cascaded H-bridge structure for energy management purposes.

This chapter describes a novel PLC method that, in contrast to the prior art described above, enables the transmission of digital data from a remote terminal computer to the individual power modules that synthesize a cascaded H-bridge power converter via their power circuits and the power cable that is also used to transmit power simultaneously. The suggested PLC approach has the following advantages: (i) it does not need extra coupling circuits or power amplifiers for PLC implementation, and (ii) it may be used to cascaded H-bridge converters regardless of the size of implementation or kind of power-supplied load.

This approach consists of an integrated framework comprising a digital data transmitter, receiver, and communication protocol, all of which are depicted as a scalable multi-layer architecture. The experimental findings demonstrate that the designed PLC system works well.

The following section (§ 5.3) describes the PLC method and the digital circuit-level designs of the data transmitter and receiver. The experimental prototype and results are presented in section § 5.4.

5.3. The developed downlink PLC method

In accordance to the general diagram presented in the beginning of every chapter of this PhD thesis, Fig. 91 highlights the position of the system to be described in the following sections, focusing solely on the Downlink transmitting and receiving units.

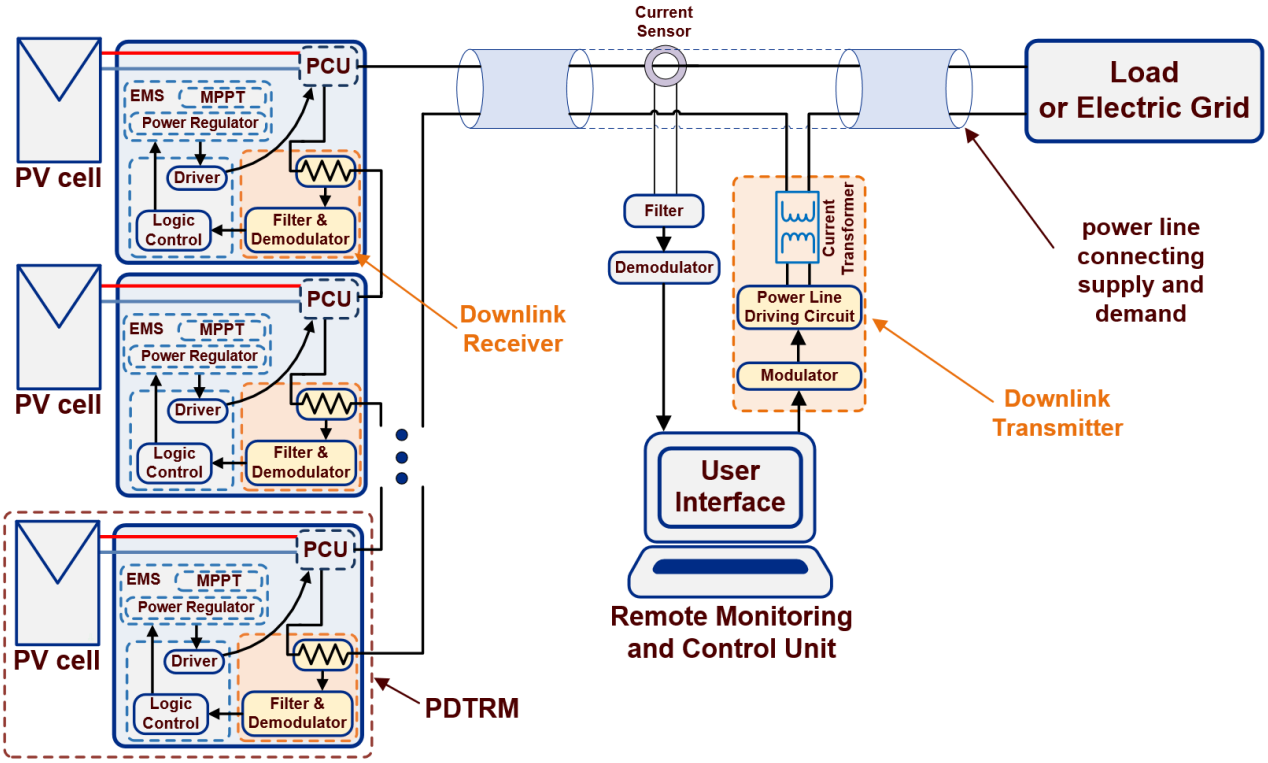


Fig. 91: General diagram of the PV system investigated in this PhD thesis presenting the Downlink PLC units.

5.3.1. Presentation of the downlink PLC design principles

A block diagram of the power system under consideration for developing the proposed downlink PLC method is shown in Fig. 92. The cascaded H-bridge converter comprises multiple DC power sources, V_i, each connected to an H-bridge that is controlled by a digital control unit, thus forming the elementary building blocks of the power system, indicated as RPDTRMs.

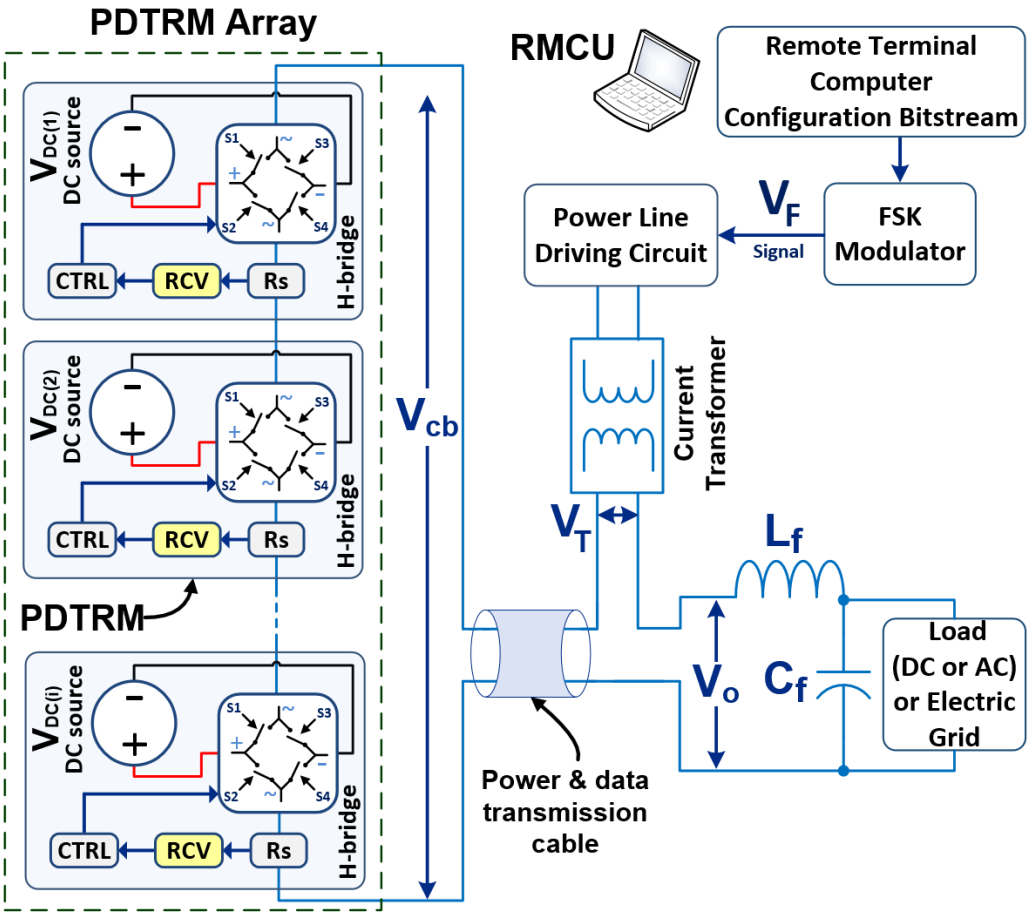


Fig. 92. Block diagram of the downlink PLC scheme under study for simultaneous generation of power and reception of digital data by the PDTRMs of a cascaded H-bridge converter.

The target of the downlink PLC method developed in this PhD thesis is to transmit digital data from the RMCU to the individual PDTRMs of the cascaded H-bridge converter through the same power cable that interconnects the cascaded H-bridge power converter with the electric load or electric grid for power transmission purposes. In order to produce power and simultaneously receive digital data, each PDTRM controls the H-bridge power switches by a digital control unit (CTRL in Fig. 92) which operates according to the commands it acquires from the digital data receiver unit of the PDTRM (i.e. RCV in Fig. 92).

The RCV detects the digital data supplied by the RMCU (shown above as the "Remote Terminal Computer" or RTC) by detecting the current ripple going via a current sensing resistor, R_S, connected in series to one of the H-bridge output terminals of each PDTRM (alternatively, a current transformer or a Hall-effect current sensor can also be used for that purpose). The receiver circuit of each PDTRM is provided with a digital identity (ID) vector that distinguishes it from other PDTRMs when information broadcast by the RTC refers to it. This ID is given through a hardwired external link in each PDTRM.

On the opposite end of the communication connection, as illustrated in Fig. 92, the RTC transmits the configuration bitstream to an FSK modulator unit (i.e., parameterization commands to control the operation of the PDTRMs as desired). The modulator's output is then sent as a square signal via a power line driving circuit linked to the power line by a current transformer. The sent data flow to the PDTRMs through the power wire connecting the PDTRM string to the (DC or AC) load or electrical grid.

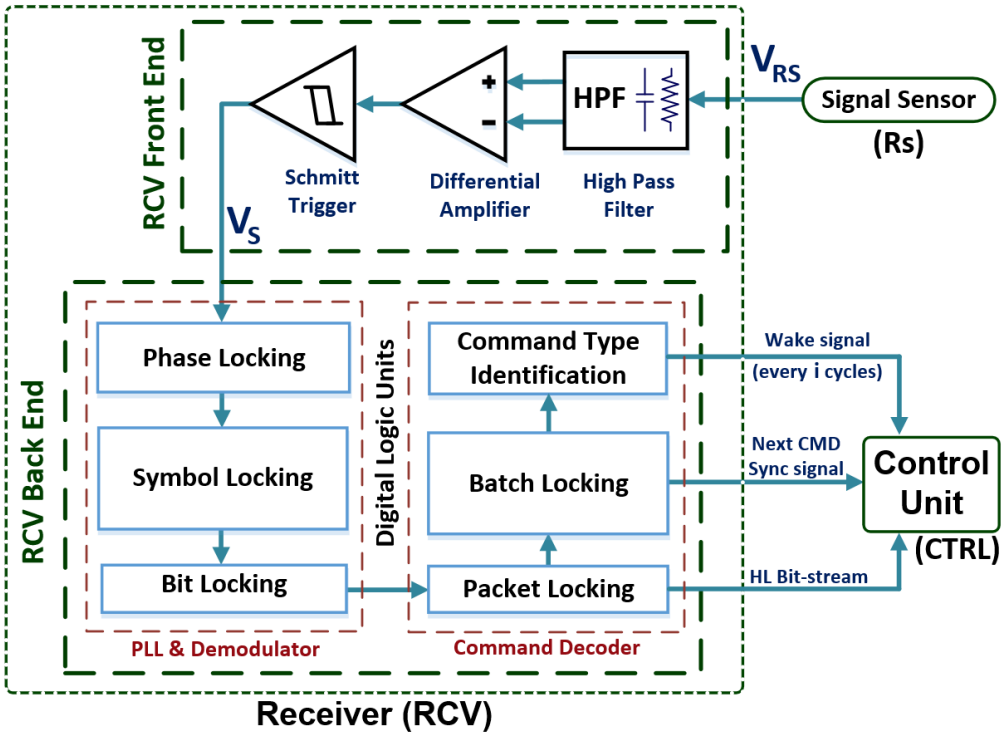


Fig. 93. Block diagram of the receiver unit in each PDTRM of the CHB converter.

Fig. 93 depicts a block schematic of the data receiver (RCV) in each PDTRM. The receiver front-end is responsible for filtering, amplifying, and digitizing the voltage created across the sensing resistor R_S, which is proportional to the current flowing through the PDTRM H-bridge. The back-end consists of two major components: a digital PLL structure with a demodulator and a decoder made up of digital logic units that include command type identification logic.

Once the low-frequency of the power signal waveform is filtered, the receiver performs signal demodulation for the receiving interface by evaluating the relevant pulses of the information bitstream. As can be shown in the following analysis, the communication protocol has been created such that the transmitted signal retains command level integrity despite interference from power circuit noise (e.g., due to the switching operation of the H-bridges in the PDTRM string). To provide communication resilience, an approach based on

Maximum-Length Sequence (m-sequence) digital encoding and pattern recognition [108] is used. This important approach helps the differentiation of transmitted symbols in a noisy environment and permits exact locking on the receiver end, i.e., the identification of the beginning of the data reading process. Encoding and bit representation of all sequences utilized in this study are shown in Table 5.1.

Table 5.1. Encoding of Sequences.

Type of Sequence	Bit Realization
15-bit m-sequence	0101 1001 1100 001
7-bit m-sequence	0010 111
31-bit m-sequence	0011 0000 0111 0010 0010 1011 1101 101
20-bit distinctive seq.	0011 0011 0010 1010 1010

The transmission of the digital information is performed through the creation of a square waveform that undergoes an FSK modulation. This square waveform forms the signal developed as a PDTRM configuration bitstream. The FSK modulation alternates the square wave output between two frequencies, f_1 and f_2, where f_1 is used on the symbol that represents bit 1 and f_2 on the symbol that represents bit 0.

The frequencies f_1 and f_2 can be expressed as symmetrical deviations of a central carrier frequency, f_c in order to create the two alternating square wave signals s_1 and s_2, as follows:

$$\begin{aligned} \mathrm{s_1(t_k)} &= \mathrm{sgn_b}\big(\cos(2 \times \pi \times (\mathrm{f_c} + \Delta_\mathrm{f}) \times \mathrm{t_k})\big) \\ \mathrm{s_2(t_k)} &= \mathrm{sgn_b}\big(\cos(2 \times \pi \times (\mathrm{f_c} - \Delta_\mathrm{f}) \times \mathrm{t_k})\big) \end{aligned} \tag{5.1}$$

where t_k (sec) is the time instant of the $\mathrm{k^{th}}$ clock edge, Δ_f is the frequency deviation, and $sgn_b(x)$ is defined as follows:

$$\mathrm{sgn_b(x)} = \begin{cases} 0, & \text{if } \mathrm{x} \le 0, \\ 1, & \text{if } \mathrm{x} > 0. \end{cases} \tag{5.2}$$

The FSK modulator transmits s_1 and s_2 interchangeably according to the binary value of the data signal $m(t_k)$ which leads to the combined signal expression of the transmitted signal $s_{BFSK}(t_k)$ as follows:

$$s_{BFSK}(t_k) = m(t_k) \times s_1(t_k) + (1 - m(t_k)) \times s_2(t_k) \tag{5.3}$$

where

$$\mathrm{m(x)} = \begin{cases} 0, & \text{if bit to trasmit is 0} \\ 1, & \text{if bit to transmit is 1} \end{cases} \tag{5.4}$$

The highest rate of change of $m(t_k)$ is the data symbol rate i.e., the frequency of the data signal f_m. The deviation ratio D of non-sinusoidal signals is the ratio Δ_f/f_m, which also suggests that, according to Carson's rule [109], the 98% of signal power is occupied in a bandwidth B_T that is given by:

$$\mathrm{B_T} = 2 \times \mathrm{f_m} \times (\mathrm{D} + 1) \tag{5.5}$$

Table 5.2. Design parameters of the communication protocol in the developed downlink PLC scheme.

Parameter of the PDTRM system	Symbol	Dimension
Carrier period for symbol=1	$\boldsymbol{D_1 = f_{clock}/f_1}$	20 CLKs
Carrier period for symbol=0	$\boldsymbol{D_2 = f_{clock}/f_2}$	30 CLKs
Number of periods in symbol=1	$\boldsymbol{n_{d1}}$	6
Number of periods in symbol=0	$\boldsymbol{n_{d2}}$	4
Bit (LLB) Size of 1	$\boldsymbol{d_1 \times n_{D1}}$	60 μsec
Bit (LLB) Size of 0	$\boldsymbol{d_2 \times n_{D2}}$	60 μsec
Packet (MLB) Size	$\boldsymbol{n_p}$	15 Symbols
Batch (HLB) Size	$\boldsymbol{n_b}$	10 Packets
Downlink time-slot duration	$\boldsymbol{T_{DL}}$	9 msec

The information of the data bits is transmitted serially according to the bitstream that is set by the electronic circuit of the RTC (Fig. 92). The design parameters that describe the communication protocol of this work are summarized in Table 5.2. The selected carrier frequency f_c is 5/6 of 100 kHz and Δ_f = 1/6 of 100 kHz, which translates to the FSK frequencies f_1 = 100 kHz and f_2 = 2/3×100 kHz = 66.6 kHz. The symbol duration d_{LLB} ($1/f_m$), was chosen to be 60 μsec and therefore f_m = 1/6 × 100 kHz, D=1 and $B_T = 4/6 \times 100 \;=\; 66.6$ kHz. The symbol that represents bit = 1 is comprised of n_{D1} = 6 periods of frequency f_1 ($n_{D1} \times D_1$ = 6 × 10 μsec = 60 μsec) and the symbol that represents bit = 0 is comprised of n_{D2} = 4 periods of frequency f_2 ($n_{D2} \times D_2$ = 4 × 15 μsec = 60 μsec).

The composite signal that passes through the High-Pass Filter (HPF) is amplified and digitized in order to be sent to the PDTRM receiver's digital demodulating and decoding stages. Therefore, on the RCV front-end output, each properly rebuilt symbol will resemble its original square shape, where each bit is represented by a brief (60 μsec) square-wave oscillation (BSWO). The first three stages of the receiver's digital logic units are devoted to demodulating the BSWO stream, while the latter three stages are devoted to decoding the regenerated bitstream into valid instructions. The demodulation logic is intended to distinguish between the two symbols by correctly locking at the beginning of each BSWO. It consists of three sub-stages whose operations are outlined in the following paragraphs.

5.3.2. 1st demodulation stage - Phase locking

The first stage of the receiver measures the time interval (in clock ticks or CLKs) between the rising pulses of the received signal and then estimates an average duration d_1 (also measured in CLKs) for the narrowest period once it receives a sufficient number of samples. Through this process, the digital logic can safely predict the majority of the near-future starting points of the pulses with frequency f_1, which facilitates the successful locking of the next stage.

5.3.3. 2nd demodulation stage - Symbol locking

The estimated period d_1 is compared with the anticipated value of D_1, and if the deviation is slight then the receiver recognizes that this corresponds to a symbol of the highest frequency (i.e. f_1). The receiver is designed to expect pulses with a duration D_2 that is wider by 3/2 of the estimated average duration d_1, so upon the reception of such a signal, it can safely infer the acquisition of the lowest frequency symbol (i.e. f_2). The identification of a signal that is comprised of n_{D1} periods of duration D_1 and/or a signal that is comprised of n_{D2} periods of duration D_2, is called 'Symbol Locking'.

5.3.4. 3rd demodulation stage - Bit locking

In this stage the digital logic identifies the beginning of every BSWO and the locking is set once the system receives two consequent diverse symbols. In principle, this can be either a series of narrow pulses (bit 1) followed by a series of wide pulses (bit 0) or vice versa. Fig. 94

that follows, presents an expanded view of the receiver back-end, mostly focusing on the PLL and demodulation logic for the 2-bit sequence 10.

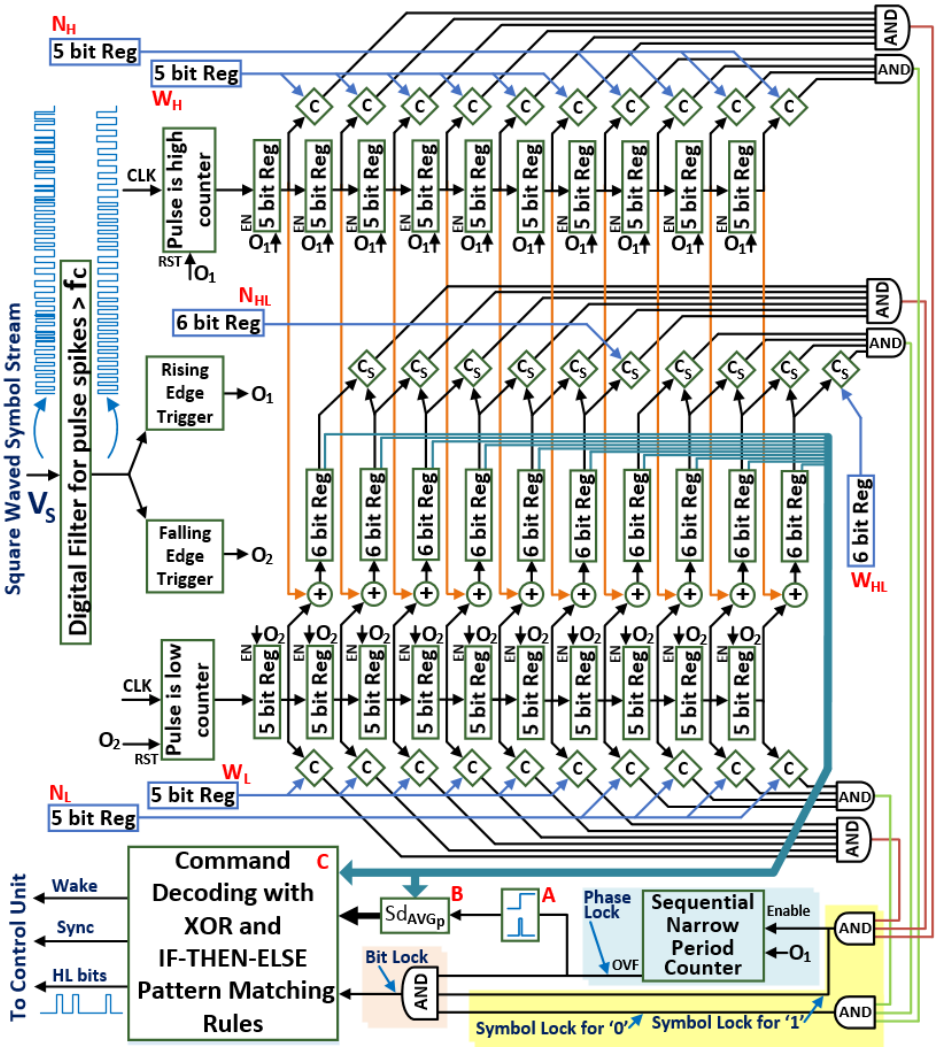


Fig. 94. Block diagram of the receiver digital back-end in each PDTRM of the cascaded H-bridge converter.

The 1st part includes a digital filter that removes any high-frequency digitation spikes lasting less than a quarter of f_{clock}/f_c clock periods. This guarantees that any square wave with a frequency higher than $2 \times f_c$ Hz will be digitally filtered and the same will apply to any other noise. The 2nd part begins with two digital counters with the one counting the clock ticks (CLKs) of the positive pulse peaks ('Pulse is high' counter) and the second counting the CLKs of the negative pulse peaks ('Pulse is low' counter).

The sampled counter values of each counter are fed to a series of $n_{D1} + n_{D2} = 10$-position shift-registers which store the consequent values (in CLKs) of the high and the low parts (widths) of the $n_{D1} + n_{D2} = 10$ most recent periods of the incoming signal. Between these two sets of shift-registers, one extra set stores the consecutive sums of their respective values

(i.e., the periods of each pulse). Each of the registers is accompanied by a dedicated comparator that compares its stored value against a preset one. The comparators are shown in Fig. 94 as C and C_S, respectively. They have a comparison threshold of $Sd_p/2$ and Sd_p CLKs, respectively, in order to compensate for any digital noise that still exists in the received signal. Out of the 10 positions of every shift-register, the first 6 (n_{D1}) are dedicated to sense a narrow-pulse BSWO and the last 4 (n_{D2}) are dedicated to sense a wide-pulse BSWO. In this work, the design has defined N_H=N_L=$D_1/2$ CLKs and W_H=W_L=$D_2/2$ CLKs because the expected carrier signal is a square wave with a 50 % duty cycle. Also, N_{HL}=$N_H + N_L$=D_1 CLKs and W_{HL}=$W_H + W_L$=D_2 CLKs.

When all of the first 6 dedicated comparators of the three shift-registers of Fig. 94 send a positive signal for at least 4×6 = 24 periods (where 4 is the maximum number of bits equal to logic 1 in the selected 15-bit m-sequence) then the 'Sequential Narrow Period Counter' overflows by signaling a 'Phase Lock' to the next stage. Block 'B' sends the estimation of the moving average carrier period when triggered, and block 'A' ensures that this triggering will only happen once. Block 'A' is re-enabled only when another mechanism detects that no packets are being received for time interval R_T. Each time that the first 6 and/or the last 4 comparators of every shift-register sense the appropriate pulses that indicate the passing of the respective BSWO, they send a 'Symbol Lock' signal. However, the 'Bit Lock' is achieved when all three conditions (a 'Phase Lock' and both 'Symbol Locks') are triggered. This means that the bit-locking will only happen when the receiver of Fig. 94 successfully senses a zero BSWO followed by a one BSWO.

The remote user-interface (or RMCU) can favor the operation of the locking mechanism of the receiver by broadcasting a synchronization sequence (a few narrow pulses for phase-locking followed by a few alternating BSWOs for symbol- and bit-locking, respectively) before command transmission in order to enhance the quality of data reception.

Once 'Bit Locking' has been achieved, the next stage begins the reception of the period values of the center shift register, and by using a net of XOR gates (for bit-wise comparison) and conditional cases in the form of IF-THEN-ELSE, it checks if the sequence of the bits matches with the expected m-sequence encoding, layer by layer. This process operates as described in the following paragraph.

5.3.5. 4th demodulation stage - Packet locking

In a similar fashion to 'Bit Locking', the 4th stage checks the degree of similarity of binary sequences against a rule-based pattern recognition logic. This stage receives the stream of binary data, and by using an XOR-based comparison it identifies if a series of n_p consecutive bits (comprising a data packet) matches one of two pre-designated m-sequences. The number of bits of an m-sequence is, by definition, a power of 2 minus 1. In this work n_p is 2^4-1, so n_p = 15 bits. The m-sequences have been selected in order to minimize these packets' autocorrelation property. A cyclic shifting of the packet bits generates n_p-1 new packets, called binary vectors. The binary vectors generated by shifting an m-sequence are as independent as possible, i.e., the count of the bits with the same logic level to be holding the same positions is minimal. The transmitter is designed to encode the required information into two specific binary m-sequences (two specific 15-bit packets) complementary to each other, here 0101 1001 1100 001 and 1010 0110 0011 110. The first of the two m-sequences represents bit=0, and the second represents bit=1.

These packets are referred to as medium-layer bits (MLBs) to distinguish them from the low-layer bits (LLBs) that these packets are comprised of. The minimal autocorrelation guarantees that the probability of a misidentification (i.e. the interpretation of a binary vector as the inverse of what was intended) is very low. The fact that there are no binary vectors that can pay significant resemblance to the original m-sequence minimizes the miss-hits of the 'Packet Locking' process and maximizes the punctuality of the packet start definition. For the case of time periods where the power circuit noise is so corruptive that the packet is not identifiable, the receiver examines the condition of the received packets by using a matching comparator that counts the number of LLBs that own the anticipated logic level given their position in the packet. If a satisfactory number of LLBs ($m_p < n_p$) is found to carry the proper logic level in the proper position of the packet, then this bit vector is considered valid and the packet is identified either as the predesignated m-sequence or its complementary one. In the first case, the MLB is identified as bit 1, and in the second case, it is identified as bit 0.

If a series of consequent packets is not identifiable, then the ratio of invalid to valid consequent packets reaches a remarkable level, indicating an out-of-order packet reading process. In order to re-calibrate the packet starting point, a triggering mechanism forces the decoder to re-estimate d_1, d_2 and proceed back to proper 'Symbol Locking' and, subsequently, to proper 'Bit Locking' and 'Packet Locking'.

5.3.6. 5th demodulation stage - Batch locking

In order to further enhance the robustness of the transmitted data, the communication protocol assumes an extra layer of m-sequence encoding of n_b bits (here n_b = 2^3−1=7). Similarly, the two n_b-bit complementary m-sequences (comprised of MLBs) are designed to be identified as bits 0 and 1, here 0010 111 and 1101 000, respectively. The pattern recognition follows the same idea and the locking is referred to as 'Batch Locking'. However, contrary to the 4th stage, on this decoding layer, the batch has a length of n_b+3 MLBs. More specifically, the 7-bit m-sequence is contained in a 10-bit batch where the first 2 MLBs are referred to as 'Head' and the last MLB is referred to as 'Tail'. The 7-bit m-sequence in the middle is referred to as 'Payload'. For the 1st Payload (0010 111) the head is fixed to bits '01' and the tail is fixed to bit 1 and for the 2nd Payload (1101 000) the head is fixed to bits '10' and the tail to bit 0. This way, the two valid batches, which are also referred to as high-layer bits (HLBs), are designed to be complementary, with the first one representing bit 0 and the second one representing bit 1.

Since the Payload is the key binary sequence that is being compared against the selected m-sequences, the head and the tail can contribute as safe margins when the communication in the power line is utilized to its half-duplex potential. Additionally, the head of every batch is dedicated towards the facilitation of the locking mechanisms (Phase, Symbol and Bit Locking) and along with the tail, they both contribute to the synchronization of the PDTRMs. This synchronization is important for synchronizing the power vector components of the individual H-bridges to achieve proper power production by the overall cascaded H-bridge converter. The structural breakdown of an HLB (Batch) consists of n_b+3 MLBs (Packets), where each MLB consists of n_p LLBs (Bits or Symbols), and each LLB has a duration of ($n_{D1} \times D_1$ or $n_{D2} \times D_2$). So, here, every HLB has a duration of T_{DL}= (n_b+3)× $n_p \times n_{D1} \times D_1$ =10×15×6×10 μsec = 9 msec.

5.3.7. 6th demodulation stage - Command identification

This layer of the communication protocol assumes a prefixed number M of HLBs (here M = 51) that form the PDTRM parameterization commands. Depending on their goal, these fall under two main categories: (a) synchronization commands and (b) functional commands.

A. Synchronization commands

The synchronization commands require the creation of a precise synchronization action and take advantage of the m-sequence encoding to further lower any misapplication risk. They are split into two parts, Ms_1 and Ms_2. In this work, Ms_1 reserves the corresponding space of 20 HLBs (20 x T_{UL_DL} = 1.2 sec) and Ms_2 the space of 2^5–1=31 HLBs (31 × T_{UL_DL} = 1.86 sec). Part Ms_1 is comprised of a special sequence of BSWOs designed to excite the locking mechanisms of the receiver. Specifically, Ms_1 is split into three parts Ms_{11}, Ms_{12} and Ms_{13}, with Ms_{11} having a duration of 10 x T_{UL_DL} = 0.6 sec, and Ms_{12}, Ms_{13} of 5 x T_{UL_DL} = 0.3 sec, each.

During Ms_{11} the transmitter is silent, while during Ms_{12} the transmitter sends BSWOs that correspond to bit 1 (which is the same as the transmission of a narrow-period square wave, i.e., the one of D_1 for a duration of Ms_{12}). Finally, during Ms_{13} it sends interchanging (narrow- and wide-period) BSWOs (i.e., the LLB stream "0101010101…"). The software of the RTC is programmed to transmit M bits of information formed as commands. Each time the system pulls a 51-bit command out of the commands queue, it checks if this is a syncing command by comparing its 20 first digits with the distinctive sequence 0011 0011 0010 1010 1010.

	Command break-down structure			
Type	**10 HLBs**	**10 HLBs**	**10 HLBs**	**21 HLBs**
1. Wake	**0011001100**	**1010101010**	**0011000001**	**110010001010111101101**
	Silence for time equal to 10 bits, then frequency f_1 for time equal to 5 bits, then swap BSWOs for time equal to 5 bits		*31-bit m-sequence*	
2. Sync	**0011001100**	**1010101010**	**1100111110**	**00110111010100001001O**
	Silence for time equal to 10 bits, then frequency f_1 for time equal to 5 bits, then swap BSWOs for time equal to 5 bits		*complementary 31-bit m-sequence*	
3. Functional	**Cascaded H-bridge PDRM parameterization command**	**DC voltage regulation value**	**DC power regulation value**	**CRC**
	Command-type control bits	*V-regulation bits*	*P-regulation bits*	*Cyclic Redundancy Check bits*

Fig. 95. Breakdown structure of the PDTRM configuration commands in the downlink PLC method developed.

As shown in Fig. 95, both 'Sync' and 'Wake' instructions intentionally begin with that sequence to differentiate from the general situation, which occurs when the RTC provides a functional command. This is how the RMCU (or RTC) codes the transmission of the Ms_1 portion of information, as opposed to the sequence of BSOWs suggested by the real HLB

vector. Part Ms_2 of a synchronization instruction is intended to include one of the two HLB complimentary m-sequences known as 'Sync' or 'Wake'.

These m-sequences are configured to be the binary vector 0011 0000 0111 0010 0010 1011 1101 101 with a decimal value of 406394349 and its binary inverse with a decimal value of 1741089298. When a PDTRM receiver recognizes one of these two m-sequences, it executes the corresponding synchronizing algorithm. The sent 'Sync' instruction is intended to inform all PDTRMs of the overall cascaded H-bridge power converter when a new zero crossing on the power channel should occur (and can also be used to define the time instant that a transmission from the PDTRMs to the RMCU could take place). The broadcasted 'Wake' command signals the start of a fresh cycle of PDTRM transmissions and thereafter specifies the reserved (pre-ordered) time period during which each PDTRM may communicate its status information (for the case of half-duplex linking).

B. Functional commands

The functional commands are intended to carry useful parameterization information for the operation of the PDTRMs in the target application (such as for switching between a stand-alone and grid-connected operation or between DC and AC voltage production by the cascaded H-bridge converter, the definition of the desired regulation value of the DC source voltage or power if the PDTRMs are powered by a PV or battery source, and/or the output frequency of the chopper). Such an instance is shown in Fig. 95.

These instructions are likewise divided into Mf_1 and Mf_2 halves. Part Mf_1 reserves 30 HLBs for transmitting the instruction's data. In addition, section Mf_2 reserves 21 HLBs as a Cyclic Redundancy Check (CRC) encoding [110] to simplify error detection (if there are virtually any burst faults or 2, 4, or odd numbers of random HLB errors) and repair of Mf_1 data (if there exists 1 HLB error). The selected 21-bit CRC polynomial (1011 0010 1011 1010 1000 1) has one of the greatest 21-bit Hamiltonian values under the assumption of a constant, low, and independent random Bit Error Rate (BER). The CRC polynomial is represented in decimal as 1464145. The RMCU must always account for periods when a communication of type 'Wake' is required. This is accomplished through the proper prioritization of the 'Wake' command on the RTC site, where the transmitter permits any 'Sync' or Functional commands to be sent, as long as the available time frame exists (i.e. 51 HLBs for a 'Sync' or 'Wake' command and 51 HLBs for the functional command that follows). In this work, the information about all PDTRMs has been programmed to be updated every 4 minutes, therefore (in the event of a half-duplex

situation) there is a time constraint during which all PDTRMs must broadcast their data (here, 4 minutes). In accordance with TDMA, each PDTRM broadcasts its status within a predetermined time range based on its (hard-wired) ID. The 'Wake' command serves as a reminder to all PDTRMs that a new status reporting cycle has begun for each PDTRM. Akin to the 'Sync'-type command, the 'Wake' command specifies the times at which each PDTRM may send. This indicates that if the internal clock time shifting of the PDTRMs is so minimal that corrections are not required more often than every 4 minutes, the type 'Sync' command may only be utilized for locking improvement reasons right before to the transmission of a functional command. Moreover, if functional instructions are given less often than once per 4 minutes, the 'Sync' command may be omitted since a 'Wake' command will be mediated, necessitating a synchronization process. This also indicates that it is desirable to send a functional command immediately after the 'Wake' command, since it has the same locking-enhancement effect as 'Sync'.

5.3.8. Design parameters of the developed downlink PLC Method

Table 5.3 presents the parameters related to reception sensitivity. While setting these parameters, the designer must ensure that the design choices enable the receiver to ignore suspicious packets unless it is guaranteed that the commands will be interpreted correctly. The clock of the experimental setup is set to f_{clock} = 2 MHz. The two ideal periods of the symbols involved in the FSK transmitter scheme are T_{D_1} and T_{D_2}, where T_{D_1} = 1/f_1 = 10 μsec and T_{D_2} = 1/f_2 = 15 μsec. This translates to an anticipated measured period D_1 = f_{clock}/f_1 = 20 CLKs and D_2 = f_{clock}/f_2 = 30 CLKs.

Table 5.3. Design parameters related to reception sensitivity in the developed downlink PLC method.

Parameter	Symbol	Unit
Clock frequency of the PDTRM	$\boldsymbol{f_{clock}}$	2 MHz
BSWO frequency representing bit=1	$\boldsymbol{f_1}$	100 kHz
BSWO frequency representing bit=0	$\boldsymbol{f_2}$	66.6 kHz
BSWO period locking threshold	$\boldsymbol{S_d}$	±4 CLKs
BSWO AVG period locking threshold	$\boldsymbol{S_{d-AVG}}$	±2 CLKs
Moving average BSWO samples number	$\boldsymbol{S_n}$	20
Packet error tolerance / Packet Size	$\boldsymbol{n_{p_{er}}/n_p}$	2/15 LLBs
Batch error tolerance / Batch Size	$\boldsymbol{n_{b_{er}}/n_b}$	2/10 MLBs

The 'Symbol Locking' mechanism allows for a deviation S_d up to ±4 CLKs to any pair of the sequential periods of a symbol. The same mechanism allows for a deviation of S_{d-AVG} up to ±2 CLKs between the calculated average of the symbols' duration S_{AVG} and the ideal value $S = n_{D1} \times D_1 = n_{D2} \times D_2 = 120$ CLKs. This shows that the designed tolerance of the receiver to both frequencies of the FSK scheme is $S_{d-AVG}/S = 1.66$ %. The moving average of the symbol's duration is calculated by taking into consideration $S_n = 20$ samples of the most recent symbol duration measurements. This duration S_n is considered a sensitivity design parameter because it indirectly dictates the time limit R_T that is calculated according to:

$$R_T = S_n \times S + S_{d-AVG} \tag{5.6}$$

This time limit suggests that if the receiver has not successfully received a single valid packet up to that time, the control circuit will reset all locking mechanisms. For the design developed in this work the R_T has been set to $R_T = 20 \times 120 + 2 = 2402$ CLKs. In addition, a single packet is considered valid if the errors are no more than $n_{p_{er}}$. Therefore, if the reception guarantees that an adequate number m_p of symbols (LLBs) present the proper value (0 or 1) in the anticipated position (according to the m-sequence encoding), so that $n_p = m_p + n_{p_{er}}$, then the packet is considered as valid, else it is labeled as invalid and it is ignored. Subsequently, the same logic stands for the next layer, i.e., the case of batches (HLBs). A batch that consists of n_b packets (MLBs) is considered as valid if the corrupted (dropped) packets are not more than $n_{b_{er}}$. So, the sufficient number of packets m_b is such that $n_b = m_b + n_{b_{er}}$.

The head of every transmitted HLB is designed to facilitate the receiver tuning-in (i.e., 'Phase Locking', 'Symbol Locking', and 'Bit Locking'), respectively. Towards that goal, the Ms_1 space of the Syncing commands, which reserves the corresponding timeslot of 20 HL bits, is filled with a special pattern of symbols. The first 10 HL bits are filled with BSWOs of frequency f_1 (square waves at 100 kHz), and the 11th to the 20th bits are filled with BSWOs that interchange between symbols 0 and 1 to facilitate the operation of the 'Symbol locking' mechanism. The choice of including locking assistance in the transmission of the syncing commands is regarded as an extra step to ensure that the receivers of the PDTRMs will be in a Bit-Locked state just before receiving the 31 HLBs of the syncing command. So, given that Ms_1 regards a time frame of 10 HLBs, full of BSWOs of frequency f_1, the proper phase-locking can solely depend on the use of periodic syncing commands of type 'Sync'. If the level of noise and other interferences is low, the 'Sync' commands may be introduced only when required, i.e., before every functional command to guarantee proper locking of the receiver.

The time-frame definition for every PDTRM is essential when the internal clock shifting has been so high that reception errors are produced. Based on the given design choices, a type 'Sync' command can be as frequent as 51 HLBs. If the Ms_1 was selected to be narrower (for example to occupy the space of just one HLB) it would allow for the type 'Sync' commands to be sent every 32 HLBs, although the risk of phase-locking failure under a noisy environment would increase. Similarly, if the Ms_2 (the m-sequence) was chosen to be narrower, this would allow for more frequent clock shifting corrections and increase the risk of command misidentification. The designer needs to consider these trade-offs depending on the nature of the noise (narrow or broadband spikes, corruptive bursts, etc.) that will be injected into the power cable in each target application by using the power line circuit-level models presented in [81], [82].

5.3.9. Clarifications on the design of the 3-layer structure encoding

In order to support full-duplex communication, and in accordance with the analysis of Chapter 4, the downlink parameters must be carefully chosen so that the uplink broadcasting would not coincide with the transmission of the downlink information. The decision to share access to the common power line medium by utilizing a time-division technique was chosen as the most straightforward implementation that minimizes any errors that may occur during the data reception and/or transmission.

As it has already been noted, the information sent by the user-interface unit is FSK modulated, at two frequencies, 66.6 kHz and 100 kHz. The time duration of each bit of information is fixed as this lasts a total of 60 μsec as this either comes from 4 pulses of 15 μsec (for 66.6 kHz) or from 6 pulses of 10 μsec (100 kHz). The interface module sends (every 60 msec) a total of 150 bits of information which last 150 x 60 μsec = 9000 μsec or otherwise 9 msec. These 150 bits constitute the synchronization signal which is divided into 10 blocks of 15 bits. The 15 bits constitute an m-sequence polarized either forward (symbolizing 0) or reverse.

The 15-bit sequence chosen is: **010 110 011 100 001**. Therefore,

010 11 00 111 0000 1 encodes "**0**" and **101 00 11 000 1111 0** encodes 1.

The ten 15-bit sequence blocks, henceforth "packets", are divided into 3 groups. The first is the head consisting of 2 packets, the second is the load consisting of 7 packets and the third is the tail consisting of 1 packet (2+7+1 = 10 packets).

The first two packets are used for the circuit to "lock" on the bit (bit-lock), i.e., to recognize the duration of a bit and distinguish when it begins, and then "lock" on the block (packet-lock) to recognize when a 15-bit block starts and how long it lasts. So, it can then successfully read the 7-packet load to identify if it carries any information and what is the context of the information it carries.

The following 7 packets carry a 7-bit m-sequence which signals 1 synchronization signal, regardless of how it is polarized. However, its polarization is used as a bit of information that will then be used to parameterize the operation of the cascaded H-bridge converter modules and the PV sources that they comprise (downlink info).

The 7-bit m-sequence chosen is: **001 0 111**. Therefore,

001 0 111 encodes "**0**" and **110 1 000** encodes 1.

By convention, of the 10 packets of the sync signal, the first 2 packets will always represent '00', the next ones will have one of the two polarities of the 7-bit m-sequence, while the last one will also be 1 although it carries no useful information but rather occupies a time window space in which the appropriate count down is done, to produce the pulse ("SYNC NOW!") that will be properly used by the rest of the digital logic of the cascaded H-bridge converter modules. exactly at the end of this 10-bit packet series Coding with 2-level signatures (7-bit on top of 15-bit) ensures that the sync signal will be strong enough against the channel noiseIn more detail, the bits that will be sent are shown in Fig. 96.

Explanation	Bit	Packets (2+7+1) m-sequence OR m-sequence’
2 bits of 0	0	"010110011100001"
	0	"010110011100001"
7 bits of the m-sequence i.e. "0010111"	0	"010110011100001"
	0	"010110011100001"
	1	"101001100011110"
	0	"010110011100001"
	1	"101001100011110"
	1	"101001100011110"
	1	"101001100011110"
1-bit shift waiting time	.	does not matter

Fig. 96. Example of a 'Batch' packet (consisting of 10 x 15 = 150 bits/symbols).

It does not matter what the last bit is (in this implementation it is chosen to be 0) as the preceding 7-bit m-sequence ensures that once the "signature" of the sync signal is correctly obtained, the circuit must at some point output the sync pulse. This moment is chosen to be a single bit after the end of the 7-bits of the signature as it needs on the one hand a small empty period of time to detect the signature (which for this particular implementation is a little longer than ½ packet bit), on the other hand it is chosen to be done in integer multiples of packet bits as this may accommodate the way the user-interface software is implemented.

Fig. 97 presents the general diagram of the digital subsystem that undertakes the recognition of receiving a synchronization signal as well as the decoding of the information it carries. The synchronization signal is decoded in the blocks under the 'Syncing Logic' bracket. Under the bracket 'Downlink Interface' are the blocks that have already been mentioned as the ones that undertake the demodulation of the information from the two carrier frequencies.

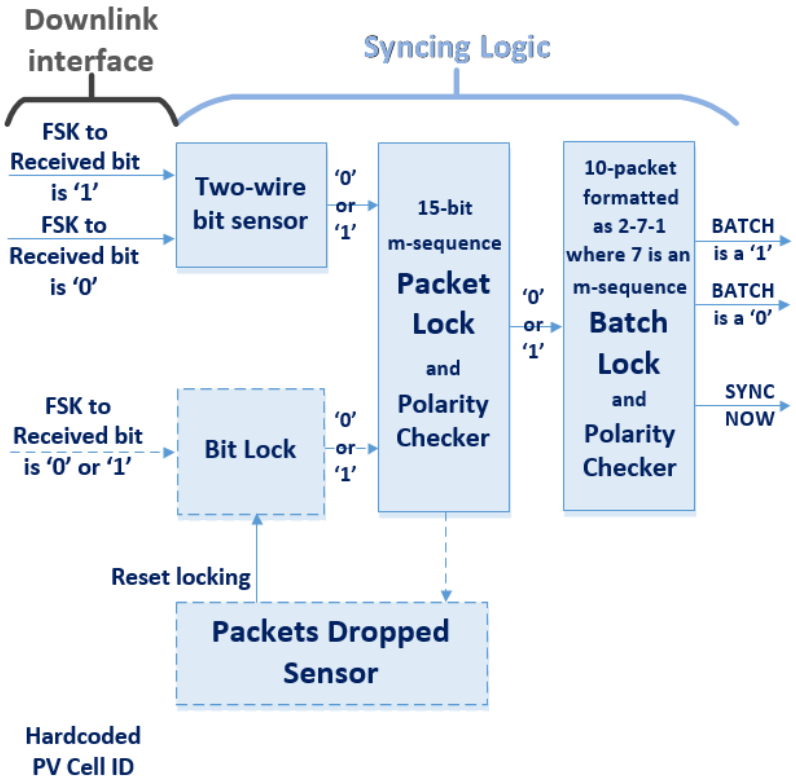


Fig. 97. General diagram of the syncing / demodulation logic of the PLC downlink receiver.

Two different approaches have been developed in the logic analyzed in the diagram above, in which the serial information obtained after the demodulation of the downlink interface circuit can be correctly located. One (two-wire bit sensor) concerns a block that

undertakes to identify the states of a bit (0 and 1) through the waveforms of two signals, while the other (Bit Lock) undertakes to identify the states of a bit (0 and 1) through the analysis of the waveform of a signal. In the event that the use of Bit Lock is chosen, it is important to use the 'Packets Dropped Sensor' block which resets the Bit Lock mechanism. This is because this mechanism is considered to be sensitive to noise and may incorrectly estimate the duration as well as the time point at which a bit of information starts. This can happen especially at that times that strong noise spikes occur on the length of the transmitting cable. It is worth noting, however, that both methods are tested as the same spikes may create similar interference in the circuit of the two-wire bit sensor (presenting twice the probability) although its implementation is the most preferable since it is characterized by design simplicity. Also, both techniques have been tested for the margins they exhibit in various enhancement techniques with digital noise rejection under the simulated environments described in § 5.4.

According to the specifications of Table 5.3, the data to be received by each PDTRM unit consists of 30 + 21 = 51 bits of information. The breakdown structure of the 51-bit packet is presented in Fig. 98.

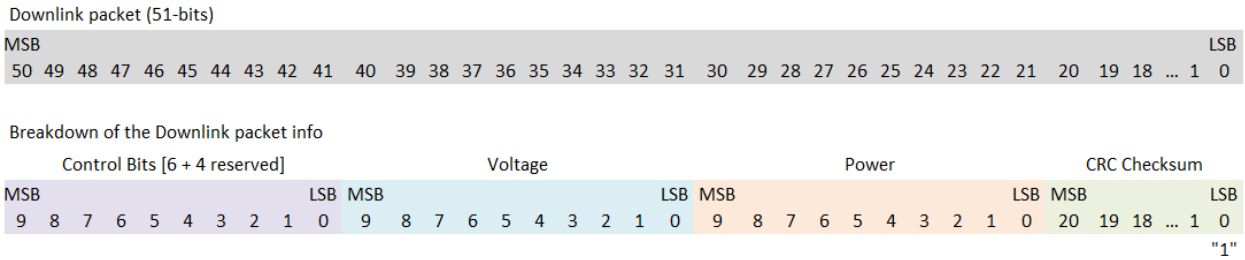


Fig. 98. Breakdown structure of the information contained in a downlink data packet.

5.3.10. Control and interpretation of configuration commands

In addition to what has been mentioned about the information carried by the 51 HL Bits, where it is noted that the first 30 of them concern the parameterization command and the 21 that follow the checksum, a suitable sequential digital circuit (Finite State Machine, FSM) was developed which implements appropriate interpretive logic so that from these 30 bits it also recognizes cases where, although they may have been transferred correctly during transmission, the information they contain as such cannot be applied or, if applied, lead to situations that either don't make sense or pose threats. This arrangement incorporated in the system of the downlink PLC control and monitoring unit, which interprets the command

information so as to apply them only if they belong to an allowed subset, helps to check the correct design and operation of the digital circuits of the communication subsystem of the cascaded H-bridge converter modules (Fig. 56).

5.3.11. Selective implementation of synchronization commands (Metronome)

Since synchronization commands in particular, may be received at the wrong time or at a variable rate, they pose the risk of inducing destabilization noise in the two-way communication of the overall system. Also, due to the fact that the clocks of the control units of the cascaded H-bridge converter modules exhibit deviations from each other, it is considered appropriate to make use of the particular synchronization commands if and only if required. This means that their presence in the protocol is not to be regarded as mandatory for the maintenance of the two-way communication, and subsequently their regular use, although encouraged since it contributes to the finest synchronization between the uplink and downlink communication interfaces, is not to be enforced in all cases.

The increase in verifiability of the control and monitoring unit offered by this function is due to the fact that the synchronization commands offer the possibility for the user to check and confirm (in the event that errors are detected on the part of the corresponding application) whether this behavior includes synchronization issues, as well as in checking how the operation of the RMCU is affected when the synchronization commands are selectively sent outside the prescribed time limits. Given the aforementioned points, the baud rate controllability process to be presented below needs to be regarded as feasible only when every PDTRMs has proven to have the ability to distinguish when it receives a valid series of consecutive HL Bits, or not.

It is noted that an HL Bit consists of 15 (low-level bits, i.e. symbols per packet) x 10 (mid-level Bits, i.e. packets per batch) = 150 symbols and lasts 9 msec, as each symbol lasts 60 μsec. Each received batch (HL Bit) is considered correct when no more than one error has been made in the 10 mid-level bits (packets) that make it up. Also, each HL bit is transmitted every 60 msec, as there are 51 bits available for use by the uplink PLC process. Therefore, programming the appropriate baud rate can take a little more than 60 msec, and so it is very easy (in e.g. 100 msec) to implement the correct baud rate programming of the HL bits since it is practically impossible to influence the communication channel in such a way and up to a degree that all PDTRMs will grasp this 'programming' opportunity, at some point. It is also

noted that until this programming occurs, the PDTRMs do not transmit information through the uplink, but only receive information through the downlink. Finally, it is important to remind that if the PDTRMs acknowledge the reception of wrong packets (mid-level bits) then they reset the read lock, until the corresponding control circuit of this level recognizes the correct packet reception.

The logic that is analyzed in this paragraph, aspiring to increase the system's reliability (in terms of synchronization maintenance), is named 'metronome' and aims to guarantee a balance between the autonomy and the adaptability of the PDTRMs, in regards to the given data transmission rate. For this to be achieved, a suitable circuit was designed which checks in a regular fashion whether the PDTRMs is allowed to become autonomous (in terms of information transmission and reception rate) in the event that the communication timing ceases to be defined (mainly due to noise or user selection). Also, the same circuit checks if a synchronization command is received at the expected time. If the synchronization command is not correctly demodulated (because its recognition has been deliberately based on very strict criteria), then the PDTRM ignores it and continues to consider valid the rate at which it was receiving until recently (i.e., the 'programmed' pace). Therefore, the system continues as if it had received each one of the two synchronization commands at the expected time. The circuitry that checks if the anticipated synchronization commands arrive at the right time takes care to readjust the beat of the 'metronome' (i.e. reprogram it in terms of rate and transmission phase) only if the commands arrive earlier than the expected time. In this way, the adaptability of the 'metronome' is constrained to the changes that arise or are imposed. For example, these may come from gradually shifting the clock of the PDTRM in relation to the corresponding one of the RMCU, as well as may be referring to changes that the user of the RMCU application wants to define.

Although the 'metronome' only refreshes if it receives synchronization commands at a time interval slightly earlier than expected, it is a stable system, as it inherently maintains a tendency to readjust its estimate (starting whenever it is not refreshed from a later point in time) so as to make it more and more likely to be renewed by an existing synchronization command every time it is not received within the expected time interval. This behavior is enforced even if due to some error (e.g. from the RMCU) the phase of the synchronization commands have changed quite abruptly and they are far apart when compared against the predetermined (programmed) position. Therefore, the extent of the 'metronome' autonomy

control (in terms of its resynchronization rate or its stability in conditions that favor its desynchronization) can be controlled, or rather exploited, through the (timely or untimely) use of synchronization commands.

5.4. Simulation results

The various versions of the downlink communication circuit that were developed during the course of this PhD thesis, have been primarily simulated in Mathworks' MATLAB Simulink. The main principles governing the designs of the Downlink communication circuits were primarily designed in Simulink and then implemented in VHDL in Quartus Prime 18.1. Their most complex parts were initially tested in Intel's Modelsim and then in Questa Sim-64 by applying specially designed workbenches that covered all operational cases.

5.4.1. Simulation of proper locking and information demodulation

As shown in the simulated timeline of Fig. 99, the pattern to be detected (shaded with a blue background) is recognized by the circuit (Batch-Lock) and then, exactly after 1 packet of 15 bits (or otherwise 1 high-level bit) its function is executed as shown by the risen "BL_NOW_SYNC" pulse. The same graph also shows the creation of the signals "BL_BATCH_IS_A_ZERO" and "BL_BATCH_IS_A_ONE" which interpret the information contained in the 7-bit load, (i.e., the polarization of 0 and 1) which is then forwarded to the parameterization information units.

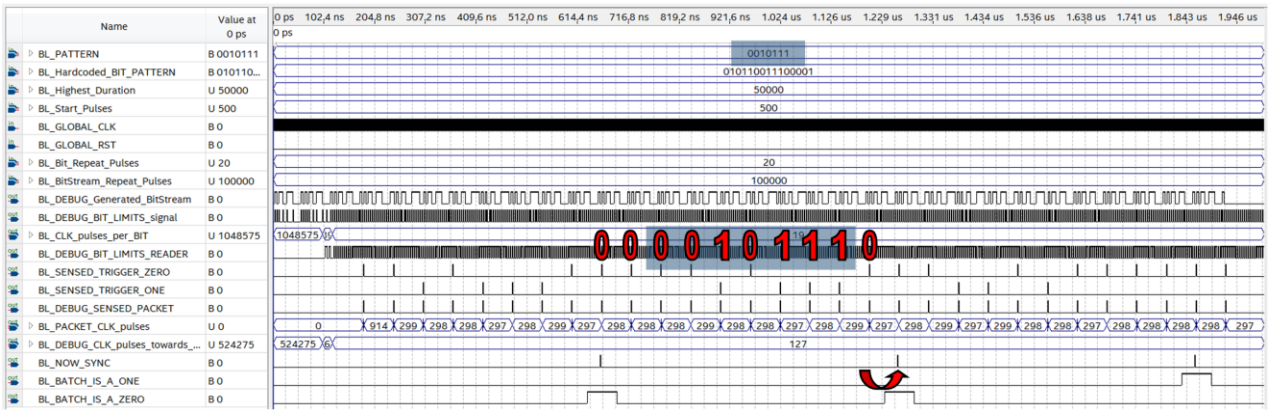


Fig. 99. Illustration of the signals that make up the batches 0 and 1 that contain the high-level (HL) bits as a load.

Regarding the parameterization information of the modules of the cascaded H-bridge converter, the specifications define that it consists of 26 bits of information, 6 for the functional control and 20 bits for the definition of the output voltage and power. For consistency reasons, better debugging, reduction of design complexity and provisioning for future improvements, the 26 bits were chosen to be followed by 4 more which are reserved for future use. In the present implementation they are alternated with the sequence 0101. The reason for this switching alteration will be explained next. As to what follows the resulting 26+4=30 bits, there are 21 more bits dedicated as the CRC Checksum, which sets a similar format to the one that was applied for the uplink data packet. Fig. 100 below depicts a downlink 51-bit package and its breakdown structure, presenting its individual parts.

The first 6 control bits are specific to the functions coded in the respective figure. In it, the 9th bit selects between DC or AC voltage production by the cascaded H-bridge converter, the 8th the AC operating frequency, the 7th whether the cascaded H-bridge converter will operate in stand-alone or grid-connected mode, and the 6th if any of the four strings of the cascaded H-bridge converter (of 250 modules each) defined by bits 5 and 4, will start or stop its operation. Bits 3 to 0 are defined as 0101.

MSB									LSB
9	8	7	6	5	4	3	2	1	0
0=DC 1=AC	0=50 Hz 1=60 Hz	0=SA 1=GC	0=ON 1=OFF	STRBit1	STRBit2	0	1	0	1

Fig. 100. Representation of the 10 control bits functions and explanation of their control nature.

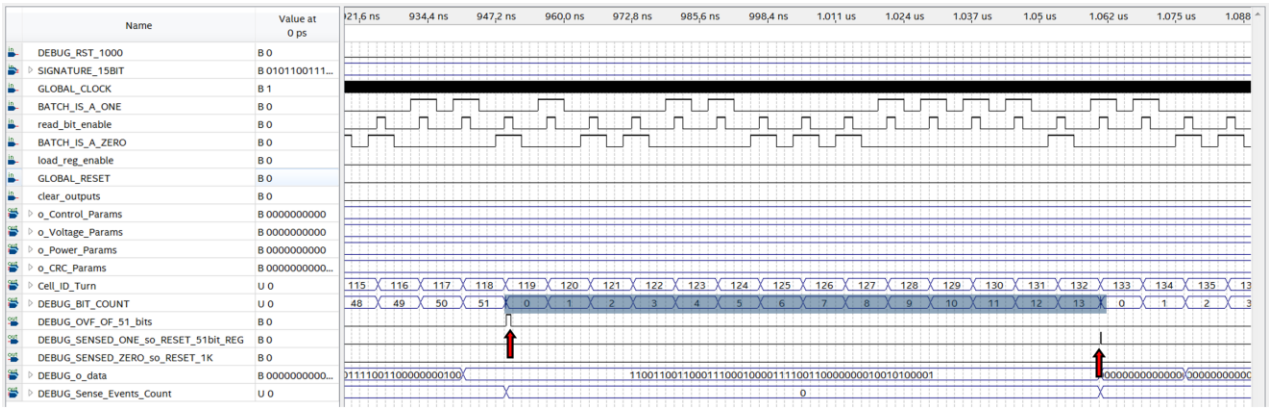


Fig. 101. Successful nulling of the serial read due to recognition of an m-sequence.

To signal the beginning of each 51-bit configuration packet, the RMCU sends the 51-bit packets framed by 15-bit m-sequences (specifically the same 15-bit m-sequences as those

selected above) with unity bias (1). Thus, when 15-bits of this bias are received, the corresponding circuit of the PDTRM resets the shift register counter and fills the 51-bit register with zeros. It also holds the current value in a 1-bit register and transfers it directly to the MSB of the next packet to be checked. Next, it starts to refill the register with the data being demodulated, one by one, until 51 synchronization signals (51-bit of information) have been received. This signals the completion of the command.

After receiving the 51-bits, the receiver resets the register that reads the sync bits serially, by settings its individual bits to zero. The timeline in the graph of Fig. 101 shows the beginning and the end of such an m-sequence. The counter "DEBUG_BIT_COUNT" from 51, resets to 14 (which lasts only a short time because an asynchronous reset is selected as soon as it determines that it has indeed received an anticipated m-sequence), so it resets to 0 once again. These bits could be n+15 (where n is an integer) and fill enough of the space between two consecutive 51-bit configuration packets. But it is better for the user-interface (RMCU) to send these packets relatively often, with the same information, so that only a short time elapses from the moment that a PDTRM starts its operation until it makes the successful coupling (power generation and emission information) with the rest of the channel.

As mentioned above, if before the 51-bit counting is complete, an m-sequence is received, either biased to 1 or 0, this register is set to zero. Especially for the case that the sequence to be received is biased to 0, in addition to the counter of this register, the counter that holds the information of how many synchronization signals have preceded also resets to zero. It is recalled that if the activation circuit of this counter has not started counting, this happens when the 15-bit m-sequence biased to 0 is received for the first time. Keeping the uplink transmission timing constant and periodic requires the user-interface to send the 15-bit m-sequence biased to 0 exactly once every 1000 sync signals. The responsibility to guarantee this pace is taken over by the RMCU software.

Thus, if it is decided to mediate exactly one m-sequence of 15-bits between 2 consecutive 51-bit parameterization packets, then it will be necessary to calculate how many 51+15 = 66s (integers) fit in 1000. In total 15 fit. Of these, 14 of the 66s will be separated by a 15-bit m-sequence biased to 1, boxed in purple, as shown in Fig. 102, and the 15^{th} m-sequence (which will be biased to 0, as shown in red frame) will be separated from its 51 bit packet to terminate its 15^{th} bit exactly at the 1000^{th} bit of the sequence. Before the 15-bit m-sequence, the sync signals (the 10bits outlined in orange) will all be ones.

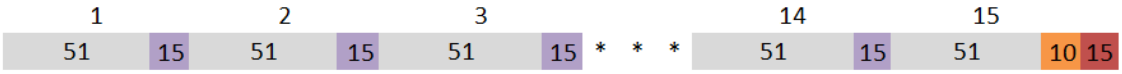


Fig. 102. Illustration of the information as it should be sent by the RMCU application based on the given communication protocol.

The reason that control bits 3 to 0 are bound to the form '0101' is because if there is an error during transmission, the first 10 51-bit bits of each packet will not look like either of the two selected 15-bit m-sequences. For the same reason it was chosen that the first bits of the 51-bit package will belong to the control bits as these are more stable (meaning that they do not change often) than the other two groups which may need to represent numerical values normalized to the corresponding 10-bit numbers (either with 2's complement or without), and more specifically to belong to 11489(dec) or 21278(dec).

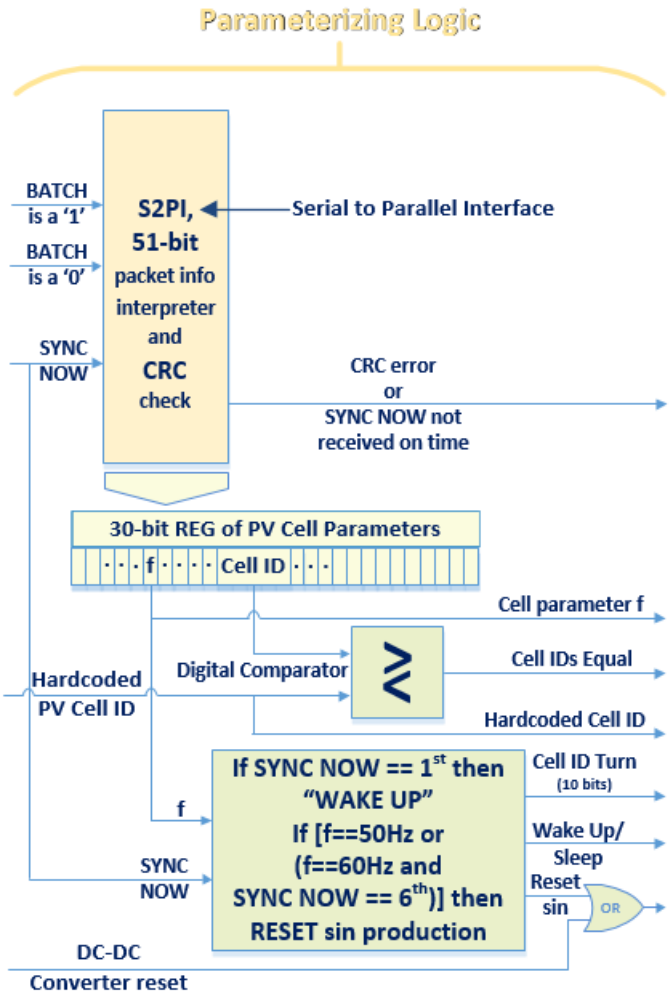


Fig. 103. The logical parameterization model, as it is configured before implementing a specialized FSM.

Fig. 103 shows the general diagram of the parameterization logic of each PDTRM. This circuit (parameterization logic) receives in its inputs the signals coming from the outputs of

the previous unit. It also takes into account the hardcoded PDTRM ID and finally provides an input for reading the zero crossings of the voltage developed in the common power channel when it is AC.

The first output of the module is a signal (CRC error or "SYNC NOW not received on time") which emits 1 when an uncorrectable error is detected or when a sync signal is not received, since this signal is normally expected to be received with some relative periodicity, and with perhaps the only exception, as developed above, at the 1000th sync signal. The last output of the unit is a signal that produces a pulse of a few clock cycles to signal the time interval to start producing the AC voltage from the DC-AC terminal full-bridge. This signal is also generated "internally" depending, as already mentioned, on the operating frequency (50 or 60 Hz) and the synchronization signals received from the downlink, as these signal the origin of the AC output voltage of the DC-AC full-bridge generated per 1 or 6 sync signal receptions. The "WakeUp/Sleep" output sends a 1 signal to the next module managing the DC-AC full-bridge of the PDTRM when a synchronization signal is first received. On the other hand, it sends "Sleep" when all the reasons mentioned above apply and there is an additional trigger for the "CRC error or SYNC NOW not received on time". The remaining 4 outputs define the DC-AC full-bridge and power converter's mode of operation, in order to produce the appropriate AC waveform component and to transmit the proper data at the anticipated time window (defined by TDMA), according to the PDTRMs ID.

5.4.2. Simulation of 1-bit error detection and correction algorithm

For verification purposes, a 21-bit CRC polynomial was used, specifically the one considered the best 21-bit CRC polynomial as it exhibits the largest Hamiltonian distance under the assumption of a low and consistently random and independent BER (bit error rate). The digital logic that produces a 21-bit CRC code (checksum) from a 30-bit information set is used to generate the extra bits sent by the uplink circuit. The same 21-bit CRC polynomial, used to produce the corresponding 21-bit checksum, is also used to decode the last 21 bits received from the downlink's 51-bit packet.

The developed circuit can detect and correct 1-bit errors as well as to detect if more than one error has been made, in which case it can reject the packet and request its retransmission. The packet is repaired using brute-force logic for the first 30-bits of the packet. The reasoning is based on the fact that if the 21-bit checksum (part B of the received

packet) does not correspond to the 30-bit info (part A of the received packet) then it can be considered that there is exactly a 1-bit reversal of value, and a calculation is made of both 30 combinations. If one gives the expected checksum received then it is considered more likely that a single bit has been reversed and corrected. If no combination gives the received checksum then it is assumed that more than one error have been made in part A (30-bit info). To check if the error has been made in part B (21-bit checksum) of the received packet, the checksum obtained by considering part A as correct is calculated, and the new checksum is compared with the one received. If they differ by only one bit then it is assumed that there was a 1-bit error (since it is very unlikely that the checksum has changed by only one bit if there has been another error on the packet) and the information carried by the packet is forwarded as correct. If the two checksums differ by more than one bit, then it is assumed that more than one error has been made.

Six different scenarios are successively presented in the timeline of the graph of Fig. 104, as well as the results of various registers for debugging, with the most important being the last signal that determines whether the packet needs to be rejected (requesting retransmission) or not. The regarded scenarios concern (from A to F) the following cases:

A. no error
B. an error in Part B (21-bit checksum)
C. three errors in Part B (21-bit checksum)
D. an error in Part A (30-bit info)
E. one error in Part A (30-bit info) and one in Part B (21-bit checksum)
F. two errors in Part A (30-bit info)

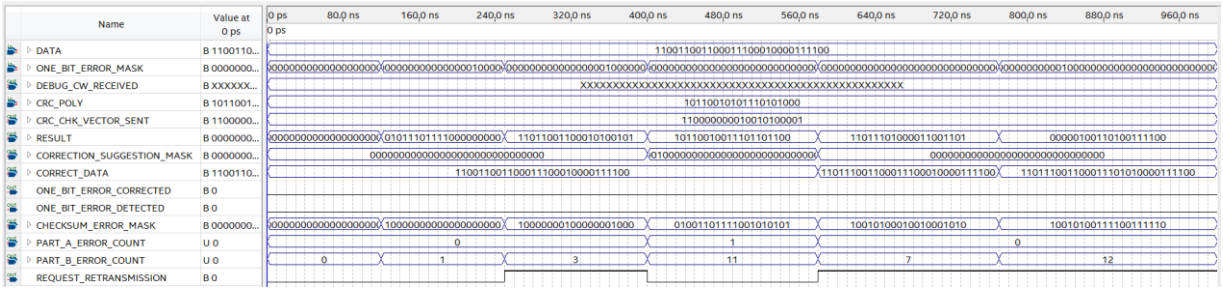


Fig. 104. Six different scenarios for examining possible errors in the 51-bit information received by the downlink receiver.

As is clear from the last bit of "REQUEST_RETRANSMISSION" scenarios A, B and D are accepted while C, E and F are rejected (and retransmission is requested). Fig. 105 displays the values obtained by the corresponding digital masks which constitutes the basis upon which

the rejection decisions are made. The 21-bit polynomial chosen to generate and decode the CRC algorithm is shown in red box in Fig. 105. In this figure, although scenario C can be corrected by assuming that both errors have been located, a retransmission is selected as the best option in order for the shared digital logic to easily cover the cases for scenario E and F, as well.

	A	B	C	D	E	F
Part A Errors	0	0	0	1	1	2
Part B Errors	0	1	2+	0	1	X
CORRECTION_SUGGESTION_MASK	0	0	0	1	0	0
CHECKSUM_ERROR_MASK	0	1	2+	x	>0	>0
C(orrect), F(alse)	C	C	C (F)	C	F	F

Fig. 105. The values taken by the masks and the corresponding rejection decisions.

The 51-bit sequences of digits used in the respective simulations are the ones in the gray boxes of Fig. 106, while the corresponding 21-bit checksum sequences corresponding to their correct reception are placed directly under them, in the green boxes. On the left is the MSB and on the right is the LSB (which for both the CRC generating polynomial and the resulting CRC checksums, is always 1).

CRC Polynomial

1 0 1 1 0 0 1 0 1 0 1 1 1 0 1 0 1 0 0 0 [1]

Example A : 30-bit info

1 1 0 0 1 1 0 0 1 1 0 0 0 1 1 1 0 0 0 1 0 0 0 0 1 1 1 1 0 0

21-bit CHECKSUM for Example A generated based on the given CRC Polynomial

1 1 0 0 0 0 0 0 0 0 1 0 0 1 0 1 0 0 0 0 1

"1"

Example B : 30-bit info

1 1 1 1 1 0 0 0 0 0 1 1 1 0 0 0 1 1 1 0 0 0 0 0 1 1 1 1 0 0

21-bit CHECKSUM for Example B generated based on the given CRC Polynomial

0 1 0 0 1 1 1 0 0 1 0 0 1 1 1 1 1 0 1 1 1

"1"

Fig. 106. Two CRC Checksum examples.

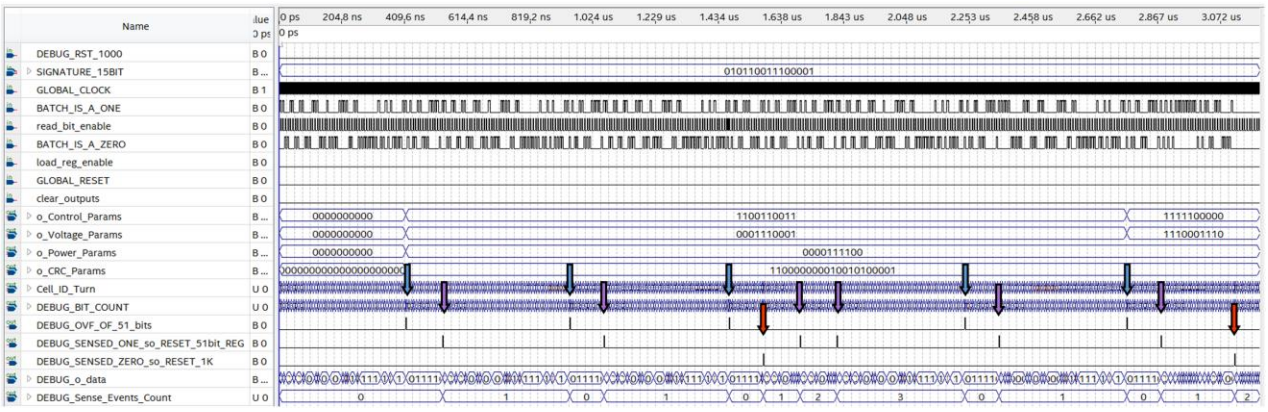


Fig. 107. Timing of batches - high-layer (HL) bits - and synchronization signals (defining the start of a new thousand).

The timeline graph of Fig. 107 presents the reception of a total of five 51-bit parameterization sequences, of which 4 are implemented with the package described as example A and the fifth with the package of example B. The timing of the reception of each of the above packets is defined by the signals presented by the blue arrows and the possible initiation of such a packet is defined by the signals presented by the purple arrows. The zeroing of the counter that counts the synchronization packets that have preceded is defined by the signals shown by the red arrows. The same counter is the one that defines the beginning of a new 1000 series.

The timeline graph of Fig. 108 presents the behavior of the CRC algorithm that is receiving the same sequence of packets as the one shown in Fig. 107. As it can be seen by observing the "DPCRC_REQUEST_RETRANSMISSION" signal, the first two packets (which are introductory) are lost, as expected, and the rest are properly received, with the 1st two belonging to the sequence of example A and the third belonging to the sequence of example B. The simulation also verifies the correct operation of the CRC checksum.

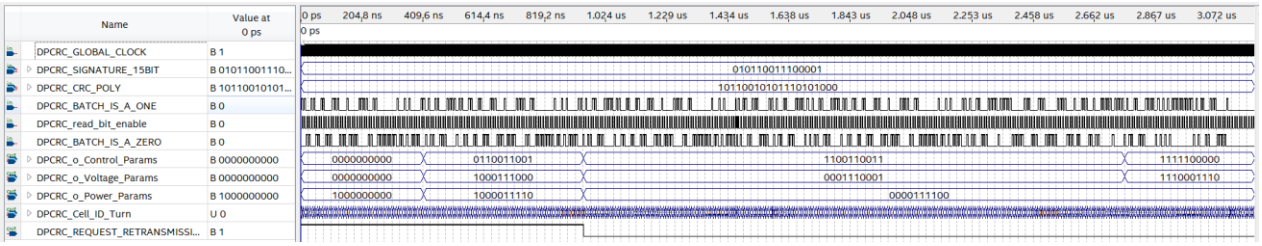


Fig. 108. Correct operation of the control and declaration signal for retransmission.

5.4.3. Simulation of Bit-lock, Packet-lock and Batch-lock digital logic

In order to detect the duration of a bit, a digital logic circuit was designed which starts by assuming that the period of a bit is long enough (e.g. 1048575 clock pulses) and gradually decreases as it detects the clock pulses intervening between two successive changes in its input. Since two consecutive changes cannot be made faster than what is preset to be anticipated as a 1-bit period, the circuit "locks" to the correct value quite easily. Then, it detects the 15-bit m-sequences, which ensure that the 1-bit lock remains correct and serves to calculate the next level where the 7-bit m-sequences are detected, meaning the batches of 7-bit packets which also indicate the correct detection of synchronization signals. If the bit lock "locks" to a period value shorter than expected, e.g. due to noise, the 15-bit m-sequences will not be detected and thus if a sufficient number of clock pulses pass without detecting

these 15-bit m-sequences, the bit-lock will start scanning for the 1-bit period from the beginning.

Two alternative methods can be employed:

i) Pattern matching:

This method concerns the pattern matching of 15-bit m-sequence packets. If there is a 1-bit error (which is very likely due to noise) the pattern matching will not work, as it is very strict and does not tolerate noise.

ii) Convolution matching:

Convolution matching can be applied instead where the tolerance can vary to some extent. In practice, ignoring 1 to 3 errors out of 15 bits is considered to be a stable implementation. Thus, the appropriate VHDL blocks are created according to this approach.

Next, various scenarios are examined where, in a bit stream consisting of a total of ten 15-bit packets, a series of bit-errors (10 in total) are introduced, as shown in the image of Fig. 109.

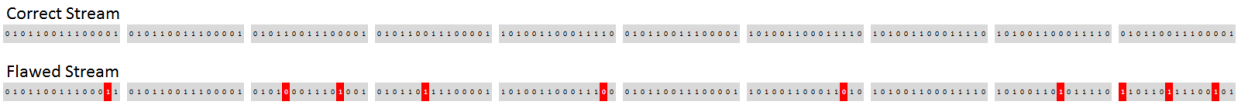


Fig. 109. Bit streams with some random errors (from 0 to 3 per 15-bit packet).

The algorithm that recognizes the logic level of the correct information (bit 0 or 1) with a tolerance of exactly 0 errors (by feeding it the correct bit stream), recognizes the correspondence of the 15-packets as shown in the signals 'PL_SENSED_TRIGGER_ZERO' and 'PL_SENSED_TRIGGER_ONE', below.

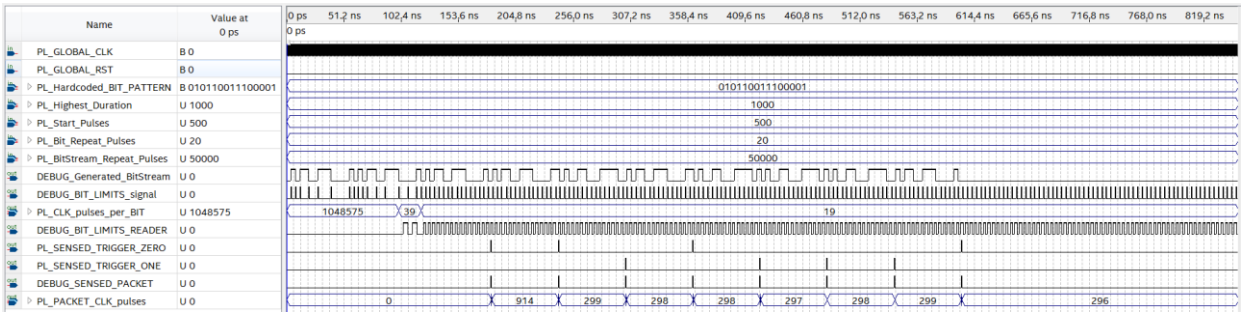


Fig. 110. The 8 recognized bit-packets.

Fig. 110 shows that the information recognized in the last 8 packets is correctly identified as 0 0 1 0 1 1 1 0. The first two packets are 'sacrificed' to facilitate the bit and packet locking, so therefore, the useful information to be transferred is ideally the last 8 bits.

Fig. 111 shows the behavior of the same algorithm when it is parameterized as before, with a tolerance of exactly 0 errors, but this time it is fed with the second bit stream showing a total of 10 errors, randomly distributed from 0 to 3 per, packet. It is observed that not many packets are recognized, resulting in a dedicated circuit that examines the percentage of dropped packets, to reset the bit locking system. This function becomes apparent at about 400 ns where the PL_CLK_pulses_per_BIT looks to recognize how many clock pulses are covered for the duration of one bit. The correct bit-locking occurs when L_CLK_pulses_per_BIT - 1 = PL_Bit_Repeat_Pulses.

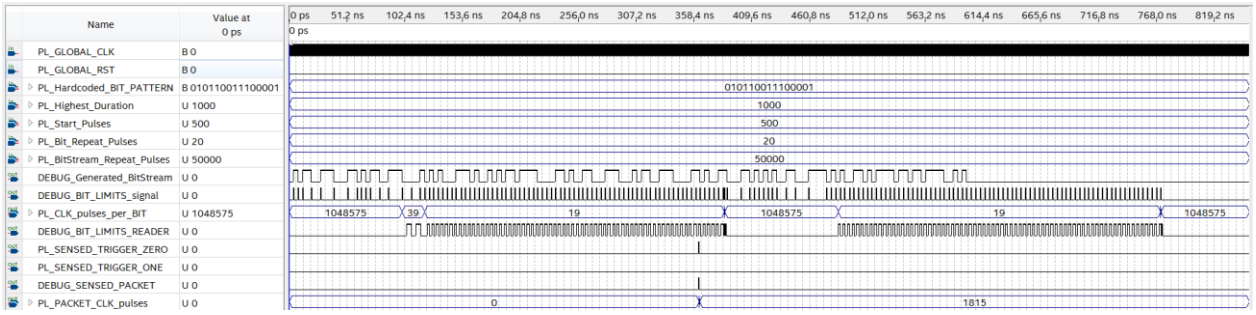


Fig. 111. Unable to identify all errors. The sequence resets due to high percentage of dropped packets.

This reset circuit works by taking into account the pulses between 15-bit packets combined with how many packets have been recognized in a reasonable amount of time. Specifically, the parameterization for the scenarios considered is sufficient for at least 3 recognized packets in an interval corresponding to 5, i.e. > 60 % packet sensitivity. Starting from Fig. 112 up to Fig. 116, the packet recognition results gradually increasing the tolerance to more and more errors every 15 consecutive bits.

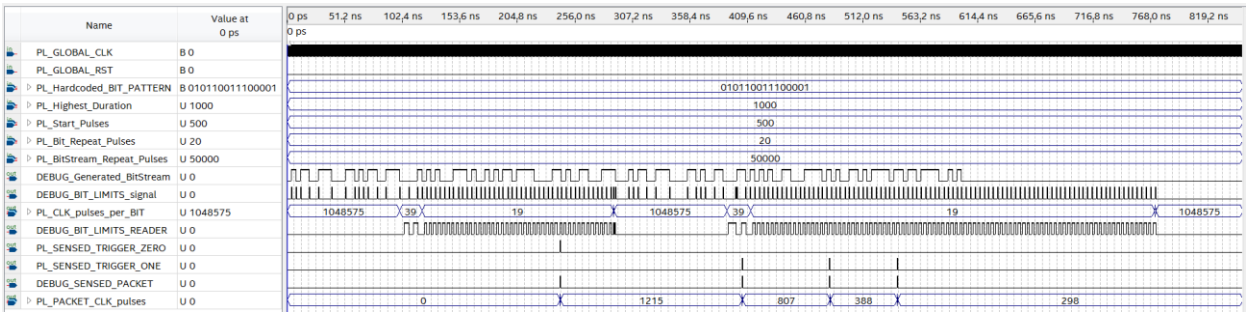


Fig. 112. Tolerance of at most 1 error in 15-bit sequences.

Next, the 15-bit register is configured (to check for the correlation of its bits to the 15-bit m-sequence signature) in such a way that whenever a packet is detected, it resets 14 of the 15 its bits (that is, those containing the 14 most recent values). This results in examining only the most recent 15 bits that precede a packet-lock occurrence. Otherwise, if the 14 bits of the register were not reset, all the intermediate (14 in total) consecutive sets of 15-bits would end up being examined with no reason. As expected, the new digital circuit that exercises a tolerance of 1 error at most, can correctly recognize 6 out of 8 bits and fails on the first and last one of the 8 15-bit sequences in total, as shown in Fig. 113.

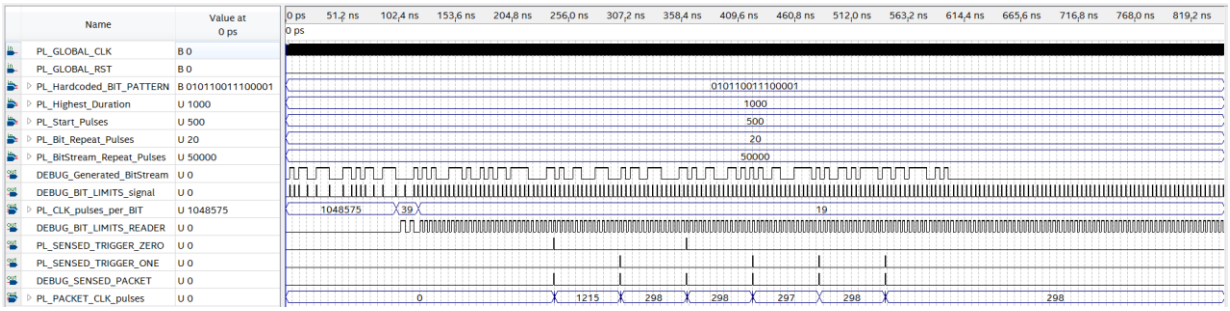


Fig. 113. The information is correctly identified as X 0 1 0 1 1 1 X.

Another simulation follows, shown in Fig. 114, where the updated circuit is parameterized to tolerate a maximum of 2 errors in the 15-bit packets. Here, the only packet that is not recognized correctly is the last one with a total of 3 errors at 15-bits.

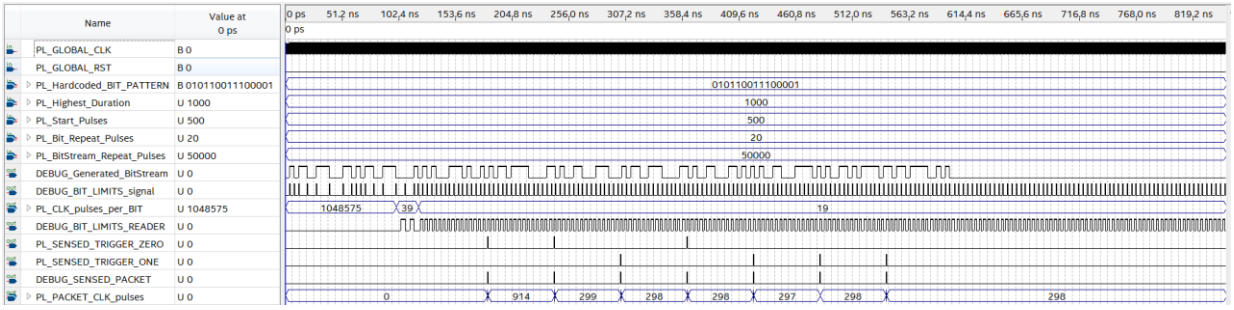


Fig. 114. The information is identified as 0 0 1 0 1 1 1 X.

Likewise, the update of the digital circuit that tolerates a maximum of 3 errors in the 15-bit packets, is shown in Fig. 115. In this case all packages are correctly recognized.

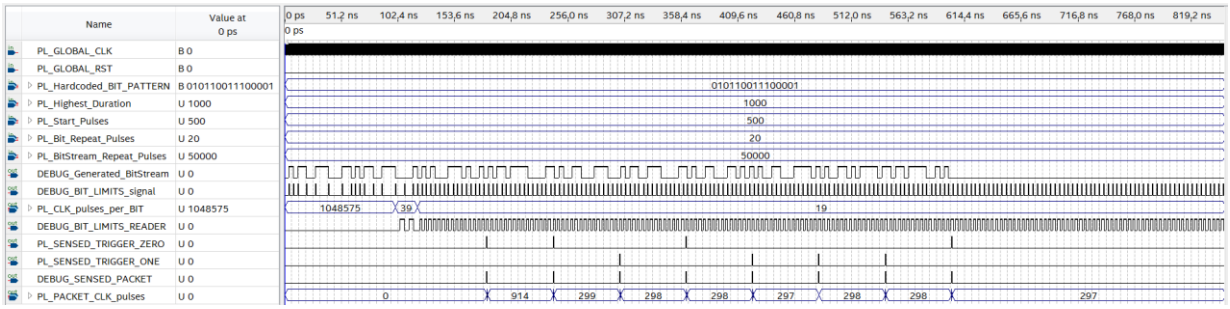


Fig. 115. The information is correctly identified as 0 0 1 0 1 1 1 0.

Finally, the same applies to a digital circuit that tolerates a maximum of 4 errors in the 15-bit packets, as shown in Fig. 116.

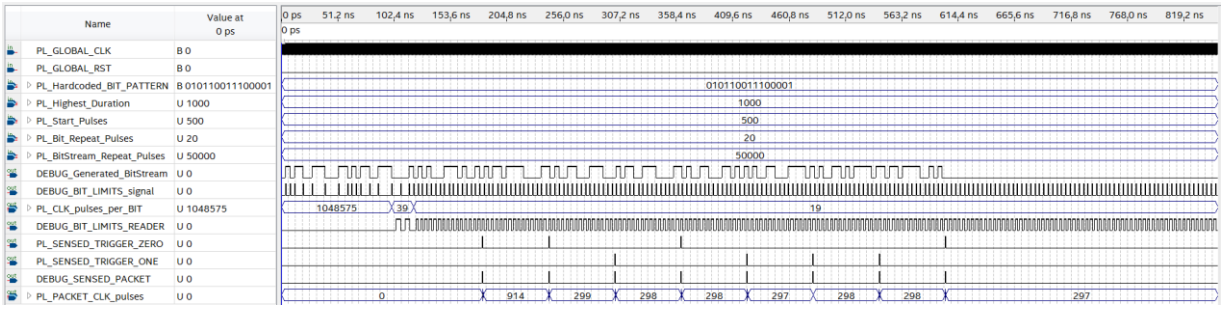


Fig. 116. The information is correctly identified (even in the case of 3 errors) as 0 0 1 0 1 1 1 0.

iii)Two-wire coding

A third alternative focuses on the bit-locking circuit while keeping the packet locking and the checks mentioned above, as is. This alternative concerns the use of 2 signals where, since the data is transferred with FSK, the first channel undertakes to transfer the information 'void' (silence) or 1 and the second channel 'void' or 0. In this way, a time gap is allowed between the 1 signal and the 0 signal, without this affecting the result.

The use of bit-locking is not required as both the duration of each pulse of the FSK signal and the silence interval of the channels can be varied without creating a problem in receiving the correct information. The error tolerances in this alternative implementation are much higher, the periodicity of the data is not required – although desirable – and the entire circuit is satisfied with the consistency of the signal sequence, so that it follows the analog 15-bit m-sequence, forward or reverse biased.

The graph in Fig. 117 illustrates the principle of the third alternative implementation.

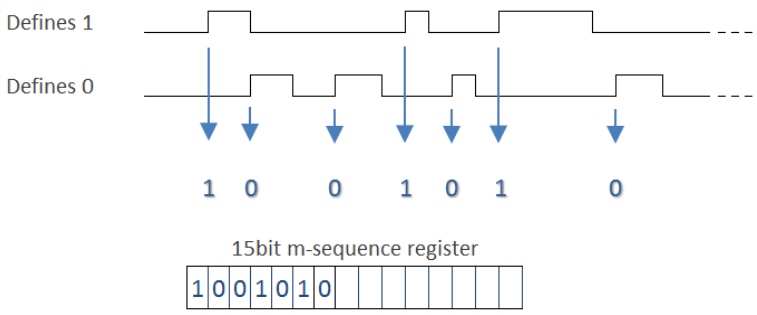


Fig. 117. Schematic illustration of asynchronous reception in two-wire coding.

Finally, the waveforms in Fig. 118 show a sequence version of the corresponding signals (FSK_IS_A_ONE and FSK_IS_A_ZERO) in the 30-bit register "o_data" (from left to right, i.e. from MSB to LSB).

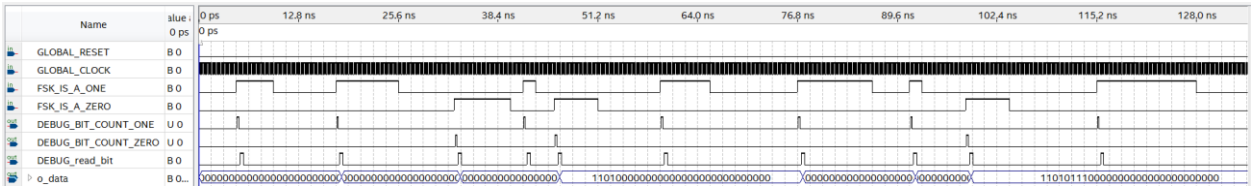


Fig. 118. Graph where the correct implementation of the two-wire coding logic is certified according to the values received by the "o_data" register.

5.4.4. Illustration of the Uplink-Downlink digital logic interconnection

The diagram of Fig. 119 depicts the general diagram of the uplink digital circuit of each PDTRM. This circuit has as inputs, the outputs of the previous unit while also taking into account the hardcoded PV cell ID as well as a possible external signal (reset of the DC/DC converter included in the power circuit of each module of the cascaded H-bridge converter) that defines the beginning of the power production.

The 'Reset sin' is a debug signal which was used during the development phase of the Uplink design to define the beginning of the pseudo-sinusoidal waveform generation. This signal was vital during the experiments where a pair of PDTRMs required to be re-synchronized in order to create the anticipated complex signal. The 'DC-DC converter reset' was regarded to function as a hard reset of the whole system. In later versions this input signal was substituted by the internal FSM operations, based on the data received by the downlink interface of each PDTRM.

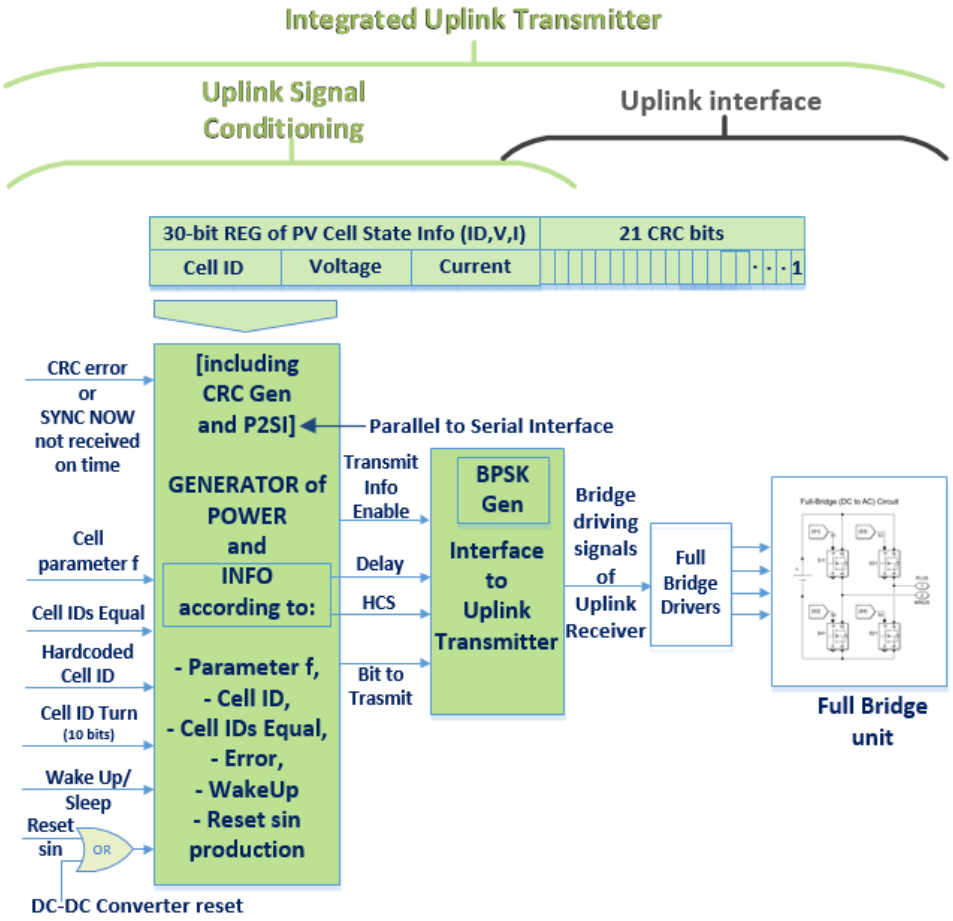


Fig. 119. General diagram illustrating the subsystems of the digital part of the uplink circuit and their logical interconnection.

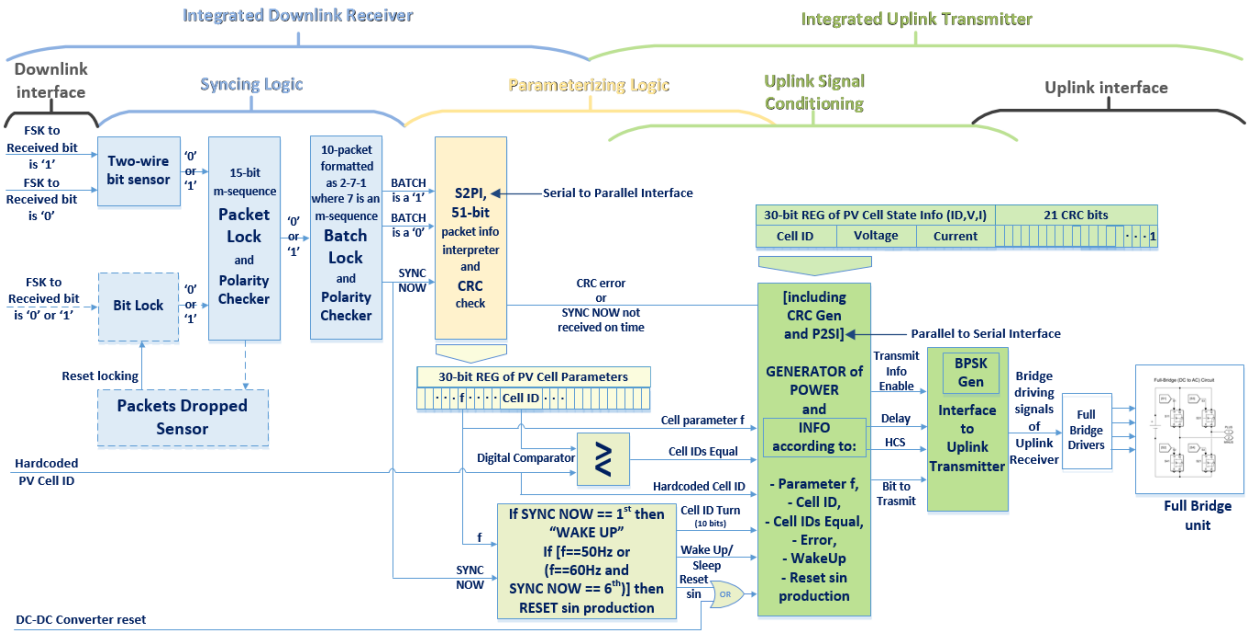


Fig. 120. General diagram illustrating the interconnection of the downlink and uplink digital circuits.

In this section, the mixed waveform containing the power signal component (to be contributing to the final pseudo-sinusoidal wave of the cascaded H-bridge converter output voltage) and the data signals are generated, which in turn form the driving control signals of the full-bridges of each PDTRM. The diagram of Fig. 120, depicts the interconnection of the communication and intermediate logic stages, illustrating the flow control which begins at the downlink reception modules on its left side and ends at the four power switches of the full-bridge arrangement (the uplink transmission interface) on its right side.

5.4.5. Design of the synchronization unit

The purpose of the synchronization unit is to mark the time point at which the uplink subsystem of each PDTRM starts sending data. Marking this time point correctly is important for smooth time-multiplexing communication. As already mentioned in § 5.4.4, the synchronization module, which is contained in each module of the cascaded H-bridge converter (PDTRM), ensures that the starting time point coincides in time for all modules. Also, with periodic repetitions, the same signal ensures that all units will maintain a common 'sense' of time.

The actual time for each unit is estimated relative to its clock pulses. However, it is certain that each unit faces a number of fabrication and operating conditions differences (e.g. due to ambient temperature variation between the modules of the cascaded H-bridge converter) when compared to the rest, resulting to slightly different operation. Therefore, the clock pulses of each unit change over time in a different way than the pulses of the rest, resulting to a difference in the clock pulse rate. Given sufficient time this may lead to differences in the perception of time. If this phenomenon is ignored then this difference will become large enough that the time deviation of the clocks of the PDTRMs will begin to cause errors both in the generation of alternating current and in the modulation and demodulation of the information signal.

Therefore, the synchronization principle serves a double role as it is aiming to define the starting time point of all units and to determine the intermediate time points at which all units will be able to zero their relative time deviations. This synchronization is triggered by the common point of reference of the system which is the RMCU, through the syncing commands of the Downlink channel.

The synchronization circuit which has been developed in this PhD thesis, serves so that each PDTRM knows what is the appropriate time interval within which it can and must transmit its information package, even if it is out of operation for a certain period of time, i.e. without enough power to maintain in some memory its operating state. Finally, since the synchronization signal is required to have periodicity but also to carry a strong digital signature for robustness against noise, this signature does both, by containing the parameterization information of the PDTRMs.

So, for proper synchronization, the common reference (the commonly accepted source of time information) is chosen as the RMCU, holding the responsibility of sending appropriate coded signals to be received by the operating PDTRMs. Whenever such a module gets enough power to begin operating, it keeps its output full-bridge drive on standby mode for as long as it does not receive proper information at its downlink receiver. When it recognizes (demodulates) the sync signal, it starts to decode the (1-bit) information it contains.

The RMCU module sends synchronization signals with a suitable configuration so that - in addition to the parameterization information - it becomes clear to the PDTRMs which pulse of these is considered as the start of the remaining 999 that will follow. Thus, each PDTRM, regardless of when it was set into operation, is able to know its order in relation to the others after one or more synchronization signals. To achieve this, it suffices to demodulate the information of each synchronization packet it receives in order to know whether this synchronization packet (or rather the present sequence of synchronization pulses) signals the beginning of the next thousand or not. If this packet marks the beginning of the next thousand then the PDTRM starts counting from that point on the new synchronization pulses it receives and compares this number with its hardcoded ID. As expected, the same counter is also reset to zero every time the PDTRM receives a sequence of pulses that marks the beginning of the next thousand. In this way, all PDTRMs, regardless of the random moment they are set into operation, they will all be able to start their normal operation 999 times the time that elapses between two synchronization pulses, at the latest.

The RMCU can configure the synchronization pulses in a suitable way so that the activation of the corresponding registers containing the 51-bit parameterization of the operation of the PDTRMs, coincides in time with the zero-crossing of the generated voltage, i.e. taking into account the frequency of the generated current (i.e. 50 or 60 Hz). By ensuring the above, the operation of any PDTRM that was shut-down due to low power can, in terms of

power generation, start much earlier than the anticipated passing of a thousand uplink transmission time-windows. This is enhanced by the fact that the periodicity of the power current is much greater than that of the information. In particular, the power generation can start in 3 or 18 periods of the power current (60 or 300 msec, depending on whether the generation concerns 50 or 60 Hz, respectively).

Until the unit starts normal operation so that it can receive sync signals (which it will then be able to decode and parameterize accordingly), the unit is designed to keep its full-bridge circuit in a non-disruptive state for the entire string, and this is the state it returns to if it can't diagnose a sync signal or if it detects communication errors that it can't fix. Thus, it is ensured that in case of faults, then the problematic unit will not affect the operation of the other units of the same string of the cascaded H-bridge converter.

In any case, the above will ensure that each PDTRM can know at all times how to drive its full-bridge power switches so that its coupling with the other PDTRMs on the common channel is seamless both for the power generation as well as information transmission.

Therefore, if for some reason a PDTRM is temporarily disabled e.g. due to intense shading of the PV cell(s) that it comprises it continues to allow the current flow of the remaining PDTRMs of the same string through the upper switches of the full-bridge which will continue to be in the ON state. When it is reactivated, it is reconfigured by the user-interface so that it can be recoupled into the group of PDTRMs that provide power to the string. So when the power of the unit returns to normal levels of proper operation (because e.g. there is no longer strong shading of the PV cells), this PDTRM will start to operate normally, i.e. its electrical circuit will produce the appropriate additional current and will start sending data about its state once it receives a sync signal again. The worst case scenario applies to the PDTRM with ID 999 which happens to "wake up" exactly on the "0" pulse that marks the beginning of the whole thousand, at which point it has to wait 999 more sync signals until it starts sending its telemetry data.

5.5. Experimental results

The experimental prototype depicted in Fig. 121 has been constructed for testing and verifying the developed downlink PLC method, according to the specifications shown in Table 5.2.

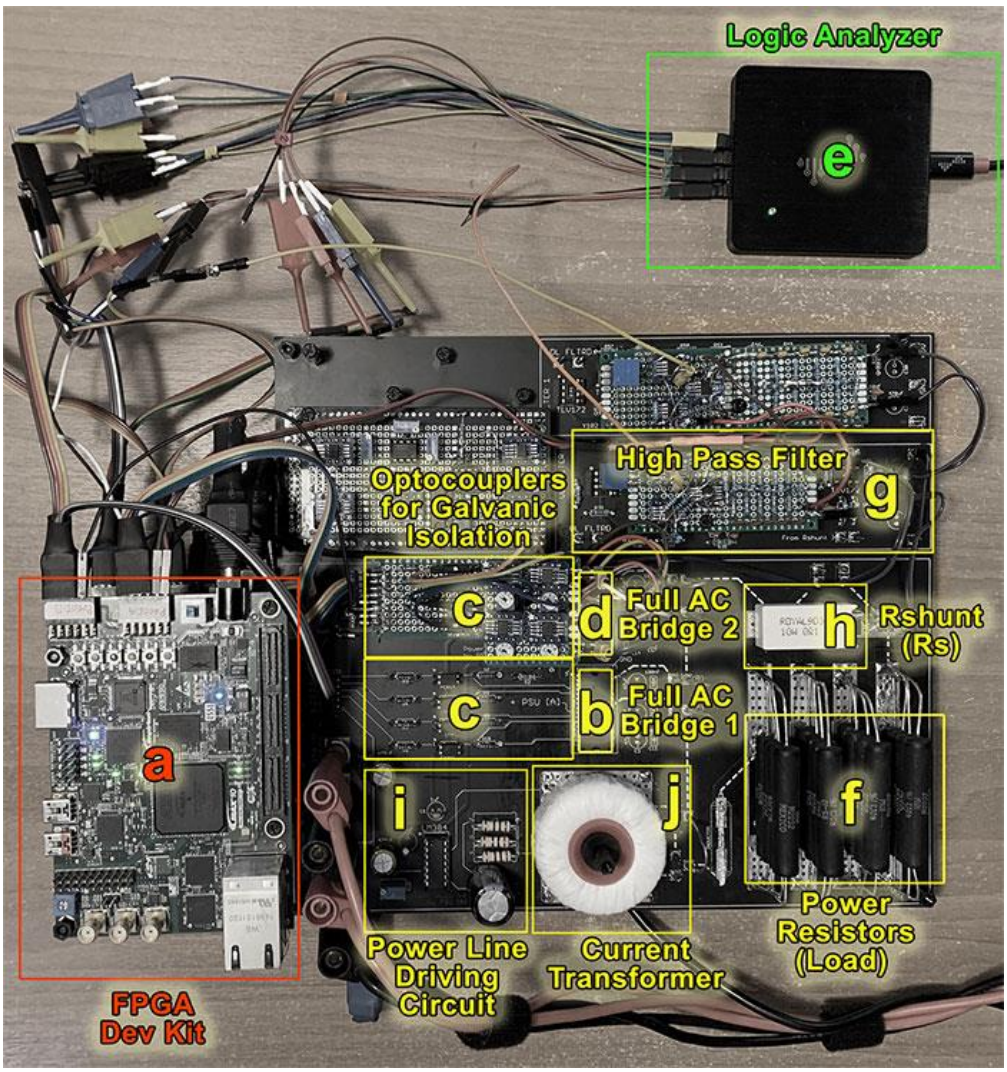


Fig. 121. The experimental prototype developed to verify the operation of the developed downlink PLC method.

The Altera chipset from Intel (10M50DAF484ES) serves as the foundation for the FPGA development board, designated as 'a' in Fig. 121. It includes the software code that was created using VHDL and synthesized to build the digital circuits for the RMCU and PDTRM control logic, or the data transmission and reception units, respectively. Its software synthesis and programming were carried out using Quartus Prime v18.1, and ModelSim v10.5b was used to simulate the functioning of the VHDL code.

For real-time monitoring and storing for the operational assessment and debugging of the whole system, a 16-channel logic analyzer, denoted as 'e' in Fig. 121, and a 2-channel digital oscilloscope were utilized. The PDTRM array is made up of two PDTRM H-bridges that are linked in series, denoted by the letters 'b' and 'd' in Fig. 121, together with a resistive load of 40 denoted by the letter 'f,' an L-C filter (L_f =400 µH and C_f =19.7 µF) at its output, and a resistive load of 40. The STGIPQ5C60T HL chip's inbuilt IGBTs make up each H-bridge. The

receiver's sensor, a 0.1 Ω shunt resistor (R_S), is denoted by the letter 'h'. The MCP6022 operational amplifier was used to construct the RCV front end designated 'g,' which has an HPF with a 284.2 Hz cut-off frequency.

When the PDTRM units are configured to create an AC output voltage and no data is broadcast over the power line, the experimental oscilloscope waveforms in Fig. 122 show the PDTRM string output voltage and data transmitter output signal (i.e., V_o and V_F, respectively, in Fig. 92).

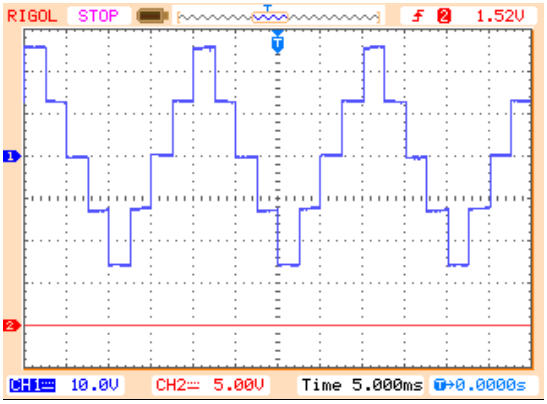
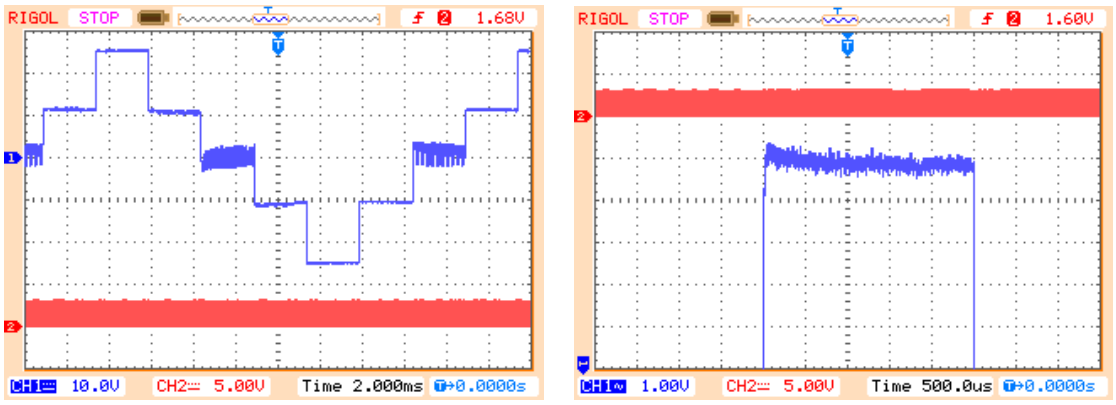


Fig. 122. Oscilloscope waveform of V_o (the two H-bridge PDTRM string voltage, channel 1, 10V/div, 5ms/div) and V_F (Channel 2, 5V/div) when the two PDTRM units are set to produce an AC voltage and no information is transmitted through the power cable.

Fig. 123 displays the waveforms of V_o and V_F when the PDTRM units are set to produce an AC output voltage and at the same time information is transmitted from the RMCU (Fig. 92) to the PDTRMs through the power cable. Fig. 123(b) focuses on a positive peak of the pseudo-sinusoidal AC signal shown in Fig. 123(a) to reveal the signal in detail.



(a) (b)

Fig. 123. Oscilloscope waveform of V_o (Channel 1, 10V/div) and V_F (Channel 2, 5V/div) when the two PDTRM units are set to produce an AC voltage and information is transmitted through the power cable: (a) at 2ms/div, (b) zoom-in view at 500us/div focusing on a peak of the AC signal.

Fig. 124 presents the corresponding waveforms of the transmitter signal injected into the power line and the signal developed at the receiver current sensor (i.e. V_T and V_{RS}, respectively, in Fig. 92).

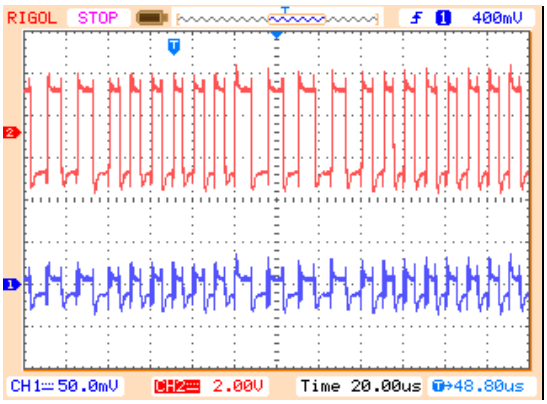


Fig. 124. Oscilloscope waveform of V_{RS} (Channel 1, 50mV/div, 20us/div) and V_{T} (Channel 2, 2V/div, 20us/div).

The corresponding spectral diagram of V_{RS} is depicted in Fig. 125 for the case that the two units of the experimental PDTRM array generate a pseudo-sinusoidal AC voltage and no data are transmitted over the power cable.

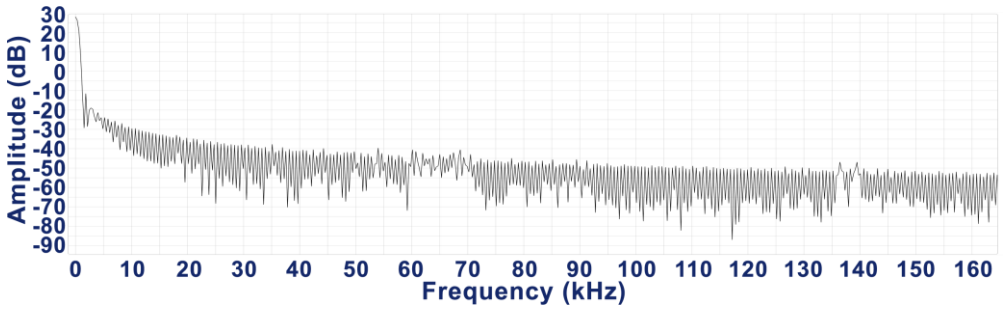


Fig. 125. The experimentally measured spectrum analysis of V_{RS} when no data are transmitted over AC through the power cable.

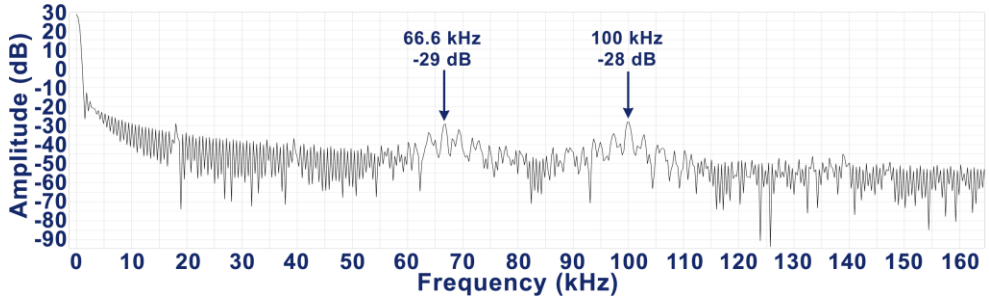
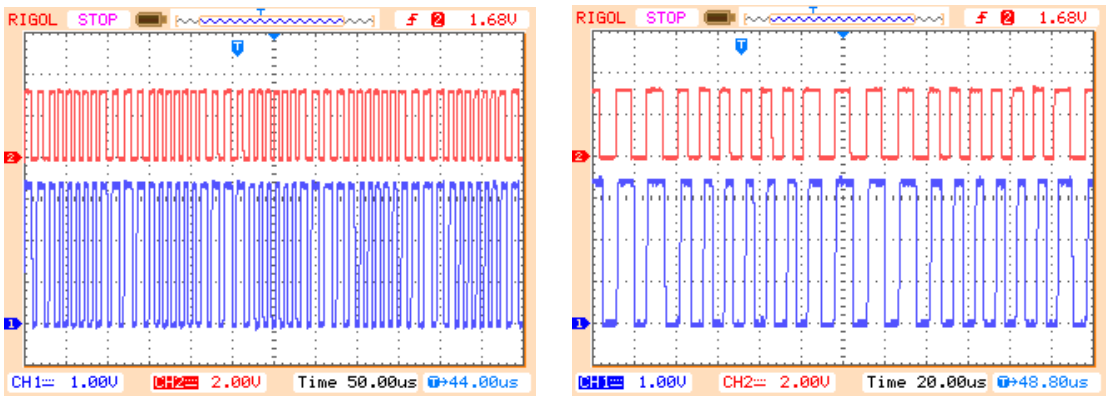


Fig. 126. The experimentally measured spectrum analysis of V_{RS} when data are transmitted over AC through the power cable.

A similar spectral diagram of V_{RS} is shown in Fig. 126 for the case that the two units generate the same AC power components while data is also broadcasted through the power cable.

The arrows point to the anticipated two main frequencies of the broadcasting carrier, with the first being at 66.6 kHz (-29 dB) and the second at 100 kHz (-28 dB).

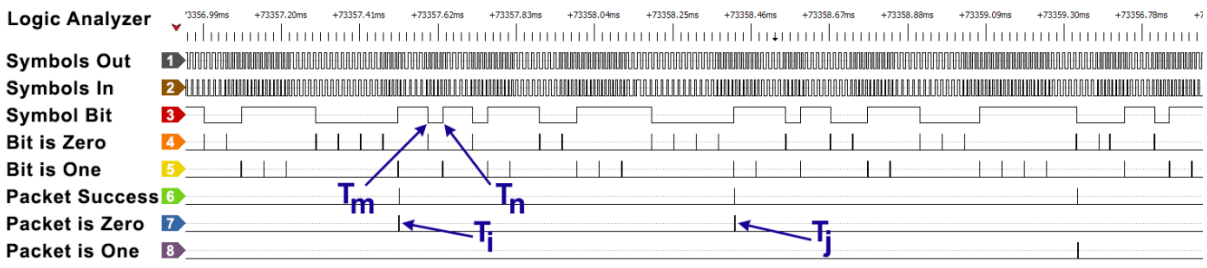


(a) (b)

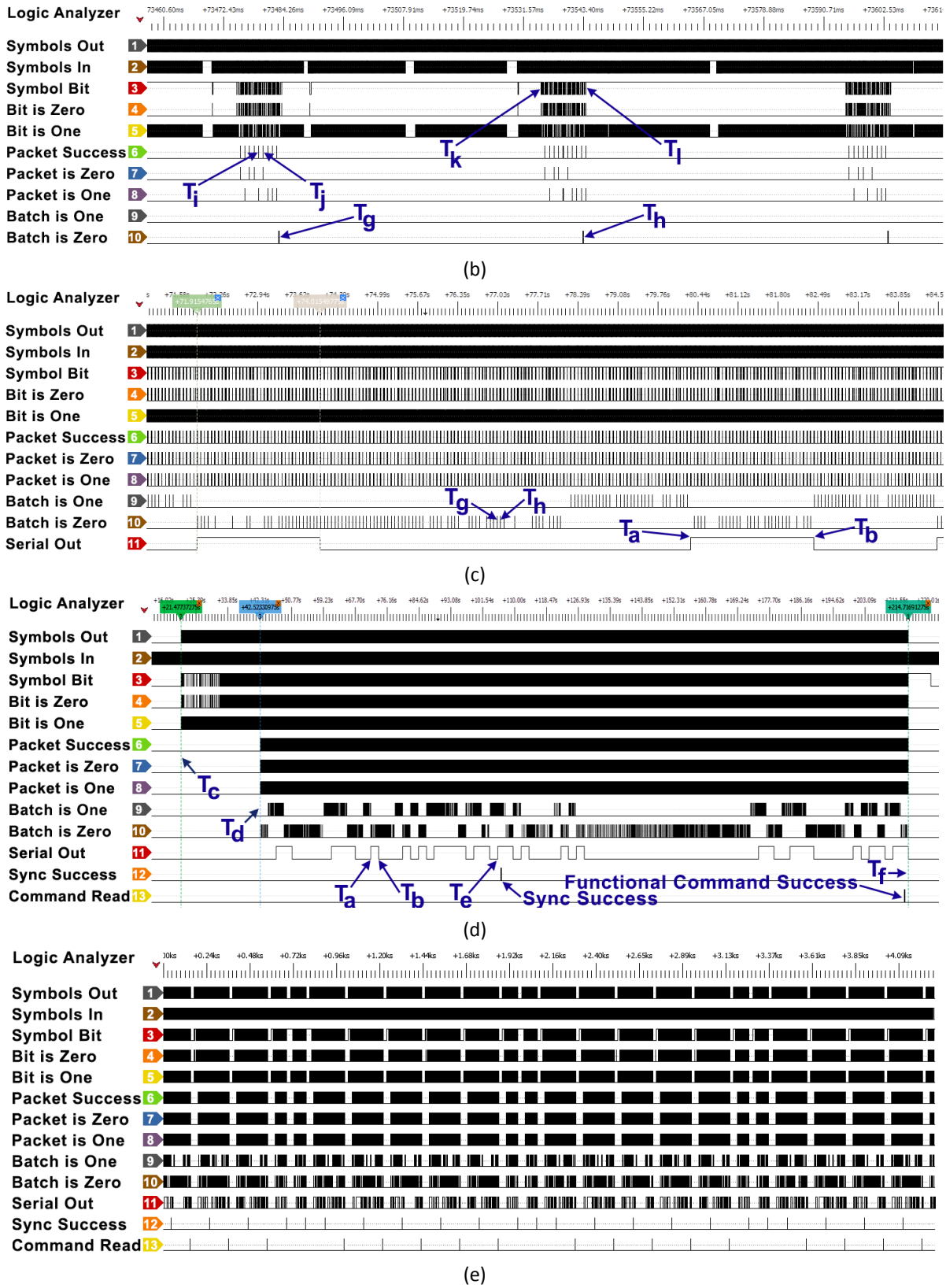
Fig. 127. Oscilloscope waveform of V_S (Channel 1, 1V/div) and V_F (Channel 2, 2V/div) with the application of FSK at 66.6 kHz and 100 kHz for 60 μsec per symbol: (a) at 50μs/div, (b) at 20μs/div.

The successful operation of the PDTRM receiver front-end is depicted in the similarities of the waveforms of V_S (i.e., the RCV front-end output voltage in Fig. 93) and V_F (i.e., the transmitter output voltage in Fig. 92) as illustrated in Fig. 127.

In order to verify the successful transfer of information from the RMCU to the PDTRMs of the cascaded H-bridge converter through the power cable, Fig. 128 illustrates five timeline graphs which gradually zoom out, aiming in a detailed presentation of all the layers of the decoding progress from the LLBs up to the HLBs and the synthesis of the configuration commands.



(a)



(b)

(c)

(d)

(e)

Fig. 128. Logic analyzer experimental waveforms of the PDTRM receiver digital subsystem, which present the successive synthesizing of the received demodulated bitstream into bits, packets, batches, commands, and proper responses to these commands: (a) bit series and packet detection, (b) packet series and batch detection, (c) batches and effective bits, (d) effective bits that form a sync and a functional command, (e) successful reception of a series of 40 commands (23 sync and 17 functional).

In these waveforms, the 'Symbols Out' illustrates the digital transmitter output voltage, V_F, and 'Symbols In' the voltage V_S, which enters the PDTRM receiver back-end interface (Fig. 93).

The signals 'Symbol Bit', 'Bit is Zero' and 'Bit is One' are used for debugging and demonstrating purposes. As shown in Fig. 128(a), all symbols are successfully demodulated into LLBs (bits). Each LLB has a duration of T_n-T_m = 60 μsec. In the same figure, the signals 'Packet Success', 'Packet is Zero' and 'Packet is One' are used to debug and demonstrate the successful decoding of the 15-LLB streams into packets that represent a medium-layer bit (MLB) of 0 and 1, respectively. The T_i and T_j time markers measure an MLB duration that is calculated as T_j-T_i = 900 μsec. In a wider view, Fig. 128(b) presents the signals 'Batch is Zero' and 'Batch is One', which verify the successful decoding of a 10-MLB stream into a batch that represents either a bit 0 or 1, in a similar fashion to what has been already described for the layer of packets.

The time markers T_i and T_j are used for reference to the previous image. The time markers T_k and T_l measure the duration of an HLB (batch) to be T_l-T_k = 9 msec. The time that mediates between two successive HLBs is periodic, as designed. It is measured by the time markers T_g and T_h as T_h-T_g = 60 msec. The 51 msec in between have been committed to occupy space for the optional realization of communication for the transmission of information from the PDTRMs to the RMCU. Zooming out, Fig. 128(c) reveals that some of the HLBs (shown by the aperiodic spikes of the signals 'Batch is Zero' and 'Batch is One') are missing. This is due to errors attributed to power line noise, which has been alleviated by repeating the HLBs (here, 35 times) to ensure that at least one HLB will be successfully received during that time. A stream of HLB repetitions constitutes the effective HLB, or eHLB, which, as shown by the time markers on the 'Serial Out' signal, has a duration of T_b-T_a= 35×60 msec = 2.1 sec. For the worst case of burst errors shown in Fig 128(c), the receiver fails to decode 4 successive HLBs. The missing spikes can be spotted on the right side of the time markers T_g and T_h. The worst case of burst errors was experimentally measured to be 6 successive HLBs. Although this suggests that a receiver with an eHLB = 7 HLBs (i.e. a baud rate of 2.38 bps) would be sufficient to decode all commands without any errors, a much higher value was selected to minimize the burst error risk.

The formation of a syncing and a functional command side-by-side is shown in Fig. 128(d). The 'Serial Out' signal hosts the actual eHLBs that form these two commands. The

time markers T_a and T_b pinpoint one of these bits, as a reference to Fig. 128(c). The time markers T_c and T_d indicate the beginning and the end of the symbol patterns that assist the locking mechanisms described in § 5.3. The first pattern is the repetition of a narrow-pulse BSWO for (T_d-T_c)/2 = 10.5 sec and the second pattern is the alternating narrow-to-wide pulse BSWOs, also for (T_d-T_c)/2 = 10.5 sec. The time T_d-T_c is equivalent to 10 eHLBs by design. The lock assisting patterns are preceded by a broadcast silencing period. By convention, this period was chosen to be an additional T_d-T_c = 10.5 sec (a time equivalent to 10 more eHLBs). A syncing command is 31 eHLBs wide, and a functional command is 51 eHLBs wide. In this way, all commands are equivalent to 51 eHLBs which simplifies the command issuing on the RMCU. The time markers T_d and T_e pinpoint the beginning and ending of a syncing command. The functional command begins at the time instant marked as T_e and completes at T_f. Every command lasts for 51×2.1 = 107.1 sec, so here a 'Wake' command followed by a functional command has a duration of 214.2 sec. This time satisfies the 4-minute limit as analyzed in § 5.3.7, for the scenario where all PDTRMs are required to transmit their data back to the RMCU.

As a best practice, every functional command was preceded by a synching command in this work for demonstration purposes. This, however, is not required by the PLC protocol, which has been developed, for the general case. The successful reception by the PDTRM of the cascaded H-bridge converter of all commands transmitted by the terminal device through the power cable is verified by the short duration pulses presented in the signals 'Sync Success' (for both 'Sync' and 'Wake' commands) and 'Command Read' (for the Functional commands), shown in Figs. 128(d) and 128(e).

6. Design for enhanced robustness and verifiability

6.1. Introduction

This chapter presents the controllability enhancement techniques that have been incorporated into the digital control and monitoring unit of the PDTRMs in order to facilitate the debugging of the overall system, to enhance its robustness, and to confirm its correct design and proper operation.

6.2. The operating principles of the techniques applied

This section presents the operating principles of the techniques for increasing the controllability of the circuits of the control and monitoring unit of the PDTRMs, which were applied during its design in order to confirm its correct design and operation. The general trend in increasing controllability is based on the use of Built-in Self-Test (BIST) techniques, whereby the Circuit Under Test (CUT) is modified.

6.2.1. Embedded off-normal and within normal self-test techniques

A built-in off-normal self-test technique is used to check the circuit when it is not operating. These techniques can be used either for manufacturing testing, or for periodic testing, field testing, but in this case the unit under control must be taken out of operation. In-circuit self-testing of a Circuit Under test (CUT) with an out-of-normal on-board self-test technique, requires a Test generator (TG) with an input multiplexer (mux), a response compression unit output (Response Verifier, RV) and a control unit (control) to coordinate the verification process of correct design and operation [111].

Built-in self-test techniques within normal operation utilize system-specific behaviors or intrinsic properties of the circuit which are exploited in ways that can enhance the overall robustness. This is realized by creating self-diagnostic circuits that are dedicated in readjusting various aspects of the system's design parameters in order to guarantee that its output(s) will always create the anticipated response. The paragraphs to follow describe the

built-in self-test techniques within normal operation that were used in the framework of this PhD thesis.

6.2.2. Proper carrier locking and reading of bits

One of the most basic techniques to increase controllability in the transmission of information carried out by the control and surveillance unit of the PDTRMs, was implemented with the aim of identifying errors related to the reading of the symbols transmitted from the RMCU by the downlink interface of PDTRMs. This technique is based on pattern recognition in order to facilitate the distinction between the two symbols on the one hand and to locate with one clock cycle precision the beginning and end of each symbol. This technique enhances the proper control operation of the symbol reading circuits by adjusting the appropriate starting position of the reading process.

6.2.3. Correct packet reception

Following the above procedure, in the first experimental versions of the control and monitoring unit of the PDTRMs, a second check was applied that examined whether the most recent symbols period was estimated correctly and whether their starting points had been precisely recognized. This circuit continuously checked if a sufficient percentage of accumulated data (specifically 15-bit packets) could be interpreted in terms of their contents. If not, the logic of symbol recognition and locking for proper reading was restarted and the locking process was re-initiated.

In the final design of the RMCU, this technique is facilitated by interposing a downlink mute time to help the aforementioned symbol reading circuit to restart after a predetermined time (about 60 msec). Also, the control logic that triggers a reset in case a large percentage of erroneous data is accumulated, is used in the layer that estimates the number of high-level (HL) bits being received. This is programmed to reset the whole process if a time greater than the duration of three HL bits elapses, which corresponds to a duration of 9 msec, but since each HL is a fixed time apart from the next (either 180 msec or 9 sec, depending on the rate setting), this may take from 387 msec to 18027 msec. This check helps in debugging, as the designer can reason that the constant resets may be due to errors related to noise, and also enhances the robustness of the receiving end. This digital logic ensures that the interpretation of an instruction will not freeze before completion, like for example in the

event of a malfunction during synchronization. Instead, the instruction will be ignored and discarded without affecting the reception of the subsequent HL bits.

6.2.4. Enhancing verifiability through m-sequence encoding and sync commands

In the communication system of the PDTRMs developed in the framework of this PhD thesis, the sending and receiving of information is carried out through the power line conductors that are conventionally intended for the transfer of power. However, the square waves of the uplink/downlink transmission processes may also contain high-amplitude harmonics, as well as electric noise, which reduces the reliability of the data transmission. For this reason, an appropriate coding was chosen, both in the downlink and uplink communication protocol, formed according to specific sequences of bits, modulated in FSK and R-PAM, respectively. For the downlink transmission, the increase in the verifiability of the relevant circuits of the control and surveillance unit was implemented through the use of m-sequences, while for both the downlink and the uplink transmissions it was implemented with the addition of CRC Checksum.

More specifically, during the transmission of information through the downlink interface of the RMCU, the symbols (low-level bits) follow one of the two appropriately selected 15-bit m-sequences, complementary to each other, to define the (mid-level) bit 0 or 1. This tactic increases the verifiability of correct design and operation of the digital circuits that read this information, as it makes it easier to check and then discard any sequence of symbols that does not match these two 15-bit standards. The same tactic is applied to the next level, where the 15-bit m-sequences (mid-level bits) must follow in turn one of the two appropriately chosen 7-bit m-sequences, also complementary to each other. These two m-sequences make up the HL bits.

As a reminder, the mentioned 7-bit m-sequences are contained in a 10-bit batch where the first 2 mid-level bits are called Head, the following 7-bits are called Payload and the last 1 mid-level bit is called Tail, with the Payload being the recognizable, by the corresponding control circuit, m-sequence. Among the 10-bits of the batch, the first two (Head) are the ones that, with the information they contain, serve the circuit that recognizes the symbols (low-level bits) to lock through constant checks the reading at the right time. By implementing this coding, it was possible to confirm the correctness of the received data (and therefore check the correct design and operation of the corresponding circuits), as otherwise even sporadic errors due to noise would lead to mediocre decisions as to the identity of

corresponding mid-level bits. The use of robust sequences with low-autocorrelation makes it easier to confirm the correct design and operation of the circuits that recognize the encoding of each mid-level bit.

Finally, the same tactic is applied to both special synchronization commands which, due to their nature, require checking mechanisms to confirm their correct reception, since a wrong interpretation of their content would desynchronize the entire communication system. These control mechanisms were also used to check and confirm proper operation of the corresponding circuit design of the control and surveillance unit. The first of the two (syncing) commands is responsible to define the exact time point that a parameterization command (functional command) begins, while the second one is responsible to define the time point that the available information transmission time window of the PDTRM with hardwired ID = 0 begins. The synchronization commands consist, by extension of what has been mentioned, of 31 high-level Bits which strictly follow one of two appropriately chosen m-sequences (also complementary to each other) with the first one concerning the synchronization of the 51 bit functional commands and the second one the synchronization of the 1000 time windows (during which the uplink subsystem with the corresponding hardwired ID is allowed to transmit). The synchronization commands increase the controllability of the respective communication layers of the control and monitoring unit of the PDTRMs by offering the possibility to confirm the correctness of the data to be identified.

6.2.5. Enhancing robustness by including CRCs

In continuation to what has been mentioned about the verifiability of the levels of the control and surveillance unit which collect and form the parameterization information through the downlink, especially for the functional commands, a 21-bit CRC checksum is added. The functional commands consist of 51 bits, of which the first 30 carry the useful information while the following 21 constitute the CRC checksum of the first 30. The goal is to check the correct operation of the subsystems for receiving the parameterization information, since according to this implemented mechanism, any emerging error during the transmission of information, is detected and either corrected automatically (if it is an HL-Bit error) or not corrected (if there are more than one HL-Bit errors). In the second case, any transmitted command is not accepted by the communication subsystem of the respective PDTRM and its operation remains unaffected.

The same technique has been applied for verification purposes on the RMCU side. This is why the transmission of the information sent by the uplink subsystem (51-bits of which the last 21-bits concern the checksum of the first 30). The 21-bit CRC polynomial chosen is common to both cases and is considered the best available 21-bit CRC, as it exhibits the largest Hamiltonian distance under the assumption of a low and stable random and independent BER (bit error rate).

6.2.6. Embedding a pre-set downlink transmitter

Another key technique to increase the verifiability of the designed control and monitoring unit is to reproduce and then directly implement the commands generated by the RMCU, so as to allow the control of the receiver logic, and the rest of the demodulation systems, free from intermediate problems that may occur during the data transferring in the communication channel (power lines) of the downlink transmission. This was performed by inserting a downlink transmitter module and by adding a suitable 1-bit input, which gives the downlink receiver module the option to receive data either from the built-in downlink transmitter, or from the external link as provisioned in the prior design. The same technique allows the simultaneous control of the subsystems of the external experimental downlink transmitter since it also uses the same units based on the same composition and the same operating principles with the only difference regarding its parameterization.

The built-in (embedded) downlink transmitter contains pre-defined test commands, which have been purposefully selected to examine the main features of the system's functionality. A suitable 1-bit input is provided from which the end-user can choose whether to sequence the test commands periodically, one after the other, in a loop, or to switch them at specific times chosen (manual override). In this case, the manual change of instructions is applied once a positive edge is given to the signal of the given input, at which point the mode changes, starting with the first instruction, and continuing by issuing the next instruction on every new positive edge introduced by the user.

6.2.7. Circuit auditing the data to be sent to the RMCU

In order to implement a similar technique to increase the verifiability of the 30-bit data available to be sent by the last stage of the uplink transmission, corresponding to the previous ones, an appropriate multiplexer (MUX) was added. This MUX selects, based on the input bits

"Uplink mode 0" and "Uplink mode 1", among the choice of sending the hardwired ID and the real-time values obtained by the sampling circuits (samplers) of the measurements of the sensors V-to-F and I-to-F (to measure the voltage and the current, respectively), or by three more prefixed-value choices. Thus, the four different cases have the following form:

- hardwired ID, real time voltage, real time current

  or one of three predefined pairs:
- prefixed ID 1, prefixed voltage 1, prefixed current 1,
- prefixed ID 2, prefixed voltage 2, prefixed current 2,
- prefixed ID 3, prefixed voltage 3, prefixed current 3.

6.2.8. Segmentation and reassembly of modular subunits

Aiming to increase the verifiability of the individual units that will be included in the final digital system and at the same time to speed up debugging during the previous stages where intensive design is performed, the technique of segmenting the overall system into 5 individual sections (sub-units) was chosen. The segmentation was done appropriately, so as to reduce the set of required signals that will interconnect the 5 subunits with each other. At the same time, these signals offer characteristic data for the investigation (and eventual debugging) of the correct design and operation of each subunit. Fig. 129 shows the top-level layout of the digital system (revealing all of the main subsystems) where the composition of 6 sub-systems (the green parts) can be distinguished, of which 4 are the main ones as they concern the Downlink, Uplink, MPPT/Reg and FSM units.

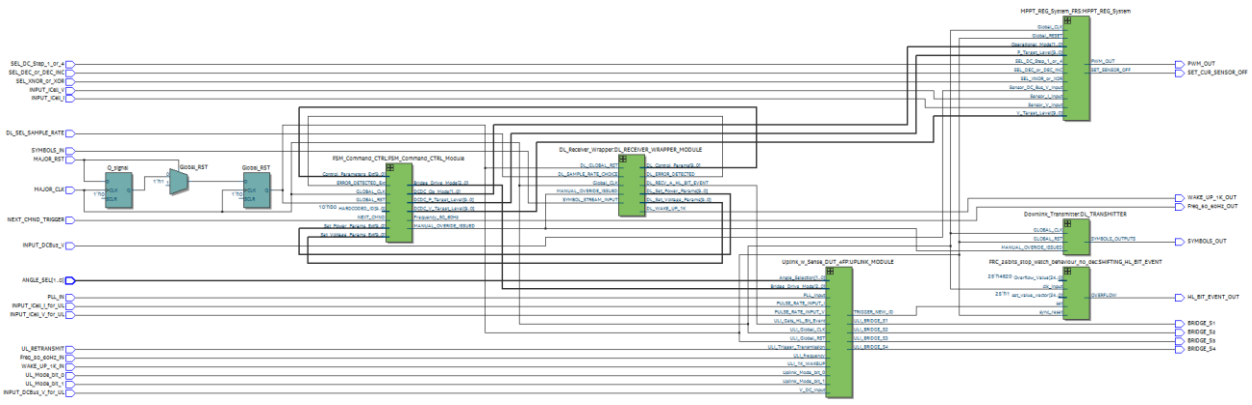


Fig. 129. The RTL model of the composition of the parts of the control and monitoring unit of the modules of the cascaded H-bridge converter.

One of the other 2 green blocks on the lower right corner of Fig. 129 depicts an internal downlink transmitter (implemented for debugging purposes) which operates independently

from the rest of the system. The 6th block on the right next to the downlink transmitter concerns a counter that aims to time shift a signal, and more specifically a signaling indication of the correct reception of a high-level (HL) Bit from the downlink subsystem, so that it is applied at the right time. This is important as it adjusts the uplink transmission synchronization accordingly, by receiving information from the downlink transmission process. In short, this block sets the timings of the uplink time-windows allowing for the proper full-duplex broadcasting on the common communication channel.

Fig. 130 depicts the block diagram of the register-transfer level model shown in Fig. 129, depicting the signals used in the blocks' interconnection.

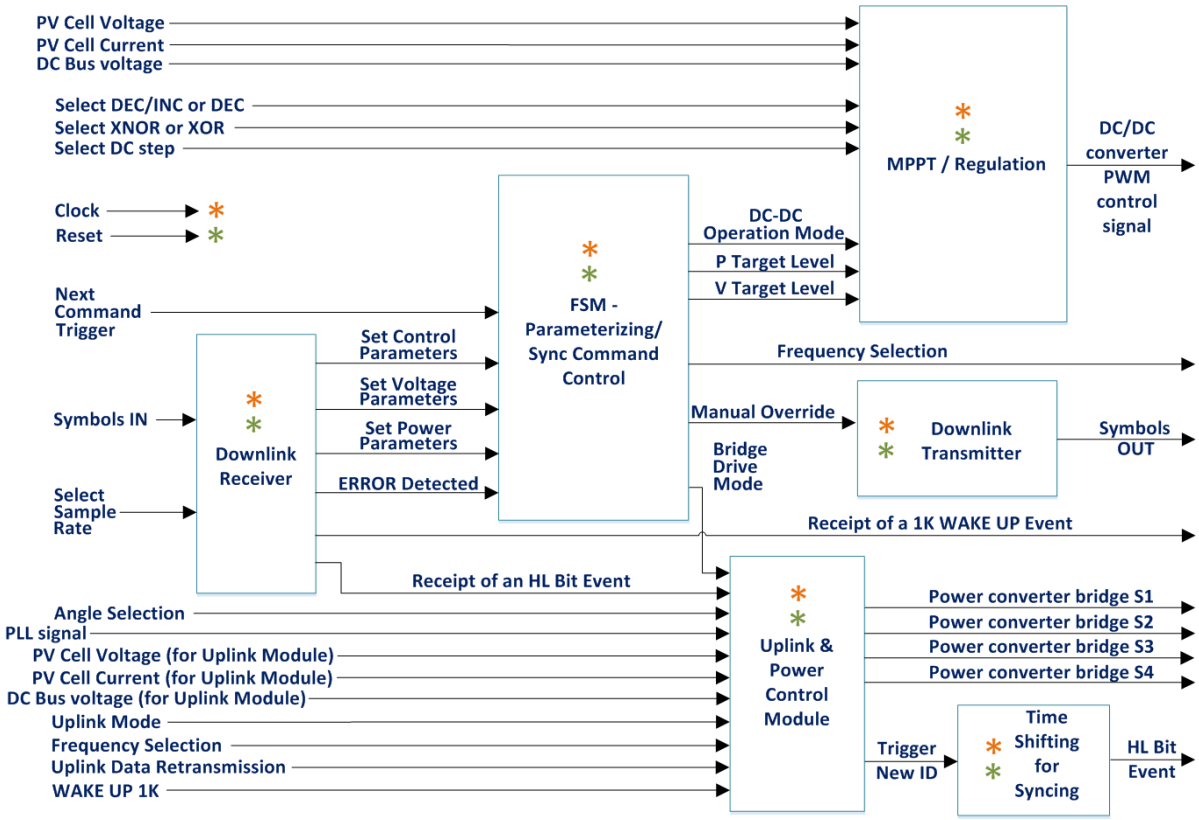


Fig. 130. The general diagram of the implemented control and monitoring unit architecture, with the illustration focus paid on the input/output signals of the respective blocks.

The system as a whole consists of 20 inputs and 7 outputs (22 pins and 10 pins, respectively), of which 14 inputs including the RST signal and 4 outputs which are added to be exclusively used for increasing the controllability of the aforementioned units.

In Table 6.1 below, the names of the inputs and outputs (I/O) of the system are presented in detail, as shown in Fig. 130, highlighting the ones that mostly enhance the controllability of the system, in yellow, green and orange.

The orange color refers to the common reset of the system, which is practically used during the process of experiments and debugging and is normally not required as an input, since the system is designed to perform an automatic reset (auto-reset) after a given period of time that will has been supplied with the required power to operate.

Table 6.1. Inputs and outputs of the overall digital system of the control unit of the modules of the cascaded H-bridge converter (in highlight those that increase controllability).

Inputs	Outputs
1. MAJOR_CLK (1-bit signal)	1. PWM_OUT (1-bit signal)
2. MAJOR_RST (1-bit signal)	2. SET_CUR_SENSOR_OFF (1-bit signal)
3. Freq_50_60Hz_IN (1-bit signal)	3. SYMBOLS_OUT (1-bit signal)
4. WAKE_UP_1K_IN (1-bit signal)	4. WAKE_UP_1K_OUT (1-bit signal)
5. UL_RETRANSMIT (1-bit signal)	5. HL_BIT_EVENT_OUT (1-bit signal)
6. ANGLE_SEL (2-bit signal)	6. Freq_50_60Hz_OUT (1-bit signal)
7. PLL_IN (1-bit signal)	7. Outputs S1 to S4 (4-bit signal)
8. UL_Mode (2-bit signal)	
9. INPUT_iCell_V_for_UL (1-bit signal)	
10. INPUT_iCell_I_for_UL (1-bit signal)	
11. INPUT_DCBus_V_for_UL (1-bit signal)	
12. NEXT_CMND_TRIGGER (1-bit signal)	
13. SYMBOLS_IN (1-bit signal)	
14. DL_SEL_SAMPLE_RATE (1-bit signal)	
15. INPUT_iCell_V (1-bit signal)	
16. INPUT_iCell_I (1-bit signal)	
17. INPUT_DCBus (1-bit signal)	
18. SEL_XNOR_or_XOR (1-bit signal)	
19. SEL_DEC_or_DEC_INC (1-bit signal)	
20. SEL_DC_Step_1_or_4 (1-bit signal)	

The yellow color refers to signals that have been added to increase the verifiability and controllability of the main blocks (modules) of the overall system of the control and monitoring unit of the PDTRMs.

Finally, the green color refers to output signals which are able to provide feedback to the corresponding inputs, thus allowing the control of subsystems even if the outputs do not produce the expected results or the control of subsystems in the case that special scenarios are considered, in order to check the response of the system to the corresponding conditions (e.g. extreme conditions or commands that have not been provisioned in the given design).

The 'SYMBOLS_OUT' output is intended to be connected to 'SYMBOLS_IN' when using the built-in downlink transmitter. Otherwise, the 'SYMBOLS_IN' output receives the downlink information directly from the corresponding external link (i.e., the output of the corresponding high-pass filter).

The output 'WAKE_UP_1K_OUT' is connected to 'WAKE_UP_1K_IN' and the signal it carries is necessary to indicate to the system that an appropriate command has been received, allowing it to start its operation. This also shows why the expression 'wake up' has been used. The "1K" refers to the indication that at this time point the beginning of the time-window (during which the PDTRM with hardcoded ID = 0 can transmit data) is defined. Subsequently, the same signal defines the timings of all 999 PDTRM o follow, which will be able to transmit data in a sequential fashion, every 60 msec, from that point onwards. The voluntary use (or lack of use) of this signal at given time intervals serves for functional checks and error diagnosis of the associated subsystems of the control and monitoring unit of the PDTRMs.

The output 'Freq_50_60Hz_OUT' is connected to the corresponding output 'Freq_50_60Hz_IN' and aims to set the value of the frequency of the current produced by the corresponding driving circuit of the DC/AC full-bridge of the power converters of the PDTRM. As before, the at-will use (or lack of use) of this signal at given time intervals serves for functional checks and fault diagnosis of the associated subsystems of the control and surveillance unit. For example, checking this control bit when sending commands that cause the given control bit to change ensures that the intermediate circuits recognize all 51-bits correctly, and thus have 'locked in' to the correct command and thus all systems synchronization function, as desired.

Finally, the 'HL_BIT_EVENT_OUT' output is connected to the corresponding 'UL_RETRANSMIT' and is used to define (schedule) the rate, and the exact time points, of information transmission from the uplink interface to the RMCU. The names indicate that whenever the downlink receiver recognizes an HL-Bit, it outputs a positive edge for a few clock cycles, which, depending on whether the on-board transmitter is used or not, is shifted appropriately (from the 6^{th} block mentioned in Fig. 129) to be received from the 'UL_RETRANSMIT' input. This input recognizes when it receives this positive edge that signals the appropriate time for starting the subsystem that expects to transmit the 30-bit information to the uplink, although only if the given time period coincides with the one corresponding to in transmission for the PDTRM with the given hardcoded ID. The fact that the given bit is available for inspection offers the possibility of confirmation (or debugging) the expected sequence of demodulation and decoding of the data, as well as testing the

imposed synchronization rate of the uplink module through the downlink interface, while increasing the verifiability of the operation each of these two units separately.

What follows below is an elaborative description of the role (and use and features per case) of the I/O presented in Figs. 129 and 130.

Inputs:

- **MAJOR_CLK (1-bit signal)**
  Main system clock input: 2.0 MHz clock.
- **MAJOR_RST (1-bit signal)**
  General Reset (Active High).
- **Freq_50_60Hz_IN (1-bit signal)**
  Signal indicating the frequency of the power signal to be generated (0 means 50 Hz, 1 means 60 Hz).
- **WAKE_UP_1K_IN (1-bit signal)**
  As long as this signal remains zero the full-bridge signals are shorted to allow current to bypass the PDTRM(in series). When this signal becomes 1 the full-bridge signals start operating normally to generate power and transmit information.
- **UL_RETRANSMIT (1-bit signal)**
  If a 1 is received at this input, then the information available for sending from the respective uplink registers is (re)transmitted. In the event that the feedback of this input is selected from the corresponding 'HL_Bit_EVENT_OUT' output of the system, the appropriate moment of sending the information is practically defined immediately after the successful recognition of receiving a high-level bit by the receiver, as mentioned in § 5.4.1. In order to allow sending, it is not enough that this input becomes 1, but that a 1 has been received at least once from the 'WAKE_UP_1K_IN' input, as well as that the hardwired ID of the given PDTRM matches the ID it is expected to transmit in the current time window.
- **ANGLE_SEL (2-bit signal)**
  Selects 1 of 4 presets of the firing angle of one of the two pairs of the full-bridge power switches (e.g. MOSFETs)..
- **PLL_IN (1-bit signal)**
  The signal sampled to "sync" the full-bridges PDTRMs when they need to connect their output to the electric grid.

- **UL_Mode_bit_0 (1-bit signal)**

  Along with the next input, it selects the source of the 10-bit values for current and voltage (by counting pulses received per unit time or preset).

- **UL_Mode_bit_1 (1-bit signal)**

  Along with the previous input, it selects the source of the 10-bit values for current and voltage (by counting pulses received per unit time or preset).

- **INPUT_iCell_V_for_UL (1-bit signal)**

  A bit input that measures the rate of incoming pulses from the voltage sensor (V to F). It refers to the PRM modulated PV voltage signal PDTRMs. It is directed to the uplink module for transmission. It is updated with the sampling rate of the MPPT process depending on the amount of received power (1 or 2 samples per second).

- **INPUT_iCell_I_for_UL (1-bit signal)**

  One-bit input that measures the rate of incoming pulses from the current sensor (I to F). It refers to the PRM modulated PV current signal PDTRMs. It is directed to the uplink module for transmission. It is updated with the sampling rate of the MPPT process depending on the amount of received power (1 or 2 samples per second).

- **INPUT_DCBus_V_for_UL (1-bit signal)**

  One-bit input that measures the rate of incoming pulses from the DC-bus (V to F) sensor PDTRMs. It refers to the DC-bus voltage signal modulated by PRM. It is directed to the uplink module. It updates at the sampling rate of 1k samples per second.

- **NEXT_CMND_TRIGGER (1-bit signal)**

  Allows (when set to 1) to automatically override the interpretation of commands to be received by the downlink receiver. This simulates receiving commands (from a predetermined set) in order to test the further functionality of the system. Use of this input is for debugging purposes only.

- **SYMBOLS_IN (1-bit signal)**

  This is the input that receives the external signal on the downlink module (in FSK configuration, where each symbol lasts 60 μsec – and consists of square pulses - 4 periods of 15 μsec or 6 periods of 10 μsec).

- **DL_SEL_SAMPLE_RATE (1-bit signal)**

  Selection of the communication rate in downlink communication (baud rate). It determines whether the receiver should "listen" to the internal transmitted signal,

from the internal transmitter, as mentioned for the 5th subsystem above, or from the link with the external receiver. In case it receives internal data, it expects to receive one HL Bit every 60msec. If the input becomes 1 then the receiver is configured to expect to receive one HL Bit every 2.1 seconds.

- **INPUT_iCell_V (1-bit signal)**

  Input similar to 'INPUT_iCell_V_for_UL', with the difference that this signal is forwarded instead of the uplink to the MPPT / Reg module. Enables it to be fed a different signal than the one interpreted by the uplink interface for debugging purposes.

- **INPUT_iCell_I (1-bit signal)**

  Input similar to 'INPUT_iCell_I_for_UL', with the difference that this signal is forwarded instead of the uplink to the MPPT / Reg module. Enables it to be fed a different signal than the one interpreted by the uplink interface for debugging purposes.

- **INPUT_DCBus (1-bit signal)**

  One-bit input that measures the rate of incoming pulses from the DC-bus sensor (V to F) that is provided to the MPPT / Reg module. It disables PWM if the DC-bus voltage exceeds V_{DC_max} (e.g. 3.0V) and re-enables PWM switching if the DC-bus voltage falls below V_{DC_reg} (e.g. 2.5V).

- **SEL_XNOR_or_XOR (1-bit signal)**

  Selection of XOR or XNOR logic at the MPPT output: changes the duty cycle increase / decrease policy. Useful for debugging and switching control between Buck or Boost DC/DC converters controlled by the P&O MPPT algorithm.

- **SEL_DEC_or_DEC_INC (1-bit signal)**

  DEC or INC / DEC option: when 1, it overrides the policy that chooses case-by-case between increasing or decreasing by forcing the constant decrease of the duty cycle.

- **SEL_DC_Step_1_or_4 (1-bit signal)**

  Choice of increasing or decreasing the duty cycle by 1 or 4 steps: 0 means every 1 step while 1 means every 4 steps.

Outputs:

- **PWM_OUT (1-bit signal)**

  The PWM signal whose pulses appropriately drive the DC/DC converter of the modules of the cascaded H-bridge converter.

- **SET_CUR_SENSOR_OFF (1-bit signal)**

  When this signal is 1 it keeps the current sensor off so it doesn't consume power.

- **SYMBOLS_OUT (1-bit signal)**

  This signal is produced by the internal (independent) downlink transmitter. By appropriately choosing 'DL_SEL_SAMPLE_RATE' = 0, and feeding this signal to 'SYMBOLS_IN', it becomes possible to probe for possible problems related to the connection of the external downlink transmitter.

- **WAKE_UP_1K_OUT (1-bit signal)**

  Signal that indicates that in the current time window the channel is available for sending the information available in the uplink interface of the PDTRM with ID = 0. Therefore, this signal defines the beginning of a new thousand of the corresponding time windows, which alternate with the rate imposed by correctly receiving an HL Bit, i.e. every 60 msec (more on this in the description of the next output). The output of this signal feeds back the corresponding input ('WAKE_UP_1K_IN') of the system (for the synchronization of the uplink information transmission).

- **HL_BIT_EVENT_OUT (1-bit signal)**

  Signal indicating correct reception of an HL-Bit by the system receiver. As the case may be, it needs to feedback the corresponding input ('UL_RETRANSMIT') of the system (to indicate the transition to the next time window and, by extension, the synchronization of the transmission of the uplink information, at the appropriate time, i.e. not only in the correct time window corresponding to in the hardcoded ID PDTRMs but also at the appropriate time within this 60 msec window).

- **Freq_50_60Hz_OUT (1-bit signal)**

  Signal indicating the selected AC output frequency. Where applicable, it needs to feedback the corresponding system input.

- **Outputs S1 to S4 (4-bit signal)**

  The output signals that control the drivers of the full-bridge power switches (e.g. power MOSFETs).

6.2.9. Simulations for each subunit and for each complex hierarchy

Finally, one of the most widespread techniques to increase verifiability was applied, examining the results obtained using various simulation tools as well as real measurements by controlling the behavior of various debug signals over time. During the design of the control and monitoring unit system, a lot of simulation files and FPGA setups were created for receiving experimental data, which were checked through appropriate simulators and logic analyzers, respectively.

Fig. 131 shows the simulation result of a digital low-pass filter arrangement, which was designed to prohibit the propagation of any square pulse with a positive edge duration of less than 7 clock pulses. Analog filters were used on the 'SYMBOLS_IN' input of the final system and on the outputs forwarded to the DC/AC full-bridge drivers of the power converter.

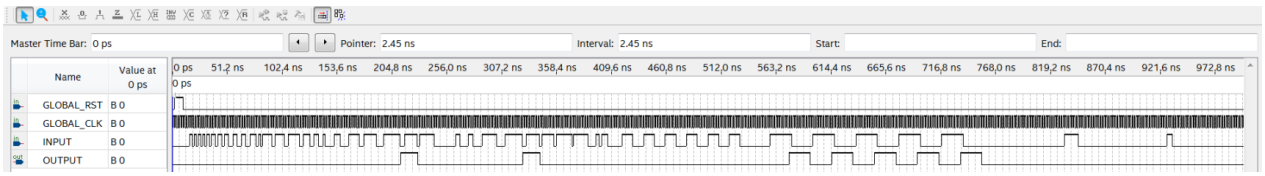


Fig. 131. Typical image from the simulation environment of Quartus Prime Lite Edition.

The goal was to remove short-duration pulses that in both cases can cause communication and power-driving problems, respectively. The choice to use this filter to drive the full-bridge was made to lower the risk of short-duration pulses which can be generated at the transitional times from power signal generation to information signal generation, i.e. when the switching is interrupted too early (in less than 7 clock cycles from the moment it was 'high') then a power signal pulse that had just started to develop may be injected as a spike.

In the graph of Fig. 131, the 3 input signals (reset, clock, input) and the output signal are distinct. It is observed that, the output signal is delayed by 7 clock cycles relative to the input signal but manages to perfectly reject any pulse that lasts for no more than 7 clock pulses.

Fig. 132 shows a complex testbench, which examines a series of states in which the final system will be operating under and checks how the logic circuits transition from one state to another, as well as whether the complex behavior throughout the whole control process (here 20 seconds) is the anticipated one.

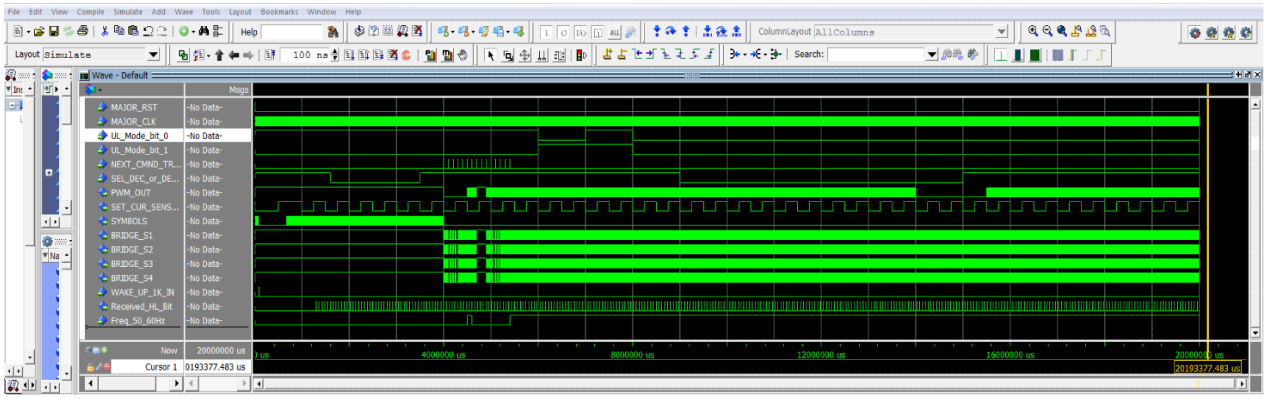


Fig. 132: Typical image from the simulation environment of ModelSim.

It is worth noting that:

- the circuit recognizes, immediately after the first 300 msec from the beginning of the transmission of the SYMBOLS signal, the rate (and phase) of the transmission of the HL bits, which it maintains periodically (as shown by the 'Received_HL_BIT' signal) even after the freezing of the 'SYMBOLS' broadcast, at the time point 4 sec.
- the freeze, which is done intentionally by applying positive edges to the 'NEXT_CMND_TRIGGER' signal, which as its name states takes over the manual switching of the predefined parameterization commands, also affects some other signals as expected. The influence of changing the commands is in some cases clearly reflected in the driving signals of the DC/AC full-bridge ('BRIDGE S1..S4'), as well as in the 'PWM_OUT' output where in one of these commands the freezing of the switching function of this output is defined. It is also manifested in the change of the power generation frequency from 50 to 60 Hz, as can be seen from the 'Freq_50_60Hz' signal, at approximately 4.5 sec and then approximately from 5.4 sec until the end of the simulation.
- the 'SET_CUR_SENSOR' signal clarifies that the estimated power is below a predetermined level, starting from time zero (the beginning) and changes at twice the rate that it changes in normal mode, which indicates that the system is in soft-start mode, during that time. Then the estimated power increases above the preset limit and the 'SET_CUR_SENSOR' switching, as well as the MPPT sampling, are fixed to twice the original rate.
- 'PWM_OUT' interrupts its operation between 14 and 15.5 sec, which happens because the estimation of the DC-bus voltage has exceeded the value of V_{DC_max} (e.g. 3.0 V).

After 15.5 sec the estimate of the DC-bus voltage falls below V_{DC_reg} (e.g. 2.5 V) so the PWM signal continues its switching function, normally.

- the three 1-bit input signals for the PV cell output current and voltage of the modules of the cascaded H-bridge converter as well as the DC-bus voltage are input as variable frequency events in the background and are not displayed in the simulation window of Fig. 132 because their input delays the processing of the results. However, their function is revealed through their effects on the output signals, such as changing the pulse rate of 'SET_CUR_SENSOR', changing the duty cycle of 'PWM_OUT' pulses, and interrupting 'PWM_OUT' as mentioned above.

These 5 points are some examples of the testbenches implemented to check the correctness of the design and operation of the control and monitoring unit system, every time. With appropriate selection of input signals and their combinations, it is possible to improve the control of the correct design and operation of the control and monitoring unit, enhancing design validity and reducing overall development time. To create the specific graph (of 20 sec) approximately 18 hours of simulation execution time were needed and the control mechanisms were based on composition models.

Thus, in order to reduce these required times of testing and correct operation verification for the structures whose complexity requires faster prototyping and more extensive checks, the synthesis of the corresponding subsystems in an actual experimental FPGA array followed to enable the examination of the respective behavior on longer time scales (such as a few tens of minutes). This allowed for the manifestation of phenomena and signals that in shorter times cannot appear, and vice versa, it is impossible to guarantee that the only phenomena to be emerging in such a case will be the ones provisioned by the designer.

Fig. 38 of § 3.3.1 shows a snapshot of the 8-bit logic analyzer where it is experimentally examined whether the embedded transmitter's predefined commands are received correctly by the downlink receiver (i.e., read and demodulated correctly), and whether the FSM interprets each of them by selecting the appropriate state for the multiplexers of 3-bit "Bridge Driving Mode" and 2-bit "DC/DC Op Mode", respectively.

The first of the 8-bit signals (channel 00 in the logic probe) captures the bits of the 'SYMBOLS_OUT' output which is then routed to the 'SYMBOLS_IN 'input. Each of the first 5 instructions consists of 10+10+31 = 51 bits (sync instruction), preparing to read the 30 + 21 CRC = 51 bits functional instruction that follows. The sixth command consists of 10+10+31 = 51 bits for 'WAKE_UP_1K' type synchronization and 30+21 = 51 bits of another functional command.

Synchronization commands contain a small space (channel mute) at the beginning of them, which makes them easy to be distinguished in the diagram. The second, third and fourth bits (channels 01, 02 and 03 in the logic probe) capture the bits of the 3-bit multiplexer "Bridge Driving Mode" which by extension define the driving mode of the DC/AC bridge. The fifth and sixth bits (channels 04, 05 in the logic probe) capture the bits of the 2-bit multiplexer "DC/DC Op Mode" which by extension defines the driving mode of the DC/DC stage of the power converter. The seventh bit (channel 06 in the logic probe) captures the successful acknowledgment of a synchronization command (either of the two available types). The eighth bit (channel 07 in the logic probe) captures the ERROR that prevents the FSM from applying a change.

As can be seen in Fig. 38, this signal is kept at a high level until it recognizes the second functional command, while it does not become high again as it does not detect any error in the transmission. As shown in Fig. 38, the indicators A1 and A2 allow the control of the time intervals between specific events such as, for example, the time interval occupied by the transmission of a sync and a functional command. As expected, this interval is equal to (51+51) x 60 msec = 6.12 sec.

Finally, to increase the verifiability of the control and monitoring unit PDTRMs, a software tool was used that calculates the time that elapses between specific patterns and displays the time that a positive (or negative) edge lasts and the corresponding period, as well as the resulting frequency. This tool was used several times to check the frequency of various signals, in real measurements. Fig. 133 shows an example of focusing on the symbols that form the low-level Bits of 'SYMBOLS_OUT'.

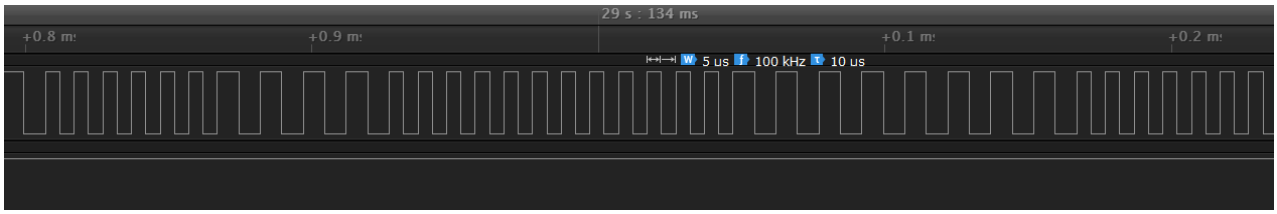


Fig. 11: Enlarged sample from channel 00 where the symbols of the information extracted from the 'SYMBOLS_OUT' pin (and correspondingly inserted into the SYMBOLS_IN pin) can be distinguished.

The figure shows the sequence ..1011001.. from left to right where the 1 consists of 6 periods of 100 kHz, while the symbol 0 consists of 4 periods of 66.66 kHz (in both cases the baud rate is 16.66 kbps – since each symbol lasts 60 μsec).

6.2.10. Provisioning for metastability issues

Finally, similar to the enhancements that were described in § 2.5.7, all input and output signals of the system, and all the internal signals that presented an asynchronous behavior, were protected with the addition of two 2-stage DFF synchronizers during the preparation of the digital system for fabrication in an integrated circuit, in order to reduce the probability of any metastability phenomena occurrences.

7. Conclusions

The research presented in this PhD thesis comprises novel techniques that aim towards the facilitation of the energy management in PV systems and microgrids or smart grids. The broadening of modern PV energy harvesting applications markets depends on the use of power management methods and devices which implement an efficient MPPT process for maximizing power production. The main challenge –common to many renewable sources– is their stochastic power generation nature due to the continuously changing weather conditions. Among the alternative MPPT techniques, the P&O method has the advantages of operational and implementation simplicity. In this PhD thesis, a novel PV MPPT control system has been presented which is suitable for a viable on-chip implementation of the P&O MPPT method. The target is to create a low power, low complexity, and low-cost device that can be dedicated to either a single PV cell, or a set of PV cells, in order to increase the overall PV system power production. When compared to the past-proposed on-chip MPPT implementations at both the scientific and commercial levels, the MPPT system developed in this PhD thesis, along with its power management logic presented in Chapters 2 and 3, respectively, pose a plethora of advantages:

(a) it is implemented based on purely digital circuits without requiring the use of complex circuits such as analog multipliers, S/H units, A/D converters or microprocessors.
(b) its operation does not require a priori knowledge of the operational characteristics of the PV source.
(c) it can be used in combination with switching power converters of any power rating.
(d) it can be easily implemented on-chip with low design complexity, while simultaneously retaining the high-performance features of the P&O MPPT technique.

The experimental results that were obtained under real operating conditions verified the successful operation of the digital PV MPPT control unit and its ability to achieve a high MPPT efficiency over a wide range of operating solar irradiation values. This novel MPPT system design is universal and its operation does not depend on the chip fabrication technology. Finally, it can also be used for performing the MPPT process of thermoelectric

generators (TEGs), which are frequently employed in ambient energy harvesting applications [25].

Following to the introduction of the 4th chapter, it is clearly established that interconnectivity and interoperability are very important attributes in monitoring and controlling the distributed power sources that are dedicated to support the energy management operations in smart grids and microgrids. After a thorough literature review it was found that among the PLC implementation alternatives, the solutions requiring no additional components for transmitting data are the most advantageous in cost and simplicity.

The PLC method presented in this PhD thesis, exploits the power switch driving signals in distributed switching power converters, and more specifically focuses on the cascaded H-bridge converters, to enable the transmission of digital information data along with their power generation capabilities. Following the extensive review of the prior art it was demonstrated that, compared to the existing solutions, the proposed uplink PLC technique introduced in this PhD thesis, combines the following advantages:

(e) enables the application to cascaded H-bridge structures with either a DC or an AC output,

(f) avoids the use of an additional power amplifier or coupling circuit for the transmission of information, and this is done while keeping its independence from the implementation scale and its ability to supply all kinds of power-load types.

Therefore, it is characterized by low implementation complexity, high versatility and, high scalability features. The uplink PLC method was applied on an experimental FPGA prototype of a two-cell cascaded H-bridge inverter, where the information transmission and reception units were implemented in an FPGA device. On a second experiment the same digital system was fabricated in an ASIC Both experiments verified the successful transmission of telemetry data through the power converter circuit and their retrieval by a receiver attached in the power loop. Simultaneously, the transmission of power to the load was performed, thus verifying the validity and applicability of the uplink PLC technique. The uplink PLC method presented in this PhD thesis could also enable the integration of communication capabilities to stacked power converters (e.g. [81], [82]) if digitally (i.e., ON/OFF) controlled power switches are employed at their output. Depending on the target application specifications, this novel PLC method is applicable to cascaded H-bridge

converters with either isolated DC sources (e.g. [94]), or a single DC source topology such as in [112]. This uplink PLC method has proven to simplify the hardware infrastructure required for monitoring power production sources synthesized by multiple individual cells (e.g. PV modules, batteries, etc.). One important aspect that was further researched was issues regarding the THD of the cascaded H-bridge converter output voltage when this method is applied. For that purpose, various control schemes were introduced and compared, aiming to lower the THD of a PLC system that transmits power and data by using a multilevel inverter based on cascaded H-bridge topology. A series of parametric Simulink models were applied to determine the conditions under which each policy of simultaneous data and power transmission presents the most favorable THD response while ensuring reliable data communication. The comparison of the results highlighted useful insights regarding the applicability of each control scheme per case. The simulation results revealed that:

(g) the PD-SPWM may be outperformed by a simple NLC when both operate over a high-frequency data carrier.
(h) if an L-C filter is employed at the end of the power cable, the system can transmit power and data with a THD of less than 4.2% as long as 10 or more modules are used in the CHB-MLI converter structure.

The uplink PLC method was complemented by the development of a downlink PLC communication technique for the implementation of the reverse process, i.e., the transmission of digital information from the terminal computer (RMCU) to the individual modules of a cascaded H-bridge converter through their power circuit and the power cable which interconnects the power converter with the load, in order to facilitate their remote control. This is because the PLC technologies provide not only enhanced monitoring but also broad control capabilities to the power production and consumption units, and this is a very useful feature for all modern smart grids, distributed PV systems, energy storage systems, etc. The developed technique comprises an integrated framework of a digital data transmitter, receiver, and communication protocol, all portrayed as a scalable multi-layer design. In contrast to the existing PLC techniques, the downlink PLC method presented in this PhD thesis exhibits the following advantages:

(i) supports digital data transmission for integrated parameterization and command functionalities,

(j) it does not require the use of additional coupling circuits or power amplifiers for the PLC implementation, and

(k) its operation does not depend on the scale of implementation and the type of the power-supplied load.

The experimental results verified the successful operation of the developed PLC technique through the transmission of digital data by a terminal computer (RMCU) and their reception by the individual power modules of a two-cell cascaded H-bridge converter along with the simultaneous transmission of power to the load over the common power cable.

The aforementioned electronic systems can be used independently which suggests that, in principle, each one is unique and autonomous and thus can be utilized either alone or be integrated with the rest, in all possible combinations. Also, these electronic systems can:

- be implemented either in an integrated circuit or in FPGA/microcontrollers/DSP,
- be applied at a PV cell, PV module or PV array level and
- be extended to other non-PV-cell related applications (e.g. with thermoelectric generators TEGs, distributed RES applications etc.)

Finally, the implementation choices that were adopted during the development course of this work were specifically designed to enhance the verifiability and robustness of the overall system. The extended documentation, the segmentation of work in autonomous milestones that could be assembled in a variety of configurations, as well as the inclusion of the FPGAs introducing the hierarchical format, allowed for a versioning system which expedited the testing and debugging procedures. All the techniques were proven to facilitate the verifiability and enhance the robustness of the developed system.

As regards the future research that could complement this work, it is interesting to focus in increasing the baud rate and the security of the transmitted data in the uplink and downlink PLC techniques which have been presented in this PhD thesis. This can be performed by including simple but strong data compression and data encryption techniques. Also, for that purpose, the implementation of a handshaking sequence which would adjust the PLC parameters in real-time, similar to what is performed with the modern modem technologies, could be investigated. It would also be important to expand the same principles for application in other types and configurations of distributed energy sources and other power converter topologies.

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