Automated Prior Knowledge Aware Optimization For Radio Frequency Integrated Circuits

A Master Thesis

by

George Konstantopoulos

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Chapter 1 : Introduction

1.1 Motivation

Wireless communication has experienced a global boom in the last decade because it enables easier communication among individuals. For example, the cellular telephone will become even more popular because of its convenience and added features. Wireless communication also provides more convenient access to information; e.g., wireless LAN allows one to access the Internet without having to connect to the network physically. Nowadays it is very common to see people exploring the Internet at a coffee bar. The huge market value of wireless communication systems has driven non-stop efforts in the information industry to improve the performance of wireless communication systems. Academia has also witnessed a flourish of wireless communications research in the fields of communication, digital signal processing and integrated circuit design.

In wireless communications, the information must be transmitted and received with acceptable fidelity. Unfortunately, wireless communication systems usually operate in a hostile environment, which makes transmission and reception more difficult. One of the great challenges in wireless communications is that the system should tolerate a hostile environment, as for example in the presence of “unwanted signals”, while at the same time the demand for portability of handset devices – systems poses strict requirements in power consumption. More specifically, interferers from the environment that contains many unrelated RF signals and noise associated with the device itself, together with low signal output power due to low available supply power, can degrade transceiver performance drastically if care is not taken in designing such systems.

Recently, much research effort has been focused on CMOS implementations of low-cost high-performance wireless communication systems, mainly owing to the aggressive scaling of CMOS, which provides the capability of integrating large scale complex digital signal processing circuitry with lower cost compared to Bipolar, SiGe and GaAs integrated circuit technologies.

The market motivates the technology evolution by putting aggressive demands on the performance, cost, and power consumption of the circuits that operate at high frequencies. The main problem that arises for the design of RF basic building blocks of every transceiver is that the trade-offs among linearity – gain, noise – power consumption of each individual block must be resolved efficiently, in order to satisfy the strict specifications of various wireless standards such as UWB, WiFi, WiMax in a cost effective manner.

In that sense, a multitude of circuit design variables have to be simultaneously selected – optimized to achieve compliance with the specifications. This is a time-consuming design effort and hence it is quite difficult for an analog designer to find the optimized trade-off points and produce truly optimized circuits by hand. Thus, the need for an efficient methodology that leverages design expertise and leads to satisfaction of wireless standards specifications while minimizing optimization time, is apparent.

In this dissertation an automated optimization methodology for analog RF IC circuit design is described. Multiple design goals such as noise, gain, and power consumption are met by a system that exploits and combines the optimization properties of genetic algorithm (GA) and the precision of the Spectre RF circuit simulator. Human-prior knowledge has been incorporated into the system to solve complex optimization problems for the design of various voltage-controlled-oscillators (VCOs), while a knowledge free approach has been adopted for the case of a variable-gain-amplifier (VGA). The tool optimizes active device sizes along with the geometrical parameters of on-chip inductors, allowing the designer to extract from circuit topologies the best they can deliver. The overall system together with results of four 5.4GHz oscillator topologies and a 2 GHz current-steering variable-gain-amplifier in 180nm IBM BiCMOS technology are demonstrated.

1.2 Overview

This dissertation is organized as follows. Chapter 2 begins with a brief introduction to basic oscillation principles followed by a detailed discussion of phase noise of an oscillator. Various diffential and quadrature oscillator topologies are assessed in terms of phase noise and power consumption performance. Finally comparisons between cross-coupled, Colpitts LC, parallel and serial coupled quadrature oscillators, based on performance parameters such as phase noise, start-up characteristics and tuning range, are given.

In chapter 3, design considerations of CMOS RF variable gain amplifiers are discussed. In chapter 4, an automated optimization methodology for four voltage-controlled-oscillators and a variable-gain-amplifier is presented. Specifically, we describe how hand-made optimization in the circuit level can be automated. Results that validate our approach are presented in chapter 5. Finally in chapter 6, the layout of the cross-coupled voltage-controlled-oscillator produced by our automated design methodology along with post-layout simulations are illustrated.

Chapter 2 : Design of Voltage Controlled Oscillators

2.1 Principle of Operation

An ideal oscillator generates a periodic output signal. Its mathematical model is described by the following expression $v(t) = A(t)\sin(\omega_o t + \phi_o))$, where *A* is the amplitude, ω_o the oscillation frequency and ϕ_o is the phase reference.

In a practical LC oscillator the output is given by:

$$v(t) = A(t)[\sin \omega_o t + \phi(t)] \qquad (2.1)$$

The instantaneous frequency of oscillation is the time derivative of the total phase given by:

$$\phi(t) = \frac{\partial}{\partial t}\left[\omega_o t + \phi(t) = \omega_o + \frac{\partial}{\partial t}[\phi(t)] \right] \qquad (2.2)$$

In general, both the amplitude *A(t)* and phase *φ(t)* of a practical oscillator are functions of time, which reveals the fact that in nature, the oscillator is a ***time variant*** system. The fluctuations of the phase and amplitude in time domain lead to the existence of sidebands around the resonant frequency ω_o in the spectrum of a practical oscillator. The time variant phase causes frequency deviation, as is implied by equation (2.2). This phenomenon is referred to as phase noise in the spectrum of oscillator output.

An oscillator can be viewed as a feedback system or, equivalently, from a one-port point of view. Next, we consider the principle of oscillation from both points of view.

2.1.1 Feedback Model

Most RF oscillators can be viewed as a feedback system [1] as depicted in Figure 2-1 where the transfer function from *X(s)* to *Y(s)* is:

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 - H(s)} \qquad (2.3)$$

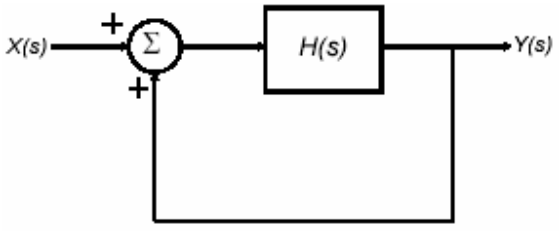


Figure 2-1 Feedback oscillatory system.

A self – sustaining mechanism arises at frequency s_o without an input stimulus, i.e., $X(s)=0$, if $H(s_o)=1$. To maintain a constant amplitude, s_o must be purely imaginary, that is

$$H(j\omega_o)=1 \qquad (2.4)$$

For steady state oscillation, two necessary but yet not sufficient conditions must be simultaneously met at ω_o:

$$|H(j\omega_o)|=1$$

$$\angle H(j\omega_o)=n\cdot 360^o \quad \textit{(n=0, 1, 2,…)} \text{ at frequency } \omega_o$$

Known as the Barkhausen's criteria, the above conditions imply that any feedback system can oscillate if its loop gain and phase shift are chosen properly.

However, in most oscillators, a *frequency-selective* network (resonator) is included in the loop so as to determine the oscillation frequency and filter out higher-order harmonics (Figure 2-2).

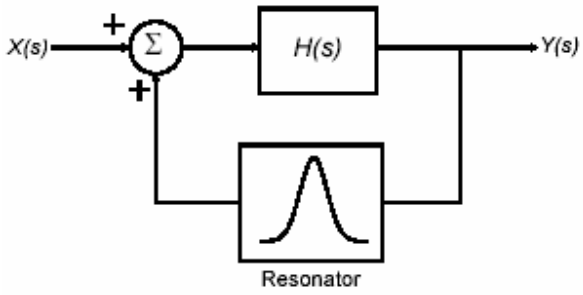


Figure 2-2 Feedback model with frequency-selective network (resonator).

The resonant circuit in Figure 2-2 is usually implemented as an LC tank (Figure 2-3).

The Barkhausen criteria for oscillation at frequency ω_o for the resonator-based oscillator shown in Figure 2-3 instruct that:

$$G_m Z(j\omega_o) = 1 \qquad (2.5)$$

and $$\angle G_m Z(j\omega_o) = n \cdot 360^o$$

where G_m is the two-port *short-circuit transconductance*.

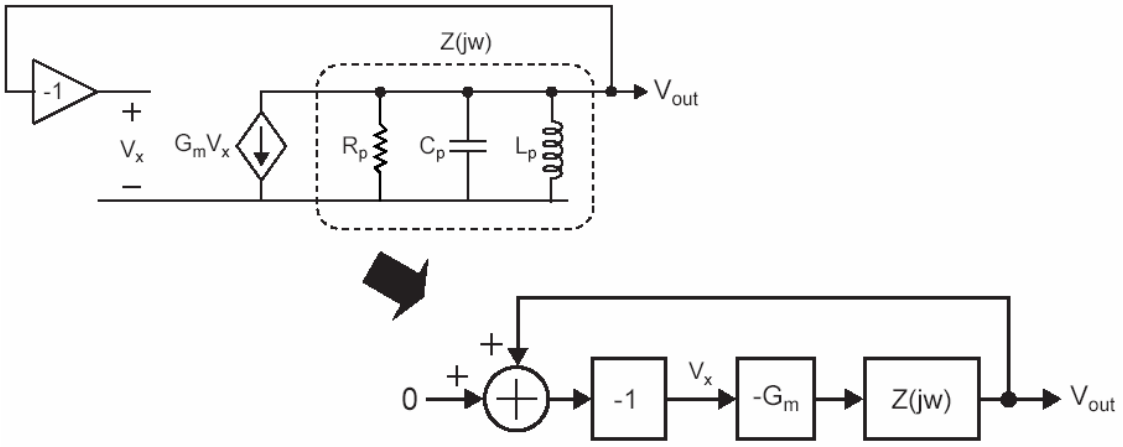


Figure 2-3 Resonator based oscillator.

Assuming that G_m is purely real, $Z(j\omega_o)$ must also be purely real. Figure 2-4 shows that the parallel-resonator at resonance looks like a resistor (i.e., purely real) and that the phase condition is satisfied. The magnitude condition can be achieved by setting

$$G_m R_p = 1 \qquad (2.6)$$

where R_p is the parallel equivalent resistance of the LC tank.

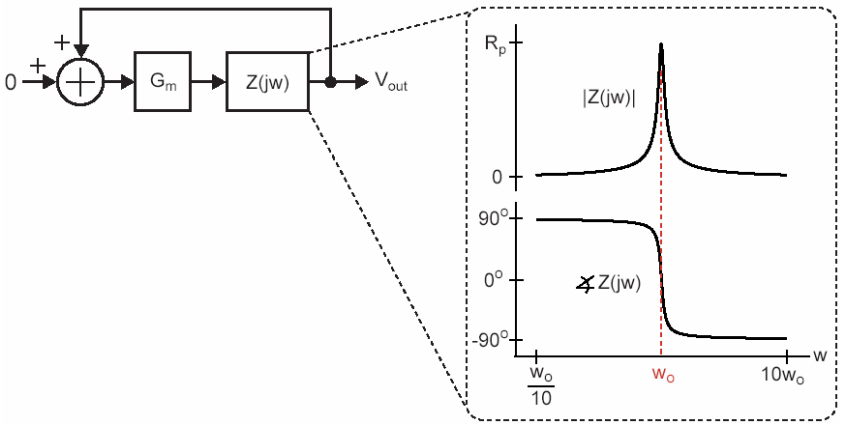


Figure 2-4 Parallel resonator at resonance.

An alternative study approach of oscillators consists in the observation of the poles, on the S-plane, that are the roots of the characteristic equation:

$$1 - H(s) = 0 \qquad (2.7)$$

where *H(s)* is also called the *loop gain* of the circuit.

The root locus plot allows us to view closed loop pole locations as a function of open loop poles/zero and open loop gain $(G_m R_p)$.

As the loop gain $G_m R_p$ increases, closed loop poles move into right half S-plane.

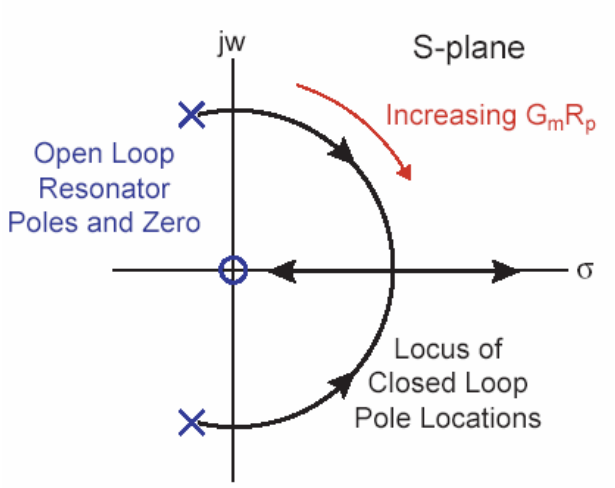


Figure 2-5 Impact of increasing *Gm*.

Setting G_m too low results in a $G_m R_p < 1$ condition, the closed loop poles end up in the left half S-plane and finally an overdamped response occurs, that is the oscillation dies out as illustrated in Figure 2-6.

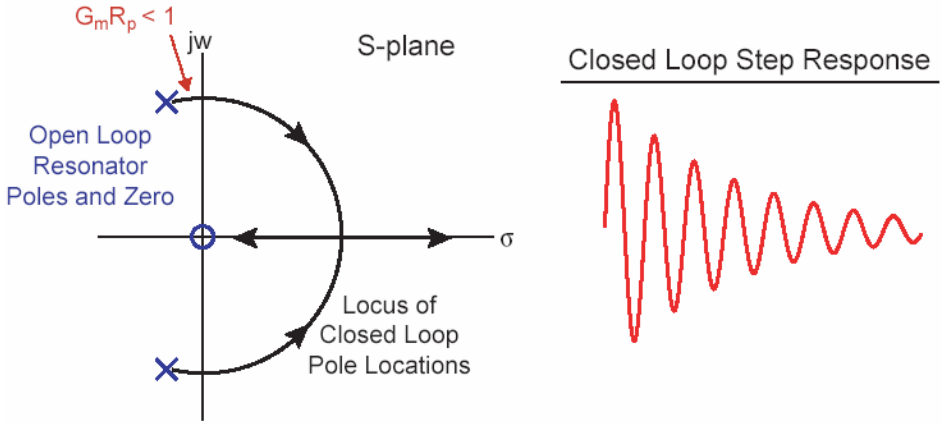


Figure 2-6 Impact of setting *Gm* too low.

Setting G_m too high results in a $G_m R_p > 1$ condition, the closed loop poles end up in the right half S-plane and finally an unstable response occurs, the waveform Figure 2-7 blows up.

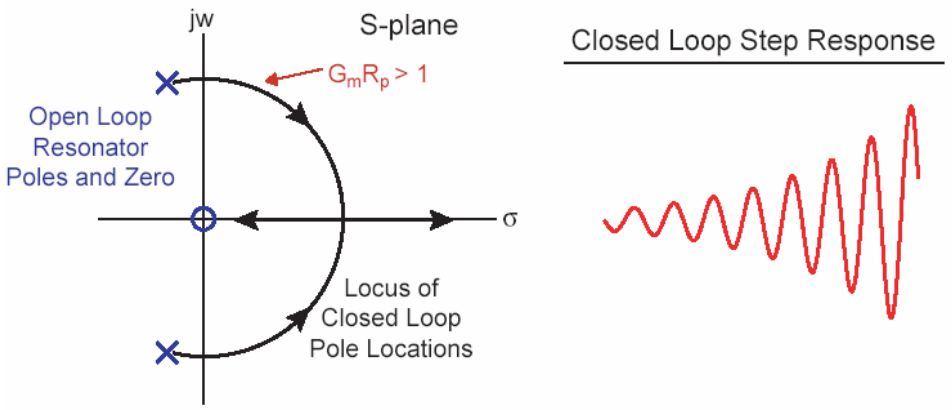


Figure 2-7 Impact of setting *Gm* too high.

To sustain steady oscillation in a center frequency ω_o the characteristic equation (2.7) must have roots of the form $s = \pm j\omega_o$, in other words the roots must be purely imaginary (Figure 2-8).

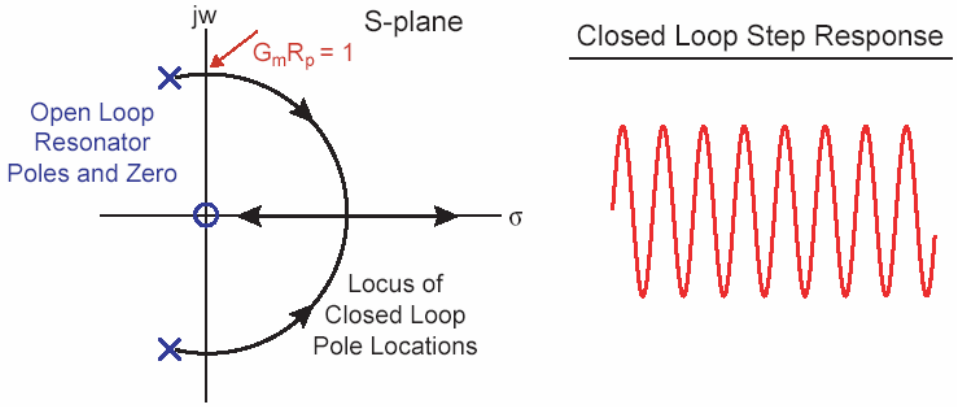


Figure 2-8 Setting *Gm* to the right value.

Among various approaches the most effective way to achieve a loop gain $G_m R_p$ exactly equal to one, is to leverage amplifier non-linearity as feedback. Practical transconductance amplifiers have saturating characteristics. As input amplitude is increased, the effective gain from input to fundamental of output drops and amplitude feedback occurs resulting in $G_m R_p = 1$ in steady state (Figure 2-9).

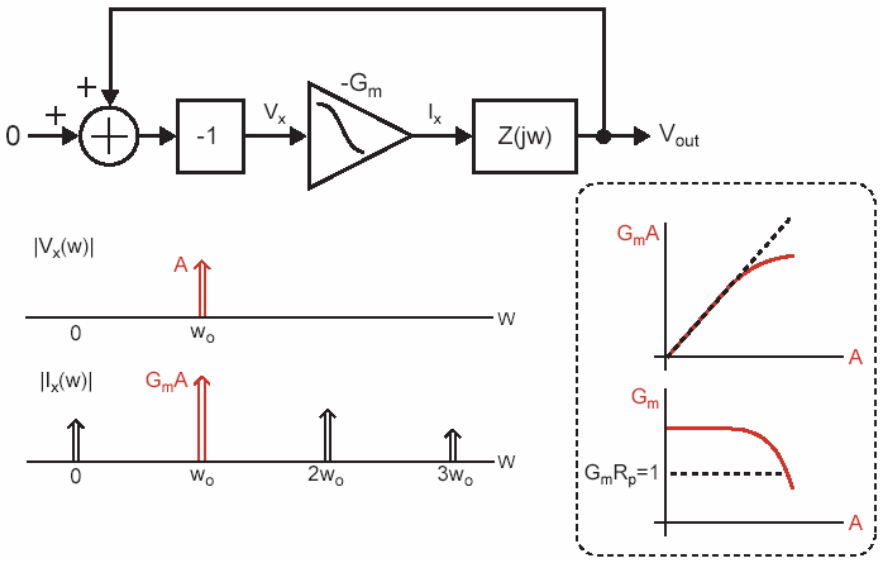


Figure 2-9 Amplifier non-linearity as feedback for gain control.

2.1.2 One Port Model

In LC oscillators we seek to cancel out the energy loss in the tank caused by parasitic R_p with a negative resistance element. Active components form a small-signal negative resistance that replenishes the loss during every oscillation cycle (Figure 2-10).

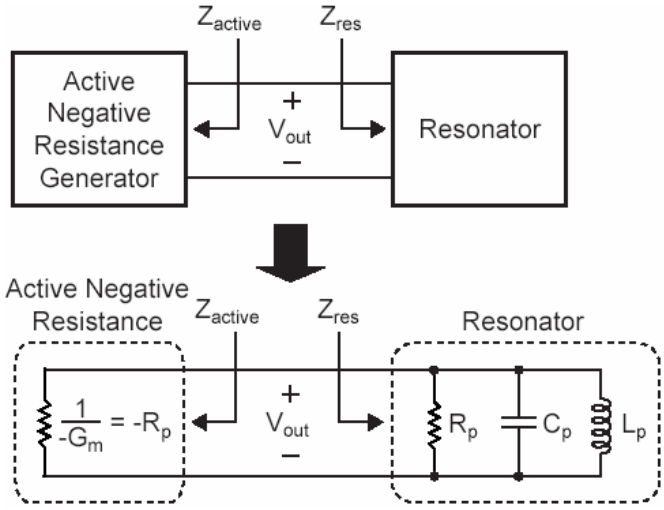


Figure 2-10 One port view of LC oscillator.

To achieve sustained oscillation, we must have

$$\frac{1}{G_m} = R_p \Rightarrow G_m R_p = 1 \qquad (2.8)$$

Since oscillators operate over a very narrow band of frequencies, we can always do series to parallel transformations to achieve a parallel network for analysis (Figure 2-11) [2].

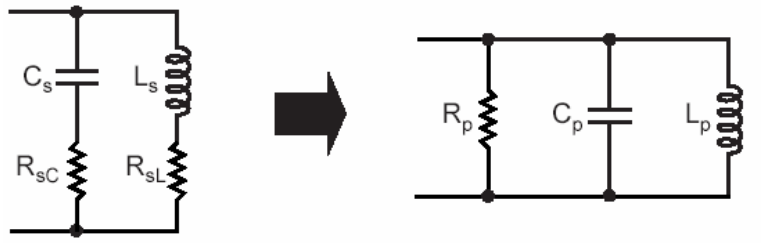


Figure 2-11 Series to parallel transformation for one port oscillator analysis.

A one-port representation provides an alternative view of the basic principle, which is simpler giving more insight into the behavior of oscillators and making it convenient for intuitive analysis.

2.2 Phase Noise in Oscillator

As other analog circuits, oscillators are susceptible to noise. Noise injected into an oscillator by its constituent devices or by external means may influence both the frequency and the amplitude of the output signal. In most cases, the disturbance on the amplitude is negligible or unimportant, and only the random phase variation in the oscillator's output oscillating signal is considered [3] (***phase noise***). The latter can also be viewed as random variation in the period or deviation of the zero crossing points from their ideal position along the time axis (***jitter noise***). Thus, phase noise and jitter noise are defined at frequency and time domain, respectively (Figure 2-12).

Recalling (2.1) for a nominally periodic sinusoidal signal, we can write:

$$out(t) = 2\cos[2\pi f_o t + \phi_{out}(t)] \qquad (2.9)$$

where $\phi_{out}(t)$ is a small random excess phase representing variations in period. The function $\phi_{out}(t)$ is called ***phase noise***.

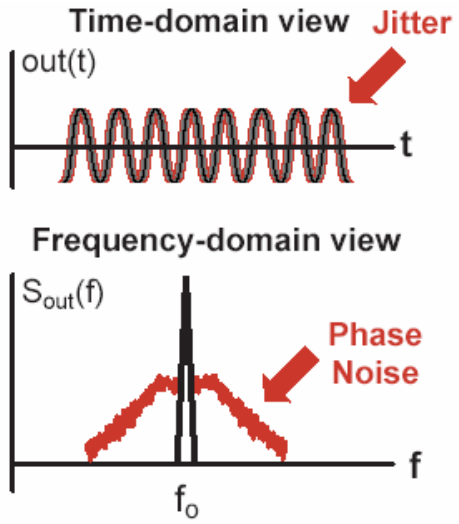


Figure 2-12 Definition of phase and jitter noise.

Using a familiar trigonometric identity, we can rewrite (2.9) as:

$$out(t) = 2\cos(2\pi f_o t)\cos(\phi_{out}(t)) - 2\sin(2\pi f_o t)\sin(\phi_{out}(t)) \quad (2.10)$$

given that phase noise is small $|\phi_{out}(t)| << 1$ rad (2.10) reduces to:

$$out(t) = 2\cos(2\pi f_o t) - 2\sin(2\pi f_o t)\phi_{out}(t) \quad (2.11)$$

Assuming $\phi_{out}(t)$ is bandlimited and adopting an LTI (linear time invariant) approach, we perform a Fourier transform of (2.11) to get the spectrum:

$$S_{out}(f) = S_{\sin}(f) + S_{\sin}(f) * S_{\phi out} \quad (2.12)$$

For an ideal sinusoidal oscillator operating at f_o, the spectrum assumes the shape of an impulse at $\pm f_o$, whereas for an actual (noisy) oscillator, the spectrum exhibits “skirts” around the carrier frequency (Figure 2-13).

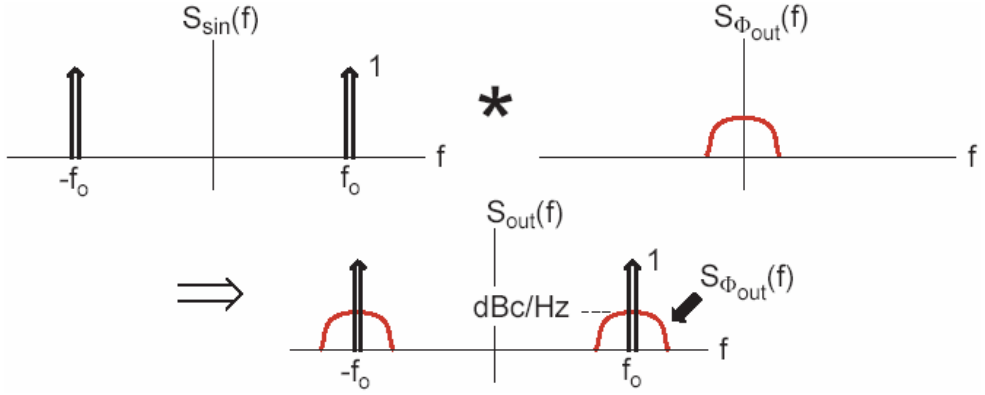


Figure 2-13 Spectrum of an oscillator’s output signal.

To quantify phase noise, we consider a unit bandwidth at an offset $\Delta\omega$ with respect to f_o, calculate the noise power in this bandwidth, and divide the result by the carrier (average) power. Thus, phase noise is mathematically expressed by:

$$L(f)=10\log\left(\frac{S_{\phi out}}{P_{sig}}\right)=10\log\left(\frac{2S_{\phi out}}{2}\right)=10\log(S_{\phi out})\ {}^{dBc}/_{Hz} \quad (2.13)$$

In the single sided version (Figure 2-14) *L(f)* remains the same and it is given by:

$$L(f)=10\log\left(\frac{S_{\phi out}}{P_{sig}}\right)=10\log\left(\frac{S_{\phi out}}{1}\right)=10\log(S_{\phi out}) \quad (2.14)$$

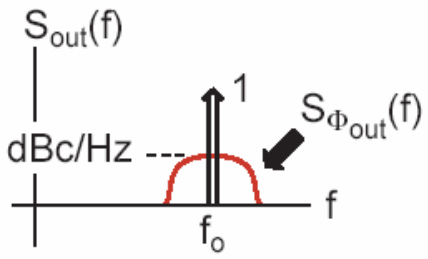


Figure 2-14 Single sided spectrum.

So we can work with either one-sided or two-sided spectral densities since *L(f)* is set by the ratio of noise density to carrier power.

In order to calculate the intrinsic phase noise in oscillators we must take into account two categories of noise sources (Figure 2-15, 2-16).

1. Noise due to tank loss
2. Noise due to active negative resistance

Impedance calculation across an ideal tank gives:

$$Z_{\tan k}(\omega)=\frac{1}{j\omega C_p}//\ j\omega L_p=\frac{j\omega L_p}{1-\omega^2 L_p C_p} \quad (2.15)$$

About resonance, i.e., $\omega=\omega_o+\Delta\omega$, $Z_{\tan k}$ takes the form:

$$Z_{\tan k}(\omega)=-\frac{j}{2}\frac{1}{\omega_o C_p}\left(\frac{\omega_o}{\Delta\omega}\right) \quad (2.16)$$

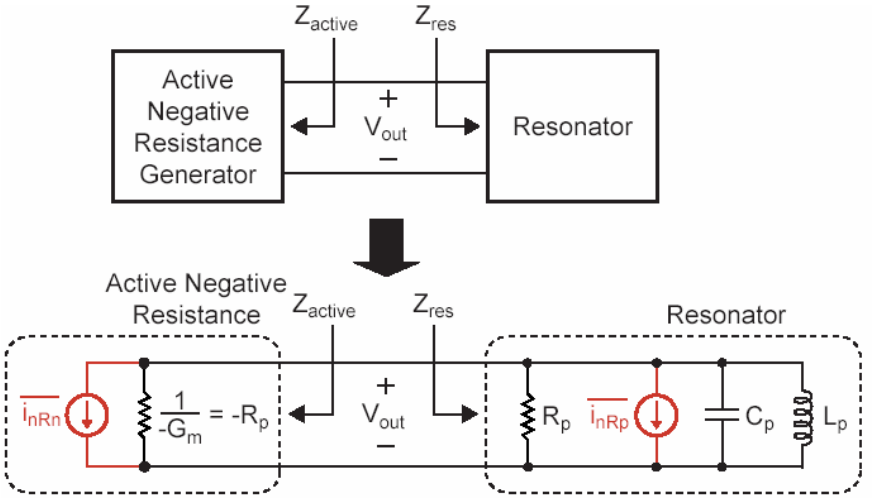


Figure 2-15 Calculation of intrinsic phase noise.

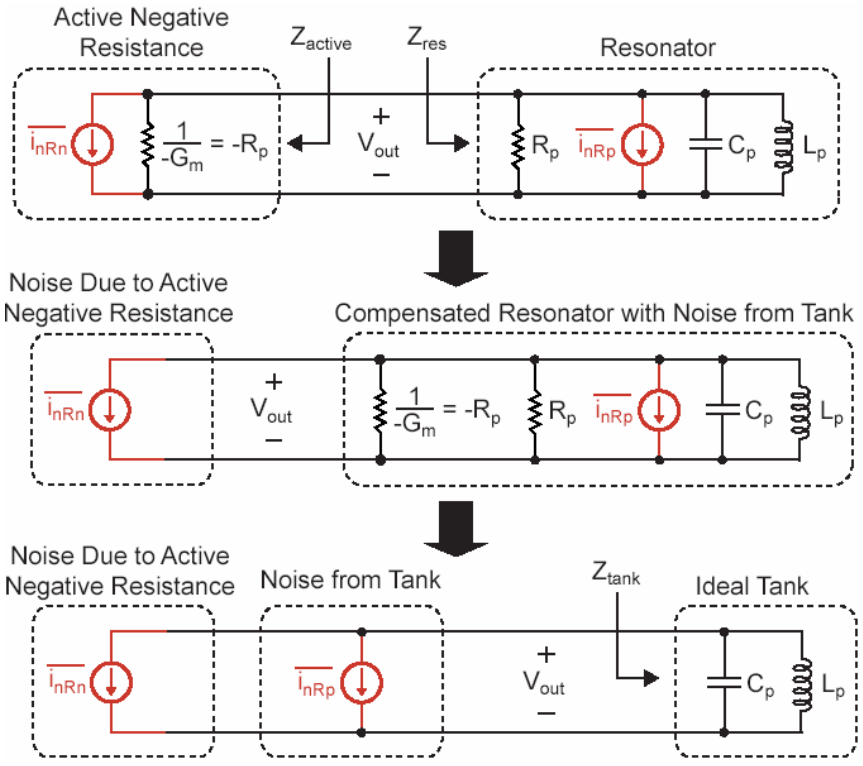


Figure 2-16 Equivalent model for noise calculation.

The loss of an actual tank is modeled with R_p. We can relate the quality factor *Q* of the tank with its parallel parasitic resistance by:

$$Q = R_p \omega_o C_p \Rightarrow \frac{1}{\omega_o C_p} = \frac{R_p}{Q} \qquad (2.17)$$

Parameterizing the ideal tank impedance in terms of Q of the actual tank we get from (2.16) using (2.17):

$$Z_{\tan k}(\Delta\omega) \approx -\frac{j}{2}\frac{R_p}{Q}\left(\frac{\omega_o}{\Delta\omega}\right) \Rightarrow$$

$$\left|Z_{\tan k}(\Delta f)\right|^2 \approx \left(\frac{R_p}{2Q}\frac{f_o}{\Delta f}\right)^2 \qquad (2.18)$$

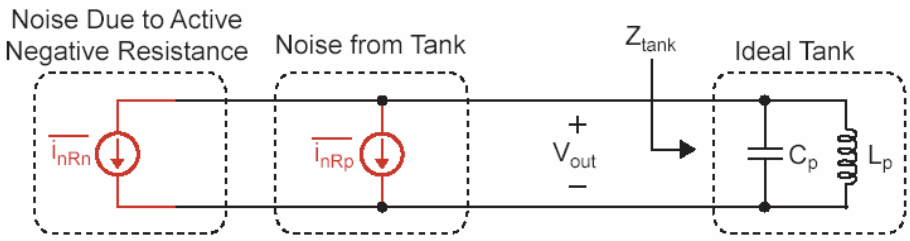


Figure 2-17 Overall noise output spectral density.

Assuming noise from the active negative resistance and the tank are uncorrelated:

$$\frac{\overline{u_{out}^2}}{\Delta f} = \left(\frac{\overline{i_{nRp}^2}}{\Delta f} + \frac{\overline{i_{nRn}^2}}{\Delta f}\right)\left|Z_{\tan k}(\Delta f)\right|^2 = \frac{\overline{i_{nRp}^2}}{\Delta f}\left(1 + \frac{\frac{\overline{i_{nRn}^2}}{\Delta f}}{\frac{\overline{i_{nRp}^2}}{\Delta f}}\right)\left|Z_{\tan k}(\Delta f)\right|^2 \quad (2.19)$$

We must note that the above expression represents total noise that impacts both amplitude and phase of oscillator output. The second term of (2.19) is called ***noise factor*** ($F(\Delta f)$) and it expresses the ratio of the total noise in tank at frequency Δf to the noise in the tank due to tank loss at frequency Δf .

Noise from the tank is due to the resistor R_p:

$$\frac{\overline{i_{nRp}^2}}{\Delta f} = 4kT\frac{1}{R_p} \qquad (2.20)$$

Noise from the active gain cell is due to:

- ***Thermal Noise*** – Thermally agitated carriers in the channel cause a randomly varying current, given by:

$$\overline{i_n^2} = 4kT\gamma g_{do}\Delta f \quad (2.21)$$

where γ is called excess noise factor and is equal to 2/3 for long-channel transistors (in saturation) and 2 or 3 to short-channel, and g_{do} the drain-source conductance.

- ***Flicker Noise (1/f)*** – Traps at channel/oxide interface randomly capture/release carriers.

$$\overline{i_n^2}\Big|_{1/f} = \frac{K}{f}\frac{g_m^2}{WLC_{ox}^2}\Delta f \quad (2.22)$$

Noise in MOS transistors generally depends on technology, device size and bias conditions. Flicker noise performance of pMOS transistors is often better compared to nMOS, as $K_p << K_n$.

From (2.19), (2.20) and (2.18) we get the following single sided output noise spectral density expression:

$$\frac{\overline{u_{out}^2}}{\Delta f} = 4kTF(\Delta f)R_p\left(\frac{1}{2Q}\frac{f_o}{\Delta f}\right) \quad (2.23)$$

According to the equipartition theorem [4] the noise impact splits evenly between amplitude and phase for a sine wave output. Thus, the phase output noise is the half of that defined in (2.23). Amplitude variations are suppressed by feedback in the oscillator, thus only phase noise must be considered.

Figure 2-18 Amplitude and phase noise.

Finally the spectrum of the phase noise substituting (2.23) in (2.13) is:

$$L(f) = 10\log\left(\frac{S_{\phi out}}{P_{sig}}\right) = 10\log\left(\frac{2kTF(\Delta f)}{P_{sig}}\left(\frac{1}{2Q}\frac{f_o}{\Delta f}\right)^2\right) \quad (2.24)$$

The phase noise produced by the active elements is the same as the tank noise, thus

$$L(f) = 10\log\left(\frac{4kTF}{P_{sig}}\left(\frac{1}{2Q}\frac{f_o}{\Delta f}\right)^2\right) \quad (2.25)$$

Expressions (2.24), (2.25) known as Leeson's expressions are valid only in the $-20dB/decade$ region of the whole phase noise spectrum of a practical oscillator, which is shown in Figure 2-19.

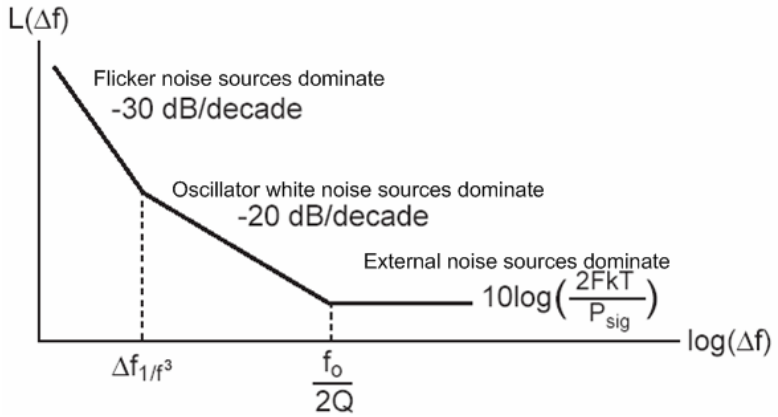


Figure 2-19 Typical Phase Noise Curve for an Oscillator.

Treating $F(\Delta f)$ in an empirical way Leeson-Cutler [44] proposed an ad hoc modification of the noise expression to capture the above noise profile:

$$L(f) = 10\log\left(\frac{2kTF}{P_{sig}}\left(1+\frac{1}{2Q}\frac{f_o}{\Delta f}\right)^2\left(1+\frac{\Delta f_{1/f^3}}{|\Delta f|}\right)\right) \quad (2.26)$$

Although the expression for the noise in the $1/f^2$ region is thus easily obtained, the expression for the $1/f^3$ portion of the phase noise is completely empirical. As such, the common assumption that the $1/f^3$ corner of the phase noise is the same as the $1/f$ corner of device flicker noise has no theoretical basis.

While (2.26) provides insight into how intrinsic noise sources impact phase noise performance, it is generally difficult to calculate *F a priori*. One important reason is that much of the noise in a practical oscillator arises from periodically

varying processes and is therefore cyclostationary, thus LTI is insufficient and a linear time variant (LTV) approach is needed [5].

The question remains: what determines the value of the noise factor F and how is it related to the circuit parameters for different oscillator topologies.

The question posed above is addressed using a non-empirical phase noise model. Clearly, the model should deal in an analytic way with the inherent time-variant nature of phase noise. Recently, Hajimiri and Lee proposed a linear time-variant (LTV) phase noise model [5][6][7] based on the following assumptions:

- The random phase shifts are added linearly.
- The phase shift introduced by the noise current is time variant, i.e., the same amount of noise generates a different level of phase noise, depending on when the noise source is active.

The first assumption is easily understood since random noise from either passive or active devices is usually in such a small magnitude that its effect can be regarded as a perturbation that is accurately treated using the superposition principle.

The second assumption is appreciated in view of the following important observation. The phase shift introduced in the output waveform by the noise current injected into the LC tank depends on the specific time instant when it is injected (Figure 2-20). In the third graph of Figure 2-20, for example, the noise current injected at the peak of the voltage waveform causes an amplitude fluctuation but no phase shift at all in the zero crossing point. In contrast, in the first graph of Figure 2-20, the noise current injected exactly at the zero crossing point results in zero amplitude error but a maximum phase shift error that cannot be corrected.

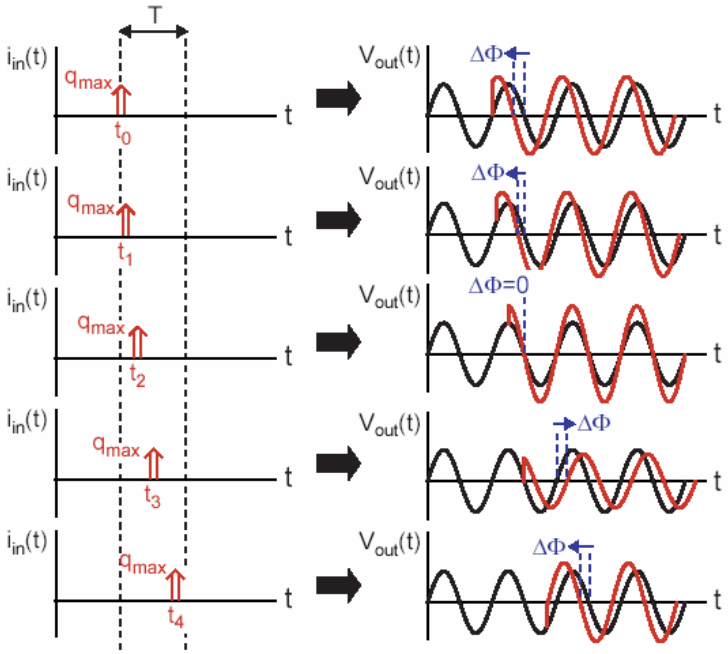


Figure 2-20Time varying impact of noise on phase.

From Figure 2-20, we conclude that the magnitude of the excess phase shift error not only depends on the power spectral density of the noise current, but also on the time instant when the noise current is injected into the tank circuit. In other words, the impulse response $h_\phi(t,\tau)$ is time variant, where τ is the time at which the noise current impulse is injected. The time dependency is conveniently described using the so-called impulse sensitivity function (ISF) $\Gamma(\tau)$; it represents the amount of phase shift that results from the injection of an impulse of noise current at time τ. Because $\Gamma(\tau)$ is periodic, it can be written as $\Gamma(\omega_o\tau)$. The impulse response $h_\phi(t,\tau)$ is related to ISF as:

$$h_\phi(t,\tau) = \Gamma(\omega_o t)\cdot u(t-\tau) \quad (2.27)$$

Based on the assumption that the phase shift errors add linearly, the total phase shift error can be expressed as:

$$\phi(t) = \int_{-\infty}^{+\infty} h_\phi(t,\tau) i(\tau) d\tau = \int_{-\infty}^{t} \Gamma(\omega_o t)\cdot i(\tau) d\tau \quad (2.28)$$

After obtaining the phase shift $\phi(t)$ and relating it to (2.9), it can be shown that the phase noise due to noisy current with power spectral density $\overline{i_n^2}/\Delta f$ is

$$L\{\Delta\omega\} = \frac{\overline{i_n^2}/\Delta f}{2q_{\max}^2} \cdot \frac{\Gamma_{eff,rms}^2}{\Delta\omega^2} \qquad (2.29)$$

where $\Delta\omega$ is the offset frequency from the carrier frequency, $\Gamma_{eff,\max}$ is the rms value of the effective impulse sensitivity function associated with that particular noise source and $q_{\max}$ is the maximum charge swing across the LC tank.

2.3 Oscillator Topologies

A major challenge in the design of future single-chip RF transceivers is the integration of the voltage-controlled oscillator (VCO) that generates the local oscillator (LO) carrier signal. The most important specifications of a VCO are low phase noise, low power, and high-frequency operation. Passive LC-oscillators tend to be the best choice for integration of high performance VCOs on silicon substrates by integrating on-chip spiral inductors. The most common CMOS RF LC-VCO topologies are discussed next.

2.3.1 Cross-Coupled LC Oscillator

This type of oscillator structure is quite popular in current CMOS implementations for its simple topology and its good phase noise performance.

As shown in Figure 2-21, it comprises the LC tank and the negative conductance circuit formed by cross-coupled transistors M1 and M2.

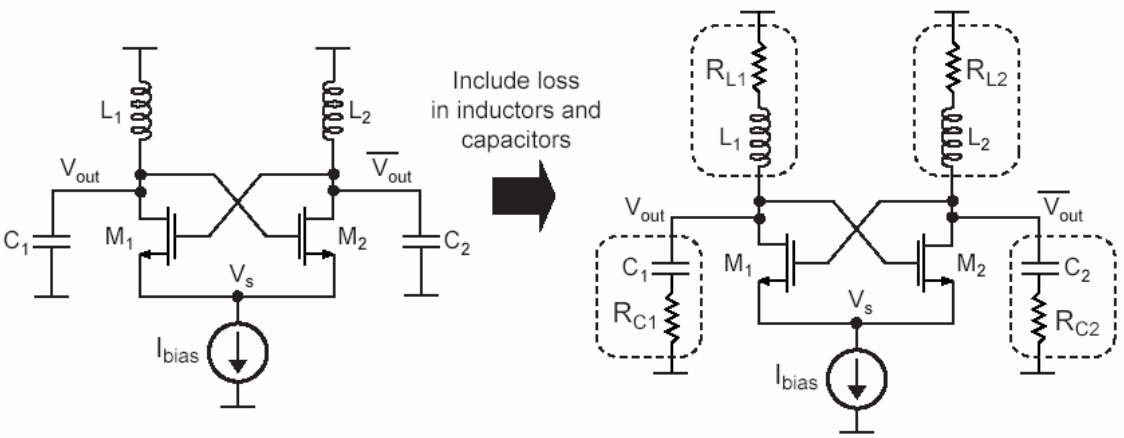


Figure 2-21 Cross-Coupled LC differential with parasitics included.

From a small-signal point of view, the cross-coupled transistor pair provides the negative resistance required to compensate for the losses in the LC tank circuit. Deriving the parallel RLC network that includes the loss of the tank inductor (Figure 2-22) and splitting the oscillator circuit into half circuits to simplify analysis the small-signal impedance looking into drains of M1 and M2 is $-2/g_m$ assuming the parasitic capacitance is neglected.

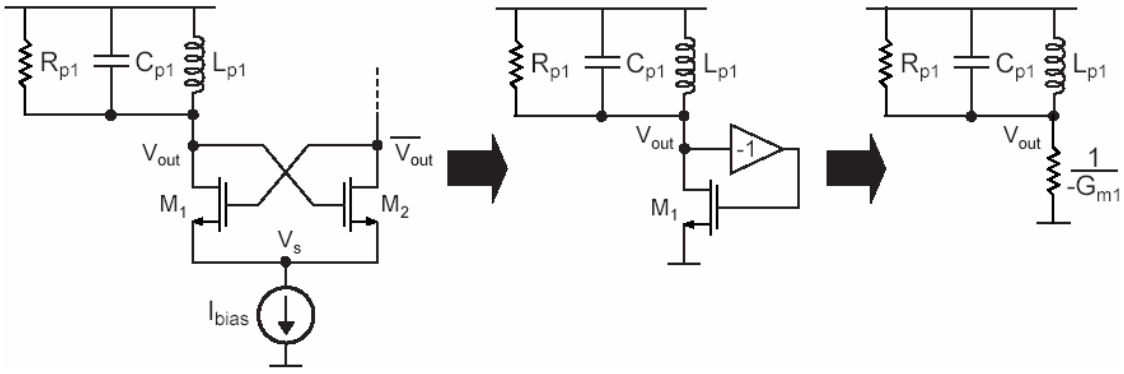


Figure 2-22 Equivalent circuit.

To enable oscillation, the negative small-signal conductance added by the cross-coupled transistor pair should overcome the loss in R_p; hence,

$$g_m > 1/R_p \Rightarrow g_m R_p > 1 \qquad (2.30)$$

The above inequality is commonly referred to as the ***start-up condition***. It imposes a lower bound on the power dissipation of the overall oscillator circuit. In practice, because process variations can be as large as 20%, a suitable safety margin (e.g., 3X) ensures reliable start-up over all possible operating conditions.

In order to calculate the oscillator's output voltage amplitude on the parallel resistance R_p we assume that the current flowing through M1, M2 is a square wave (Figure 2-23) and take into account that DC and harmonics are filtered by the tank.

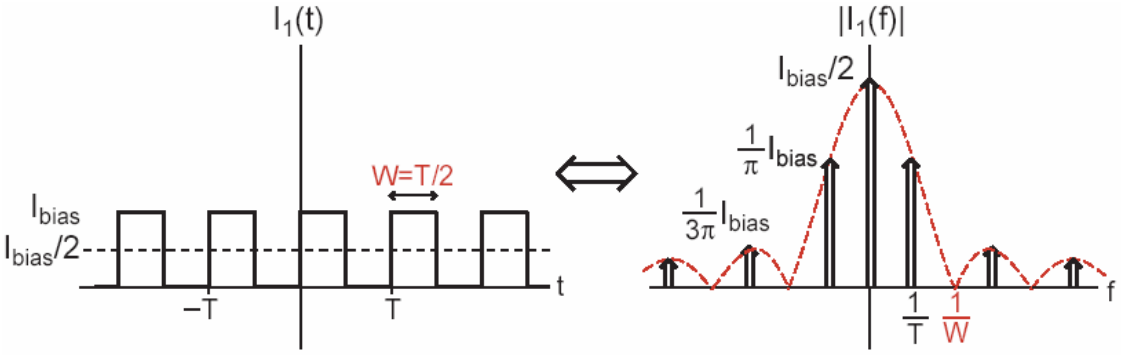


Figure 2-23 Oscillatory current waveform on time and frequency domain.

The fundamental current component is:

$$I_1(t) = \frac{2}{\pi} I_{bias} \sin(\omega_o t) \qquad (2.31)$$

Thus, the resulting oscillator amplitude is:

$$A = \frac{2}{\pi} I_{bias} R_p \qquad (2.32)$$

2.3.1.1 Cross-Coupled LC Oscillator Variations

Several variations of the basic cross-coupled configuration (Figure 2-21) have been proposed aiming at the minimization of phase noise at the topology level.

The current source in differential LC oscillators is required to set the bias current and provides high impedance in series with the switching active devices of the differential pair. In a perfectly balanced circuit, odd harmonics circulate in a differential path with no current flowing through the current source (out-of-phase

operation). At the same time, even harmonics flow in a common-mode path through the active devices, resonator circuit and current source (in-phase operation). Because of the mixing effect provided by the nonlinearities (nonlinear transconductance and intrinsic capacitances, i.e., C_{gd} of the current source transistor) of the oscillator transistors, the low frequency noise (***flicker noise***) of the current source is initially upconverted to high frequency noise around even harmonics and then downconverted to the phase noise around the fundamental. Since the level of the third and higher-order harmonics in the resonant LC oscillator is negligibly small, the effect of the second harmonic can be taken into account. Thus, to prevent the effect of current source low frequency noise modulation of the second harmonic, it is necessary to provide low impedance for the second harmonic. In other words, it is necessary to create a condition of current source bypassing for the second harmonic. Such an approach to the phase noise improvement is called a ***filtering technique***.

Several examples of the filtering technique applied to differential LC oscillators are given in [8]. The simplest circuit solution, which can be applied to the differential tail-biased oscillator shown in Figure 2-24.a, is to place the shunt capacitance C_s with a large value (resulting in a small reactance at the second harmonic) in parallel to the current source M_1.

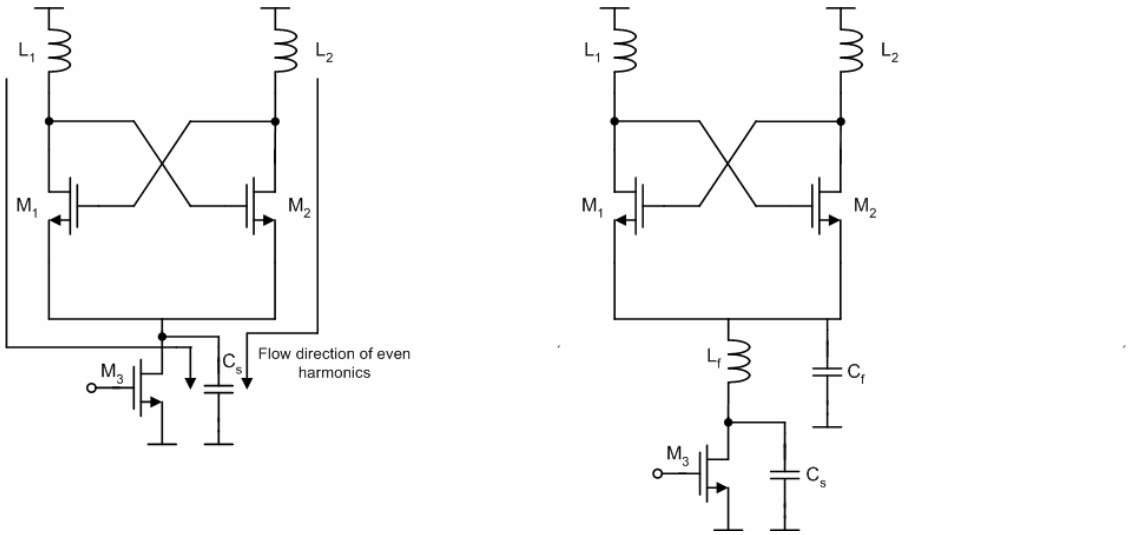


Figure 2-24 a) Tail-biased oscillator with capacitive noise filter, b) with complete noise filter.

However, care is required with the large value of shunt capacitance in order to eliminate the self-modulation phenomenon resulting in AM-FM conversion. As an alternative, inserting the series inductance between the current source and the tail creates high impedance for the second harmonic minimizing its contribution to the signal spectrum. Figure 2-24.b shows the circuit schematic with parallel filter based on the series inductance L_f connected in parallel to the capacitance C_f in addition to the shunt capacitance C_s. This parallel filter resonates on the second harmonic. Its impedance is limited only by the quality factor of the inductance. As a result, the inserted inductance and two capacitances comprise a complete noise filter for the tail-biased differential LC oscillator.

A variant of the tail-biased LC oscillator described previously is the top-biased differential LC oscillator (Figure 2-25.a). The current source is connected between the positive voltage supply and center tap of the differential inductor. From the principle of DC operation, both tail-biased and top-biased schematics are identical and the position of the current source can be exchanged. However, in a practical implementation, their RF performances are different. For instance, the top-biased oscillator is more immune to substrate noise because the current source is placed in an n-well, rather than in the substrate [8]. However, from an analysis of the flow directions of even harmonics shown in Figure 2-24.a it can be seen that the top-biased oscillator upconverts less flicker noise into phase noise around the fundamental frequency. This means that the level of the second harmonic flowing through the current source for the top-biased differential oscillator is less than for the tail-biased oscillator. To minimize the phase noise, the complete noise filter for the top-biased oscillator represents the large shunt capacitance connected in parallel to the current source and the second-harmonic filter comprising the parallel inductance L_f and capacitance C_f having high reactance at the second harmonic.

Figure 2-25.b shows the tail-biased differential oscillator using a low noise suppression technique, which includes inductive degeneration and low-pass filtering [9]. An off-chip degeneration inductor L_s is placed between the source of

the tail transistor M_3 and ground. In this case, the noise current power of the current source transistor is reduced by the factor of $[1+jg_m\omega L_s]^2$, where g_m is the transconductance of the transistor M_3.

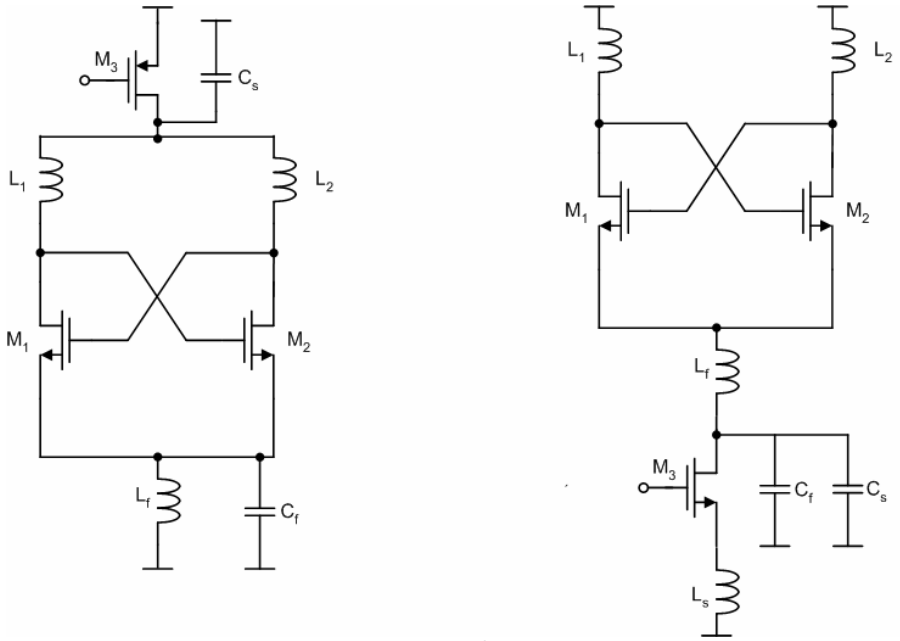


Figure 2-25 a) Top-biased oscillator, b) Oscillator with tail current noise suppression.

Another approach [10] employs a resistor for biasing of the basic configuration (Figure 2-21), avoiding in this way the common tail current source based on active circuitry (e.g., current mirrors in CMOS designs). This choice prevents the flicker device noise upconversion, leading to improved spectral purity in the $1/f^3$ region of the phase noise spectrum.

2.3.2 Colpitts Oscillator

A negative conductance can also be synthesized using only a single active device, which is highly desirable for noise consideration. The Colpitts configuration is one such one-transistor oscillator (Figure 2-26), in which the negative conductance is formed using transistor M_1 and capacitive divider C_1 and C_2 in a positive feedback arrangement.

It consists of a parallel LC tank with a capacitive voltage divider that produces a positive feedback while it reduces the loading on the tank (avoiding

degradation of the tank's Q factor) by increasing the negative resistance of NMOS transistor.

It can be shown that the small-signal impedance looking into the drain of M_1 is

$$\frac{V_x}{I_x} = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} - \frac{g_m}{\omega^2 C_1 C_2} \quad (2.33)$$

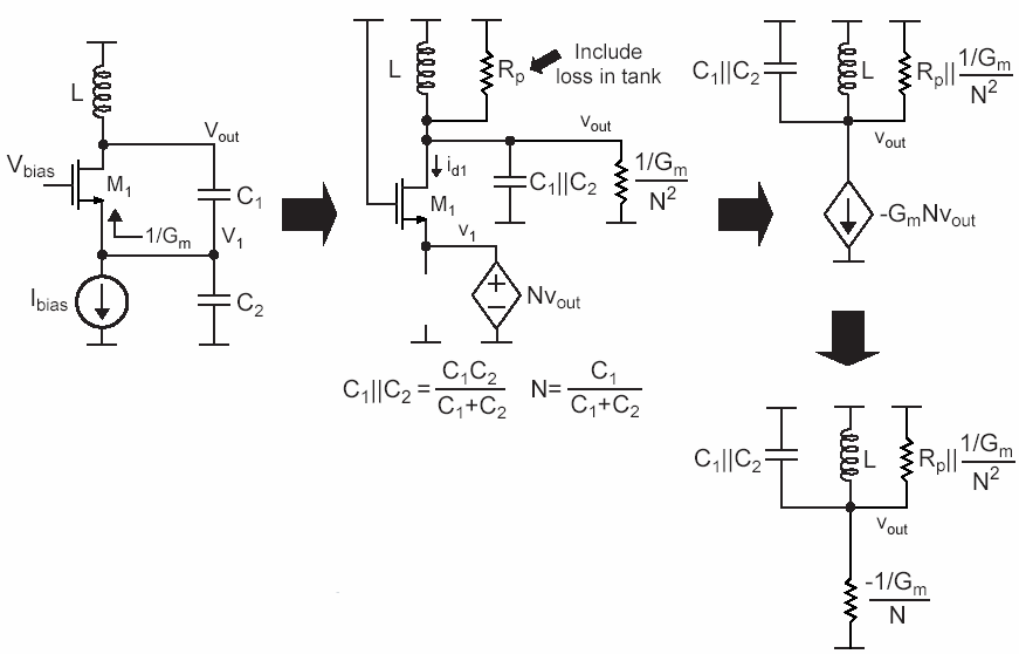


Figure 2-26 Colpitts oscillator – A simplified model.

Therefore, the interaction between M_1 and the capacitive divider C_1 and C_2 results in a small signal negative resistance of $-g_m/\omega^2 C_1 C_2$. The capacitive component loading the tank circuit is given by the series combination $C_1 C_2/(C_1 + C_2)$.

Performing a series to parallel transform, the negative conductance loading the tank is found to be

$$G_m = -\frac{g_m C_1 C_2}{C_1 + C_2} \quad (2.34)$$

Therefore, the start-up condition for the Colpitts oscillator is

$$\frac{g_m C_1 C_2}{C_1 + C_2} > \frac{1}{R_p} \Rightarrow g_m R_p > \frac{(C_1 + C_2)^2}{C_1 C_2} \quad (2.35)$$

Considering the typical condition $C_2 = 4C_1$ for best phase noise performance [4], (2.35) becomes $g_m R_p > 6.25$ (2.36)

The current flowing through M_1, M_2 consists of pulses whose shape and width are a function of the transistor behavior and transformer ratio $N = \frac{C_1}{C_1 + C_2}$ (Figure 2-27). It can be approximated by narrow wave pulses with width *W*.

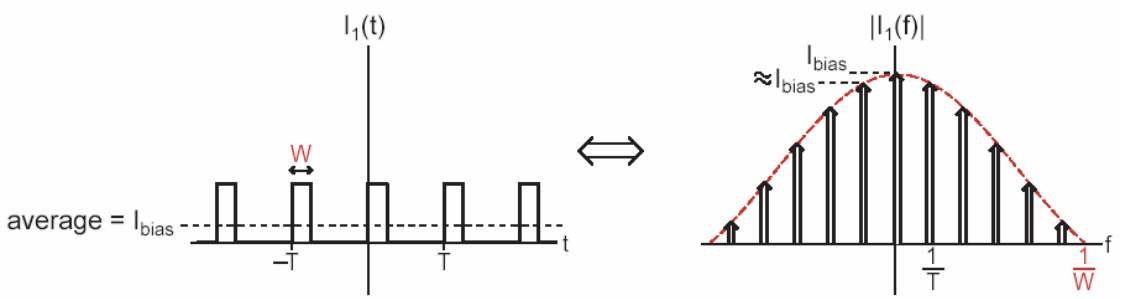


Figure 2-27 Oscillatory current waveform on time and frequency domain.

The fundamental current component is:

$$I_1(t) = 2I_{bias}\sin(\omega_o t) \qquad (2.36)$$

Thus, the resulting oscillator amplitude is:

$$A = 2I_{bias}R_{eq} \qquad (2.37)$$

where $$R_{eq} = R_p \,//\, \frac{1/G_m}{N_2} \qquad (2.38)$$

A differential output can also be provided by coupling two identical single-ended Colpitts oscillators and sharing their source-to-ground capacitors, as shown in Figure 2-28a). Since the center node where both capacitors are connected together is a differential virtual ground, the original operation of the oscillators remains unchanged when the two sides oscillate 180° out of phase. The differential operation will be guaranteed if the center node is left floating and is not grounded.

While this topology inherits the excellent phase noise performance of the single-ended structure, it also relaxes the start-up condition (2.35) by a factor of two as the effective small-signal transconductance is doubled, though at the expense of double power consumption if the same start-up condition is to be met.

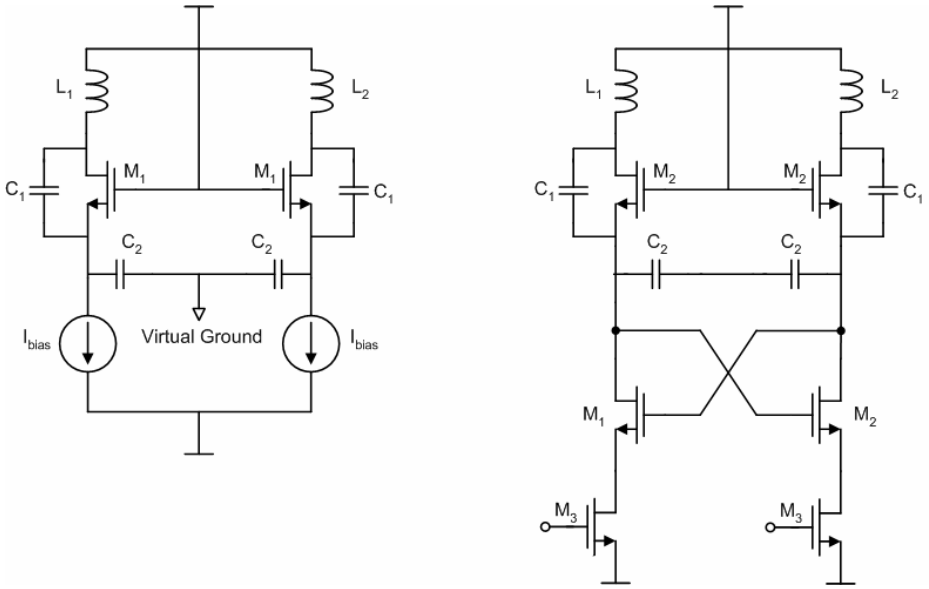


Figure 2-28 a) Differential Colpitts Oscillator, b) Power relaxed topology

In the conventional differential Colpitts oscillator (Figure 2-28a), the tail current source is always ON. To reduce power consumption, a switching current source can be employed [11]. The key point is that because in a Colpitts oscillator the MOSFET is ON for less than half of a cycle, two switches can be used to steer one current source to the two MOSFETs while sustaining oscillation (Figure 2-28b).

2.3.3 Comparison of Cross-Coupled and Colpitts Oscillators

Comparing the start-up conditions for the Cross-Coupled and single-ended Colpitts oscillators, given in (2.30) and (2.36) respectively, it is apparent that the former can easily start-up oscillations contrary to the latter. Thus, a higher small-signal transconductance and therefore greater power consumption are required for the Colpitts oscillator to achieve reliable start-up.

This issue is overcome by the differential Colpitts oscillator where the start-up condition has been significantly reduced and lies close to that of the Cross-

Coupled oscillator. At the same time a bias current switching strategy decreases the required power consumption. Although the differential Colpitts oscillator improves significantly the power performance with respect to the single-ended one, it remains more power hungry than the Cross-Coupled oscillator.

On the other hand, the Colpitts oscillator has better cyclostationary noise properties, i.e., the maximum noise generation instant is aligned with the oscillator's minimum sensitivity point and can hence potentially achieve lower phase noise [11] (Figure 2-29). Also, the Colpitts oscillator presents a smaller rms and dc value of its effective ISF than the Cross-Coupled oscillator. A more symmetrical effective ISF will significantly reduce the up-conversion of the low-frequency noise of the transistor [5].

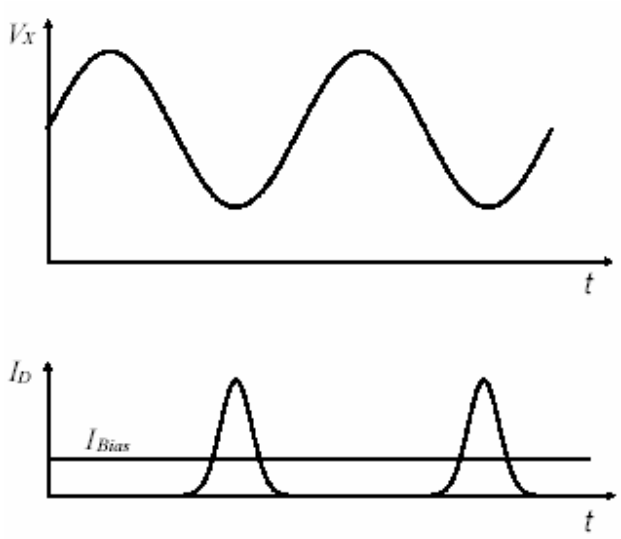


Figure 2-29 Voltage and Current waveforms of Colpitts Oscillator.

While the better cyclostationary properties of an oscillator alone would enhance the phase noise performance, a large oscillation amplitude results in improved phase noise. In that sense the Colpitts oscillator is superior to the Cross-Coupled pair as it exhibits an output voltage amplitude significantly higher for a given bias current.

$$A_{Colpitts-diff} = 4R_{\tan k} I_{bias} > A_{cross-coupled} = \frac{2}{\pi} R_{\tan k} I_{bias} \qquad (2.39)$$

Despite the apparent superiority that the Colpitts oscillator presents in phase noise performance, in a comparison [12] between Cross-Coupled and Differential

Colpitts oscillators, taking use of the ISF theory, it has been shown that the first presents better phase noise performance beyond the $1/f^2$ region.

It must be underlined that the same noise sources impact differently the phase noise performance of each circuit. This means that in different topologies, different mechanisms are usually responsible for degrading phase noise. For example, the low frequency noise contribution of the tail current source of a Colpitts oscillator (Figure 2.28b) is negligible, while this is not the case for the Cross-Coupled oscillator (Section 2.3.1.1). This means that the Colpitts topology upconverts less flicker noise than the Cross-Coupled around the carrier's frequency.

2.3.4 Quadrature Oscillators

Quadrature down-conversion is often required in direct conversion, image reject and wideband IF receiver architectures. There are several choices for this purpose. For example, quadrature operation can be achieved using frequency division from an oscillator operating at twice the desired LO frequency. The drawbacks of this approach are that the oscillator operates at a higher than needed frequency and the additional frequency division circuitry also consumes additional power.

The quadrature LO signals can also be synthesized by applying differential signals from an oscillator to an RC polyphase filter [13]. Unfortunately, undesirable attenuation from the passive RC filter necessitates the use of buffers and therefore entails higher power consumption.

The third choice comes at the cost of double oscillator die area and it is based on quadrature signals generation through the use of a quadrature VCO, which is essentially a pair of oscillators coupled to each other so that it outputs quadrature signals directly [14][15]. This option outperforms the other solutions in terms of power consumption.

There are many ways to achieve quadrature coupling of two independent VCOs to obtain quadrature oscillation; e.g., parallel or series. The key point is that the unidirectional coupling between the two VCOs should always be in an inverse sense. A parallel and a serial coupled quadrature oscillator are shown in Figures 2-30 and 2-31 respectively.

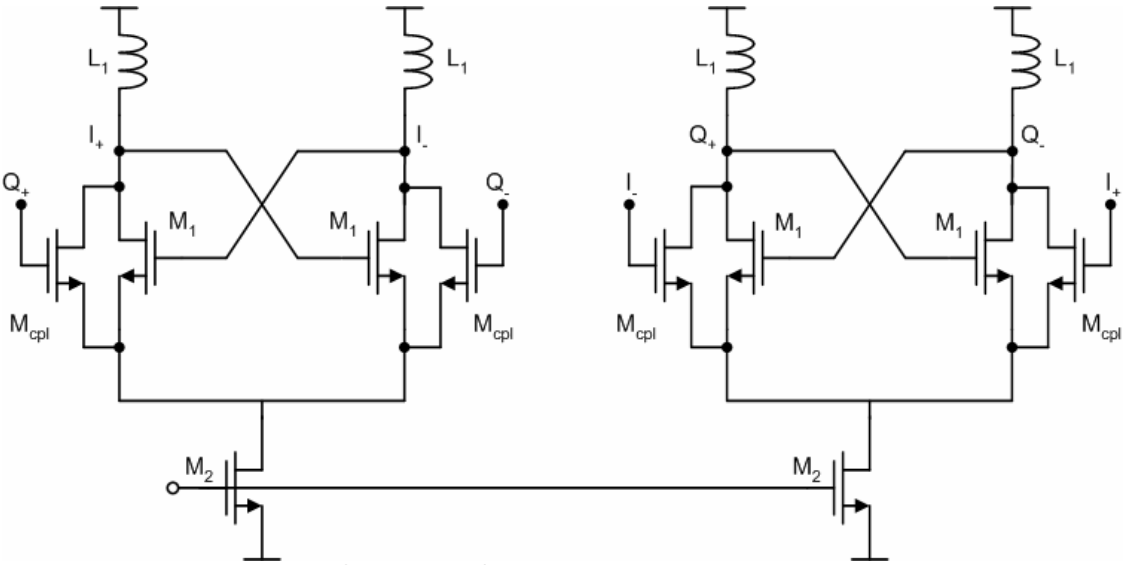


Figure 2-30 Parallel coupled Quadrature Oscillator.

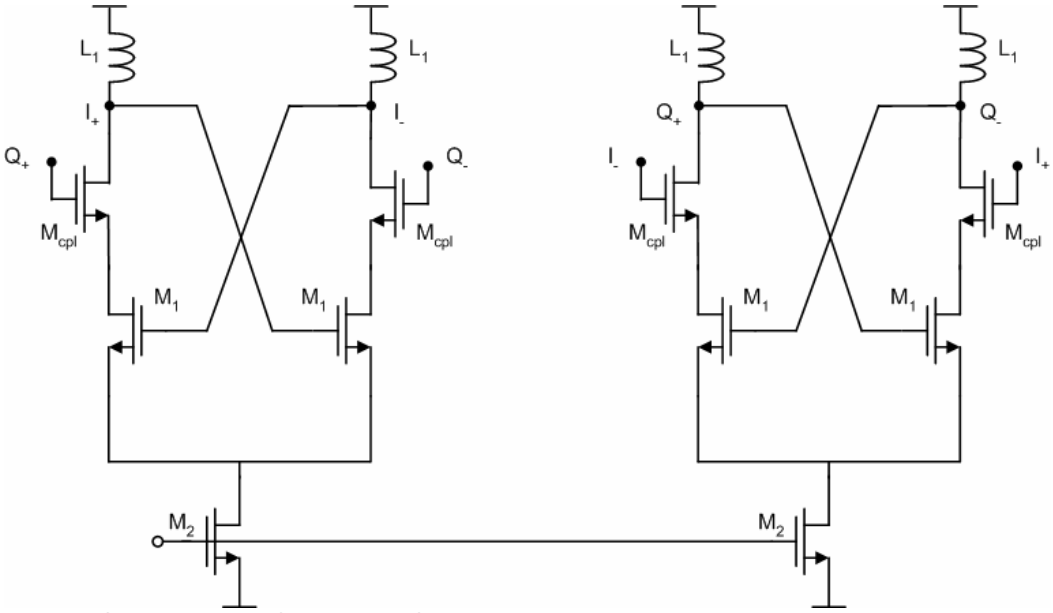


Figure 2-31 Serial coupled Quadrature Oscillator.

Serial coupling [14] is motivated by the consideration that M_{cpl} in the P-QVCO is responsible for a large contribution to the overall phase noise, and connecting M_{cpl} in series with M_1, in a cascode-like fashion, should greatly reduce the noise from the cascode device. This serial way of coupling displays excellent phase noise behavior.

An important factor that affects both phase noise and phase error performance of the mentioned QVCOs is the coupling ratio *a* which is defined as the ratio between the negative resistance transistor M_1 and the coupling transistor M_{cpl}, thus

$$a = \frac{M_1}{M_{cpl}} \quad (2.40)$$

The optimum range of values are *a* = 0.2 – 0.35 for the parallel case [15] and 3 – 5 for the serial case[14].

Figure 2-32 introduces a linear model for the P-QVCO, where G_m represents the transconductance of the negative-resistance pair M_1, and G_c the transconductance of the coupling pair M_{cpl}. Referring to this figure, we consider voltage and current signals to be fully differential: the current flowing into the tank is the difference between the currents in the two branches of the differential stage. As a consequence, R_p is the loss resistance of one half-tank.

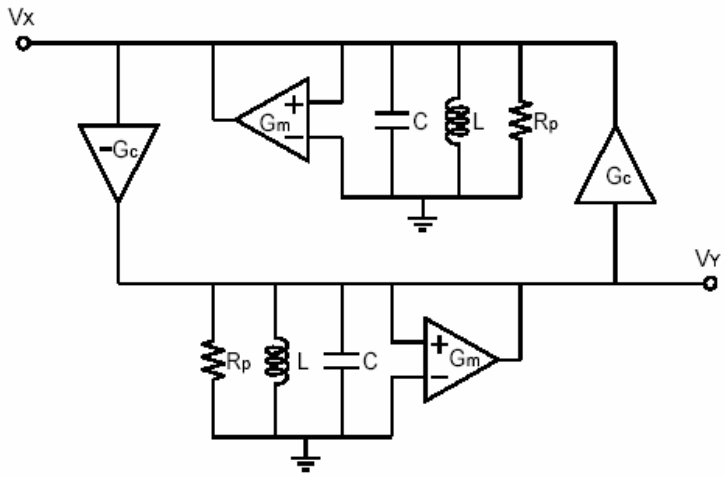


Figure 2-32 Linear model of Quadrature Oscillator.

The oscillation frequency ω_{out} results slightly displaced from the tank resonance $\omega_0 = 1/LC$ by an offset $\Delta\omega$ due to $\pi/2$ delay at nodes V_x and V_y, its magnitude depends on G_c.

Referring to V_x in Figure 2-32, the losses in tank-X are balanced by a current in phase with V_x, $I_I = G_m V_x = V_x / R_p$, which is provided by G_m. The tank is now lossless, and the current from G_c acts on an ideal LC-parallel. This second current, I_Q, is thus in quadrature with V_x, which in turn implies that V_x and V_y are phase shifted by $\pi/2$.

In order to find the oscillation frequency for the linearized QVCO circuit in Figure 2-32, the loop gain must first be calculated. The loop gain is given by

$$G_{loop}(s) = -G_c^2 \left(\frac{sL}{1 + sL\left(1/R_p - G_m\right) + s^2 LC} \right)^2 \quad (2.41)$$

According to Barkhausen's criteria, the circuit oscillates when the condition $G_m = 1/R_p$ is satisfied. Thus, by multiplication of (2.35) by R_p and equation with one, two possible oscillation frequencies result:

$$\omega_1 \approx \omega_o + \frac{G_c}{2C}\ ,\ \omega_2 \approx \omega_o - \frac{G_c}{2C} \quad (2.42)$$

Chapter 3 : Design of Variable Gain Amplifier

3.1 Gain and Bandwidth Specifications

A simple differential amplifier is given in Figure 3-1. The gain of the amplifier is given by

$$A_v = g_m\left(r_{o2} \,//\, r_{o4}\right) \qquad (3.1)$$

where g_m is the transconductance of the input transistors M_1 and M_2. The –3dB bandwidth is given by

$$\omega_{-3dB} = \frac{1}{C_L\left(r_{o2} \,//\, r_{o4}\right)} \qquad (3.2)$$

Equations (3.1) and (3.2) indicate that the gain of the amplifier is directly proportional and the -3dB bandwidth is inversely proportional to its output resistance, leading to a trade-off between the maximum gain that can be achieved and the speed of the amplifier. Two stage amplifiers could be implemented to obtain higher gain, at the cost of additional poles and increased power consumption.

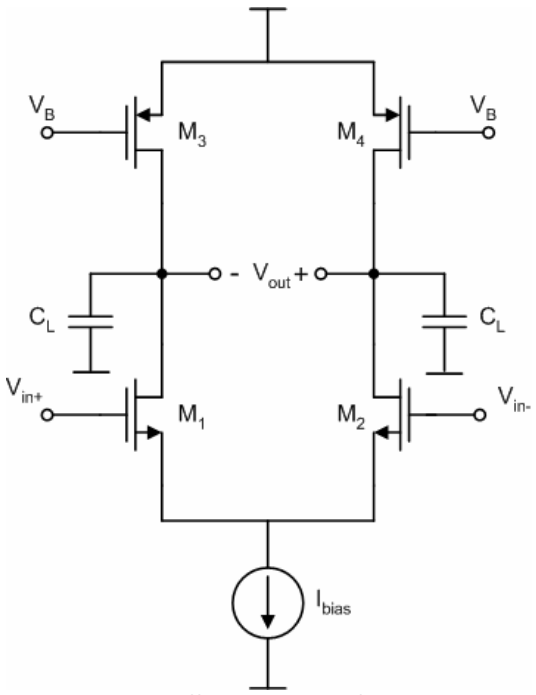


Figure 3-1 Differential amplifier with active load.

A. Cascoding

By compromising the output voltage swing, the same gain as a two-stage amplifier could be obtained by using a cascode structure with lower power dissipation.

The gain of the cascode stage shown in Fig. 3 is given by

$$A_v = g_{m1} g_{m2} r_{o1} r_{o2} \quad (3.3)$$

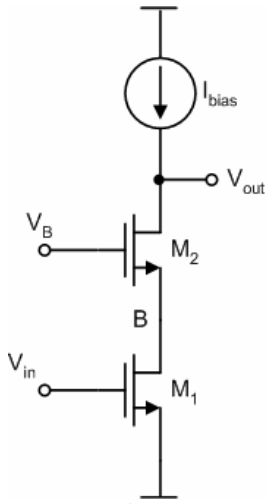


Figure 3-2 Cascode amplifier.

An advantage of the cascode structure over a common-source stage is the significant reduction in the Miller effect observed by the gate-drain capacitor C_{GD1} due to the low impedance seen by the capacitor, looking into node B, for small values of R_D [16]. The pole associated with the capacitors at node B is given approximately by

$$\omega_{-3dB} \approx \frac{g_{m2}}{2C_{GD1} + C_{GS2}} \quad (3.4)$$

This normally results in a better frequency response of the cascode structure as compared to a simple common-source amplifier. A disadvantage of the cascode structure is its limited output voltage swing, and consequently it is not used frequently in low voltage applications. Higher voltage swing can be obtained by using a folded cascode structure as shown in Fig. 4. The primary advantage of this topology is the availability of more headroom for the transistors, hence avoiding stacking of the cascode transistor on top of the input device. However,

the folded cascode amplifier generally provides lower gain at lower bandwidth (due to lowering of the pole at the folding point) while consuming higher power.

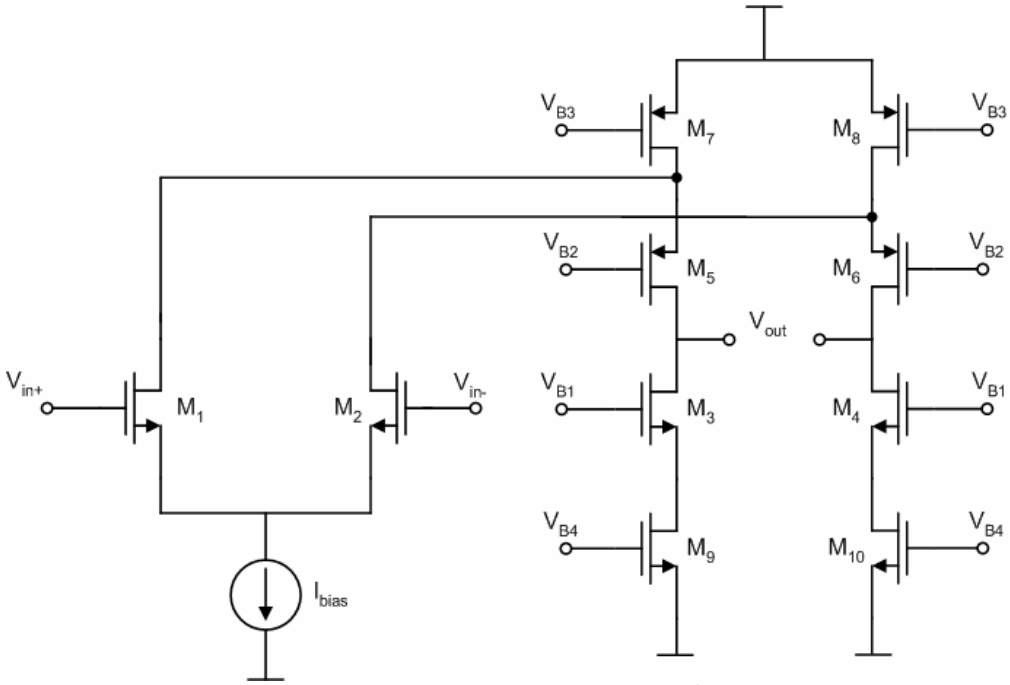


Figure 3-3 Folded cascode amplifier.

B. Capacitive neutralization to increase bandwidth

One of the commonly used techniques other than cascoding to reduce the Miller effect experienced by the gate-to-drain capacitor of the input transistors in a fully differential amplifier is capacitive neutralization [17], which is illustrated in Fig. 6. This technique is sometimes used in wideband circuits to increase the bandwidth of multi-stage amplifiers [18].

Without including capacitance C_{GDN}, the capacitance seen at the gate of transistor M_1 is given by:

$$C_{in} = C_{GS1} + C_{GD1}(1 - A_v) \quad (3.5)$$

where Av is the gain from the gate to the drain of M_1. Since the amplifier is perfectly balanced, the gain from the gate of M_1 to the drain of M_2 is $-Av$. As a result, the total capacitance at the gate of M_1 after including capacitor C_{GDN} in the circuit is given by

$$C_{in} = C_{GS1} + C_{GD1}(1 - A_v) + C_{GDN}(1 + A_v) \quad (3.6)$$

If the value of C_{GDN} is selected such that $C_{GDN} = C_{GD1}$, equation (3.6) simplifies to

$$C_{in} = C_{GS1} + 2C_{GD1} \quad (3.7)$$

This is very similar to the input capacitance of a cascode configuration.

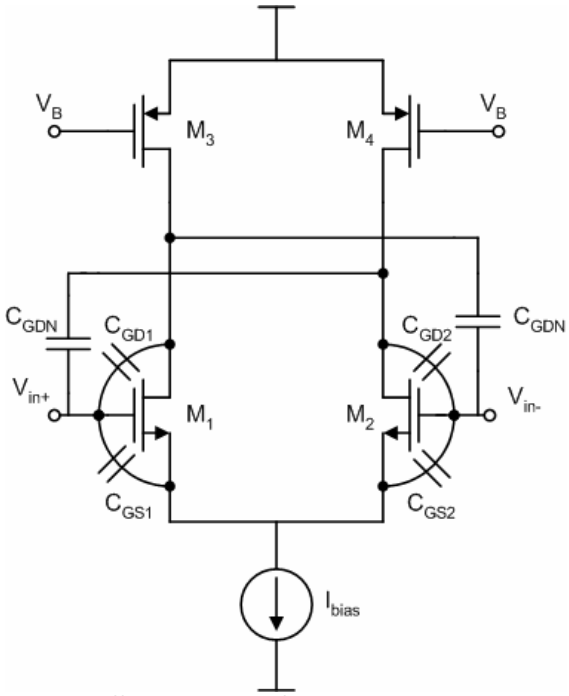


Figure 3-4 Differential amplifier with capacitive neutralization.

C. Gain boosting in differential amplifiers with diode connected loads

In differential pair amplifiers with diode-connected loads, the loads consume voltage headroom, limiting the output voltage swing, gain and the input common mode range. In order to obtain a higher gain, the transconductance of the load transistor has to be decreased. This can be done by decreasing the W/L value of the load. However, a disadvantage of this solution is the corresponding increase in the overdrive voltage, which in turn lowers the output common mode level as well as the voltage swing. This problem can be avoided by adding MOS current sources [16] in parallel to the load transistors, as indicated in Figure 3-5. Since the current is now split between the load and the current source, the W/L value of the load transistor can be decreased without changing the overdrive voltage.

Hence, the transconductance of the load can be decreased without compromising the output voltage swing.

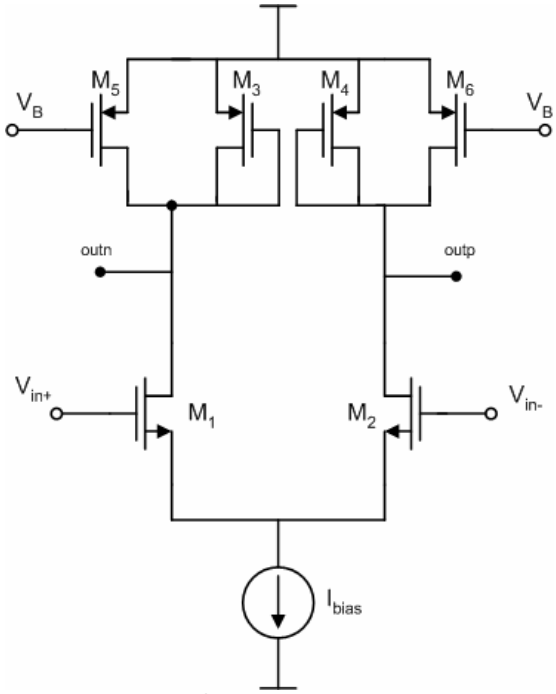


Figure 3-5 Addition of current sources to increase the gain of differential amplifier with diode connected load.

If transistors M_5 and M_6 of Figure 3-5 carry 40% of the drain current of M_1 and M_2, and the load transistors M_3 and M_4 carry the remaining 60%, their transconductance decreases by a factor of 2/5 since the W/L ratios of M_3 and M_4 can also be decreased by the same amount without affecting their overdrive voltage. Thus, the differential gain increases by approximately 5/2 times compared to the case when the PMOS current sources are not included in the circuit. A disadvantage of this method of increasing the gain is that the current sources add parasitic capacitances to the output node of the circuit, slightly lowering the -3dB bandwidth.

3.2 Conventional Variable Gain Amplifier Design

The core of the conventional VGA topology that is widely used [19,20,21,22] is shown in Figure 3-6. It consists of a differential amplifier ($M_{1,2}$) and diode-connected loads ($M_{5,6}$). The differential gain of this VGA is equal to

$$A_v = g_{m-M1,2} \times R_{out} \quad (3.8)$$

where the output resistance R_{out} is proportional to $1/g_{m-M5,6}$.

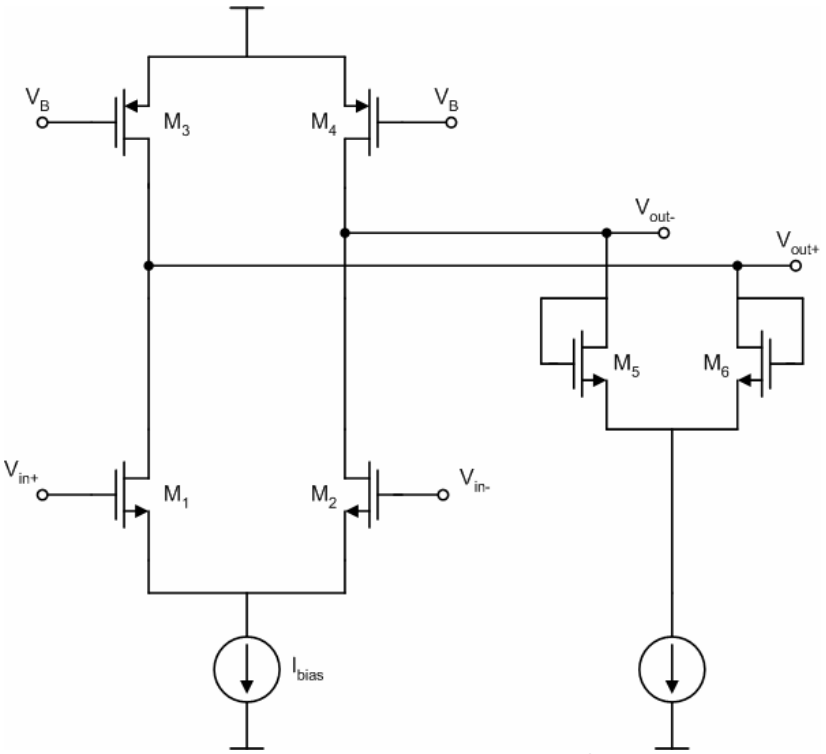


Figure 3-6 Variable gain amplifier core.

Since the transconductance is a function of the bias current, the gain variation is obtained by controlling the bias currents of the input-pair ($M_{1,2}$) and loads ($M_{5,6}$). The gain of the VGA shown in Figure 3-6 is given by

$$A_v = \frac{g_{m-M1,2}}{g_{m-M5,6}} = \sqrt{\frac{(W/L)_{M1,2} I_{M1,2}}{(W/L)_{M5,6} I_{M5,6}}} \quad (3.9)$$

Considering the frequency response of the circuit shown in Figure 3-6, the bandwidth of the VGA is dominated by the input and output poles. Since the output loads are diode-connected transistors, the output pole is mainly

dependent on the bias current of the transistors $M_{5,6}$. At a lower gain setting, $I_{M5,6}$ and the bandwidth are extended. However, at a higher gain setting, $I_{M5,6}$ is reduced, reducing the bandwidth [21]. The input pole is a function of input capacitances. In Figure 3-6, the total capacitances at the input node of M_1 is equal to C_{GS} plus Miller multiplication of C_{GD}: $C_{GS}+\left(1+\left|A_v\right|C_{GD}\right)$, where C_{GS} and C_{GD} are the gate-source and gate-drain capacitances of transistor M_1, A_v is given in (3.9). Consequently, the input pole is proportional to the gain A_v that the bandwidth is reduced significantly at higher settings.

Another approach for VGA design, shown in Figure 3-7, is based on ***current steering*** [23,24,25]. While it does not incorporate a diode-connected load, it uses differential cascode transistors to steer current to and from the load. The advantage of this approach is that it allows a high gain control range, and the disadvantage is that it tends to suffer more from noise.

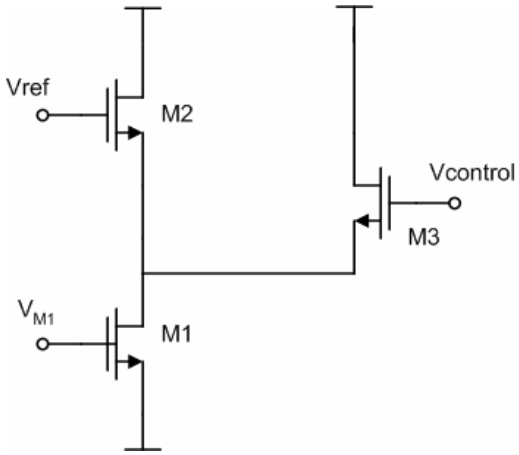
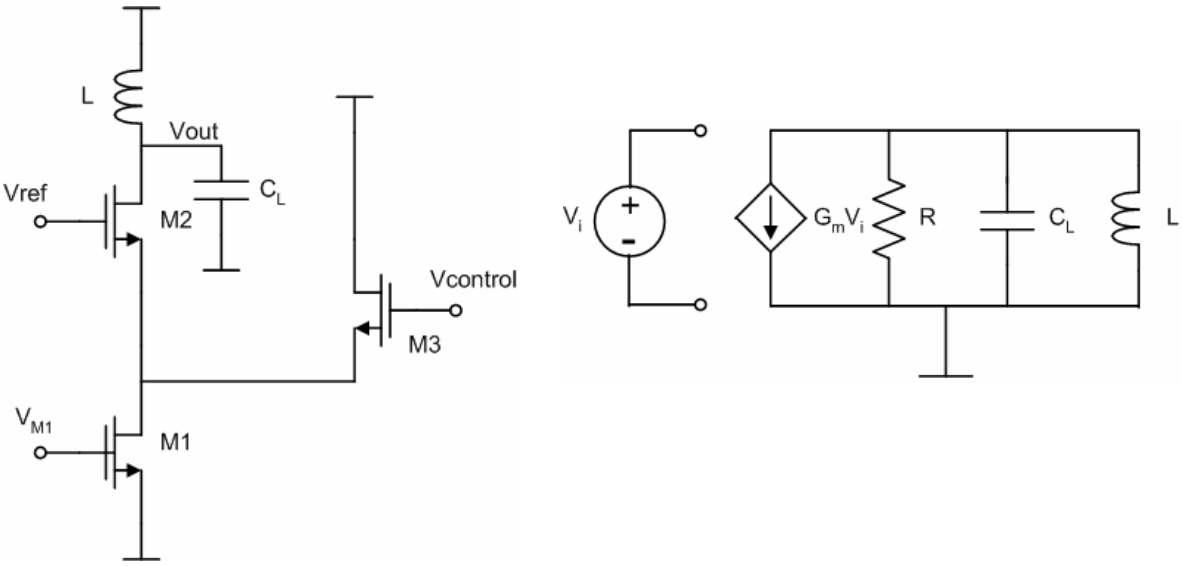


Figure 3-7 Current steering variable gain amplifier.

3.3 Tuned Variable Gain Amplifier

While the previous amplifiers have a frequency response around zero, in RF design, amplification around much higher center frequencies is needed.

The basic principle of operation behind the design of tuned variable gain amplifiers is the use of a parallel LC tank as a load on the output node of an active gain cell, such as those in previous figures (Figure 3-8a) [26]. The parallel LC tank acts as a bandpass filter, the pass band zone of which is amplified by the gain of the active cell. The properties of such circuits are similar to those mentioned previously extended by the center frequency of operation ω_o, the 1dB or 3dB bandwidth *B*, and the range of the pass band zone known as ***selectivity***, which is determined by the quality factor *Q* of the LC tank and is defined either as the ratio of the 30dB bandwidth to the 3dB bandwidth or that associated with



1dB.

Figure 3-8 a) Tuned current steering variable gain amplifier, b) Small signal model.

The small signal equivalent circuit of the tuned variable gain amplifier of Figure 3-8a is illustrated in Figure 3-8b. From Figure 3-9 it follows that

$$V_o = \frac{-G_m V_i}{Y_L} = \frac{-G_m V_i}{sC + 1/R + 1/sL}$$

$$\Rightarrow \frac{V_o}{V_i} = \frac{-G_m}{C} \frac{s}{s^2 + s(1/CR) + 1/LC} \quad (3.10)$$

Equation (3.10) is a second order bandpass function with a center frequency of

$$\omega_o = 1/\sqrt{LC} \quad (3.11)$$

The 3dB bandwidth is given by

$$B = 1/CR \quad (3.12)$$

The quality factor *Q* is given by

$$Q = \omega_o/B = \omega_o CR \quad (3.13)$$

and the center frequency voltage gain by

$$A_v = -G_m R \quad (3.14)$$

3.4 Noise–to–Power Ratio

In communication systems, the linearity of amplifiers is normally measured by evaluating the third order input intercept point (IIP3). Due to the inherent non-linearity of amplifiers, an input signal *x(t)* results in an output as given below:

$$y(t) = k_o + k_1 x(t) + k_2 x^2(t) + k_3 x^3(t) \quad (3.15)$$

The above relation is based on the assumption that the circuit is memoryless and is driven by a small signal excitation reasonably below the 1 dB compression point (1 dB compression point is the point at which the gain deviates from its ideal small signal value by 1dB). It follows from equation (3.15) that when the input signal is of the form $x(t) = x\cos(\omega_1 t) + x\cos(\omega_2 t)$, the in-band output of interest is [19]:

$$y_{in-band} = k_1 x[\cos(\omega_1 t) + \cos(\omega_2 t)] + \frac{k_3}{4} x^3 \left\{ \begin{matrix} 9\cos(\omega_1 t) + 9\cos(\omega_2 t) + \\ 3[\cos(2\omega_2 - \omega_1)t + \cos(2\omega_1 - \omega_2)t] \end{matrix} \right\} \quad (3.16)$$

It can be observed from the above equation that the third order distortion components include nine new mixing products at ω_1 and ω_2 and three at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. The components at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are the intermodulation distortion components.

The fundamental component in equation (3.16) increases with a slope of 1dB/dB while the third order intermodulation component rises at a rate of 3dB/dB with respect to the input power. The third order input intercept point is defined as the input power for which the distortion power at $2\omega_1 - \omega_2$ (or $2\omega_2 - \omega_1$) is the

same as the linear output power at ω_1 (or ω_2). Normalized to a 1Ω load resistance, the IIP3 is given by:

$$x_{IIP3}^2 = \frac{4}{3}\frac{k_1}{k_3} \quad (3.17)$$

The intermodulation distortion ratio (IMR) is defined as the ratio between the linear output power per tone and the output power of adjacent channel tones. The value of the two-tone IMR normalized to the total linear output power is:

$$IMR_{two-tone} = \frac{\frac{k_1^2}{2}x^2}{9\frac{k_3^2}{32}x^6} = \frac{16}{9}\frac{k_1^2}{k_3^2}\frac{1}{x^4} \quad (3.18)$$

With increasing complexity of communication systems, the two-tone standard is no longer a sufficient test for the linearity of amplifiers used in such systems. More robust figures of merit that give better representations of the system's final operation are used to characterize circuits [27], [28]. The measurement setup includes excitation of the circuit with a multi-tone signal in which all the tones are equally spaced and have uncorrelated phases. These figures of merit include:

1. ***Adjacent Channel Power Ratio (ACPR)*** – This is the ratio between the adjacent channel (upper or lower) integrated output power and the total linear output power of the useful signal band.

2. ***Noise-to-Power Ratio (NPR)*** – NPR is the ratio between the in-band distortion and the useful signal power per tone when the circuit is excited with a multi tone signal that has a prelocated notch (i.e. a slice of the signal spectrum is removed).

3. ***M-IMR*** – This is the ratio between the linear output power and the highest distortion tone power outside but close to the useful band. M refers to the number of tones used in the input signal.

4. ***Co-channel Power Ratio (CCPR***) – CCPR is the ratio between the total distortion power collected in the input bandwidth and the total linear output power. CCP cannot be directly measured because the in-band distortion components are normally masked by the circuit's linear output component.

Unlike the NPR test, the CCPR does not involve shutting down of any tone, and the distortion in that particular band is measured in the presence of the corresponding input spectral line. Hence, the CCPR is a more accurate estimate of the in-band distortion due to the non-linear components that arise when the circuit is excited by a multi tone input. The measured value of NPR is normally lower than the actual value by about 6dB.

Chapter 4 : Optimization

Several automated design techniques have been reported to date on RF IC design. In [29], VCOOPT, a tool that optimizes phase noise of an NMOS transistor and a complementary VCO was presented. It employed Cadence's Spectre RF™ circuit simulator as an evaluation tool for the phase noise, the Quasi-Newton method as an optimizing algorithm and the electromagnetic solver ASITIC [30] to calculate the losses of the on-chip spiral inductor. While this technique optimizes phase noise, it does not optimize the bias current [12]. At the same time it requires an initial guess for the sizing of the MOS transistors in the gain cell, the geometrical parameters of the spiral inductor and the value of the capacitance of the tank.

In [31], AMIGO, a simulation based automated synthesis of integrated LC VCOs employing genetic algorithms as an optimization algorithm is presented. This tool does not require initial guesses, provides the best values of the variables that satisfy certain design constraints but the topological parameters of the coil and the sizing parameters of the MOS varactor are not incorporated in the optimization process.

In [32] an equation based method for optimizing and automating component and transistor sizing for a CMOS LC oscillator is reported using geometric programming. This approach enables the designer to explore in a short period of time the globally optimal trade-off curves such as among phase-noise and bias current. While analytical expressions are easy to use, they yield only approximate results.

In [33], CYCLONE, a tool for automated design and layout of LC-oscillators, phase noise is optimized with minimal power consumption, taking into account the trade-offs between phase noise and power consumption. An electromagnetic solver is used to calculate the losses of the on-chip inductor, analytical expressions are used to estimate phase noise and simulated annealing is used as an optimizing algorithm. Since this is implemented in a single step, the

optimizer demands many iterations of relatively long simulations, in order to assess the design space and effectively derive an optimum.

In our approach all design variables are assessed in the optimization process. A circuit simulator based on BSIM3v3.2.4 model accuracy evaluates the circuit's performance while the GA based optimization algorithm converges very close to the global optimum solution. The procedure does not require initial guesses. Moreover, in order to reduce the complexity of the problem, facilitate convergence, minimize simulation time and leverage prior knowledge in design synthesis [34], we split the optimization procedure in several steps.

Contrary to the mentioned approaches where the optimizer is viewed as a black box adopting a knowledge free approach, our methodology offers the means to make the resultant circuit more predictable and readily monitored by the designer leading to intuitive automated circuit design.

4.1 System Description

Our methodology, illustrated in Figure 4-1, incorporates the use of a circuit evaluation tool, an optimizing algorithm and a fitness function. The latter reflects designer expertise and drives the optimization process improving computational efficiency and simulation time.

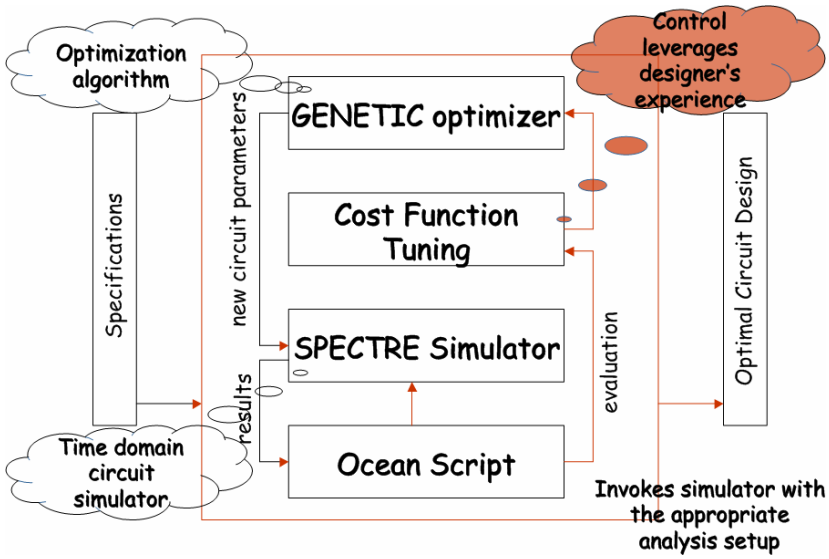


Figure 4-1 Overall system.

4.1.1 Evaluation Tool

To establish an automated optimization procedure, the selected simulator (Spectre RF™) is invoked through the use of scripts outside the graphical user interface. The scripts were written in Ocean™ [35], a built-in Cadence language that allows users to specify a list of analyses in one or more designs and instruct the simulator to perform them. Subsequently, results can be processed by equations included in the script, i.e. fitness functions etc.

4.1.2 Optimizing Algorithm

We chose to employ a ***Genetic Algorithm*** (GA) based optimizer [36-39],. The genetic algorithm is a method for solving optimization problems that is based on natural selection, the process that drives biological evolution. In GA, each unknown circuit design variable is called ***gene*** and the vector of design variables ***chromosome***. It repeatedly modifies a population of individual solutions, chromosomes; ***a population*** is a group of randomly initialized chromosomes. At each step, the genetic algorithm selects chromosomes (or individuals) at random from the current population to be parents and uses them to produce the children for the next generation. Over successive generations, the population "evolves" toward an optimal solution. The genetic algorithm can be applied to solve a variety of optimization problems that are not well suited for standard optimization algorithms, including problems in which the objective function is discontinuous, nondifferentiable, stochastic, or highly nonlinear.

The genetic algorithm uses three main types of rules at each step to create the next generation from the current population:

- ***Selection rules*** select the individuals, called parents that contribute to the population at the next generation.
- ***Crossover rules*** combine two parents to form children for the next generation.
- ***Mutation rules*** apply random changes to individual parents to form children.

At each step, the genetic algorithm uses the current population to create the children that make up the next generation. The algorithm selects a group of chromosomes in the current population, called parents, who contribute their genes to their children. The algorithm usually selects chromosomes that have better fitness values as parents.

The genetic algorithm creates three types of children for the next generation:

- ***Elite children*** are the individuals in the current generation with the best fitness values. These individuals automatically survive to the next generation.
- ***Crossover children*** are created by combining the vectors of a pair of parents.
- ***Mutation children*** are created by introducing random changes, or mutations, to a single parent.

The algorithm shown in Figure 4-2 works like:

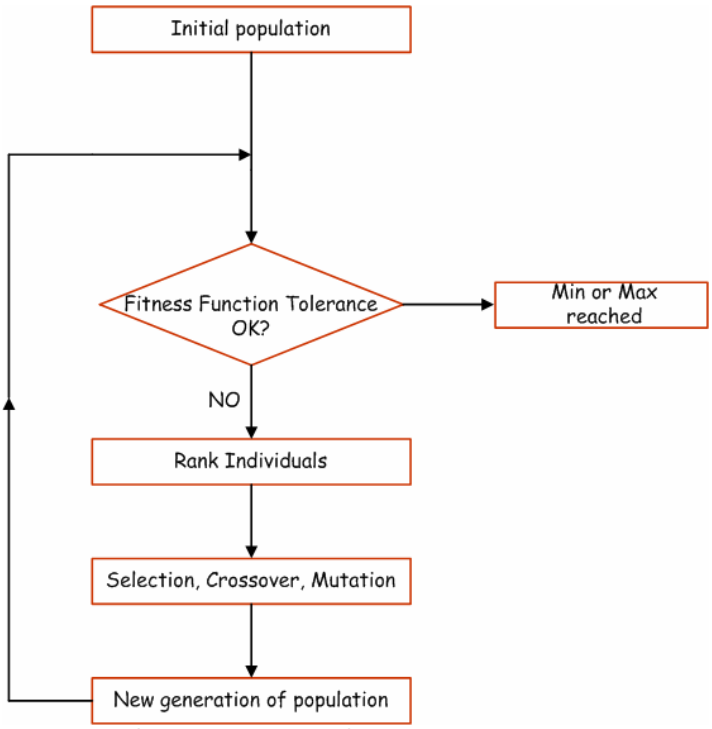


Figure 4-2 Genetic Algorithm Optimizer.

1) The algorithm begins by creating a random initial population.
2) The algorithm then creates a sequence of new populations, or generations. At each step, the algorithm uses the individuals in the current generation to

create the next generation. To create the new generation, the algorithm performs the following steps:

i) Scores each member of the current population by computing its fitness value.
ii) Scales the raw fitness scores to convert them into a more usable range of values.
iii) Selects parents based on their fitness.
iv) Produces children from the parents. Children are produced either by making random changes to a single parent -- mutation -- or by combining the vector entries of a pair of parents -- crossover.
v) Replaces the current population with the children to form the next generation.

3) The algorithm stops when the value of the fitness function stops varying for a certain number of evaluations.

GA is advantageous over conventional optimizing algorithms. The latter have some shortcomings that need to be overcome, which are as follows [38]:

- An initial guess is normally required, followed by an iterative method to approach an extremum. It is difficult to find a quick path approaching the near global extremum without confusion by local extrema, especially when the process should be suitable for general needs, independent from any individual case.
- Conventional algorithms are useful over a relatively narrow value probability range.

On the contrary GA does not require initial guesses or derivative information and selecting the next population of solutions by computations that involve random choices is capable of skipping local minima and settle to a near globally optimum solution.

The algorithm is implemented [40] in octave, a matlab open source equivalent and is integrated to the ocean environment through ocean text scripts.

4.1.3 Fitness Function

The accuracy of the GA algorithm directly depends on the fitness function [36]. Formulation of elaborate fitness functions in complex optimization problems increases the search space and compromises convergence and computational efficiency. Thus the set of parameters has to be limited [36]. In many cases (such as, for example, the oscillators of this work), this can be achieved by splitting the optimization problem in subtasks and define more than one fitness function. As a result, the number of design variables that needs to be optimized in each step is reduced.

The fitness function has the form of:

$$fitness = \sum_{i=1}^{N} W_i \cdot \left| P_{ar} \right| \qquad (4.1)$$

where P_{ar} are performance metrics and W_i are their weighting factors. Examples of P_{ar} are, in the case of oscillators, the phase noise, the current, and the quality factor Q of the LC-tank and in the case of amplifiers the gain, the current and the noise figure.

The algorithm shown in Figure 4-2 generates a random initial set of design variables. Afterwards, the required analyses are executed through the Ocean™ script and the appropriate fitness function is evaluated. Its value is subsequently fed to the GA, which produces a new set of variables maximizing or minimizing the fitness function. The process is repeated until such goals are achieved.

4.2 Automated Optimization

In chapter 2 we have seen phase noise optimization based on topology selection. In this section we will demonstrate how phase noise theory (Leeson formula, ISF theory) can be utilized in order to optimize a given design in terms of low phase noise and low power consumption.

A classical design approach relies on a number of well-known rules that aim at the minimization of phase noise. At the same time the power consumption must be kept at a low level at the expense of phase noise degradation, revealing a

trade-off between phase noise and power consumption that must be treated in an efficient way. The following analysis stands for both four-oscillator topologies and it will be carried out only for the Colpitts oscillator case while it is straightforward to apply it also to the other cases.

4.2.1 Design Description

The designs employed to demonstrate our methodology are the differential Colpitts, the cross-coupled LC, the serial and parallel-coupled quadrature oscillators illustrated in Figures 2-21, 2-28b.2-30 and 2-31 respectively. All designs have been optimized for operation at 5.4GHz.

- *MOS varactor*. Tuning capabilities have been added by using components that generate variable capacitance controlled by DC voltage. MOS varactors have been selected because of their high $C_{\max}/C_{\min}$ ratio, providing consequently larger tuning range than conventional *pn-junction* varactors [41] (Figure 4-4).

  For operation in accumulation region nMOS varactors outperform pMOS in terms of higher *Q* factor. The electrons have higher mobility than holes leading to lower series resistance, thus higher *Q*. In the same time for maximal varactor *Q*, a minimal length of 0.18um preferred to minimize the resistive paths in the channel [42,15]. A multifingered folded layout is used for minimal gate resistance or maximal varactor *Q* (section 4.2.1).

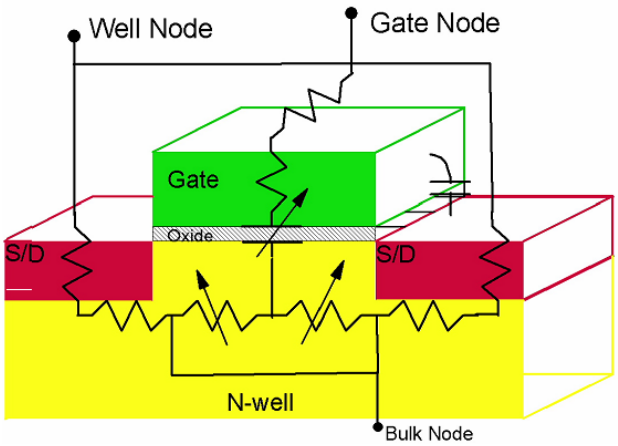


Figure 4-3 MOS varactor model.

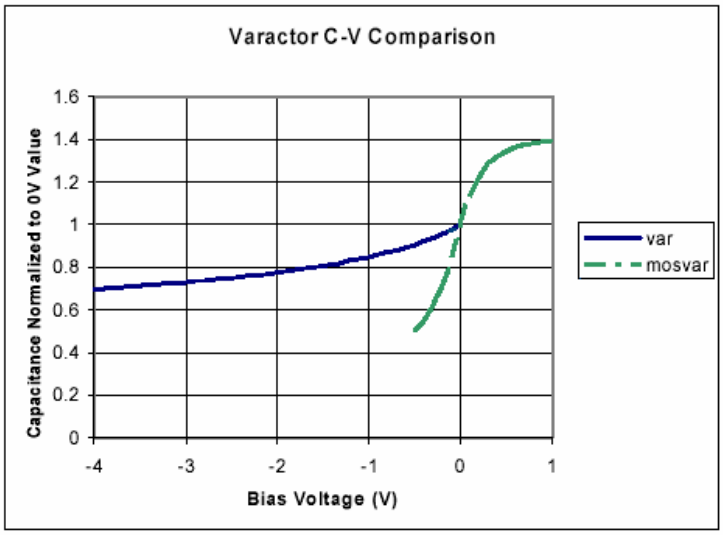


Figure 4-4 C-V plots for a pn-junction varactor and a MOS varactor.

All of the varactor diodes have a significant parasitic junction between the n+ region and the substrate. If the varactor is operated such that the n+ region and the substrate are at AC ground, there is no current across this junction. If the AC signal is on the n+ junction and the substrate is at AC ground, this capacitance appears in parallel with the varactor. The tuning properties and the quality factor are affected. For the MOS varactor, the n+ region is the body, so gate excitation is preferred [43] (Figure 4-3).

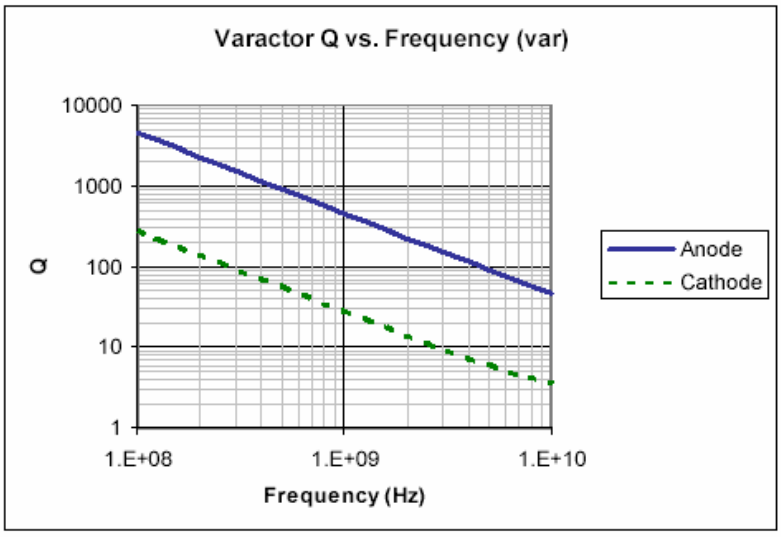


Figure 4-5 Cathode vs. Anode excitation.

- *Spiral inductor*. The BiCMOS 7WL technology offers a scalable, high *Q* octagonal spiral inductor with low parasitic capacitance. The inductor has two ground plane options. The TI ground plane option provides the lower parasitic capacitance. The M1 ground plane option uses an array of M1 wires as a shield to isolate the inductor from substrate noise and prevents capacitively coupled currents in the substrate, which lead to lower *Q*.

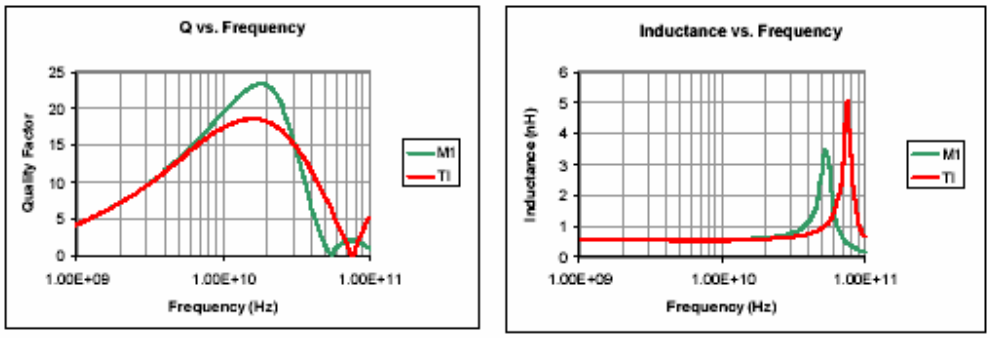


Figure 4-6 Influence of ground plane on inductor properties.

The Figure 4-6 above shows the simulated inductance and quality factor for a typical inductor for the two ground plane options. As shown on the left, the peak *Q* of the inductor is higher with the M1 ground plane (Faraday shield) because the shield prevents capacitively coupled energy loss in the substrate. The plot on the right shows that this increased *Q* comes at the cost of reduced self-resonant frequency. The M1 shield is closer to the inductor coils than the substrate. This increases the parasitic capacitance and lowers the self-resonant frequency.

In our designs a M1 ground plane has been chosen for its high *Q* factor at the expense of lower self-resonance frequency, thus higher capacitive parasitics.

- *Bias circuitry*. All designs have been tail biased by a simple nMOS current mirror. Although top biasing by pMOS transistors upconverts less flicker noise as discussed in section 2.3.2, we emphasize that our aim is to optimize a given topology at the circuit level and not at the topology level.

The final designs used as vehicle to demonstrate our optimization methodology that follows are illustrated in Figures 4-6 – 4-8.

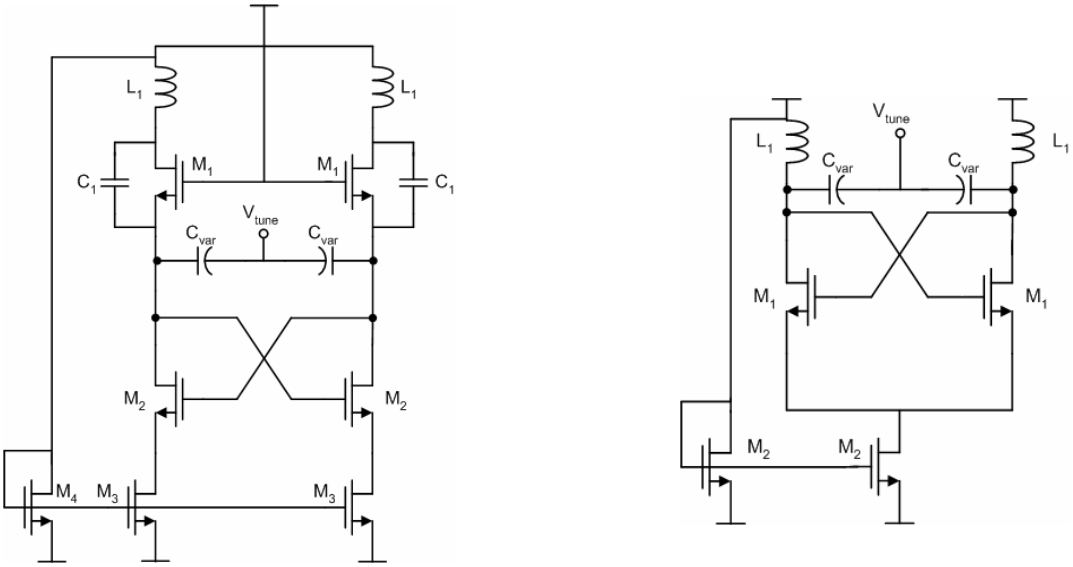


Figure 4-6 Differential Colpitts and Cross-Coupled LC VCOs.

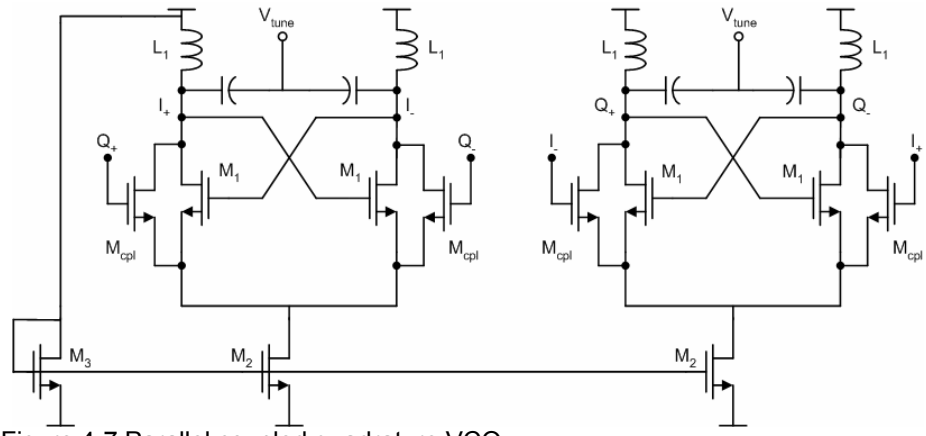


Figure 4-7 Parallel coupled quadrature VCO.

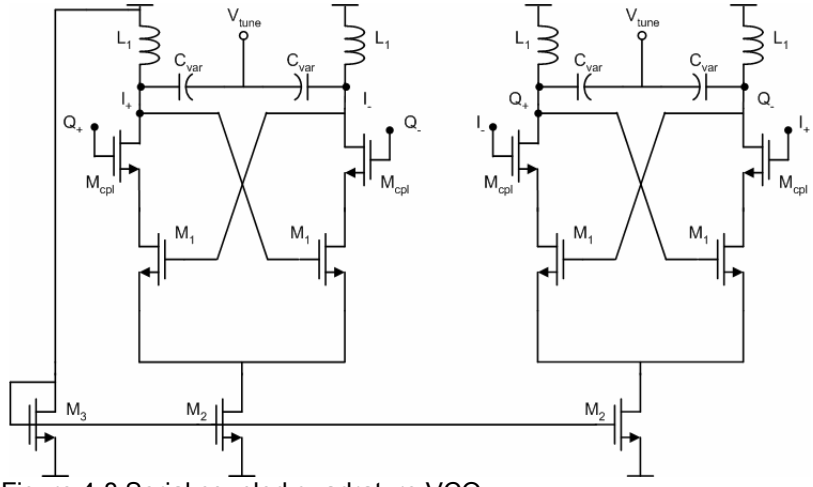


Figure 4-8 Serial coupled quadrature VCO.

4.2.2 Manual Design Approach

The differential Colpitts oscillator of Figure 4-6 [11] consists of a parallel LC-tank with a capacitive voltage divider that produces a positive feedback that effectively increases the negative resistance of the nMOS transistors M_2, which in conjunction with M_1 comprise the active, gain cell.

A. Tank Quality Factor

According to Leeson's formula [44],

$$L(\Delta f) = 10\log\left(\frac{2KTF(\Delta f)}{P_{sig}}\left(\frac{1}{2Q}\frac{f_o}{\Delta f}\right)^2\right) \quad (4.2)$$

where $L(\Delta f)$ is the phase noise, *Q* is the quality factor of the tank, *F* is the noise factor of the oscillator, P_{sig} is the power of the output signal, f_o is the oscillation frequency and Δf the offset frequency.

The quality factor of the tank in Fig. 2 is given by:

$$Q = \frac{1}{real(Y_{11}) \cdot \sqrt{LC_{pl}} \cdot L} \quad (4.3)$$

where *L*, $real(Y_{11})$ are the inductance of the spiral inductor and the parallel conductance of the tank respectively. C_{pl} is the parallel capacitance combination of the fixed capacitor and the MOS varactor.

Decoding (4.3), we observe that the *Q* factor has not only dependence on the values of *L* and C_{pl} but also on their geometry and sizing since those affect the parallel conductance of the tank. Although many different on-chip spiral inductors and varactors can be generated in any technology with the same *L* and C_{pl}, using different geometrical and sizing parameters, only one will offer the minimum parallel conductance [45].

The capacitive transformer's ratio in the Colpitts oscillator of Fig 2 (a) given by:

$$N = \frac{C_1}{C_1 + C_{\text{var}}} \quad (4.4)$$

is also critical in the design procedure as it affects the noise performance. As proposed in [11] the value of this ratio must be chosen around 0.2.

Further reduction of phase noise is achieved by both proper layout and fine bias current selection.

B. Parasitic Gate Resistance

In the first case, the parasitic gate resistance significantly affects phase noise performance at high frequencies as it induces thermal noise at the gate node of the MOS transistor, which is then amplified to the drain node.

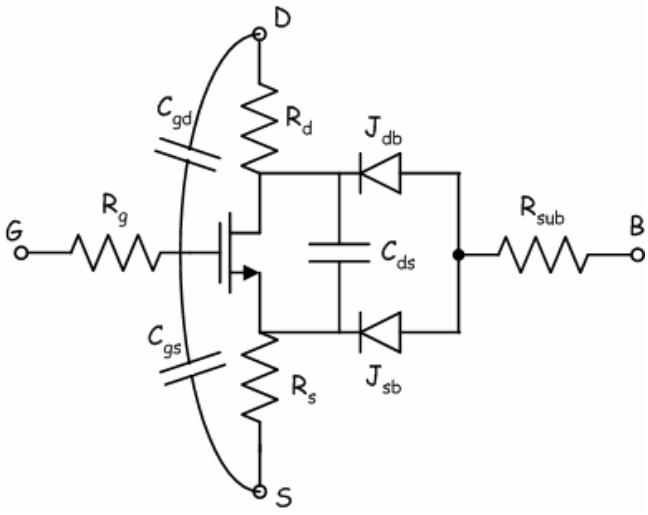


Figure 4-9 Simple high frequency MOS model.

A simple expression of gate resistance, R_g, based on that in DC or low frequency has been used to calculate the value of gate resistance accounting for the distributed nature of the gate at high frequencies. However, a factor of *a* is introduced, which is 1/3 or 1/12 depending whether the gate terminal is brought out from one side or connected on both sides [46] to account for the distributed RC effects at RF. The distributed electrode resistance R_g from the polysilicon gate, is given in the following [47]:

$$R_g = \frac{R_{gsh}}{N_f L}\left(W_{ext} + aW_f\right) \quad (4.5)$$

In equation (4.5), R_{gsh}, is the gate sheet resistance, W_f is the channel width per finger, *L* is the channel length, N_f is the number of fingers and W_{ext} is the

extension of the polysilicon gate over the active region. In reality the gate resistance is the sum of two terms, the one given in (4.5) that is insensitive in bias and frequency and a second term that accounts for NQS effects and is of no interest in our case [47].

From (4.5) it is apparent that the parasitic gate resistances can be eliminated by folding the active devices M_1, M_2 and by using double-sided gate contacts (Figure 6-1b), thus canceling out this noise contributor [48], [49]. It is well known that, if the gate is connected by metal lines on both source and drain sides, the gate resistance is four times smaller than what is obtained for a gate connected only on one side [50].

Finally the low value of resistors R_d, R_s and the fact that their noise does not get amplified allow us to neglect them as significant noise contributors.

C. Voltage Amplitude

Moreover, (4.2) indicates that maximizing the output signal's power reduces phase noise. As the output power depends on the bias current, selecting the latter in a fashion that simultaneously results in low phase noise and power budget is not straightforward.

There are two regimes that describe the operation of an oscillator [45], the current limited regime where the oscillation's amplitude is given by:

$$A = 4I_{bias} \cdot R_p \qquad (4.5)$$

where R_p is the parallel resistance of the tank, and the voltage limited regime where the oscillation amplitude is saturated to the voltage supply level.

As can be inferred by [14], where phase noise dependence is given by,

$$L\{f_{off}\} \propto \frac{L^2 I_{bias}}{V_{\tan k}^2} \qquad (4.6)$$

increasing bias current improves noise only when $V_{\tan k}$ increases. This occurs when the oscillator is operating in the current-limited regime. When the oscillator enters the voltage-limited regime, $V_{\tan k}$ saturates and higher values of bias current

result in a degraded noise performance and waste of power. Therefore best phase noise can be achieved at the boundary between these regimes.

4.2.2.1 Design Variables

The design variables involved in the optimization procedure, are categorized in a group of dependent and a group of independent variables.

A. Dependent Variables

Inductance *L* of the on-chip spiral inductor, the maximum and minimum capacitance $C_{\max}, C_{\min}$ of the MOS varactor, the overall width of the MOS transistors M_1, M_2, M_3 and the bias current I_{bias}. We must point out that the tuning range is not included in the optimization because the range $C_{\min}$-$C_{\max}$ is determined by the underlying physics of the MOS varactor, which cannot be controlled in a design process.

B. Independent Variables

The geometrical parameters of the inductor (outer dimension, spiral width, number of turns), the fixed capacitance C_1, the sizing parameters (finger width, number of fingers, multiplicity) of the MOS varactor and the sizing parameters (finger width, number of fingers) that determine the overall width of MOS transistors. Channel length does not comprise an optimization variable and is set to the minimum feature size given by the process technology, that is 0.18um.

C. Design Variables Overview

We consider the finger widths of transistors M_1, M_2 to be equal. In the case of M_3 and M_4 there is no particular reason to optimize the finger width as their parasitic gate resistance does not comprise a noise contributor and only their overall width is of interest, as it determines the bias current. Therefore we set M_3 and M_4 finger width to 5um and optimize the second sizing parameter e.g. the number of fingers. Additionally, the number of turns of the inductors is fixed to 1.5 turns, yielding a total of eleven independent variables. Table I gives an overview of the dependent design variables and their relationship to the independent variables for all topologies.

TABLE I
DESIGN VARIABLES

Topology	Dependent Variables	Independent Variables	Constants
Colpitts	L C_{max} MOST Widths, M_1-M_4 I_{bias}	Outer Dimension Spiral Width Finger Width Number of Gates Multiplicity Fixed Capacitance C_1 Finger Width W_f Number of Fingers MOST Sizes	1.5 Number of Turns $Wf_{3,4}$=5um V_{cc}=2V
Cross – Coupled	L C_{max} MOST Widths, M_1-M_3 I_{bias}	Outer Dimension Spiral Width Finger Width Number of Gates Multiplicity Fixed Capacitance C_1 Finger Width W_f Number of Fingers MOST Sizes	1.5 Number of Turns Wf_3=5um V_{cc}=1V
PQVCO	L C_{max} MOST Widths, M_1-M_3, M_{cpl} I_{bias}	Outer Dimension Spiral Width Finger Width Number of Gates Multiplicity Fixed Capacitance C_1 Finger Width W_f Number of Fingers MOST Sizes	1.5 Number of Turns $Wf_{2,3}$=5um V_{cc}=1V
SQVCO	L C_{max} MOST Widths, M_1-M_3, M_{cpl} I_{bias}	Outer Dimension Spiral Width Finger Width Number of Gates Multiplicity Fixed Capacitance C_1 Finger Width W_f Number of Fingers MOST Sizes	1.5 Number of Turns $Wf_{2,3}$=5um V_{cc}=1V
VGA	Gain MOST sizes I_{bias}	MOST Sizes $V_{control}$, V_{ref}, V_{M1} Number of Fingers NF_1-NF_3	V_{cc}=1.8V Wf_1-Wf_3=2um

4.2.3 Automated Design Approach

From the foregoing analysis it is apparent that simultaneously tuning a multitude of variables in order to satisfy the mentioned constraints may lead to uncertainty in obtaining an optimum solution that exploits the full capabilities of a Colpitts oscillator.

The Colpitts-Oscillator design approach of this work to ensure robustness of the obtained solution concentrates in implementing the following set of rules:

a) Design of a high Q LC-tank for large swing, leading to better phase noise performance.

b) Choose transformer ratio for best phase noise performance, $N_{ratio} = 0.2$ *.*

c) Maximize bias current, I_{bias} *, without going far into saturation.*

d) Split transistors into multiple fingers in order to minimize thermal noise, due to parasitic gate resistance.

The previous rules set can be encoded into an automated procedure that reduces the complexity of the problem and results in a near global optimum design solution, meeting the specifications defined in Table II. This is achieved by splitting the problem into a two-step process.

TABLE II
VCO and VGA SPECIFICATIONS

	VCO (Colpitts, Cross-Coupled, PQVCO, SQVCO)	VGA
Phase Noise @ 100KHz	minimal	
Oscillation Frequency	5.4 GHz	
Power Supply	2V, 1V, 1V, 1V	1.8V
I_{bias}	minimal	minimal
Noise Figure (dB10)		minimal
S21 (dB20)		10

4.2.3.1 LC Tank Optimization – Step 1

Figure 4-10 shows how the LC-tank is optimized. The geometrical parameters of the on-chip inductor, the fixed capacitance and the sizing parameters of the MOS varactor must be determined in a way that rules (a) and (b) are satisfied.

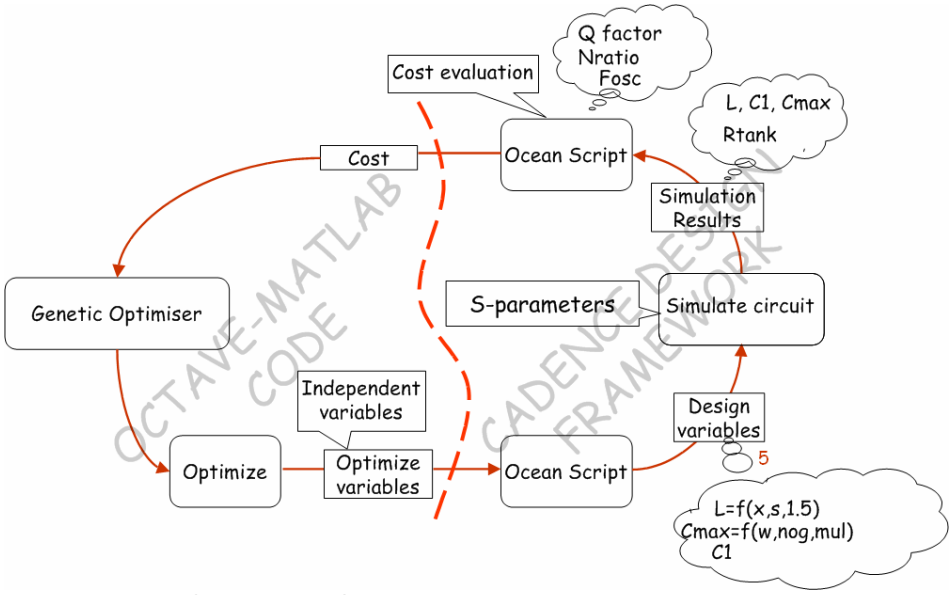


Figure 4-10 First Optimization Step.

The optimization starts by calling the SPECTRE™ simulator to perform the appropriate analyses with a vector of independent variables that has been randomly generated by the genetic algorithm. This is done through an Ocean™ script that is set to do the following analyses: S-parameters analysis to calculate the inductance of the coil using the form $L = imag(Z_{11})/2\pi f_o$, the maximum capacitance of the MOS varactor from $C_{\max} = 2\pi f_o / imag(Z_{11})$ and the parallel conductance $real(Y_{11})$ of the LC-tank, at $f_o = 5.4GHz$. Once calculated, these quantities are then used to estimate the *Q* from (3), the oscillation frequency from $f_{osc} = 1/2\pi\sqrt{LC_{pl}}$, and the capacitive divider ratio that is given by (4). Subsequently, the fitness function is calculated and its value is passed to the genetic algorithm, which in turn produces a new, optimized vector of variables that is fed to the simulator. This iterative procedure continues until the fitness function converges to a constant value.

4.2.3.2 Phase noise-Current Optimization – Step 2

In this step, shown in Figure 4-11, we optimize the active gain cell with the resulting LC-tank from *step 1* attached to it.

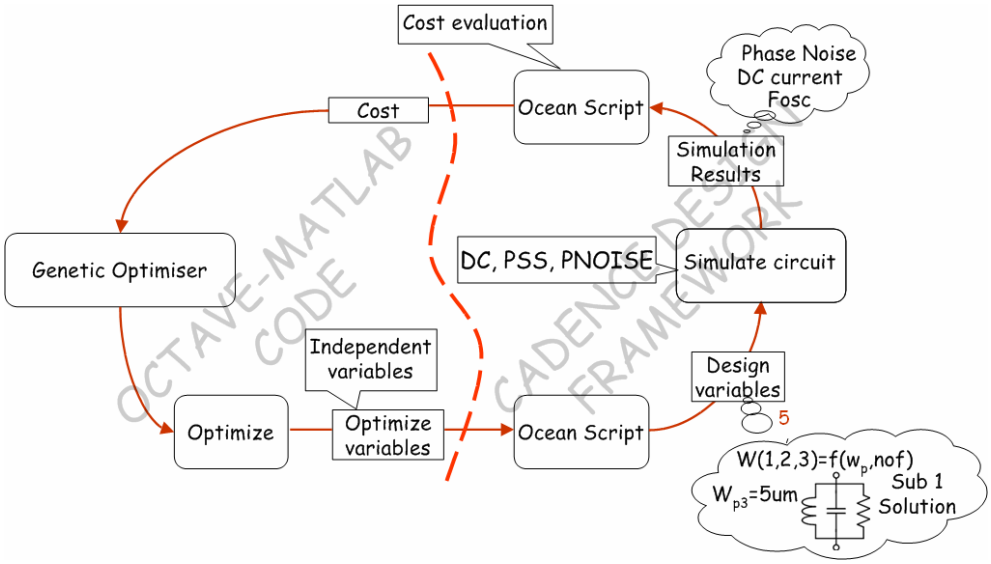


Figure 4-11 Second Optimization Step.

The optimization's loop principle of operation is similar to that of the first phase. After connecting the optimal LC-tank derived from the first step, the script instructs the simulator to perform dc operating-point (DC), periodic steady state (PSS) and periodic noise (PNOISE) analysis, in order to determine the power consumption, the oscillation frequency and the phase noise of the circuit respectively. Then the script calculates the fitness function and the iterative process continues until some stop criteria are met.

4.2.3.3 Fitness Function

The fitness function that is maximized is formulated so that it monitors performance metrics such as phase noise and current as well as their tradeoffs as experienced in an actual design procedure. It is given for step 1 by the relation,

$$F_{step1} = a_1 \cdot Q - a_2 \left| F_{osc} - F_{spec} \right| - a_3 \cdot \left| N_{ratio} - 0.2 \right| \quad (4.7)$$

where a_1, a_2, a_3 are normalizing weighting coefficients, *Q* is the quality factor of the parallel LC-tank, F_{osc} the oscillation frequency, F_{spec} is the targeted oscillation frequency (e.g. 5.4GHz) and N_{ratio} is the ratio of equation (4).

The quantity F_{step1} increases as the difference between targeted and actual specifications ($F_{step1} = 5.4GHz$, N_{ratio}=0.2) decreases and *Q* increases. The second and third terms are subtracted from the first in a sense of penalizing a *Q* that does not correspond to an oscillation frequency near to the specified one and to the optimum ratio of the capacitive voltage divider. In a sense, F_{step1} is formulated in a way that factors in human experience – prior knowledge.

Similarly, the fitness function for step 2 must include the elements that must be also maximized: phase noise, oscillation frequency and current consumption. It is given by

$$F_{step\,2} = b_1 \cdot PN - b_2 \left| F_{osc} - F_{spec} \right| - b_3 I_{bias} \quad (4.8)$$

where b_1, b_2, b_3 are normalizing weighting coefficients, *PN* is the phase noise at 100KHz offset from the $F_{step1} = 5.4GHz$ carrier, and I_{bias} the bias current.

The above function illustrates the tradeoff between phase noise and bias current. Subtracting the third term from the first ensures that if two solutions exist with the same phase noise but different bias currents the optimization will be directed to a solution that produces low phase noise (high in absolute value) and low bias current, satisfying rule (c).

4.2.4 Other VCO Topologies

Figures 4-6b, 4-7, 4-8 show an nMOS transistor based VCO, a parallel and a serial coupled quadrature VCO [14] respectively. The previous methodology was applied in a similar fashion for the latter designs except that the capacitive divider and its relevant term in equation (7) was not employed.

The design variables associated with all four topologies are shown in Table I.

4.2.5 Variable Gain Amplifier

The current steering variable gain amplifier presented in Figure 3-8a [25] is optimized for noise figure for a specified maximum gain and bias current. Transistor M_3 is used to steer current from the cascode pair or from the load.

The optimization goals are also shown in Table II. During optimization the sizing parameters of the MOS transistors must be determined along with the associated voltages. The design variables are the number of fingers of M_1, M_2, M_3 and the voltages $V_{control}$, V_{ref}, V_{M1}. The finger width is the same for all MOS transistors and was fixed to a value of 2μm [49]. The LC-tank is chosen in order to tune the amplifier to a center frequency of 2GHz and it does not contribute to noise.

The small number of design variables does not necessitate in this case the use of multiple optimization steps, so a knowledge-free approach was adopted. One fitness function is therefore needed and is defined as:

$$F_{VGA}=a_1 \cdot NF - a_2 \left| G - G_{spec} \right| - a_3 \cdot \left| I_{bias} - I_{b,spec} \right| \qquad (4.9)$$

where a_1, a_2, a_3 are normalizing weighting coefficients, *G is* the gain at a certain iteration, G_{spec} is the specified maximum gain, I_{bias} is the bias current and $I_{b,\,spec}$ is the specified bias current.

The design variables associated with the optimization process and the optimization goals of the variable gain amplifier design are shown in Table I and II respectively.

Chapter 5 : Optimization Results

5.1 VCO Optimization Results

A. Colpitts VCO

Figures 5-1 – 5-4 show the convergence of design parameters and performance metrics for the Colpitts VCO.

In figure 5-1 the maximization of the LC tank's quality factor is shown while the ratio of the capacitive divider has converged to the optimal targeted value that is 0.22.

The finger width for the MOS transistors of the active gain cell shown in Figure 5-3 settled to a value of 2.24um, while the finger width of the MOS varactor settled to 2.18um. These results are consistent to the common practice in RF design of selecting a low finger width in order to significantly reduce the parasitic gate resistance of MOS transistors. As referred in [47] an optimal value is below 3um.

The frequency variation around 5.4GHz shown in Figure 5-3 is caused by the varying parasitic capacitances (Figure 4-3), produced by the MOS transistor sizing that is connected to the tank. It turns out that this will not affect the validity of the optimal solution since the fitness function associated with the second step will drive the optimization sequence toward the specified oscillation frequency.

Moreover, by observing Figure 5-3 we see that there are several phase noise-I_{bias} transient states where a low phase noise value is produced by either a high or low bias current. Fortunately, the fitness function defined in *step 2* forces the GA to reject a low phase noise - high I_{bias} state and converge to a minimal one.

In Figure 5-4 the maximization of the fitness function associated with the first and second steps of the optimization process are shown.

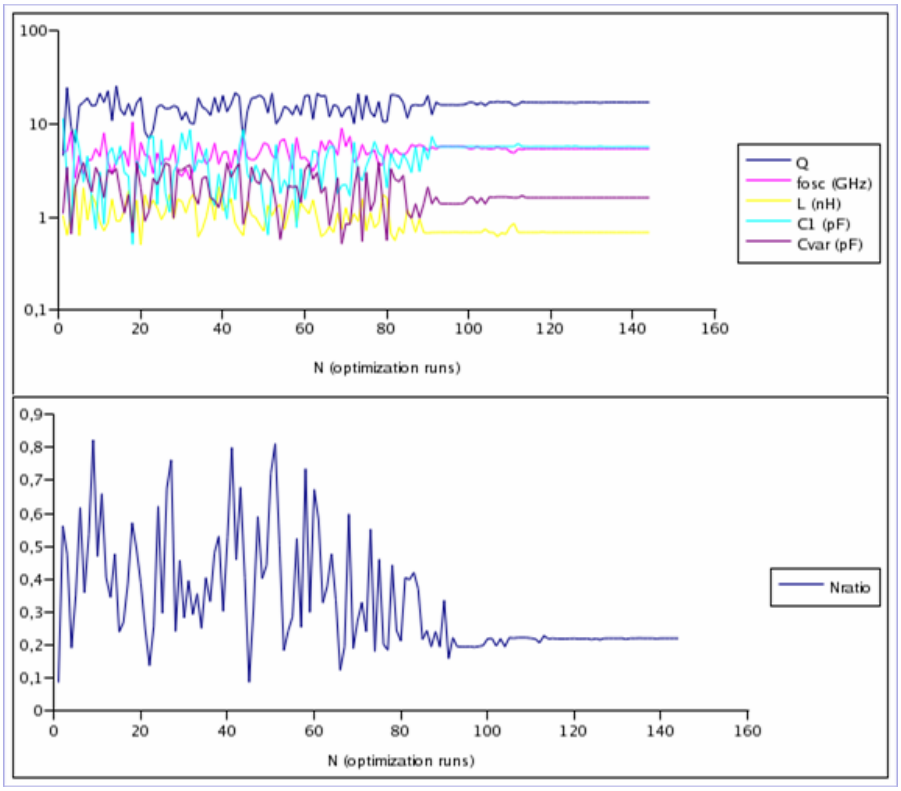


Figure 5-1 LC tank quality factor and passive elements optimal evolution

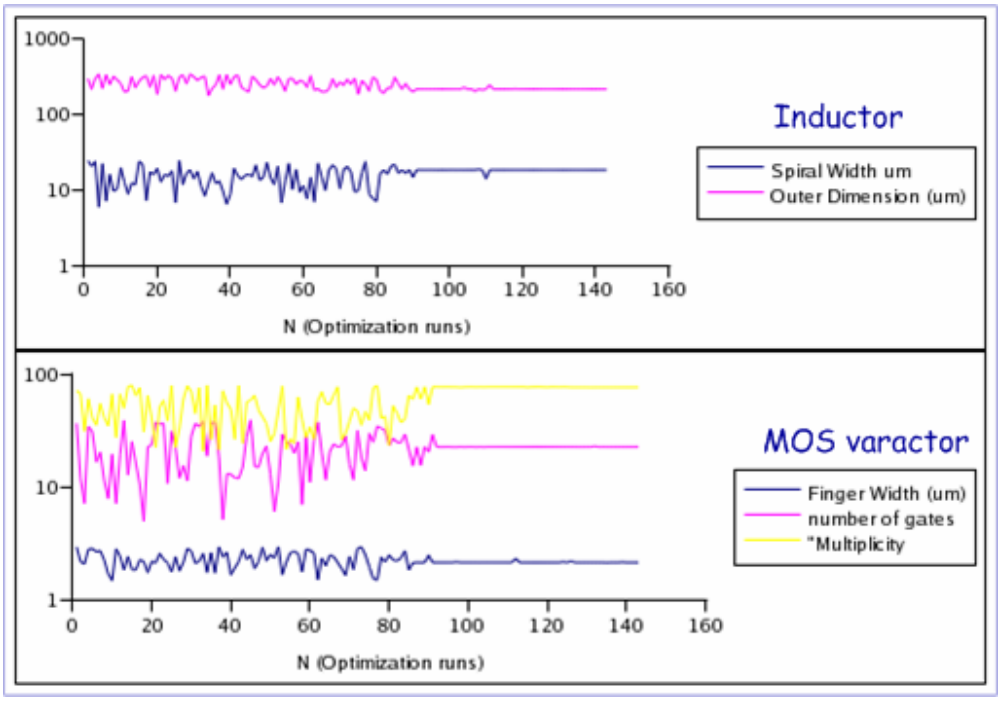


Figure 5-2 Optimal evolution of geometrical and sizing parameters of spiral inductor and MOS varactor.

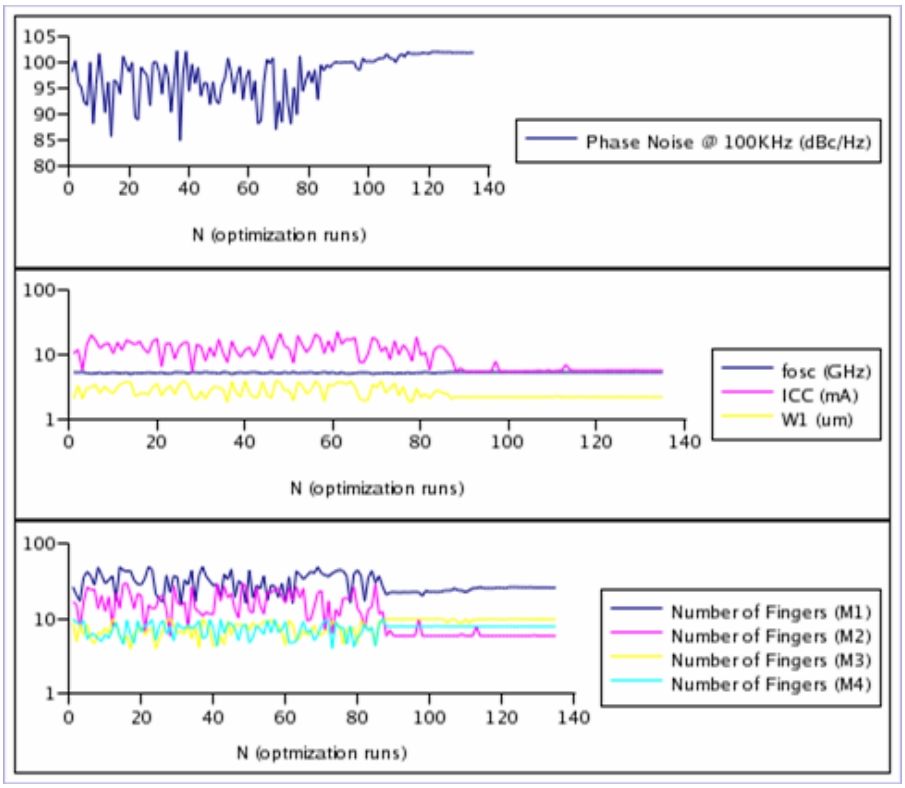


Figure 5-3 Phase noise, bias current and MOS sizing optimal evolution.

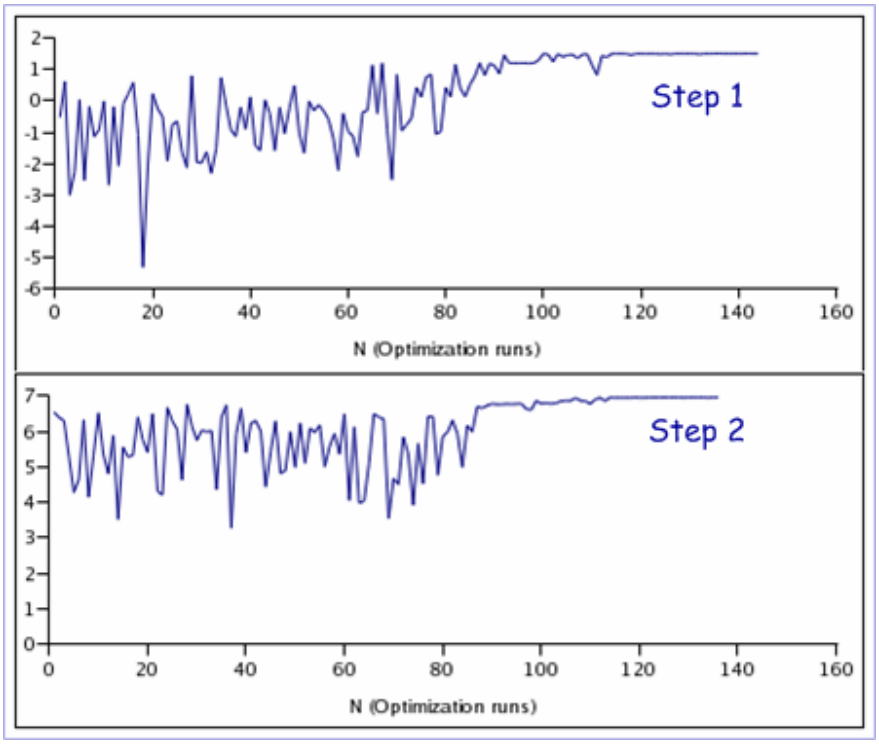


Figure 5-4 Maximization of the fitness function for step 1 and 2.

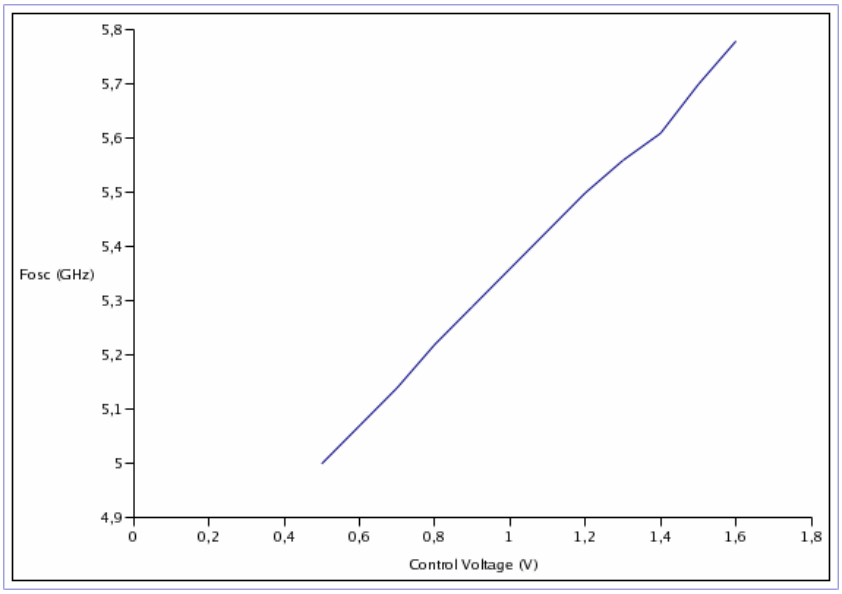


Figure 5-5 Tuning Range.

B. Cross-Coupled LC VCO

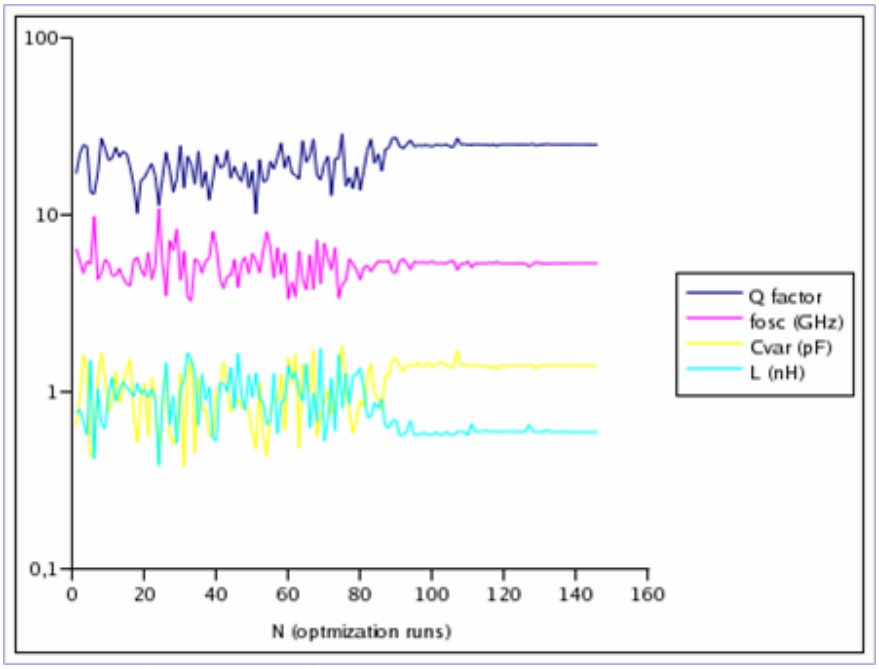


Figure 5-6 LC tank quality factor and passive elements optimal evolution.

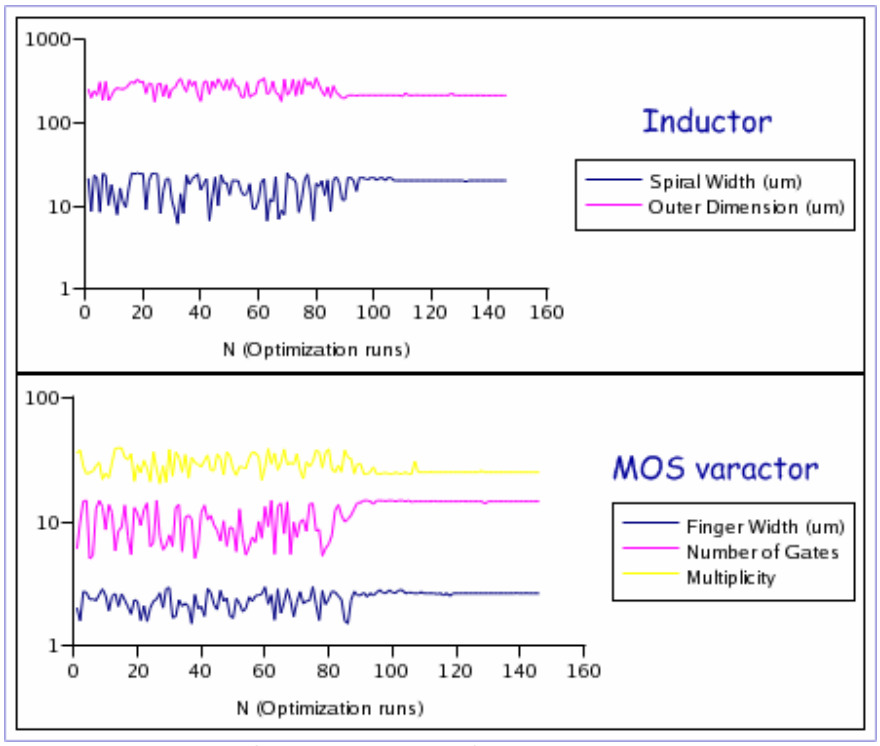


Figure 5-7 Optimal evolution of geometrical and sizing parameters of spiral inductor and MOS varactor.

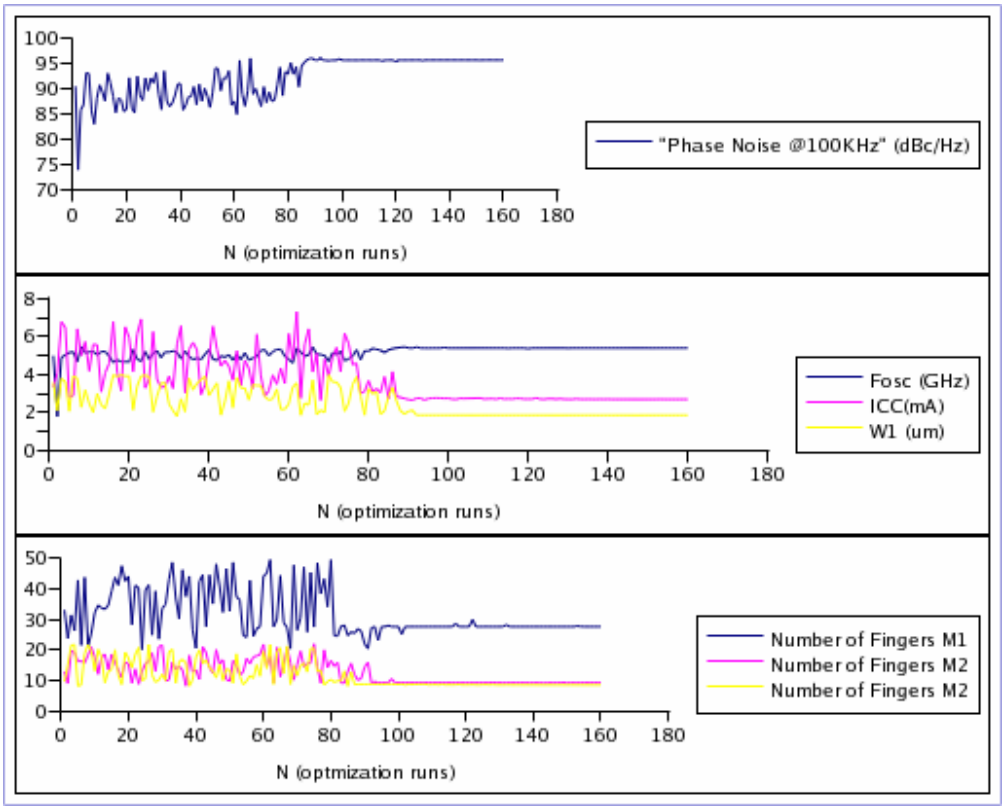


Figure 5-8 Phase noise, bias current and MOS sizing optimal evolution.

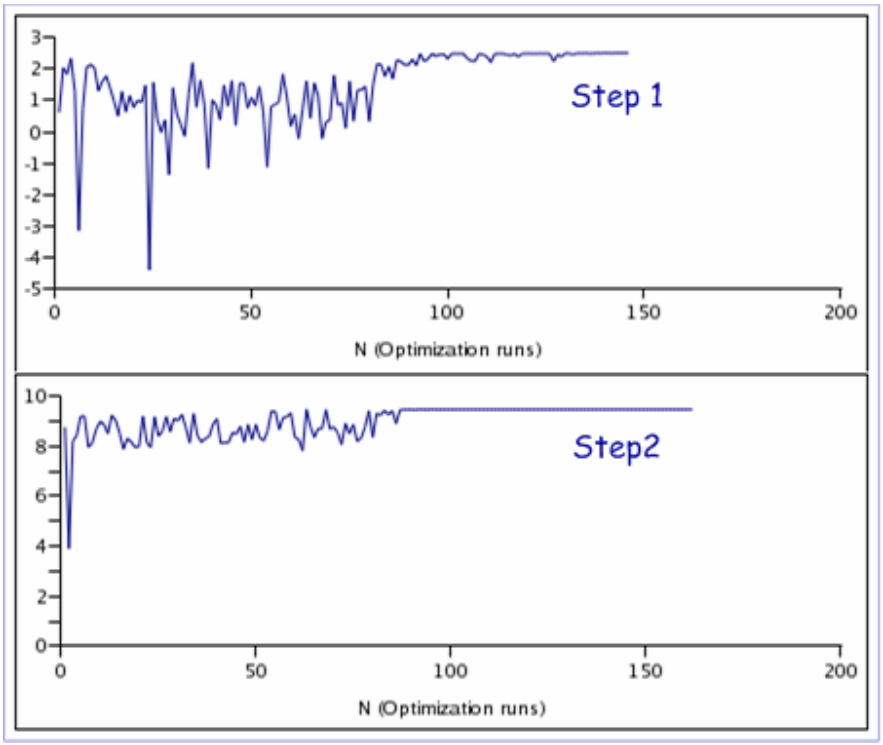


Figure 5-9 Maximization of the fitness function for step 1 and 2.

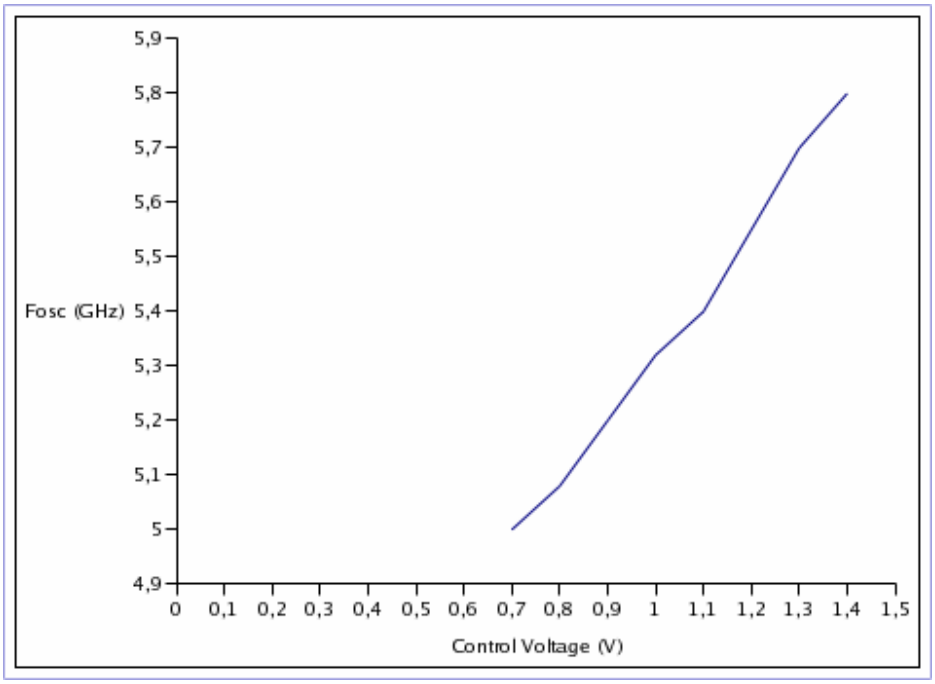


Figure 5-10 Tuning Range.

C. Serial Coupled Quadrature VCO

Validating our results we must mention that the resulting coupling ratio $a = M_{cpl} / M_1$ has a value of 5.3 that is in agreement with the optimal coupling ratio of 5 proposed in [14].

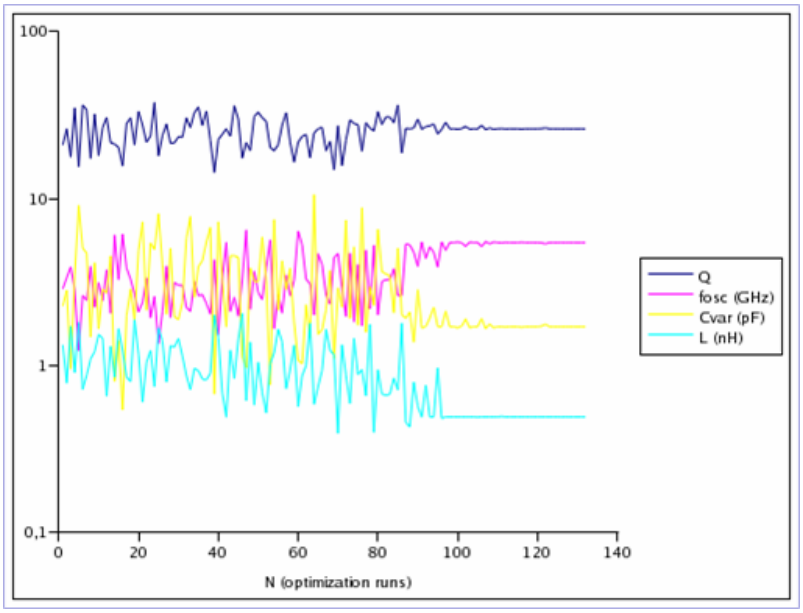


Figure 5-11 LC tank quality factor and passive elements optimal evolution.

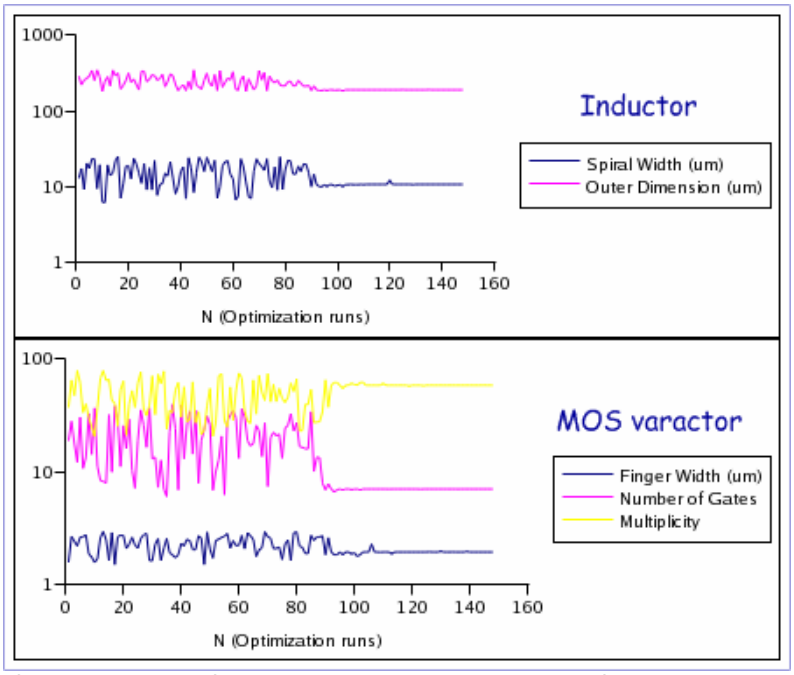


Figure 5-12 Optimal evolution of geometrical and sizing parameters of spiral inductor and MOS varactor.

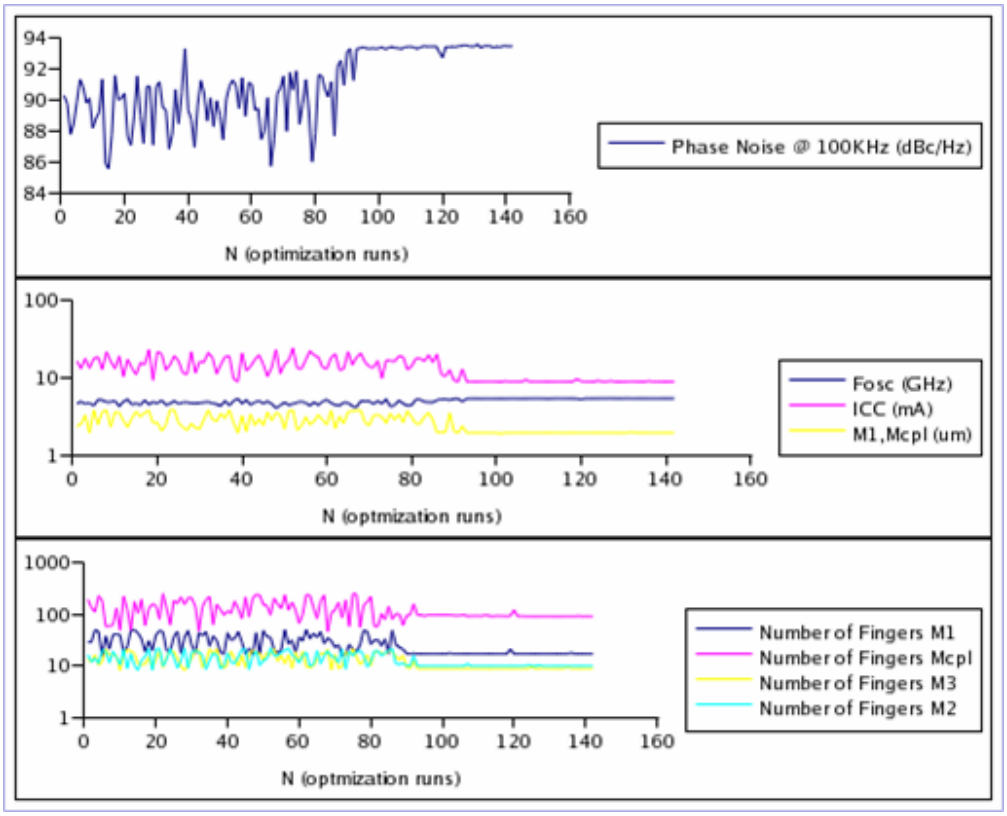


Figure 5-13 Phase noise, bias current and MOS sizing optimal evolution.

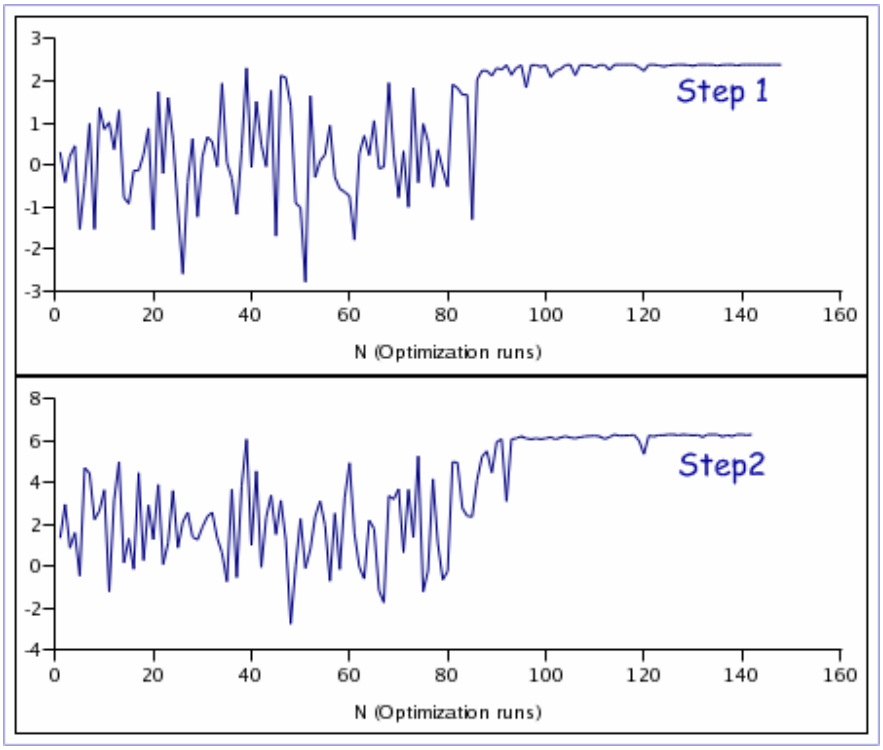


Figure 5-14 Maximization of the fitness function for step 1 and 2.

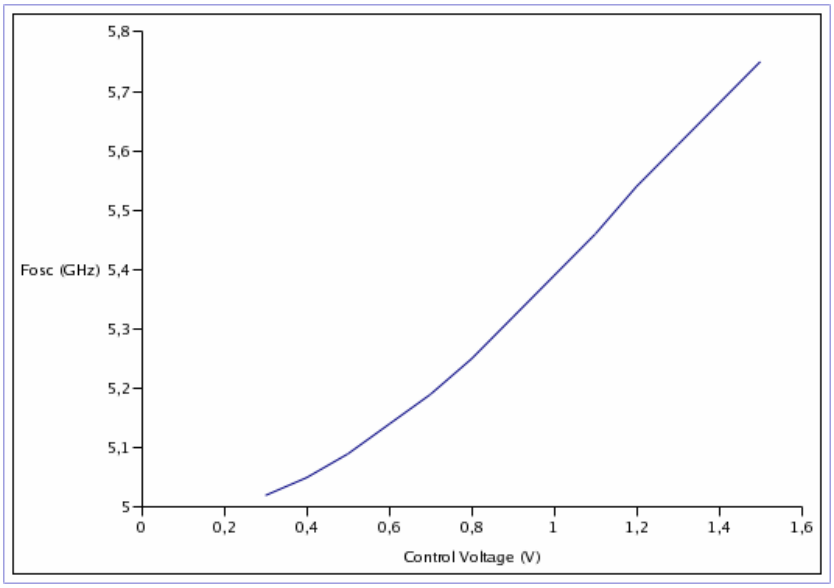


Figure 5-15 Tuning Range.

D. Parallel Coupled Quadrature VCO

The resulting coupling ratio $a = M_{cpl} / M_1$ has a value of 0.21 that is in agreement with the optimal coupling ratio of 0.2 proposed in [15].

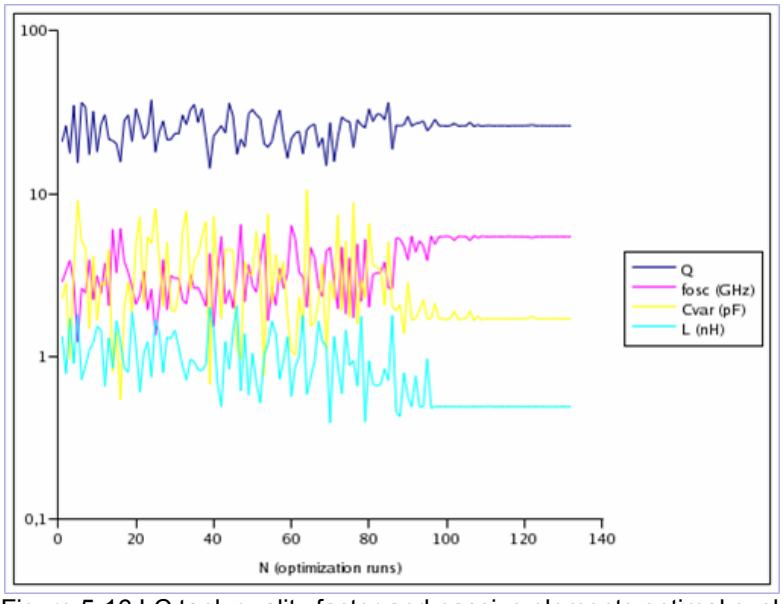


Figure 5-16 LC tank quality factor and passive elements optimal evolution.

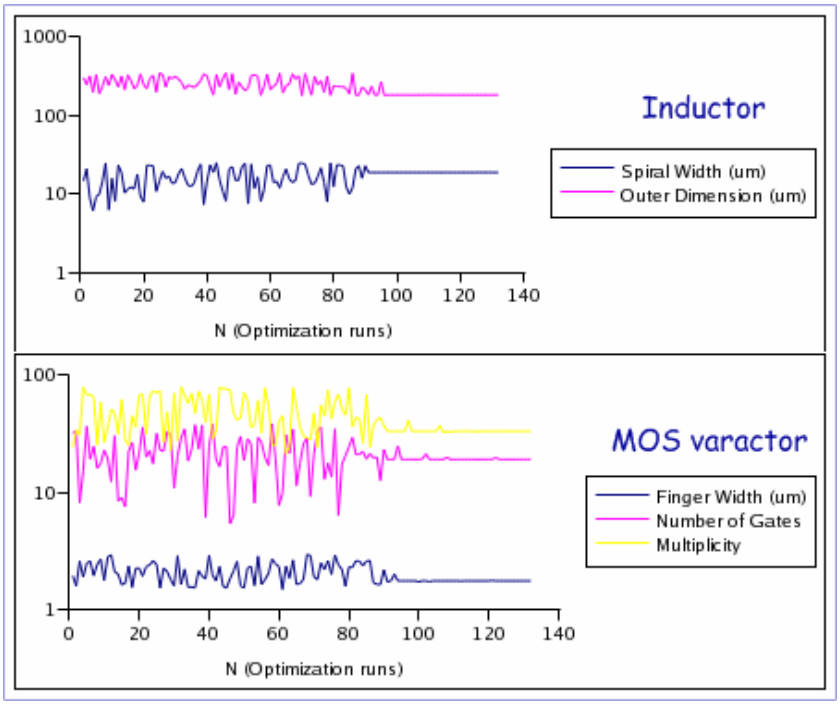


Figure 5-17 Optimal evolution of geometrical and sizing parameters of spiral inductor and MOS varactor.

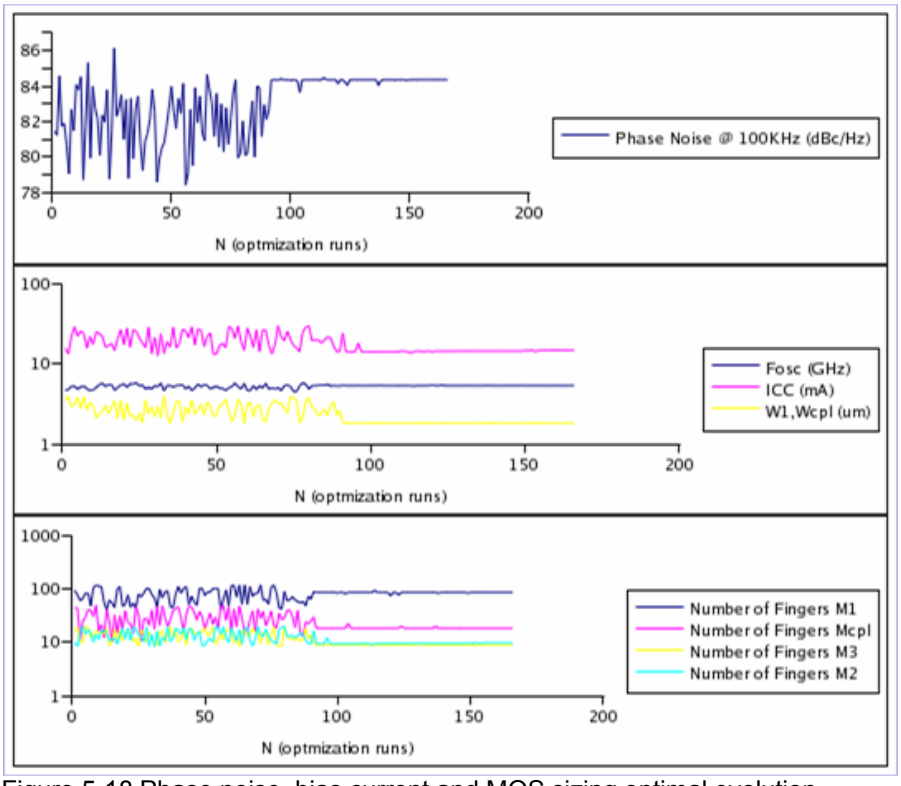


Figure 5-18 Phase noise, bias current and MOS sizing optimal evolution.

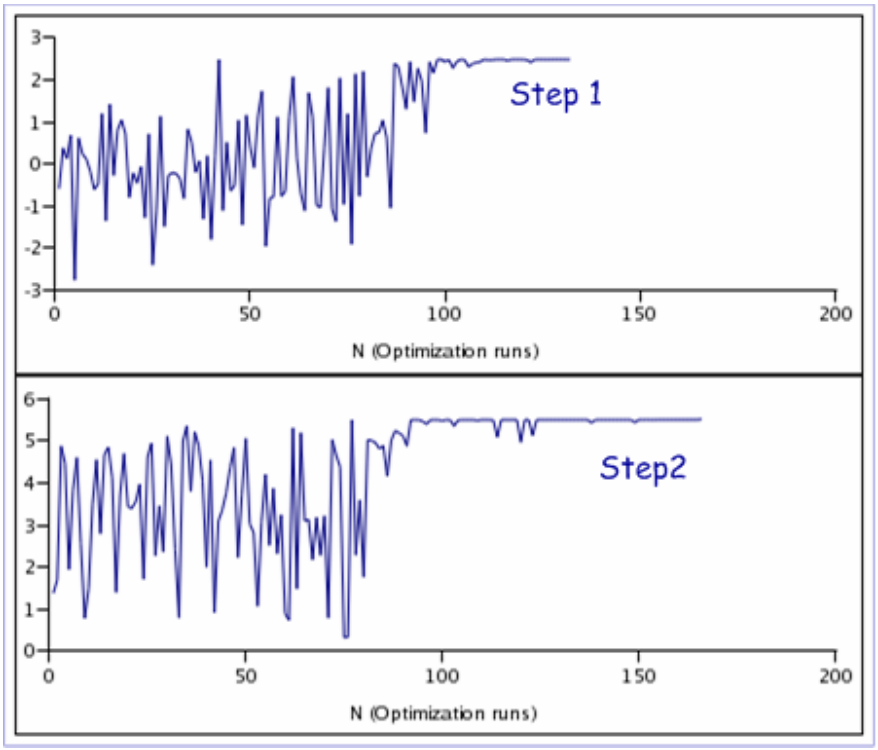


Figure 5-19 Maximization of the fitness function for step 1 and step 2.

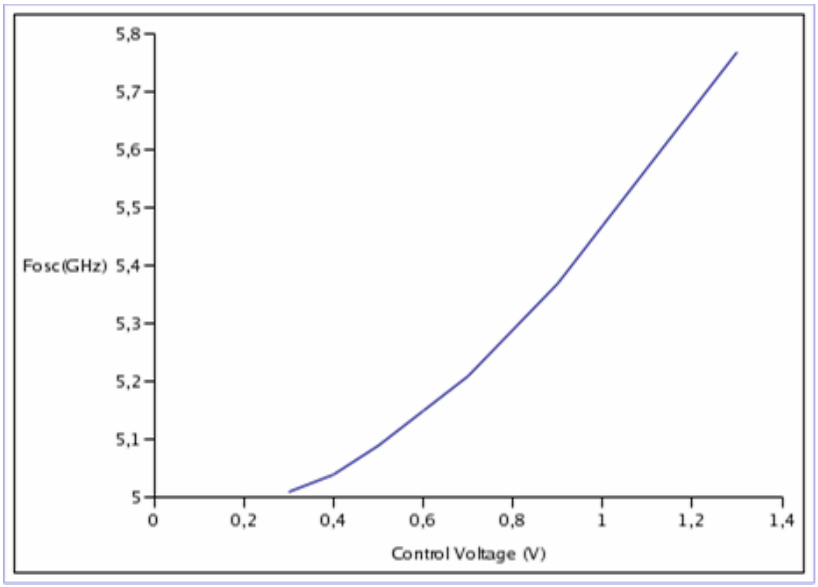


Figure 5-20 Tuning Range.

5.2 Variable Gain Amplifier Optimization Results

Figure 5-17 shows the noise figure, gain and bias current after 145 evolutions of the optimizing algorithm. The resulted noise figure is 1.14dB and the minimum noise figure as can be seen in Figure 5-18 is 0.25 dB for a maximum S21 of 10dB and a bias current of 2.57 mA. The simulated bandwidth was 696MHz for a center frequency of 2 GHz (Figure 5-19).

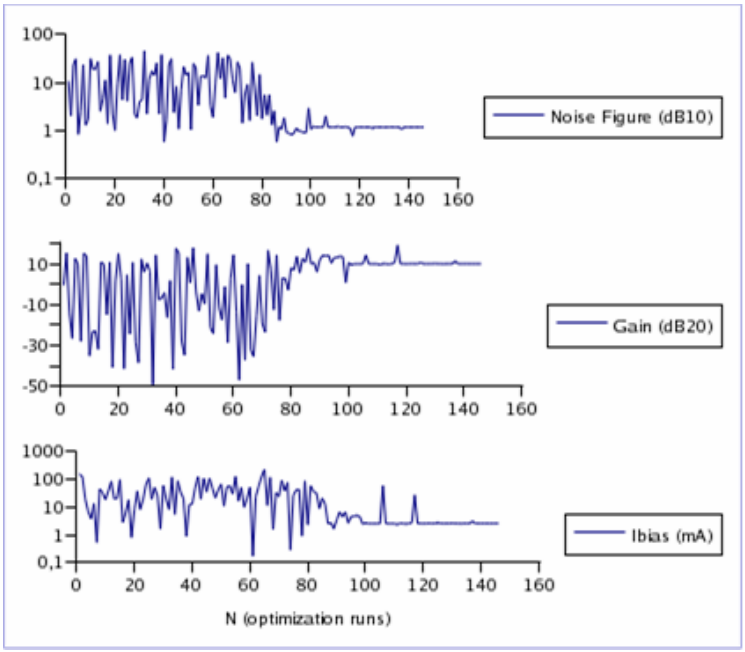


Figure 5-21 Noise figure, gain and bias current evolution.

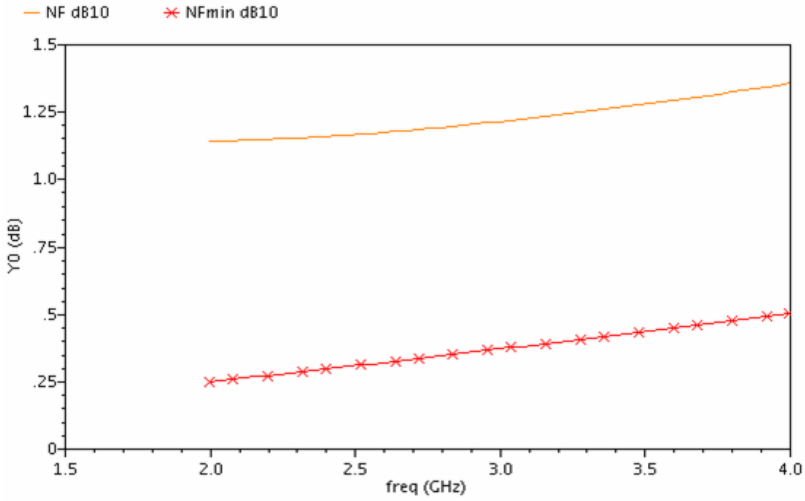


Figure 5-22 Noise figure, gain and bias current evolution.

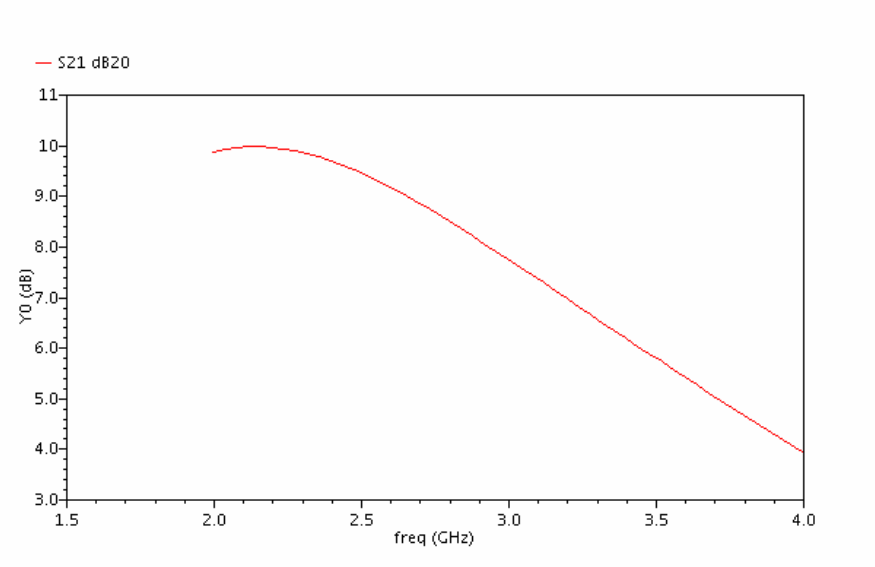


Figure 5-23 S21 Bandwidth.

In Figures 5-20 and 5-21 the sizes of the MOS transistors and the associated bias voltages are illustrated.

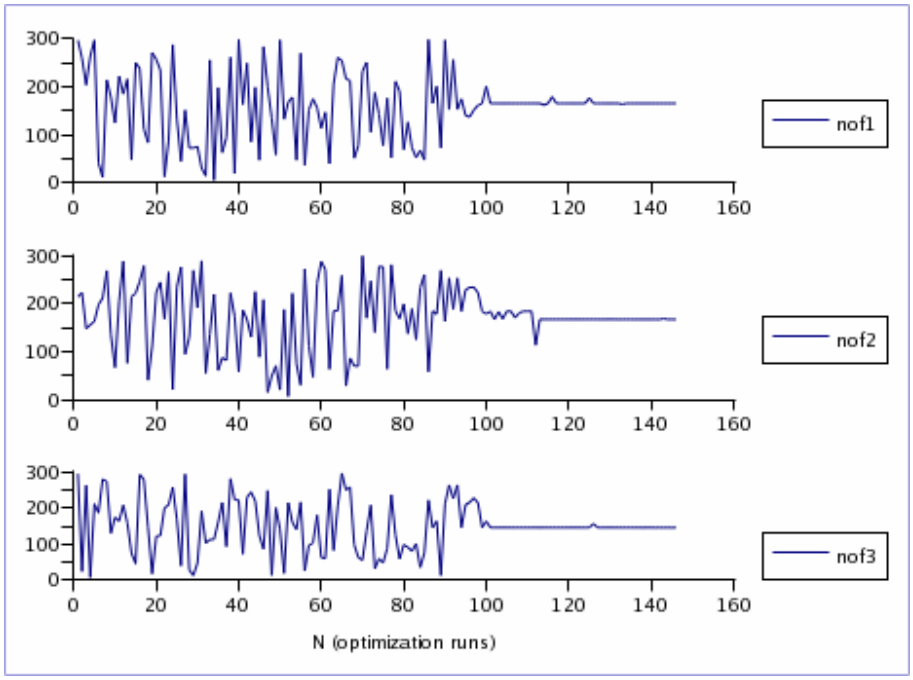


Figure 5-24 Number of fingers of the cascode transistors M_1, M_2 and the current steering transistor M_3.

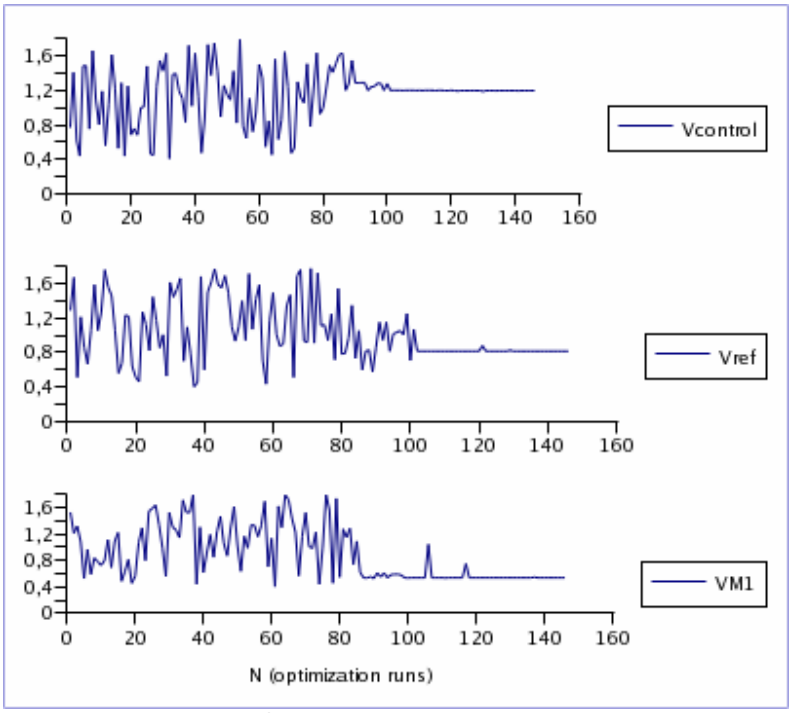


Figure 5-25 Evolution of bias voltages.

Finally in Figure 5-22 the gain as a function of control voltage is shown.

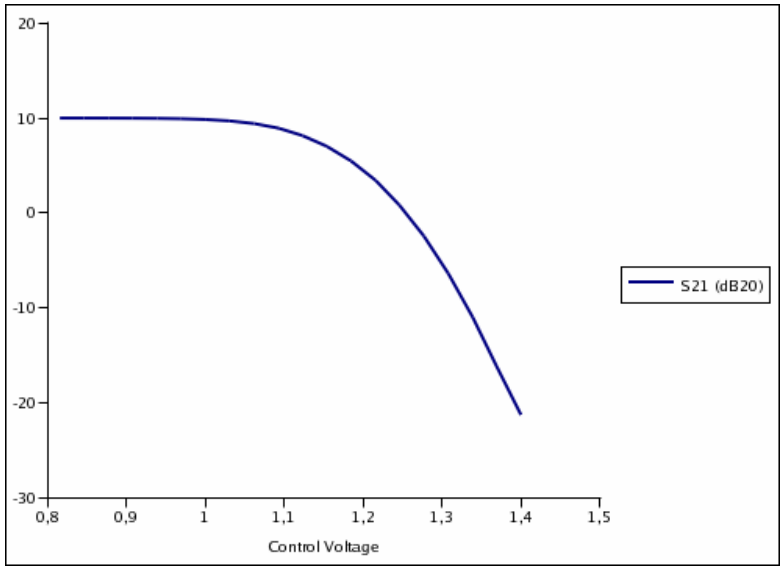


Figure 5-26 Variable gain.

The VGA results summarized in Table IV, produced in a small period of time only 12 min, constitute a truly optimal solution compared with the results reported in [25] for the same topology, where for a maximum gain of 20.6 dB and a bias current of 2mA, with the same center frequency the noise figure was 1.47 dB and the minimum noise figure was 0.76dB.

5.3 Summary-Comparison

The LC-tank optimization process of the Colpitts VCO of Fig. 2(a) required 144 iteration with a total duration of 36 minutes on a 2.6GHz Pentium 4 Linux PC. This could be significally improved (to less than 15 minutes) if interprocess communication between octave and ocean is used, since the penalty of the overhead of ocean start up and spectre licence checkout will be paid only once (not 144 times). Due to simulation intensive PSS simulations in SPECTRE™, the active circuit optimization required 135 iterations with a total execution time of 6 hours. This can be significally reduced if the PSS/PNOISE tolerances are dynamically straighten as the algorithm approaches settling space, previous PSS transient information is reused and or a harmonic simulator is used.

The optimization variables and simulation times for all three VCO topologies of Figures 2-21, 2-30 and 2-31 are summarized in Table III. It should be noticed that the overall optimization time for the quadrature oscillators is significally higher than that of the other two topologies. This is attributed to the complexity of the circuit, which doubles the PSS simulation time.

TABLE III
VCO OPTIMIZATION RESULTS

	Colpitts	Cross Coupled	PQVCO	SQVCO
Oscillation Frequency (GHz)	5.44	5.40	5.40	5.40
Phase Noise @ 100KHz (dBc/Hz)	-102	-95.8	84.36	-93.5
I_{bias} (mA)	5.94	2.7	15	8.89
Quality Factor Q	17.11	25.2	26.2	25.1
N_{ratio}	0.22			
Inductance L (nH)	0.682	0.600	0.493	0.700
Coil Radius, Spiral Width (um)	220 18.7	214 20.2	188 18.3	189 10.6
Max Variable Capacitance C_{max} (pF)	5.68	1.42	1.71	1.21
MOS varactor sizing : finger width, # gates, multiplicity	2.18 23 77	2.65 15 25	1.77 19 33	1.95 7 58
Fixed Capacitance C_1 (pF)	1.61			
Finger Width	M1=2.23 M2=2.23	M1=1.27	M1=1.83 M_{cpl}=1.83	M1=1.92 M_{cpl}=1.92
# Fingers	M1=26 M2=6 M3=10 M4=8	M1=27 M2=9 M3=8	M_{cpl}=18 M1=87 M2=9 M3=8	M_{cpl}=90 M1=17 M2=10 M3=9
Tuning Range	5.1 – 5.8	5.1 – 5.8	5.1 – 5.8	5.1 – 5.8
Total Evolutions	279	277	300	289
Total Time	6h,36min	7h,56min	15h	14h,9min

The results illustrated in Table III are in agreement with the theory in sections 2.3.3 and 2.3.4. The differential Colpitts oscillator indeed, presents a superior phase noise performance with -102 dBc/Hz against the cross-coupled LC oscillator with -95.8 dBc/Hz in 100KHz offset from a 5.4GHz carrier. At the same time as theory predicted the power consumption for the Colpitts oscillator has double the power consumption of the cross-coupled LC oscillator.

In the case of the two quadrature oscillators the serial coupled while it consumes less power than the parallel coupled, improves phase noise performance of the latter by almost 10dBc/Hz.

Finally a summary of VGA results is illustrated in Table IV.

TABLE IV
VGA OPTIMIZATION RESULTS

VGA		M_1 M_2 M_3	$V_{control}$ V_{ref} V_{M1}
NF (dB10)	1.14		
Bandwidth (MHz)	696		
Max S21 spec(dB20)	10		
Max S21 (dB20)	9.99		
Min S21 (dB20)	-21		
I_{bias} spec (mA)	2		
I_{bias} (mA)	2.57		
# Fingers		166 167 146	
Voltages (V)			1.2 0.816 0.536
Evaluations	145		
Total Time (min)	12		

Chapter 6 : Layout

Layout in 0.18μm technology requires careful attention to the effects of parasitics that can heavily affect the performance of the circuits. Symmetry and minimization of area are other important layout considerations for any circuit. The layout of the Cross-Coupled VCO designed in chapter 4 has been developed to meet all these factors as closely as possible. Some of the techniques that have been employed for creating a good layout [10] are described below.

6.1 Multi-finger transistors

When very wide transistors need to be laid out, the use of multiple fingers, while the gate is double sided and connected by metal lines, is common practice (Figure 6-1).

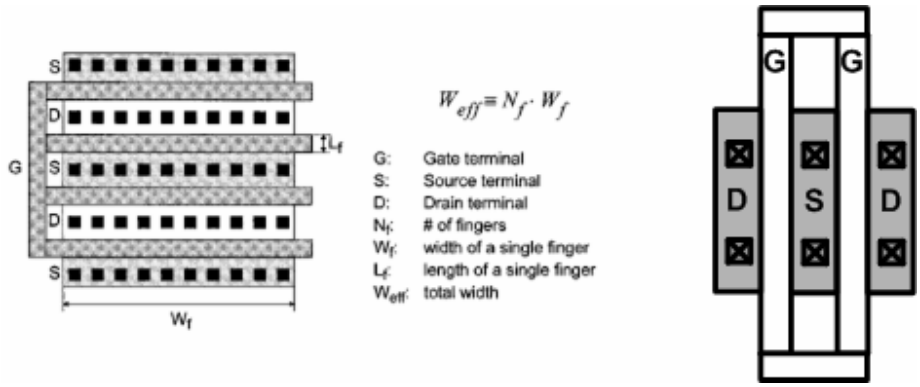


Figure 6-1a)Layout of a typical RF MOS transistor and b) double sided gate connection.

The number of fingers is decided based on the drain current of the transistor and the need for minimization of gate resistance as shown in section 4.2.

A trade-off involved in using a large number of fingers to minimize gate resistance is the increase in the capacitance associated with the perimeter of the source and drain areas.

6.2 Symmetry

It is essential to have a very symmetric layout in order to minimize mismatches and the resulting input referred offset voltage. Other advantages of symmetry are better common mode and power supply noise rejection and reduced even-

harmonic distortion. The use of dummy transistors (or resistors and capacitors depending on the component under consideration) on either side of a matched pair of transistors helps prevent asymmetries by ensuring that both sides of the two transistors see approximately the same environment. To achieve very good matching between two components, it is very important that they be laid out in the same orientation. This is because certain steps in lithography and wafer processing behave differently along different axes, giving rise to mismatches if two components are not oriented along the same axis. Using very wide transistors also increases the probability of mismatch due to the gradients along a certain axis. To ameliorate this problem, common centroid configurations are used in cases requiring a high degree of matching. However, routing of interconnects becomes very tedious if the circuit is large, often giving rise to systematic mismatches. The layout of the nMOS cross-coupled transistors is schematically reproduced in Figure 6-2.

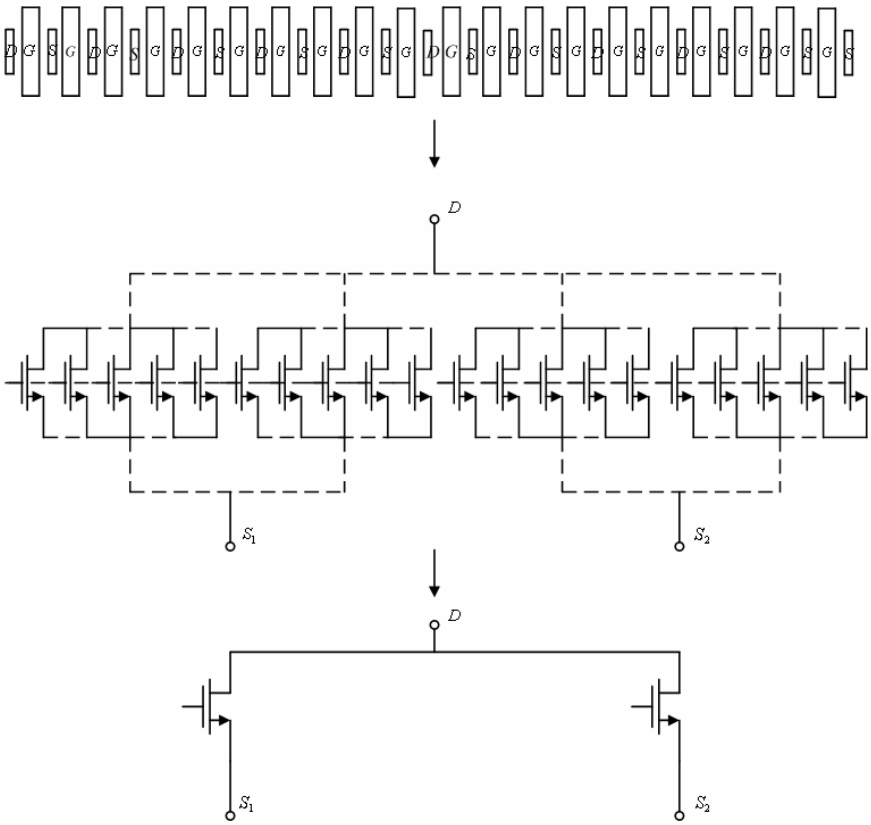


Figure 6-2 Matching of the cross coupled nMOS transistors.

6.3 Top level layout

The top-level layout of the cross-coupled VCO is shown in Figure 6-3.

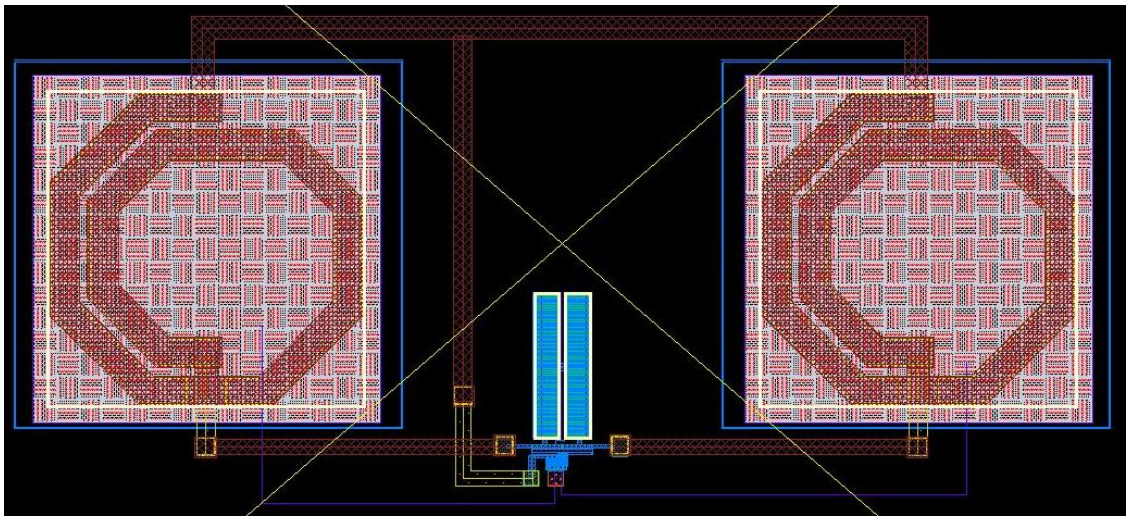


Figure 6-3 Cross coupled voltage controlled oscillator.

6.4 Post-layout Simulations

Post-layout simulation results are provided for the cross-coupled VCO designed in 0.18µm CMOS technology. The effects of parasitic resistances and capacitances are observed in these simulations, as a result of which the specifications achieved are slightly different from those of the schematic.

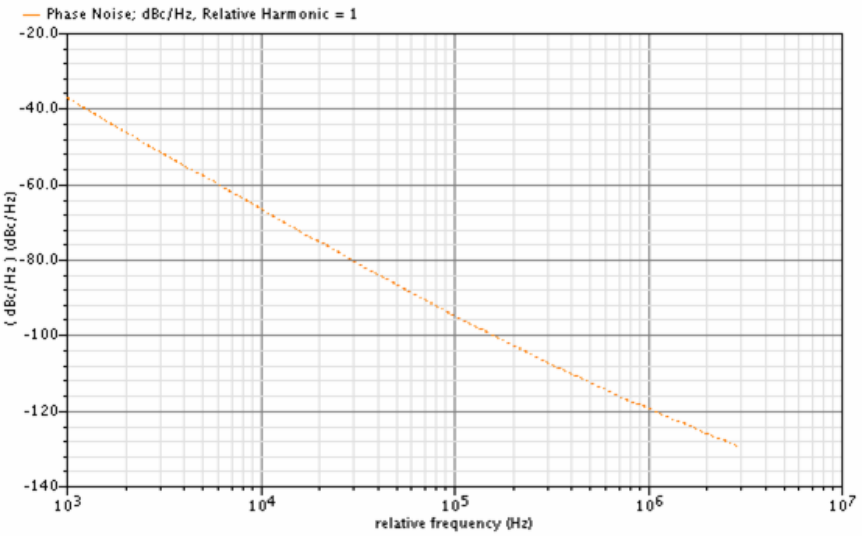


Figure 6-4 Phase noise spectrum.

The oscillation frequency has been slightly shifted to 5.35 GHz and phase noise has been degraded by 0.8 dBc.

Chapter 7 : Conclusion

The main contribution of this work includes introducing a novel approach [51] on automated RF IC optimization that is the built in of prior knowledge in the core of the selected optimizing algorithm. It has been shown how designer's experience can be leveraged in an automated simulation-based optimization scheme, helping the genetic algorithm to gain efficiency minimizing simulation time and converging to a near globally optimal solution. First, the technique has been applied on various oscillator topologies to solve the phase noise – power consumption trade-off in an effective way, producing satisfying results in a small period of time. Afterwards, a simple variable gain amplifier has been optimized in a knowledge-free approach, targeting minimal noise figure and power consumption. The successful application of knowledge and knowledge-free optimization in complex and non-complex circuits respectively, demonstrates the usability of the presented technique for a wide variety of circuits, regardless of their complexity.

APPENDIX A

The ocean script of the first optimization phase is shown below.

```
1.  simulator( 'spectre )
2.  design(  "/home/george/simulation/LC-tank/spectre/schematic/netlist/netlist")
3.  resultsDir( "/home/george/simulation/LC-tank/spectre/schematic" )
4.  modelFile(
5.  '("/home/george/libraries/IBM_PDK/bicmos7wl/V1.3.2.0DM/Spectre/models/design.scs"
    "")
6.  '("/home/george/libraries/IBM_PDK/bicmos7wl/V1.3.2.0DM/Spectre/models/process.scs"
    "")
7.  analysis('sp ?ports list("/PORT0")  ?start "1000000000"  ?stop "20000000000"  )
8.  temp( 27 )
9.  load "parameters.ocn"
10. run()
11. L = (x = (value(imag(ZP("/PORT0" "/PORT0")) 5.47e+09) / (6.28 * 5.47e+09)))
12. myport = outfile("inductance" "a");
13. fprintf(myport "%e\n" L );
14. design(  "/home/george/simulation/mos-cap/spectre/schematic/netlist/netlist")
15. resultsDir( "/home/george/simulation/mos-cap/spectre/schematic" )
16. modelFile(
17. '("/home/george/libraries/IBM_PDK/bicmos7wl/V1.3.2.0DM/Spectre/models/design.scs"
    "")
18. '("/home/george/libraries/IBM_PDK/bicmos7wl/V1.3.2.0DM/Spectre/models/process.scs"
    "")
19. analysis('dc ?saveOppoint t  )
20. analysis('sp ?ports list("/PORT0")  ?start "1000000000"  ?stop "20000000000"  )
21. temp( 27 )
22. load "parameters.ocn"
23. run()
24. C = (x1 = abs((1 / (6.28 * 5.47e+09 * value(imag(ZP("/PORT0" "/PORT0")) 5.47e+09)))))
25. myport2 = outfile("capacitance" "a");
26. fprintf(myport2 "%e\n" C );
27. design(  "/home/george/simulation/LC-tank11/spectre/schematic/netlist/netlist")
28. resultsDir( "/home/george/simulation/LC-tank11/spectre/schematic" )
29. modelFile(
30. '("/home/george/libraries/IBM_PDK/bicmos7wl/V1.3.2.0DM/Spectre/models/design.scs"
    "")
31. '("/home/george/libraries/IBM_PDK/bicmos7wl/V1.3.2.0DM/Spectre/models/process.scs"
    "")
32. analysis('sp ?ports list("/PORT0")  ?start "1000000000"  ?stop "20000000000"  )
33. temp( 27 )
34. load "parameters.ocn"
35. run()
36. C1 = evalstring(desVar("C1"));
37. Cpl = (qwe = ((C1*C)/(C1+C)))
38. Cl = (qw = (C1/(C1+C)))
39. myport23 = outfile("Cparallel" "a");
40. fprintf(myport23 "%e\n" Cpl );
41. myport22 = outfile("Nratio" "a");
42. fprintf(myport22 "%e\n" Cl );
43. myport20 = outfile("C1" "a");
44. fprintf(myport20 "%e\n" C1 );
45. Qt = (s = ((1 / value(real(YP("/PORT0" "/PORT0")),5.47e+09)*sqrt(L*Cpl))/L))
```

```
46. Fosc= (qwee = (1 / (6.28*sqrt(L*Cpl))))
47. Cost = (c = ((Qt*0.95e+8) - abs(Fosc - 5.47e+9) - (3.87e+9*abs(Cl-0.2)))
48. ocnPrint(?output "./konstantopoulos" ?numberNotation "engineering" Cost);
49. ocnPrint(?output "./Res_Freq" ?numberNotation "engineering"  Fosc);
50. myport3 = outfile("Qt_frequency" "a");
51. fprintf(myport3 "%e        %e\n" Qt Fosc );
```

First the spectre simulator is invoked. In lines 2 – 6 the paths for the oscillator design, the directory where the results will be saved and the models of the various circuit components necessary for the simulations to be performed are defined respectively. In line 7, S-parameters analysis is defined. The *load* command in line 9 passes to the simulator the circuit design parameters generated by the genetic algorithm in each loop. The lines below the command *run* are used for post-simulation processing. Especially in line 11 the inductance of the coil is estimated and its value is saved in a file in line 12.

Similarly in lines 13 – 51 two more designs are simulated, the MOS varactor and the LC-tank in order to estimate the capacitance of the first component and the quality factor of the second. Finally, in line 47 the fitness function is defined and its value is saved in a file which the octave script that implements the genetic algorithm will open to retrieve (line 51).

In the first octave script, optimization.m, the bounds of the independent variables involved in the optimization process are defined and the function that implements the genetic algorithm [39] is called. In the file, evolve.m, the circuit design parameters generated by the, optimization.m, are written in the parameters.ocn in a special format that can be recognized and processed by the ocean script described above that is finally invoked. The file evolve.m is shown below:

```
1.  function y = simple(sol)
2.  fid=fopen('parameters.ocn','w');
3.  qwe = fopen('param_trace.dat','a');
4.  fprintf(fid,'desVar("SW" %e)\n',sol(1));
5.  fprintf(fid,'desVar("OD" %e)\n',sol(2));
6.  fprintf(fid,'desVar("RX" %e)\n',sol(3));
7.  fprintf(fid,'desVar("nog" %e)\n',sol(4));
8.  fprintf(fid,'desVar("multiplicity" %e)\n',sol(5));
9.  fprintf(fid,'desVar("C1" %e)\n',sol(6));
10. fprintf(qwe,'%e  %e      %e      %e      %e
            %e\n',sol(1),sol(2),sol(3),sol(4),sol(5),sol(6));
11. fclose(qwe);
```

```
12. fclose(fid);
13. system("ocean")
14. sid=fopen('konstantopoulos','r');
15. A = fscanf(sid,'%e',inf);
16. fclose(sid);
17. zid=fopen('Res_Freq','r');
18. Res_Freq = fscanf(zid,'%e',inf);
19. fclose(zid);
20. y=A
21. a=y
22. asd=fopen('Yresults','a');
23. fprintf(asd,'%e\n',a);
24. fclose(asd);
```

The ocean script of the second optimization phase is shown below.

```
1. ocnWaveformTool( wavescan )
2. simulator( spectre )
3. design(
   "/home/george/simulation/collpitts_noise_anal_diff_vco/spectre/schematic/netlist/netlist")
4. resultsDir( "/home/george/simulation/collpitts_noise_anal_diff_vco/spectre/schematic" )
5. modelFile(
6. '("/home/george/libraries/IBM_PDK/bicmos7wl/V1.3.2.0DM/Spectre/models/design.scs"
   "")
7. '("/home/george/libraries/IBM_PDK/bicmos7wl/V1.3.2.0DM/Spectre/models/process.scs"
   "")
8. analysis('dc ?saveOppoint t  )
9. analysis('pnoise ?sweeptype "relative"  ?relharmnum "1"  ?start "1000"
        i.  ?stop "3e+6"  ?maxsideband "7"  ?p "/voutP"  ?n "/voutN"
       ii.  ?oprobe ""  ?iprobe ""  ?refsideband ""  )
10. analysis('pss ?fund "5e+9"  ?harms "3"  ?errpreset "moderate"
        i.  ?tstab "200n"  ?p "/voutP"  ?n "/voutN"  )
11. option(  vabstol  "1e-8" reltol  "1e-5")
12. temp( 27 )
13. load "parameters.ocn"
14. save( i "/TN4/D" )
15. run()
16. current = (I = IDC("/TN4/D"));
17. cost = (c = abs(harmonic((v "/voutP" ?result "pss-fd.pss" ?resultsDir
    "/home/george/simulation/collpitts_noise_anal_diff_vco/spectre/schematic") 1)));
18. Fosc = (fo = harmonic(xval((v "/voutP" ?result "pss-fd.pss" ?resultsDir
    "/home/george/simulation/collpitts_noise_anal_diff_vco/spectre/schematic")) 1));
```

19. *PPNoise = (x = abs(value(phaseNoise(1 "pss-fd.pss" ?result "pnoise-pnoise") 100000)));*
20. *Cost = (c = ((PPNoise*1e+8)*0.7 - 6*abs(Fosc - 5.4e+9) - 6e+10*abs(current)));*
21. *ocnPrint(?output "./konstantopoulos" Cost ?numberNotation "engineering");*
22. *myport = outfile("/home/george/Desktop/icfb_work/PhaseNoise" "a");*
23. *fprintf(myport "%e %e\n" PPNoise Fosc);*
24. *myport1 = outfile("/home/george/Desktop/icfb_work/CurrentSave" "a");*
25. *fprintf(myport1 "%e \n" current);*
26. *ocnPrint(?output "/home/george/Desktop/Fosc" Fosc ?numberNotation "engineering");*

First the spectre simulator is invoked. In lines 2 – 7 the paths for the oscillator design, the directory where the results will be saved and the models of the various circuit components necessary for the simulations to be performed are defined respectively. In lines 8 – 10 the type of the required analyses in order to characterize the performance of the oscillator are defined, while in line 11 some variables that controls the accuracy of the simulations are shown. The *load* command in line 13 passes to the simulator the circuit design parameters generated by the genetic algorithm in each loop and finally in line 14 the simulation is started. The lines below the command *run* are used for post-simulation processing. Especially to declare and retrieve performance metrics, such as the bias current (line 16), the oscillation frequency (line 18) and the phase noise (line 19), in order to calculate the fitness function defined in line 20. Then the performance metrics are stored to separate files (lines 22-26), while the value of the fitness function is also saved in a file which the octave script that implements the genetic algorithm will open to retrieve (line 21).

The interaction with the octave files of genetic algorithm is similar as mentioned previously for the first optimization phase.

The bounds configured in the file, optimization.m, or in other words the optimization search space is shown for both VCO and VGA cases in Table V.

TABLE V VCO and VGA SEARCH SPACE					
	Colpitts	Cross Coupled	PQVCO	SQVCO	VGA
Outer Dimension (um)	180 – 450	180 – 450	180 – 450	180 – 450	
Spiral Width (um)	5 – 25	5 – 25	5 – 25	5 – 25	
MOS varactor Finger Width (um)	1.5 – 4	1.5 – 4	1.5 – 4	1.5 – 4	
Number of Gates	5 – 40	5 – 40	5 – 40	5 – 40	
Multiplicity	20 – 80	20 – 80	20 – 80	20 – 80	
Fixed Capacitor (pF)	0.5 – 4				
MOS M_1 Finger Width (um)	1.8 – 4	1.8 – 4	1.8 – 4	1.8 – 4	
Number of Fingers M_1	15 – 50	20 – 40	40 – 120	15 – 50	5 – 300
Number of Fingers M_2	5 – 30	8 – 22	10 – 50	8 – 22	5 – 300
Number of Fingers M_3	4 – 10	8 – 22	8 – 22	8 – 22	5 – 300
Number of Fingers M_4	4 – 10		8 – 22		
Number of Fingers M_{cpl}				45 – 250	
Voltage V_{ref} (V)					0.4 – 1.8
Voltage V_{M1} (V)					0.4 – 1.8
Voltage $V_{control}$ (V)					0.4 – 1.8

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