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Telecommunication Circuits Design and Development Using FPGA Technology

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Abstract: The wide application of FPGA chips becomes a trend in telecommunications and wireless communications era. FPGAs have been deployed in numerous fields of electronics engineering. Thus, the adoption of FPGAs in telecommunications curriculum it is necessity. This paper emphasizes on a collaborative approach to teach undergraduate state of the art telecommunications and wireless communications in the Broadband Communications & ElectroMagnetic Applications (BCEMA) Laboratory of the Department of Electronic Engineering (DoEE) of the Technological Educational Institute of Crete (TEIoC).

Keywords: *Wireless communications, FPGA, Microstrip antenna, Filter, Model course*.

1. INTRODUCTION

The embedded systems technology is increasingly bringing new levels of performance to next-generation circuitry for several applications. With the inclusion of FPGA chips in communication systems, substantial processing power along with software programmability and upgradability are combined with the performance, robustness and flexibility of a custom circuit design. FPGA's holding many advantages, such as the high processing speed, the inherent flexibility, the low level reconfigurability, the parallelism ability, the rapidly decreasing price and the high performance/cost ratio, FPGAs have become the ideal choice for application-specific circuits and devices. In the early 1990s, FPGAs were primarily used in telecommunications and networking and soon found their way into consumer, automotive and industrial applications. For example, many of today's RF instruments already benefit from fixed-functionality FPGA's, in order to execute tasks such as flatness correction, ADC linearization, IQ calibration and digital down-conversion [1]-[2].

This paper focuses on telecommunications education at the DoEE of TEIoC, whose undergraduate curriculum includes an advanced elective course in communication electronics, called "Electronic and RF Technologies". This course is fully supported by the BCEMA Lab, with exercises, simulations, measurements and lab projects, like the presented herein. The results obtained herein are based on work carried out by students of the DoEE of TEIoC, during their six month workplace learning period at the BCEMA Lab. Under the supervision of academic and technical staff, the students upgrade their skills and professional qualifications through their involvement in research-related tasks with the use of specialized hardware and software. Furthermore, the laboratory's resultant overall research and development work promotes the innovation and knowhow transfer processes in the areas of wireless communications, antennas, microwave structures, electromagnetic radiation, etc..

In order to make our students ready for the complex requirements and difficult problems they will face as radio frequency (RF) engineers, we guide them to use and develop supple solutions. And embedded systems provide a flexible solution for many telecom applications, as they can be modified not only during system development but also after being deployed in the field.

The design process of FPGA-based circuits for educational purposes is described with the use of Matlab, Simulink and Xilinx ISE Design Suite. These software tools are used to translate the advanced Matlab code into VHDL code for hardware-level implementation, and finally design and develop simple and complex communication circuits. Moreover, a few advanced students combine their circuits with FPGA-based signal processing, resulting in usage of the developed configurations in a wide range of embedded applications [3]-[4].

2. FPGA BOARD AND SOFTWARE

After a comparative of the available boards and software tools the decision for this course was use Digilent's Nexys 2 FPGA board which features Xilinx' Spartan3E FPGA as shown in Figure 1.

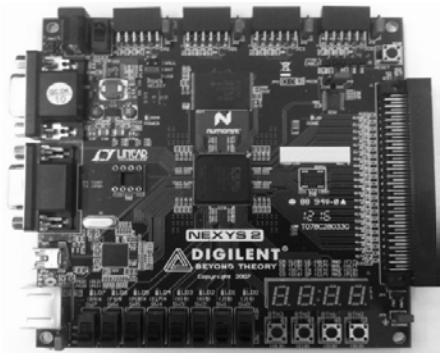

Figure 1: The Nexys 2 board.

On the other hand the software that we used to our course was the combination of Mathworks MATrixLABoratory and Xilinx Integrated Software Environment Design Suite. More details about the board and the software are given below [5]-[6].

2.1. DIGILENT NEXYS 2 FPGA BOARD

This board features Xilinx's Spartan3E 500K gate FPGA, USB-based FPGA configuration and high-speed data transfers, 16MB of Micron PSDRAM & 16MB of Intel Strata Flash ROM, Xilinx Platform Flash for nonvolatile FPGA configurations, Efficient switch-mode power supplies (good for battery powered applications), 50MHz oscillator plus socket for second oscillator, 60 FPGA Inputs/Outputs routed to expansion connectors (one high-speed Hirose FX2 connector and four 6-pin headers) and 8 LEDs, 4-digit 7-segment display, 4 buttons plus 8 slide switches.

Table 1: Spartan3E 500K specifications.

Device	CLB Rows	CLB Columns	CLB Total	Slices	LUTs / Flip-Flops	Equivalent Logic Cells	RAM16 / SRL16	Distributed RAM Bits
XC3S-500E	46	34	1,164	4,656	9,132	10,476	4,656	74,496

The Spartan3E 500K gate FPGA features 46 rows and 34 columns of configurable logic blocks (CLB) offering a total of 1,164 CLBs, 4,656 slices which offer 9,132 Flip-Flops and look up tables (LUT), 10,476 logic cells (each logic cell consists of a lookup table, a flip-flop

and connections to adjacent cells), 4,656 blocks of 16-bit RAM / 16-bit Shift Registers (SRL) and 74,496 distributed RAM bits. This example's requirements don't exceed the board specifications but more advanced implementations require larger capacity (i.e. porting a trained neural network or installing IP cores for specific instructions). Within Table 1, the characteristics of the Spartan3E 500K gate FPGA are presented [2], [4].

2.2. MATHWORKS MATLAB

Mathworks Matlab provides us with a set of powerful,yet easy to use, tools to design, visualize and simulate a countless number of design in a wide range of areas. One of these tools is Simulink. Simulink is a simulation and model based design tool which, when combined with the Xilinx System generator toolbox, can help among others in designing DSP's, telecommunications, aerospace, and embedded system designs.

We will be using the system generator library with which we can create subsystems for these equations and simulate their behavior. By doing so we can easily create a model that consists of those subsystems and by giving it the geometrical characteristics of a microstrip antenna it can calculate, for example, the resonant frequency or the effective dielectric constant. Depending on the mathematical analysis that we choose we could make our model calculate any characteristic of the microstrip we need.

After we have decided on what our models purpose will be, we can easily translate it into VHDL code using Simulink's HDL Workflow Advisor tool as shown in Figure 2. This tool will help with the debugging of our design and the VHDL code conversion. At the end of this process we will have the testbench file, which will contain signals to test our system, along with the generated code for use with the FPGA design software to finally program the FPGA.

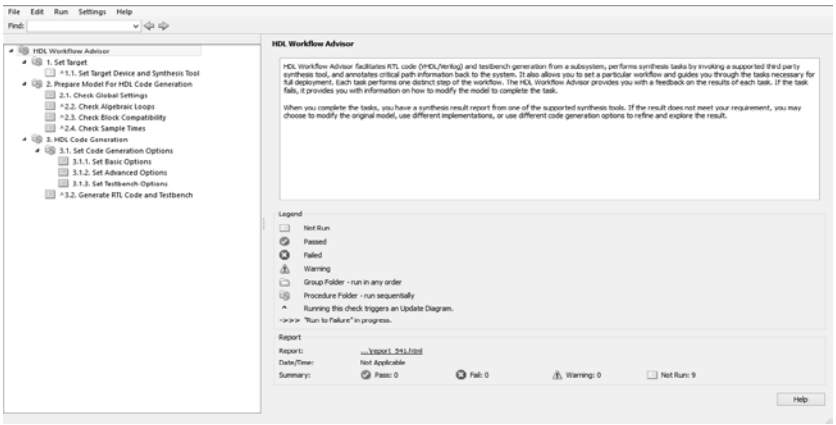

Figure 2: Simulink's HDL workflow advisor.

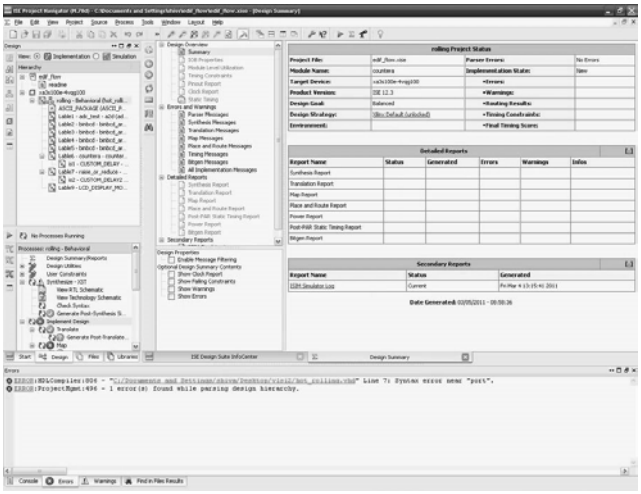

Figure 3: The graphical user interface of the Xilinx ISE Design Suite.

There are many tools to transfer the VHDL code in the FPGA. Xilinx's ISE Design Suite is a complete solution for the design of any implementation as shown in Figure 3. After choosing the correct FPGA options (depending on the make and model) we can add the VHDL code and testbench file that was generated in Simulink to begin the synthesizing process. In this stage the Design Suite runs a few checks to validate our code. When these tests are done and passed with no errors we can begin finalizing our implementation and bring our code to its final form which is the actual ROM file that will program the FPGA [2].

3. MICROSTRIP ANTENNAS

In applications where size, weight, cost, performance, ease of installation, or even aerodynamic profile are constraints, it is mandatory to use low profile antennas. Most of these requirements are met by microstrip antennas [7]. They are low-profile, simple, easy to manufacture using printed circuit technology, and when the specific patch shape and mode are selected, they are very versatile in terms of resonant frequency, polarization, pattern and impedance [7]. Their biggest disadvantages are: low efficiency, low power, poor polarization purity, poor scan performance, spurious feed radiation and very narrow frequency bandwidth [7]. Microstrip antennas consist of a very thin metallic strip (with thickness $t << \lambda_0$, where λ_0 is the free-space wavelength) placed above a ground plane (at a small height $h << \lambda_0$, usually $0.03\lambda_0 \leq h \leq 0.05\lambda_0$) [7]. The microstrip patch is designed, so its pattern maximum is normal to the patch. This is accomplished by properly choosing the excitation mode beneath the patch [7].

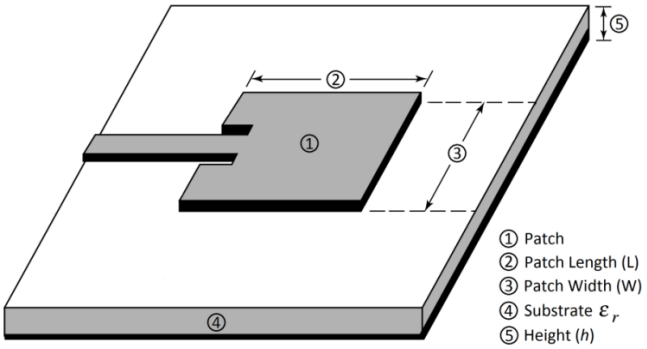

Figure 2: Microstrip antenna geometry [7].

Our goal is to take the following equations, which compute the characteristics of a microstrip antenna, and create Simulink models that produce accurate results when applied to the FPGA development board. In our Simulink models we used the following equations [7]:

$$L = \frac{c}{\sqrt{2f_r \varepsilon_{reff}}}$$

$$W = \frac{c}{2f_r}\sqrt{\frac{2}{1+\varepsilon_r}}$$

$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[1 + 12\frac{h}{W}\right]^{-\frac{1}{2}}$$

$$\frac{\Delta L}{h} = 0.412\frac{(\varepsilon_{reff} + 3)\left[\frac{W}{h} + 0.264\right]}{(\varepsilon_{reff} - 0.258)\left[\frac{W}{h} + 0.8\right]}$$

$$f_r = \frac{1}{2L\sqrt{\varepsilon_r}\sqrt{\varepsilon_0 \mu_0}}$$

where L is the patch length, W is the patch width, ε_{reff} is the effective dielectric constant, $\Delta L/h$

is the normalized extension length, and fr is the resonant frequency (for the dominant mode in case of L>W and no fringing).

4. RESULTS

Figure 3 presents the model of the ε_{reff} implementation consisted from the constant, divide, addition, substraction, multiplication, input and output blocks. The HDL code generated from the above block diagram presented in Figure 4.

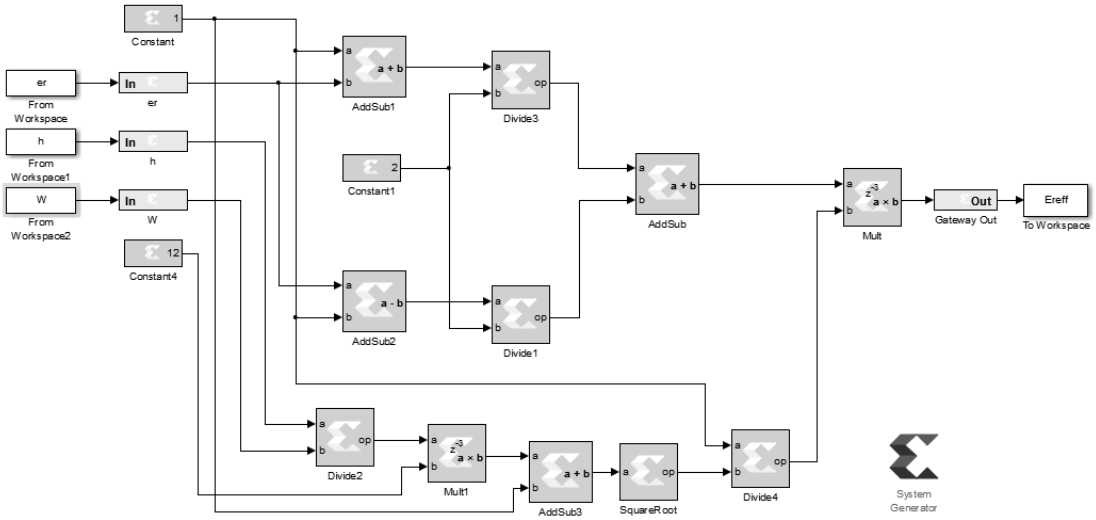

Figure 3: Behind the mask of the ε_{reff} implementation.

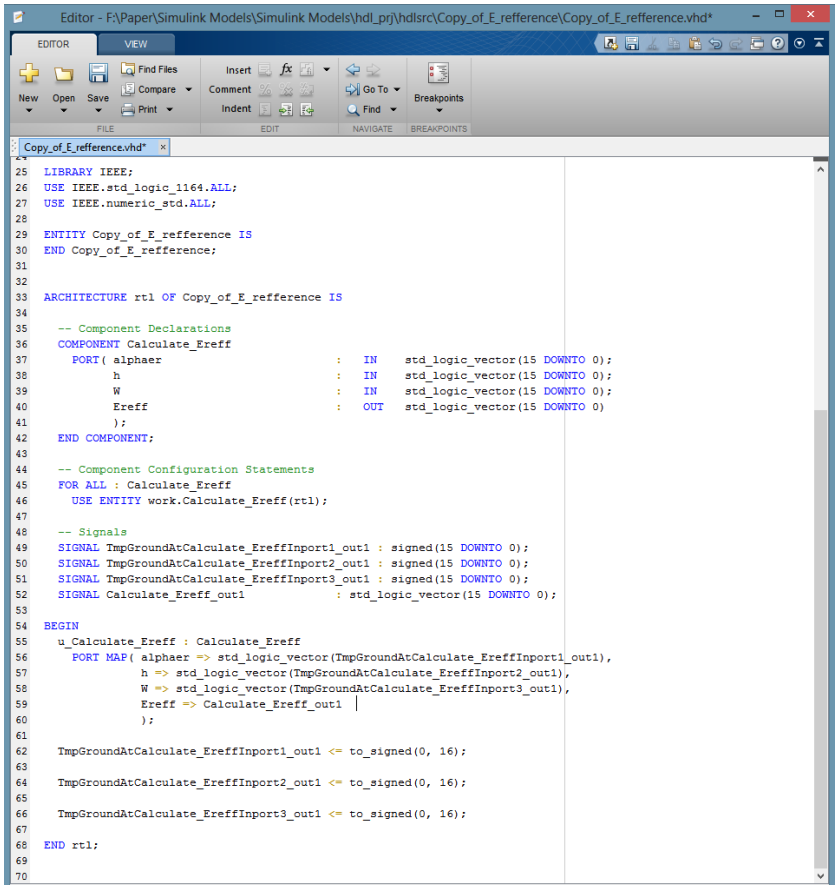

Figure 4: VHDL code as generated from MATLAB HDL coder.

5. CONCLUSION

During this process we have created a Simulink model consisting of several subsystems which can provide us with the characteristics of a microstrip antenna given its geometrical specifications. By converting this model to a VHDL code we used the Xilinx ISE design Suite to validate and finalize our project and ultimately install it on a FPGA board. Although the Xilinx ISE Design Suite is a complete set of tools to create any model without the use of Matlab or Simulink, by using the compatibility between them it is easier to visualize and this way better understand the structure and functionality of the design. One thing about FPGAs is that they can be transformed into powerful tools that can be reconfigured and redeployed countless times to suit the needs of the applications. By going through these steps the electronics engineering candidates have the chance to scrape the surface of the design and prototyping procedures or even go further than that, should they choose so, into advanced circuit implementations such as LTE transceiver design or even artificial neural networks.

Most students find that the FPGA projects interesting, challenging and engaging. More specifically, the number of students wishing to carry out their diploma thesis in this field of communications has increased and their interest to experiment with new. The latter is related to issues concerning the modification and extensions such as software defined radios (SDR) of FPGAs in telecommunications, issues that are planned to be covered in future offerings of our lab course.

6. ACKNOWLEDGMENT

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