TECHNICAL UNIVERSITY OF CRETE

School of Electrical & Computer Engineering

Study of Enclosed Gate N-Type MOS Field Effect Transistors – Characterization and Variability

Diploma Thesis

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Abstract

MOSFETs are by far the most commonly used transistors in digital circuits, as millions of them may be included in a memory chip or a microprocessor. Since they can be made with either P-type or N-type semiconductors, complementary pairs of MOS transistors can be used to make switching circuits with very low power consumption, in the form of CMOS logic.
Being such an essential part of microelectronics, different types of MOSFETS need to be studied in order to find the optimal for each need of the industry. Transistors with enclosed gate layouts seem to be the optimal solution for applications in radiation-hard environments since due to their geometry and the absence of STI corners, there is no possible leakage current path along the edge of the active area.
In this thesis we study enclosed gate N-type MOS Field Effect Transistors. Specifically, we study the voltage – current relation, the transconductance, the threshold voltage, the electron mobility, the slope factor. These characteristics are the result of an experimental measurement procedure. The characteristics above have been extracted from seven transistors with different geometry, each with a different channel length and width. The study covers both linear and saturation modes of operation. Furthermore, matching properties, for different electrical characteristics of transistors with the same geometry, have been extracted, in view of using enclosed gate transistors in analog integrated electronics.

Περίληψη

Το MOSFET είναι μακράν το πιο συνηθισμένο τρανζίστορ στα ψηφιακά συστήματα, καθώς εκατομύρια από αυτά μπορεί να περιλαμβάνονται σε ένα τσιπ μνήμης ή έναν μικροεπεξεργαστή. Αφού μπορούν να κατασκευαστούν είτε με τύπου-P είτε με τύπου-N ημιαγωγούς, συμπληρωματικά ζεύγη από MOS τρανζίστορ μπορούν να χρησιμοποιηθούν για να κατασκευάσουμε κυκλώματα διακοπτών με πολύ χαμηλή κατανάλωση ενέργειας, στην μορφή της λογικής CMOS.

Το γεγονός ότι τα MOSFET είναι ένα τόσο σημαντικό στοιχείο στα ηλεκτρονικά κυκλώματα, δημιουργεί την ανάγκη μελέτης διαφορετικών τύπων MOSFET έτσι ώστε να βρεθεί ο ιδανικός για κάθε διαφορετική ανάγκη της βιομηχανίας. Τα τρανζίστορ με περικλεισμένη πύλη φαίνεται να είναι η βέλτιστη λύση για εφαρμογές σε περιβάλλοντα με έντονη ραδιενέργεια καθώς εξαιτίας της γεωμετρίας τους και της έλλειψης γωνιών STI, περιορίζεται κατά πολύ το ρεύμα διαρροής.

Σε αυτή την διπλωματική μελετόνται τρανζίστορ επίδρασης πεδίου MOS τύπου-N με κυκλική πύλη. Πιο συγκεκριμένα, μελετάται η σχέση τάσης – ρεύματος, η διαγωγημότητα, η τάση κατωφλίου, η κινητικότητα των ηλεκτρονίων, ο συντελεστής κλήσης μετά από εκστρατεία πειραματικού χαρακτηρισμού. Τα παραπάνω χαρακτηριστικά έχουν εξαχθεί για επτά διαφορετικά τρανζίστορ με διαφορετικό μήκος και πλάτος καναλιού. Η ανάλυση αυτή συμπεριλαμβάνει τόσο την γραμμική λειτουργία όσο και την λειτουργία κορεσμού. Επιπροσθέτως, έχει μελετηθεί το ταίριασμα (matching) ομοίων τρανζίστορ με ίδια γεωμετρία, με στόχο την χρήση των τρανζίστορ με κυκλική πύλη σε αναλογικά ολοκληρωμένα ηλεκτρονικά ακριβείας.

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1. INTRODUCTION

1.1 The MOSFET

The basic principle of the field-effect transistor (FET) was first proposed by Austro-Hungarian physicist Julius Edgar Lilienfeld in 1925. However, his early FET concept was not a practical design. The FET concept was later also theorized by Oskar Heil in the 1930s and William Shockley in the 1940s, but there was no working practical FET built at the time. A breakthrough came with the work of Egyptian engineer Mohamed M. Atalla in the late 1950s. He investigated the surface properties of silicon semiconductors at Bell Labs, where he adopted a new method of semiconductor device fabrication, coating a silicon wafer with an insulating layer of silicon oxide, so that electricity could reliably penetrate to the conducting silicon below, overcoming the surface states that prevented electricity from reaching the semiconducting layer. This is known as surface passivation, a method that later became critical to the semiconductor industry as it made possible the mass-production of silicon semiconductor technology, such as integrated circuit (IC) chips. For the surface passivation process, he developed the method of thermal oxidation, which was a breakthrough in silicon semiconductor technology. The surface passivation method, which substantially reduced the influence of the dangling bond that had prevented Shockley's research team from building a working FET, was presented by Atalla in 1957. Building on the surface passivation method, Atalla developed the metal–oxide–semiconductor (MOS) process, with the use of thermally oxidized silicon. He proposed that the MOS process could be used to build the first working silicon FET, which he began working on building with the help of his Korean colleague Dawon Kahng. The standard MOSFET was invented by Mohamed Atalla and Dawon Kahng in 1959.

Since then, different MOSFET layouts and their behaviour in specific applications, are being studied around the world. Recently, we have been introduced to enclosed gate layout MOSFETs. This type of MOSFET solves problems presented in high radiation environments.

This thesis mainly focuses on transistors with enclosed gate layout.

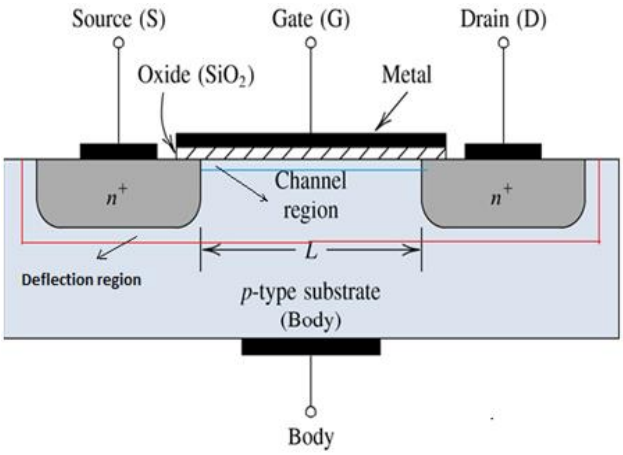
1.2 Thesis Structure

The thesis is divided into five chapters. In this chapter (the one you are reading) there is some information about the origin of the MOSFET and mentioning of the type of MOSFET that this thesis is focused on. In the second chapter, the basic MOSFETs structure and operation along with the special characteristics of MOSFETs with enclosed gate layout, will be demonstrated. In the third chapter we focus on the theory of MOSFET characteristics that later on are going to be studied in the experimental process. The fourth chapter contains the complete experimental process and it's results are presented and analyzed. In the fifth and last chapter, conclusions will be drawn.

2.Device Structure & Physical Operation

2.1 Basic MOSFET structure

A metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a field-effect transistor (FET with an insulated gate) where the voltage determines the conductivity of the device. It is used for switching or amplifying signals. In Figure 2.1 the simplified structure of an NMOSFET is depicted. The four terminals of a MOSFET are: Gate (G), Source (S), Drain (D) and Body or Bulk (B). The transistor is fabricated in a p-type substrate silicon wafer, which provides physical support for the device, and consists of two heavily doped n-type diffusion regions, indicated in the figure as n+ drain and n+ source. The dimension of the gate along the source-drain path is called length L, whereas W is the width.



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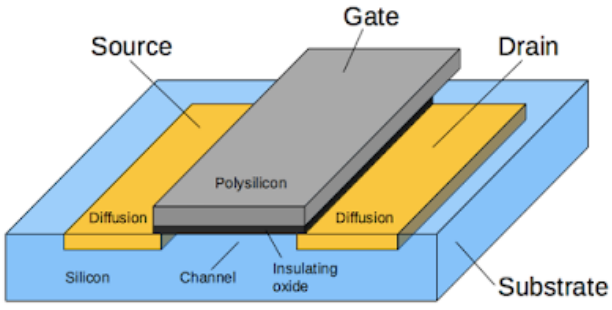
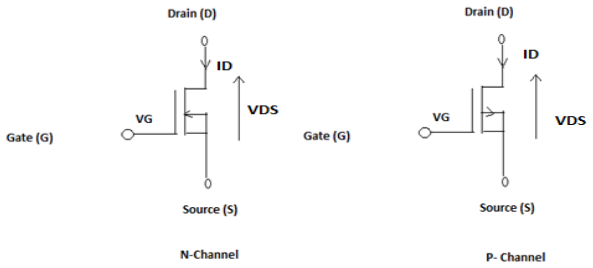


b)

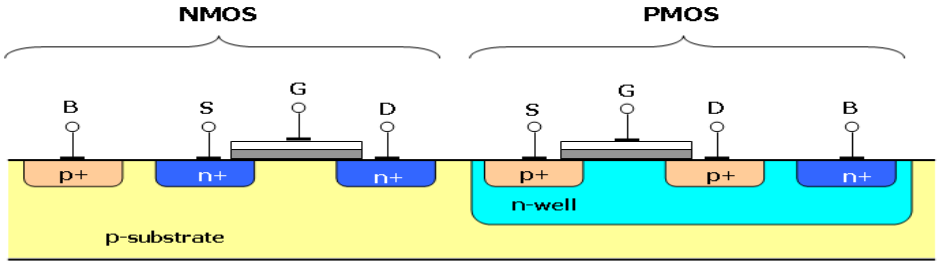
Figure 2. 1 a)Cross-Section of an n-type MOS Transistor b)3D perception of an NMOS device.

The surface between drain and source regions is covered with a thin layer of silicon dioxide (SiO2), which is an excellent electrical insulator, while a layer of polycrystalline silicon(or aluminum in older technologies) is deposited on top of the dielectric of the gate. The transistor structure is completely

symmetrical with respect to source and drain. The role is defined by terminal voltages which establish the direction of carriers flow [1, 2].
The PMOS transistor is a complementary structure to the NMOS transistor as depicted in Figure 2.2 b). P-type MOSFETs, have a similar structure with n-type MOSFETs and they are fabricated in the same substrate. They have opposite doping types, with p+ drain and p+ source diffusions placed in a local substrate called n-type 3 well. In a PMOSFET the minority carriers are the positive holes whereas in an NMOSFET the negative electrons [2].



a)



b)

Figure 2. 2 a) Circuit symbols, b) (left) Cross-Section of an NMOS device and (right) Cross-Section of a PMOS device.

The potential of the substrate that the device is fabricated influences the device characteristics. In an NMOSFET the substrate is usually connected to the most negative supply of the system, usually the ground, and the actual connection is implemented through a p+ diffusion region, as illustrated in Figure 2.3 a). The n-type local substrate of a PMOSFET is tied to the most positive supply voltage through an n+ diffusion region (Figure 2.3 b) [1]).

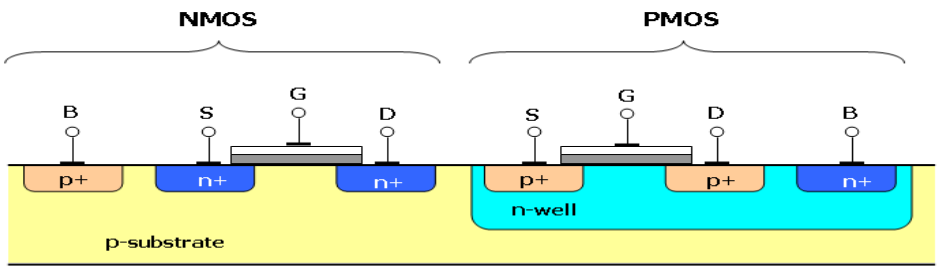


Figure 2. 3 Substrate connection of an NMOSFET and a PMOSFET.

2.2 MOSFET Operation

In the operation with zero gate voltage (VGS=0), the two back-to-back diodes formed by the pn junctions between p-type substrate and n+ drain and n+ source regions, prevent current conduction from drain to source, when a voltage VDS is applied (Figure 2.4).

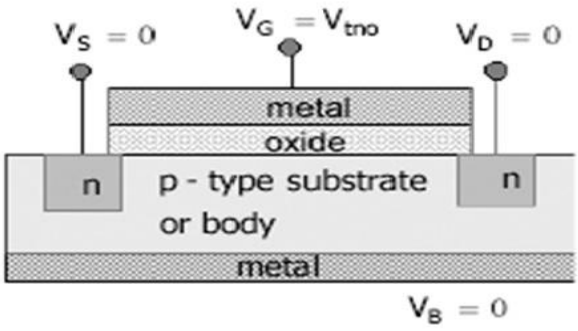


Figure 2. 4 Cross-section of an NMOSFET on zero gate voltage operation.

When gate voltage increases from zero (VGS>0), since gate and substrate form a capacitor (dielectric is SiO2), free holes are repelled from the substrate region under the gate leaving negative ions behind, thus a depletion region is formed (Figure 2.5 a)).

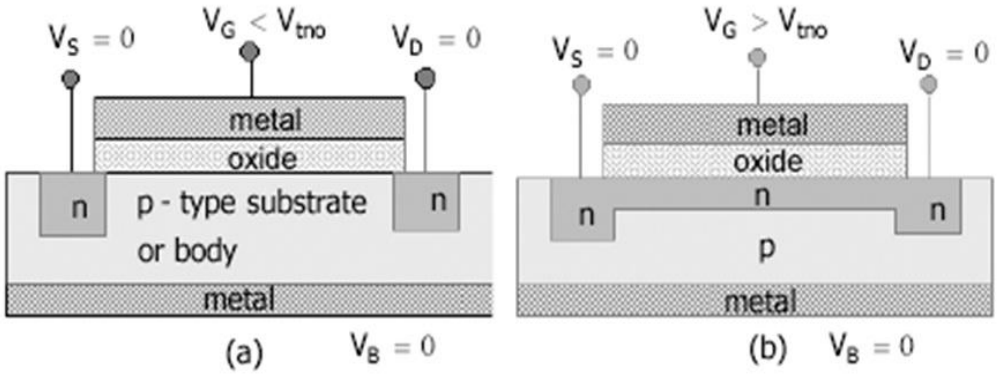


Figure 2. 5 a) Formation of depletion region and b) shaping of n-type channel.

As the gate voltage increases more, the width of the depletion region expands further and electrons are attracted from n+ drain and source areas, near the surface of the substrate under the gate oxide [2]. When the gate voltage approaches a sufficiently positive value called the threshold voltage (VGS≈VTH), an n-type channel of charge carriers, or inversion layer, is formed connecting drain and source regions. If a voltage is applied between drain and source terminals (VDS>0), current flows through this induced n-type region from drain to source (Figure 2.5 b)). For small values of the potential difference VDS, ID value increases progressively with the increase of VDS and the channel acquires a tapered shape at the drain end side (Figure 2.6 a)). The device operates in the "linear" region [1, 2]. When drain-source voltage exceeds a specific value called saturation value, VD,SAT, the depth of the channel at the drain end approaches zero, the channel is pinched-off, drain current becomes relatively constant and the device operates in the "saturation" region (Figure 2.6 b)). In this operation region the device acts as a current source under control of the gate-source voltage.

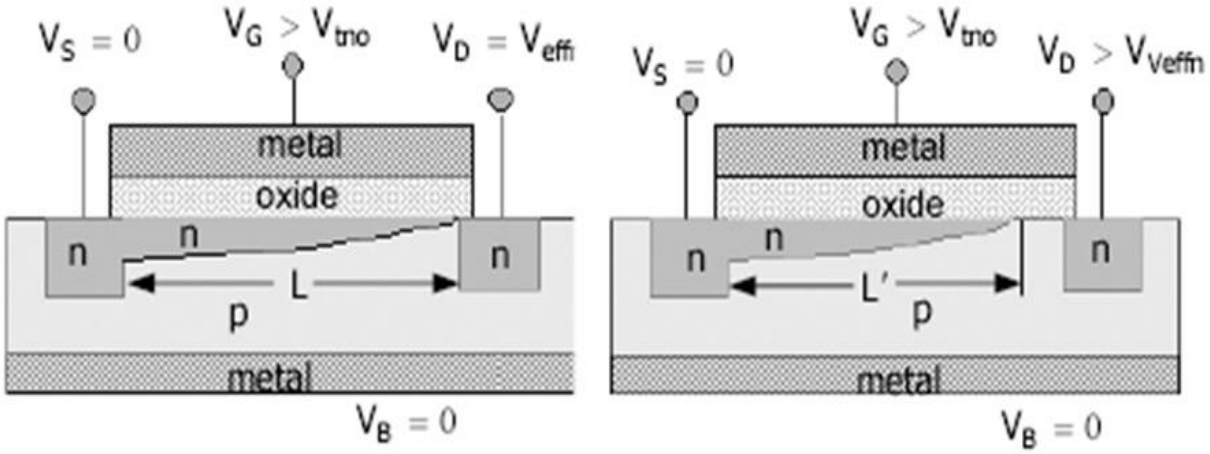


Figure 2. 6 a) Linear region of MOSFET operation and b) channel pinch-off.

So far the basic operation of an NMOS device was demonstrated. A PMOS device, follows exactly the same operational characteristics with the difference that negative gate and drain voltages must be applied [1].

2.3 Regions of inversion

As described in the previous section gate voltage is responsible of forming the inversion layer, or channel, under the gate oxide, whereas the value of drain voltage defines two regions of operation linear and saturation. Additionally, depending on the value of the gate-source voltage, the MOSFET has two distinct physical regions of operation: weak (WI) and strong (SI) inversion. Between them there is a transition region known as moderate inversion (MI) [3].
In weak inversion the channel is weakly inverted and drain diffusion current dominates. This occurs when the device is operating at sufficiently low effective gate-source voltage (VEFF=VGS-VTH≈-72mV) where the gate-source voltage is below the threshold voltage (sub-threshold region) by at least 72 mV. MOS weak inversion drain current in saturation is approximated by:

$$ID(WI,SAT) = 2n\mu Cox' UT^2 (W/L) e^{(VG - nVS - VTH/nUT)} \qquad (2.1)$$

where, n (n ≈1.4) is the substrate factor, μ is the channel carrier mobility, COX' is the gate-oxide capacitance per unit area:

$$Cox' = eSiO2 / Tox \quad (2.2)$$

and UT the thermal voltage:

$$U_T = kT/q \quad (2.3)$$

where εSiO2 = 3.45 · 10-11 F/m is the permittivity of silicon dioxide, q = 1.602 · 10-19 C is the magnitude of electron charge, Tox is the oxide thickness which is determined by the process technology used to fabricate the MOSFETs (Tox = 3.3 nm for 0.18 um CMOS technology), k = 1.3086 · 10-23 J/K is the Boltzmann's constant and UT = 25.8 mV at room temperature (T=300 K).
When the gate-source voltage exceeds the threshold voltage by at least 225 mV, the channel is strongly inverted and drift current dominates [3]. At this point the device is operating in strong inversion. Drain current for strong inversion and saturation is defined as:

$$ID(SI, SAT) = 1/2n(\mu Cox')(W/L)(VG - nVS - VTH)^2 \quad (2.4)$$

For the two different regions of inversion, weak inversion (WI) and strong (SI) inversion, the drain-source saturation voltage, VD,SAT, can be calculated from the following equations:

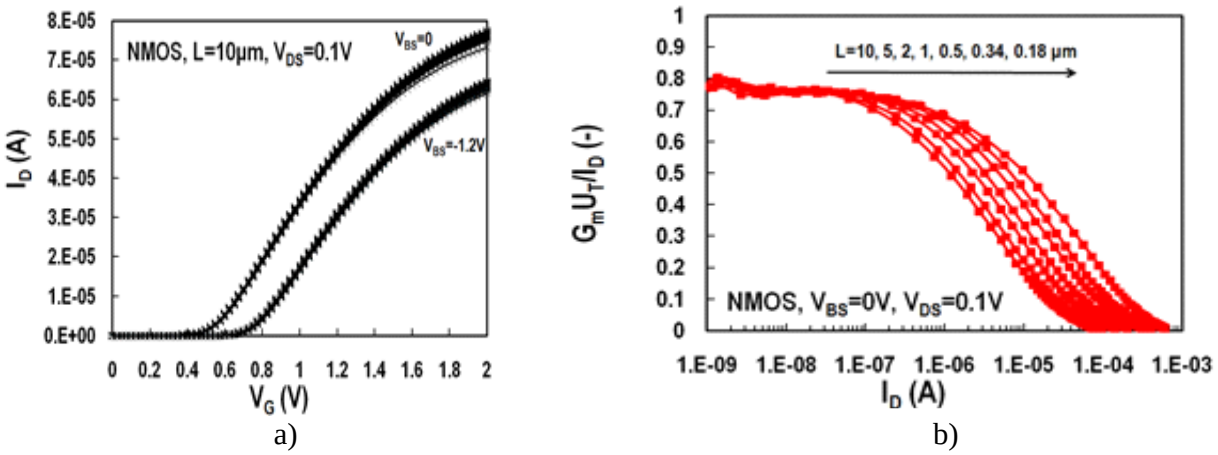
$$V_{D,SAT}(WI) = 4U_T \quad (2.5)$$

$$V_{D,SAT}(SI) = V_G - nV_S - V_{TH} \quad (2.6)$$

The drain current for both weak and strong inversion, in linear region of operation can be approximated from the following equation:

$$I_{D,LIN} \approx (\mu C_{OX}')(WL)[V_G - V_{TH} - n\,2(V_D + V_S)]\cdot(V_D - V_S) \quad (2.7)$$

The typical ID versus VG plot of a MOS device, also called transfer characteristic along with GmUT/ID versus ID plot, are presented in Figure 2.7. In weak inversion ID presents an exponential behavior.



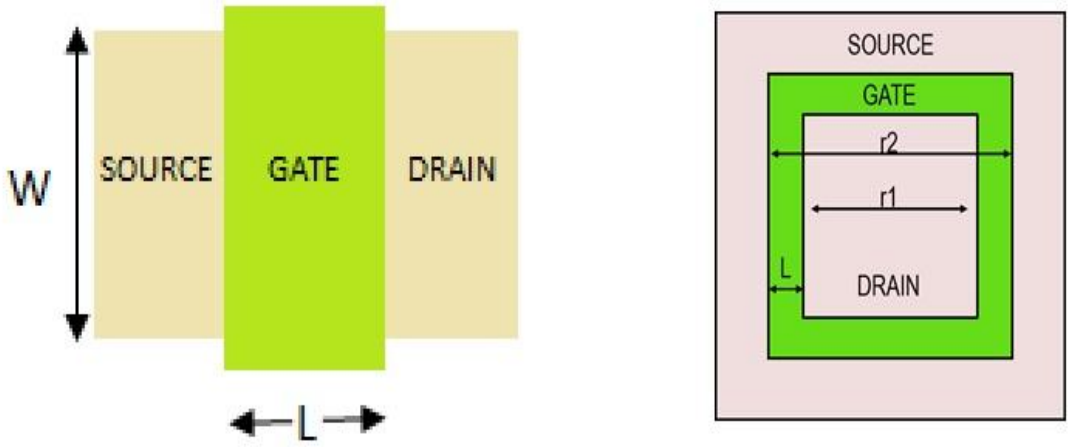
a) b)

Figure 2. 7 a) ID vs.VG transfer and b) GmUT/ID vs. ID, of an NMOS transistor from weak to strong

inversion.

2.4 MOSFETs with enclosed gate layout

CMOS integrated circuits nowadays are widely used in many areas with high requirements for radiation resistance such as high energy physics, nuclear physics, aerospace and defense industry. Furthermore, as technology nodes scale down (under 0.18um), the impact of RTS (Random Telegraph Signal) noise is becoming a crucial factor in the performance of applications like multilevel-shell flash memories, CMOS image sensors, voltage controlled oscillators(VCOs) and mixers. In this section, a MOS transistor with a radiation hard topology and less vulnerable to RTS noise, due to the absence of STI corners, will be presented. In Figure 2.8 b) the basic layout of such a device, called enclosed gate MOSFET, is illustrated.



a) b)

Figure 2. 8 a) Planar view of a standard MOSFET and b) an enclosed gate MOSFET.

In MOSFETs with enclosed gate layout the drain (or source) diffusion is fully surrounded by the gate polysilicon and the source (or drain) diffusion. The choice of the inner electrode as drain or source is defined by the bias voltage although as reported at [4] and [5] with the selection of the outer electrode as the drain, a device with an annular structure will exhibit lower drain electric fields and better reliability than a conventional one. On the other hand, if the inner electrode is selected as the drain, the substrate contact will be closer to the source and the drain resistance will be reduced resulting to higher output conductance [4]. In Figure 2.9 a cross section of an enclosed gate n-type MOSFET is depicted [6].

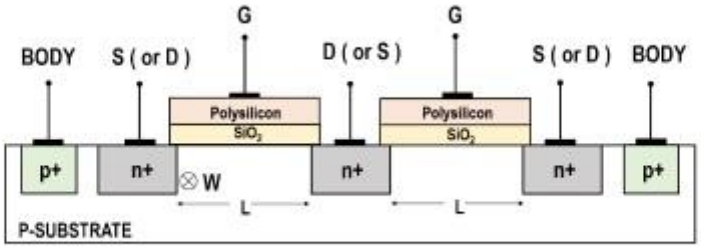


Figure 2. 9 Cross section of an enclosed gate NMOSFET with a p+ diffusion bulk connection.

Enclosed gate transistors come in a variety of different shapes. In Figure 2.10 some of the most widely used layouts like, square, circular, square with corners cut at 45o and square with 45o outer poly-edge cut, are presented [4,7]. In quarter-submicron process, due to design rules, neither circular layout nor 90o gate corners are possible to be manufactured, thus the shapes chosen are those with the 45o corners cut [4].

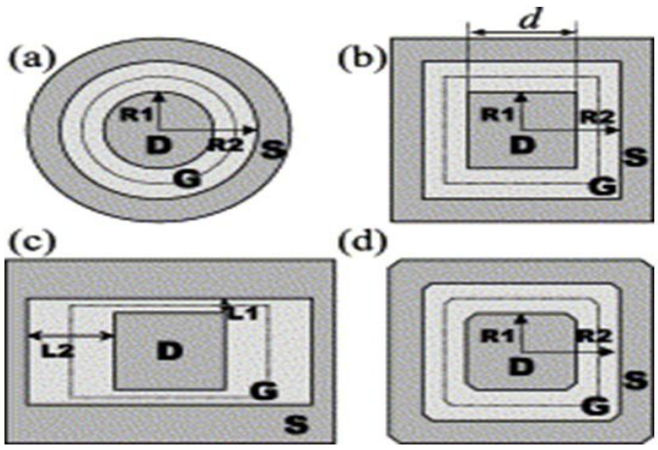
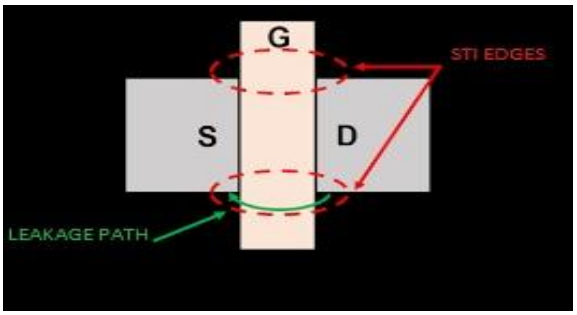


Figure 2. 10 Common enclosed gate MOSFET shapes. a)circular, b)square, c)rectangular and d) square with 45o outer poly-edge cut.

In conventional MOSFETs, techniques like STI (Shallow Trench Isolation) and LOCOS (Local Oxidation of Silicon) are used in order to provide better isolation between different devices and define the active silicon area. In radiation environments, due to positive charge trapping at the edges of STI corners (Figure 2.11b), or Bird's Beak region [8], an induced inversion layer will give rise to a transistor leakage current path from drain to source, as illustrated in Figure 2.11a). Enclosed gate MOSFETs without STI along with guard rings (Figure 2.12), can eliminate the edge leakage and



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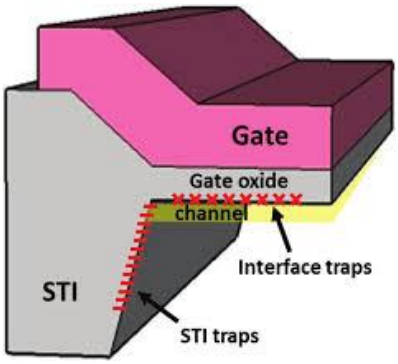

b)

Figure 2. 11 a) Current leakage path in a conventional NMOSFET with STI and b) Bird's Beak region with trapped holes.

prevent leakage current between components. This can be realized because any current between source and drain has to flow underneath the gate oxide and there is no possible current path along the edge of the active area [7]. Additionally RTS noise, which is related to trapping sites within the gate oxide-silicon interface due to structural defects, can be affected by the presence of shallow trench isolation. During the STI process, the device

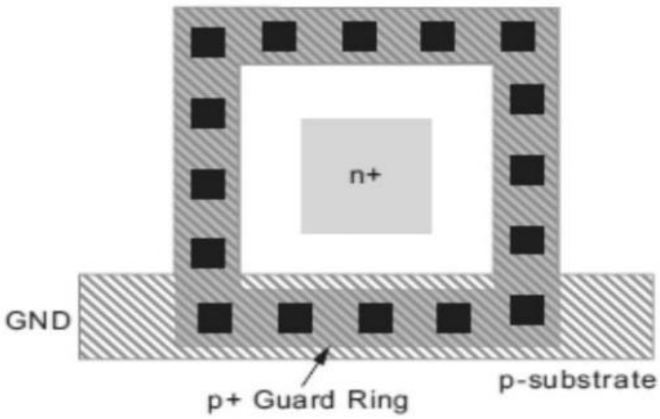

Figure 2. 12 Square NMOSFET with 45₀ outer poly-edge cut, p+ guard rings and polysilicon gate extension.

can be damaged at the STI boundary resulting to the generation of extra traps at the edge of the channel under the gate region [8]. As the device dimensions scales down the ratio of device gate edge to area increases and the STI edge effect dominates the overall RTS performance [9]. Since low frequency noise is strongly related to RTS noise, as will examined in detail in Chapter 3, devices without STI, like enclosed gate transistors, are expected to exhibit greatly improved 1/f noise characteristics like lower drain current PSDs and lower relative current variations (ΔID/ID) [10].

2.5 Modeling the W/L ratio in enclosed gate MOSFETs

Unlike the conventional MOSFETs in transistors with enclosed gate geometries the definition of the

aspect ratio W/L, is not trivial. The extraction of the W/L values comes from the comparison of the ID-VGS characteristics between enclosed and standard devices with the same gate length (L) [4]. For rectangular and square layouts, due to the distribution of the electric field in the corners of the gate, the transistor must be divided into smaller parts with the use of conformal mapping technique. These parts can be considered as smaller transistors contributing accordingly to the drain current of the MOSFET. Figure 2.13 shows the decomposition of a broken corner square and a square MOSFET into smaller transistors with 3 different basic shapes. Trapezium 1 is the approximation of the edge transistor, trapezium 2 corresponds to the corner transistor and rectangle 3 is used to model the 45o edge cuts in the case of broken square corner MOSFET. The effective W/L ratio of a square MOSFET can be calculated from the equation [11]:

$$\left(\frac{W}{L}\right)_{eff} = 4\,\frac{2a}{\ln\left(d'/d'-2aL_{eff}\right)} + 2K\,\frac{1-a}{\frac{1}{2}\ln\frac{1}{a}\sqrt{a^2+2a+5}} + 3\,\frac{(d-d')/2}{L_{eff}} \qquad (2.7)$$

where d'=d-c√2 and a is a fitting parameter which is needed to identify the borders between transistors 1 and 2. For different CMOS technologies scaling from 2.5um to 0.25 um, a has been found to be almost technology independent with a value of 0.05. Parameter K is geometry dependent with a value of 7/2 for devices with L≤ 0.5um and 4 for longer devices [4, 11].

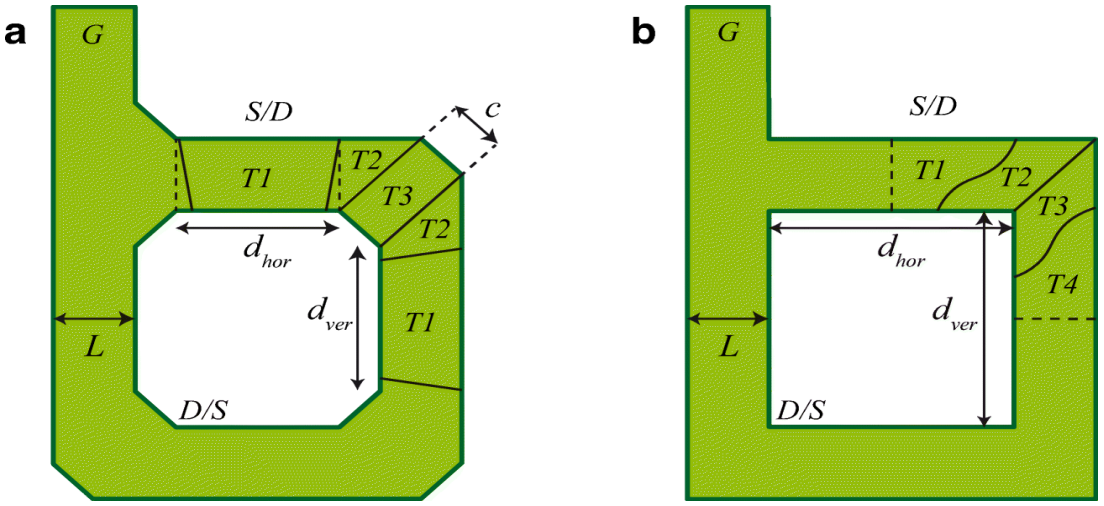

Figure 2. 13 a) Square and b) broken corner square MOSFET formed by different types of transistors in parallel.

Under the same approach, the aspect ratio of the square layout is given by [4]:

$$\left(\frac{W}{L}\right)_{eff} = 4 \cdot 2\left(\frac{a}{\ln(d/d-2aL_{eff})} + \frac{1}{\frac{1}{2}\sqrt{a^2+2a+5}} - \frac{(1-a)}{-\ln a}\right) \qquad (2.8)$$

Again a=0.05 can be chosen to assure a good W/L predictability. It should be noticed that the only way to achieve lower aspect ratios is to increase L and keep d constant. Therefore, transistors with enclosed gate layouts, cannot have aspect ratios lower than a certain value [4, 11].
For enclosed gate MOSFETs with circular geometry the effective W/L ratio can be approximated by

the following equation:

$$(W/L)_{eff,CIRC} = 2\pi/\ln(R2/R1) \quad (2.9)$$

where R1 is the inner diffusion radius and R2=L+R1. In this case if the drain radius is greater than the channel length (L<< R1) the above equation gives a very good approximation of the effective W/L ratio whereas for long channel devices overestimates the result [4].

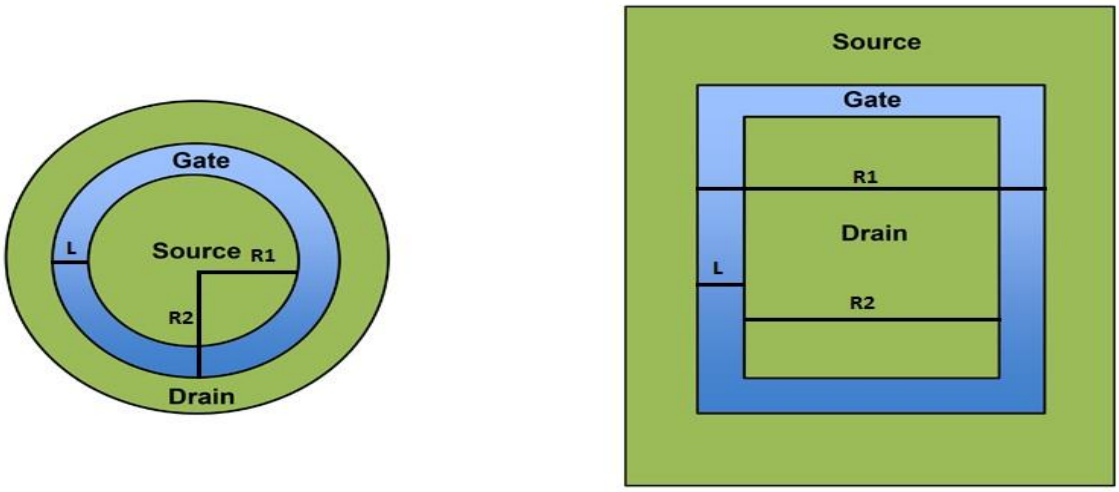

Figure 2. 14 a) Circular and b) square with 45o outer poly-edge cut MOSFETs.

For square transistors with 45o outer polysilicon-edge cut (Figure2.10b), a more compact approach of the effective W/L ratio is given by:

$$(W/L)_{eff,OUTERCUT} = 8/\ln(R2/R1) \quad (2.10)$$

where R1 is the inner diffusion length, L is the channel length and R2=R1+L [7].
As mentioned above, transistors with enclosed gate layout, can prevent current leakage in irradiated circuits and exhibit improved low frequency noise characteristics. However, drawbacks like: consumption of area, limitations in the choice of the W/L ratio, and difficulties in modeling the W/L ratio should be mentioned.

3.MOSFET electrical characteristics

In this chapter, we are going to study MOSFET characteristics that were not mentioned in the "Device Structure & Physical Operation" chapter and are going to be examined in the experimental process.

3.1MOSFET Transconductance

Transconductance (for transfer conductance), also infrequently called mutual conductance, is the electrical characteristic relating the current through the output of a device to the voltage across the input of a device. Conductance is the reciprocal of resistance[12].
Now let's take a closer look at the MOSFET transconductace, given by the following equation:

$$g_m=k'_n(W/L)(V_{GS}-V_t)=k'_n(W/L)V_{OV} \quad (3.1)$$

This relationship indicates that *gm* is proportional to the process transconductance parameter $k'_n = \mu_n C_{0X}$ and to the *W/L* ratio of the MOS transistor; hence to obtain relatively large transconductance the device must be short and wide. We also observe that for a given device the transconductance is proportional to the overdrive voltage, $Vov = V_{GS} - V_t$, the amount by which the bias voltage *VGS* exceeds the threshold voltage *Vt.* Note, however, that increasing *gm* by biasing the device at a larger V_{GS} has the disadvantage of reducing the allowable voltage signal swing at the drain.
Another useful expression for g_m can be obtained by substituting for $(V_{GS} - V,)$ in Eq. (3.1) by $\sqrt{2ID/(k'n(W/L))}$

$$gm\sqrt{2k'_n}\sqrt{W/L}\sqrt{I_D} \quad (3.2)$$

This expression shows that:
1. For a given MOSFET, g_m is proportional to the square root of the dc bias current.
2. At a given bias current, g_m is proportional to $\sqrt{W/L}$.
In contrast, the transconductance of the bipolar junction transistor (BJT) is proportional to the bias current and is independent of the physical size and geometry of the device.
To gain some insight into the values of g_m obtained in MOSFETs consider an integrated circuit device operating at I_D = 0.5 mA and having k'_n = 120 mA/V^2. Equation (3.2) shows that for *W/L* = 1, g_m = 0.35 mA/V, whereas a device for which *W/L =100* has g_m = 3.5 mA/V. In contrast, a BJT operating at a collector current of 0.5 mA has g_m = 20 mA/V.
Yet another useful expression for g_m of the MOSFET can be obtained by substituting for $k'_n(W/L)$ in Eq. (3.1) by $2I_D/(V_{GS} – V_t)^2$:

$$g_m=2ID/(V_{GS}-V_t)=2I_D/V_{OV} \quad (3.3)$$

In summary, there are three different relationships for determining g_m—Eqs. (3.1), (3.2), and (3.3) and there are three design parameters *(W/L), Vov,* and 1_D, any two of which can be chosen independently. That is, the designer may choose to operate the MOSFET with a certain overdrive voltage *Vov* and at a particular current I_D; the required *W/L* ratio can then be found and the resulting g_m determined.

In the following graph there is an example of the G_m behavior for different V_G and channel lengths.

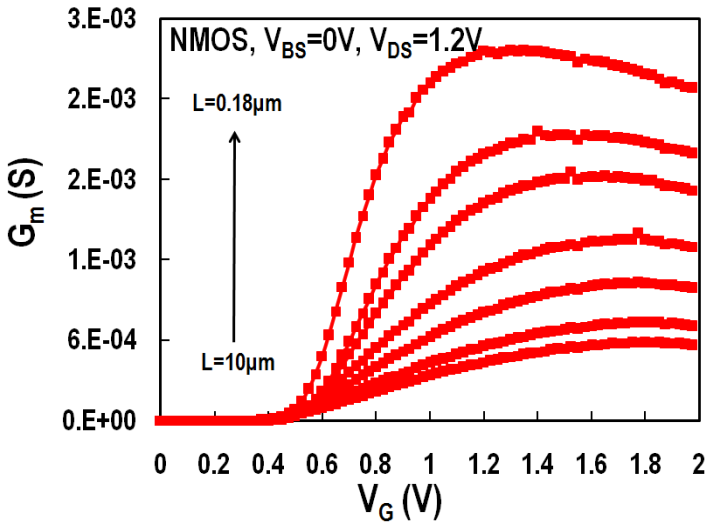

Figure 3. 1 Example of Gm vs VG graph

3.2 Mobility

In solid-state physics, the electron mobility characterizes how quickly an electron can move through a metal or semiconductor, when pulled by an electric field. There is an analogous quantity for holes, called hole mobility. The term carrier mobility refers in general to both electron and hole mobility[12].

Electron and hole mobility are special cases of electrical mobility of charged particles in a fluid under an applied electric field.

When an electric field *E* is applied across a piece of material, the electrons respond by moving with an average velocity called the drift velocity ud. Then the electron mobility μ is defined as: $u_d=\mu E$

The three major scattering mechanisms that inuence mobility are Coulomb, phonon and surface-roughness scattering; thus, the channel mobility can be calculated from:

$$1/\mu = 1/\mu_c + 1/\mu_{ph} + 1/\mu_{sr}$$

In the following graph there is an example of the mobility behavior for different V_{BS} and channel lengths.

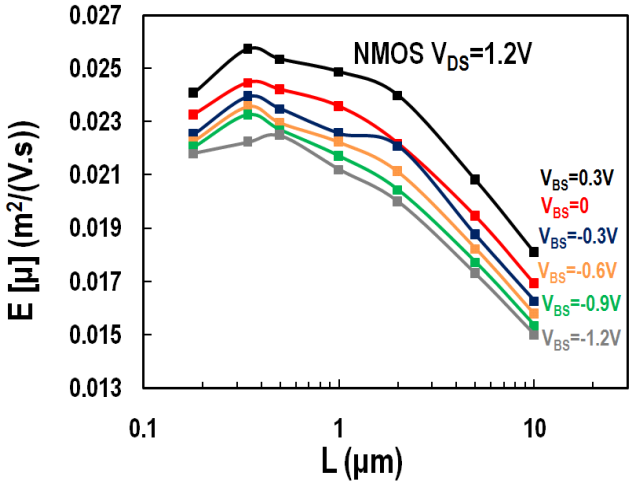

Figure 3. 2 Example of μ vs L graph

3.3 Slope Factor

One important parameter for the characterization of MOS transistors is the slope factor. The "ideal" slope factor is equal to one [13]. The slope can be derived by the following rule:

$$n \equiv \left[\frac{\partial \Psi_{SP}}{\partial V_G}\right]^{-1} = 1 + \frac{\gamma}{2\sqrt{\Psi_{SP}}} \cong 1 + \frac{\gamma}{2\sqrt{\Psi_0 + V_P}}$$

The following graph shows an example of the behavior of the slope factor for different V_{BS} and channel length.

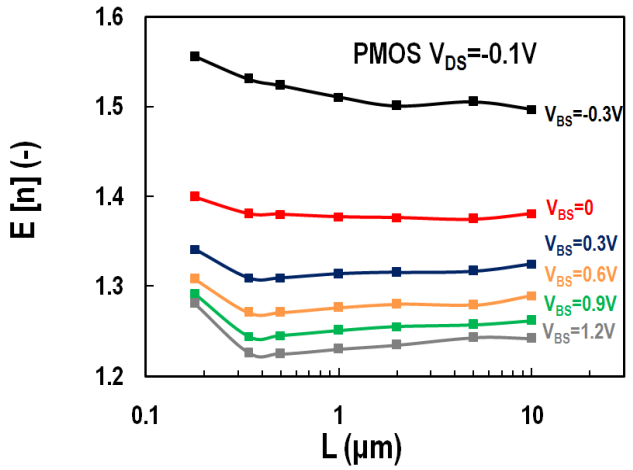

Figure 3. 3 n vs L example for various V_{BS}

3.4 Matching

MOS transistor matching is an important design parameter in many CMOS applications. MOS transistor matching in analog CMOS applications deals with statistical device differences between pairs of identically designed and identically used transistors[14]. In analog circuit blocks, like A/D converters, threshold voltage differences of millivolts or less can determine the performance and/or yield of a product[15].

There are 8 principles to achieve optimal matching:
Principle 1: Same structure
Principle 2: Same temperature
Principle 3: Same geometry
Principle 4: Proximity (minimum distance)
Principle 5: Same Symmetry center
Principle 6: Same orientation
Principle 7: Same environment
Principle 8: Non-minimum geometry

In the following graph there is an example of the threshold voltage matching behavior for different channel lengths.

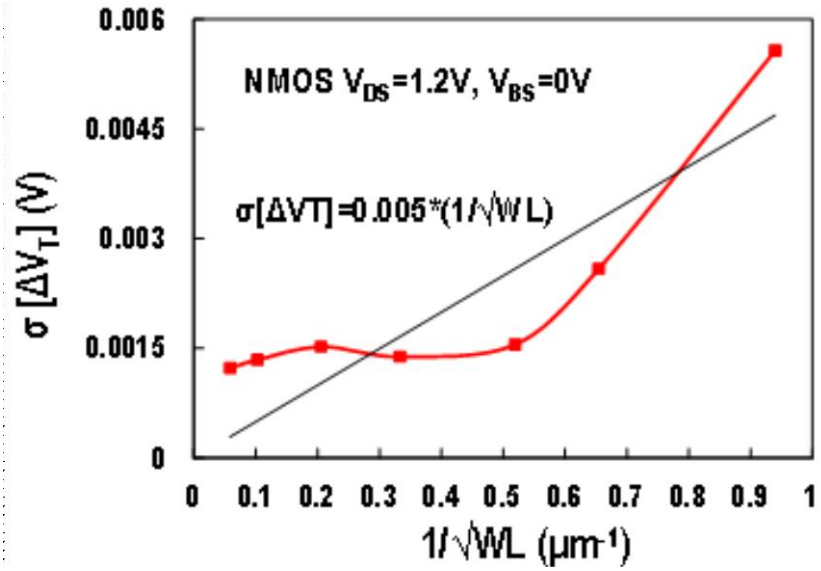

Figure 3. 4 Example of Threshold Voltage Matching

4. Experimental process

In the experimental process, data was gathered from a total of 672 circular NMOS transistors. For each of the 48 dies measured on the wafer, there were seven pairs of NMOS Circular Transistors (10um, 5um, 2um, 1um, 0.5um, 0.34um and 0.18um pairs).

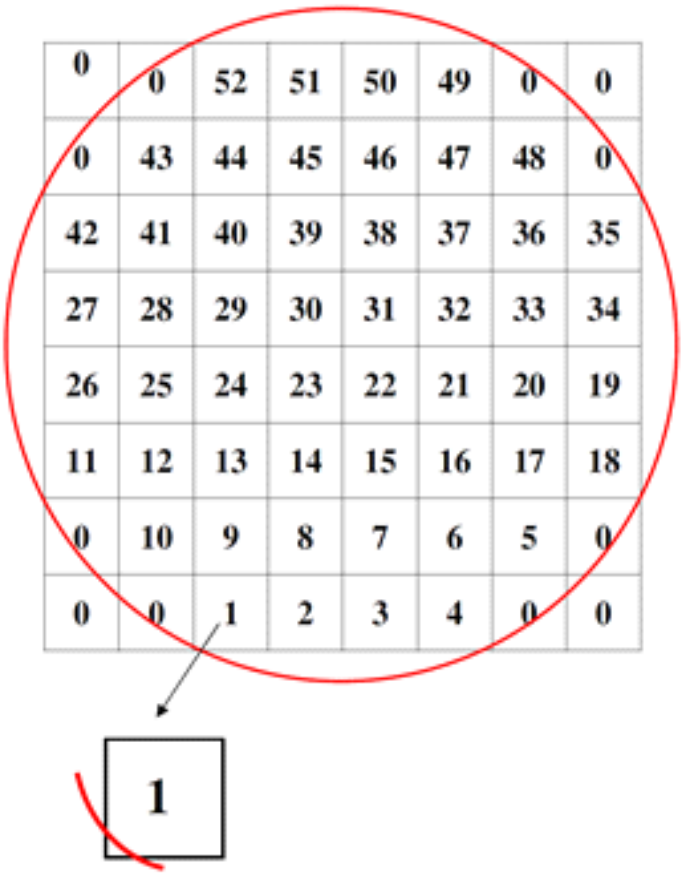

Figure 4. 1 Representation of the silicon wafer's dies

Figure 4. 2 The MOSFETs included in each die ("SPECIAL" MOSFETs were not included in the experimental process)

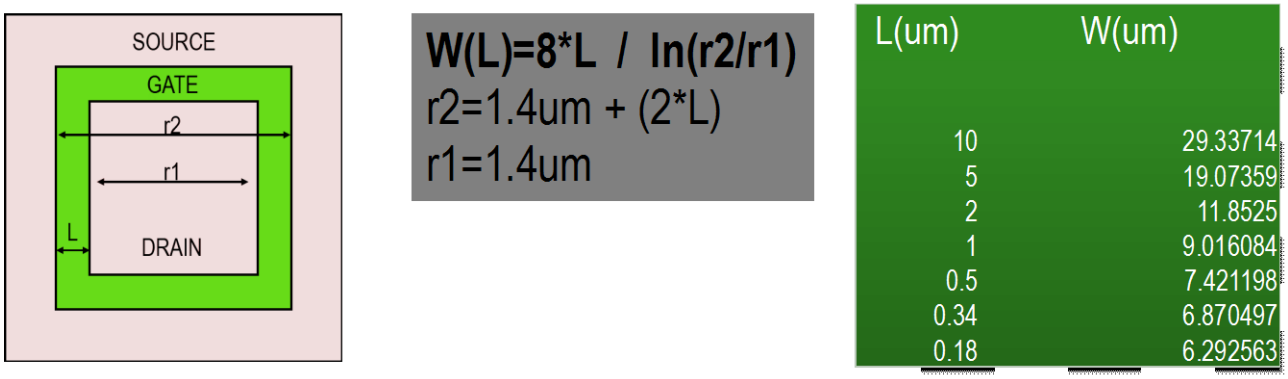

Figure 4. 3 W and L and their dependence, for every type of the measured transistors

4.1 Measurements for V_{DS}=0.1 V (linear region)

In this part of the thesis we will see the graphic representation of the MOSFET characteristics, while the drain-source voltage equals 0.1V.

4.1.1 Measured I/V characteristics

In this section, the measured ID vs. VG plots will be presented. The |ID| for every gate voltage value, represents the mean value of the measured drain current (|ID|), on a number of 96 NMOSFETs on the same gate voltage. The unitless quantity GmU_T/I_D is also calculated from the average Gm value that was extracted from measurements.

Measurements – V_{DS}=0.1V (Lin axis)

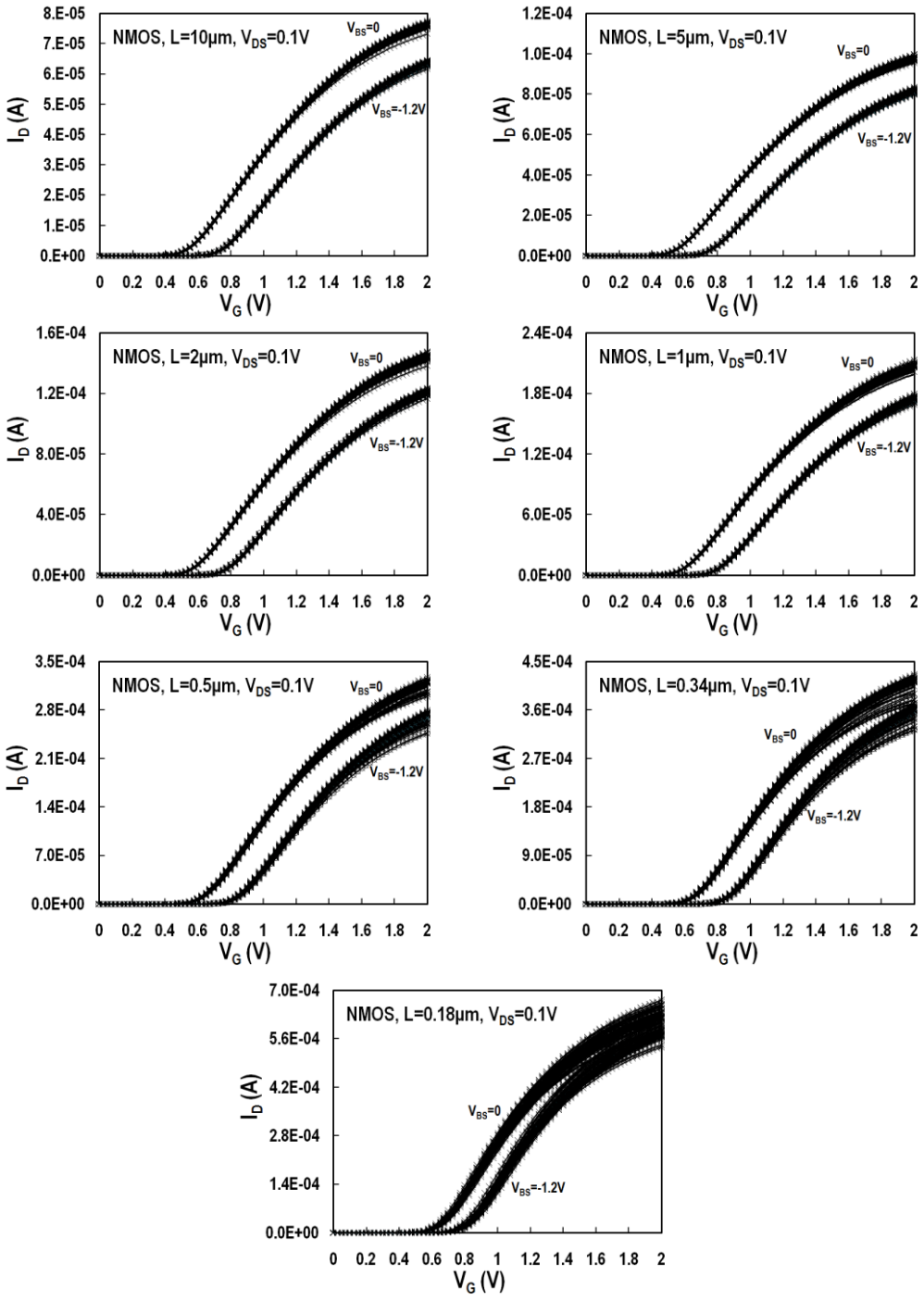

Figure 4. 4 The I_D vs V_G graphs for V_{BS}=0, -1.2 V. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um)

In the figure above we see that I_D increases when we increase the gate Voltage (as expected). Also, I_D is higher for V_{BS} = 0V than it is for V_{BS} = -1.2V. This behavior is normal and similar to standard transistors.

Measurements – V_{DS}=0.1V (Log axis)

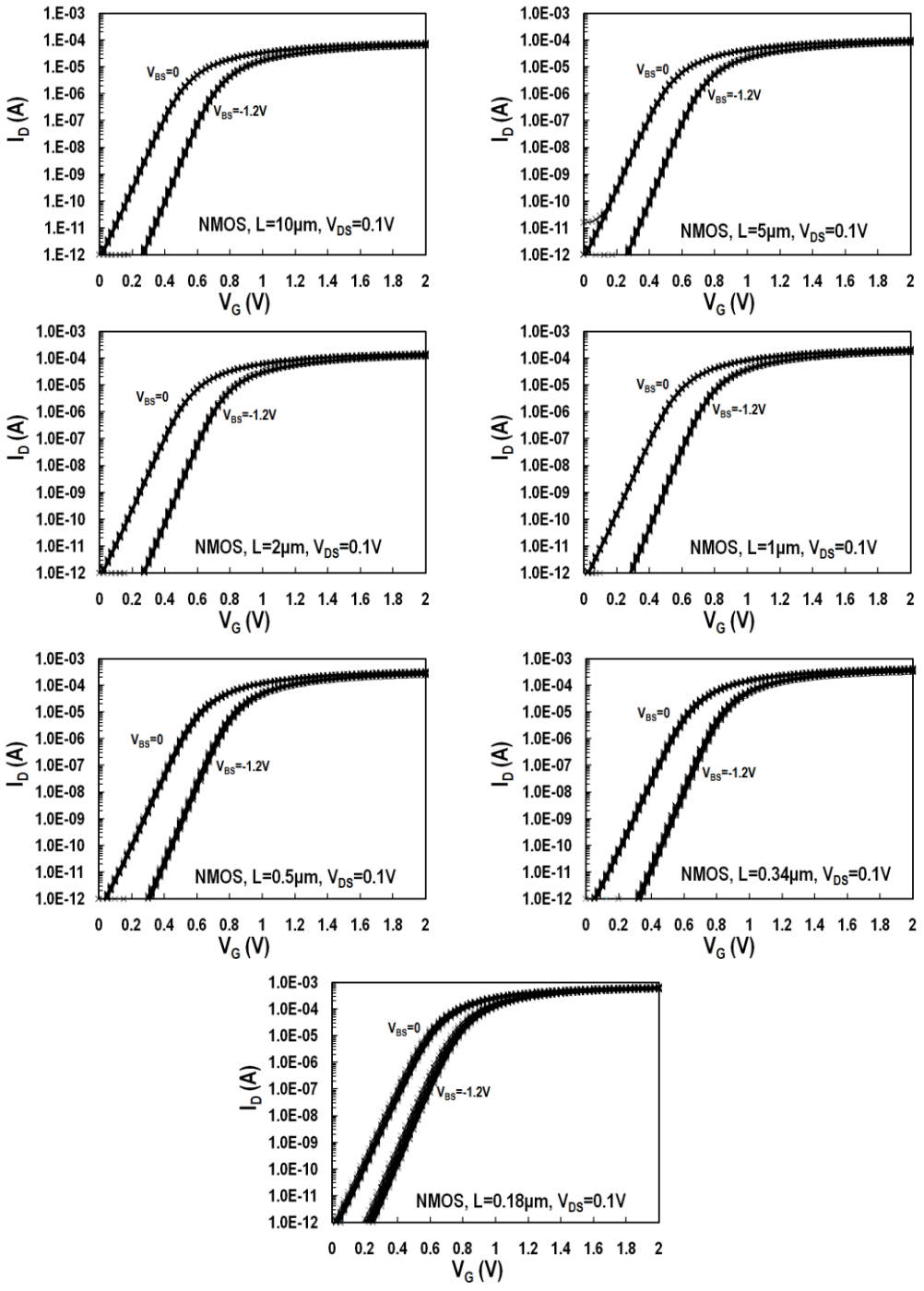

Figure 4. 5 The I_D vs V_G graphs for V_{BS}=0, -1.2 V in a logarithmic axis. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um)

gm (V_{DS}=0.1V) – Mean Value

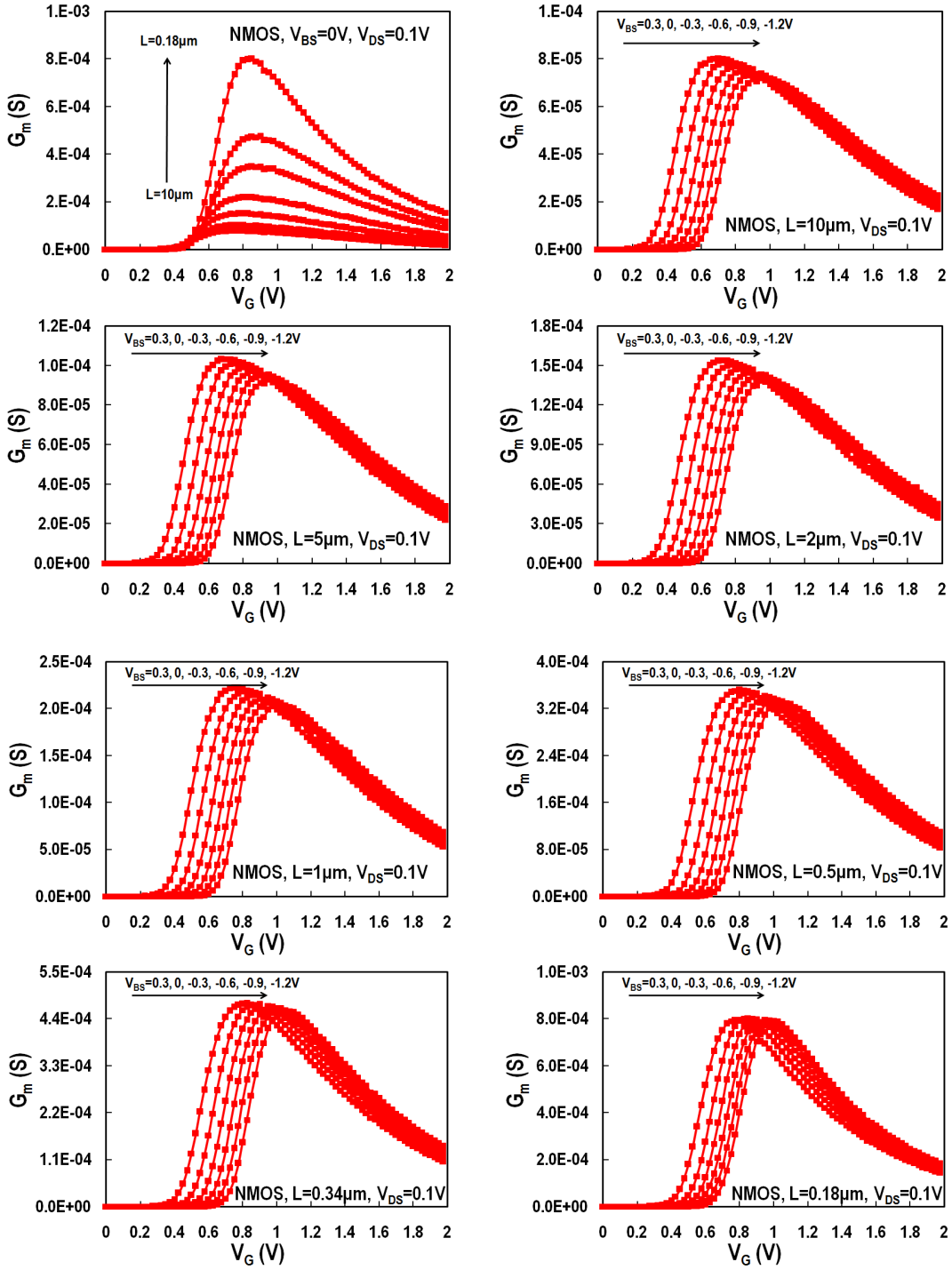

Figure 4. 6 G_m vs V_g graphs for V_{BS} =0.3, 0, -0.3, -0.6, -0.9, -1.2V are presented. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um) except for the top left graph which presents the result of all the different channel lengths when V_{BS} equals 0.

In the graphs above, we can clearly see that as the channel length gets smaller, the transconductance increases. Another observation is that G_m's peak increases with higher V_{BS}. This is the expected result which is similar to the result of the standard version of these transistors.

gmUT/ID (V_{DS}=0.1V) – Mean Value

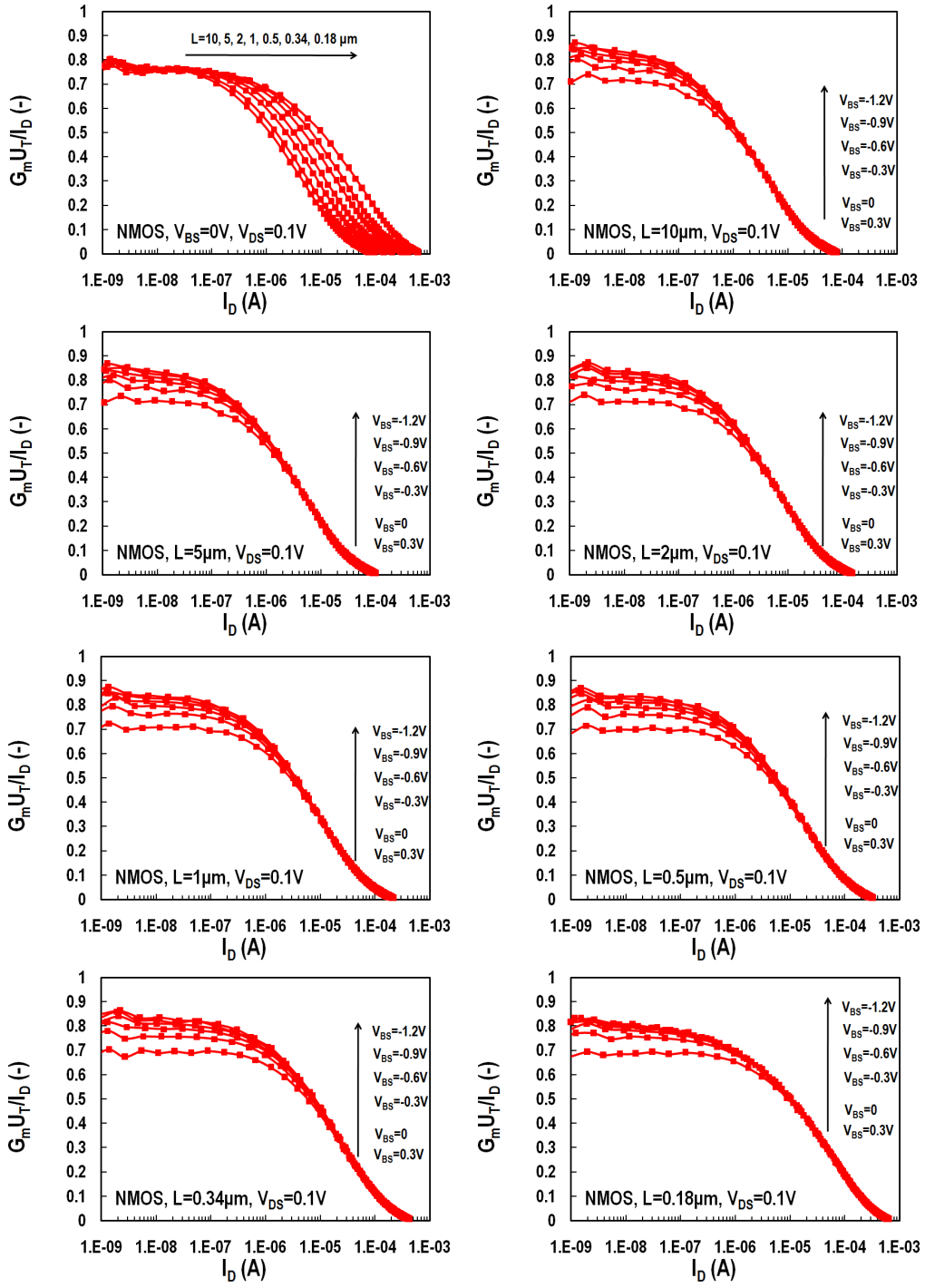

Figure 4. 7 The G_mU_T/I_D graphs for V_{BS} =0.3, 0, -0.3, -0.6, -0.9, -1.2V are presented. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um) except for the top left graph which presents the results of all the different channel lengths for V_{BS} = 0.

The unitless quantity G_mU_T/I_D is clearly higher for lower current I_D. It also appears to be higher for lower V_{BS}.

4.1.2 Threshold Voltage

In this section the threshold voltage graphs will be presented. The mean value of the threshold voltage, the threshold voltage in specific cases and it's standard deviation will be the subject of this subchapter.

V_{TH} – Mean Value

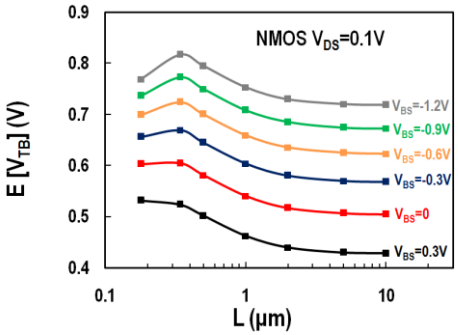

Figure 4. 8 The E[V_{TB}] vs L graph for V_{BS} =0.3, 0, -0.3, -0.6, -0.9, -1.2V is presented above.

E[V_{TB}] peaks for 180nm when V_{BS}= 0, 0.3V and drops while the channel length gets bigger. When V_{BS}=-0.3, -0.6, -0.9, -1.2V, E[V_{TB}] peaks for 340nm (the second lowest channel length) and then starts to drop while the channel length get bigger. Also, E[V_{TB}] increases while V_{BS} decreases.

V_{TH}

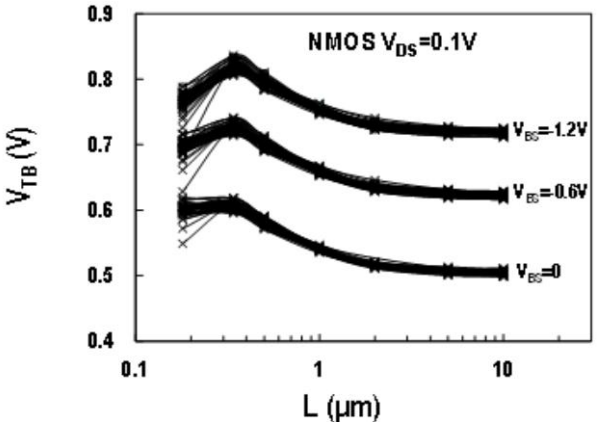

Figure 4. 9 V_{TB} vs L graph is presented. V_{DS} is 0.1 Volts and V_{BS}= -1.2, -0.6 and 0.

V_{TB} peaks for 180nm when V_{BS}= 0V and drops while the channel lengths gets higher. When V_{BS}=-0.6, -1.2V, V_{TB} peaks for 340nm (the second lowest channel length) and then starts to drop while the channel lengths get bigger.

V_{TH} – Sigma

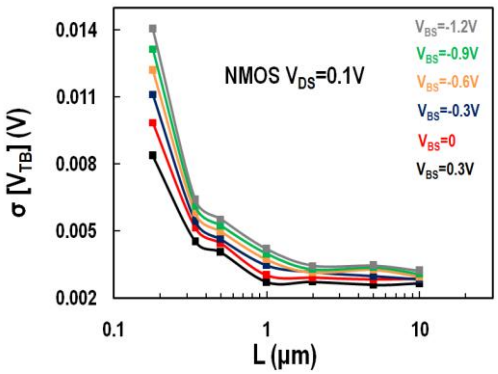

Figure 4. 10 σ[V_{TB}] vs L graph is presented for V_{BS} =0.3, 0, -0.3, -0.6, -0.9, -1.2V

The standard deviation of V_{TB} is significantly bigger for 180nm. While the channel length increases, the V_{TB} standard deviation decreases. Another conclusion made after examining the graph above, is that σ[V_{TB}] is lower for higher V_{BS}.

4.1.3 Threshold Voltage Matching

The Threshold Voltage will be our focus in this part of the thesis. Results from 48 pairs of NMOS transistors for each channel length, will be presented in the graphs below.

ΔV_{TH} – Matching (VDS=0.1V)

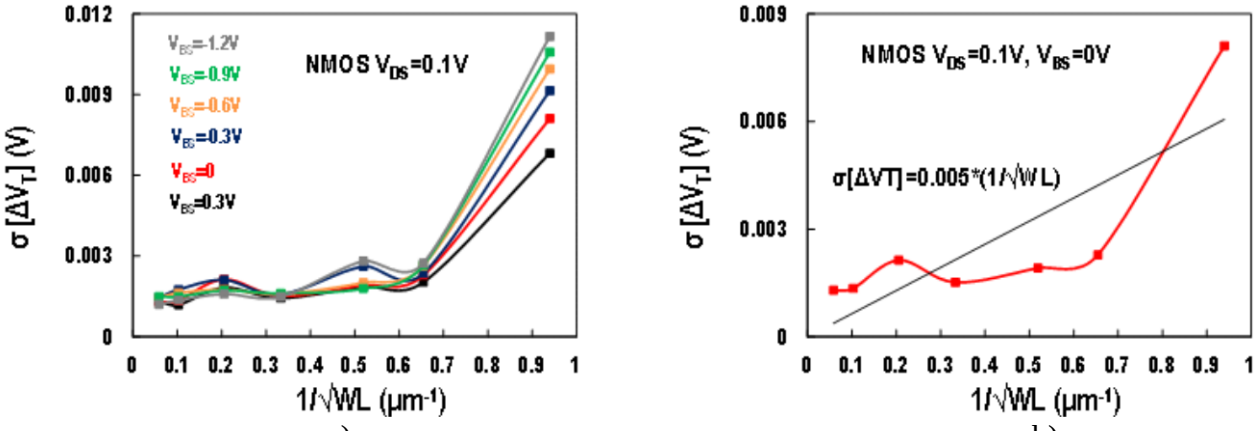

Figure 4. 11 The σ[ΔV_T] vs 1/ $\sqrt{WL}$ graph for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V is presented in a). In b) we examine V_{BS} =0 exclusively.

Examining the figure above we can conclude that σ[ΔV_T] increases with $1/\sqrt{WL}$. This makes sense because as the product of the width and the length decreases, the unitless quantity $1/\sqrt{WL}$ increases and for smaller dimensions where the distance between the different semiconductors is smaller, we expect increased deviation between the measurements.

4.1.4 Mobility

The mean value of the mobility for every channel length, the mobility for specific V_{BS} and it's standard deviation will be our focus in this subchapter. Representative graphs and their results will be presented below.

μ – Mean Value

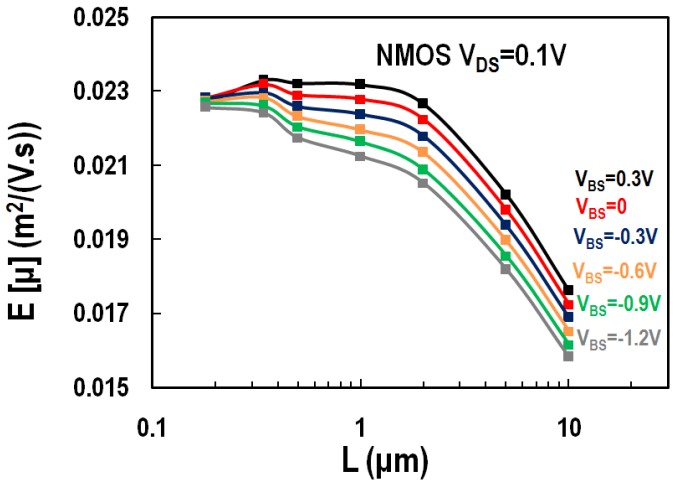

Figure 4. 12 E[μ] vs L graph for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V

The mean value of the mobility decreases with bigger channel length and lower V_{BS}, following typical behavior.

μ – Mobility

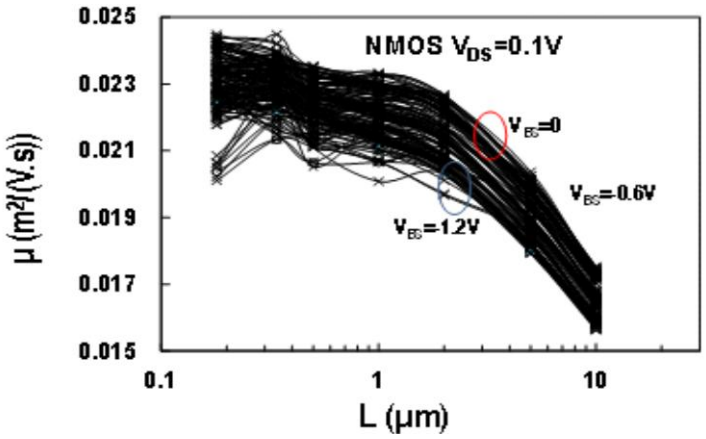

Figure 4. 13 μ vs L graph for V_{BS} = 0, -0.6, -1.2V

Mobility decreases for bigger channel length. It also decreases for lower V_{BS}. Furthermore, mobility becomes bigger for smaller channel length devices, following typical behavior.

μ – Sigma

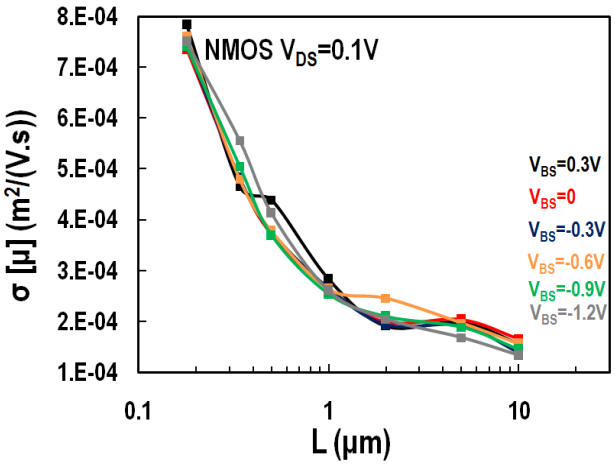

Figure 4. 14 σ[μ] vs L graph for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V

The standard deviation of μ, is higher for smaller channel lengths. This is something we expect since, as we already know, the electron mobility is inversely proportional to the channel length

4.1.5 Slope Factor

In this part of the thesis we are going to focus on the slope factor and it's behavior for transistors with different channel length and for different base-source voltages in each of them.

n – Mean Value

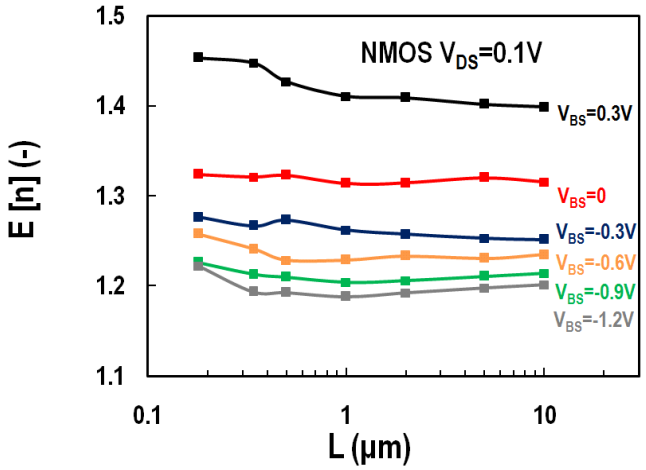

Figure 4. 15 E[n] vs L graph for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V

In the figure above we can examine the mean value of slope factor.

n

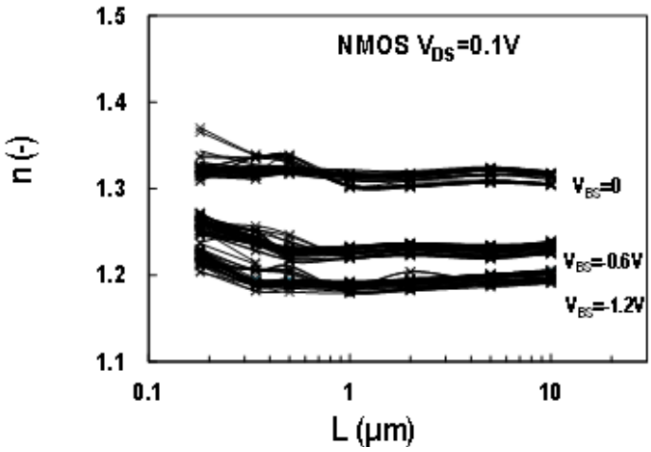

Figure 4. 16 n vs L graph for V_{BS} = 0, -0.6, -1.2V

The graph above presents how the slope factor behaves for VBS=0, -0.6, -1.2V. The slope factor increases with higher V_{BS}. It can be noticed that slope factor increases at higher VBS. Furthermore, slope factor versus channel length is almost constant with a slight increment towards smaller channel lengths as expected.

n – Sigma

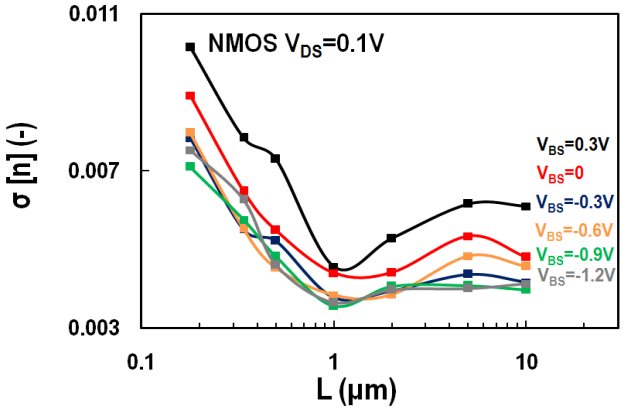

Figure 4. 17 σ vs L graph for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V

Standard deviation of n, increases with higher V_{BS} and towards minimum channel length. Similar results are extracted from respective standard transistors.

σ(ΔID/ID) – Matching (V_{DS}=0.1V)

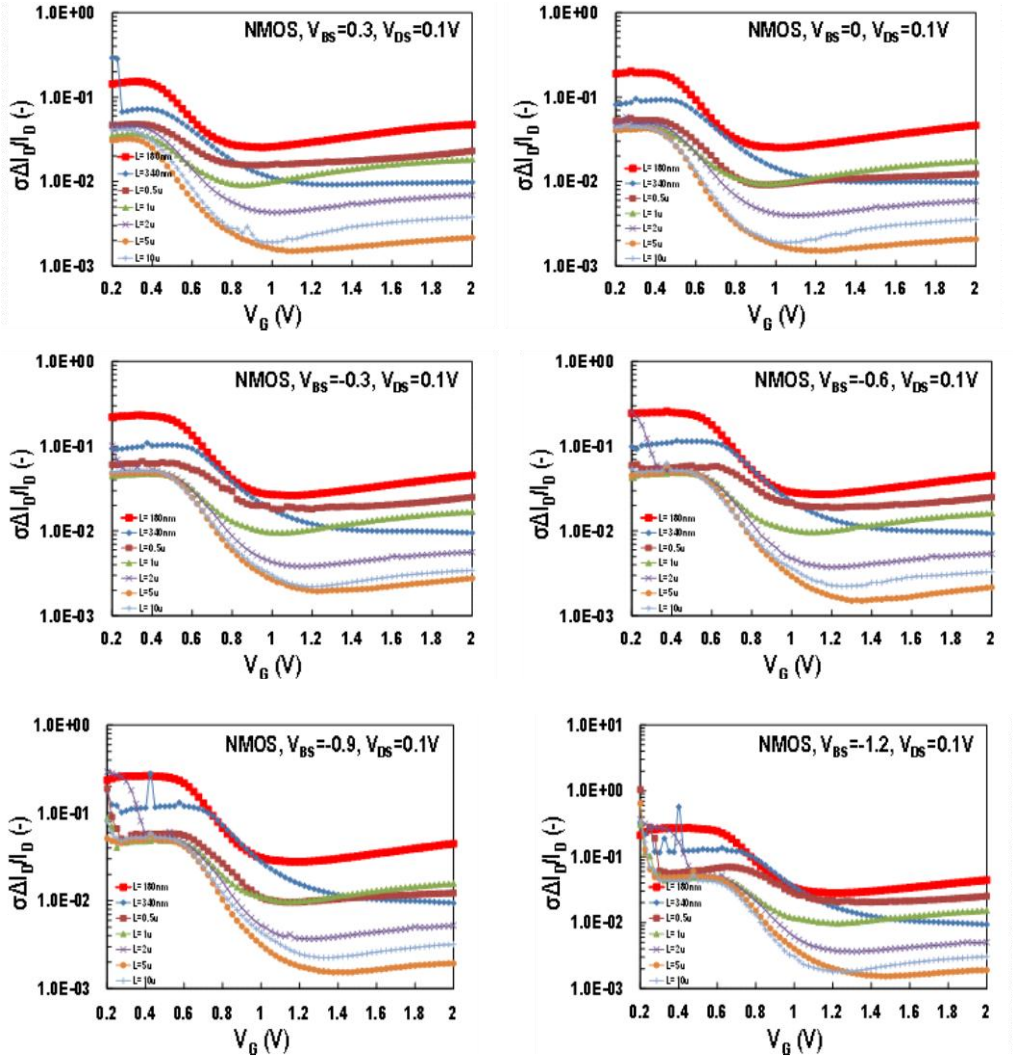

Figure 4. 18 σ(ΔID/ID) vs VG graphs for L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um. Each graph shows the results for different V_{BS} =0.3, 0, -0.3, -0.6, -0.9, -1.2V.

Drain current mismatch σ(ΔID/ID) decreases for bigger channel length L and becomes higher towards weak inversion. This is an expected behavior, since current mismatch is expected to follow the gm/ID behavior versus inversion coefficient.

4.2 Measurements for V_{DS}=1.2 V (saturation region)

In this part of the thesis we will examine the graphic representation of the MOSFET characteristics, while the drain-source voltage equals 1.2V.

4.2.1 Measured I/V characteristics

In this section the measured ID vs. VG plots will be presented. The |ID| for every gate voltage value,

represents the mean value of the measured drain current (|ID|), on a number of 96 NMOSFETs on the same gate voltage. The unitless quantity GmUT/ID is also calculated from the average Gm value that was extracted from measurements.

Measurements – V_{DS}=1.2V (Lin axis)

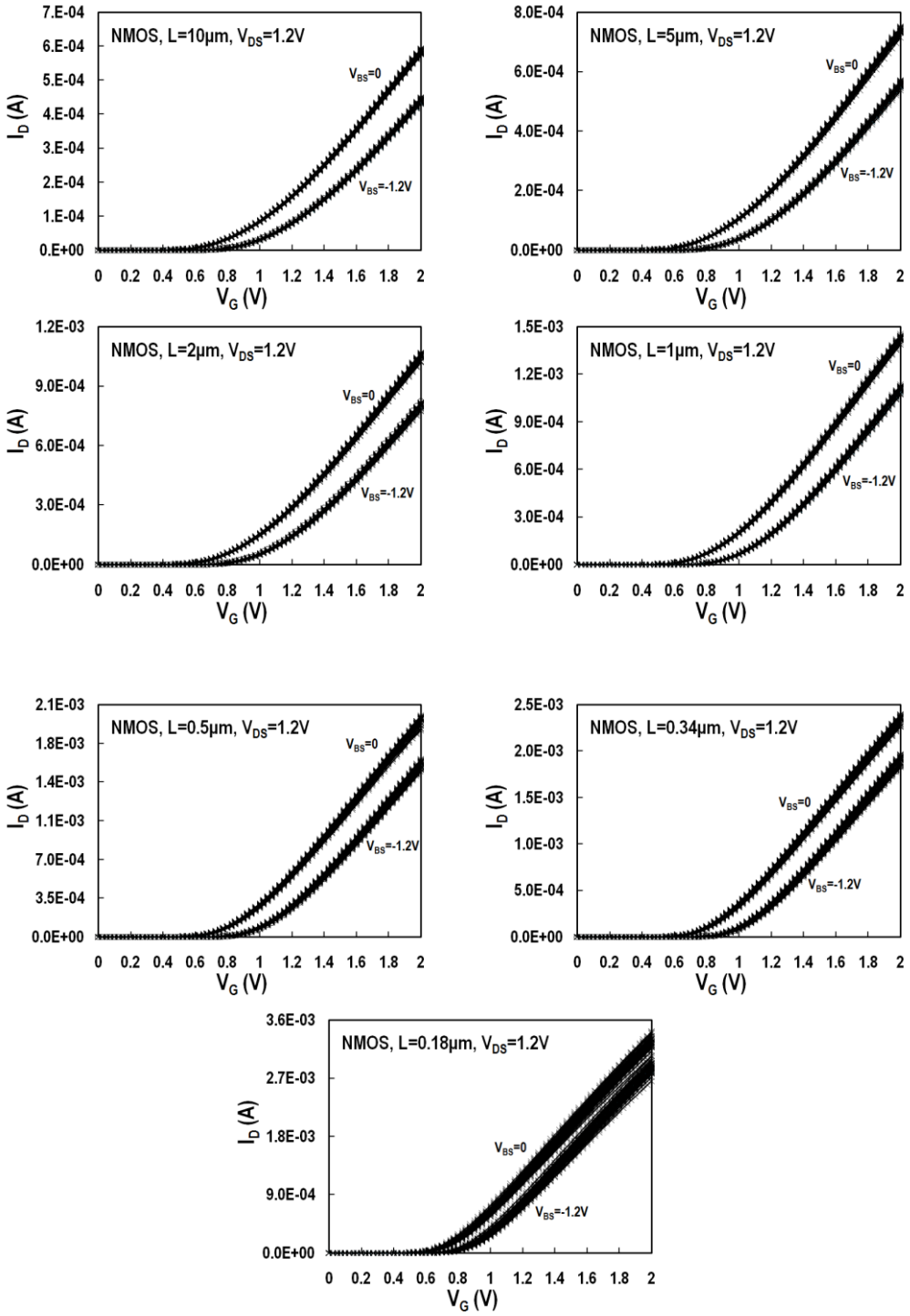

Figure 4. 19 I_D vs V_G graphs for V_{BS}=0, -1.2 V. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um)

In the figure above we see that I_D increases when we increase the gate Voltage (as expected). Also, I_D is higher for V_{BS} = 0V than it is for V_{BS} = -1.2V. This behavior is normal and similar to standard transistors.

Measurements – V_{DS}=1.2V (Log axis)

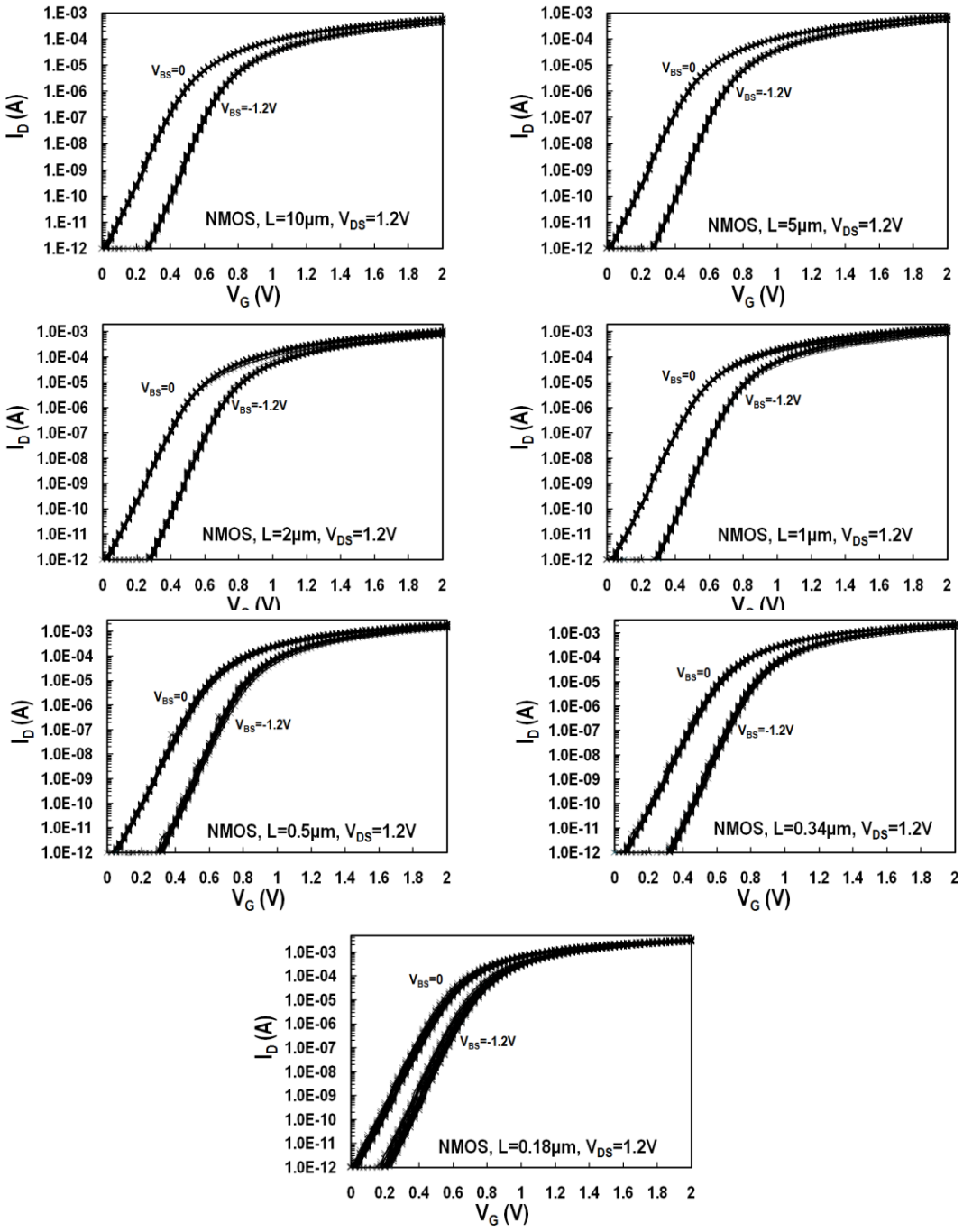

Figure 4. 20 I_D vs V_G graphs for V_{BS}=0, -1.2 V in a logarithmic axis. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um)

gm (V_{DS}=1.2V) – Mean Value

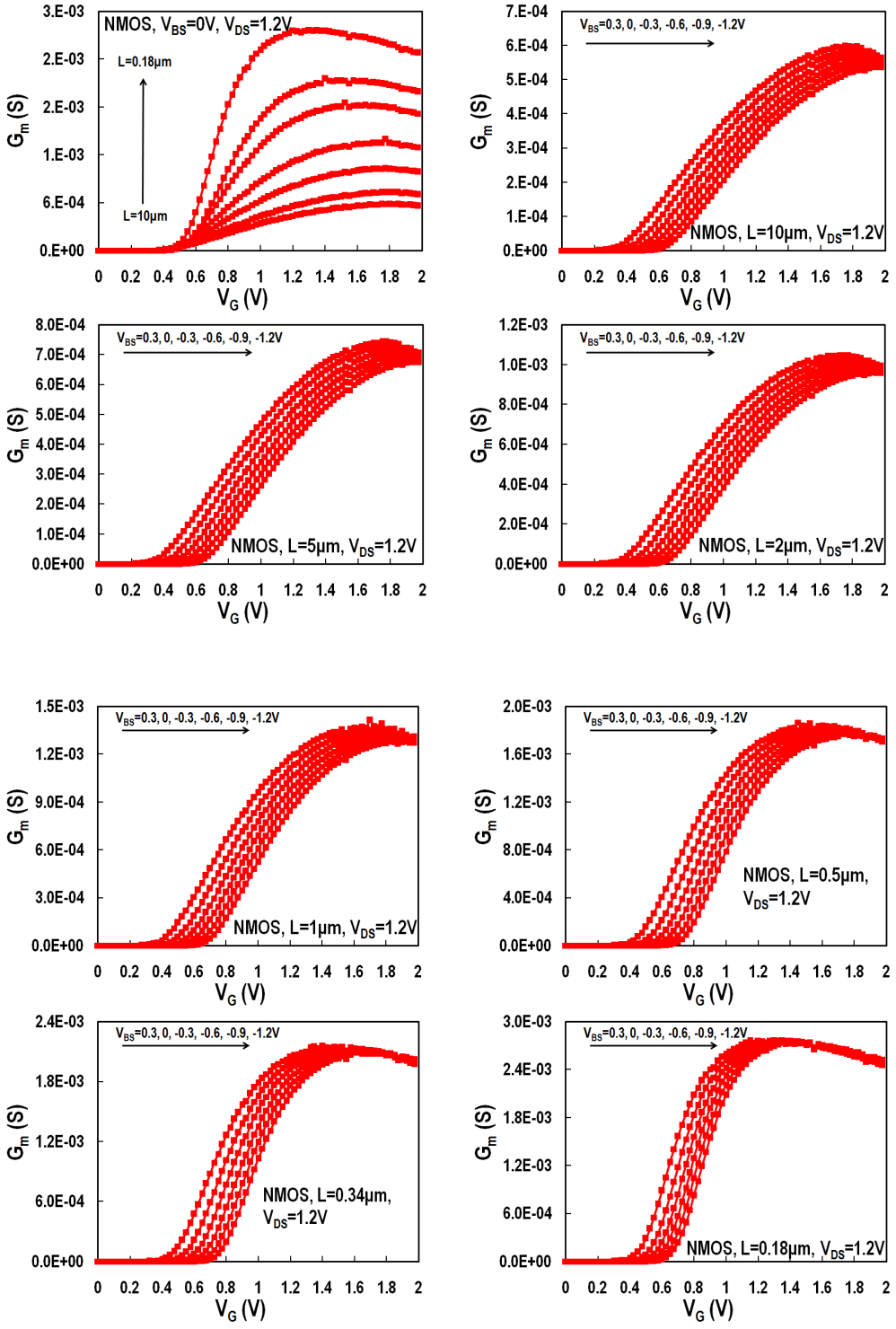

Figure 4. 21 G_m vs V_g graphs for V_{BS} =0.3, 0, -0.3, -0.6, -0.9, -1.2V are presented. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um) except for the top left graph which presents the result of all the different channel lengths when V_{BS} equals 0.

In the graphs above, we can clearly see that as the channel length gets smaller, the transconductance increases. Another observation is that G_m's peak increases with higher V_{BS}. This is the expected result which is similar to the result of the standard version of these transistors.

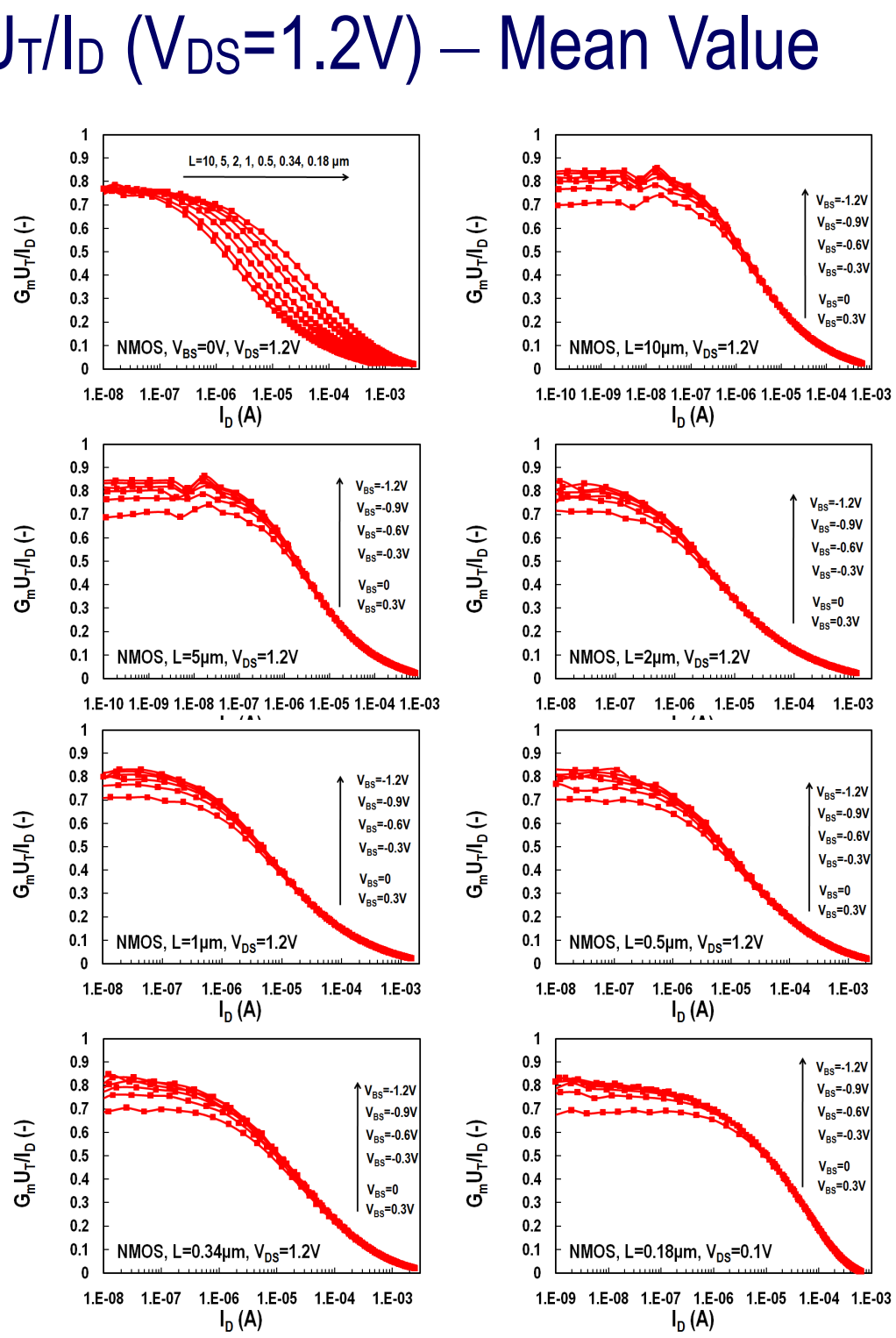

Figure 4. 22 The GmU_T/I_D graphs for V_{BS} =0.3, 0, -0.3, -0.6, -0.9, -1.2V are presented. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um) except for the top left graph which presents the result of all the different channel lengths when V_{BS} = 0.

The unitless quantity G_mU_T/I_D is higher for lower current I_D. It also appears to be higher for lower V_{BS}.

4.2.2 $(\Theta\sqrt{I_D})/(\Theta\sqrt{V_G})$

In this part of the thesis, the square root drain current to the square root gate voltage derivative will presented in graphs

$(\Theta\sqrt{I_D})/(\Theta\sqrt{V_G})$ (V_{DS}=1.2V) – Mean Value

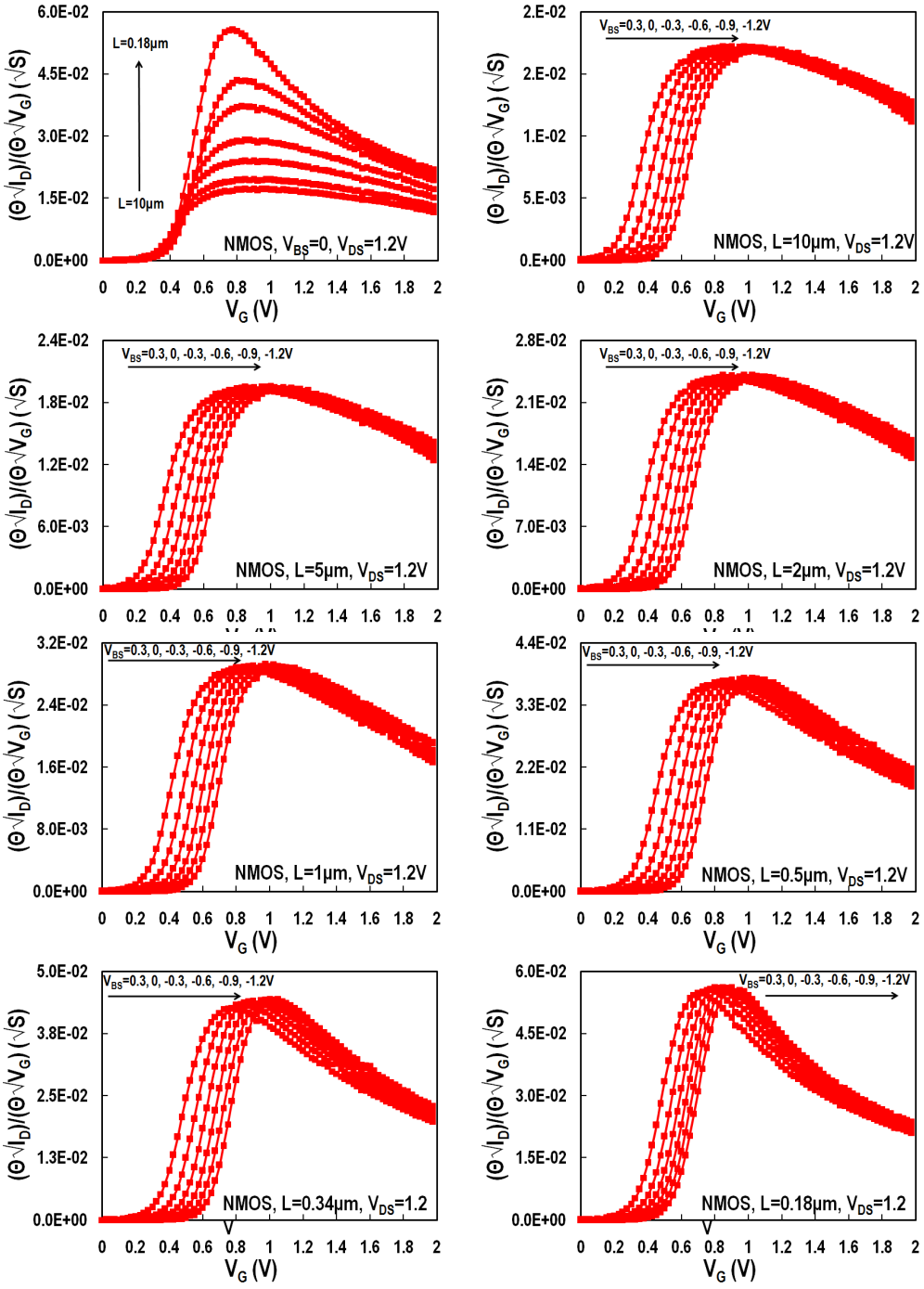

Figure 4. 23 (Θ√ID)/(Θ√VG) vs VG graphs for V_{BS} =0.3, 0, -0.3, -0.6, -0.9, -1.2V are presented. Each graph shows the results for different channel lengths (L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um) except for the top left graph which presents the result of all the different channel lengths for V_{BS} = 0.

4.2.3 Threshold Voltage

In this section the threshold voltage graphs will be presented. The mean value of the threshold voltage, the threshold voltage in specific cases and it's standard deviation will be the subject of this subchapter.

V_{TH} – Mean Value (V_{DS}=1.2V)

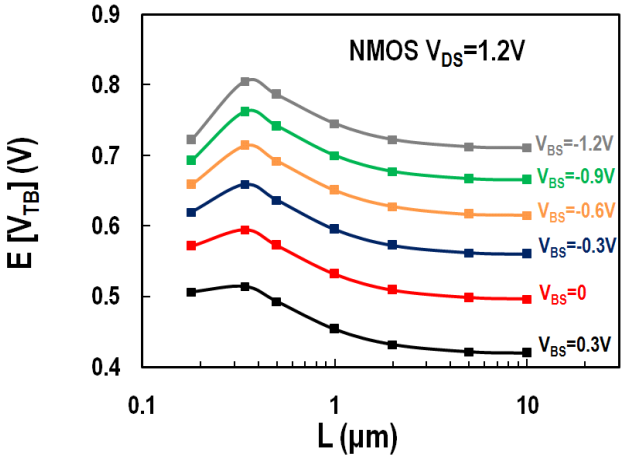

Figure 4. 24 The E[V_{TB}] vs L graph for V_{BS} =0.3, 0, -0.3, -0.6, -0.9, -1.2V is presented above.

The mean value of the threshold voltage (E[V_{TB}]) peaks for 340nm (the second lowest channel length) and then starts to drop while the channel lengths get bigger.

V_{TH} – (V_{DS}=1.2V)

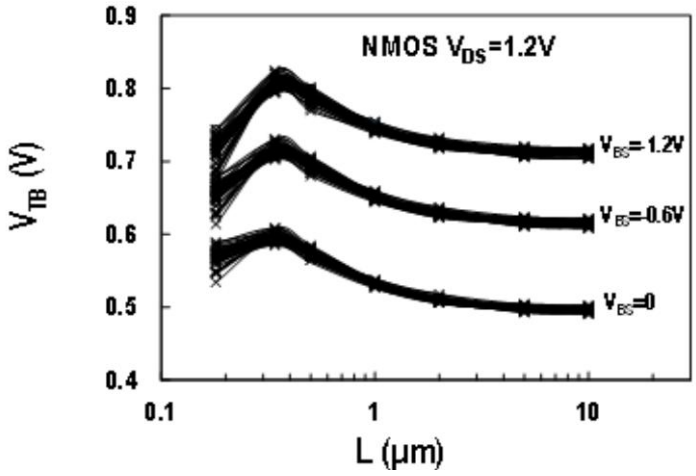

Figure 4. 25 V_{TB} vs L graph is presented. V_{DS} is 0.1 Volts and V_{BS}= -1.2, -0.6 and 0.

V_{TB} peaks for 340nm (the second lowest channel length) and then starts to drop while the channel lengths get bigger.

V_{TH} – Sigma (V_{DS}=1.2V)

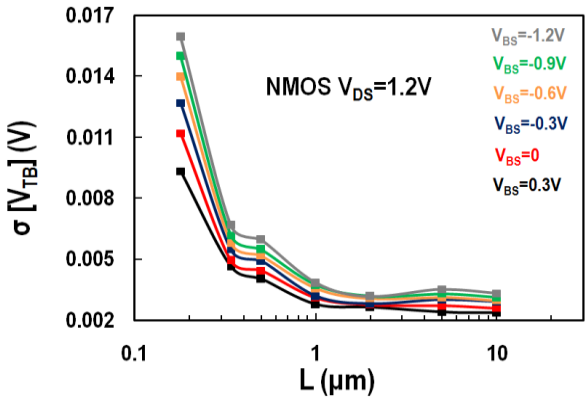

Figure 4. 26 σ[V_{TB}] vs L graph is presented for V_{BS} =0.3, 0, -0.3, -0.6, -0.9, -1.2V

The standard deviation of V_{TB} is significantly higher for 180nm. While the channel length gets bigger, the V_{TB} standard deviation decreases. Another conclusion made after examining the graph above, is that σ[V_{TB}] is lower for higher V_{BS}.

4.2.4 Threshold Voltage Matching

The Threshold Voltage will be our focus in this part of the thesis. Results from 48 pairs of NMOS transistors for each channel length, will be presented in the graphs below.

ΔV_{TH} – Matching (V_{DS}=1.2V)

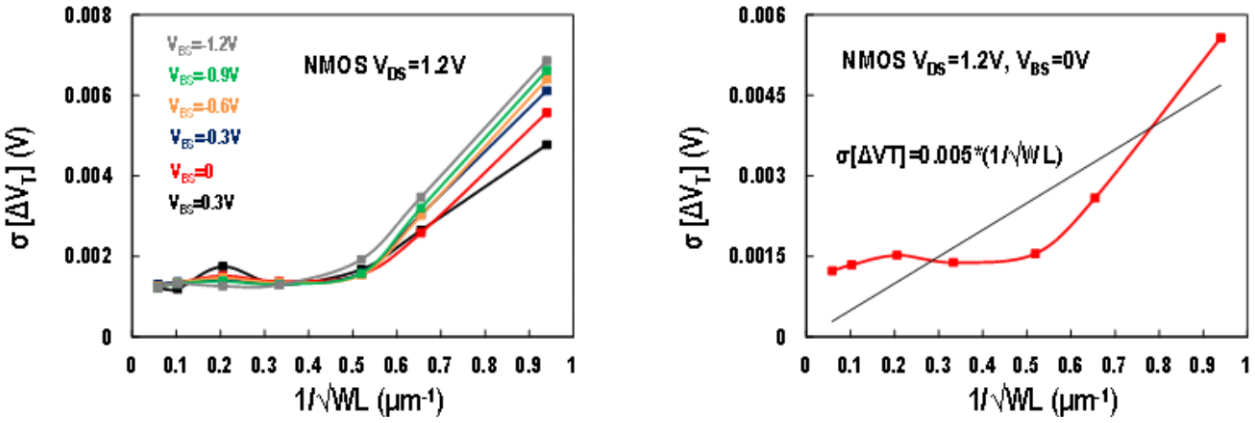

Figure 4. 27 The σ[ΔV_T] vs 1/$\sqrt{WL}$ graph for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V is presented in a). In b) we examine V_{BS} =0 exclusively.

Examining the figure above we can conclude that the matching get better for bigger 1/$\sqrt{WL}$. This makes sense because as the product of the width and the length decreases, the unitless quantity 1/ $\sqrt{WL}$ increases and for smaller dimensions where the distance between the different semiconductors is smaller, we expect increased deviation between the measurements.

4.2.5 Mobility

The mean value of the mobility for every channel length, the mobility for specific V_{BS} and it's standard deviation will be our focus in this subchapter. Representative graphs and their results will be presented below.

μ – Mean Value (V_{DS}=1.2V)

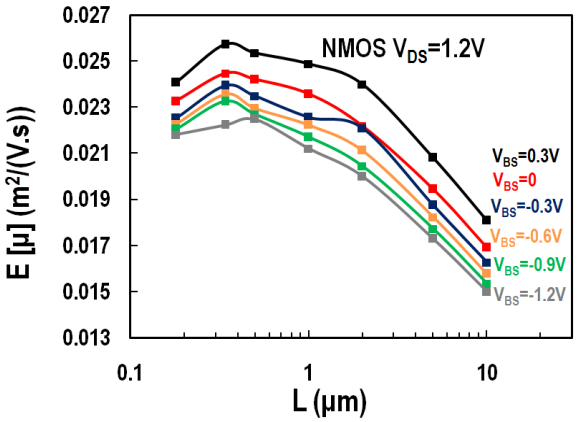

Figure 4. 28 E[μ] vs L graph for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V

The mean value of the mobility decreases for bigger channel length and lower V_{BS}. Furthermore, mobility becomes bigger for smaller channel length devices, following typical behavior.

μ – (V_{DS}=1.2V)

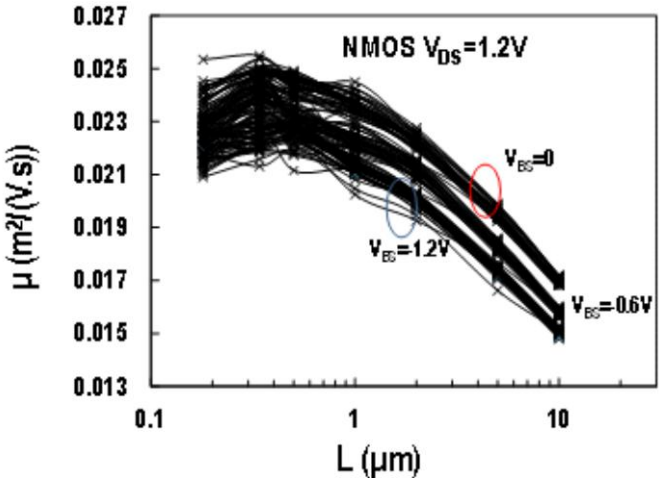

Figure 4. 29 μ vs L graph for V_{BS} = 0, -0.6, -1.2V

Mobility decreases for bigger channel length. It also decreases for lower V_{BS}. Furthermore, mobility becomes bigger for smaller channel length devices, following typical behavior.

μ – Sigma (V_{DS}=1.2V)

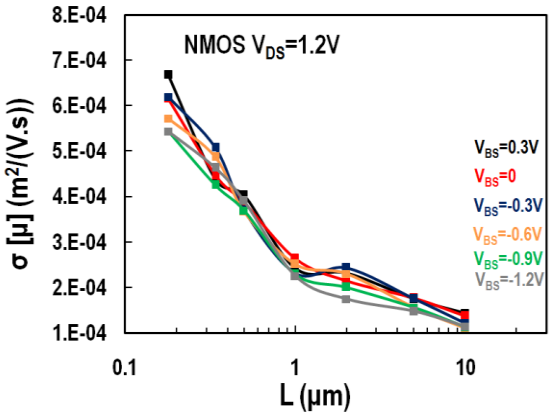

Figure 4. 30 σ[μ] vs L graph for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V

The standard deviation of μ, is higher for smaller channel lengths. This is something we expect since, as we already know, the electron mobility is inversely proportional to the channel length.

4.2.6 Mobility Matching

In this part of the thesis our focus will be on the matching of the mobility. Results of 48 pairs of NMOS transistors for each channel length, will be presented in the graphs below.

Δμ/μ – Matching (V_{DS}=1.2V)

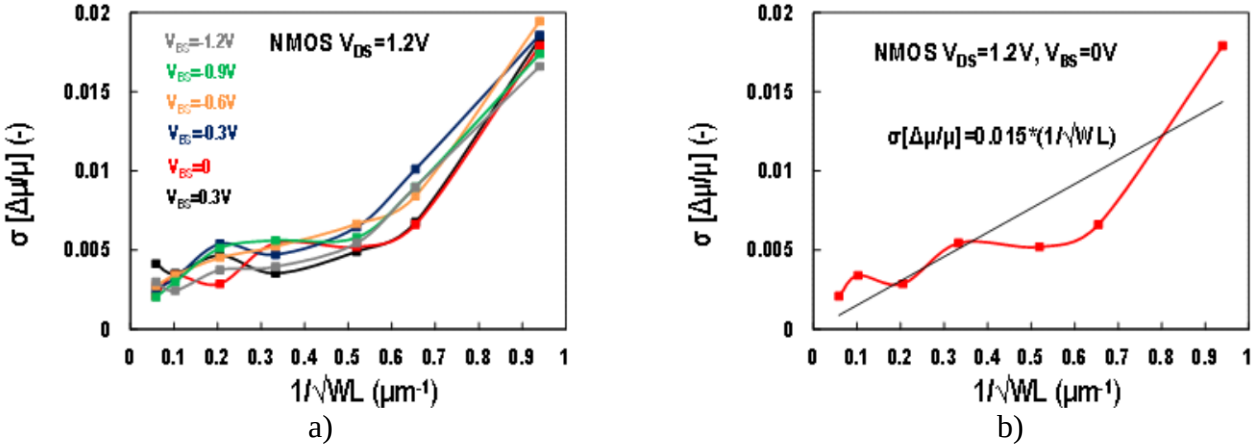

Figure 4. 31 a) σ[Δμ/μ] vs 1/ $\sqrt{WL}$ for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V. b) σ[Δμ/μ] vs 1/ $\sqrt{WL}$ for V_{BS} = 0V

In figure 4.31 we see that σ(Δμ/μ) increases with 1/ $\sqrt{WL}$ and is independent to V_{GB}, as expected and similar to the respective standard transistors.

4.2.7 Slope factor

In this part of the thesis we are going to focus on the slope factor and it's behavior for transistors with different channel length and for different base-source voltages in each of them.

n – Mean Value (V_{DS}=1.2V)

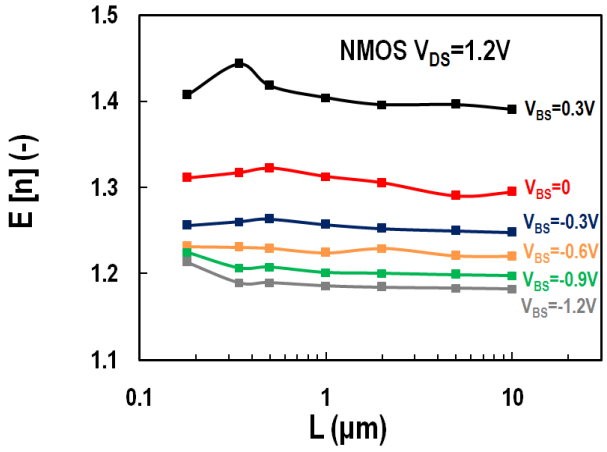

Figure 4. 32 E[n] vs L graph for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V

In the figure above we can examine the mean value of the slope factor. It increases with higher V_{BS}.

n (V_{DS}=1.2V)

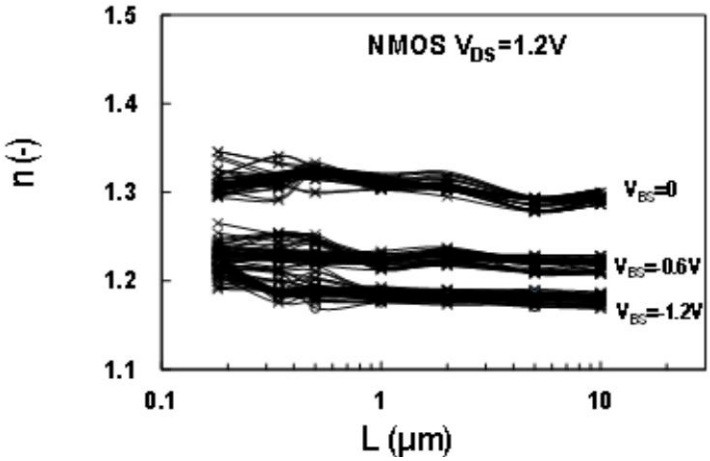

Figure 4. 33 n vs L graph for V_{BS} = 0, -0.6, -1.2V

Slope factor increases with higher V_{BS}. It can be noticed that slope factor increases at higher VBS. Furthermore, slope factor versus channel length is almost constant with a slight increment towards smaller channel lengths as expected.

n – Sigma (V_{DS}=1.2V)

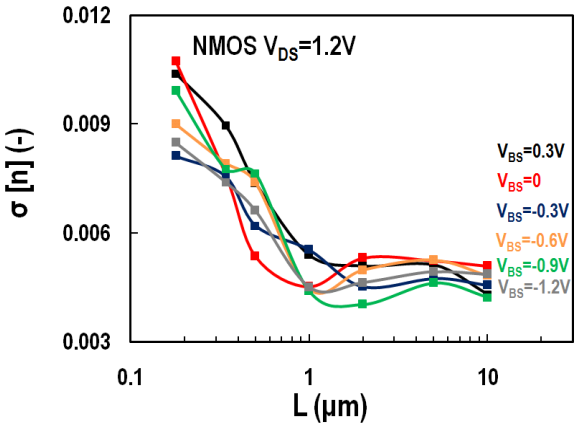

Figure 4. 34 σ vs L graph for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V

Standard deviation of n, increases with higher V_{BS}. Similar results are extracted from respective standard transistors.

Δn/n – Matching (V_{DS}=1.2V)

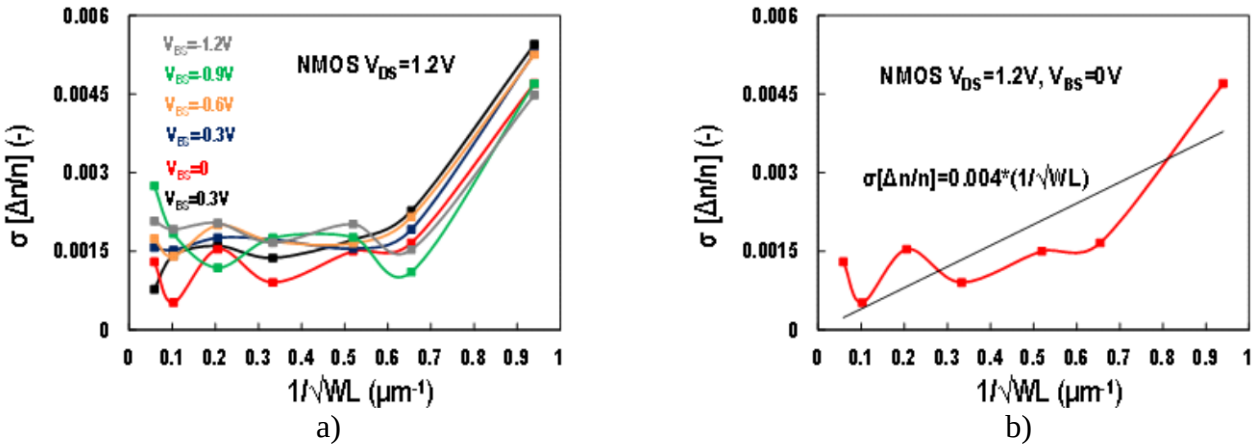

Figure 4. 35 a) σ[Δn/n] vs 1/$\sqrt{WL}$ for V_{BS} = 0.3, 0, -0.3, -0.6, -0.9, -1.2V. b) σ[Δn/n] vs 1/$\sqrt{WL}$ for V_{BS} = 0V

As we can see in the graphs above, σ[Δn/n] increases with $1/\sqrt{WL}$. This behavior of the graphs is normal.

σ(ΔI$_D$/I$_D$) – Matching (V$_{DS}$=1.2V)

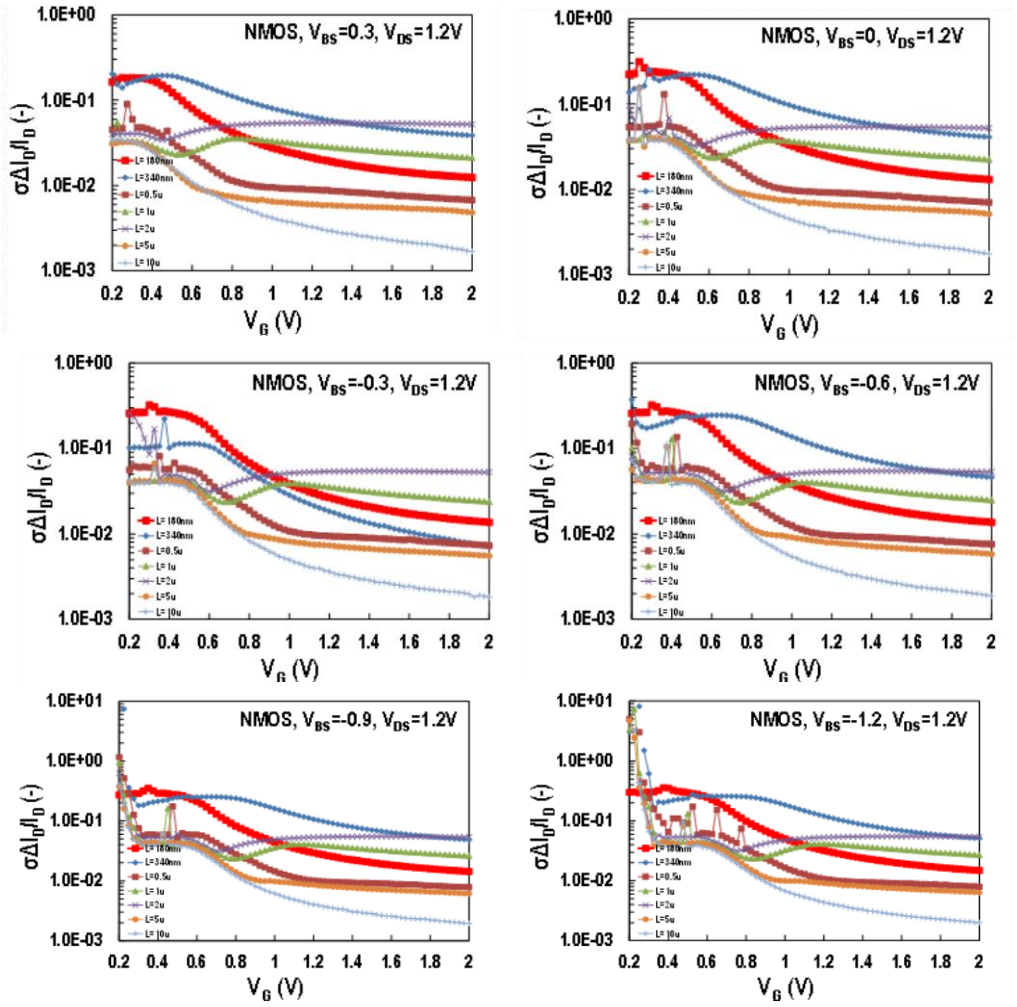

Figure 4. 36 σ(ΔI$_D$/I$_D$) vs V$_G$ graphs for L=10um, 5um, 2um, 1um 0.5um, 0.34um and 0.18um. Each graph shows the results for different V$_{BS}$ =0.3, 0, -0.3, -0.6, -0.9, -1.2V.

Drain current mismatch σ(ΔID/ID) decreases for bigger channel length L and becomes higher towards weak inversion. This is an expected behavior, since current mismatch is expected to follow the gm/ID behavior versus inversion coefficient.

5.Conclusions

5.1 Summary

This thesis offers interesting results of enclosed gate NMOS transistors. The range of the channel length (0.18μm, 0.34μm, 0.5μm, 1μm, 2μm, 5μm, 10μm), as well as the total numbers of the MOSFETs (672) measured gives as a valid picture of the operation of this type of MOSFETs. Results of all regions of inversion, for both linear and saturation region of operation were extracted.

EG MOSFETs present identical behavior with that of the standard layout MOSFET transistors as expected. Basic parameters, such as: weak inversion slope, threshold voltage, mobility, and mismatch, where extracted based on the typical extraction methods used in the ST layout MOSFETs. The statistical behavior of the extracted parameters follows that of the standard MOSFETs in all cases.

5.2 Future work

The results of the thesis give potential for future work: Comparison with PMOS transistors of the same type, comparison with standard MOSFETs and the respective channel length, studying of the result of each die separately and examining how the position of the die on the wafer affects the results (if it does), etc. The results can also be used to extract a model for this type of MOSFETs.

References

[1] Behzad Razavi, *Design of Analog Circuit Integrated Circuits.* Boston, McGraw-Hill 2001.

[2] Adel S. Sedra and Kenneth C.Smith, *Microelectronic Circuits*, Oxford 2009.

[3] David M. Binkley, Tradeoffs and Optimization in Analog CMOS Design. John Wiley 2008.

[4] A. Giraldo, A.Paccagnella, A. Minzoni, "Aspect ratio calculation in n-channel MOSFETs with a gate-enclosed layout", Solid State Electronics, vol. 44, p981-988, 2000.

[5] D. C. Mayer, R. C. Lacoe, E. E. King and V. Osborn, "Reliability Enhancement in High Performance MOSFETs by Annular Transistor Design", IEEE Transactions on Nuclear Science, vol. 51, no.6, 2006.

[6] Z. Jia, Y. Haigang, S. Jiabin, Y. Le and W. Yuanfeng, "Modeling of enclosed-gate layout transistors as ESD protection device based on conformal mapping method", Journal of semiconductors, vol. 35 no .18, 2014.

[7] L. D. Mei, W. Z. Hua, H. L. Ying and G. Qui-Jing, "Study of total ionizing dose radiation effects on enclosed gate transistors in a commercial CMOS technology", Chinese Physics, vol. 16, no. 12, 2007.

[8] Chin-Yuan Chan, Yu-Syuan Lin, Yen-Chun Huang, Shawn S.H. Hsu and Y.-Z. Juang, "Impact of STI Effect on Flicker Noise in 0.13-μm RF NMOSFETs", IEEE Transactions on Electron Devices, vol. 54, no. 12, 2007.

[9] R. V. Wang, Y. H. Lee, Y. L. Ryan Lu, W. McMahon, S. Hu and A. Ghetti, "Shallow Trench Isolation Edge Effect on Random Telegraph Signal Noise and Implications for Flash Memory", IEEE Transactions on Electron Devices, vol. 56, no. 9, 2009.

[10] S. K. Kwon, H. M. Kwon, W. L. Choi, H. S. Song, H. D. Lee, "Effects of Shallow trench isolation on low frequency noise characteristics of source-follower transistors in CMOS image sensors", Solid State Electronics, vol. 119, p29-32, 2016.

[11] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Florian, A.Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, W. Snoeys, "Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects", IEEE Transactions on Nuclear Science, vol. 46, no.6, 1999.

[12] wikipedia.org

[13] C. Galup-Montoro and M. C. Schneider, "MOSFET Modeling For Circuit Analysis And Design", World Scientific 2007

[14] M. J.M. Pelgrom, H. P. Tuinhout and M. Vertregt, "Transistor matching in analog CMOS applications" International Electron Devices Meeting, San Francisco CA USA, 1988

[15] P. G. Drennan, C. C. McAndrew, "Understanding MOSFET Mismatch for Analog Design", Proceeding of the IEEE 2002 Custom Integrated Circuits Conference, Orlando FL USA, 2002

[16] H.P. Hsu, Theory and Problems of Signals and Systems, McGraw-Hill 1995.